Investigation of p-GaN tri-Gate normally-Off GaN Power MOSHEMTs

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***Abstract*— In this work, we present the investigation of the combination of p-GaN gate and tri-gate structures to achieve normally-off operation on GaN-on-Si MOSFETs. We have developed and optimized a selective and low-damage p-GaN etching recipe to stop at the AlGaN barrier and minimize the degradation in on-resistance (R_{ON}). The p-GaN length and tri-gate filling factor (*FF*) were optimized to achieve a good trade-off between high threshold voltage (V_{TH}) and low R_{ON}. The excellent channel control capability offered by tri-gate structure led to a reduced OFF-state leakage current (I_{OFF}), higher ON/OFF ratio, smaller sub-threshold slope (*SS*) compared to similar planar p-GaN devices. These results unveil the excellent prospects of p-GaN tri-gate technology for future power electronics applications.**

***Keywords*— Gallium Nitride, p-GaN gate, normally-off, MOSFET, tri-gate, recess, high breakdown, low leakage**

I. Introduction

GaN MOSHEMTs offer a huge potential for future high-frequency power applications with low On-resistance, low switching losses and high blocking voltages [1], [2]. Normally-off is a necessary requirement to guarantee a safe operation and a simple gate driving configuration for power electronics applications [3]. It is currently challenging to demonstrate concurrently a sufficiently positive threshold voltage (V_{TH}) with low on resistance (R_{ON}), along with high breakdown voltage (V_{BR}) to achieve a high performance and reliable normally-off operation [4]–[6].

To achieve normally-off operation, techniques such as p-GaN gate [7], fluorine-based plasma treatment [8], [9], and recessing the barrier [10]–[13] under the gate region were reported. One of the most promising method for normally-off operation nowadays is based on p-GaN gates, in which the conduction band of the AlGaN/AlN/GaN at the channel is lifted up by using a p-GaN gate, depleting the 2DEG under the gate. This results in positive V_{TH}, but however degrades the R_{ON}. Reducing the p-GaN gate length can improve R_{ON} at the cost of a negative shift of V_{TH}. Tri-gate structures have shown significant potential for power electronic devices with an improved gate control [14]–[16] and larger V_{BR} compared to planar devices, without degrading R_{ON} [17]–[19]. In addition, a significant positive shift of V_{TH} can be achieved by simply reducing the width of tri-gate structures. Nonetheless, a positive V_{TH} relying solely on tri-gates can be achieved by very narrow tri-gates (down to 15 nm-wide) [20].

This work was supported in part by the ECSEL Joint Undertaking (JU) under grant agreement No 826392.The JU receives support from the European Union's Horizon 2020 research and innovation programme and Austria, Belgium, Germany, Italy, Norway, Slovakia, Spain, Sweden, Switzerland.

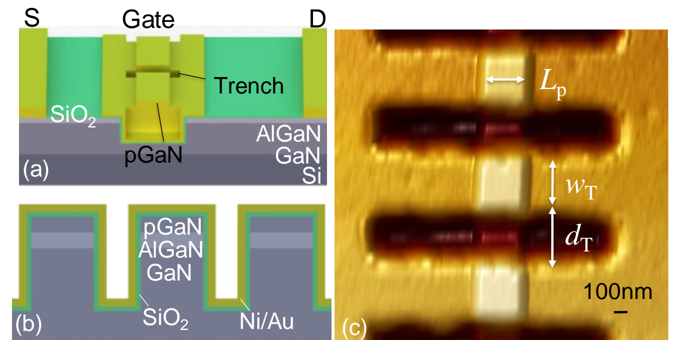

Fig. 1. (a) 3D Schematic of fabricated p-GaN tri-gate MOSHEMTs and (b) cross-sectional views of p-GaN tri-gate region. (c) Top-view AFM image of p-GaN on top of tri-gate nanowire.

In this work, we address these challenges by combining short p-GaN gates with tri-gate structures, which resulted in high V_{TH} and low R_{ON} simultaneously, and presented excellent normally-off performance. The structure is based on tiny portion of p-GaN on top of the tri-gate fins to locally lift the conduction band together with the tri-gate sidewalls, to yield a positive $V_{TH.}$ This combination maintains a relatively low R_{ON} by significantly reducing the p-GaN length. The devices presented V_{TH} of 1.78 V (0.9 V at 1μA/mm) and high I_D^{max} of 520 mA/mm.

II. Device Structure and Fabrication

Fig.1 illustrates the 3D (Fig. 1(a)) and, cross-sectional schematics (Fig. 1(b) of the fabricated p-GaN tri-gate GaN MOSFETs based on commercial p-GaN/AlGaN/GaN-on-Si wafers. The device fabrication started with mesa and tri-gate regions defined by e-beam lithography, and followed by Cl_2-based ICP etch. The major challenge for p-GaN gated HEMTs is to obtain uniform p-GaN etching of non-gated active regions and to minimize etching plasma damage [3], [7], [21]. A 200 nm-wide p-GaN (Fig. 1 (c)) was protected with e-beam lithography resist, followed by a 75 nm-deep low-damage slow-etch-rate $Cl_2/O_2/Ar$-based selective ICP etch. The slow-rate selective etching combined with O_2 plasma/ HCl treatment is a critical process for smothering the etched surface, which minimizes the surface damage and results in low R_{ON}. As we can see from Fig. 2 (a), the etch of 75 nm p-GaN took around

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58 s while the etch of 20 nm $Al_{0.25}Ga_{0.75}N$ took 542 s, which resulted in a very high selectivity of ~35:1 between p-GaN and $Al_{0.25}Ga_{0.75}N$. The etched surface was then treated with O_2 plasma/HCl, followed by surface annealing under 500 °C to further smoothen the surface and recover the dry etching damages. The surface morphology comparison of etched surface by traditional and selective recipe is shown in Fig. 3 (b-c). A metal stack composed of Ti /Al/Ti/Ni/Au was deposited in both source and drain regions, followed by rapid thermal annealing (RTA) at 780°C under N_2 atmosphere. The 25 nm-thick SiO_2 gate dielectric was deposited by atomic layer deposition (ALD) at 300°C, immediately after a surface treatment in 37% HCl for 1 min and 500°C bake for 5 min. Finally, gate metal was formed by 50 nm Ni/ 150 nm Au.

III. Results and Discussion

The SEM picture of fabricated p-GaN-gated transistor is shown in Fig. 3(a) and the comparison of the DC transfer characteristics of planar and p-GaN-gated planar devices is shown in Fig. 3(b) and (c). A shift of V_{TH} was observed from –2.6 V for the planar devices, to -0.1 V for the 150 nm-long p-GaN-gated planar devices and +1.3 V for the 1.5 µm-long p-GaN planar device (V_{TH} was defined at 1 µA/mm) (Fig. 3(b-c)). As the V_{TH} shifted more positively with the increase of the p-GaN length, the current density was reduced dramatically from ~400 mA/mm (planar MOSHEMT), ~300 mA/mm (150 nm-long p-GaN gate) to ~150 mA/mm (1.5 µm-long p-GaN gate). However, while reducing the p-GaN length diminishes the current degradation, the V_{TH} is not positive enough to ensure the safe operation of GaN transistor.

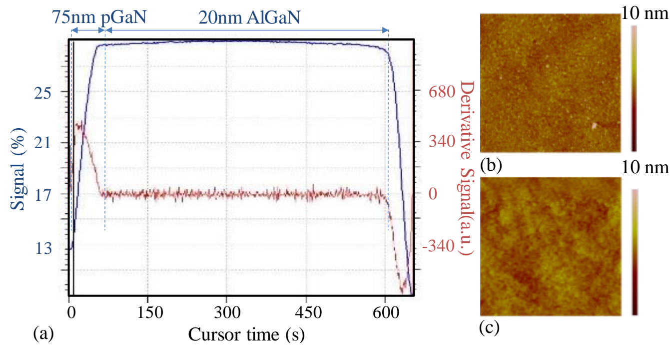

Fig. 2. (a) Laser detector of ICP etching. The surface morphology after (b) traditional ICP etching and (c) the selective ICP etching.

In this work, we have combined a short p-GaN gate with tri gate structures (Fig.1), which achieves high V_{TH} and low R_{ON} simultaneously. We have optimized the tri-gate geometry (Fig. 4) in the gate region (p-GaN gate length and *FF* of tri-gate) to obtain the optimum R_{ON} and V_{TH} simultaneously. As we can see from Fig. 4 (a), the p-GaN length did not have a strong effect on V_{TH} for p-GaN lengths over 200 nm, however, the current density dropped significantly with the increase of p-GaN length. Thus, reducing the p-GaN length is favorable, with length larger than 100nm (since this device exhibited low V_{TH} of 0.3 V). Moreover, the tri-gate filling factor (*FF*) ($w_T/(w_T+d_T)$, in which the w_T is the width of nanowires and d_T is the trench spacing) had relatively strong effect on V_{TH} and barely degraded the current density (Fig. 4(b)). We have compared the dependence of V_{TH} and R_{ON} on p-GaN gate length for p-GaN planar and p-GaN tri-gate devices (Fig. 4(c)). For p-GaN planar devices, the V_{TH} has shifted from -0.3 V to 0.4V with p-GaN length varying from 100 nm to 600nm, while for the p-GaN tri-gate devices has changed from 0.3 V to 0.9 V. The slope of V_{TH} versus p-GaN length is much smaller for p-GaN tri-gate devices compared with p-GaN planar devices, since the tri-gate structure also contributes to the V_{TH} shift.

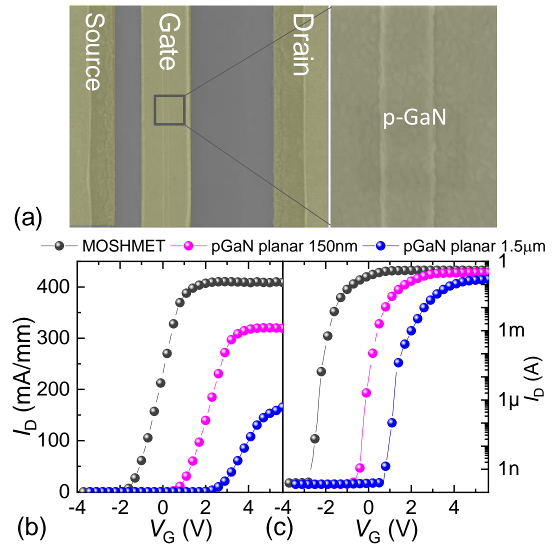

Fig. 3. (a) Top view of planar p-GaN transistors. Transfer characteristics of MOSHEMT and p-GaN planar MOSHEMT in (b) Linear and (c) logarithmic scale for $V_{DS} = 5$ V.

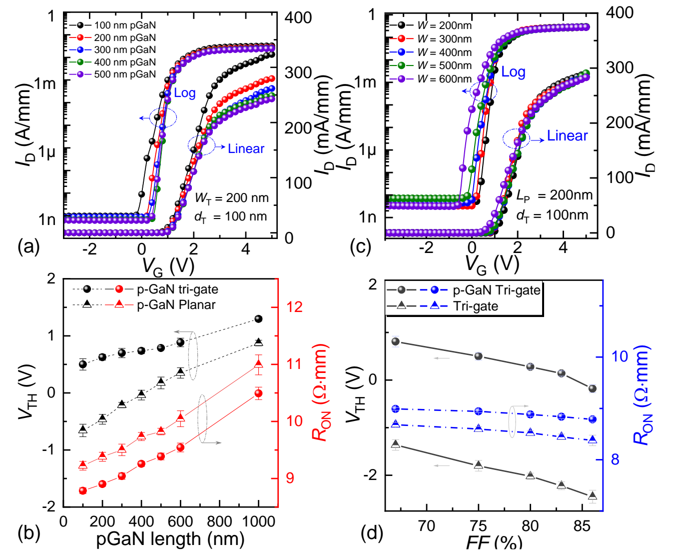

Fig. 4. (a) The Log and linear transfer characteristics at $V_{DS} = 5$ V of normally-off p-GaN tri-gate with different (a) p-GaN length and (b) Filling factor (*FF*) of Tri-gate (w_T/w_T+d_T). The L_{GS}, L_G and L_{GD} were 1.5, 2 and 15 µm, respectively. Standard deviation bars were determined from the measurement of 6 devices of each type, revealing their consistent performance. (c) The p-GaN length – V_{TH} and R_{ON} dependence of p-GaN planar and p-GaN tri-gate devices. (d) *FF* – V_{TH} and R_{ON} dependence of Tri-gate (Normally-on) and p-GaN tri-gate (Normally-off) transistors (The p-GaN length is fixed at 200nm).

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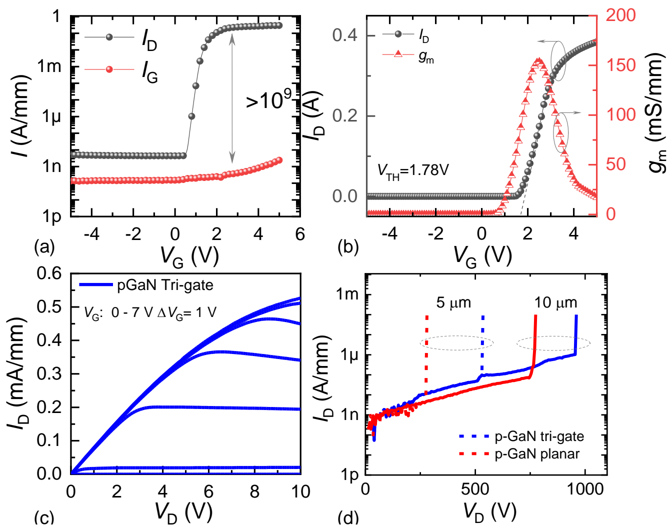

Fig. 5. (a) Device transfer characteristic in log scale and (b) linear scale, and the corresponding gate leakage and transconductance (g_m) for V_{DS}=5 V. V_{TH} is 0.85 V defined at 1 μA/mm, which would be 1.72 V from linear extrapolation. (c) Output characteristics with V_G ranging from 0 V to 7 V with ΔV_G=1 V. (d) Breakdown characteristics of p-GaN planar and p-GaN tri-gate devices were measured for L_{GD} of 5μm and 10 μm.

However, the V_{TH} difference between these two kinds of devices becomes very small with large p-GaN length (above 1 μm). The R_{ON} of these two devices is almost linearly dependent on the p-GaN length. We have also compared V_{TH} and R_{ON} dependence on tri-gate *FF* for Tri-gate (Normally-on) and p-GaN tri-gate (Normally-off) transistors (Fig. 4 (d)). The d_T is fixed at 100nm and the w_T was varied from 200nm to 600nm, which corresponded to *FF* varying from 0.66 to 0.87. The p-GaN length is fixed at 200nm. As the *FF* increase, the V_{TH} dropped from 0.9 V to -0.2 V for the p-GaN tri-gate devices, in contrast, the V_{TH} of tri-gate-only devices shifted from -1.3 V to -2.8 V (Fig. 4 (d)). When *FF* varied from 0.66 to 0.87, the R_{ON} of p-GaN tri-gate has almost remained constant with reduction of 0.2 Ω·mm, while the reduction of tri-gate R_{ON} was slightly higher up to 0.4 Ω·mm. In summary, the p-GaN length and tri-gate *FF* can be tuned to obtain an optimum balance between V_{TH} and R_{ON}.

The transfer and output characteristic of p-GaN tri-gate transistor with p-GaN gate length (L_P) = 200 nm and *FF* = 0.66 is shown in Fig. 5(a-c), presenting V_{TH} of 0.94 V (at I_{DS} = 1 μA/mm), and 1.78 V from the linear extrapolation. Thanks to the tri-gate structure and small gate oxide leakage, the gate control is excellent with ON/OFF ratio > 10^9, subthreshold slope (*SS*) of 98 mV/dec, large transconductance peak of 160 mS/mm and small gate leakage of less than 1 nA/mm. The output characteristic is shown in Fig. 5(c), presenting large I_D^{max} of 525 ± 12 mA/mm at V_G = 7 V and low R_{ON} of 9.2 Ω·mm with L_{GD} of 15 μm. The comparison of breakdown characteristics between the p-GaN planar and p-GaN tri-gate is shown in Fig. 5(d). The V_{BR} of p-GaN tri-gate was extracted for V_G of 0 V with grounded substrate at 1 μA/mm (Fig.5 (d)), resulting in 520 V and 980 V for L_{GD} of 5 μm and 10 μm, respectively, compared to 380 V and 750V, for p-GaN planar devices. The p-GaN tri-gate devices showed higher breakdown voltage with lower L_{GD} due to the integrated tri-gate field plate [22]. The p-GaN tri-gate devices also presented lower R_{ON} with the same L_{GD}, revealing an extraordinary prospect of this technology for future power electronics applications.

IV. Conclusion

In this work, we present the investigation of the combination of short p-GaN gate and tri-gate structures to achieve normally-off and low R_{ON} in GaN-on-Si MOSFETs. P-GaN tri-gate devices presented V_{TH} of 0.9 V at 1μA/mm, low R_{ON} of 9.2 Ω·mm and high V_{BR} of 960 V (L_{GD} of 10 μm) with grounded substrate. The results show the extraordinary prospects of p-GaN tri-gate devices for future power electronics applications.

Acknowledgment

We would like to thank the staff in CMi and ICMP cleanrooms at EPFL for technical support and advice.

References

[1] M. Tao *et al.*, "Characterization of 880 V Normally Off GaN MOSHEMT on Silicon Substrate Fabricated With a Plasma-Free, Self-Terminated Gate Recess Process," *IEEE Trans. Electron Devices*, vol. 65, no. 4, pp. 1453–1457, Apr. 2018, doi: 10.1109/TED.2018.2808345.

[2] P. Fiorenza, G. Greco, F. Iucolano, A. Patti, and F. Roccaforte, "Channel Mobility in GaN Hybrid MOS-HEMT Using SiO2as Gate Insulator," *IEEE Trans. Electron Devices*, vol. 64, no. 7, pp. 2893–2899, Jul. 2017, doi: 10.1109/TED.2017.2699786.

[3] G. Greco, F. Iucolano, and F. Roccaforte, "Review of technology for normally-off HEMTs with p-GaN gate," *Mater. Sci. Semicond. Process.*, Oct. 2017, doi: 10.1016/j.mssp.2017.09.027.

[4] J. Wei *et al.*, "Low On-Resistance Normally-Off GaN Double-Channel Metal–Oxide–Semiconductor High-Electron-Mobility Transistor," *IEEE Electron Device Lett.*, vol. 36, no. 12, pp. 1287–1290, Dec. 2015, doi: 10.1109/LED.2015.2489228.

[5] L. Zhang *et al.*, "AlGaN-Channel Gate Injection Transistor on Silicon Substrate With Adjustable 4–7-V Threshold Voltage and 1.3-kV Breakdown Voltage," *IEEE Electron Device Lett.*, vol. 39, no. 7, pp. 1026–1029, Jul. 2018, doi: 10.1109/LED.2018.2838542.

[6] J. Zhang *et al.*, "High-mobility normally-off Al2O3/AlGaN/GaN MISFET with damage-free recessed-gate structure," *IEEE Electron Device Lett.*, pp. 1–1, 2018, doi: 10.1109/LED.2018.2872637.

[7] Y. Zhou *et al.*, "p-GaN Gate Enhancement-Mode HEMT Through a High Tolerance Self-Terminated Etching Process," *IEEE J. Electron Devices Soc.*, vol. 5, no. 5, pp. 340–346, Sep. 2017, doi: 10.1109/JEDS.2017.2725320.

[8] Y. Zhang, M. Sun, S. J. Joglekar, and T. Palacios, "High threshold voltage in GaN MOS-HEMTs modulated by fluorine plasma and gate oxide," in *71st Device Research Conference*, 2013, pp. 141–142, doi: 10.1109/DRC.2013.6633833.

[9] L. Yang *et al.*, "High-Performance Enhancement-mode AlGaN/GaN high electron mobility transistors combined with TiN-based Source Contact Ledge and Two-Step Fluorine Treatment," *IEEE Electron Device Lett.*, pp. 1–1, 2018, doi: 10.1109/LED.2018.2864135.

[10] Z. Xu *et al.*, "Fabrication of Normally Off AlGaN/GaN MOSFET Using a Self-Terminating Gate Recess Etching Technique," *IEEE Electron Device Lett.*, vol. 34, no. 7, pp. 855–857, Jul. 2013, doi: 10.1109/LED.2013.2264494.

[11] M. Hua *et al.*, "Integration of LPCVD-SiNx gate dielectric with recessed-gate E-mode GaN MIS-FETs: Toward high

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performance, high stability and long TDDB lifetime," in *2016 IEEE International Electron Devices Meeting (IEDM)*, 2016, pp. 10.4.1-10.4.4, doi: 10.1109/IEDM.2016.7838388.

[12] W. B. Lanford, T. Tanaka, Y. Otoki, and I. Adesida, "Recessed-gate enhancement-mode GaN HEMT with high threshold voltage," *Electron. Lett.*, vol. 41, no. 7, pp. 449–450, Mar. 2005, doi: 10.1049/el:20050161.

[13] J. He, M. Hua, Z. Zhang, and K. J. Chen, "Performance andVTHStability in E-Mode GaN Fully Recessed MIS-FETs and Partially Recessed MIS-HEMTs With LPCVD-SiNx/PECVD-SiNxGate Dielectric Stack," *IEEE Trans. Electron Devices*, vol. 65, no. 8, pp. 3185–3191, Aug. 2018, doi: 10.1109/TED.2018.2850042.

[14] B. Lu, E. Matioli, and T. Palacios, "Tri-Gate Normally-Off GaN Power MISFET," *IEEE Electron Device Lett.*, vol. 33, no. 3, pp. 360–362, Mar. 2012, doi: 10.1109/LED.2011.2179971.

[15] S. Liu *et al.*, "Enhancement-Mode Operation of Nanochannel Array (NCA) AlGaN/GaN HEMTs," *IEEE Electron Device Lett.*, vol. 33, no. 3, pp. 354–356, Mar. 2012, doi: 10.1109/LED.2011.2179003.

[16] J. Ma and E. Matioli, "High Performance Tri-Gate GaN Power MOSHEMTs on Silicon Substrate," *IEEE Electron Device Lett.*, vol. 38, no. 3, pp. 367–370, Mar. 2017, doi: 10.1109/LED.2017.2661755.

[17] J. Ma and E. Matioli, "Slanted Tri-Gates for High-Voltage GaN Power Devices," *IEEE Electron Device Lett.*, vol. 38, no. 9, pp. 1305–1308, Sep. 2017, doi: 10.1109/LED.2017.2731799.

[18] J. Ma, M. Zhu, and E. Matioli, "900 V Reverse-Blocking GaN-on-Si MOSHEMTs With a Hybrid Tri-Anode Schottky Drain," *IEEE Electron Device Lett.*, vol. 38, no. 12, pp. 1704–1707, Dec. 2017, doi: 10.1109/LED.2017.2761911.

[19] J. Ma and E. Matioli, "2 kV slanted tri-gate GaN-on-Si Schottky barrier diodes with ultra-low leakage current," *Appl. Phys. Lett.*, vol. 112, no. 5, p. 052101, Jan. 2018, doi: 10.1063/1.5012866.

[20] L. Nela, M. Zhu, J. Ma, and E. Matioli, "High-Performance Nanowire-Based E-Mode Power GaN MOSHEMTs With Large Work-Function Gate Metal," *IEEE Electron Device Lett.*, vol. 40, no. 3, pp. 439–442, Mar. 2019, doi: 10.1109/LED.2019.2896359.

[21] Y. Zhong *et al.*, "Self-terminated etching of GaN with a high selectivity over AlGaN under inductively coupled Cl2/N2/O2 plasma with a low-energy ion bombardment," *Appl. Surf. Sci.*, vol. 420, pp. 817–824, Oct. 2017, doi: 10.1016/j.apsusc.2017.05.185.

[22] J. Ma, D. C. Zanuz, and E. Matioli, "Field Plate Design for Low Leakage Current in Lateral GaN Power Schottky Diodes: Role of the Pinch-off Voltage," *IEEE Electron Device Lett.*, vol. 38, no. 9, pp. 1298–1301, Sep. 2017, doi: 10.1109/LED.2017.2734644.

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