Proceedings of the 32th International Symposium on Power Semiconductor Devices & ICs
May 17-21, 2020, Vienna, Austria

High-Frequency GaN-on-Si power integrated circuits based on Tri-Anode SBDs

Luca Nela, Georgios Kampitsis, Halil Kerim Yildirim, Remco Van Erp, Jun Ma, and Elison Matioli
Power and Wide-band-gap Electronics Research Laboratory (POWERLAB),
École Polytechnique Fédéral de Lausanne (EPFL), Lausanne, Switzerland, luca.nela@epfl.ch

***Abstract*—In this work, we report on the switching performance of AlGaN/GaN lateral Tri-Anode SBDs. The Tri-Anode architecture leads to a more than 50% reduction in the device charge with respect to conventional planar structure, confirmed both by capacitive and reverse-recovery measurements, which results in a much improved $R_{ON}{\cdot}Q_{rr}$ figure-of-merit. The Tri-Anode excellent switching performance, combined with the superior DC behavior, makes these devices very promising for future ultra-fast and high-power applications. The diode performance was demonstrated by realizing a monolithically-integrated Diode Bridge Rectifier able to operate at high frequency and achieve AC to DC conversion. These results reveal the outstanding potential of GaN Tri-Anode SBD for ultra-fast, large power-density and high-efficiency future power integrated circuits.**

Keywords—GaN diode, Tri-Anode, reverse recovery, Power ICs, Diode Bridge Rectifier

I. Introduction

Lateral GaN-on-Si devices are promising candidates for ultra-fast, high power density and high-efficiency future power electronics [1]–[3]. Moreover, thanks to their lateral geometry, several devices can be monolithically integrated on the same chip to realize power integrated circuits (ICs). This enables high-frequency operation, thanks to the reduced parasitic components, reduction of the manufacturing cost and significant power density increase. Recently, a significant effort has been put in the development of High-Electron-Mobility Transistors (HEMT) with integrated driving circuit, leading today to several commercially available solutions [4], [5]. Another important step toward the realization of power ICs consists in the integration of high-voltage GaN diodes, which would significantly expand the design possibilities and topologies. While typical Schottky Barrier Diodes (SBDs) are not suited for high-voltage applications due to the high leakage through the Schottky barrier, lately novel architectures such as recessed anodes [6]–[9], double field plates [10], [11] and Tri-Gate/Tri-Anode hybrid structures [12]–[15] have enabled to effectively overcome this limitation, resulting in an improvement of SBDs R_{ON} vs V_{BR} figure-of-merit. In particular, Tri-Anode GaN SBDs, in which the diode anode

This work was supported in part by the Swiss National Science Foundation under Assistant Professor (AP) Energy Grant PYAPP2_166901, in part by the Swiss Office of Energy Grant No. SI501568-01 and in part by the European Research Council under the European Union's H2020 Program/ERC Grant Agreement 679425. The authors are with the Power and Wide-band-gap Electronics Research Laboratory (POWERLAB), École Polytechnique Fédérale de Lausanne (EPFL), CH-1015 Lausanne, Switzerland (e-mail: luca.nela@epfl.ch; elison.matioli@epfl.ch).

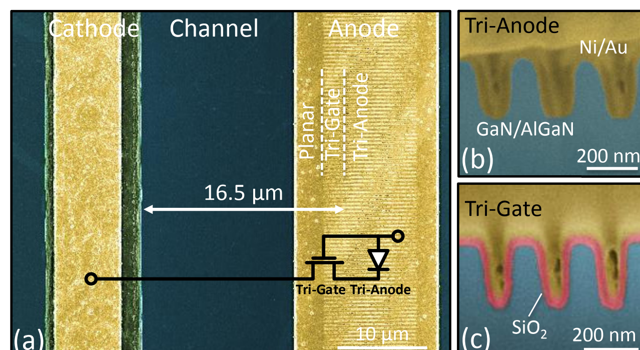

Fig.1. (a) SEM image of a finger of the scaled up Tri-Anode SBD. The Anode contact is nanostructured into a Tri-Gate and Tri-Anode region. (b-c) Focused Ion Beam (FIB) cross-section of the Tri-Gate and Tri-Anode structure.

region is nanostructured into fins, have demonstrated superb DC performance with large breakdown voltage (V_{BR}) up to 2 kV and low turn-on voltage [16]. However, there is a need to investigate the switching behavior of Tri-anode SBDs, as its 3D nature may increase the device capacitance, leading to higher switching losses. In this work, we perform a complete switching characterization of Tri-Anode SBDs, whose performance are then compared to conventional planar AlGaN/GaN diodes and commercial fast-recovery Si diodes. The presented results demonstrate that not only the Tri-Anode structure does not degrade the diode switching performance, but instead it considerably improves its dynamic behavior with respect to planar devices. In addition, the excellent performance of the Tri-Anode SBDs is applied to demonstrate a monolithically-integrated Full Bridge Rectifier for AC to DC rectification, which clearly show the promising potential of diode-based GaN power ICs.

II. Device structure

The device were fabricated on a GaN-on-Si heterostructure consisting of 4.2 µm of buffer, 420 nm of unintentionally doped GaN (u-GaN) channel, 20 nm of $Al_{0.25}Ga_{0.75}N$ barrier and 2.9 nm of u-GaN cap-layer. The epi-structure presented electron concentration and mobility of the two-dimensional electron gas (2DEG) from Hall measurements at room temperature of 1.25×10^{13} cm^{-2} and 1700 cm^2/V·s, respectively. The fabrication process started with a 100 nm LPCVD Si_3N_4 deposition to passivate the device surface. The passivation layer was then patterned using wet etching (HF 50%). The mesa and nanowires in the anode region were defined by electron-beam lithography and then etched by Cl_2-based inductively coupled plasma (ICP) etching to a depth of 200 nm. The cathode ohmic contact was formed by lift-off of a metal stack of Ti (20 nm)/Al (120 nm)/Ti (40 nm)/Ni (60 nm)/Au (50 nm), which was annealed at 780 °C

© 2020 IEEE. Personal use of this material is permitted. Permission from IEEE must be obtained for all other uses, in any current or future media, including reprinting/republishing this material for advertising or promotional purposes, creating new collective works, for resale or redistribution to servers or lists, or reuse of any copyrighted component of this work in other works.

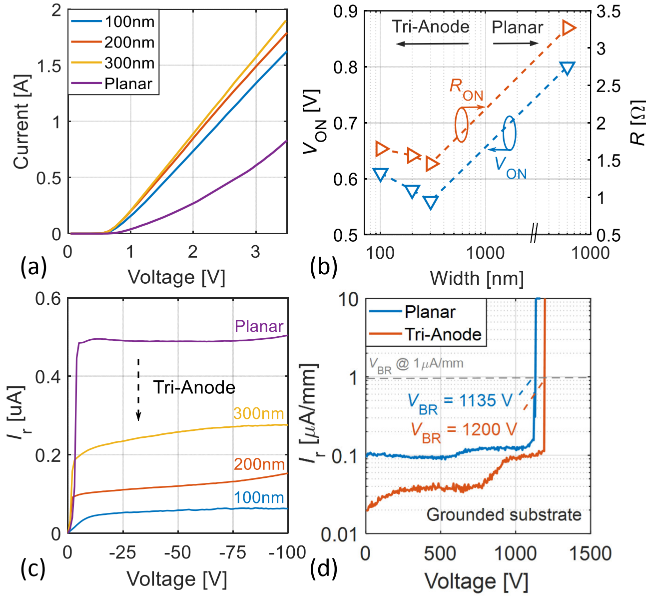

Fig.2. (a) SBD I-V curve for Tri-Anode diodes with different width and a planar device. (b) Turn-on voltage (V_{ON}) and on-resistance (R_{ON}) for planar and Tri-Anode devices with different width. (c) Diode reverse leakage current (d) Breakdown voltage for a planar and Tri-Anode SBD (w=200 nm). V_{BR} has been defined at I_D=1 μA/mm with grounded substrate.

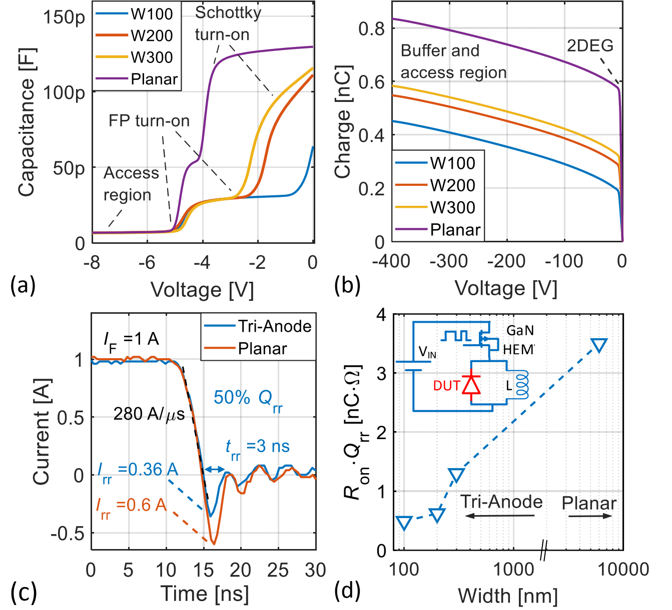

Fig.3. (a) Diode off-state capacitance for a conventional planar architecture and for Tri-Anode devices having nanowire widths of 100 nm, 200 nm and 300 nm. (b) Diode capacitive charge obtained from the integration of the device capacitance for $V_R \in$ [-400 ; 0] V. (c) Reverse recovery measurement for a Tri-Anode device having w=200 nm and a planar reference device. The reverse voltage was set to -100 V, the *di/dt* to 280 A/μs and the forward current in the on-state to 1 A. (d) $R_{ON} \cdot Q_{rr}$ figure-of-merit for a planar reference device and for Tri-Anode diodes with different widths. The top-left inset shows the double pulse tester circuit used for reverse-recovery measurement.

for 30 s. A 20 nm-thick SiO_2 layer was conformally deposited by ALD and then removed in the schottky anode region by wet etching. Lastly, the anode contact was formed by Ni (50 nm)/Au (100 nm), followed by the deposition of thick metal pads for the interconnections. Three types of devices were fabricated having nanowires widths (w) of 100 nm, 200 nm and 300 nm plus a conventional planar diode that was used as reference. To provide a fair comparison, the same total field plate length of 3 µm and the same cathode to anode distance of 16.5 µm was designed for Tri-Anode and planar devices. The devices were scaled up by integrating 50 interdigitated finger for a total device active width of 9.9 mm. Scaled-up devices were designed to minimize the effect of parasitic component in the measurement circuit and provide a more reliable switching characterization. A scanning electron microscopy image of the Tri-Anode SBD fingers is shown in Fig. 1(a) while a Focused Ion Beam cross-section of the Tri-Anode and Tri-Gate region is presented in Fig. 1(b-c).

III. Device Characterization

The Tri-Anode architecture leads to a significant improvement of the diode DC performance with respect to the planar reference, as shown in Fig. 2 (a-c). On the one side, the diode turn-on voltage is reduced thanks to the 2DEG Schottky side contact while, on the other side, the reverse leakage current decreases thanks to the electric field shielding by the Tri-Gate field plate. This results in highly performing devices with low forward voltage (V_F) and high breakdown voltage V_{BR} of 1200 V at 1 µA/mm (Fig. 2(d)).

To understand the effect of the Tri-Anode structure on the device switching performance, the diode off-state capacitance was measured using a Keysight B1505 analyzer, applying a 100 mV signal at 1 MHz. From Fig. 3(a), three different regions can be identified: for V_{AC} < -5 V the capacitance is small and dominated by the buffer and access regions contribution, showing no clear difference between the various architectures. For V_{AC} > -5 V, the field plate region turns on, leading to a first step in the capacitance curve, followed by a second step corresponding to the Schottky region contribution. While this sequence is consistent for all the architectures considered, the capacitance value and the position of the steps strongly depend on the device design. In particular, as the nanowire width is reduced, the Tri-Gate and Tri-Anode turn-on shifts closer to 0 V, as a result of the variation in the nanowire threshold voltage [17]–[19]. Additionally, while the capacitance per each nanowire indeed increases due to the 3D structure, leading to a better control as shown by the excellent Tri-Anode blocking performance, the overall device capacitance decreases. This is due to the partial 2DEG removal in the trench region and to the diminished charge in the nanowire due to sidewalls depletion and strain relaxation [20], [21]. This behavior results in an overall decrease in the capacitive charge for the Tri-Anode devices with respect to the planar reference, which further reduces as the nanowire width decreases (Fig. 3(b)). To confirm these results, a diode reverse-recovery measurement was performed through the use of double-pulse-tester circuit (DPT) [22]–[24]. Such technique allows to observe the effect of the total on and off-state device charge when the diode is suddenly switched off with a high *di/dt*.

Fig. 3(c) clearly shows an improvement in the diode reverse-recovery behavior for the Tri-Anode SBD (w=200 nm) with respect to the planar reference, resulting in a 50% decrease in the reverse recovery charge (Q_{rr}). While the Q_{rr} can be significantly reduced by tuning w, the device on-

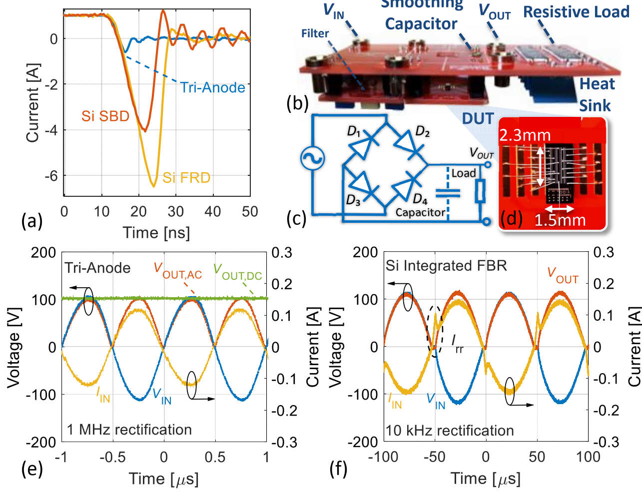

Fig.4. (a) Reverse recovery measurement for a GaN Tri-Anode SBD, a commercial 600 V-rated fast-recovery Si diode and a commercial 200 V-rated Si SBD. The reverse voltage was set to -100 V, the *di/dt* to 280 A/µs and the forward current in the on-state to 1 A. (b) PCB setup for the FBR testing with the corresponding circuit schematics (c) and image of the wire-bonded die (d). (e) 1 MHz full-wave rectification for a Tri-Anode based FBR with a 250 V peak-to-peak signal. Full AC-to-DC rectification was achieved by the addition of an output smoothing capacitor. (f) Commercial Si FBR operation for a 250 V peak-to-peak signal with 10 kHz frequency.

resistance (R_{ON}) is only slightly affected by the nanowire widths considered in this study (Fig. 2(a)). This is an important results as it leads to a considerable $R_{ON}\cdot Q_{rr}$ figure-of-merit reduction for the Tri-Anode architecture (Fig. 3(d)). The presented Tri-Anode GaN SBDs were then compared with a commercial Si fast-recovery diode with similar rating [25] and a 200 V-rated Si SBD [26]. Fig. 4(a) clearly shows a significant reduction in the reverse recovery time and peak current for the GaN Tri-Anode diode, which results in a more than 80x-decrease in the reverse-recovery charge, leading a much more efficient operation, especially at high frequency.

To investigate the effect of the diminished diode charge in a real circuit and showcase the potential of this technology for future power integrated circuits (ICs), four of the presented SBDs were monolithically integrated on the same chip to form a Full Bridge Rectifier (FBR), whose operation was then compared with a FBR using commercial Si devices.

Fig. 4(b-d) shows the PCB testing setup, the circuit schematics and the wire-bonded chip, whose total dimensions are 2.3 mm x 1.5 mm. Thanks to the small Tri-Anode SBDs charge, the FBR can properly operate at a frequency of 1 MHz without signal distortion (Fig. 4(e)). Additionally, by adding an output smoothing capacitor, full AC-to-DC rectification was achieved, with minimum output ripple thank to the high frequency operation. These results were compared to a commercial Si FBR with similar rating [27], which instead show a clear current spike every half-period, in correspondence with each diode-pair turn-off. Such behavior derives from the consistent diode reverse recovery current and is already present for an input signal at 10 kHz, severely limiting the device operation at higher frequency.

IV. Conclusions

In this work, we performed a thoroughly investigation of the switching performance of GaN Tri-Anode SBDs. The presented results demonstrate that the Tri-Anode architecture is not only highly beneficial for the diode DC performance, but can also significantly improve its switching behavior. In particular a considerable reduction in the $R_{ON}\cdot Q_{rr}$ figure-of-merit was demonstrated for Tri-Anode SBDs with respect to conventional planar devices, which shows their great potential for fast–switching power applications. The Tri-Anode excellent performance were demonstrated in a real circuit by realizing a monolithically integrated FBR able to achieve full AC to DC rectification at a frequency of 1 MHz, which represents a significant improvement with respect to state-of-the-art commercial solutions based on Si.

Acknowledgment

The authors would like to acknowledge the staff of CMI and ICMP cleanrooms at EPFL for their technical support. In particular, they would like to thank Giancarlo Corradini for his help with the device packaging.

References

[1] N. Kaminski and O. Hilt, “SiC and GaN devices – wide bandgap is not all the same,” *IET Circuits, Devices Syst.*, vol. 8, no. 3, pp. 227–236, 2014.

[2] D. Garrido-DIez and I. Baraia, “Review of wide bandgap materials and their impact in new power devices,” *Proc. 2017 IEEE Int. Work. Electron. Control. Meas. Signals their Appl. to Mechatronics, ECMSM 2017*, pp. 1–6, 2017.

[3] J. Millan and P. Godignon, “Wide Band Gap power semiconductor devices,” *Proc. 2013 Spanish Conf. Electron Devices, CDE 2013*, pp. 293–296, 2013.

[4] “GaN Power ICs : Integration Drives Performance Navitas Semiconductor Inc,” 2017. [Online]. Available: http://files.iccmedia.com/events/powercon17/munich_02_navitas.pdf.

[5] “EPC2112 – 200 V, 10 A Integrated Gate Driver eGaN® IC,” 2003. [Online]. Available: https://epc- co.com/epc/Portals/0/epc/documents/datasheets/EPC2112_prelim inary.pdf.

[6] Q. Zhou *et al.*, “High reverse blocking and low onset voltage AlGaN/GaN-on-Si lateral power diode with MIS-gated hybrid anode,” *IEEE Electron Device Lett.*, vol. 36, no. 7, pp. 660–662, 2015.

[7] J. Hu *et al.*, “Performance Optimization of Au-Free Lateral AlGaN/GaN Schottky Barrier Diode With Gated Edge Termination on 200-mm Silicon Substrate,” *IEEE Trans. Electron Devices*, vol. 63, no. 3, pp. 997–1004, 2016.

[8] J. Lei *et al.*, “650-V Double-Channel Lateral Schottky Barrier Diode with Dual-Recess Gated Anode,” *IEEE Electron Device Lett.*, vol. 39, no. 2, pp. 260–263, 2018.

[9] J. Lei *et al.*, “An Interdigitated GaN MIS-HEMT/SBD Normally-Off Power Switching Device wit Low ON-resistance and Low Reverse Conduction Losses,” *IEDM*, vol. 33, no. December, pp. 609–612, 2017.

[10] M. Zhu *et al.*, “1.9-kV AlGaN/GaN Lateral Schottky Barrier Diodes on Silicon,” *IEEE Electron Device Lett.*, vol. 36, no. 4, pp. 375–377, 2015.

[11] B. Weiss, R. Reiner, P. Waltereit, R. Quay, and O. Ambacher, “Analysis and modeling of GaN-based multi field plate Schottky power diodes,” *2016 IEEE 17th Work. Control Model. Power Electron. COMPEL 2016*, pp. 1–6, 2016.

[12] J. Ma and E. Matioli, “High-voltage and low-leakage AlGaN/GaN tri-anode schottky diodes with integrated tri-gate transistors,” *IEEE Electron Device Lett.*, vol. 38, no. 1, pp. 83–86, 2017.

[13] E. Matioli, B. Lu, and T. Palacios, “Ultralow leakage current AlGaN/GaN schottky diodes with 3-D anode structure,” *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3365–3370, 2013.

[14] J. Ma and E. Matioli, “Slanted Tri-Gates for High-Voltage GaN

Power Devices," *IEEE Electron Device Lett.*, vol. 38, no. 9, pp. 1305–1308, 2017.

[15] L. Nela, G. Kampitsis, J. Ma, and E. Matioli, "Fast-Switching Tri-Anode Schottky Barrier Diodes for Monolithically Integrated GaN-on-Si Power Circuits," *IEEE Electron Device Lett.*, vol. 41, no. 1, pp. 99–102, 2020.

[16] J. Ma and E. Matioli, "2 kV slanted tri-gate GaN-on-Si Schottky barrier diodes with ultra-low leakage current," *Appl. Phys. Lett.*, vol. 112, no. 5, 2018.

[17] L. Nela, M. Zhu, J. Ma, and E. Matioli, "High-performance nanowire-based E-mode Power GaN MOSHEMTs with large work- function gate metal," *IEEE Electron Device Lett.*, vol. 40, no. 3, pp. 439–442, 2019.

[18] B. Lu, E. Matioli, and T. Palacios, "Tri-gate normally-off GaN power MISFET," *IEEE Electron Device Lett.*, vol. 33, no. 3, pp. 360–362, 2012.

[19] J. Ma, G. Santoruvo, L. Nela, T. Wang, and E. Matioli, "Impact of Fin Width on Tri-Gate GaN MOSHEMTs," *IEEE Trans. Electron Devices*, vol. 66, no. 9, pp. 1–7, 2019.

[20] M. Azize and T. Palacios, "Top-down fabrication of AlGaN/GaN nanoribbons," *Appl. Phys. Lett.*, vol. 98, no. 4, 2011.

[21] M. Hugues *et al.*, "Strain evolution in GaN nanowires: From free-surface objects to coalesced templates," *J. Appl. Phys.*, vol. 114, no. 8, 2013.

[22] J. H. Lee, J. K. Yoo, H. S. Kang, and J. H. Lee, "840 V/6 A-AlGaN/GaN schottky barrier diode with bonding pad over active structure prepared on sapphire substrate," *IEEE Electron Device Lett.*, vol. 33, no. 8, pp. 1171–1173, 2012.

[23] S. Han, S. Yang, R. Li, X. Wu, and K. Sheng, "Current-Collapse-Free and Fast Reverse Recovery Performance in Vertical GaN-on-GaN Schottky Barrier Diode," *IEEE Trans. Power Electron.*, vol. 34, no. 6, pp. 5012–5018, 2019.

[24] L. Efthymiou, G. C. G. Longobardi, F. Udrea, E. Lin, T. Chien, and M. Chen, "Zero reverse recovery in SiC and GaN Schottky diodes: A comparison," *Proc. Int. Symp. Power Semicond. Devices ICs*, vol. 2016–July, pp. 71–74, 2016.

[25] "http://www.vishay.com/docs/86040/byv26.pdf." .

[26] "https://eu.mouser.com/datasheet/2/395/SS1H4LW%20SERIES_A1606-1114442.pdf." .

[27] "http://www.vishay.com/docs/88572/dfma.pdf." .