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High-Current Low-Voltage Power Supply for Superconducting Magnets

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Aux collègues qui sont devenus amis, aux amis qui font partie de la famille, à ma famille...

Abstract

In the wide range of applications for power supplies, the ones dedicated to feeding superconducting magnets occupy a niche. This particular kind of magnets has the intrinsic property of having zero resistance, and is only used in high-end facilities for fundamental research or medical application to produce large magnetic fields. This implies that powering superconducting magnets requires a very high current combined with a low voltage only due to the interface between the power supply and the superconducting circuit.

The case study developed in this thesis is based on European Organization for Nuclear Research (CERN) High Luminosity LHC (HL-LHC) project where an upgrade of the present Large Hadron Collider (LHC) installations needs to be developed. The objective is to increase the overall performances of the collider, targeting to augment the experimental data sets by one order of magnitude compared to the present one. To achieve this goal, a stronger magnetic field is needed to enhance the collision rate of particles by having a thinner particle beam, thus directly impacting the power supply ratings and driving many design choices for the power supply.

This thesis is divided into two parts where at first a global system level approach is adopted, the definition of the operational requirements and the constraints related to high-current low-voltage power supplies in the context of CERN environment are detailed. As the new powering scheme of the dedicated *Inner-Triplet magnets* imposes a 2-quadrant operation of the supply, there is a need to locally integrate an energy storage solution in the supply to recover the magnetic energy when de-energizing the magnet. The integration of such storage element impacts the complete power flow of the power supply, as well as the sizing of the various stages of power conversion. To this extent a study of the best location of the storage within the supply is conducted and gives the basis for the power converters sizing. Additionally, a complete overview of the selected storage technologies is conducted, where supercapacitors and batteries are compared. The overall layout and suitable storage technologies are highlighted regarding the design of this new 2-quadrant high-current low-voltage power supply for superconducting magnets.

The second part focuses on the power stage which processes the high current, the DC/DC output stage. By nature, because of the high level of current, the strict precision and the extended lifetime required for the power supply are such that a modular design is mandatory. Considering the case of a 18 kA nominal current output rating, an in-depth study of an optimized novel 2-quadrant high-current low-voltage DC/DC building block is presented. It is achieved through a multi-objective optimization that includes the core elements of the topology as well as the defined optimal modulation pattern. Volume and efficiency are considered as the main criteria during this process, the best compromise between those two is considered as the optimal solution. An elementary building block rated for 250 A, ±10 V is selected, where eight paralleled blocks are composing a *sub-converter*, and nine of those *sub-converters* in parallel allow to reach the nominal current requirement. The overall control strategy and experimental performances are demonstrated at a small scale, paving the way to a viable full-scale demonstrator that could effectively be used in a new generation of power supplies for superconducting magnet at CERN.

Keywords high-current, low-voltage, DC/DC power supply, energy storage, multi-objectives optimization, prototype, experimental results

Résumé

Dans la large gamme d'applications des alimentations électriques, celles dédiées à l'alimentation des aimants supraconducteurs occupent un marché de niche. Ce type particulier d'aimant a la propriété intrinsèque d'avoir une résistance nulle, et n'est utilisé que dans des installations de pointe pour la recherche fondamentale ou dans le domaine médical afin de produire des champs magnétiques imporants. Cela implique que l'alimentation des aimants supraconducteurs doit fournir un courant très élevé combiné à une tension très basse uniquement due à l'interface entre l'alimentation et le circuit supraconducteur.

L'étude développée dans cette thèse est basée sur le projet HL-LHC de l'Organisation Européenne pour la Recherche Nucléaire (CERN) où une mise à niveau des installations actuelles du Grand collisionneur de hadrons (LHC) doit être étudiée. L'objectif est d'améliorer les performances globales du collisionneur, en visant à augmenter d'un ordre de grandeur les données récoltées par les expériences. Pour atteindre cet objectif, un champ magnétique plus puissant est nécessaire afin d'améliorer le nombre de collision des particules, en ayant un faisceau de particules plus fin, ce qui a un impact direct sur la puissance nominale de l'alimentation électrique et détermine de nombreux choix de conception de l'alimentation électrique.

Cette thèse est divisée en deux parties où, dans un premier temps, une approche globale au niveau système est adoptée, la définition des besoins opérationnels et les contraintes liées aux alimentations électriques à courant élevé et basse tension dans le contexte de l'environnement CERN sont détaillées. Comme la nouvelle stratégie d'alimentation des aimants *Inner-Triplet* impose un fonctionnement à 2-quadrants de l'alimentation, il est nécessaire d'intégrer une solution de stockage d'énergie local dans l'alimentation pour récupérer l'énergie magnétique lors de la désexcitation de l'aimant. L'intégration d'un tel élément de stockage a une incidence sur le flux de puissance complet de l'alimentation, ainsi que sur le dimensionnement des différents étages de la conversion de puissance. Dans cette mesure, une étude de l'emplacement le plus approprié pour l'élément de stockage est menée et donne la base du dimensionnement des convertisseurs de puissance. En outre, une vue d'ensemble complète des technologies de stockage sélectionnées est réalisée, où les supercondensateurs et les batteries sont comparés. L'agencement global et les technologies de stockage appropriées sont mis en évidence en ce qui concerne la conception de cette nouvelle alimentation électrique à courant élevé et basse tension fonctionnant en 2-quadrants pour les aimants supraconducteurs.

La deuxième partie se concentre sur l'étage de puissance qui traite le courant élevé, l'étage de sortie DC/DC. Par sa nature, en raison du niveau élevé de courant, la précision stricte et la durée de vie prolongée requises pour l'alimentation électrique sont telles qu'une conception modulaire est obligatoire. Dans le cas d'un courant nominal de sortie de 18 kA, une étude approfondie d'un nouveau bloc élémentaire d'électronique de puissance optimisé pour le fonctionnement 2-quadrants à courant élevé et basse tension est présentée. Elle est réalisée grâce à une optimisation multi-objectifs qui comprend les éléments fondamentaux de la topologie ainsi qu'un modèle de modulation optimal. Le volume et l'efficacité sont considérés comme les principaux critères au cours de ce processus, le meilleur compromis entre ces deux facteurs étant considéré comme la solution optimale. Un bloc de construction élémentaire conçu pour 250 A, ±10 V est sélectionné, où huit blocs en parallèle composent un *sous-convertisseur*, et neuf de ces *sous-convertisseurs* en parallèle permettent d'atteindre le courant nominal requis. La stratégie de contrôle globale et les performances expérimentales sont démontrées à échelle réduite, ouvrant la voie à un démonstrateur grandeur nature viable qui pourrait être utilisé efficacement dans une nouvelle génération d'alimentations pour aimant supraconducteur au CERN.

Mots-clés courant élevé, basse tension, alimentation électrique DC/DC, stockage d'énergie, optimisation multi-objectifs, prototype, résultats expérimentaux

Zusammenfassung

Netzgeräte werden heutzutage überall gebraucht und eingesetzt, wenn es jedoch um die Versorgung von supraleitenden Magneten geht, so besetzen Diese nur eine Nische. Eine Besonderheit solcher Magneten ist, dass sie keinen elektrischen Wiederstand aufweisen, und werden nur in Spitzeneinrichtungen für fundamentale Forschung und in medizinischen Anwendungen eingesetzt um ein starkes Magnetfeld zu erzeugen. Dies bedeutet, dass das verbundene Netzgerät in der Lage sein muss sehr hohe Ströme bei sehr niedriger Spannung zu erzeugen wegen der Schnittstelle zwischen dem Netzgerät und dem supraleitenden Stromkreis.

Die Fallstudie, welche in dieser Doktorarbeit entwickelt wurde, basiert auf dem CERN HL-LHC Projekt wo eine Verbesserung von der aktuellen LHC Einrichtung entwickelt werden sollte. Das Ziel ist die insgesamte Leistung des Teilchenbeschleunigers zu erhöhen und dabei gezielt die experimentellen Datensätze um eine Größenordnung im Vergleich zu den bestehenden Datensätzen zu erweitern. Um das gesetzte Ziel zu erreichen wird ein stärkeres Magnetfeld, welches die Kollisionsrate der Teilchen durch einen dünneren Teilchenstrahl verbessert, benötigt. Dies beeinflusst die Nennwerte der Netzgeräte als auch viele andere dies bezogene Designwahlen.

Die Doktorarbeit ist in zwei Teile aufgeteilt. Im ersten Teil wurde eine globale Herangehensweise auf der Systemebene angenommen, zusätzlich wurden die Betriebsanforderungen und die Beschränkungen bezüglich Hochstrom- und Niederspannungsnetzteil im Rahmen von der CERN Umgebung näher definiert. Da das neue Antriebsschema für die zugehörigen *Inner-Triplet Magneten* Zwei-Quadranten-Operation des Speisegeräts verlangt, ist es notwendig einen Energiespeicher lokal in das Netzgerät einzufügen. Dadurch kann die magnetische Energie, die durch Entmagnetisierung der Magnete entsteht, zurückzugewonnen werden. Die Integration eines solchen Speicherelements beeinflusst nicht nur den ganzen Leistungsfluss des Netzgerätes, sondern auch die Dimensionierung von bestimmten Stufen der Energieumwandlung. Diesbezüglich wurde eine Studie durchgeführt, um die beste Plazierung des Energiespeichers innerhalb vom Netzgerät zu bestimmen, womit eine Grundlage für die Dimensionierung des Leistungswandlers gewonnen wird. Darüber hinaus wurde eine umfassende Übersicht über die ausgewählten Speichertechnologien geschaffen, in der die Superkondensatoren und die Batterien miteinander verglichen wurden. Schließlich wurden das Gesamt-Layout und die passenden Speichertechnologien für das Designs des neuen Zwei-Quadranten-Hochstrom- und Niederspannungsnetzteil für supraleitenden Magneten hervorgehoben.

Der zweite Teil beschäftigt sich mit der Leistungsendstufe, d.h. mit der Ausgangsstufe vom DC/DC Netzgerät, die den Hochstrom verarbeitet. Da von Natur aus, wegen des hohen Stromwertes, strikte Genauigkeit und verlängerte Laufzeit des Netzgerätes erforderlich sind, ist ein modulares Design Pflicht. Unter Berücksichtigung von 18 kA Ausgansstromnennwert wurde eine gründliche Studie über den optimierten und neuartigen Zwei-Quadranten-DC/DC Baustein mit Hochstrom und Niederspannung dargestellt. Mithilfe mehrkriterieller Optimierung, wurden die Hauptelemente der Topologie sowie das optimale Modulationsmuster bestimmt. Dabei wurden Volumen und Effizienz im Optimierungsprozess als Hauptkriterien berücksichtigt und der Kompromiss zwischen den beiden wurde als die optimale Lösung beachtet. Der grundlegende Baustein mit Nennwerten von 250 A und ± 10 V wurde ausgewählt und dabei setzten acht parallele Bausteine den sogenannten *Sub-Wandler* zusammen. Zusätzlich ermöglichen neun parallel geschaltete *Sub-Wandler* den Stromnennwert zu erreichen. Die gesamte Regelungsstrategie und die experimentellen Ergebnisse wurden im Kleinformat demonstriert, was im Endeffekt die Errichtung eines umsetzbaren maßstäblichen Prototyps ermöglicht, der bei CERN als neue Generation von Netzgeräten für supraleitenden Magneten verwendet werden könnte.

Schlüsselwörter: Hochstrom, Niederspannung, DC/DC Netzgerät, Energiespeicher, Pareto-Optimierung, Prototyp, Versuchsergebnisse

Acknowledgements

Electricity is power
John Roderick [1]

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To the colleagues who have become friends, to the friends who have become family - Merci à vous.

Coppet, April 2020
Emilien

[1] Roderick on the Line, Ep. 340: *Scared and Stupid*

List of Abbreviations

B2B	Board-to-Board
CCM	Continuous Conduction Mode
CERN	European Organization for Nuclear Research
DCCT	DC Current Transformer
EMC	Electromagnetic Compatibility
ESR	Equivalent Series Resistance
HL-LHC	High Luminosity LHC
IEC	International Electrotechnical Commission
IMS	Insulated Metal Substrate
IPOP	Input Parallel Output Parallel
LFP	Lithium Ferrophosphate
LHC	Large Hadron Collider
LTO	Lithium-Titanate
MEG	Multi-port Energy Gateway
MRI	Magnetic Resonance Imaging
PCB	Printed Circuit Board
PSU	Power Supply Unit
PWM	Pulse-Width Modulation
RMS	Root Mean Square
SCL	SuperConducting Link
SoC	State-of-Charge
SR	Synchronous Rectification

Contents

1 Introduction

A magnet is an object or material that produces a magnetic field. From its early discovery, several centuries before Christ, the lodestone (naturally magnetized piece of the mineral magnetite) were find to attract iron, and started fascinating people. It took a few millennium to learn and understand what was first thought to be magical power, in making a practical use of it in navigation systems with the compass. It is not before Hans Christian Ørsted (1777-1851) that the link between electric current and magnetic field was discovered [1], [2]. Eventually James Clerk Maxwell (1831-1879) was the one to formulate the equations governing electromagnetism in *'A Dynamical Theory of the Electromagnetic Field'* [3], bringing together the concepts of electricity, magnetism and light.

History retains William Sturgeon to be the person who built the first electromagnet in 1824 [4]. His prototype consisted of an iron core wrapped in 18 turns of bare copper wire supplied by a single-cell battery, a scheme of his assembly is depicted in **Fig. 1.1(a)**. The concept of electromagnet evolved from this time forth until reaching the ferromagnetic limit of 1.6 T. This limit has been overpassed with the development of superconducting magnets (c.f. **Fig. 1.1(b)**) [5]–[7], where the current can flow in the conductors with no resistance. Their main use is for Magnetic Resonance Imaging (MRI) [8] or particle accelerators [9]. The improvement of such magnets goes together with the development of adequate power supplies [10], which is the topic of this thesis. The power supply allows to regulate, very precisely, the current flowing through the magnet, thus enables to control the generated magnetic field. In the specific case of particle accelerator facilities, dedicated power supplies [11]–[13] are nowadays the interface between the power grid and all the different electromagnets.

(a) (b)

Fig. 1.1 Evolution of electromagnets: (a) first electromagnet prototype by Sturgeon (1824)[1]and (b) model of a particle accelerator (LHC) superconducting dipole magnet (1994)[2].

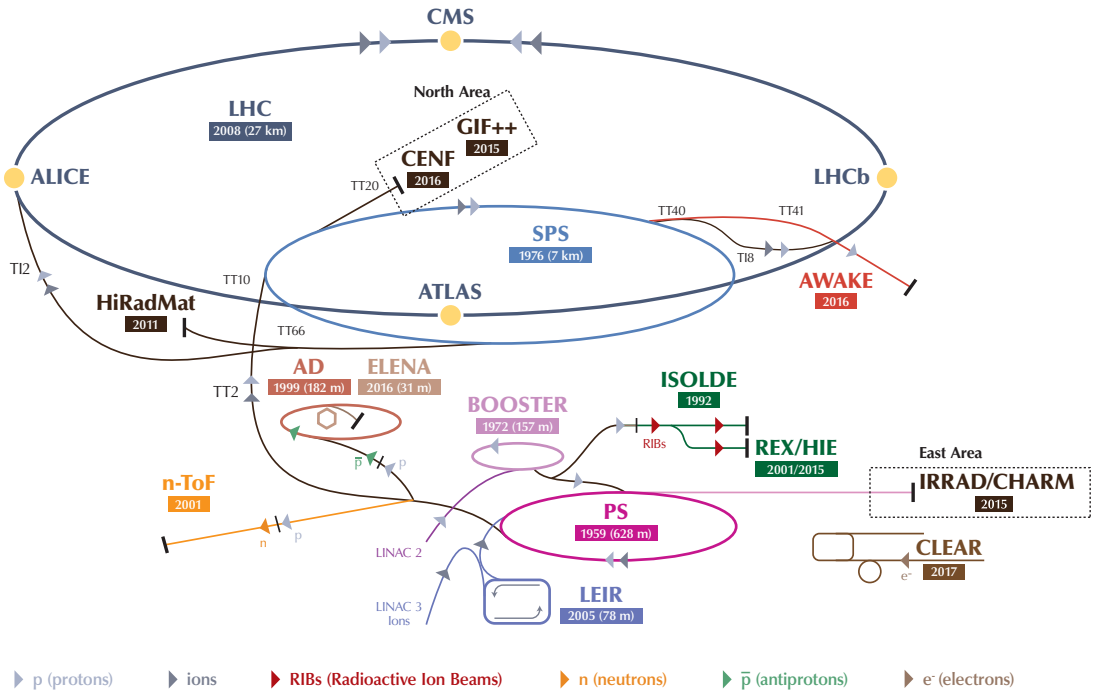
[1] *'Improved Electro Magnetic Apparatus'* Transaction of the Royal Society of Arts Manufactures and Commerce, Volume 43, Plate 3, Figure 13.

[2] CERN image library: CERN-AC-9402027.

1.1 Background and Motivation

European Organization for Nuclear Research (CERN) is a European research organization whose focus is particle physics. In order to do so, it operates a complex of particle accelerators as depicted in **Fig. 1.2**. In these installations, the magnets are to the particles beams what lenses are to the optical beams. In other words, the beam of particles can be shaped by the magnetic field in its trajectory, its configuration (focus, defocus, polarization) and other properties depending on the nature of its particles, thanks to various configurations of electromagnets. The Large Hadron Collider (LHC) [14], [15] is the largest and the most powerful particle accelerator, not only in CERN, but in the world. The level of energy at which operates the LHC requires the use of superconducting magnets to produce a field over 8 T, when powered by a current of 11 kA [14, Chapter 10].

To power those superconducting magnets, a variety of specialized power supplies have been developed. Their main characteristics is to provide a large current under a reduced voltage thanks to the zero resistance of the superconducting magnets themselves, usually several kilo amperes with a voltage below 200 V [16]. At CERN, the installed base for LHC has a total of 1 700 different power supplies which deliver a total of 1.7×10^6 A [17] for a proper operation of the system.



LHC - Large Hadron Collider // SPS - Super Proton Synchrotron // PS - Proton Synchrotron // AD - Antiproton Decelerator // CLEAR - CERN Linear Electron Accelerator for Research // AWAKE - Advanced WAKefield Experiment // ISOLDE - Isotope Separator OnLine // REX/HIE - Radioactive EXperiment/High Intensity and Energy ISOLDE // LEIR - Low Energy Ion Ring // LINAC - LINear ACcelerator // n-ToF - Neutrons Time Of Flight // HiRadMat - High-Radiation to Materials // CHARM - Cern High energy AcceleRator Mixed field facility // IRRAD - proton IRRADiation facility // GIF++ - Gamma Irradiation Facility // CENF - CErn Neutrino platForm

Fig. 1.2 The CERN accelerator complex as of August 2018[3]. Nature of the particles and name of the experiment are also given, where LHC is the particle accelerator of interest for the thesis project.

[3]CERN image library: OPEN-PHO-ACCEL-2018-005.

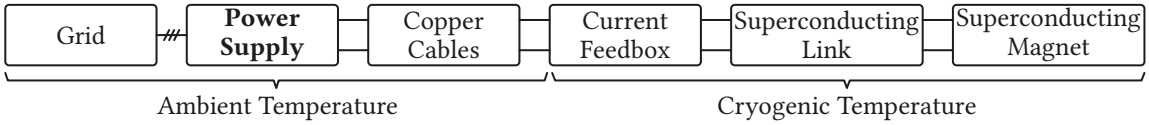


Fig. 1.3 Overall structure of the interface between the electrical grid and a superconducting magnet.

As the connection to superconducting materials cannot be made at the power supply level, there is a need for copper cables to transmit the power to the current feedbox [18], [19], which is the interface from the normal to the superconducting world. The overall structure of this interface between a superconducting magnet and the electrical grid is given in **Fig. 1.3**. On the scheme, ambient temperature is the one of the environment in which the power supply is installed, the cryogenic temperature is 1.9 K. The position of the current feedbox influences the ratings of the power supply: its voltage is imposed by the length and properties of the copper cables to the feedbox, whereas the current ratings are governed by the superconducting magnets needs.

As of 2013, the High Luminosity LHC (HL-LHC) project [20]–[22] was launched as an upgrade of the actual LHC in order to increase its performances by a factor of five at the horizon of the year 2026. One of the main change in this upgrade is the powering structure of several magnets, including the specific ones called *Inner-Triplet magnets*, which are the ones of interest for the work presented in this thesis. Those *Inner-Triplet magnets* are a series of superconducting magnets, consisting of three quadrupole optical elements and four magnets. They provide the final focusing of the particle beam right before the four interaction points (CMS, LHCb, ATLAS and ALICE in **Fig. 1.2**) along the LHC ring. In total, it is eight of such magnets that are present in the collider, each of them being powered by a dedicated power supply.

The HL-LHC upgrade focuses particularly on ATLAS and CMS interaction regions *Inner-Triplet magnets* because of their critical role in the performance of the collider. They are improved to produce a stronger magnetic field, integrating a novel superconducting material, and fed with a state of the art SuperConducting Link (SCL), also using the superconducting technology. The improved physical layout of the elements, even if in the same structure as the one depicted in **Fig. 1.3**, will greatly affect the ratings of the power supply as the energy dissipation in the transmission line between the power supply and the magnet becomes negligible [23].

To be more concrete, some numbers are gathered in this paragraph regarding the CERN energy consumption for the year 2018 [24]. During that year, the CERN overall consumption was 1 251 GWh, where LHC represents 53 % of the total. In the LHC share (664 GWh), 42 % are dedicated to the cryogenics, required to provided the low temperature of the system (1.9 K) that is necessary to obtain the superconducting behavior of the magnets. Only a reduced share of the LHC consumption (5 %) is due to magnets and their power supplies. Nevertheless, it still represents 31 GWh over one year. In the actual trend of making good use of the resources at our disposal, it is legitimate to use the energy wisely in taking advantage of the cycling operation of the particle accelerator: recovering the energy of an ending cycle to reuse it for the upcoming one. The energy integration options are analyzed in order to keep a low footprint of the power supply on the electrical utility grid.

As the LHC is a circular collider relying on superconducting magnets, its operation is based on a cycle of several hours, being repeated once or twice per day depending on the operational conditions. An overview of a typical LHC cycle is given in **Fig. 1.4** [25]–[27], representing the current feeding the main dipoles through time, this is the typical reference profile that all the other magnets follow.

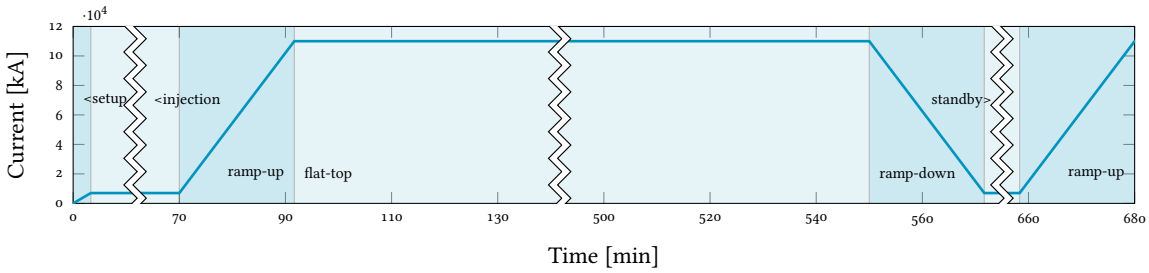


Fig. 1.4 Typical cycling profile of the LHC (simplified). The y-axis is the current feeding the main dipole magnets, reference of the whole facility.

In the simplified profile presented in **Fig. 1.4**, typical phases can be identified as follow.

- *Setup* is when no beam in is present the accelerator ring.
- *Injection* is a constant reduced current phase, a few hundred amperes, the beam of particle is established in the LHC. The length of this operation depends on the filling scheme of the particle accelerator [28], it usually lasts for 70 min.
- *Ramp-up* start once the initialization phase is completed. It is verified that a stable circulating beam is ready to be taken to higher intensities needed for physics. All the systems are then ramping gradually towards their nominal point of operation. This phase is 20 min long.
- *Flat-top* is when physics is happening and systems are running at their nominal operation point, this phase can be up to 15 h long if no problem occurs.
- *Ramp-down* happens once the system is decided to be ramped down or a fault occurs, it consists in de-energizing all the systems in order to return to a the setup or injection mode of operation. There are no more particles in the accelerator during this phase which lasts 22 min.
- *Standby* is the phase between two runs. During regular operation, it is desired to be as short as possible in order to maximize operational time for physics, which is the flat-top phase.

The HL-LHC will rely on the heritage passed by LHC and adopt the same modes of operation, as the upgrade is mostly focused on hardware. Nevertheless, a new requirement on the ramp-down time is adopted, in order to reduce it to 20 min. The addition of this operational constraint and the modification in the powering layout makes the actual *Inner-Triplet magnets* power supplies obsolete. A simplified depiction of the powering layout is given in **Fig. 1.5**. Commissioned in the early 2000's, the actual power supplies are relying on the resistivity of the copper cables (cf. **Fig. 1.5(a)**) to dissipate the energy stored in the magnets, limiting their operation to 1-quadrant only.

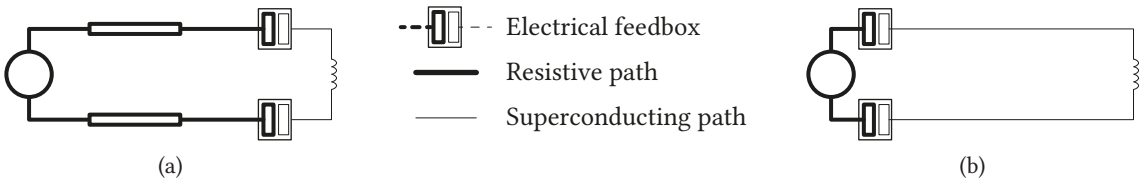


Fig. 1.5 Simplified powering scheme of the *Inner-Triplet magnets*: (a) current one in the LHC with long copper cables and (b) future one in the HL-LHC with feedbox next to the converter and superconducting link.

The upgraded version is drastically reducing the length of the copper cables (cf. **Fig. 1.5(b)**), lowering the output voltage rating of the power supply and forcing the need for the application of a negative voltage across the load in order to ramp-down the current.

Taking those requirements into consideration makes the development of modern high-current low-voltage power supplies necessary. Thanks to the new powering layout jointly with the cycling operation of the system, some attention can be focus on the energy recovery of the system in order to optimize the use of the energy at the power supply level. Additionally, switched mode based power supply approach is considered as research track of the thesis.

1.2 Scope and Objectives of the Thesis

This work focuses on the design optimization and verification of a high-current low-voltage power supply dedicated to the powering of superconducting magnets. Ratings and characteristics of such power supply are gathered hereafter, it should also respect the HL-LHC requirements for unprecedented precision [22]. In order to reach the ramp-down time constraint, it should be able to operate in 2-quadrant by applying a negative voltage across the magnet. During the ramp-down, the energy stored in the magnet could be recovered and stored for the next cycle in a dedicated energy storage unit, thus the use of energy storage technologies is also analyzed at the system level. The design of a DC/DC power supply stage that fits those requirements is the core of the thesis.

- Maximum output current: 18 kA.
- Output voltage range: ±10 V.
- Lifetime expectancy: 20 years; 20 000 cycles expected.

The main contributions of the thesis are:

- A careful definition of the need and constraints regarding power supply for superconducting magnet, where a state of the art about high-current low-voltage power supply is conducted.
- A study about the use of energy storage system in such power supply is conducted, taking advantage of the cycling operation of the particle accelerator; integration possibilities and overview of the storage technologies are presented.
- A multi-objectives design optimization of the power supply is detailed, supported by mathematical tools and components integration, with the goals to obtain a highly efficiency and compact solution.
- The implementation of the selected optimal design for a reduced scale power supply prototype, able to provide 750 kA, ±10 V is realized, including advanced integration of the components. This constitutes a proof of concept for a full size converter.

1.3 Structure of the Thesis

The thesis is organized as follow.

Chapter 1 contains the introduction, background, objectives and structure of the thesis.

Chapter 2 presents the state of the art in the high-current low-voltage power supplies, for various applications with a particular focus on the superconducting magnets where the specific challenges related to the particle accelerator applications are assessed. The specific case of CERN is detailed where a larger picture at the system level is introduced in order to get a good understanding of the environment surrounding the power supply.

Chapter 3 details the power supply structure and explore the possibilities to integrate an energy storage system in the specific case of the *Inner-Triplet magnets* powering for HL-LHC. The definition of the storage requirements is established and a brief overview of the energy storage technologies is performed. Findings of the study reveal that the battery based solutions are the most suited for the dedicated application.

Chapter 4 focuses on the DC/DC output stage of the power supply: this is the converter that processes the full load current. As the modularity is a key concept of such power supplies, and paralleling is necessary in order to achieve the desired ratings, the modularity structure and terminology is introduced in this chapter. The scope is then narrowed down to an individual *sub-converter* able to deliver 2 kA. Moreover, the definition of the topology and the way to achieve the 2-quadrant operation is defined.

Chapter 5 presents the hardware selection and optimization for the critical part of the converter: semiconductors and passives constituting the output filter of the stage. A structure and mathematical tools are established in order to compare and optimize the designs according to the defined requirements. As the topology heavily relies on parallelization, the interleaving between stages is considered to relax constraints on individual stages. An optimization tool is implemented and used to sweep the parameters in order to obtain the most efficient of the realistic designs. The results of the design optimization imply that the optimal solution is to divide the *sub-converter* in eight branches, where each switch is composed by six parallel MOSFETs. The implementation of such optimal building block of the system is detailed and verified through testing.

Chapter 6 presents the control of multiple modules in parallel, taking the optimal *sub-converter* design previously determined, with eight *branches* in parallel. The control system design is carried out, implementing adequate controllers and tunning them to achieve required performances. The experimental results are collected from three realized *branches* operated in parallel, both in steady-state and dynamic operation.

Chapter 7 concludes the work and highlights the learnings taken from the thesis, laying down the path for future development in what could be even larger particle accelerators.

1.4 List of Publications

Journal papers:

J1. E. Coulinge, S. Pittet, and D. Dujic, "Design optimization of two-quadrant high-current low-voltage power supply," *IEEE Transactions on Power Electronics*, 2020

J2. E. Coulinge, S. Pittet, and D. Dujic, "High-current low-voltage interleaved power supply for superconducting magnets," *IET Power Electronics*, (under review)

Conference papers:

C1. E. Coulinge, J. Burnet, and D. Dujic, "High-current low-voltage power supplies for superconducting magnets," in *2017 International Symposium on Power Electronics (Ee)*, Oct. 2017

C2. E. Coulinge, J. Burnet, S. Pittet, and D. Dujic, "Comparative study of two-quadrant dc/dc stage in power supply for superconducting magnets," in *2018 IEEE International Conference on Industrial Technology (ICIT)*, Feb. 2018, pp. 652–657

C3. M. Papamichali, E. Coulinge, F. Freijedo, and D. Dujic, "Power supply system with integrated energy storage for supeconducting magnets," in *PCIM Europe 2018; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, Jun. 2018, pp. 1–6

Other publications, not directly related to the scope of the thesis:

O1. E. Coulinge, A. Christe, and D. Dujic, "Electro-thermal design of a modular multilevel converter prototype," in *PCIM Europe 2016; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, May 2016, pp. 1–8

2
State of the Art

This chapter presents the state of the art in the high-current low-voltage power supplies, for various applications with a particular focus on the superconducting magnets where the specific challenges related to the particle accelerator applications are assessed. The specific case of CERN is detailed where a larger picture at the system level is introduced in order to get a good understanding of the environment surrounding the power supply.

2.1 State of the Art

High-current low-voltage power supplies are a niche in the power supply domain. The output range of the power supply is a constraint given by the nature of the load, and only a few specific applications are demanding a high-current with a very low voltage. This implies a load with a very low resistance, such as the one for welding systems, the more advanced inductive loads that use superconductivity or the process of electrolysis which force a non-spontaneous chemical reaction by applying a DC current. The classical topologies and challenges for those specific applications are detailed in the next paragraphs, an illustration of their practical use is depicted in **Fig. 2.1**.

The voltage class of an generic electricity supply is defined by the international standard International Electrotechnical Commission (IEC) *60038:1983*, where in the DC voltage range, the low voltage is between 120 V and 1500 V and extra-low voltage is everything below 120 V. In the following review, this voltage range is considered jointly with a current rating above 100 A.

(a) (b) (c)

Fig. 2.1 Photos of various industries involving the use of high-current power supplies (a) arc welding technique, welder in action, (b) primary casting of the aluminum, last step of the *Hall-Héroult* smelting process and (c) production line of chlorine through *chlor-alkali* process in Rotterdam.

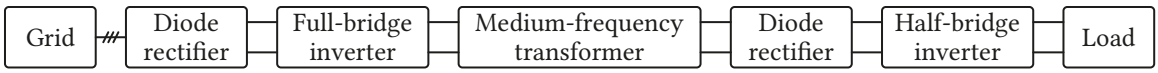


Fig. 2.2 Conventional structure for an arc welding inverter.

2.1.1 Welding

The welding process consists in joining materials by meting the parts together using a process generating a high heat. One particular technique of welding is the arc welding as depicted in **Fig. 2.1(a)**, which is used to join metal to metal where the source of heat is based on an electrical pulse [31].

As the name suggests, an electrical arc is created between an electrode and the base material, that is melted at the point of contact. This technique can then be divided into several specific methods depending on the gas used and the properties of the arc, such as metal/inert-gas (MIG), tungsten/inert-gas, flux-cored, submerged or plasma arc welding. The common characteristic between all of them is their reliance on a high current, which is produced by a power supply usually in the range of tens of kilo-watt, with a current rating above 100 A. A typical mobile MIG welding station for domestic use, is around 1.5 kW with an output regulated range between 32 A and 120 A depending on the set duty-cycle for a voltage rating around 30 V and a weight of 20 kg [32].

The classical structure of the power supply is given in **Fig. 2.2**, based on [33]–[35]. Even for industrial use the connection is made on the standard low-voltage AC grid, with standards rated sockets depending on the power of the supply as it is meant to be portable and used in various environments. The input stage allows to create the desired voltage level on medium frequency transformer, where the switching frequency is in the range of several tenth of kilo-Hertz. This transformer also provides galvanic isolation. A passive rectifier stage and a low frequency half-bridge inverter are the last stages before the resistive load. The output current can either be DC or AC with a low frequency, depending on the material to be welded.

2.1.2 Aluminum Smelter

The primary aluminum is the one directly produced from mined ore, opposed to secondary or recycled aluminum that is manufactured from various forms of aluminum scrap. In order to transform the raw ores into pure aluminum metal, a critical step is to force a chemical reaction at a temperature around 950 °C, this is the most energy consuming step of the process.

In order to provide the sufficient current, the power structure depicted in **Fig. 2.3** is classically implemented. Multiple of those elementary structure can even be paralleled to obtain larger ratings, and to do so phase shifted transformers are used in order to reduce the stress and harmonics on the grid [36], [37]. The rating for the industrial facility that is named the *potline* is the one that defines the power of the supply, being usually several hundreds of kilo-amperes. The electricity both helps the chemical reaction to happen and maintains the temperature of the cell around 950 °C. A rule of thumb gives a production of 7.5 kg of aluminum per day and per cell for a thousand amperes.

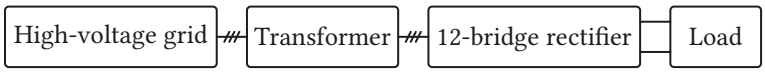


Fig. 2.3 Conventional elementary structure for an industrial aluminum smelter.

This *Hall-Héroult* process is now being used for many years, and even if its efficiency has been improved mostly by advancing the auxiliaries that treat the by-products of the reaction, the main process is intrinsically very energy demanding. This makes the process very heavy and a large consumer, so much so that in some countries, exemptions on the renewable energy targets are given. To meet those requirements, the installation relies on a higher voltage grid for its supply and can even be used to regulate the electrical network demand, that is why they are located in areas with reliable and low cost energy.

2.1.3 Electrolysis

The previously presented aluminum smelting process is actually a particular case of electrolysis named electro-metallurgy. Electrolysis which consists in the passing of a direct electric current through an ionic substance that is either molten or dissolved in a suitable solvent, produces chemical reactions at the electrodes and decomposition of the materials.

According to Faraday's first law of electrolysis, as summarized by its mathematical form in (2.1), the amount of produced material at an electrode during an electrochemical reaction is directly proportional to the average current multiplied by the total time.

$$m = \frac{Q \times M}{F \times z} \tag{2.1}$$

Where m is the mass of substance interacting at the electrode, Q is the total electric charge that passes through the substance, M is the substance molar mass, F the Faraday constant and z the valence of the substance ions. This process is used at large industrial scale, as depicted in **Fig. 2.1(c)**, to produce chlorine, sodium hydroxide, oxygen, hydrogen, and many mores.

The role of the current is at the very heart of this process, making it very demanding when rated up to the industrial level. At this scale, the reliability of the power supply must be guaranteed, and simplicity is again key. The structure is classically very similar to the one presented in **Fig. 2.3**, and even though DC current should be regulated, the precision is not imposed, because of the inertia and the time constants involved. That is also a reason why those facilities can be used to mitigate the grid consumption.

The high-current rectifier is the power supply of choice for those industrial class applications, such as any furnace linked industry or chemistry processing. Typical products from ABB, as the medium current rectifiers or the high current rectifiers families, satisfy this electrochemical and electro-metallurgy industries demand. Their rating can go up to 220 kA with a wide range of voltages, up to 2 kV [38], [39]. There is the possibility to parallel connect the units in order to reach even higher current level, as for this case example of 500 kA [40].

2.1.4 Particle Physics

Another very specific but different activity compared to the previous applications is the use of high-current low-voltage power supplies in the particle physics domain, where a strong magnetic field that interacts with the charged particles needs to be generated. Once again, the range of applications in this field is wide, from particle detectors [41], to specific magnets or superconducting magnets [42], [43] or even fusion applications [44], [45].

In that area, as every application is very unique, the topology is adapted and there are no global standards on the design of such power supplies. As most of the industrial application already presented, the reliability of the system is the highest on the priorities list. Additionally, the high current precision is a particular goal that any particle physics related power supply needs to achieve. As the current is the quantity that defines the magnetic field, which directly affects the trajectory of the particle, this should be finely controlled at all time. To this extent, some elements are always present in one form or another: a transformer for galvanic isolation, usually in the medium frequency range, a high precision current measurement device, classically a DC Current Transformer (DCCT) and some kind of redundancy in order to reduce the downtimes.

The case study on which the thesis project focuses is a particular set of superconducting magnets within CERN LHC, the design and the commonalities of their high-current low-voltage power supplies is reviewed here after.

2.2 Existing Technologies at CERN

CERN LHC experiment relies on superconducting magnets to accelerate, bend, focus and keep control over the particle beam. The role of the superconducting magnet power supply is to provide reliably a large amount of current in a controlled way and with high precision, because any variation in the delivered current impacts the magnetic field which in turn affects the particle trajectories, which could lead to a premature stop of the experimental run. Quantitatively, 10 parts-per-million (ppm) is the targeted precision for the power supplies, which means 2 mA on a 2 kA power supply. Consequently, in order to maintain a steady operation, both precision and reliability are important.

To achieve both of those objectives, parallel connection of elementary *sub-converters* is often used to reach the desired ratings and take advantage of the modularity in terms of redundancy and interleaving to improve the electrical characteristics of the output waveforms of the power supply. Additionally, a not limited list of other aspects should be considered during the design phase of any CERN dedicated power supply.

The overall volume of the system should be kept low, because of their specific locations that the power supplies could be installed in, for example a confined space in an underground area or a technical gallery. Such kind of restricted emplacement imposes the need to carefully manage the losses as the heat should be evacuated by the dedicated water cooling system or the ambient air circulation system. For instance, the use of soft switching technique [11], [13], [46] helps to minimize switching losses in semiconductors. Another consequence that follows the limited access positions of the power supply imposes a very high availability of the power systems in order to maximize the operational time of the infrastructure with no human intervention.

In terms of safety, the grounding of the magnets requires a galvanic isolation inside the power supplies and the norm Electromagnetic Compatibility (EMC) *IEC61000* level 4 must be respected because of the proximity with other sensitive systems like cryogenic instrumentation or quench protection systems. Finally, the impact on the CERN power grid should be considered and techniques for peak shaving and perturbation rejection are favored.

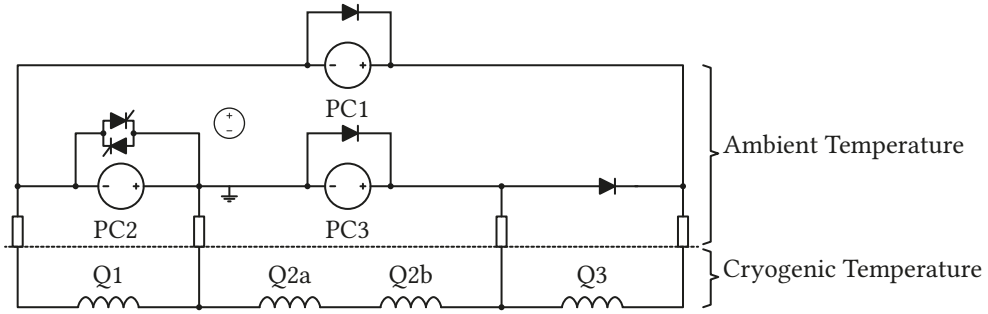


Fig. 2.4 Actual *Inner-Triplet* powering scheme. The *Inner-Triplet magnets* is composed by a series of four magnets named Q1, Q2a, Q2b and Q3, powered by three nested power supplies PC1, PC2 and PC3 and with some additional free-wheeling diodes.

Tab. 2.1 *Inner-Triplet magnets* power supply specifications.

Supply name	Ratings		Operation	Cooling
	Voltage [V]	Current [A]		
PC1	+ 8	+ 8000	1-quadrant	Water
PC2	+ 8	+ 6000	1-quadrant	Water
PC3	± 10	± 600	4-quadrant	Water, forced air

The case study of this thesis is about a set of magnets named *Inner-Triplets magnets* whose role is to perform the last focusing of the particle beam before the interaction points, where the collisions happen. Presently, to power those magnets, two families of switch-mode power supply have been developed: a 1-quadrant type for the main circuit and a 4-quadrant type to locally trim the current across one magnet [47], [48]. Their actual powering scheme is provided in **Fig. 2.4**, and the power supply parameters are gathered in **Tab. 2.1**. They are arranged in a combination of three nested converters to feed the current in the series of four magnets. They operate as current controlled voltage source whose command signal comes from the control center and is processed through a decoupling matrix to give their individual set-point. The overall electrical system can be seen as voltage sources feeding a standard *RL* load, where the *R* comes from the copper cables and the *L* from the superconducting magnets.

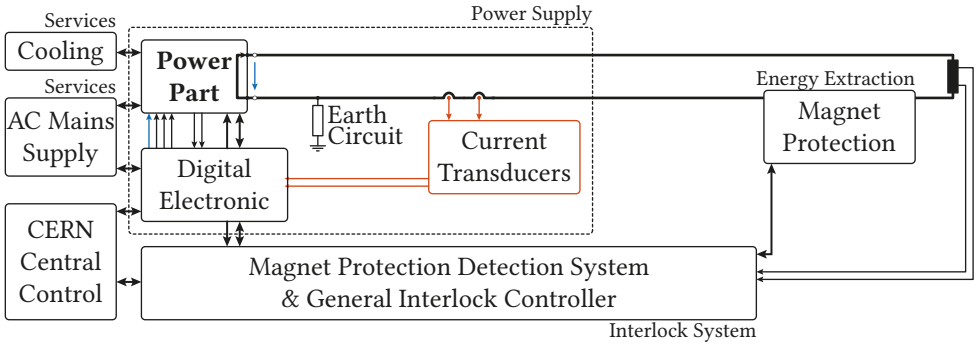


Fig. 2.5 Simplified integration of power supplies. Thin line represents signals while thick ones represent power exchange between entities.

More generally for the CERN designs, the power part is always integrated as depicted in **Fig. 2.5**. As the current measurement is a critical part to reach the precision level, it is done internally with redundant DCCTs and is used to feed the Digital Electronic controller. This one is in charge of the regulation, and it takes its reference comes from further up, via the CERN Central Control which defines the operating point of all the systems according to the experimental run to perform. The most important services that surround the power supply are the AC supplies for main power and auxiliaries supplies, as well as the cooling, which can be air or water based depending on the location and the power rating of the supply. Finally a set of protection features are mandatory and implemented to provide safety for both equipment and personal. The earth monitoring circuit measures the current to the ground from the main current loop and the magnet protection systems are present to extract the energy in case of quench (when the superconducting state is lost locally in the magnet).

A selection of the most widely spread high-current low-voltage power supplies used in CERN installations are grouped in **Tab. 2.2** and their topologies are presented in the following paragraphs.

2.2.1 1-Quadrant Power Supply Family

The family of 1-quadrant power supplies is designed in modular fashion, with many *sub-converters* in parallel. Each input module has a simple diode rectifier, providing a DC link voltage to the full-bridge soft-switched inverter of a DC-DC converter. To give a feeling of the size of such converters, picture of their final implementation in racks, including control, auxiliaries and bus-bars is given in **Fig. 2.6**.

Tab. 2.2 The high-current low-voltage power supplies already existing at CERN.

Converter	Type	IN		OUT		Power module		Section
+4;+6;+8 kA, +8 V	1Q	3~ 400 V	100 A	+8 V	+4;+6;+8 kA	+8 V	+2 kA	**Sec. 2.2.2**
+13 kA, +18 V	1Q	3~ 230 V	420 A	+18 V	+13 kA	+18 V	+3.25 kA	**Sec. 2.2.3**
±60 A, ±8 V	4Q	3~ 230 V	1.2 A	±8 V	±60 A	-		**Sec. 2.2.6**
±600 A, ±10 V	4Q	3~ 230 V	16 A	±10 V	±600 A	-		**Sec. 2.2.5**

(a) (b)

Fig. 2.6 Photos of the complete high-current 1-quadrant power supply presented in the following paragraphs (a) 6 kA; 8 V and (b) 13 kA; 18 V.

2.2.2 2 kA Based Converters

This family is designed as a 1-quadrant, positive voltage, positive current converters. It is constructed on a modular architecture relying on 2 kA sub-converters, which is easily scalable to 4, 6 or 8 kA with an output voltage of 8 V. This design is based on the elementary *sub-converter* depicted in **Fig. 2.7**, where the galvanic isolation is achieved by means of several medium-frequency transformers, connected in series on the primary side, with center-tapped rectifiers connected in parallel on the secondary side. The output of each rectifier features in this case a second order low-pass filter providing attenuation of the voltage ripple.

As it can be seen from the output module, the parallelization is heavily used to obtain the current rating. The current is only measured once per output module (red arrow), and the stage relies on the symmetry for the sharing between the four parallel branches, no active balancing is performed. Having multiple rectifier output stages ease the design of the magnetic parts, allowing to use lower-rated fuse for the protection of the whole system, and bring the high availability required: such a module can be up and running even if a secondary is fused out. Modularity greatly helps for the assembly and maintenance of the complete system, keeping the form factor of basic building block rather compact, and enabling the quick swap of module in case of fault.

Regarding the control and regulation, the *sub-converter* can be considered as a high-frequency current source, which is regulated by a 1 kHz bandwidth voltage loop, and where the phase-shifted PWM operates at 20 kHz. Some additional details about this family of converter is given in **Tab. 2.3**. Then several of those*sub-converters*are parallelized to achieve higher currents, when this is done, an active $N + 1$ redundancy is implemented: e.g. a 6 kA power supply is composed by four elementary 2 kA sub-converters.

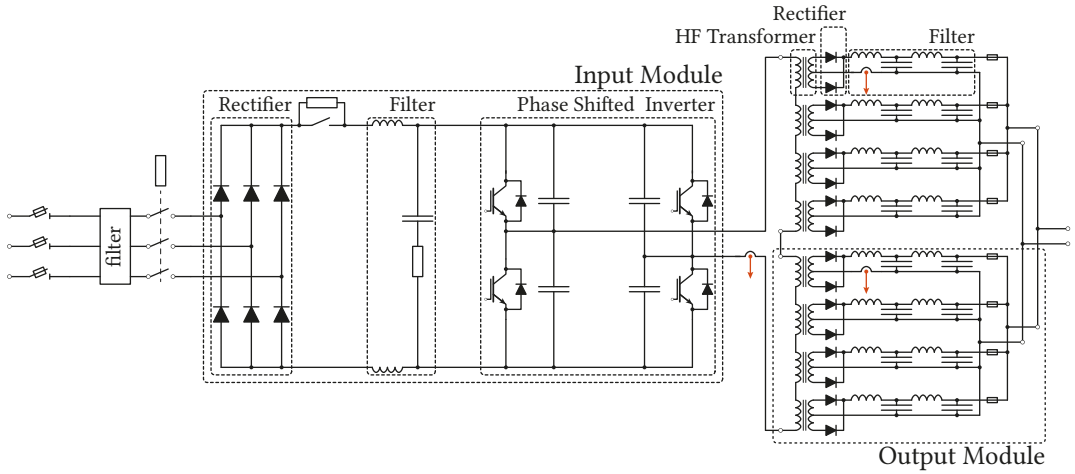


Fig. 2.7 Simplified architecture of the power *sub-converter* 1-quadrant, 2 kA, 8 V.

Tab. 2.3 Details about the 1-quadrant, 2 kA based family that compose the 4 kA; 6 kA; 8 kA, 8 V converters.

Cooling	Accuracy			Developer	Manufacturer
Water	5 ppm @ 30 min	10 ppm @ 24 h	70 ppm @ 1 yr	Kempower	Kempower

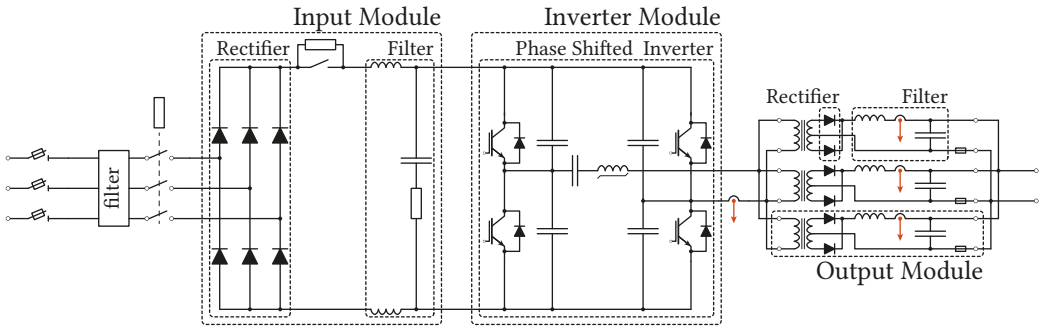


Fig. 2.8 Simplified architecture of the power *sub-converter* 1-quadrant, 3.25 kA, 18 V.

Tab. 2.4 Details about the 1-quadrant, 3.25 kA based family that compose the 13 kA; 20.5 kA, 18 V converters.

Cooling	Accuracy			Developer	Manufacturer
Water & forced air	3 ppm @ 30 min	5 ppm @ 24 h	50 ppm @ 1 yr	Transtechnik	Transtechnik

2.2.3 3.25 kA Based Converters

This family of converters is very similar to the one previously presented. A 13 kA 1-quadrant, positive voltage, positive current converters with scaled up ratings for the sub-converter: 3.25 kA, 18 V, depicted in **Fig. 2.8** and which is constructed in the same fashion as the 2 kA one. Additional details about this family of converter is given in **Tab. 2.4**. A unique converter of 20.5 kA has been realized for a specific project, based on the same modules, with a greater number of them in parallel.

2.2.4 4-Quadrant Power Supply Family

When a power supply is characterized as a 4-quadrant one, it is restricted to the output stage, the power supply has no ability to feed back power to the grid. Nevertheless, locally in the output stage, the current can flow in both direction and the voltage be any polarity. This is a way to have a more flexible control on the load. As the rating of this family of power supply is lower, because they are only used as correctors on the magnet current, they rely less on parallelization and can be integrated in a single module as shown in **Fig. 2.9**.

(a) (b)

Fig. 2.9 Photos of the 4-quadrant power supply presented in the following paragraphs (a) ±600 A; ±10 V and (b) ±60 A; ±8 V.

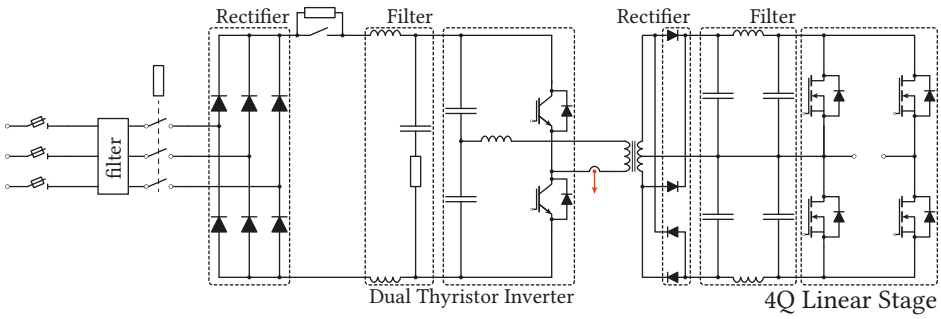


Fig. 2.10 Simplified architecture of the 4-quadrant power sub-converter, ±600 A, ±10 V.

Tab. 2.5 Advanced details about 4-quadrant, ±600 A, ±10 V converter family.

Cooling	Accuracy			Developer	Manufacturer
Water & forced air	10 ppm @ 30 min	50 ppm @ 24 h	200 ppm @ 1 yr	EEI-CIRTEM	EEI-CIRTEM

2.2.5 600 A Power Supply

The topology of a 4-quadrant power supply is very similar to the previously described 1-quadrant topology, where the output ratings are 600 A, 10 V, and is presented in **Fig. 2.10** with some additional details in **Tab. 2.5**. The input stage is rather identical up to the medium frequency transformer, then the output stage is a combination of a center-tapped passive rectifier and a 4-quadrant linear stage, which uses MOSFET in their linear region of operation to dissipate the recovered energy.

The voltage source is based on a variable switching frequency, between 50 kHz and 200 kHz half-bridge resonant topology followed by a linear stage. This topology gives a very low output EMC noise, at the cost of control complexity.

The output is designed around a linear stage relying on power MOSFET which provide the 4-quadrant operation. They behave as gate voltage controlled current source. In this case, the power supply is not recovering any energy from the load, but it is dissipated as heat inside the power semiconductors. More recently, redundancy feature and tolerance to radiation has been developed by CERN for this type of converter [49]. While the efficiency of this kind of system is not very high, this method guarantees the precision and accuracy in operation.

2.2.6 60 A Power Supply

This converters adopt a similar topology as the 4-quadrant 600 A, with some additional filtering and a crowbar for the dissipation of the energy recovered from the magnet. Its complete topology is illustrated in **Fig. 2.11**, additional details are given in **Tab. 2.6**.

Tab. 2.6 Advanced details about 4-quadrant, ±60 A, ±8 V converter family.

Cooling	Accuracy			Developer	Manufacturer
Forced air	50 ppm @ 30 min	100 ppm @ 24 h	1000 ppm @ 1 yr	CERN	CEL

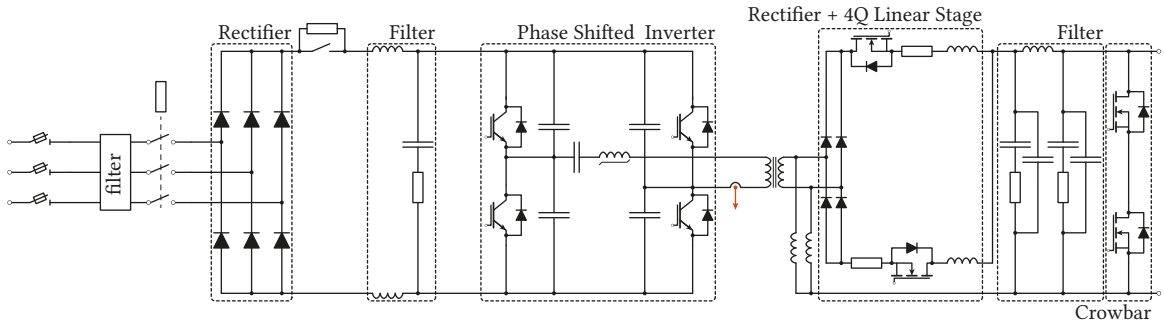


Fig. 2.11 Simplified architecture of the power *sub-converter* 4-quadrant, ±60 A, ±8 V.

2.3 Summary

In this chapter a wide variety of power supply is presented, where all of them have a role to feed the dedicated load with high current. Those loads are very specific, mostly part of some industrial complex or advanced research facilities. With a focus narrowed down to the CERN case, the family of high-current supplies for superconducting magnets is detailed, being either 1-quadrant or 4-quadrant and dissipating the recovered magnetic energy. To complete these existing solutions and to follow the operational constraints imposed by the new powering scheme of the *Inner-Triplets magnets*, there is a need for a 2-quadrant operating power supply that integrate energy storage instead of dissipation. Those solutions are presented in the next **Chap. 3**.

3
Energy Storage Integration

This chapter details the power supply structure and explore the possibilities to integrate an energy storage system in the specific case of the Inner-Triplet magnets powering for HL-LHC. The definition of the storage requirements is established and a brief overview of the energy storage technologies is performed. Findings of the study reveal that the battery based solutions are the most suited for the dedicated application.

3.1 Power Supply Concept

The role of the power supply, from a system level point of view, is to interface the load to the grid providing galvanic isolation and giving the possibility to recover part of the energy stored in the load. This concept is depicted in the block diagram in **Fig. 3.1**. The grid and the load are perfectly known and assumed to be ideal. On one side, the grid is considered to be 400 V three-phase AC lines, outputs of a 18 kV, 2 MVA distribution transformer. On the other side, the load combines the *Inner-Triplet* super-conductive magnets, the super-conductive link, the electrical feed-box that interfaces traditional and superconducting circuits, and the copper cables at the output of the power supply. Thus it can be considered as a simple *RL* equivalent circuit where R is only defined by DC cables. Quantitatively, L is 255 mH and the considered value of R is 0.13 mΩ, this value is frozen during the course of the thesis to be independent from the evolutions of the project that is tunning the values according to the work packages inputs and developments.

3.1.1 Operational Cycle

Particle accelerators are characterized by a cycling way of operation where the operational cycle is well known and predictable when no unforeseen events occur. For the system of interest, the *Inner-Triplet magnets*, an overview of the defined cycle is given in **Fig. 3.2**. As it can be seen, after an initial ramp-up of the magnets current during approximately 20 min at a given rate of 16 A s^{-1}, the steady-state current value is regulated for several hours as collisions are happening for as long as the beam quality is good enough for the experiments to collect data and no problem appears anywhere else in the accelerator. The average duration of this phase is around 12 h.

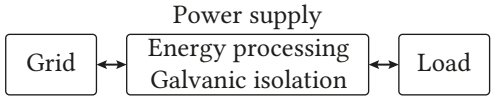


Fig. 3.1 Block diagram of the power supply at the system level. The galvanic isolation is necessary because the magnet is grounded for safety reasons.

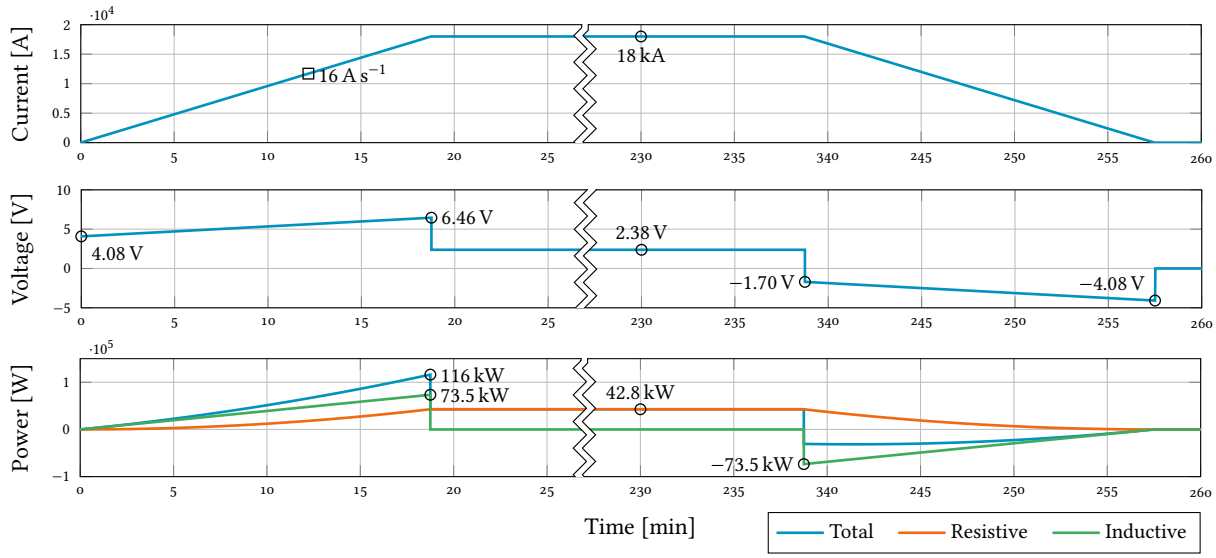


Fig. 3.2 Current and voltage profile of a typical cycle for the *Inner-Triplet magnets*, with a cable equivalent resistance of 0.13 mΩ, corresponding to 20 m of water cooled 2600 mm^2 copper cables.

As particles are present in the experiment the precision must be guaranteed at all time during those previous operational phases. The last phase of the cycle is the ramp-down.

Finally, when the ramp-down procedure is triggered, the magnet current should be lowered to its standby level in a similar time as the ramp-up time of 20 min. As there are no more particles circulating in the experiment, the precision is less critical during this phase. As the future power supplies for HL-LHC upgrade will be located in underground galleries, closer to magnets, the cable resistance is removed from the equation. Thus there is a need to apply a negative voltage across the magnet to force the ramp-down of the current.

Thanks to this cycling operation, there is the possibility to reuse the recovered energy during the ramp-down phase of the cycle for the next ramp-up, or even injected it (this energy) back to the grid. It is worth providing a few energetic considerations about the cycle presented in **Fig. 3.2**. While taking into account specifications of the magnet, the calculation presented in (3.1) is performed to get the amount of magnetic energy stored in the load.

$$1/2 \times L \times I^2 = 1/2 \times 0.255 \times (18.10^3)^2 \simeq 40\,\text{MJ} \tag{3.1}$$

This represents the amount of energy to ideally recover in each cycle, that could be then processed elsewhere in the system or used for the next cycle. Evidently certain amount of energy will be lost in the resistance of the system, and the goal is to have the power supply as efficient as possible to reuse most of that energy. The benefit of having an energy storage inside the power supply leads to a better controllability of the power flow, allowing a peak shaving of the input power which could have a major impact on the infrastructure of the electrical grid side: the power coming from the grid side is rated to cover the losses in the system (resistive power in **Fig. 3.2**), whereas the inductive power needed during the transition phases is handled by the local energy storage element. This is the opportunity to downsize the input power compared to the peak power of the power supply, which is a feature that CERN highly values.

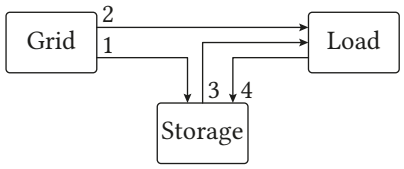
The goal of this part is to size the storage to handle the inductive part of the power whilst the input stage of the converter is rated for the resistive power during the flat-top. A consideration on the inductive power and its associated energy is given in **Sec. A.1**.

To put this number into perspective, 40 MJ is the energy of 1 L of oil, or 11 kW h of electricity which represents a monetary value of around 2 CHF in the very idealistic case. Over the lifetime of the power supply, the financial value of the recovered energy is not to be considered of great importance. The shift towards the new solution with local energy storage is a decision driven by controllability and scale of the input infrastructure rather than the raw monetary argument.

3.1.2 Requirements

Considering the CERN specific requirements, electrical performances, reliability, modularity and availability are the most important key performance indicators, thus representing the priorities when it comes to a new design. The developed 2-quadrant power supply has to comply with the integration scheme previously presented and has to consider the operating cycle of **Fig. 3.2** as nominal. The requirements can be summarized as:

- Peak output power rating: 180 kW.
- Input power rating: minimal; enough to cover the resistive losses.
- Output voltage rating: ± 10 V.
- Output current rating: +18 kA.
- Class 0 precision (cf. [22]).
- Dynamics: ± 16 A s^{-1} for a ramp-up/down in around 20 min.
- Lifetime expectancy: 20 years, accounting for 200 days of physics operation a year, and considering 1000 cycles per year; adding up to 20 000 cycles.
- Load resistance: 0.13 mΩ, which represents around 20 m of copper cables.
- Load inductance: 255 mH.
- From CERN legacy and traditional design rules, based on electrical performances and decoupling arguments, there needs to be at least one input rectifier per magnet, i.e. no DC bus sharing between several loads.
- Any failure of one module composing the power supply should not impact the load, i.e. no change in the load current; the sizing is thus based on the loss of one module, which results in a $N + 1$ redundancy philosophy.
- Innovation: implementation of energy storage capabilities in the power supply, focused on an energy efficient design.
- Mandatory feature: galvanic isolation and mitigation of the grid perturbations.



(a)

	Pre-charge	Ramp-up	Flat-top	Ramp-down
Energy path	1	2+3	2	4

(b)

Fig. 3.3 Energy flow between the grid, the energy storage element and the superconducting magnet (a) conceptual scheme and (b) strategy during the different phases of the cycle.

3.1.3 Power Flow Strategy

For any type of retained storage solution, a global strategy can be adopted regarding the power flow. **Fig. 3.3(a)** shows the possible energy flow paths between the grid, the energy storage element and the magnet, where the arrows indicate the direction of the energy flow. Based on this, **Fig. 3.3(b)** shows the paths used during each part of the cycle, for a possible energy management strategy. The goal is to take advantage of the storage to support the peak power, which is more than 2.7 times higher than the steady-state power.

During the pre-charge stage, the energy storage element receives energy from the grid in order to be prepared for the beginning of the cycle (path 1). Then, during the ramp-up, the grid supplies the active power (path 2) whilst the energy storage element takes care of the reactive power (path 3). During the steady operation, the energy is mainly provided by the grid (path 2) and, depending on its characteristics, by the energy storage element (path 3). Finally, during the ramp-down, the energy stored in the load is recovered via path 4.

3.2 Energy Recovery

There are two main approaches that can be considered for the implementation of the local energy recovery: either a fully reversible power supply that can feed back the energy to the grid, which is not *per se* a dedicated storage, or a local energy storage solution. This section explores those possibilities in detail.

3.2.1 Feeding Energy Back to the Grid

Rather than temporarily storing the energy, this more complete solution avoids the need for any local energy storage and provides full control over the recovered energy as well as the power coming from the grid. While this approach gives certain benefits from the power quality and grid support point of view, it also has certain drawbacks when considered inside the CERN environment, as there is not much possibility to mitigate the grid perturbations. A block diagram of this approach is given in **Fig. 3.4**, where blocks represent power supply functions but neglect actual technical implementation, arrows indicate the direction of the power flow. Note that isolation is mandatory and can be implemented either in the AC/DC or the DC/DC converter.

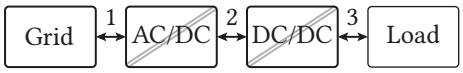


Fig. 3.4 Possible implementation of full 4-quadrant power supply, with full reversibility.

This approach is characterized by having every stage of the power supply fully bidirectional, making it a sophisticated 4-quadrant. Moreover, every stage has to be able to handle the peak power, even though the operational cycle requires this only at the end of the ramp-up, which represent only a minor portion of the overall operating time. On the cost aspects, the overall monetary value to inject energy back in the grid is negligible compared to the added complexity of the system. Finally, as the solution is already convoluted and the modular design philosophy is imposed to parallel the structure, the control becomes very fastidious moving away from robustness and simplicity.

These are some of the arguments against the approach that feeds back energy directly to the grid, as the potential gains in flexibility and control of the power flow are drowned by its complexity - such kind of power supply is over-dimensioned, because peak power is only needed for a limited amount of time in the normal cycle and only a 2-quadrant operation is necessary for the application. This contrasts with the simplicity, reliability and availability that are highly valued for the design of the power supply, considering particularities of the application.

3.2.2 Storing and Reusing Energy

In this second approach, there is a net gain in using a local energy storage solution as it can act as an energy buffer between the grid and the superconducting load, providing flexibility in the powering strategy, peak shaving as well as robustness to grid perturbations. This then implies that the sizing of the different stages can be made accordingly to their worst case stress. This stress directly depends on the energy storage position and operating voltage, these two parameters add degrees of freedom in the structure of the converter that impacts its overall design. Finally, the energy storage can be modularized to respect the requirements in terms of availability and redundancy.

In terms of operation, only the stages between the load and the energy storage need to be reversible, making the global power supply only 2-quadrant. The arrows in the block diagram of the power supply in **Fig. 3.5** indicates the direction of the power flow. The galvanic isolation needs also to be implemented in one of the converter interfacing the storage to the grid or the load.

The main benefit of having an energy storage locally in the power supply is to shave the power peaks of the input power which could have a major impact on the infrastructural cost for the electrical grid side. With this configuration, the grid size converter remains passive and with reduced ratings, compared to a fully bidirectional solution. The required peak power on the grid side can be reduced to the power needed to cover the losses during the steady-state operation.

This local storage of energy is certainly the preferred solution. Nevertheless, the way for it to be implemented defines the global structure of the power supply. This point is now further investigated, with the description of the advantages, drawbacks and requirements for the various topologies regarding the battery position, as well as converters sizing considerations.

Fig. 3.5 Implementation of 2-quadrant supply, with energy recuperation functions, integrated inside the main power flow.

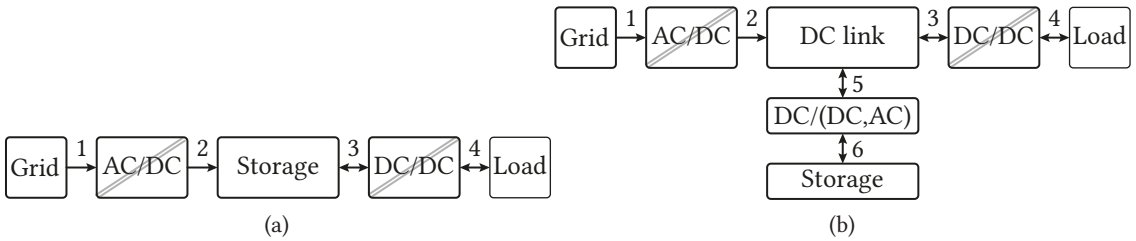


Fig. 3.6 Implementation of 2-quadrant supply with energy storage (a) integrated inside the main power flow and (b) integrated outside the main power flow.

3.2.3 Connection of the Energy Storage

Within the local storage solutions, several implementations can be identified, considering the energy storage that are either inside or outside the main power flow. On the one hand the energy storage element can be directly integrated in the main power path, as presented in **Fig. 3.5**, where it is used as a direct buffer between the grid and the load. The storage element could be charged from the grid independently of the load behavior, through the input AC/DC converter of reduced ratings. In this case, the input AC/DC converter has to be able to regulate its output voltage in a given range, defined by the choice of the energy storage technology. On the load side, the DC/DC converter stage has to provide bidirectional power flow and must be sized for the full power.

On the other hand, there is a way of implementing the storage outside the main power path, as depicted in **Fig. 3.6(b)**. This allows to split the power delivered to the load: one part can be provided directly from the grid and the other part can be provided by the energy storage element. The interface between the energy storage element and the DC link is made through a dedicated converter. This DC/(DC,AC) energy storage dedicated converter, depending on the nature of the energy storage, can be relaxed on its specifications since it only operates during a small fraction of the cycle, mainly during the ramp-up and ramp-down phase.

As already defined, the supply comes as three-phase 400 V lines from a CERN distribution transformer. The first stage of power electronics is a rectifier that is used to create a high-voltage DC-bus and is the same in all the possible implementations of the storage. Having a classic passive diode rectifier, because there is no need for reversibility, brings the voltage level on the bus to approximately $400 \times {}^{3\times\sqrt{2}}/_{\pi} \simeq 540\,\text{V}$. It also complies with the simplicity and reliability criteria for the new design.

The definition of the storage requirements are defined later in **Sec. 3.3**, keeping the nature of the storage very generic for the following study.

3.2.3.1 Storage on the High-Voltage DC Link

In the first approach, presented in **Fig. 3.7**, the storage is integrated right after the primary stage of the converter, on the high-voltage DC bus. Depending on the voltage level of the energy storage system, it can either be directly integrated on the DC link or interfaced through a converter that adapts the voltage level and could even accept a AC storage technology. This solution allows for reduced current in the storage element as the DC voltage of 540 V is well above the output voltage rated 10 V. The output DC/DC should then provide both galvanic isolation and reversibility as well as be rated for the full power.

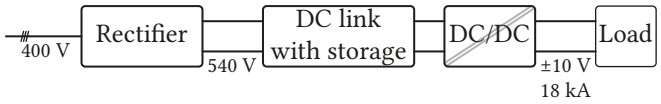


Fig. 3.7 Implementation of the local storage on the high-voltage DC link of the power supply.

In order to provide the required galvanic isolation, a medium frequency transformer needs to be integrated in the power supply which is the opportunity to interface the storage element.

3.2.3.2 Storage on a Separate Transformer Winding

This approach, depicted in **Fig. 3.8**, is inspired by Multi-port Energy Gateway (MEG) [50] which provide galvanic isolation and adaptation to different voltage levels, interfaced using a multi-windings transformer, which is the key part of the design. The surrounding converters are then operating as resonant ones, in order to limit the system losses, keeping the efficiency high. All the power paths can be considered, even the hybrid ones when the grid side supplies both the storage and the load. This is a very flexible solution, but it adds complexity to the control as well as some constraints to the hardware, for example, the sizing of the resonant tanks for a broad operation range.

This solution relies on a complex transformer design, and requires to have two converters to interface the storage to the load. When this kind of transformer interfaces high-voltage and low-voltage levels, the transformer cannot be optimized for both, and would only be optimal for one port, it would then be sub-optimal in terms of losses and volume for the other ports. Additionnaly care should be taken when coupling different converters on the same transformer core regarding the saturation and insulation levels depending on the voltages of the ports.

Investigating the position of the energy storage in the power supply, with the goal to get a high efficiency, invites in having it as close as possible to the load, leading to the option presented next.

3.2.3.3 Storage on the Low-Voltage DC Link

This solution represents the one where the energy storage is the closest to the load, and is depicted in **Fig. 3.9**. The rest of the topology is given in detail in order to show the different stages, from the simple passive diode rectifier, followed by a DC/DC which includes a medium-frequency transformer in order to provide galvanic isolation as well as adapting the voltage level to the low voltage DC link with storage capabilities. Once again, depending on the technology of the storage, it can either be directly on the link or interfaced through a dedicated converter. In this solution only the last stage converter has to handle the full power.

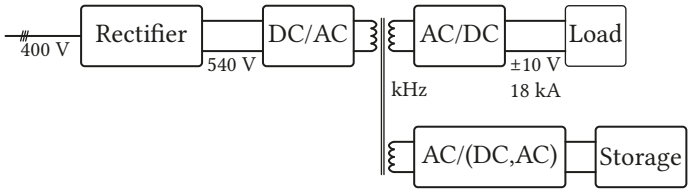


Fig. 3.8 Implementation of the local storage on a multi-port medium frequency transformer of the power supply, providing both galvanic isolation and voltage level adaptation.

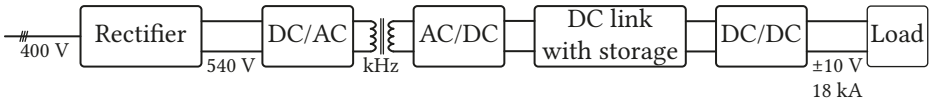


Fig. 3.9 Implementation of the local storage on the low-voltage DC link of the power supply.

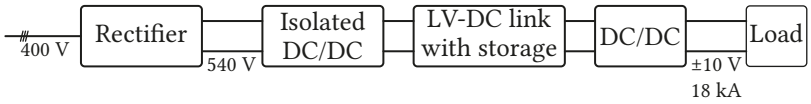


Fig. 3.10 Adopted implementation of the power supply with the storage on the low-voltage DC link.

3.2.4 Adopted Structure

The further the storage is from the load, the more complexity is added to the topology, as more stages should be reversible. Moreover, the further it stands from the load, the poorer the efficiency, as the round trip cycle involves more conversion stages. As the overall incentive to shorten the resistance of the load by shortening the copper cable is to gain in efficiency, the objective of the power supply must be aligned with that. Thus in order to minimize the losses in the conversion stages, the storage element is placed directly on the low-voltage DC link, as depicted in **Fig. 3.10**.

The first stages of the power supply remains fairly traditional with a passive rectifier and an isolated DC/DC converter, which does not need to be reversible. The solution with an H-bridge, medium frequency transformer and passive rectifier seems like the simplest and proven one. There is not much area for improvement in those stages.

Nevertheless, the integration of storage as well as a 2-quadrant converter able to process high-current from the low-voltage DC link is a challenging part. As the output voltage is rated at a maximum of 10 V, this DC link is not to exceed the 100 V, remaining in the *extra-low voltage* category as defined by the IEC [51].

In this approach, the main considerations regarding the storage element: nature, technology, voltage level, optimal cycle, and the output DC/DC converter which should be able to handle the 20 kA under a very low voltage. The storage aspect is addressed in the following sections of this chapter while the converter stage part is developed in the upcoming chapters, as this is the core part of the converter, it is the one to lead the sizing and split of the power supply into elementary blocks.

3.3 Energy Storage Technology

A thorough study about the energy storage technologies is conducted based on the *Inner-Triplet magnets* nominal cycle as case study, where the two competing technologies are considered supercapacitor and battery, in particular lithium-ion batteries. For this analysis, the two main parameters to be taken into account are the energy and the power, or the energy density and the power density.

The supercapacitors are considered because of their higher power density compared to batteries, which also come at the price of a lower energy density than the batteries but higher than traditional capacitors. This is illustrated in **Fig. 3.11**, by a Ragone plot that allows to compare the energy storing technologies. For the sake of completeness, different technologies are shown but are not considered in the study because of their lack of availability and complexity to be integrated.

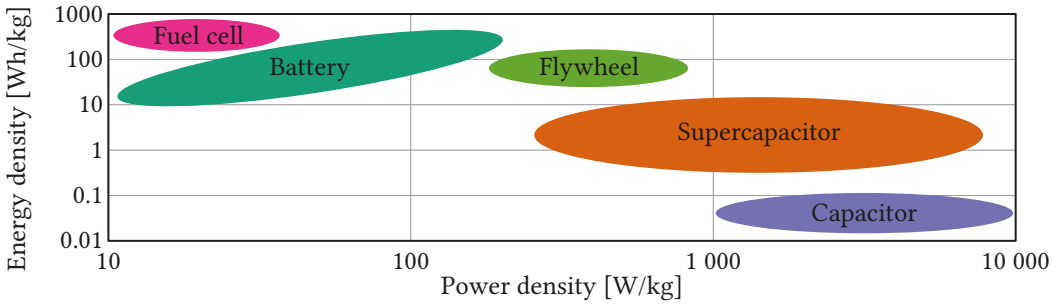


Fig. 3.11 Ragone plot of various energy storage technologies.

The use of supercapacitors has already been investigated in fast pulsed cycling particle accelerator in [52], [53], but the LHC follows the operating cycle previously described because of the superconducting nature of the magnets. The hypotheses for the power flow and the energy requirements are then completely different and the sizing of the storage is done hereafter.

3.3.1 Supercapacitors

The supercapacitor technology is the suitable choice for storing and releasing large amounts of power relatively quickly. Even though the targeted area is high power application, supercapacitors are also applicable in low power applications, where batteries have insufficient lifetime performance. Supercapacitors use in today's industry is very broad, such as consumer electronics, energy harvesting or transportation.

In the capacitor range of components, depending on the material between the electrodes [54], three types can be distinguished: electrostatic, electrolytic, electrochemical. The latter one is of interest for the focus of the study, where the supercapacitors belong. Depending on the way the energy is stored inside the component, the distinction can be made between double-layer capacitors, pseudo-capacitors, and hybrid ones.

As the most common and proven supercapacitors are double-layer capacitors, this is where the focus is set. The working principle is based on the Helmholz layer: the energy is stored in an electrostatic form: the charges are separated in the regions of the two electrodes and not transferred.

3.3.1.1 Structure and Principle of Operation

The capacitance is given by (3.2), where ϵ is the electric constant, A is the surface of the electrodes and d is the distance between the polarized charges. Supercapacitors are constructed by two electrodes, the material of which plays a key role for the high capacitance capability, typically it is carbon based. The important characteristic of the electrode material is its porosity, which defines the apparent surface: increasing the surface means increasing the capacitance.

$$C = \epsilon \times \frac{A}{d} \tag{3.2}$$

Moreover, the charges are separated via the electrode-electrolyte interface at the two electrodes, hence the name *double-layer* capacitors, where the distance is in the order of magnitude of Å (Angstrom). Those two factor combined allow to reach very high capacitance values.

Fig. 3.12 Structure of a supercapacitor.

The supercapacitor structure is presented in **Fig. 3.12**, it includes also an electrolyte, which fills the porosities of the two carbon electrodes, the used material can be organic, aqueous or polymer. The energy is stored in the supercapacitor by polarizing the electrolytic solution: it is charged by ions moving to the carbon surface of the electrode and discharged by ions moving away from the carbon surface.

Finally, the two electrodes are mechanically separated by a separator, which is an ion-permeable membrane insulating electrically electrodes and supporting the charge transfer.

3.3.1.2 Equivalent Electrical Circuit

There is an effective way to implement the behavior of the supercapacitor in simulation [55], based on a simplified *RC* network model, with an internal DC resistance and a linear voltage-dependent capacitance, as depicted in **Fig. 3.13**. This model neglects the transient phenomena of different time constants due to the electrode porosity of various depths and is applicable in studies, where the energy stored is the factor of importance, such as the application considered in this study.

The quality of the deposits from the porous materials on the metallic sheets which creates the electrodes is the cause of the Equivalent Series Resistance (ESR) of the supercapacitor. This parameter is provided by the supplier and is determined, along with the capacitance value, based on the assumption that the supercapacitor can be modeled as a simple series *RC* circuit.

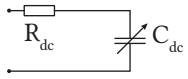


Fig. 3.13 Equivalent electrical circuit of the supercapacitor.

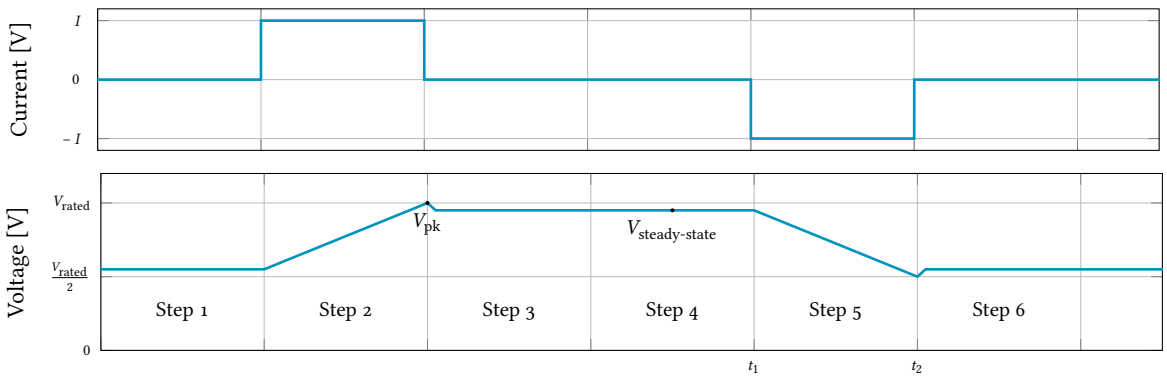


Fig. 3.14 Six-step process that allows to determine the characteristics of the supercapacitor, R_{ESR} and C.

During the characterization testing, the charge/discharge steps have to at least include the range from half to rated voltage. In the manufacturer application note [56] this *six-steps process* is based on a succession of charge, discharge and open circuit operation, as depicted in **Fig. 3.14**, where the ESR is computed during the discharge process as in (3.3).

$$R_{\text{ESR}} = \frac{V_{\text{pk}} - V_{\text{steady-state}}}{I} \tag{3.3}$$

The rated capacitance, as provided by suppliers is found through the same procedure and computed thanks to (3.4).

$$C = \frac{I \times (t_2 - t_1)}{V_{\text{rated}}/2} \tag{3.4}$$

The internal structure of the supercapacitor is affected by an increased accumulation of charges. It presents a non-linear charge-voltage characteristics, which leads to a capacitance of variable nature depending on the voltage [55]. At zero voltage, the supercapacitor has a base capacitance, C_0, and as the voltage increases, the capacitance increases in an approximately linear fashion. Within the recommended operational range it can be approximated by a linear law as $C(V) = C_0 + k \times V$, where C_0 is the initial capacitance at $V = 0$ and k is the parameter describing the linear relationship.

A possible explanation is the existence of two diffusion layers within the electrolyte, each directly in contact with each of the two double-layers. Each of these diffusion layers has a capacitance, whose value is inversely proportional to their size. When the voltage at the terminals of the supercapacitor increases, the size of the diffusion layers is reduced, which leads to an increase in its capacitance.

The linear dependence on the voltage is an approximation which can improve the modeling by 10 %, compared to the constant capacitance approximation. The parameter of the voltage-dependent capacitance is not given by manufacturers and should ideally be determined by experimental results.

Supercapacitor cells are components of low voltage, typically rated between 2.3 V and 2.8 V. Thus, in order to satisfy the voltage requirements, the components are placed in series. However, due to tolerance differences between manufactured cells in capacitance, resistance and leakage current, a series connection of individual cells is accompanied by an imbalance in the voltage across the cells. Thus, it is important to ensure the operation inside the recommended voltage range, in order to avoid electrolyte decomposition, gas generation, or ESR increase which ultimately reduces the life-time of the component.

The most important fact that should be taken into account while analyzing the operation and the sizing of a supercapacitor is the minimum voltage, below which the supercapacitor should not be discharged, while respecting the constant power stability limit of the device [57]. A general practice is to bound the supercapacitor discharge to half of the rated voltage [58], leading to an useful energy as expressed in (3.5). This equation also highlights the exponential relation between energy and voltage.

$$E_{\text{useful}} = \frac{1}{2} \times C \times \left(V_{\text{rated}}^2 - \left(\frac{V_{\text{rated}}}{2} \right)^2 \right) = \frac{3}{4} \times \frac{C \times V_{\text{rated}}^2}{2} \tag{3.5}$$

Tab. 3.1 Characteristics of the selected supercapacitors, and their series (S) parallel (P) combination to achieve both voltage and energy requirements.

Reference	Capacitance [F]	V_{rated} [V]	Dimensions [mm]	Weight [g]	Number of devices		
					[12; 24V]	[16; 32V]	[24; 48V]
BCAP3000 P270 K04	3000	2.70	L:138, ⌀:60.7	510	S:9, P:560	S:12, P:420	S:18, P:280
BCAP3400 P285 K05	3400	2.85	L:138, ⌀:60.7	520	S:9, P:500	S:12, P:370	S:17, P:240
ESHSR-3000C0-002R7A5	3000	2.70	L:138, ⌀:60.2	530	S:9, P:560	S:12, P:420	S:18, P:280
NE03V03400SW001	3400	3.00	L:138, ⌀:60.3	500	S:8, P:440	S:11, P:340	S:16, P:220

3.3.1.3 Supercapacitor Sizing

The voltage across the supercapacitor terminals is selected considering three different rated voltages $V_{\max}$ and their halves $V_{\min} = V_{\max}/2$. The considered cases are within the following ranges [12; 24 V], [16; 32 V] or [24; 48 V].

A selection of capacitors from two manufacturers is considered, within a similar cylindrical form factor family. This selection is presented in **Tab. 3.1** [59], [60].

The first numbers to be determined are the number of components that should be connected in series (S) to reach the voltage requirement, taking into account the reduction of the overall energy capacity value as expressed in (3.5), and the number of parallel branches (P) that should be connected to reach the energy requirement of 40 MJ. As seen in the table, it sums up to thousands of supercapacitor devices in total.

Subsequently, an estimation of the physical requirements in terms of weight and volume is conducted, and presented in **Tab. 3.2**. These results are over-scaled by a factor of 1.3, in order to account for the extra balancing electronics and the mechanical support of the structure.

Those numbers allow to get the order of magnitude of physical dimensions needed to satisfy the requirements of the nominal operating cycle in the most idealistic case, where all of the energy from the magnet is recovered. To give a base for comparison, a standard industrial cabinet is 960 L (2000 mm × 800 mm × 1200 mm). It means that any supercapacitor based solution is at least filling three of those industrial cabinets.

Tab. 3.2 Physical characteristics of the supercapacitor assembly required to process 40 MJ of energy.

Reference	Total capacitance [kF]			Total weight [kg]			Total volume [L]		
	[12; 24V]	[16; 32V]	[24; 48V]	[12; 24V]	[16; 32V]	[24; 48V]	[12; 24V]	[16; 32V]	[24; 48V]
BCAP3000 P270 K04	190	110	50	3340	3340	3340	3300	3300	3300
BCAP3400 P285 K04	190	110	50	3050	3000	2750	2950	2900	2670
ESHSR-3000C0-002R7A5	190	110	50	3470	3470	3470	3280	3280	3280
NE03V03400SW001	190	110	50	2290	2430	2290	2300	2400	2300

3.3.2 Batteries

Batteries are a technology that covers another area of the power/energy density diagram (cf. **Fig. 3.11**), it is analyzed in the following paragraphs.

3.3.2.1 Chemistry

The energy stored in batteries is of electrochemical form and Faradaic type, where charges are being transferred during the reaction. They are classified in primary and secondary batteries, depending on their capability of being electrically recharged. The former can only be discharged once, while for the latter, the chemical reactions are reversible, making them rechargeable [61]. This section focuses on the secondary batteries due to the cycling nature of the targeted application.

The chemical principle of batteries is based on the reduction-oxidation process. They are composed of three major components: two electrodes, one anode and one cathode, as well as a separator for electronic insulation. The electrodes are soaked in an electrolyte acting as an ionic conductor and may or may not participate in the chemical processes.

During the discharge operation, the electrode metallic foils are connected to a load. The anode (negative electrode) material experiences oxidation (gives up electrons) forming positive ions (cations). The electrons travel through the load towards the cathode (positive electrode), which experiences reduction, (receives electrons) forming negative ions (anions). Cations migrate through the electrolyte towards the cathode and anions perform the trip of opposite direction. During the charge operation, the electrical circuit is completed by connecting a DC source. In this case, the material in the anode receives electrons and experiences reduction and the material in the cathode is giving up electrons to the DC source experiencing oxidation. Electro-neutrality is achieved by the corresponding migration of negative ions from the anode to the cathode and positive ions from the cathode to the anode through the electrolyte [62].

3.3.2.2 Electrical Behavior

The current in the battery cell arises from the electron transfer from one electrode to another. When no current flows through the cell, the difference between the potentials at the electrodes gives an open-circuit voltage of the cell. When current flows, mass transport is required to bring the reacting substances to the electrode surface or carry them away. As a result, the effective voltage is decreased on the one hand due to over-voltage at the electrodes caused by the electrochemical reactions and the concentration deviations because of transport phenomena and on the other hand due to the ohmic voltage drops caused by the electronic and ionic current flows. The result of both is called polarization [63].

A typical battery discharge curve is shown in **Fig. 3.15(a)**, where it can be observed that a fully charged battery has a higher voltage than the rated one. Then, for about 80 % of the rated capacity, the voltage remains fairly constant, but the voltage drops significantly due to its internal resistance increase in what is called the knee of the discharge curve [64].

The components contributing to the terminal voltage drop are current-dependent since they exhibit themselves when current flows through the cell. Therefore the output current can be used as a metric for battery performance. The term most often used to indicate the rate at which battery is discharged is the C-rate. The discharge rate of a battery is expressed as C/r, where r is the number of hours

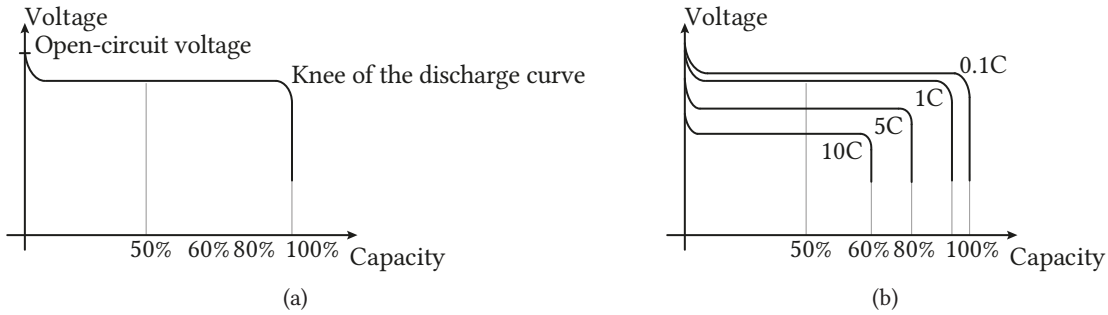


Fig. 3.15 Typical battery behavior (a) discharge curve and (b) effect of increasing C-rate for the battery discharge.

required to completely discharge its nominal capacity. The terminal voltage and the energy supplied by the battery cell vary significantly with increasing C-rates, as shown in **Fig. 3.15(b)** [65].

3.3.2.3 Battery Technologies

A brief overview of the existing battery technologies is given in **Tab. 3.3**, based on the type of electrolyte. Additionally, a comparison of their main features is gathered in **Tab. 3.4**.

In general, there are three common charging methods for batteries [67]:

1. Constant Voltage. This is the simplest charging scheme and is suitable for all types of batteries. During this type of charging, the battery current varies along the charging process and may be large at the initial stage and gradually decreasing to zero when the battery approaches its full charge. The drawback of this method is the requirement of high power in the early phase.
2. Constant Current. The battery voltage is controlled such that it maintains the current through it constant. The challenge of this method is to find the criterion of a fully charged state.
3. Constant Current Constant Voltage. At the initial stage, the battery is charged with a low constant current, when the State-of-Charge (SoC) reaches a certain threshold, the mode of charging changes to constant voltage until the battery reaches the fully charged state.

Tab. 3.3 Battery technology categorization based electrolyte type and application areas [66].

Type of electrolyte		Battery technology	Cell voltage [V]	Application
Aqueous	Alkaline	NiCd	1.2	Mobile equipment: 2; 100 W h
		NiMH	1.2	Mobile equipment: 2; 100 W h Transportation: 20; 600 kW h
	Acid	Lead-Acid	2.0	Lighting and ignition: 100; 600 W h Stationary: 0.5; 5000 kW h Load leveling: 5; 100 MW h
Non-Aqueous		Li-Ion	3.0	Mobile equipment: 2; 100 W h Transportation: 20; 600 kW h Stationary: 0.5; 5000 kW h Load leveling: 5; 100 MW h

Tab. 3.4 Comparison between different battery technologies.

Characteristics	Battery technology			
	Lead-Acid	Ni-Cd	Ni-MH	Li-ion
Specific energy [W h kg^{-1}]	30 – 50	45 – 80	60 – 120	90 – 250
Life cycle	200 – 300	1000	300 – 500	500 – 7000
Discharge time range [hour]	8 – 16	1 – 2	2 – 4	1 – 4
Safety requirements	Thermally stable			Protection circuit mandatory
Discharge rule	Partial possible	Full	Partial possible	Partial recommended
Toxicity	Very high	Very high	Low	
Cost	Low	Moderate		High

More particularly, the rate at which the battery is charged or discharges is tied to the particularities of the chemistry of each battery. Having an adapted way to process the energy through the battery can significantly improve its performances and life cycles. There are various categorizations regarding the rate of charge or discharge, it is a relative notion closely linked to the targeted application. For instance, in automotive applications, the characterization of the type of charging is compared to the time needed to fill the fuel tank in conventional (internal combustion engine) car. A summary of this categorization is given in **Tab. 3.5**.

For the application under consideration, the energy storage selected has to receive and deliver energy to the load for a duration of 20 min, or 3 C in battery language. The *fast/ultra-fast* category detailed in the table is the one of interest. It is important to note that this rate of charging needs appropriate cooling in order to prevent cell temperature rise above critical levels which reduces the life-cycle of the battery.

At this point it is important to note that Li-ion batteries are a broad family that includes many sub-technologies, each defined by their own characteristics. Based on [68] and [69], two particular Li-ion technologies appear to be more suitable for handling fast charging than the others: Lithium-Titanate (LTO) and Lithium Ferrophosphate (LFP).

Nickel-based technologies have admittedly two weak points with respect to the Li-ion technologies: lower energy/power density and a lower nominal cell voltage at 1.2 V. For a 24 V system, 20 battery cells should be connected in series. In addition, some manufacturers state that discharge at high-rate is possible for their NiCd products, however recharge is recommended with a much lower current, in

Tab. 3.5 Charge rate battery categorization.

Charge rate	Suitable chemistry	C-rate	Standard charging time
Slow	NiCd Lead-acid	0.1 C	14 h
Rapid	NiCd NiMH Li-ion	0.3 – 0.5 C	3; 6 h
Fast/Ultra-fast	NiCd NiMH Li-ion	1 – 10 C	10; 60 min

the order of magnitude of $0.2 - 0.5$ of the current corresponding to the rated capacity C_5 [70]. So in order to be able to receive the current recovered from the magnet, the battery system should be sized for its charging and not the discharging ratings, resulting in a higher number of paralleled batteries. Additionally, the NiCd technology presents a memory effect, forcing to perform deep cycles instead of partial, and NiMH charging chemistry is exothermic, thus extra care should be taken to dissipate the additional heat.

Finally, Li-ion battery candidates are considered and therefore, the following section is dedicated to a further analysis of this technology.

3.3.2.4 Li-Ion Technologies

Li-ion technology strong point is its ability to combine high energy and power density, yet it is a young technology on which research is being heavily invested, which is pushed thanks to the development of electrical and hybrid transportation [71].

Its working principle is based on intercalation electrodes with an electrochemical process involving the removal-insertion of lithium ions between anode and cathode via shuttling across the electrolyte [72], while electrons are performing the same direction route through the external circuit. Sub-technologies are distinguished depending on the materials used in the electrolyte, anode and cathode, with the latter being the factor most commonly altered.

A typical Li-ion technology safety issue is thermal runaway, a phenomenon during which the high-rate cathode and/or anode reactions cause temperature to rise rapidly and flame or rapid disassembly may follow. Thermal runaway might take place either due to physical damage or due to careless battery management (over-charge or over-discharge) [73].

A list of promising variation is given, and their main characteristics are presented in **Tab. 3.6**.

- Lithium Cobalt Oxide: LCO ($LiCoO_2$).
- Lithium Manganese Oxide: LMO ($LiMn_2O_4$).
- Lithium Nickel Manganese Cobalt Oxide: NMC ($LiNiMnCoO_2$).
- Lithium Iron Phosphate: LFP ($LiFePO_4$).
- Lithium Titanate: LTO ($Li_4Ti_5O_{12}$).

Tab. 3.6 Characteristics of Li-ion battery variations.

Characteristics	Li-ion technology				
	$LiCoO2$	$LiMn_2O_4$	$LiNiMnCoO_2$	$LiFePO_4$	$Li_4Ti_5O_{12}$
Nominal voltage [V]	3.6	3.7	3.6	3.3	2.4
Voltage operating range [V]	$3.0 - 4.2$	$3.0 - 4.2$	$3.0 - 4.2$	$2.5 - 3.65$	$1.8 - 2.85$
Specific energy [W h kg^{-1}]	$150 - 200$	$100 - 150$	$150 - 220$	$90 - 120$	$70 - 80$
Charge rate	$0.7 - 1$ C	$0.7 - 1$ C	$0.7 - 1$ C	1 C	5 C
Discharge rate	1 C	1 C	1 C	1 C	up to 10 C
Cycle life	$500 - 1000$	$300 - 700$	$1000 - 2000$	$1000 - 2000$	$3000 - 7000$
Thermal runaway [°C]	150	250	210	270	One of the safest

3.3.2.5 Battery Sizing

As suggested in [74], in order to prolong the life of a lithium-ion battery, it should be utilized in the SoC windows defined by [20 %, 90 %]. Discharging the battery below 20 % SoC, causes high discharge stress and reduces the discharge efficiency. Charging it above 90 % SoC causes high charging stress, and the risk of overcharge is real. Consequently, the battery operation is suggested to reserve 30 % of its capacity, so the battery sizing will be performed for an energy target of $E_{\text{target}} = {}^{40\,\text{MJ}}/_{0.7} = 60\,\text{MJ}$, or $E_{\text{target}} = 16.7\,\text{kW h}$.

Given the duration of the ramp-up and ramp-down of 20 min, the selected battery should be able to provide current with discharge and charge rate of 3 C, as already mentioned. Data-sheets of battery modules capable of withstanding fast-charging or discharging present this information with the C-rate terminology. It should be noted that as the C-rate increases, the capacity decreases (Peakart's effect) and the voltage of the battery presents a steeper negative slope.

The simple computation to multiply the nominal capacity by three is only giving the order of magnitude, but is not accurate for the 20 min duration. When the manufacturer does not give sufficient information, this approximation is used.

Tab. 3.7 summarizes the specifications of battery sizing. It is reminded that in order to reach a voltage target, battery cells should be connected in series. In order to reach the capacity and/or the maximum continuous current target, battery modules/in series cells should be connected in parallel.

The sizing method for the battery considers a set of assumptions in order to obtain the correct number of battery cells in series and parallel to reach the requirements, considering no losses in the power converter. If the considered product is a battery cell, the first step is to get the adequate number of series connected cells to reach the minimal voltage of 24 V. The total capacity is obtained via the E_{target} and nominal voltage, and verified against manufacturer data to ensure that the C-rate can be reached, if not, the paralleling of extra module is considered. The critical point is to obtain the least amount of batteries to satisfy **Tab. 3.7**.

Similarly as for the supercapacitors case, a 1.3 factor multiplies the end result to account for the volume of auxiliaries and mechanics around the battery cells. The table that compiles the results is given in **Tab. 3.8**.

It can be seen that promising battery technologies for the application of interest are LTO, NMC/NG and Super LFP. Also it is interesting to note that in all cases, the battery systems can easily handle higher than 1 C discharge current, while the recommended charge current is often lower. This means that the period during which energy is transferred from the magnet to the battery is often the decisive factor of whether a battery system is suitable or not.

Tab. 3.7 Target specifications for the battery sizing.

Energy	Voltage	Capacity	Current
60 MJ	24; 60 V	Function of the voltage: $f(V)$	3 C

Tab. 3.8 Sized batteries comparison in terms of weight, volume, nominal voltage, stored energy, number in parallel to withstand the current requirement and battery technology.

Manufacturer	Reference	Weight [kg]	Volume [L]	$V_{nominal}$ [V]	Energy [J]	Parallel	Oversizing	Technology
Kokam	KBM216 14S	420	270	51.8	100	10	2.5	Li-Polymer
	KBM255 14S	260	240	51.8	140	10	3.5	
Enerdel	MP320-049	320	190	43.8	100	20	2.5	Li-Ion
Altairnano	24 V 60 A h	550	260	24	100	20	2.5	LTO
Leclanché	936Co8 Titanate	990	910	46	150	10	3.7	LTO
EiG	ePLB C	760	370	25.9	370	110	9.4	NMC
A123	A123 prismatic cell	1030	550	26.4	370	100	9.4	Nano LFP
Toshiba	Type 3-20 2P12S	280	170	27.6	80	20	2	LTO
Valence	P20-24 Power	830	550	25.6	180	50	4.6	Li-Iron-Mg-Ph
Electrovaya	LITACORE 1150	270	190	25.6	12	30	3	NMC/NG
Saft	Modul'ion-12-20.60PFe	320	230	19.8	85	20	2.1	Super LFP
	Xcelion	410	320	26.4	110	20	2.9	

3.3.2.6 Comparison Between Supercapacitors and Batteries

The comparison between the mean of energy storage is made on the key point which is the overall volume. As all the solutions presented are compliant with the requirements, because of the underground and constraint location of the power supply, their physical footprint needs to be low. The most compact solutions are preferred, and the summarizing tables **Tab. 3.2** and **Tab. 3.8** give a clear result. The battery solutions are at least eight times smaller than their supercapacitor equivalent.

The supercapacitors shine by their expected lifetime, but with a careful management of the energy flowing through the battery, it is feasible to reach a thousand cycles, and replacement of the storage element over the life-time of the power supply can also be an option when the volume advantage for the batteries is so important.

3.4 Conclusions

During this system level analysis of the power supply, many lessons are learned to frame the requirements for what appears to be the critical part of the system, namely the 2-quadrant output stage of the power supply. This is the stage that needs to handle the full current and the voltage reversibility across the load. Regarding the position of the storage, the further it is from the load, the more complexity it adds to the topology, as more stages should be reversible in current/voltage and also the poorer the round trip efficiency.

As for the position of the storage on the low-voltage DC bus, the approach where it is directly on the DC link ties its voltage strongly to the load one, and bounds its lower value. In addition, it is important to keep in mind for the implementation that there will be some fast pulsating currents on the battery, requiring the addition of a strong capacitor bank. The approach where the storage is interfaced on the DC link with a converter gives more flexibility but is discarded due to the mandatory additional conversion stage required.

The properties of the chosen storage devices does not take into account the internal losses of the storage or the ones of the power supply. In using the 40 MJ as the energy need, the different solutions could be compared. Eventually this would results in a higher value of stored energy to compensate those internal losses.

As the storage technology analysis allows to define Li-ion battery technology to be the most promising one, it shows that the energy need for the whole converter can be fitted in a reasonable amount of space. The challenge is now to define the structure of the power supply in elementary sub-converters. This number should be determined with respect to the various ratings of the stage and the possible modularization.

4
DC/DC Stage Design Optimization

This chapter focuses on the DC/DC output stage of the power supply: this is the converter that processes the full load current. As the modularity is a key concept of such power supplies, and paralleling is necessary in order to achieve the desired ratings, the modularity structure and terminology is introduced in this chapter. The scope is then narrowed down to an individual sub-converter able to deliver 2 kA*. Moreover, the definition of the topology and the way to achieve the 2-quadrant operation is defined.*

4.1 DC/DC Output Stage

The simplified layout of the power supply is shown in **Fig. 4.1**. The focus of this chapter is on the output DC/DC converter stage, that is interfaced to the load and supplied from the grid side through a rectifier followed by an isolated step-down DC/DC converter. The low-voltage (LV) DC link includes an energy storage element in order to locally manage recovered energy from the load.

The rating and output characteristics of the final stage of the power supply are gathered in **Fig. 4.2**. The converter should be able to reach any operating point within its characteristics, even if in the actual application, some output operating V-I combinations are not expected. There are two possible modes of operation for the DC/DC converter highlighted in **Fig. 4.1**:

- Positive voltage output mode or *feeding mode* where $v_{\text{load}} \geq 0$:

  The power flow is from the LV-DC link to the load.

- Negative voltage output mode or *recovering mode* where $v_{\text{load}} \leq 0$:

  The power flow is from the load to the LV-DC link, the energy stored in the load is recovered locally in the power supply.

Those modes made the 2-quadrant operation possible, where the current keeps flowing in the same direction, and the voltage applied across the load can be controlled in sign and amplitude within the limits of the converter.

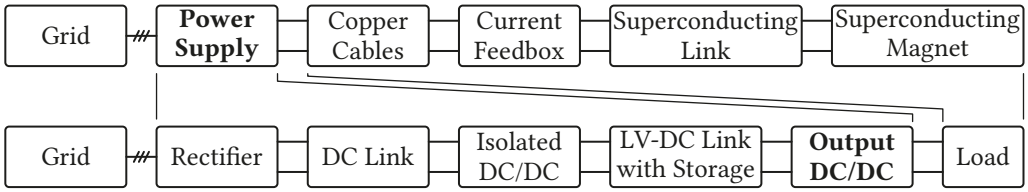
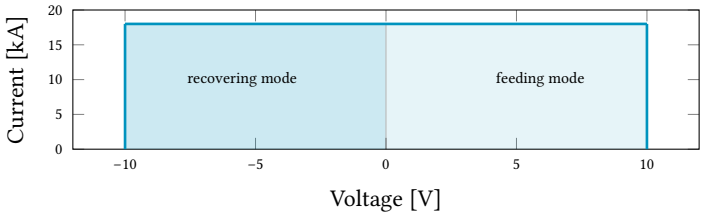


Fig. 4.1 Structure of the power supply and location of the output DC/DC stage.

Rated input voltage	v_{LV}	24 V
Input voltage variations	Δv_{LV}	±6 V
Rated output current	i_{load}	18 kA
Rated output voltage	v_{load}	±10 V

(a)



(b)

Fig. 4.2 Output DC/DC ratings: (a) input/output ratings and (b) output characteristics.

4.1.1 Modularity

Considering the required current rating of 18 kA for the whole converter, the limited ratings of single semiconductor devices, and to satisfy modularity and redundancy requirements, the structure depicted in **Fig. 4.3** is considered. Partitioning is done as such:

- The complete converter is made of N *sub-converters* in parallel configuration (cf. **Fig. 4.3(a)**).
- Based on typical CERN ratings, N is set to nine, leading to a rating of 2 kA per *sub-converter*.
- $N + 1$ redundancy principle is deployed at the converter level in order to guarantee availability of the system in case of fault of an individual N^{th} *sub-converter*.
- Those N parallel *sub-converters* are themselves composed of m parallel *branches* (cf. **Fig. 4.3(b)**).
- The *branches* are a basic building bricks of the converter including a semiconductor stage and passive filtering elements (cf. **Fig. 4.3(c)**).

In order to obtain the required output from the low-voltage DC bus, a switching stage is required, and the topology depicted in **Fig. 4.3(c)** is proposed. It is defined from the specification of the converter that each *sub-converter* provides its own and single low-voltage DC bus: v_{LV} which is unique and shared by all its *branches* . Eventually, this is where the energy storage element is placed, with a direct connection respecting the voltage levels requirements.

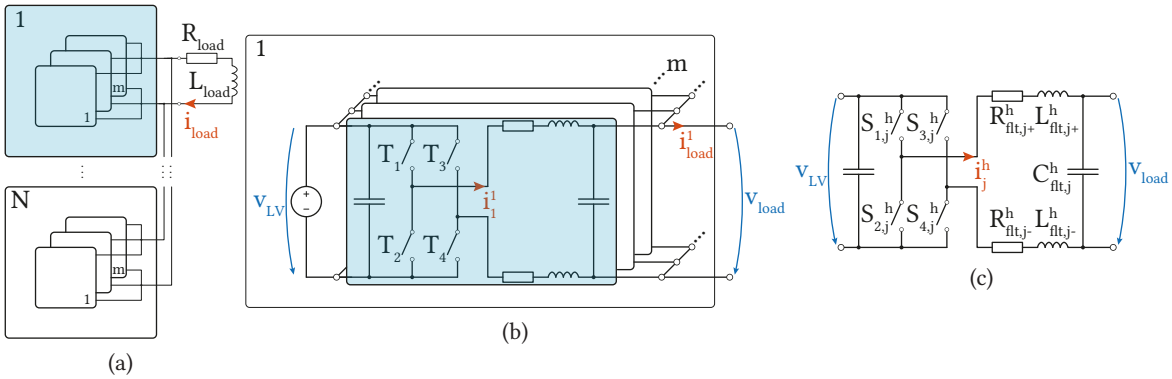


Fig. 4.3 Converter modularity: (a) division into N *sub-converters* composed of m *branches*, (b) *sub-converter* 1 composed of m parallel connected *branches* and (c) one *branch* composed of the power stage and the output filter. The main voltages and currents names are given at the different levels.

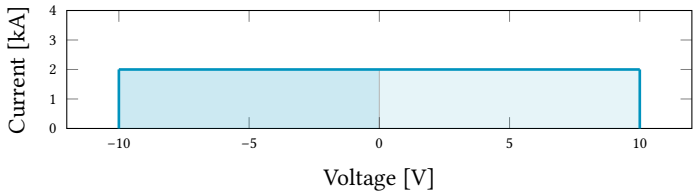


Fig. 4.4 Output characteristics of a 2 kA *sub-converter*.

The nomenclature is given as X_j^h with X being the quantity of interest with the subscript $j \in \{1; m\}$ being the index of the *branch* and the superscript $h \in \{1; N\}$ being the index of the *sub-converter*.

In **Fig. 4.3(c)** the *branch* structure is given with the naming convention: switch (S) is the generic name as in the proposed topologies it can either be a diode (D) or a MOSFET (T). The switching stage is followed by a single stage *LC* filter, and parallelization of the *m branches* is done after the filter to compose one *sub-converter* in an Input Parallel Output Parallel (IPOP) configuration.

For the study of the topology, the focus is put on the 2 kA *sub-converter*, with characteristics as given in **Fig. 4.4**.

4.1.2 Branch Topology

The 2 kA *sub-converter* is composed by a number m of *branches* made of a full-bridge semiconductor structure as the power stage followed by a single stage *LC* filter.

Because of the IPOP configuration, the current at semiconductor level is defined as $i_j^h = {}^{i_{\text{load}}}/_{(N \times m)}$, as shown in **Fig. 4.3**, with a blocking capability of at least 50 V, considering an input voltage up to $v_{\text{LV}} + \Delta v_{\text{LV}} = 30\,\text{V}$ and including safety margins. The main focus of this chapter is the topology definition of the DC/DC output converter, the semiconductors choice and output filter design are not detailed here, but are the core of the next chapter centered around the optimization process.

The simplest topology that provide a 2-quadrant operation is given in **Fig. 4.5**: it allows to reverse the voltage on the load while the current keeps flowing in the same direction. This implementation includes the minimum number of active switches, four, and is the basic one that is taken as a reference for the comparison to come.

The output *LC* filter is represented split in two paths: $L_{\text{flt,j}}^h = L_{\text{flt,j+}}^h + L_{\text{flt,j-}}^h$ and $R_{\text{flt,j}}^h = R_{\text{flt,j+}}^h + R_{\text{flt,j-}}^h$.

For the sake of simplicity and readability, in the continuation of the chapter the indices j and h are omitted as the focus in only on a single *branch* of the sub-converter.

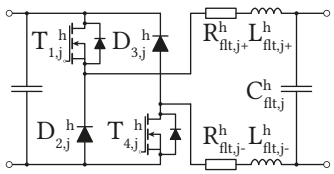


Fig. 4.5 Electrical circuit for the simplest *branch* of the converter: made of two transistors and two diodes in a H-bridge alike configuration followed by a single stage *LC* filter.

4.2 2-Quadrant Operation

4.2.1 Modes of Operation

To achieve the 2-quadrant operation with the topology introduced in **Fig. 4.5**, the mode of operation described hereafter are deployed:

- For a positive voltage output: T_4 is turned-on constantly, while the pair T_1/D_2 is operated in Pulse-Width Modulation (PWM) mode and consequently, D_3 remains turned-off. The topology generates a positive voltage on the capacitor C_{flt}, v_{load}. In this mode, the operation is similar as a buck converter, where the duty-cycle is defined as the ON time of T_1.

- For a negative voltage output, the role of the switches are changed: T_1 is turned-off, D_2 is forward biased, and the pair T_4/D_3 operates in PWM mode. This configuration allows to apply a negative voltage on the load, which depends on the duty-cycle of T_4/D_3, d is defined as the ON time of T_4.

The topology can be seen as two nested buck converters that allow the voltage reversibility. In **Fig. 4.6** is depicted a conceptual representation of the current through the device for a typical output mission profile of the power supply. The figure is only conceptual, it relies on a typical operation cycle and the presented duty-cycle is only qualitative, the switching, blocking or conducting states of the four semiconductors are presented.

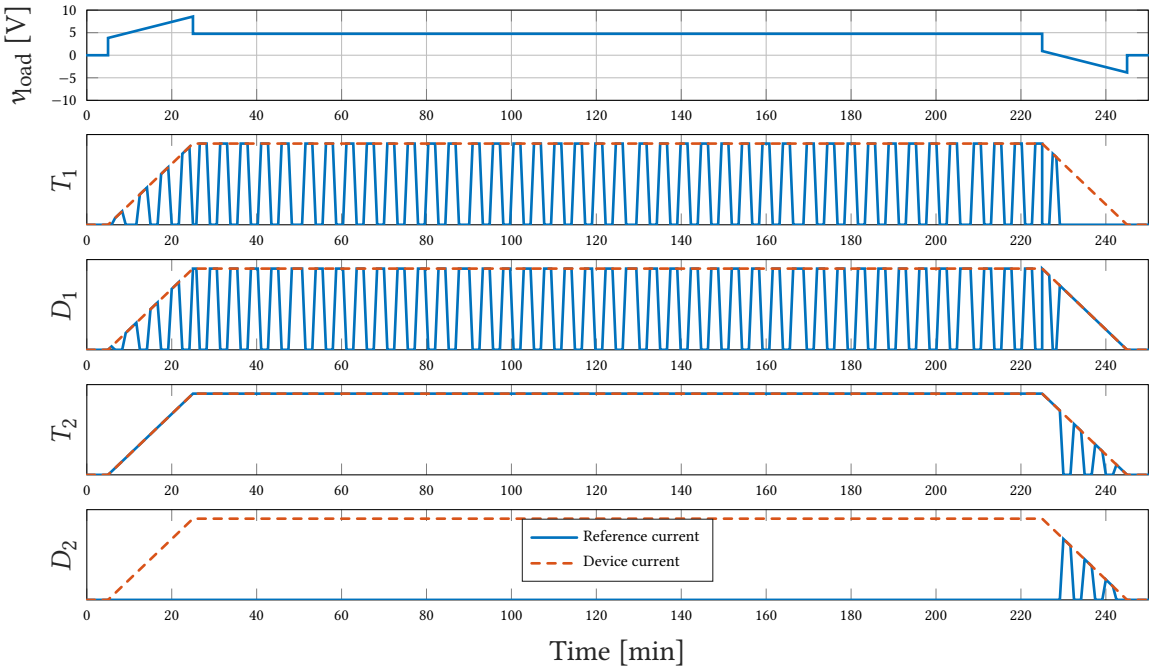


Fig. 4.6 The upper plot represents the load voltage on a typical mission profile, the lower ones detail the current in the devices with the current reference in dashed orange line: $i_{\text{ref}} = {}^{i_{\text{load}}}/_{(m \times N)}$.

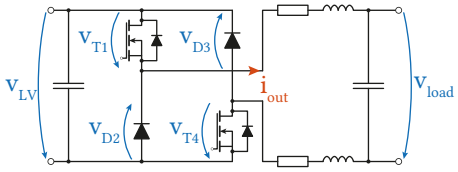


Fig. 4.7 Electrical circuit for the simplest *branch* of the converter with voltages and current definition.

4.2.2 Mathematical Model

A mathematical model of the circuit is derived, where the ideal case is considered (no voltage drop on the components), it allows to get an understanding of the behavior of the system and is mandatory to carry out the design of the converter. The definition of the voltages is given in **Fig. 4.7**.

- v_{LV} is the voltage provided by the low voltage DC bus, always positive: $v_{\text{LV}} > 0$.
- v_{load} is the voltage delivered at the output of the *branch* and can be either positive or negative depending on the operating point of the converter.
- $i_{\text{out}} = \frac{i_{\text{load}}}{N \times m}$ is the output current of the branch.

4.2.2.1 Positive Output Voltage

The positive output voltage case is depicted in **Fig. 4.8** and equivalent as a standard Buck converter, where output voltage and current can be expressed as in (4.1) and (4.2).

$$v_{\text{load}} = d_{T_1} \times v_{\text{LV}} \tag{4.1}$$

$$i_{\text{out}} = \frac{v_{\text{load}}}{R_{\text{load}}} \tag{4.2}$$

T_1 is conducting the inductor current during the phase that a positive voltage is applied across it, causing the current to increase, as detailed in **Fig. 4.8(b)**. D_2 is the complementary switch of the leg conducing the current during the free-wheeling period, when the current decreases (cf. **Fig. 4.8(c)**). This leads to the Root Mean Square (RMS) current given in (4.3) and (4.4), based on [75]. i_{out} is the output average value and Δi is half of the ripple, as shown in **Fig. 4.8(b)**.

$$i_{T_1} = i_{\text{out}} \times \sqrt{d_{T_1}} \times \sqrt{1 + \frac{1}{3} \times \left(\frac{\Delta i}{i_{\text{out}}}\right)^2} \tag{4.3}$$

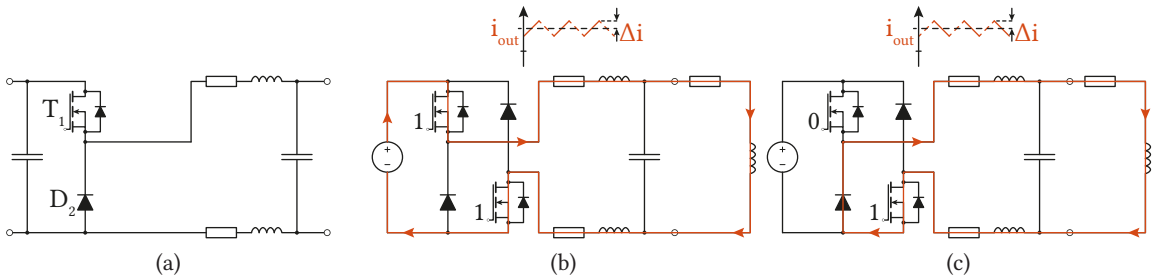


Fig. 4.8 Equivalent circuit: (a) for positive output voltage (b) current path when T_1 is ON and (c) current path when T_1 is OFF.

$$i_{D_2} = i_{\text{out}} \times \sqrt{1 - d_{T_1}} \times \sqrt{1 + \frac{1}{3} \times \left(\frac{\Delta i}{i_{\text{out}}}\right)^2} \tag{4.4}$$

In the other leg, T_4 is conducting permanently while D_3 remains blocked. The equations (4.5) and (4.6) can be de derived.

$$i_{D_3} = 0 \tag{4.5}$$

$$i_{T_4} = i_{\text{out}} \times \sqrt{1 + \frac{1}{3} \times \left(\frac{\Delta i}{i_{\text{out}}}\right)^2} \tag{4.6}$$

4.2.2.2 Negative Output Voltage

Using the same reasoning as before, based on the equivalent circuit depicted in **Fig. 4.9**, the duty-cycle of reference is the one of T_4. The equations (4.7) and (4.8) are obtained.

$$v_{\text{load}} = (1 - d_{T_4}) \times v_{\text{LV}} \tag{4.7}$$

$$i_{\text{out}} = \frac{v_{\text{load}}}{R_{\text{load}}} \tag{4.8}$$

The roles of the legs are inversed in this case compared to **Sec. 4.2.2.1**, and the first one is only used in conduction, where T_1 is constantly kept OFF. The resulting current is expressed in (4.9) and (4.10).

$$i_{T_1} = 0 \tag{4.9}$$

$$i_{D_2} = i_{\text{out}} \times \sqrt{1 + \frac{1}{3} \times \left(\frac{\Delta i}{i_{\text{out}}}\right)^2} \tag{4.10}$$

The currents in the components of the switching leg are similar as before, with d_{T_4} replacing d_{T_1}, as it can be seen in (4.11) and (4.12).

$$i_{D_3} = i_{\text{out}} \times \sqrt{d_{T_4}} \times \sqrt{1 + \frac{1}{3} \times \left(\frac{\Delta i}{i_{\text{out}}}\right)^2} \tag{4.11}$$

$$i_{T_4} = i_{\text{out}} \times \sqrt{1 - d_{T_4}} \times \sqrt{1 + \frac{1}{3} \times \left(\frac{\Delta i}{i_{\text{out}}}\right)^2} \tag{4.12}$$

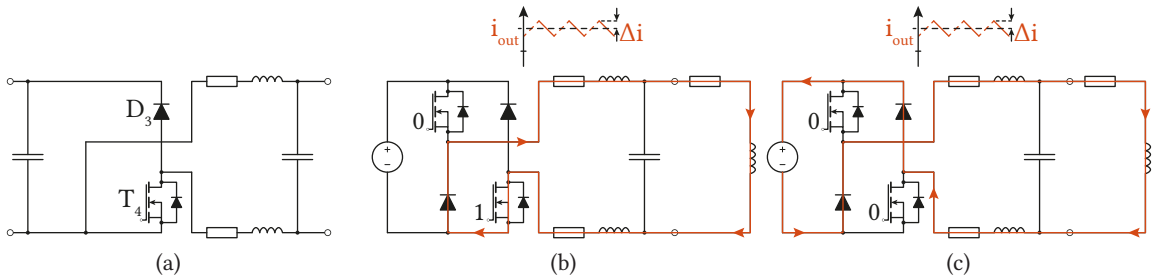
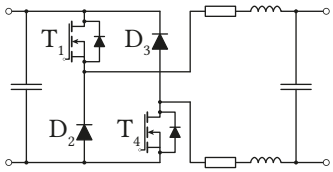


Fig. 4.9 Equivalent circuit: (a) for negative output voltage (b) current path when T_4 is ON and (c) current path when T_4 is OFF.

Mode	T_1	D_2	D_3	T_4	v_{load}
2Q-A: $v_{\text{load}} \geq 0$	switching (d_{T_1})	$\overline{T_1}$	blocked	ON	$d_{T_1} \times v_{\text{LV}}$
2Q-B: $v_{\text{load}} \leq 0$	OFF	conducting	$\overline{T_4}$	switching (d_{T_4})	$(d_{T_4} - 1) \times v_{\text{LV}}$

(a)



(b)

Fig. 4.10 2-quadrant operation with diodes: (a) modes of operation and (b) electrical scheme.

4.2.3 Summary 2-Quadrant

In a very simplified manner, the output voltage of the converter is expressed as a function of the duty-cycle and input voltage in (4.13), $d_{T_i} = T_{i,\text{on}}/T_{\text{sw}}$ and v_{LV} respectively. There are two modes of operation of the converter, each implying a different leg switching, thus the definition depends on the duty-cycle of the active element of the leg: either d_{T_1} for the feeding mode, or d_{T_4} for the recovering one.

$$v_{\text{load}} = \begin{cases} d_{T_1} \times v_{\text{LV}} & \text{if} \quad v_{\text{load}} \geq 0 \\ (d_{T_4} - 1) \times v_{\text{LV}} & \text{if} \quad v_{\text{load}} \leq 0 \end{cases} \tag{4.13}$$

In **Fig. 4.10** the states of the devices are gathered, with d being the duty-cycle of T_1 or T_4, the waveforms and gate signals are presented in **Fig. 4.11**. This topology is equivalent to a buck converter with bipolar output voltage, operated in Continuous Conduction Mode (CCM).

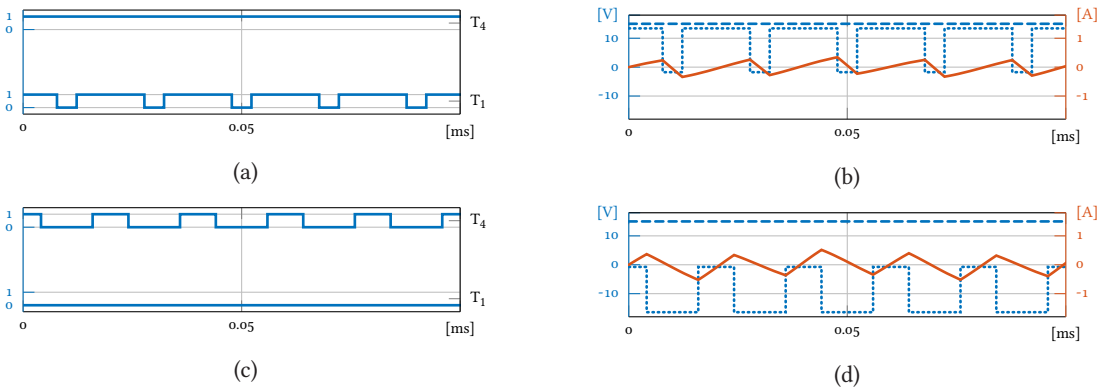


Fig. 4.11 2-quadrant (2Q) operation mode. Positive output voltage: (a) gate signals and (b) output waveforms. Negative output voltage: (c) gate signals and (d) output waveforms. In (b) and (d) dashed line is v_{LV}, dotted is output voltage (left axis) and solid is output filter current ripple (right axis, AC only).

4.3 2-Quadrant Operation with Synchronous Rectification

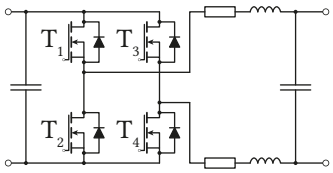
A variation of the topology previously presented is introduced in this paragraph, considering the use of four commanded switches and the MOSFET ability to carry current in both directions [76]: the Synchronous Rectification (SR) operation can be considered (2QSR), resulting in the use of four active switches, as depicted in **Fig. 4.12**. The modes of operation, for positive and negative output voltage are the same as previously described. Diodes D_2 and D_3 are replaced by MOSFETs T_2 and T_3.

Then, if the case of T_1 working in PWM mode is considered as an example, the firing of T_2 conducts complimentary with the adequate dead-times. This is known as synchronous rectification, and it is widely used in buck applications [77].

The advantages of this operation mode is the possibility to decrease the conduction losses of the switches that replace the MOSFET internal body diode, as MOSFET perform better in conduction than diodes. Although switching losses are increased with respect to the diode case, the required dead-time between the firing of the switches in the same leg to avoid a shoot-through allows the internal body diode of the switches [T_2, T_3] to start conducting before the MOSFET itself, which leads to a quasi Zero Voltage Switching operating mode [78], [79]. Consequently, the switching losses remain low. The body diode losses should also be added in the losses count.

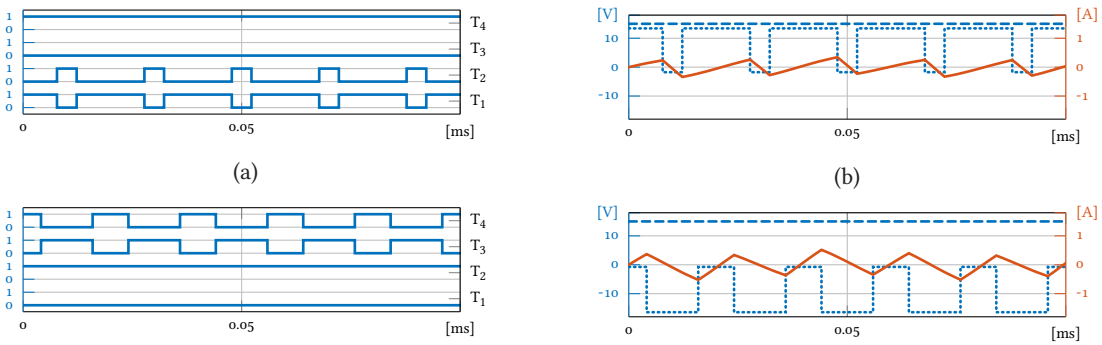
Mode	T_1	T_2	T_3	T_4	v_{load}
2QSR-A: $v_{\text{load}} \geq 0$	switching (d_{T_1})	switching ($d_{T_2} = 1 - d_{T_1}$)	OFF	ON	$d_{T_1} \times v_{\text{LV}}$
2QSR-B: $v_{\text{load}} \leq 0$	OFF	ON	switching ($d_{T_3} = 1 - d_{T_4}$)	switching (d_{T_4})	$(d_{T_4} - 1) \times v_{\text{LV}}$

(a)



(b)

Fig. 4.12 2-quadrant operation with SR: (a) modes of operation and (b) electrical scheme.



(a) (b) (c) (d)

Fig. 4.13 2-quadrant with SR (2QSR). Positive output voltage: (a) gate signals and (b) output waveforms. Negative output voltage: (c) gate signals and (d) output waveforms. In (b) and (d) dashed is v_{LV}, dotted is output voltage (left axis) and solid is output filter current ripple (right axis, AC only).

In this new configuration, the output waveforms remains almost identical to previous ones, as depicted in **Fig. 4.13**. The differences come from the voltage drop on the components.

The equations previously derived for the current flowing in each component, (4.1) to (4.12), remain valid for the positive output voltage mode A and negative output voltage mode B in the present 2QSR configuration.

4.3.1 Negative Output Voltage - Alternative Mode

This new configuration not only has the potential to lower the conduction losses, it brings another mode of operation, where the first leg is the only one switching while the second leg acts as a *polarity changer*. This mode of operation C is presented in **Tab. 4.1**, with its waveforms in **Fig. 4.14**. This is only possible with four transistors, and not with the 2Q topology presented previously because the switch 3 needs to be actively kept ON is order the revert the voltage on the load.

In this new mode of operation, the current flowing in the devices should be evaluated for the negative output voltage, using the a new equivalent circuit presented in **Fig. 4.15**. This alternative is again a buck converter where the output is inverted by the second leg, output voltage and current can be expressed as in (4.14) and (4.15).

$$v_{\text{load}} = (d_{T_1} - 1) \times v_{\text{LV}} \tag{4.14}$$

$$i_{\text{out}} = \frac{v_{\text{load}}}{R_{\text{load}}} \tag{4.15}$$

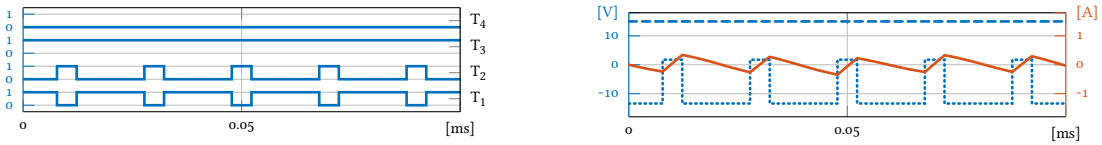
T_1 is switching as for the positive case, leading to the RMS currents given in (4.16) and (4.17).

$$i_{T_1} = i_{\text{out}} \times \sqrt{d_{T_1}} \times \sqrt{1 + \frac{1}{3} \times \left(\frac{\Delta i}{i_{\text{out}}}\right)^2} \tag{4.16}$$

$$i_{D_2} = i_{\text{out}} \times \sqrt{1 - d_{T_1}} \times \sqrt{1 + \frac{1}{3} \times \left(\frac{\Delta i}{i_{\text{out}}}\right)^2} \tag{4.17}$$

Tab. 4.1 Alternative mode of operation for negative output voltage.

Mode	T_1	T_2	T_3	T_4	v_{load}
2QSR-C: $v_{\text{load}} \leq 0$	switching (d_{T_1})	switching ($d_{T_2} = 1 - d_{T_1}$)	ON	OFF	$(d_{T_1} - 1) \times v_{\text{LV}}$



(a) (b)

Fig. 4.14 2-quadrant with SR (2QSR). Alternative negative output voltage: (a) gate signals and (d) output waveforms. In (b) dashed is v_{LV}, dotted is output voltage (left axis) and solid is output filter current ripple (right axis, AC only).

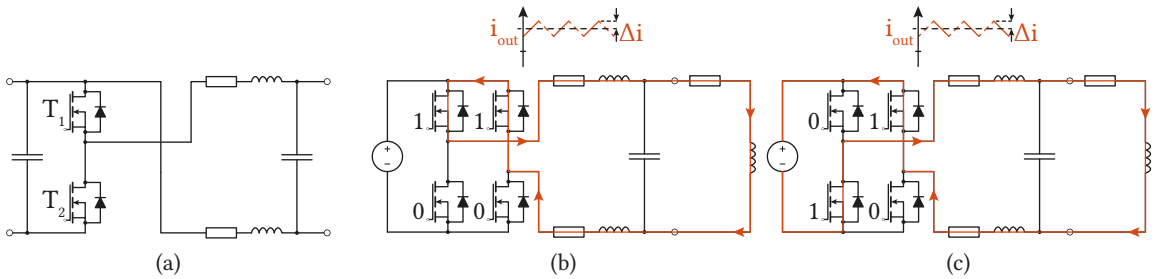


Fig. 4.15 Equivalent circuit: (a) for the alternative mode for negative output voltage (b) current path when T_1 is ON and (c) current path when T_1 is OFF.

In the second leg, called polarity changer, T_3 is ON permanently while T_4 remains OFF. The equations (4.18) and (4.19) can be derived.

$$i_{D_3} = i_{\text{out}} \times \sqrt{1 + \frac{1}{3} \times \left(\frac{\Delta i}{i_{\text{out}}}\right)^2} \tag{4.18}$$

$$i_{T_4} = 0 \tag{4.19}$$

In the case where the converter is operated with mode A (for positive output voltage) and C (for negative output voltage), the two legs have very different behavior, with one being constantly switched while the other is only used in conduction: this pattern could lead to optimize each leg according to its role, regarding the stress on the devices.

4.3.2 Summary 2-Quadrant with SR

In the case where the topology is composed by four active switches, and controlled with the SR technique, the summary of the output voltage is given in (4.20). Again, duty-cycle depends on the mode, and the improved topology adds an additional mode of operation for negative output voltage. In every case, only two devices are switching, one is conducting and one is blocked.

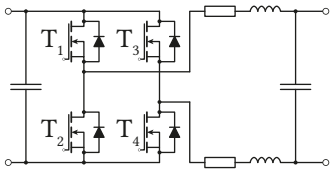
$$v_{\text{load}} = \begin{cases} d_{T_1} \times v_{\text{LV}} & \text{if} \quad v_{\text{load}} \geq 0 \\ (d_{T_4} - 1) \times v_{\text{LV}} & \text{if} \quad v_{\text{load}} \leq 0 \text{ in mode B (second leg switching)} \\ (d_{T_1} - 1) \times v_{\text{LV}} & \text{if} \quad v_{\text{load}} \leq 0 \text{ in mode C (second leg as polarity changer)} \end{cases} \tag{4.20}$$

4.4 4-Quadrant Full-Bridge

As the 2QSR topology features four active switches, it can as well be operated as a classical 4-quadrant full-bridge topology (4Q) either with bipolar (4QBI) or unipolar (4QUNI) modulation scheme as depicted in **Fig. 4.16(b)**. Even though full 4-quadrant is not needed, performances are interesting to be compared between bipolar, unipolar modulation and the considered SR. The goal is to correctly evaluate the modes of operation before reaching prototyping as any voltage drop is directly affecting the output dynamics as well as electrical losses, thus should be taken into account in the simulation. These issues are inherent to the very low output voltage, high-current power supplies.

Mode	T_1	T_2	T_3	T_4	v_{load}
4QBI	switching (d)	switching ($1-d$)	switching ($1-d$)	switching (d)	$(2\times d-1)\times v_{LV}$
4QUNI	switching (d)	switching ($1-d$)	switching ($1-d$)	switching (d)	$(2\times d-1)\times v_{LV}$

(a)



(b)

Fig. 4.16 4-quadrant operation: (a) modes of operation and (b) electrical scheme.

As it can be seen in **Fig. 4.16(a)**, the duty-cycles for both operations (bipolar and unipolar) relies on the same structure, additionally a phase shift between the switching pairs is taken into account. The resulting voltage is the same, leading to the output voltage and current expressed in (4.21) and (4.22).

$$v_{load} = (2\times d-1)\times v_{LV} \tag{4.21}$$

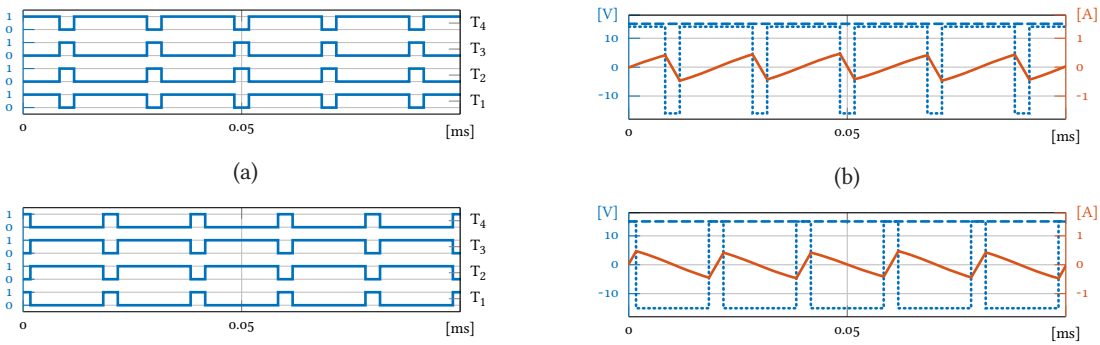
$$i_{out} = \frac{v_{load}}{R_{load}} \tag{4.22}$$

The switches (T_1;T_4) are driven with the duty-cycle d. This leads to the RMS current given in (4.23).

$$i_{T_1;T_4} = i_{out}\times\sqrt{d}\times\sqrt{1+\frac{1}{3}\times\left(\frac{\Delta i}{i_{out}}\right)^2} \tag{4.23}$$

The other switches (T_2;T_3) are driven with the complementary duty-cycle $(1-D)$. The equation (4.24) can be derived.

$$i_{T_2;T_3} = i_{out}\times\sqrt{1-d}\times\sqrt{1+\frac{1}{3}\times\left(\frac{\Delta i}{i_{out}}\right)^2} \tag{4.24}$$



(a) (b)

(c) (d)

Fig. 4.17 Full-bridge bipolar modulation (4QBI). Positive output voltage: (a) gate signals and (b) waveforms. Negative output voltage: (c) gate signals and (d) waveforms. In (b) and (d) dashed is v_{LV}, dotted is output voltage (left axis) and solid is output filter current ripple (right axis, AC only).

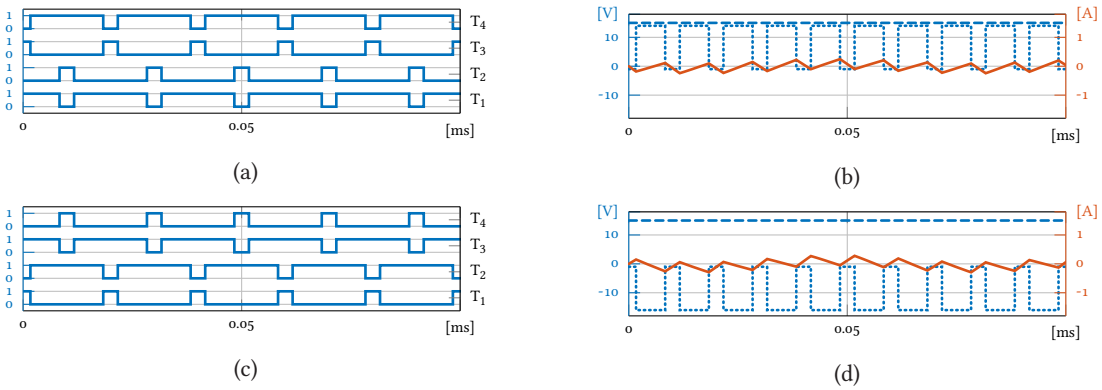


Fig. 4.18 Full-bridge unipolar modulation (4QUNI). Positive output voltage: (a) gate signals and (b) waveforms. Negative output voltage: (c) gate signals and (d) waveforms. In (b) and (d) dashed is v_{LV}, dotted is output voltage (left axis) and solid is output filter current ripple (right axis, AC only).

4.4.1 Summary 4-Quadrant

This topology with four active switches can be operated as a conventional full-bridge in the traditional switching pattern: either with bipolar modulation, using a diagonal driving with no zero voltage level at the output or the unipolar modulation where each leg has its own driving signal and the output voltage has three levels. This topology also allows full 4-quadrant operation of the converter. The definition of the output voltage is given as:

$$v_{load} = (2 \times d - 1) \times v_{LV} \tag{4.25}$$

There is no distinctions to be made between the cases, as the change of operation is simply defined by D being larger or lower than 0.5. The devices are operated in pairs and the behaviors are the same for the pairs (T_1, T_4) and (T_2, T_3).

4.5 Operating Modes Comparison

The modes of operation previously introduced are compared in this part based on the component stress. The following denomination are used:

- 2Q, 2-quadrant passive (with D_2 and D_3).
- 2QSR, 2-quadrant with synchronous rectification (with T_2 and T_3).
- 4QBI, 4-quadrant with bipolar modulation.
- 4QUNI, 4-quadrant with unipolar modulation.

4.5.1 Voltage and Current Stresses

As can be derived from the buck equations, the components are stressed according to the equations gathered in **Tab. 4.2**. The voltage rating of the selected component should be selected higher to have sufficient margins and also take into account the parasitics, mainly the over-voltage due to the commutation loop inductance.

Tab. 4.2 Stress on the components.

	Mode	$v_{\text{load}} \geq 0$	$v_{\text{load}} \leq 0$
v_{max}	2Q	$v_{T_1;D_2;D_3;T_4,\text{max}} = v_{\text{LV,max}}$	
	2QSR	$v_{T_1;T_2;T_3;T_4,\text{max}} = v_{\text{LV,max}}$	
	4Q		
i_{max}	2Q	$i_{T_1,\text{max}} = i_{\text{out}} \times \sqrt{d_{T_1,\text{max}}} \times \sqrt{1 + \frac{1}{3} \times \left(\frac{\Delta i}{i_{\text{out}}}\right)^2}$ $i_{D_2,\text{max}} = i_{\text{out}} \times \sqrt{1 + \frac{1}{3} \times \left(\frac{\Delta i}{i_{\text{out}}}\right)^2}$ $i_{D_3,\text{max}} = i_{\text{out}} \times \sqrt{1 - d_{T_1,\text{min}}} \times \sqrt{1 + \frac{1}{3} \times \left(\frac{\Delta i}{i_{\text{out}}}\right)^2}$ $i_{T_4,\text{max}} = i_{\text{out}} \times \sqrt{1 + \frac{1}{3} \times \left(\frac{\Delta i}{i_{\text{out}}}\right)^2}$	
	2QSR-B	$i_{T_1,\text{max}} = i_{\text{out}} \times \sqrt{d_{T_1,\text{max}}} \times \sqrt{1 + \frac{1}{3} \times \left(\frac{\Delta i}{i_{\text{out}}}\right)^2}$ $i_{T_2,\text{max}} = i_{\text{out}} \times \sqrt{1 + \frac{1}{3} \times \left(\frac{\Delta i}{i_{\text{out}}}\right)^2}$ $i_{T_3,\text{max}} = i_{\text{out}} \times \sqrt{1 - d_{T_1,\text{min}}} \times \sqrt{1 + \frac{1}{3} \times \left(\frac{\Delta i}{i_{\text{out}}}\right)^2}$ $i_{T_4,\text{max}} = i_{\text{out}} \times \sqrt{1 + \frac{1}{3} \times \left(\frac{\Delta i}{i_{\text{out}}}\right)^2}$	
	2QSR-C	$i_{T_1,\text{max}} = i_{\text{out}} \times \sqrt{d_{T_1,\text{max}}} \times \sqrt{1 + \frac{1}{3} \times \left(\frac{\Delta i}{i_{\text{out}}}\right)^2}$ $i_{T_2,\text{max}} = i_{\text{out}} \times \sqrt{1 - d_{T_1,\text{min}}} \times \sqrt{1 + \frac{1}{3} \times \left(\frac{\Delta i}{i_{\text{out}}}\right)^2}$ $i_{T_3,\text{max}} = i_{\text{out}} \times \sqrt{1 + \frac{1}{3} \times \left(\frac{\Delta i}{i_{\text{out}}}\right)^2}$ $i_{T_4,\text{max}} = i_{\text{out}} \times \sqrt{1 + \frac{1}{3} \times \left(\frac{\Delta i}{i_{\text{out}}}\right)^2}$	
	4Q	$i_{T_1,\text{max}} = i_{\text{out}} \times \sqrt{d_{\text{max}}} \times \sqrt{1 + \frac{1}{3} \times \left(\frac{\Delta i}{i_{\text{out}}}\right)^2}$ $i_{T_2,\text{max}} = i_{\text{out}} \times \sqrt{1 - d_{\text{min}}} \times \sqrt{1 + \frac{1}{3} \times \left(\frac{\Delta i}{i_{\text{out}}}\right)^2}$ $i_{T_3,\text{max}} = i_{\text{out}} \times \sqrt{1 - d_{\text{min}}} \times \sqrt{1 + \frac{1}{3} \times \left(\frac{\Delta i}{i_{\text{out}}}\right)^2}$ $i_{T_4,\text{max}} = i_{\text{out}} \times \sqrt{d_{\text{max}}} \times \sqrt{1 + \frac{1}{3} \times \left(\frac{\Delta i}{i_{\text{out}}}\right)^2}$	

4.6 Power Losses

In order to compare the topologies, a set of simulations is performed using standard components from a database gathering adequately rated candidates. The goal is to obtain the power losses of each topology, allowing to choose the adequate one, with the goal to maximize the efficiency.

The simulations are based on a set of Matlab scripts for the configuration of the model, PLECS is used to obtain the waveforms which are then post-processed back in Matlab. The PLECS model includes the semiconductor voltage drop and their thermal characteristics.

This section presents the calculation of power losses of each semiconductor in the topology. Both conduction and switching losses are considered, and the extraction of the required parameters from the corresponding data-sheet is detailed.

4.6.1 Conduction Losses

4.6.1.1 Diode Conduction Losses

In order to obtain the expressions for the power losses in the diode, the following assumptions are considered:

- The load during a switching period $T = 1/f_{sw}$ is considered constant.
- The instantaneous power losses is defined as the power averaged over a commutation period, i.e. $P(t) = 1/T \int_0^T v_{on}(t) \times i_{on}(t)\, dt$.
- During the conduction, the diode can be approximated by a series connection of DC voltage (v_F) representing diode on-state zero-current voltage and diode on-state resistance (R_F), i.e $v_{on}(t) = v_F + i_{on}(t) \times R_F$.

According to these assumptions, the conduction power losses in the diode can be written as in (4.28). Where RMS and average values are obtained considering a time window of one commutation period.

$$P_D(t) = \frac{1}{T}\int_0^T v_{on}(t) \times i_{on}(t)\, dt = \frac{1}{T}\int_0^T (v_F + i_{on}(t) \times R_F) \times i_{on}(t)\, dt \tag{4.26}$$

$$= \frac{1}{T}\int_0^T \left(v_F \times i_{on}(t) + i_{on}^2(t) \times R_F\right)\, dt \tag{4.27}$$

$$\Rightarrow P_D = i^2 \times R_F + i_{avg} \times v_F \tag{4.28}$$

4.6.1.2 MOSFET Conduction Losses

In order to obtain the expressions for the power losses in the MOSFET, the same assumptions as before are considered:

- The load during a switching period $T = 1/f_{sw}$ is considered constant.
- The instantaneous power losses is defined as the power averaged over a commutation period, i.e. $P(t) = 1/T \int_0^T v_{on}(t) \times i_{on}(t)\, dt$.
- The MOSFET voltage drop during conduction is $v_{on}(t) = i_{on}(t) \times R_{DS_{on}}$.

According to these assumptions, the conduction power losses in the MOSFET can be written as in (4.30). Again, RMS and average values are obtained considering a time window of one commutation period.

$$P_T(t) = \frac{1}{T}\int_0^T v_{on}(t) \times i_{on}(t)\, dt = \frac{1}{T}\int_0^T i_{on}(t) \times R_{DS_{on}} \times i_{on}(t)\, dt \tag{4.29}$$

$$\Rightarrow P_T = i^2 \times R_{DS_{on}} \tag{4.30}$$

4.6.1.3 Positive Output Voltage

For the case where the output voltage is positive, the losses can be detailed as in (4.31).

$$\begin{cases} P_{T_1} = (i_{T_1})^2 \times R_{\mathrm{DS_{on}}} \\ P_{D_2} = (i_{D_2})^2 \times R_{\mathrm{F}} + i_{D_2,\mathrm{avg}} \times v_{\mathrm{F}} \\ P_{D_3} = 0 \\ P_{T_4} = (i_{T_4})^2 \times R_{\mathrm{DS_{on}}} \end{cases} \tag{4.31}$$

4.6.1.4 Negative Output Voltage

For the case where the output voltage is negative, the losses can be detailed as in (4.32).

$$\begin{cases} P_{T_1} = 0 \\ P_{D_2} = (i_{D_2})^2 \times R_{\mathrm{F}} + i_{D_2,\mathrm{avg}} \times v_{\mathrm{F}} \\ P_{D_3} = (i_{D_3})^2 \times R_{\mathrm{F}} + i_{D_3,\mathrm{avg}} \times v_{\mathrm{F}} \\ P_{T_4} = (i_{T_4})^2 \times R_{\mathrm{DS_{on}}} \end{cases} \tag{4.32}$$

4.6.2 Switching Losses

This section outlines the switching losses calculation of the semiconductors in the considered modes of operation. The calculation, based on the switching times analysis presented in [80] is a simplification of the switching process, since it does not include the effect of the stray inductances. A more sophisticated estimation method that includes this effect can be found in [81]. In this analysis, the voltage-drop on each component is considered negligible, which represents an overestimation of the switching power losses.

Fig. 4.19 shows the waveforms corresponding to the switching transients in a power MOSFET. Additionally, the electric circuit including the inherent MOSFET capacitances is shown. Regarding these capacitances, C_{GD} and C_{DS} depend on the drain-source applied voltage, while C_{GS} is practically independent of such voltage.

Regarding switching losses, they can be split in turn-on losses and turn-off losses, as in (4.33), where $E_{\mathrm{sw}_{on[M]}}$ and $E_{\mathrm{sw}_{\mathrm{on[D]}}}$ are the turn-on losses of MOSFET and diode, respectively, while $E_{\mathrm{sw}_{\mathrm{off[M]}}}$ and $E_{\mathrm{sw}_{\mathrm{off[D]}}}$ are the turn-off losses of MOSFET and diode, respectively. Normally, the turn-off losses of diode can be neglected, since they are much lower than the remaining ones.

$$\begin{aligned} E_{\mathrm{sw}_{\mathrm{on}}} &= E_{\mathrm{sw}_{\mathrm{on[M]}}} + E_{\mathrm{sw}_{\mathrm{on[D]}}} \\ E_{\mathrm{sw}_{\mathrm{off}}} &= E_{\mathrm{sw}_{\mathrm{off[M]}}} + E_{\mathrm{sw}_{\mathrm{off[D]}}} \end{aligned} \tag{4.33}$$

The expressions for calculating the MOSFET switching losses during turn-on and turn-off are given in (4.34) and (4.35), where t_{ri} and t_{fu} are the rise time of current and the fall time of voltage during turn-on, respectively; while t_{ru} and t_{fi} are the rise time of voltage and the fall time of current during turn-off, respectively.

$$E_{\mathrm{sw}_{\mathrm{on[M]}}} = \int_0^{t_{\mathrm{ri}}+t_{\mathrm{fu}}} v_{\mathrm{DS}}(t) \times i_{\mathrm{DS}}(t)\, dt = 1/2 \times (t_{\mathrm{ri}} + t_{\mathrm{fu}}) \times U_{DD} \times i_{D\mathrm{on}} + Q_{\mathrm{rr}} \times U_{\mathrm{DD}} \tag{4.34}$$

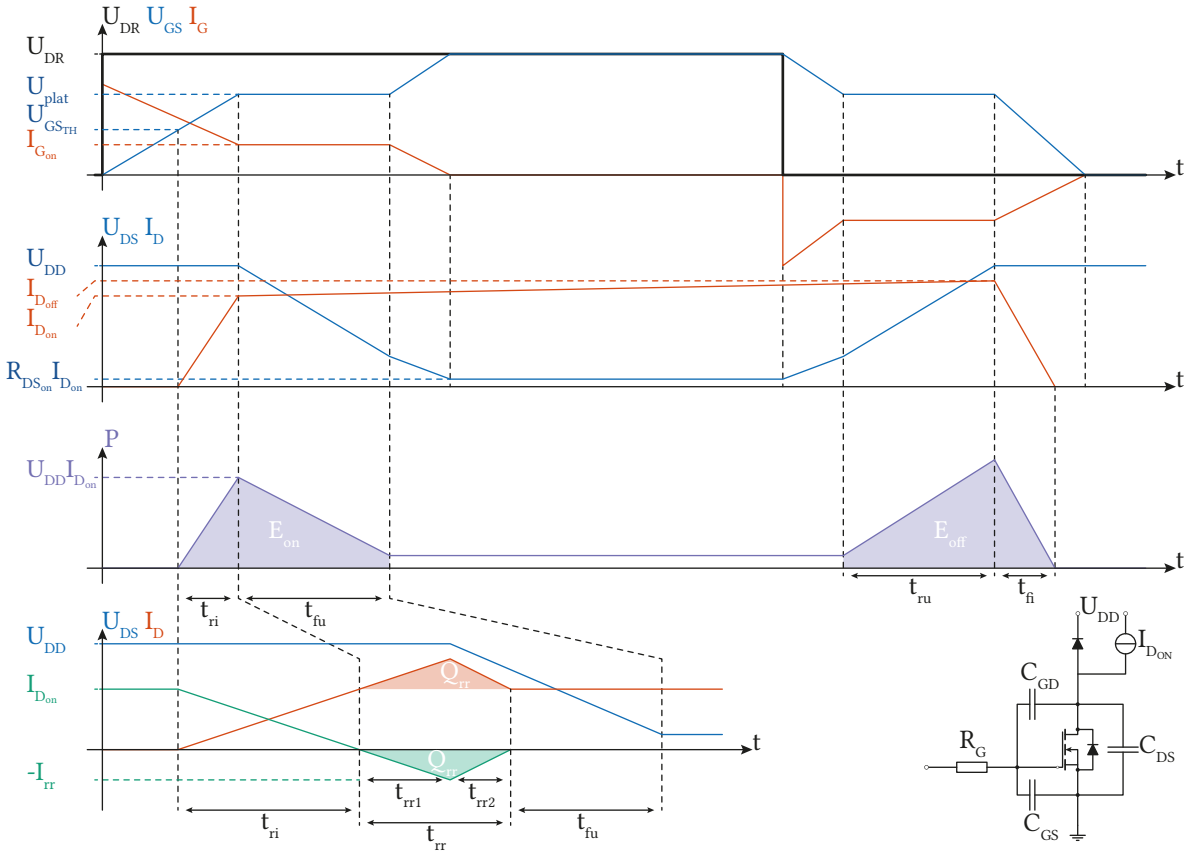


Fig. 4.19 Commutation waveforms for power MOSFET device.

$$E_{\mathrm{sw_{off[M]}}} = \int_0^{t_{\mathrm{ru}}+t_{\mathrm{fi}}} v_{\mathrm{DS}}(t) \times i_{\mathrm{DS}}(t)\, dt = 1/2 \times (t_{\mathrm{ru}} + t_{\mathrm{fi}}) \times U_{\mathrm{DD}} \times i_{D\mathrm{on}} \tag{4.35}$$

Finally, turn-on losses of diode can be estimated with the energy recovering process [82], as expressed in (4.36):

$$E_{\mathrm{sw_{on[D]}}} = \int_0^{t_{\mathrm{ri}}+t_{\mathrm{fu}}} v_D(t) \times i_F(t)\, dt \simeq \frac{1}{4} \times Q_{rr} \times U_{DD} \tag{4.36}$$

The switching power losses averaged in a commutation period are given by the equation in (4.37).

$$\begin{aligned} P_{\mathrm{sw}_{[M]}} &= (E_{\mathrm{sw}_{on[M]}} + E_{\mathrm{sw_{off[M]}}}) \times f_{\mathrm{sw}} \\ P_{\mathrm{sw}_{[D]}} &\simeq E_{\mathrm{sw}_{on[D]}} \times f_{\mathrm{sw}} \end{aligned} \tag{4.37}$$

4.6.2.1 Turn-On Losses

The process starts with the MOSFET turned-off and the driver applying U_{DR}. Then, $U_{\mathrm{GS}}(t)$ starts growing with time constant $R_{\mathrm{G}} \times C_{\mathrm{iss}}$, where $C_{\mathrm{iss}} = C_{\mathrm{gs}} + C_{\mathrm{gd}}$. While $U_{\mathrm{GS}}(t) < U_{\mathrm{GS_{TH}}}$, the output remains unchanged.

When $U_{GS}(t) = U_{GS_{TH}}$, the MOSFET turns-on; the drain current, $i_D(t)$, starts growing and the gate-source voltage continues increasing. At $t = t_{ri}$, the drain current has reached $i_{D_{on}}$ and $U_{GS}(t)$ has reached U_{plat}, which is known as the Miller plateau voltage. During this interval the diode is still conducting and $U_{DS} = U_{DD}$. The time constant of the system is still given by $R_G \times C_{iss}$. The equation (4.38) is derived.

$$t_{ri} = R_G \times C_{iss} \times \ln\left(\frac{U_{DR} - U_{GS_{TH}}}{U_{DR} - U_{plat}}\right) \tag{4.38}$$

In order to turn-off the diode, the minority carriers must be rejected from the depletion zone; the charge associated to this is known as Q_{rr}. The current generated by this carrier movement, whose maximum is named i_{rr}, is taken by the MOSFET, which implies that its maximum current during turn-on is $i_{D_{on}} + i_{rr}$. Consequently, there are additional losses in the MOSFET. The worst case operational values of Q_{rr} and its duration (t_{rr}) can be obtained from the data-sheet.

When the diode stops conducting, U_{DS} starts decreasing from U_{DD} to $i_{D_{on}} \times R_{DS_{on}}$. The Miller effect takes place, and the voltage U_{GS} remains approximately equal to the plateau voltage, U_{plat}. Then, the slope of U_{DS} is defined by a constant gate current, $i_G = {}^{U_{DR}-U_{plat}}/_{R_G}$ and the capacitance $C_{GD} = C_{rss}$. This capacitance is strongly dependent on U_{DS}. In order to take into account this dependence without complicating the calculation, a piece-wise linear function is usually used [83]. Two sections of constant capacitance are defined: the first one, considering U_{DS} is between U_{DD} and ${}^{U_{DD}}/_2$ and the second one, considering that U_{DS} is between ${}^{U_{DD}}/_2$ and 0. It is summarized in (4.39).

$$C_{GD} = \begin{cases} C_{GD_1} = C_{rss}(U_{DD}) & \text{if} \quad U_{DS}(t) \in [U_{DD},\ {}^{U_{DD}}/_2] \\ C_{GD_{12}} = C_{rss}(i_{D_{on}} \times R_{DS_{on}}) & \text{if} \quad U_{DS}(t) \in [{}^{U_{DD}}/_2,\ 0] \end{cases} \tag{4.39}$$

The $U_{DS}(t)$ variation is obtained as an average of the two capacitances. The use of C_{GD_1} defines that U_{DS} reaches its minimum in t_{fu_1}, and the use of C_{GD_2} defines that U_{DS} reaches its minimum in t_{fu_2}. The equations are presented in (4.40).

$$\begin{aligned} t_{fu_1} &= \left(U_{DD} - i_{D_{on}} \times R_{DS_{on}}\right) \times {}^{C_{GD_1}}/_{i_G} = \left(U_{DD} - i_{D_{on}} \times R_{DS_{on}}\right) \times R_G \times {}^{C_{GD_1}}/_{U_{DR}-U_{plat}} \\ t_{fu_2} &= \left(U_{DD} - i_{D_{on}} \times R_{DS_{on}}\right) \times {}^{C_{GD_2}}/_{i_G} = \left(U_{DD} - i_{D_{on}} \times R_{DS_{on}}\right) \times R_G \times {}^{C_{GD_2}}/_{U_{DR}-U_{plat}} \end{aligned} \tag{4.40}$$

Then, an average time t_{fu} is calculated in (4.41), which is used in (4.34) to obtain the MOSFET turn-on losses.

$$t_{fu} = \frac{t_{fu_1} + t_{fu_2}}{2} \tag{4.41}$$

4.6.2.2 Turn-Off Losses

The process is mainly the same than at turn-on. There are two differences:

- There is no energy recovering.
- The current when U_{DS} goes from $i_{D_{on}} \times R_{DS_{on}}$ to U_{DD} is given by $i_G = -{}^{U_{plat}}/_{R_G}$.

The times for charging C_{GD} are given by the equations in (4.42).

$$\begin{aligned} t_{ru1} &= \left(U_{DD} - i_{D_{on}} \times R_{DS_{on}}\right) \times C_{GD1}/i_G = \left(U_{DD} - i_{D_{on}} \times R_{DS_{on}}\right) \times R_G \times C_{GD1}/U_{plat} \\ t_{ru2} &= \left(U_{DD} - i_{D_{on}} \times R_{DS_{on}}\right) \times C_{GD2}/i_G = \left(U_{DD} - i_{D_{on}} \times R_{DS_{on}}\right) \times R_G \times C_{GD2}/U_{plat} \end{aligned} \tag{4.42}$$

Then, the time t_{ru} used in (4.35) is given by the equation (4.43).

$$t_{ru} = \frac{t_{ru1} + t_{ru2}}{2} \tag{4.43}$$

Finally, the current fall time, t_{fi}, is given in (4.44).

$$t_{fi} = R_G \times C_{iss} \times \ln\left(\frac{U_{plat}}{U_{GS_{TH}}}\right) \tag{4.44}$$

4.6.3 Semiconductors Parameters Extraction from the Data-Sheet

4.6.3.1 Diode

Concerning diode parameters (R_F and v_F), they can be obtained from the curve $i_{ak} = f(v_{ak})$. The diode ON state behaviour is considered a linear relationship, then $v_{ak} = v_F + i_{ak} \times R_F$. The resistive part is obtained by means of $R_F = {}^{\Delta v_{ak}}/_{\Delta i_{ak}}$, where $\Delta v_{ak} = v_{ak_2} - v_{ak_1}$ and $\Delta i_{ak} = i_{ak_2} - i_{ak_1}$. These points should be taken near to the operating point and close enough to each other so as to allow considering a linear curve. Finally, v_F is found using the equation (4.45). Where v_{ak_0} and i_{ak_0} are a pair voltage, current in the linear part of the curve. The R_F, v_F values are calculated using the data-sheet information, which can provide maximum or typical parameters, at a given junction temperature. A proper derating must be performed to calculate the parameters at the operational temperature.

$$v_F = v_{ak_0} - i_{ak_0} \times R_F \tag{4.45}$$

4.6.3.2 MOSFET

The $R_{DS_{on}}$ values given in the data-sheet usually corresponds to the maximum and typical values obtained at nominal current and $T_j = 25\,^{\circ}\text{C}$. The variation with the current is small, thus it could be neglected. However, since the ON resistance presents a remarkable variation with junction temperature (T_j), this $R_{DS_{on}}$ could not accurately represent the conduction losses if T_j is far beyond the 25 °C. In order to take into account the temperature factor, the $R_{DS_{on}}$ can be written as in (4.46), where the value $R_{DS_{on_{max}}}(25\,^{\circ}\text{C})$ can be obtained from the data-sheet.

$$R_{DS_{on}}(T_j) = R_{DS_{on_{max}}}(25\,^{\circ}\text{C}) \times (1 + \alpha)^{T_j - 25\,^{\circ}\text{C}} \tag{4.46}$$

Taking a pair $(T_{j1}; R_{DS_{on}}(T_{j1}))$ from the curve given by the manufacturer, the value of α can be estimated as in (4.47).

$$\alpha = \left(\frac{R_{DS_{on}}(T_{j1})}{R_{DS_{on_{max}}}(25\,^{\circ}\text{C})}\right)^{1/T_{j1} - 25\,^{\circ}\text{C}} - 1 \tag{4.47}$$

Then, the value of $R_{DS_{on}}$ for a given temperature can be calculated using (4.46) with the previously calculated value of α.

Normally, data-sheets supply the maximum drain current considering $T_c = 25\,^{\circ}\text{C}$ and $T_j = T_{j_{max}}$. This value is obtained under the following assumptions:

- The conventional steady-state thermal circuit is used. Then, case temperature is constant.
- The drain current is constant. Then, ΔT_j produced by switching losses is neglected.

Under these assumptions, the maximum drain current as a function of T_j and T_c is given in (4.48), where $i_{D(T_j,T_c)}$ is the current necessary to reach a junction temperature equal to T_j under a case temperature equal to T_c, R_{jc} is the thermal resistance between junction and case, and $R_{DS_{on}}(T_j)$ is the MOSFET on-state resistance when operating at T_j, obtained from (4.46).

$$i_{D(T_j,T_c)} = \sqrt{\frac{T_j - T_c}{R_{jc} \times R_{DS_{on}}(T_j)}} \tag{4.48}$$

The **Fig. 4.20(a)** illustrates the result of (4.48) for different values of T_j. Point A corresponds to the information usually obtained from data-sheet ($i_D = i_{D_{spec}}$, $T_c = 25\,^{\circ}\text{C}$, $T_{j_{max}}$). Point B is obtained when a higher case temperature is used ($T_{C_{op}} > 25\,^{\circ}\text{C}$); then the drain current decreases. Finally, if both the case temperature is increased and allowed junction temperature is decreased, a further decrease in the drain current is obtained (Point C). Notice that the above mentioned corresponds to considering the maximum achievable power under the conventional thermal model and a constant power operation (silicon limited). In general, the manufacturer bounds the maximum achievable current due to package limitations (package limited), which value is related to its capacity of heat evacuation. These limits are shown in **Fig. 4.20**. As a consequence, the maximum achievable current is usually lower than the value obtained in (4.48).

4.6.3.3 Synchronous Rectification

The diode power losses could be reduced by using synchronous rectification, i.e. the diodes are replaced by MOSFETs driven with the complementary gate signal of the switch in its leg. Power losses of a diode are dominated by conduction losses, and MOSFET exhibits conduction and switching losses. Then, the benefits of synchronous rectification can be lost when frequency increases. In the following, some equations are derived concerning this mode of operation. Note that the presented analysis is a simplification of this operation mode in order to show a tendency. For better precision in the results,

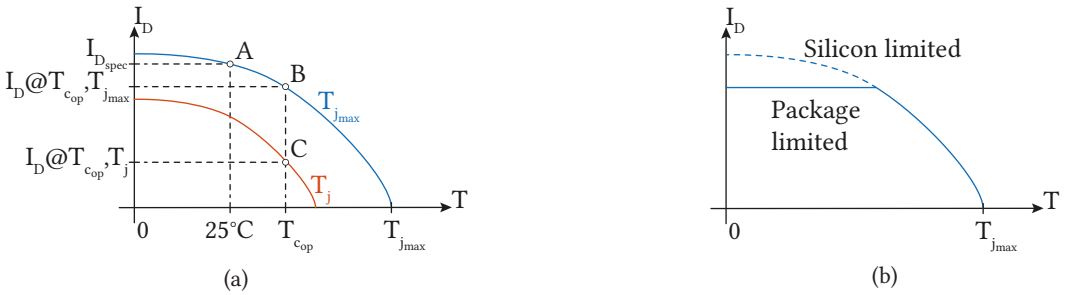


Fig. 4.20 i_D versus Temperature characteristics: (a) silicon limited and (b) package limited.

an additional analysis including the synchronous rectification main features must be performed. For instance, there is an inherent dead-time between driving the high-side and low-side MOSFETs, which turns-on the internal body diode of the synchronous MOSFETs and lead to zero-voltage transitions; consequently, switching losses in the synchronous switch are low, but other switching losses (i.e. gate losses) could be important [79].

Power losses using the body diode and the MOSFET are given by equation (4.49), where subscript [D] and [M] refers to diode and MOSFET, $P_{\text{avg}_{[\times]}}$, $P_{\text{cond}_{[\times]}}$, $P_{\text{sw}_{[\times]}}$ and $P_{\text{pk}_{[\times]}}$ are the average, conduction, switching and peak power losses of the device, d is the duty-cycle of the diode; E_{sw} is the energy loss in the switching process and f_{sw} is the switching frequency.

$$\begin{aligned} P_{\text{avg}_{[\text{D}]}} &= P_{\text{cond}_{[\text{D}]}} + P_{\text{sw}_{[\text{D}]}} \simeq P_{\text{cond}_{[\text{D}]}} = P_{\text{pk}_{[\text{D}]}} \times d \\ P_{\text{avg}_{[\text{M}]}} &= P_{\text{cond}_{[\text{M}]}} + P_{\text{sw}_{[\text{M}]}} = P_{\text{pk}_{[\text{M}]}} \times d + E_{\text{sw}} \times f_{\text{sw}} \end{aligned} \tag{4.49}$$

The expressions for $P_{\text{pk}_{[\text{D}]}}$ and $P_{\text{pk}_{[\text{M}]}}$ are given in (4.50), where the same current for both diode and MOSFET is considered, i.e. $i_{\text{ak}_{[\text{D}]}} = i_{\text{ak}_{[\text{M}]}} = i_{\text{ak}}$.

$$\begin{aligned} P_{\text{pk}_{[\text{D}]}} &= i_{\text{ak}_{[\text{D}]}} \times v_{\text{ak}_{[\text{D}]}} = i_{\text{ak}} \times (i_{\text{ak}} \times R_{\text{F}} + v_{\text{F}}) \\ P_{\text{pk}_{[\text{M}]}} &= i_{\text{ak}_{[\text{M}]}} \times v_{\text{ak}_{[\text{M}]}} = i_{\text{ak}}^2 \times R_{\text{DS}_{\text{on}}} \end{aligned} \tag{4.50}$$

Fig. 4.21 shows the representation of (4.49). It can be seen that improvement in power losses due to synchronous rectification depends on duty-cycle and switching frequency.

The improvement in power losses using synchronous rectification is obtained if $P_{\text{avg}_{[\text{M}]}} < P_{\text{avg}_{[\text{D}]}}$. The equation (4.51) can then be derived.

$$P_{\text{pk}_{[\text{M}]}} \times d + E_{\text{sw}} \times f_{\text{sw}} < P_{\text{pk}_{[\text{D}]}} \times d \tag{4.51}$$

It means that there is a minimum duty-cycle at which the synchronous rectification has an effect to reduces the losses compared to the diode, as expressed in (4.52).

$$d > d_{\text{min}} = \frac{E_{\text{sw}} \times f_{\text{sw}}}{P_{\text{pk}_{[\text{D}]}} - P_{\text{pk}_{[\text{M}]}}} \tag{4.52}$$

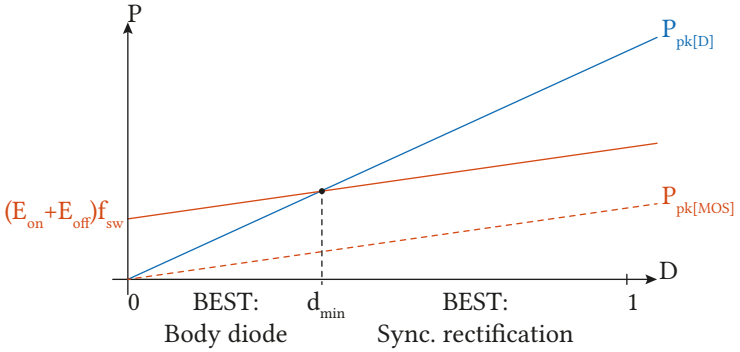


Fig. 4.21 Comparison of the losses between the internal body diode and the synchronous rectification technique.

Tab. 4.3 Driver, MOSFET and temperature parameters.

Parameter	Value
Gate voltage	15 V
External gate resistor	5 Ω
Dead time	10 ns
Modulation	2QSR

⋆

Parameter	Value
V_{DSS}	100 V
I_D	290 A
$R_{DS_{on}}$	2 mΩ
$T_{j,max}$	175 °C

Parameter	Value
Junction temperature	120 °C
Case temperature	80 °C
Ambient temperature	40 °C
Water temperature	30 °C

4.6.4 Junction Temperature

This section presents the calculation of junction temperature for each device. The conventional thermal model is used; consequently, $P(t)$ represents the instantaneous power losses, Z_{jc} is the thermal impedance between junction-case and T_c is the device case temperature, which is assumed to be constant. In the case under analysis, the use of a proper heat-sink to obtain the required case temperature is assumed. The junction temperature is given by equation (4.53).

$$T_j(t) = P(t) \times Z_{jc} + T_c \tag{4.53}$$

The power profile $P(t)$ is constant during on-time and has a negligible value during off-time. Regarding Z_{jc}, it is given by the combination of different thermal resistances and thermal capacitances; consequently, the thermal impedance value strongly depends on the on-time. For DC current operation, i.e the case $D = 1$, the thermal impedance is equal to its steady-state value, R_{jc}. For switching operation, the thermal impedance is depending on the on-time. If the on-time is higher than certain corner value (defined by the thermal characteristics of the device), the steady-state value R_{jc} can be used for Z_{jc}. On the other hand, if the device on-time is lower than that value, the simplified expression $Z_{jc} = D \times R_{jc}$ can be used. Considering the above mentioned, the expression for T_j can be obtained using in (4.54), where P_{avg} is the sum of conduction and switching power losses averaged in a commutation period.

$$T_j(t) \simeq P(t) \times d \times R_{jc} + T_c = P_{avg}(t) \times R_{jc} + T_c \tag{4.54}$$

If a better precision is required, the junction temperature under pulsed power operation and with time-dependence of thermal impedance can be obtained by means of simulation. Data-sheets usually provide the thermal resistances and time constants in order to define an *RC* thermal chain using the Foster form.

4.7 Losses Comparison

The **Tab. 4.3** gathers simulation parameters, the one flagged with ⋆ is of interest and the one to change in order to obtain the losses of the different topologies. The reference switching frequency is taken as 50 kHz which is in the typical range of operation for the selected device. For the sake of comparison, the MOSFET transistor *IRFP4468PbF* from *International Rectifier* is used, nominal ratings are 100 V, 195 A in a *TO-247* package.

Comparative results obtained from PLECS simulations are shown in **Fig. 4.22**. For all considered power supply topologies, DC/DC converter is supplied from $v_{LV} = 24$ V and at first, operates at the maximum power operating point: 10 V with 2 kA load current in feeding mode. Then, the recovering mode is also considered with −10 V output while 2 kA are flowing back from the load.

The overall losses for the *sub-converter* are summed up to obtain the losses per devices and see how they are shared, 22 devices are necessary to handle the 2 kA. The switching losses of the free-wheeling diode are neglected in comparison to conduction losses and the MOSFET switching losses.

For the 2-quadrant operation (2Q), from the loss split, it can be seen that the dominant losses are the conduction ones, particularly because of the poor performances of the diode (cf. **Fig. 4.22(a)**). Even if in this case, an external Schottky diode is selected and is taken into account for the simulations: losses in the component D_2 represents 10 % of the total output power of the stage. However it can be seen that D_3, as it is constantly blocking, does not account for any losses, there is then a strong unbalance of the losses among the semiconductor devices of the converter.

Introduction of SR (2QSR) improves the performances, as seen in **Fig. 4.22(b)**, in particular for S_2, because of the better conducting performances of the MOSFET than the selected Schottky diode: even if there are some switching losses in the component, the reduction of conducting losses account for a global improvement of the performances. The specific modulation allows to reduce switching losses, as only the minimal number of devices is switched.

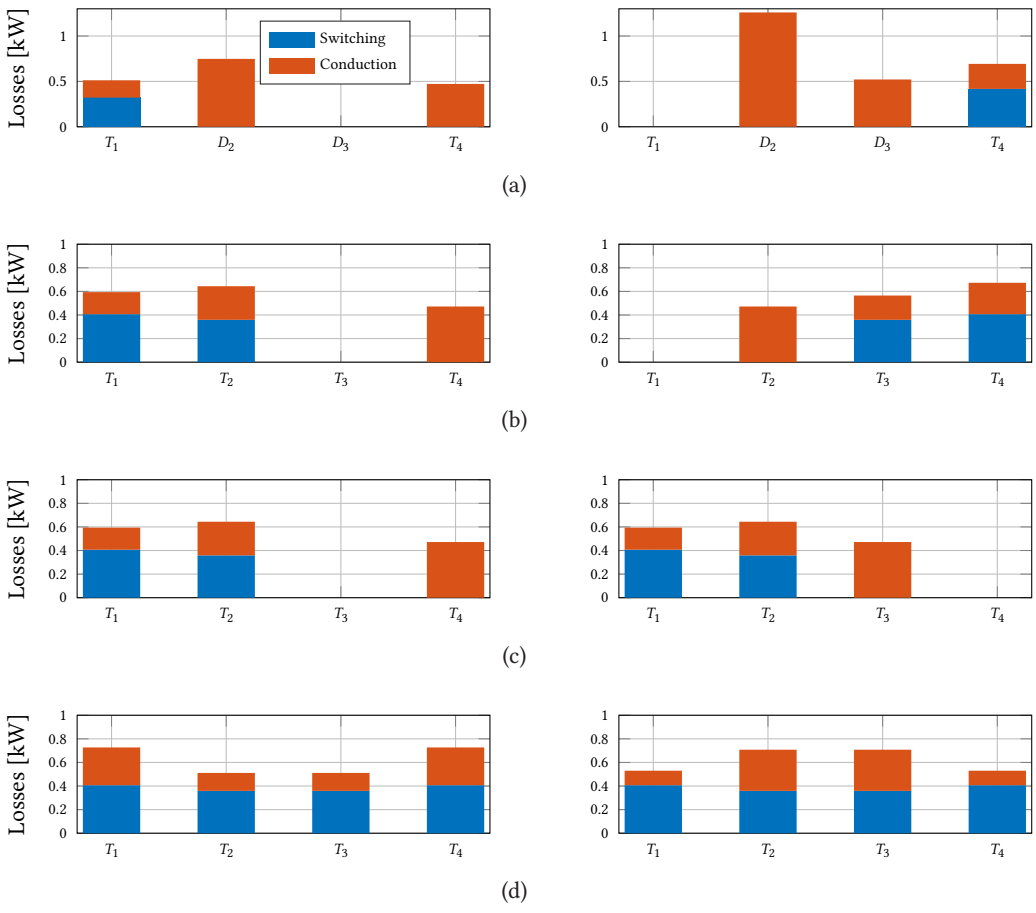


Fig. 4.22 Comparison of *sub-converter* (total of 22 switching devices) losses for different topologies at 50 kHz and maximum power operating points: 10 V; 2 kA (left hand side) and −10 V; 2 kA (right hand side). (a) 2-quadrant (2Q), (b) 2-quadrant with SR (2QSR-B), (c) 2-quadrant with SR with the alternative method to obtain the negative output voltage (2QSR-C) and (d) 4-quadrant bipolar (4QBI) and unipolar (4QUNI).

In case the alternative way to operate (with only one leg switching an the other acting as a polarity changer) depicted in **Fig. 4.22(c)**, the loss repartition is also given. This modulation includes the same number of switching events as the one studied during the loss evaluation and device selection process, where a leg is switching while on the other one device is ON. The budget of losses remains the same.

Finally, results for a classical 4-quadrant (4Q) operation are provided in **Fig. 4.22(d)**. First noticeable fact is the equal split of the losses among diagonal devices (T_1;T_4 and T_2;T_3) . Analysis of the losses at the component level can lead to some improvement (i.e. for T_2), but as all devices are constantly switching, there is an unavoidable share of switching losses in all the devices.

Out of these simulations, highlighted by the figures, some conclusions can be drawn:

- The analysis of the graph allows to establish a clear hierarchy in efficiency within the topologies, where 2QSR is the best performing one, 2Q the worst and 4Q intermediate one, rather close to 2Q.
  - The optimized switching pattern of the 2QSR topologies allows to reach higher efficiency because of having one device always off and optimized conduction paths (cf. **Fig. 4.22**).
- For 4Q unipolar or bipolar modulation, there is no difference on losses, but an impact on the output waveforms of the converter.
- As the switching losses account for a limited percentage of the overall losses, reducing the switching frequency can impact the efficiency of the converter. In the proposed case, lowering it from 50 kHz to 20 kHz increase the efficiency by 2 % (cf. **Fig. 4.23**).

High currents impact significantly achievable operational efficiency of the converter, and reaching higher efficiencies can be done by paralleling more devices as it can be seen in **Fig. 4.23**. The price to pay is to greatly oversize the system in order to reduce the current that each device has to handle.

Efficiency can be improved by paralleling more devices in the *branch* or directly at the device level, but this implies to greatly oversize the system.

There is still room for further optimization: as in the 2QSR topology there is an uneven split of losses among devices, the one that are mainly used in conduction can take advantage of a lower $R_{\mathrm{DS_{on}}}$ whereas the others T_1, T_2 should keep good performances in switching, selection of the device depending on those constraints could improve further the efficiency of the converter.

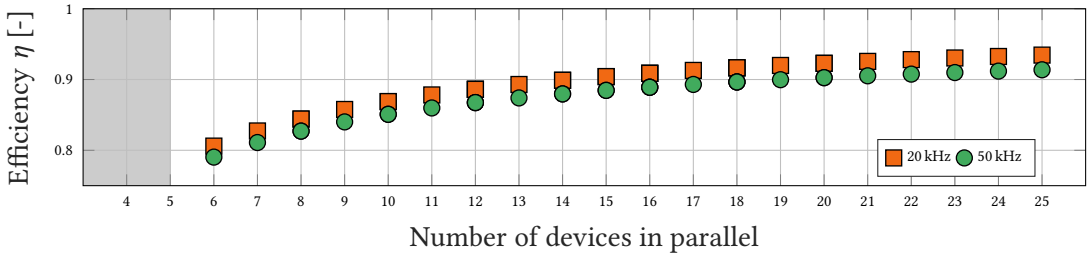


Fig. 4.23 Efficiency vs number of devices in parallel. Grey area defines thermally not viable configurations.

Tab. 4.4 Summary of the advantages and drawbacks of the modes of operation.

Mode	Advantage	Drawback
2Q	• Reduced control complexity	• High losses in the diodes • Overall poor efficiency • Uneven split of losses among devices
2QSR	• Different loss sharing than in 2Q • Overall reduced losses compared to 2Q (lower losses in T_2 and T_3 compared to D_2 and D_3)	• Uneven split of losses among devices
4QBI	• Same control complexity as 2QSR • Good controllability at low current • Identical losses in diagonal devices	• Always two switching devices • Larger output ripple
4QUNI	• Same control complexity as 2QSR • Good controllability at low current • Doubled apparent switching frequency • Identical losses in diagonal devices	• Always two switching devices

4.8 Conclusions

The table **Tab. 4.4** sums up the advantages and drawbacks of the operation of each of the compared topologies.

In this chapter, the specific requirements for a magnet power supply as well as effectiveness of various topologies under different operating modes is presented. The description as well as complete simulation and comparison of the models including losses analysis and electrical performances, taking into account temperature and operating conditions highlights the predominant role of conduction losses. The 2-quadrant topology operating with synchronous rectification is identified as the most efficient topology at any operating point of the cycle, with a possible optimization on the number of devices parallelized and the switching frequency.

5
Branch Optimization

This chapter presents the hardware selection and optimization for the critical part of the converter: semiconductors and passives constituting the output filter of the stage. A structure and mathematical tools are established in order to compare and optimize the designs according to the defined requirements. As the topology heavily relies on parallelization, the interleaving between stages is considered to relax constraints on individual stages. An optimization tool is implemented and used to sweep the parameters in order to obtain the most efficient of the realistic designs. The results of the design optimization imply that the optimal solution is to divide the sub-converter *in eight branches, where each switch is composed by six parallel MOSFETs.*

5.1 Sub-Converter Characteristics

The topology and its modulation scheme is defined in the previous chapter, where the 2-quadrant with synchronous rectification of operation is selected because it provides the best efficiency among the ones presented. Still, the hardware of the *sub-converter* offers some degrees of freedom in its implementation in order to meet the specifications, the best solution is determined, considering the highest efficiency and a small footprint for the ease of integration and modularity, through a multi-objective optimization process.

5.1.1 Requirements

The specifications of the DC/DC *sub-converter* to be designed are gathered in **Tab. 5.1**. The input voltage is provided by the upstream power stage that includes energy storage element, and it is considered to have a 24 V nominal voltage with variations between 18 V and 30 V. As the design of the power converter should take into account the worst operating conditions, and the distinction still needs to made between the positive and negative output voltage mode, the two following operating points for the *sub-converter* are defined:

- Positive output voltage mode: 2 kA; 10 V, with an input voltage of $v_{\text{min}} = 18\,\text{V}$.
- Negative output voltage mode: 2 kA; −10 V, with an input voltage of $v_{\text{min}} = 18\,\text{V}$.

Those two operating points are considered when referring to positive output voltage and negative output voltage respectively.

The output current requirement is the most constraining one, as no single semiconductor can achieve such ratings, which is why the *sub-converter* structure needs to be modular. As defined previously, the whole power supply is composed by nine*sub-converters*rated for 2 kA.

Tab. 5.1 Specifications of the sub-converter.

Input voltage	Minimum input voltage	Maximum input voltage
$v_{LV} = 24\,V \pm 6\,V$	$v_{LV,\,min} = 18\,V$	$v_{LV,\,max} = 30\,V$

Minimum apparent switching frequency	Maximum apparent switching frequency
$f_{sw,\,app\,min} = 50\,kHz$	$f_{sw,\,app\,max} = 500\,kHz$

Output voltage	Output voltage ripple	Output current	Output current ripple
−10; 10 V	0.5 %	2 kA	0.1 %

5.1.2 Modularity

When it comes to the reality of implementation, only off the shelf components are considered. There is no high-current low-voltage MOSFET on the market able to process 2 kA with a low-voltage blocking capability, the ratings of a selection of components are presented in **Fig. 5.1(b)**, the list of identifier referencs is given in **Tab. A.1**. That is why the selection is made of the highest possible rated current for a blocking voltage lower than 100 V. As depicted in **Fig. 5.1(a)**, the MOSFET perfectly fits the area that is to be explored: the *sub-converter* is having a power of 20 kW, the rating of every combination is lower and the targeted range of switching frequency is in the kilohertz range.

Some aspect of the modularity were introduced previously to allow the understanding of the topology on a conceptual level, as can be seen in **Fig. 5.2**. But as this chapter focuses on the design optimization, the modularity at the component level is introduced, this level is referred with the index k and corresponds to a parallel integration of the MOSFET themselves to constitute a single switch $T_{\#}$, as depicted in **Figs. 5.2(b)** and **5.2(c)**.

From the presented structure, the unknowns remain the number of parallel *branches* m and MOSFET devices k to parallelize. The details of the *sub-module* are recalled in **Fig. 5.3**, with its naming convention and electrical structure. The goal is to obtain the most efficient structure meeting the requirements and considering a range of commercially available products. To this extent an optimization tool able to explore multiple designs is implemented and detailed from the following section. This tool considers the requirements, the available degrees of freedom and the interleaving possibility between the multiple parallel *branches* .

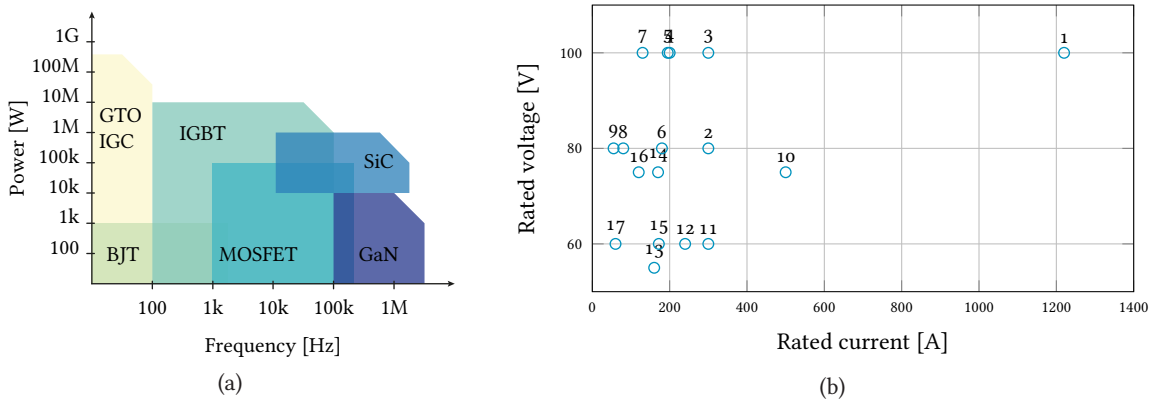


Fig. 5.1 (a) Semiconductor type and range of application [84] and (b) high-current low-voltage MOSFET map (cf. **Tab. A.1** for the device list).

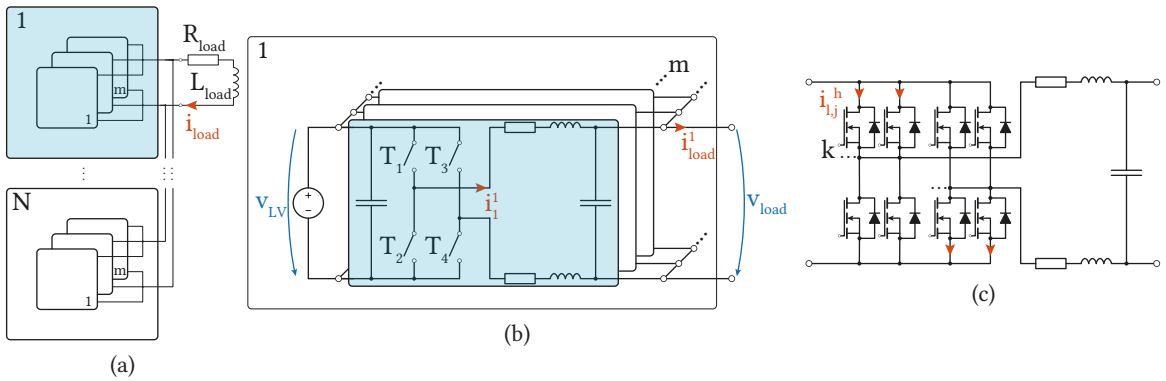


Fig. 5.2 Detailed power supply modularity: (a) division into *N sub-converter* composed of *m branches* , (b) focus on the *sub-converter* 1 with the detail of the *m branches* and (c) emphasize on the *branch* where the switches are composed of *k* parallel devices. For the device current, $h \in [1;\ N]$, $j \in [1;\ m]$ and $l \in [1;\ k]$.

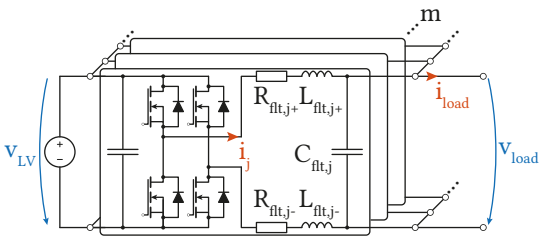


Fig. 5.3 *Sub-module* detailed circuit with the different *branches* and naming conventions.

Thanks to the input-parallel output-parallel (IPOP) configuration, the individual current seen by every semiconductors is the load current divided by $m \times k$. The filtering stage is composed by a simple *LC* structure. Thanks to the large inductance of the load, in the order of few hundreds of mH, and the low-voltage on the DC bus, the single *LC* stage is sufficient to reach the ripple requirements. Considering the large current rating expected at the level of each branch, the filter inductor is considered as a discrete component for the design optimization. Taking into account the requirements presented previously, the actual values of the *LC* filter will be adjusted for every possible design configuration.

5.1.3 Interleaving

Introducing interleaving between the parallel *branches* is a way to affect the output ripple and the apparent switching frequency at the output of the *sub-converter*. There are two levels of modularity in the sub-converter: *m* and *k*. However, it is not possible to interleave at both levels.

By the nature of paralleling the devices to constitute a single switch, no interleaving can be done at the very *k* level. It can only be considered between the *m* branches. To take the most out of the interleaving, the considered strategy is to phase shift each *branch* by a θ_m angle, defined in (5.1). At the same time, the output apparent switching frequency is increased by the same factor *m*, as expressed in (5.2).

$$\theta_m = \frac{2\pi}{m} \tag{5.1}$$

$$f_{\text{sw, app min}} \leq f_{\text{sw, app}} = m \times f_{\text{sw}} \tag{5.2}$$

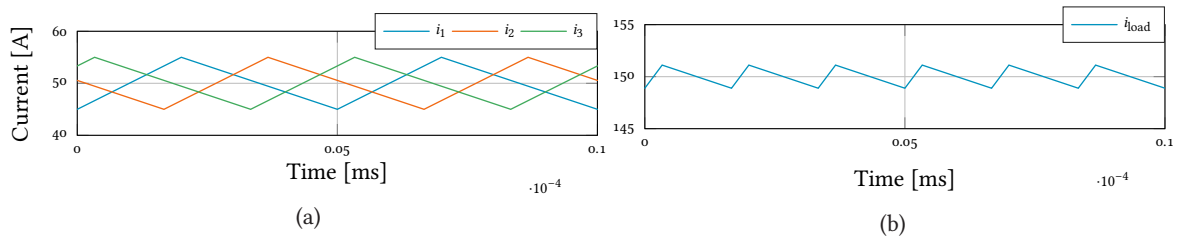


Fig. 5.4 An example of interleaving of the currents at the output of the *sub-converter* with $m = 3$ and $f_{sw} = 20\,kHz$: (a) *branch* currents and (b) *sub-converter* output current.

The advantage of interleaving is to cancel out the ripple at the output of the *sub-converter* and increasing the apparent switching frequency with keeping a lower *branch* switching frequency, as it is successfully demonstrated in [85]. It is then possible to relax constraints on the individual *branch* filters, where the ripple is allowed to be larger. The interleaving of all the *branches* currents at the output of the *sub-converter* gives a ripple lower than the individual one, at a frequency of $f_{sw,\,app}$, which is m times the effective switching frequency of the devices. This trait is further explored through the optimization process by sweeping the effective switching frequency combined with a sweeping number of parallel *branches m*.

This behavior is plotted in **Fig. 5.4**, where, for the given configuration, the output apparent switching frequency is three times the actual *branch* switching frequency and the DC current is three times higher than the *branch* current because $m = 3$.

Additionally the interleaving brings further improvements [57], [86] such as a reduction of size depending on the number of interleaved branches, stress on the DC bus capacitors because of harmonics cancellation and ripple reduction, as well as improved dynamic performances and controllability, as discussed in the dedicated **Chap. 6**.

5.2 Design Process

The design process depicted in **Fig. 5.5** is implemented with the help of Matlab in order to determine the optimal design, where a sweep is performed over several degrees of freedom: the number of *branches m*, the model of MOSFET, the apparent switching frequency $f_{sw,\,app}$, the interleaving and the number of parallel devices k. Those variables are taken into account to produce designs that reach the given requirements of the power supply. A set of input parameters are given in order to provide the algorithm with the necessary data. They are then processed to make them suitable for the script that creates the designs based on several loops, for the different possible arrangements. From those designs the losses are computed, the design of the filter is presented and the overall mechanical size of the assembly is estimated. A summary of the parameters and their variation is presented in **Tab. 5.2**.

Tab. 5.2 Allowed range of variables for the *sub-converter* design.

branches m	MOSFET	Apparent switching frequency $f_{sw,\,app}$	Interleaving	Parallel devices k
[4; 30]	[①; ⑤]	[50 kHz; 500 kHz]	[ON; OFF]	[1; 20]

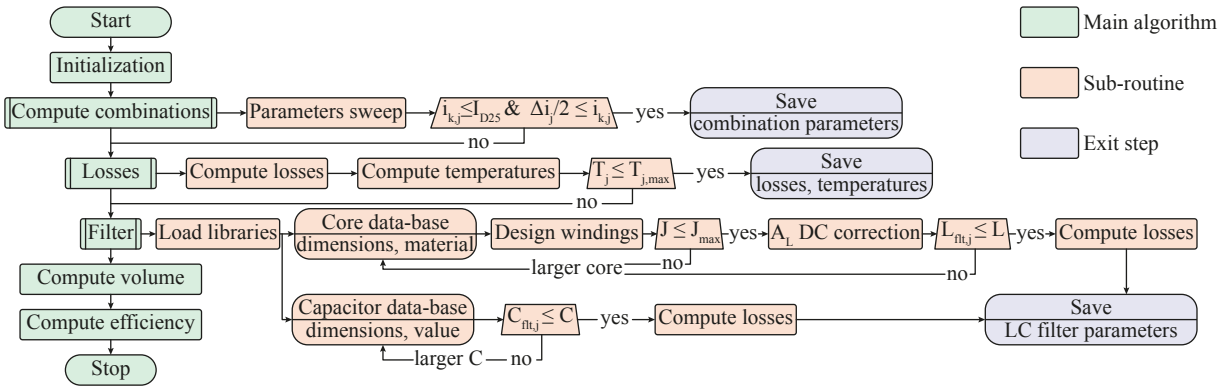


Fig. 5.5 Design process algorithm.

5.2.1 Inputs

The first step *Initialization* allows to gather the data from the various database and shape the structures that are containing the data used throughout the process. The next step is to generate the set of combinations within the range of the swept parameters for a given operational point, that happens during the *Compute combinations*.

5.2.1.1 Operating Constraints

The operation gathers the constraints of the sub-converter, as given in **Tab. 5.1**. In addition the operating point that can be chosen individually for either positive or negative output voltage. The dependence of the output voltage on the duty-cycle d is derived, as recalled from the previous chapter in (5.3) as well as the output power of the supply (5.4).

$$v_{\text{load}} = \begin{cases} d_{T_1} \times v_{\text{LV}} & \text{if} \quad v_{\text{load}} \geq 0 \\ (d_{T_4} - 1) \times v_{\text{LV}} & \text{if} \quad v_{\text{load}} \leq 0 \text{ in mode B (second leg switching)} \\ (d_{T_1} - 1) \times v_{\text{LV}} & \text{if} \quad v_{\text{load}} \leq 0 \text{ in mode C (second leg as polarity changer)} \end{cases} \tag{5.3}$$

$$P_{\text{load}} = i_{\text{load}} \times v_{\text{load}} \tag{5.4}$$

5.2.1.2 Configuration

The configuration part is where the range of m and k combinations are defined. In order to be very generic and obtain a complete range of combinations, both those values are set to be in the ranges defined as: $m \in [4; 30]$ and $k \in [1; 20]$.

5.2.1.3 Gate Driver Considerations

The gate driver definition includes three elements: the switching frequency (f_{sw}), which can be defined as a set of discrete values, the gate-source voltage applied by the driver on the MOSFET gate (v_{gs}) and the dead-time (t_{dead}), these value are used in the semiconductor loss evaluation. The degree of interleaving can also be specified for the sake of comparison: either no interleaving, where $f_{\text{sw}} = f_{\text{sw, app}}$ and the ripple is not relaxed on the *branches* or the interleaving strategy detailed previously in **Sec. 5.1.3**. If interleaving is adopted, the switching frequency is defined to meet the requirements on the output apparent switching frequency as in (5.5).

$$f_{\mathrm{sw}} = \frac{f_{\mathrm{sw,\,app}}}{m} \tag{5.5}$$

5.2.1.4 Temperatures

The *temperatures* block defines the limit temperatures for safe operation, for the case and junction, as well as the worst condition in terms of ambient temperature.

5.2.1.5 Devices Selection

Five MOSFET candidates are selected, whose characteristics should follow the requirements given hereafter. Their main characteristics are gathered in **Tab. 5.3** and they are identified by their number, ① to ⑤. The selection is done according to the following criteria.

- Drain-Source voltage: $V_{\mathrm{DSS}} = 50;\ 100\,\mathrm{V}$.
- Drain current (@25 °C): $I_{\mathrm{D25}} \geq 180\,\mathrm{A}$.
- Low $R_{\mathrm{DS_{on}}}$: $\simeq 1\,\mathrm{m\Omega}$.
- Different package for different mechanical integration approaches, details on the mechanical assembly for the packages are given in appendix **Sec. A.2.2**.

The voltage rating is selected well above the DC-link voltage to take into account the transient over-voltage issues with still a sufficient margin.

The electrical quantities are calculated from the relevant operating points of the system, while the MOSFET parameters are extracted from the data-sheet of the selected device and scaled to include temperature dependency [87]. For example, the external gate resistance considered is the one given by the manufacturer in the MOSFET data-sheet dynamics part.

Additionally, a new metric is introduced, the electrical *utilization factor* of the device defined as $^{i_j}/_{I_{\mathrm{D25}}}$. It gives an idea to which of its nominal ability the MOSFET is used. Even though the devices are rated for I_{D25} current, they are used at much lower ratings because of increased temperature during operation: this I_{D25} is the current that the MOSFET could process in the ideal situation where the case temperature is kept at 25 °C.

Tab. 5.3 MOSFETs considered for the design.

Identifier	①	②	③	④	⑤
Model	IRFP4468PbF	IXFN300N10P	MMIX1F520N075T2	STL220N6F7	IPB015N08N5
Manufacturer	International Rectifier	IXYS	IXYS	ST Microelectronics	Infineon
V_{DSS}	100 V	100 V	75 V	60 V	80 V
I_{D25}	290 A	295 A	500 A	260 A	180 A
$R_{\mathrm{DS_{on}}}$	2.6 mΩ	5.5 mΩ	1.6 mΩ	1.4 mΩ	1.5 mΩ
Package	TO-247	miniBLOC	IXYSspecial	PowerFLAT	D2PAK

5.2.2 Compute Combinations

In the *Compute combinations* block the designs are produced containing all the possible combination of the varying parameters as defined before. They are created using nested loops, taking the data from the input set. The sweep is then done over five loops, varying the following parameters:

- *loop 1*: m for the number of *branches* within the defined range $[4;\ 30]$.
- *loop 2*: MOSFET ID, ① to ⑤, with their relevant characteristics.
- *loop 3*: f_{sw} for the different *branch* effective switching frequency, ranging from 50 kHz to 500 kHz.
- *loop 4*: interleaving, in order to consider the interleaving strategy or no interleaving at all.
- *loop 5*: k for the number of MOSFET in parallel, within the defined range $[1;\ 20]$.

One combination gathers the critical parameters of the design, which makes it unique: the number of *branches* m, the selected MOSFET device, the switching frequency f_{sw}, the current per *branch* i_j ($j \in [1;\ m]$), the ripple allowed in the *branch* Δi_j, the target inductance and capacitance $L_{\text{flt},j,\text{target}}$ and $C_{\text{flt},j,\text{target}}$ respectively and the number of parallel devices k. The conditions for continuous conduction and current below the rating of the semiconductors need to be fulfilled in order for the combination to be saved and evaluated further.

In the case where the interleaving is considered, the value are computed thanks to the equations presented in (5.6).

$$i_j = \frac{i_{\text{load}}}{m}; \qquad \Delta i_j = \frac{\text{ripple}_{\%}}{100} \times m \times i_{\text{load}}; \qquad i_{l,j} = \frac{i_j}{k}; \qquad \text{and} \qquad f_{\text{sw}} = \frac{f_{\text{sw, app}}}{m} \tag{5.6}$$

The base case where there is no interleaving, the set of equations is computed as in (5.7). The effect of the interleaving is clearly highlighted in Δi_j and f_{sw}.

$$i_j = \frac{i_{\text{load}}}{m}; \qquad \Delta i_j = \frac{\text{ripple}_{\%}}{100} \times i_{\text{load}}; \qquad i_{l,j} = \frac{i_j}{k}; \qquad \text{and} \qquad f_{\text{sw}} = f_{\text{sw, app}} \tag{5.7}$$

5.2.2.1 Filter Sizing

The detailed circuits presented in **Fig. 5.6** are taken into account in order to compute the filter LC parameters thanks to the equations (5.8) to (5.10) and the values computed previously.

$$L_{\text{flt,j}} = \frac{(1-d) \times d}{\Delta i_j} \times v_{\text{LV}} \times T_{\text{sw}}; \qquad \text{with} \qquad T_{\text{sw}} = \frac{1}{f_{\text{sw}}} \tag{5.8}$$

$$L_{\text{flt,j+}} = L_{\text{flt,j-}} = \frac{L_{\text{flt,j}}}{2}; \qquad R_{\text{flt,j+}} = R_{\text{flt,j-}} = \frac{R_{\text{flt,j}}}{2} \tag{5.9}$$

$$C_{\text{flt,j}} = \frac{T_{\text{sw}}^2 \times (1-d) \times d \times v_{\text{LV}}}{8 \times L_{\text{flt,j}} \times \Delta v_{\text{load}}} \tag{5.10}$$

The structural difference between **Fig. 5.6(a)** and **Fig. 5.6(b)** comes from the control method, because there are two ways to obtain negative voltage at the output. Even though 2QSR is chosen, it is

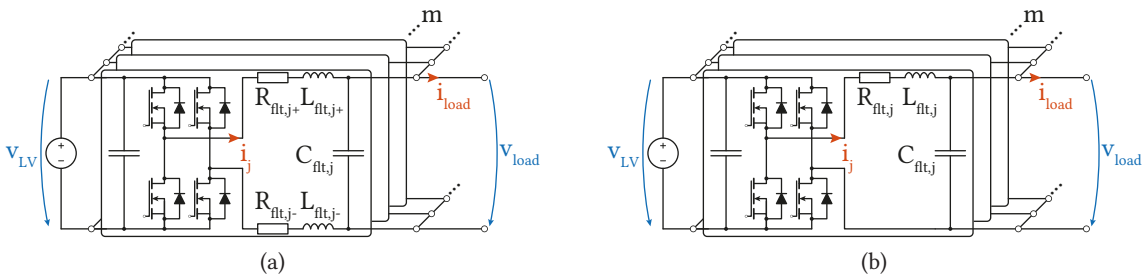


Fig. 5.6 Filter structure (a) when both legs are switching (mode 2QSR-B) and (b) when only one leg is switching (mode 2QSR-C).

still to be decided which mode for negative output voltage is the most advantageous in terms of implementation. The developed design tool allows to compare them in terms of volume and efficiency.

The design is stored only when the conditions expressed in (5.11) are fulfilled. It assures that the device can handle the current by being lower than its nominal value and that the continuous conduction mode is achieved by keeping the current positive, it means half of the ripple is lower than the DC value. That is why the devices are selected with a large I_{D25}, in order to have a reasonable number of devices to process the 2 kA.

$$i_{k,j} \leq I_{D25}; \qquad \text{and} \qquad \frac{\Delta i_j}{2} \leq i_{k,j} \tag{5.11}$$

The electrically viable designs are stored with the a collection of parameters that characterize it in an unique manner thanks to the simulation counter *simcounter*. Each design is then defined by the its electrical attributes with the number of *branches m*, the number of the MOSFET (#), the actual switching frequency of the device f_{sw}, the current per *branch* i_j, and its ripple Δi_j, the values of the *branch* filter $L_{flt,j}$ and $C_{flt,j}$, the number of MOSFET per switch k and finally the MOSFET current $i_{l,j}$.

This method is a typical optimization procedure as already referenced in the literature [88]–[90]. In this case the focus is on the *sub-converter* implementation, where the only intelligence is to discard the solutions that are not electrically feasible.

5.2.3 Losses

The losses computation is done in two parts: first, the semiconductor losses are computed and then the thermal part is tackled in order to discard thermally unrealistic combinations.

5.2.3.1 Semiconductor Losses

The core of this block is realized by a function that returns the switching and conduction losses of all four MOSFETs of the topology, the current per MOSFET $i_{l,j}$ is considered, then computed according to the equation presented in the previous chapter. The distinction between positive and negative output mode is done within the function. The summary of the losses is presented in **Tab. 5.4**. The two ways of operation for the synchronous rectification mode (previously called B or C, depending on the switching leg for the negative output current) are still under consideration, but the number of switching events is the same: there are always two devices switching, one conducting and one blocked, the losses outcome remains the same for both control modes.

Tab. 5.4 Summary of losses equations used in the tool.

Current (rms values)	switching	$i_{\text{out}} \times \sqrt{d_{T_\#}} \times \sqrt{1 + \frac{1}{3}\left(\frac{\Delta i}{i_{\text{out}}}\right)^2}$
	conducting	$i_{\text{out}} \times \sqrt{1 + \frac{1}{3}\left(\frac{\Delta i}{i_{\text{out}}}\right)^2}$
	blocking	0
Conduction losses	$i^2_{h,j,\text{rms}} \times R_{\text{DS}_{\text{on}}}$	$h \in [1,\ k];\ j \in [1,\ m]$
Switching losses	$(E_{\text{on}} + E_{\text{off}}) \times f_{\text{sw}}$	
Dead time losses	$2V_{\text{f}} \times t_{\text{dead}} \times f_{\text{sw}} \times i_{h,j,\text{dc}}$	
Reverse recovery losses	$Q_{\text{rr}} \times V_{\text{LV}} \times f_{\text{sw}}$	
Gate driver losses	$Q_{\text{g}} \times V_{\text{gs}} \times f_{\text{sw}}$	

In **Tab. 5.4**, $d_{T_\#}$ is the duty-cycle of $T_\#$, V_{f} is the forward diode voltage, t_{dead} is the dead-time introduced by the driver between the upper and lower switch, Q_{rr} is the reverse recovery charge, Q_{g} is the gate charge of the MOSFET and V_{gs} is the gate to source voltage applied by the driver on the MOSFET. All of those parameters are present in the input data set. The dead-time losses and reverse recovery losses arise from the dead-time added between the transitions, which prevents shoot-through in directing the current through the low-side body diode.

For every combination, the adequate losses are summed up to give the total switching and conduction losses of each MOSFET, as the high-side and low side component experience different losses. The overall sum is then computed in order to obtain the total losses for the 2 kA sub-converter.

5.2.3.2 Thermal Estimations

From the losses per device, the temperature is computed using the equivalent thermal resistance between junction and ambient, as depicted in **Fig. 5.7** for the IMS PCB. This is where the package of the MOSFET is taken into account: the layers and interfaces are modeled between the junction and the medium where the heat is evacuated. In the present case, it is air forced across a standard aluminum cooling heat-sink. The surface of each MOSFET is considered, then the adequate layers of PCB, metal, heat-sink or thermal grease are considered to obtain the equivalent thermal resistance. The computation is restricted to one direction, from the junction down to the ambient, where no surrounding components are taken into account. The main formula used is the one presented in (5.12).

$$R_{\text{th}} = \frac{e}{k \times A} \tag{5.12}$$

where e is the thickness of the material, k its thermal conductivity and A the area of the transfer.

Fig. 5.7 Sketch of the thermal interface between the chip and the ambient for a Insulated Metal Substrate (IMS) based Printed Circuit Board (PCB) mounted MOSFET. Because of the time constants of the system, only the steady-sate regime is taken into account.

The temperature of every device can be computed thanks to (5.13).

$$\Delta T = R_{\text{th}} \times P_{\text{losses}} \tag{5.13}$$

Following this step, the maximum temperature over the four devices is extracted and stored, because only the designs with junction temperature lower than the limit 120 °C are kept, the other designs are discarded.

5.2.4 Filter Design

The design of the filter consists in designing a magnetic structure that meets the electrical requirements and constraints [57], [86]. In order to do so, the *LC* filter is split into *L* and *C* design, where for both a database is the starting point of the process, keeping in mind the reality of implementation and available components. The goal is to obtain the most compact design.

5.2.4.1 Inductor Design Process

The design flow for the DC current inductor that is of interest is depicted in **Fig. 5.8**. The target value for the filter is considered at the worst operating point, when the duty-cycle is minimal. The minimal value of inductance to satisfy the requirements is then expressed in (5.14).

$$L_{\text{flt},j,\text{target}} = (v_{\text{LV,max}} - |v_{\text{out}}|) \times \frac{d_{\min}}{f_{\text{sw}} \times \Delta i} \tag{5.14}$$

For a given combination of m and f_{sw}, in considering the output current ripple, the desired $L_{\text{flt,j}}$ is calculated as electrical requirement. The variables expressed in (5.15) are considered for the filter design.

$$L = L_{\text{flt,j}} \qquad \text{or} \qquad \frac{L_{\text{flt,j}}}{2}; \qquad i_{\text{dc}} = i_j; \qquad i_{\text{ac}} = \Delta i_j; \tag{5.15}$$

From those variables, the characteristic currents i_{max} and i_{rms} are automatically computed as expressed in (5.16).

$$i_{\text{max}} = i_{\text{dc}} + \frac{i_{\text{ac}}}{2}; \qquad i_{\text{rms}} = i_{\text{dc}} \times \sqrt{1 + \frac{1}{3}\left(\frac{I_{\text{ac}}/2}{i_{\text{dc}}}\right)^2} \tag{5.16}$$

Two types of cores are considered, EQ and EE, based on ferrite and powder core materials. The EE cores give more freedom as they give the possibility to be stacked for a larger core cross section.

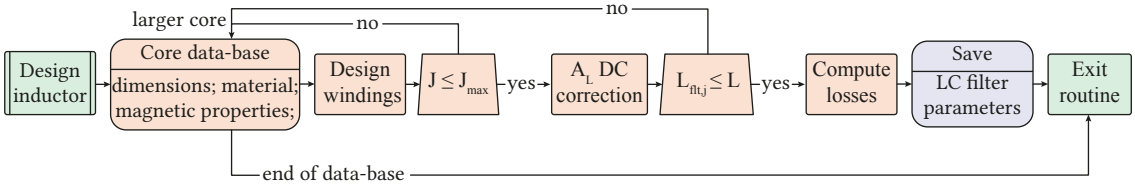


Fig. 5.8 Inductor design process algorithm.

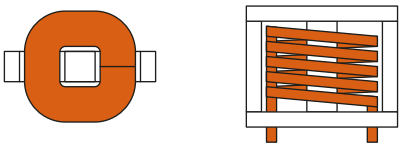


Fig. 5.9 Example of layout for an helical the inductor, terminations position and orientation to be determined during the implementation.

To design the copper flat wire windings, the window geometry is scaled with the appropriate correcting factors for winding insulation and utilization factor [91].

The process iterates on the number of turns of the inductor, which is expected to be rather low. The next step is to determine the wire size, because of the high-current DC nature of the inductor, the structure is considered to be of helical structure as sketched in **Fig. 5.9**. Then, as the windings are considered to be flat wires, filling the window area to use it at the window utilization factor K_u, in considering the standard $S_1 = 0.94$ winding insulation factor as detailed in [91] and a safety margin of $S_m = 0.9$. The wire width, thickness and area are determined using the equations (5.17) to (5.19).

$$w_w = S_1 \times S_m \times \text{width}_w \tag{5.17}$$

$$w_e = \frac{S_1 \times S_m \times \text{height}_w}{N} \tag{5.18}$$

$$A_w = w_w \times w_e \tag{5.19}$$

where w_w, w_e and A_w are the winding width, thickness and area respectively; width_w and height_w refers to the window area, taken from the core geometrical characteristics.

This computation gives an important information and allows to check the condition concerning the current density in the winding. For a given cross section of winding conductors, current density is evaluated considering predefined limit value that include the temperature dependence and respect the norm [92]. The condition is expressed in (5.20).

$$J = \frac{i_{\text{rms}}}{A_w} \leq J_{\text{norm}} \tag{5.20}$$

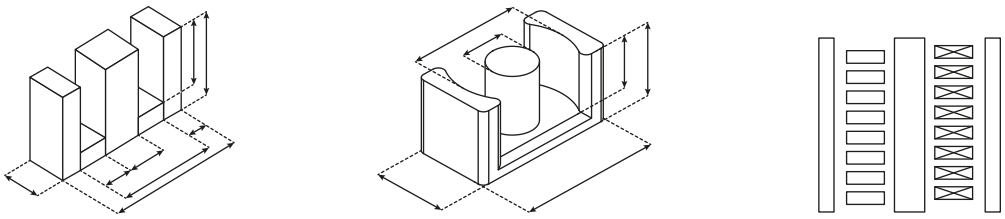
Then, the A_L value is adjusted to the DC value thanks to the data-sheet Ampere-turn characteristics as expressed in (5.21). Finally the inductance value is computed thanks to (5.22).

$$A_{L,\text{DC}} = A_{L0} + N_l \times i_{\text{pk}} \times \text{stack} \times \text{slope}_{\text{DCbias}} \tag{5.21}$$

$$L_{\text{design}} = A_{L,\text{DC}} \times N_l^2 \times 10^{-9} \tag{5.22}$$

In this set of equations, N_l is the number of turns considered in the l^{th} iteration, stack is the number of stacked cores and $\text{slope}_{\text{DCbias}}$ is a negative value corresponding to the decrease of A_L when the DC bias increases in the core. For ferrite cores, the A_L also allows to compute the value of the air gap. The 10^{-9} scaling factor is used in (5.22) because $A_{L,\text{DC}}$ is expressed in nH/turns^2.

At the end of the process, a set of parameters defining the core combination and windings is retrieved. Additionally, when inputting the electrical set point into the calculations, the core and winding losses, taking into account the skin effect, are computed [93]. The overall mechanical properties in terms of volume and weight complete the set of output parameters of the design.



(a) (b) (c)

Fig. 5.10 Core shape: (a) E core, (b) EQ core and (c) windings arrangement around the central leg.

5.2.4.2 Filter Core

The material and shape of the core are fundamental in the design because of their direct influence on the flat wire size, to explore the possibilities, several databases are implemented in order to find the most suited one. All the cores are considered gapped as stated from the standard manufacturer catalog, and their shape is depicted in **Fig. 5.10**.

Ferrite E Cores are considered because of the wide range of sizes in which they are available. The EI and EE configurations are considered to widen the possibilities. The intrinsic properties of the material make a low saturation of the flux density $B_{\text{sat}} \simeq 0.5\,\text{T}$. The product line is *Magnetics* ferrite E,I cores from 9 mm to 100 mm.

Powder EQ Cores are considered as the powder material allow a B_{sat} three times larger than the ferrite, around 1.6 T. This type of core cannot be stacked. As the central leg is circular, it makes the winding easier, and allows to reach higher window filling factor K_u. The database includes *Chang Sung* EQ special magnetic powder cores and *Magnetics* High Flux EQ cores.

Powder E Cores are considered because of their ability to be stacked, combined with the properties of powder material. Only EE configurations are considered, but taking into account several permeabilities for the same geometry. The window utilization factor K_u is lower as EQ as the square central leg and the need for space between windings for cooling purposes. The complete *Magnetics* Kool Mu EQ core catalog is considered.

5.2.4.3 Inductor Losses

Once the effective L value is checked and is above the target value, the losses of the combination can be estimated. They are divided into the winding losses and core losses.

The winding losses happen in the conductor that constitutes the windings. The main data taken from the core selection are the winding length as expressed in (5.23) and area.

$$w_l = MLT \times N \tag{5.23}$$

From this relation and considering the ripple at the switching frequency, the skin effect can be computed; only the AC part of the current causes this phenomenon. The set of equations used is described in (5.24) to (5.26). A practical approximation is used because of the low frequencies, to limit

the complexity of the computation. Anyhow, as the AC share of the current is low, the skin effect influence on the total resistance remains modest.

$$\epsilon = 503 \times \sqrt{\frac{\rho}{f_{\text{sw}}}} \tag{5.24}$$

$$A_{w,hf} = 2 \times \epsilon \times (w_w + w_e - \epsilon) \tag{5.25}$$

$$R_{\text{ac}} = \frac{\rho \times w_l}{A_{w,hf}} \tag{5.26}$$

where ϵ correspond to the skin depth, ρ is the copper resistivity in $\Omega\,\text{m}$ [94]. Then the effective area for the alternative part of the current is deduced from the rectangular geometry of the winding, before computing its resistance R_{dc} (5.27).

$$R_{\text{dc}} = \frac{\rho \times w_l}{A_w} \tag{5.27}$$

The winding or copper losses are then expressed as the sum of the DC and AC ohmic losses, as shown in (5.28), using the RMS values.

$$P_{\text{cu}} = R_{\text{dc}} \times i_{\text{dc}}^2 + R_{\text{ac}} \times i_{\text{ac}}^2 \tag{5.28}$$

The core losses are computed using the standard Steinmetz's equation (5.29) valid for a sinusoidal excitation, and with the coefficient given by the core manufacturer. Those are given for a permeability and a frequency.

$$P_{\text{fe}} = a \times B^b \times f^c \tag{5.29}$$

where a, b and c are the Steinmetz coefficient of the material, defined empirically from the B-H curve.

5.2.4.4 Mechanical Data

Weight of the inductor is the sum of the core weight taken from the data-sheet and the winding weight which is computed thanks to its length. The equation is given in (5.30).

$$W_L = W_{\text{core}} + w_l \times \rho_{\text{cu}} \tag{5.30}$$

where ρ_{cu} is the copper density, $8.98\,\text{g}\,\text{cm}^{-3}$.

The volume of the inductor is estimated considering the geometry depicted in **Fig. 5.11**.

At the end of the process, a set of parameters defining the core combination and windings is retrieved. The combination parameters also include the losses, and their characteristic value, as well as the overall mechanical properties in terms of volume and weight.

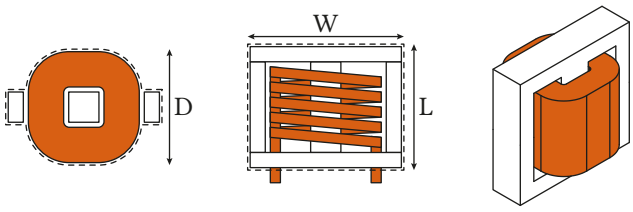


Fig. 5.11 Volume estimation of the inductor.

5.2.4.5 Capacitor Design Process

The target value for the output capacitor is given by (5.31), based on the Buck converter output capacitor sizing, and scaled to the *m branches* in parallel, where Δv is the relative output ripple.

$$C_{\text{flt},j,\text{target}} = \frac{1}{m} \times \frac{T_{\text{sw}}^2 \times (1 - d_{\text{min}})}{8 \times L_{\text{flt,j,target}} \times \Delta v} \tag{5.31}$$

The output capacitor is shared among all the branches. The goal is to find the overall smallest volume of capacitors to achieve $C_{\text{flt},j,\text{target}}$ with the *m branches* in parallel, with the possibility to have several paralleled capacitor in one branch. To this extent, a film capacitor database is created from *Vishay* MKT180 product line, with several capacitance values and their associated package for 63 V rated DC voltage.

The losses in the filter capacitors come from the Equivalent Series Resistance Ohm losses as described by (5.33), with the ESR scaled to the switching frequency, as detailed in (5.32).

$$R_{\text{ESR}} = \frac{\tan(\delta(f_{\text{sw}}))}{2\pi \times f_{\text{sw}} \times C_{\text{flt,j}}} \tag{5.32}$$

$$P_{\text{cap}} = R_{\text{ESR}} \times \frac{\Delta i_j}{N_{\text{cap}}}^2 \tag{5.33}$$

$$\tag{5.34}$$

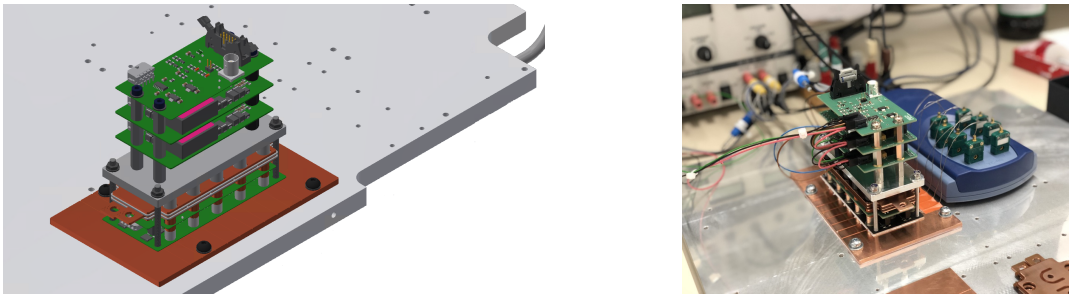
where $\tan(\delta(f))$ is the dissipation factor of the capacitor, at the frequency f, and N_{cap} the total number of parallel capacitors in the *sub-converter*.

5.2.5 Mechanical Considerations

5.2.5.1 Early Prototype

An early prototype of an half-bridge module is realized in order to verify the feasibility of operating PCB mounted MOSFETs in parallel. The final assembly is given in **Fig. 5.12**. It is composed by ten parallel MOSFET of the same family as ④, mounted on a IMS board for a better heat dissipation. The semiconductors are driven by a stage divided into one pre-driver and two drivers that amplify the complementary signals before reaching their gate. The assembly is designed in a layered approach, with a stacking of PCBs and bus-bars, sitting on a water cooled plate. More details are provided in **Sec. A.2.3**.

The goal of this first prototype is to gain experience with the implementation of parallel devices, their driving and the mechanical layout of the assembly. Unfortunately the adopted approach is not the best in terms of driving capability, because of a too complex structure that is not kept for the final implementation. Nevertheless, it is suited to drive the devices up to 100 kHz with a peak sink current of a few amperes. The key learnings of the experiments are about the good passive sharing of the current among devices: in both conduction and switching mode as well as a stable thermal behavior of the assembly.



(a) (b)

Fig. 5.12 Half-bridge module assembly: (a) CAD rendering and (b) picture with the thermal probes and acquisition system.

5.2.5.2 Volume Estimation

Based on the implementation of the early prototype of the module, some dimensions can be estimated. The semiconductor module is arranged as a half-bridge with the k devices in parallel. Two of those modules constitute the topology of the *branch* and are sharing one driver. The area required for the semiconductor part of the *branch* is defined in (5.35).

$$A_{\text{semiconductors}} = 2 \times k \times A_{\text{MOSFET}} \times 1.8 \tag{5.35}$$

where the 1.8 factor is a scaling to take into account the mechanics that comes around for the parallel connection of the devices.

The driver is not included as it is considered to be stacked on top of the modules, not requiring additional surface. On another hand, the volume is impacted by the driver as well as the mechanical arrangement that needs to be put in place to connect the modules to the filter. A constant 80 mm is considered for that, including connection layout as well as driver and heat-sink as sketched in **Fig. 5.13**.

The overall volume of the *branch* is computed as followed (5.36).

$$V_{\text{tot}} = 1.8 \times (V_{\text{semiconductors}} + V_{\text{fltr}}) = 1.8 \times (V_{\text{semiconductors}} + V_L + V_C) \tag{5.36}$$

Once again, the 1.8 scaling factor is present to account for extra volume related to element placement and interconnection, as well as interfaces to the input DC bus and the load.

5.2.6 Valid Designs

Only the designs whose filter prove to be realistic are passed in this last steps. The two key values are the overall volume and efficiency of the *sub-converter* because they enclose all the parts of the design.

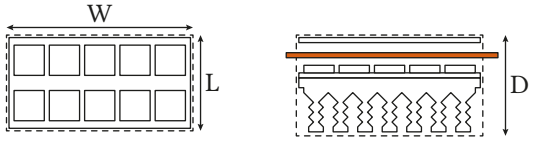


Fig. 5.13 Semiconductor volume estimation.

From the total losses, the efficiency can be derived as in (5.37).

$$\eta = \frac{1}{1 + P_{\text{tot}}/|P_{\text{out}}|}; \qquad \text{with} \qquad P_{\text{out}} = v_{\text{out}} \times i_{\text{out}} \tag{5.37}$$

Once those values are computed and stored, the adequate graphs are generated and presented in the next result section.

5.3 Optimization Results

After running the optimization routine for the different combinations some results and trends can be observed. They are described hereafter before analyzing the promising designs in detail.

5.3.1 Operating Mode

For the split L case, corresponding to mode B where both legs are switching, the smallest achievable volume is comparable to the case of a single L. As the database only contains a limited selection of cores, halving the inductance does not mean reducing the filter size by a comparable factor.

The efficiency is lower in the split L case because the conduction losses are predominant, lengthening the current path directly impacts losses. The best solution is to have the shortest path possible, which can be achieved with a single inductance because of the lowest series resistance R_{dc}.

The operation mode where only one leg is switching while the other is used as a polarity inverter (previously named mode C) is then adopted.

5.3.2 Powder EQ Cores

In this case, no stacking is possible, but for some combination a realistic filter design is produced. Nevertheless, the verification for the current density can never be passed: because of the high-current nature of the application, the condition on J is critical and discards a lot of designs. In the precise case of the EQ powder cores, there is no core able to handle the current with a lower current density than $750\,\text{A}\,\text{cm}^{-2}$, which is very high and requires specific and intensive cooling effort. No larger core from the considered manufacturer are available to complete the database.

5.3.3 Powder EE Cores

For the EE cores in powder material, some realistic design are given at the output of the process. Out of more than 12 000 electrically valid combinations and a total of 3900 realistic filters, a universe of 85 000 solutions is obtained and those results are now carefully analyzed.

Realistic Filters map is plotted in **Fig. 5.14** including information on m, L and the switching frequency f_{sw}. It is presented as a 3D map of points corresponding to the theoretical filter (in blue) needed for a given combination of m and f_{sw}. Some commercial products from *coilws* [95] are added (in green) for the sake of comparison, taken from their High Power Inductor E Series, ungaped coils. The realistic inductors are plotted (in orange) on the map: they are based on the 54 cores of the database augmented by the stacking up to three of the cores in parallel.

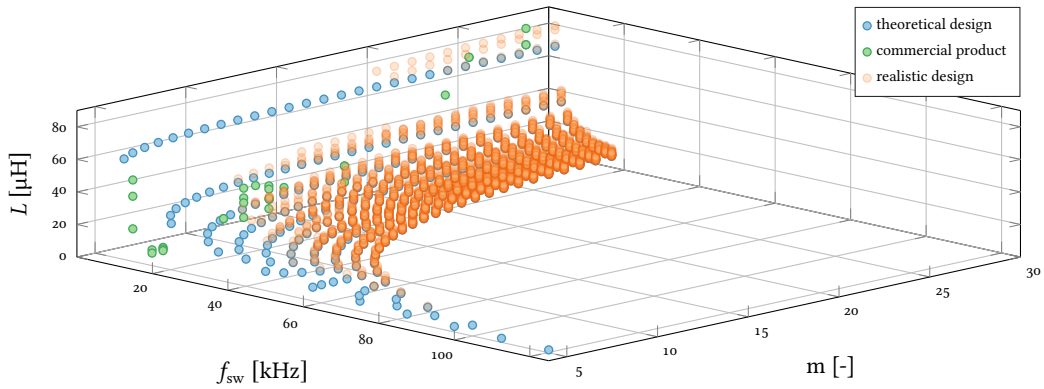


Fig. 5.14 *Branch* inductor map for a single L, with the 270 theoretical and the 3900 combinations of realistic designs. The higher the number of parallel *branches m*, the lower is the switching frequency thanks to the interleaving. The trails of orange dots represents the range of possible realistic filter for a given theoretical design.

A total number of 270 theoretical target inductances are given by the electrical combinations. Out of those, more than 3900 filters are realistic. The plot allows to visualize that the combinations with a very low number of parallel *branches m* (below 6) are not managing to obtain a realistic filter. The number of realistic filters for a combination augments when the current rating or target inductance decreases, or when the switching frequency increases.

The influence of the interleaving is seen in the maximum switching frequency reached in order to obtain $f_{\text{sw, app max}} = 500\,\text{kHz}$, that is reducing with the number of *branches m* increasing.

Volume vs Efficiency plot is given in **Fig. 5.15(a)** where the distinction between the various MOSFET is highlighted. On the zoomed version **Fig. 5.15(b)**, the discrete selection of the most efficient combination with the lowest volume is presented, considering restrictions on the numbers of *branches* and parallel devices: $m \leq 8$ and $k \leq 10$.

The entire map of theoretical design is presented with around 89 000 combinations. In the light blue are the combinations by the aforementioned criteria. The efficiency and volume are the two key values that allow to take into account the entirety of the sub-converter: the optimization is not done over each individual parts, but over their assembly.

5.3.4 Design Trends

The clearest trend in **Fig. 5.15** is about the distinction between the five types of MOSFETs directly depending on their package. The two smaller ones with an integration on a PCB (④ and ⑤) lead to the most compact designs while the larger is the MOSFET, the more the configuration occupies an important volume. On the plot it means a shift to the right. To highlight this phenomenon, a detailed plot is given in **Fig. 5.16(a)**. For a given combination of $m = 8$, $k = 6$, $f_{\text{sw}} = 37.5\,\text{kHz}$ and the same filter, the five designs have very different volume and efficiency solely because of the MOSFET choice.

The apparent trajectories of points that appear in **Fig. 5.15(b)**, are actually several numbers of k for the same combination of all other parameters, as highlighted in **Fig. 5.16(b)**. The selected combination is with $m = 7$, $k \in [2;\ 20]$, $f_{\text{sw}} = 42.8\,\text{kHz}$ and the device ④ with only a variation on the number of

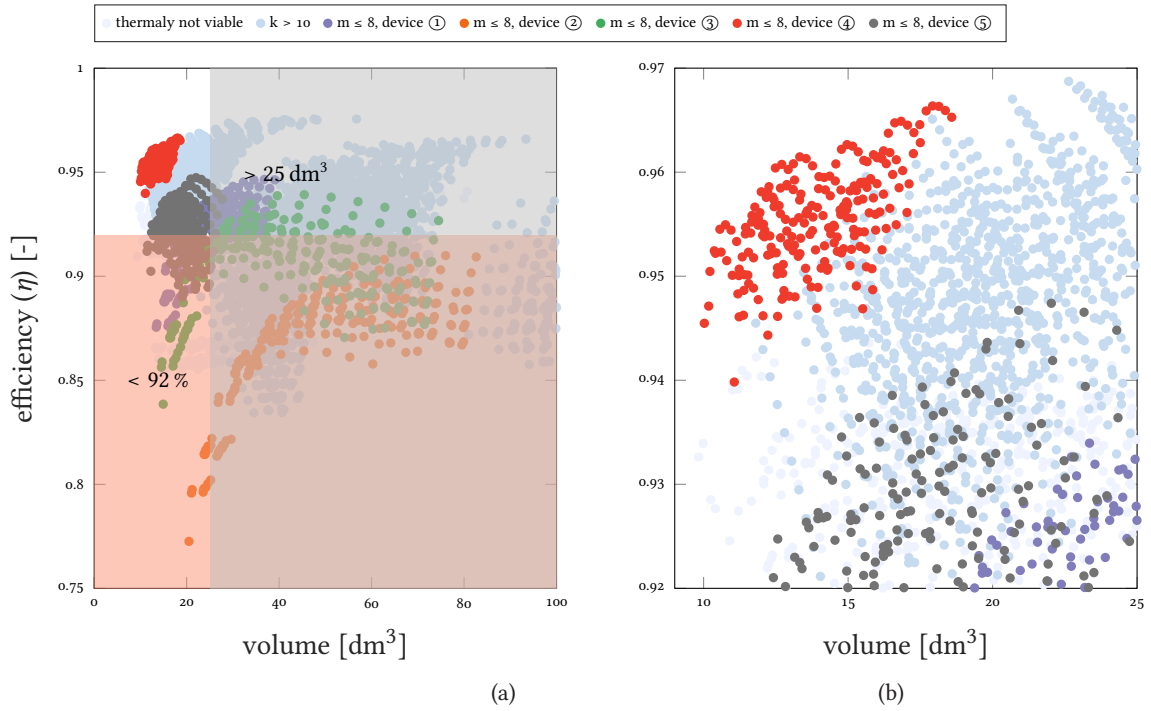


Fig. 5.15 Efficiency vs volume universe of solution for 2 kA and 10 V output: (a) entire set of points, with an highlighted on $k \leq 10$ and $m \leq 8$ (b) zoomed version in the area of interest. Grey area covers the volume above 25 l, and red area highlights the zone below 92 % efficiency. thermally not viable design; k > 10.

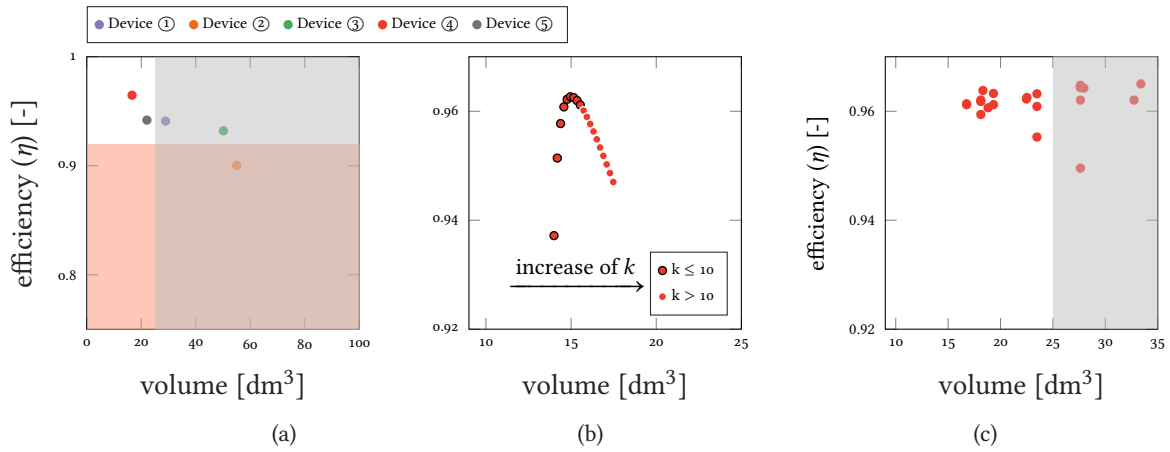


Fig. 5.16 Efficiency vs volume map detailed cases: (a) unique change of MOSFET component for a given configuration of $m = 8$, $k = 6$, $f_{sw} = 37.5$ kHz and the same filter (b) variation of $k \in [2;\ 20]$ for the same combination of all other parameters $m = 7$, $f_{sw} = 42.8$ kHz and the device ④ and (c) the spread caused by different filters on one configuration with $m = 15$, $k = 4$, $f_{sw} = 30$ kHz and the device ④.

parallel MOSFETs k. Keeping $k \leq 10$ in **Fig. 5.15** allowed to reduce the number of combination while keeping the local optimum of each combination. This parabola shape comes from the adaptation of external gate resistor that imposes a constant switching speed for all MOSFETs independently of the number of parallel devices k.

Another analysis that is possible is concerning the filter, where for one given electrical combination, several filter inductors are possible, spreading the dots according to the volume and losses in the designed inductor as can be seen in **Fig. 5.16(c)**. The configuration 9468 with $m = 15$, $k = 4$, $f_{sw} = 30\,\text{kHz}$ and the device ④ can be achieved with 21 different filters.

The combinations that have many possible filters are usually for the large numbers of *branches m*, what is already seen in **Fig. 5.14**.

The superimposition of those three trends applied to the ensemble of electrically valid combination leads to the complete universe of design plotted in **Fig. 5.15**. As already highlighted, a selection of around 200 designs with the MOSFET ④, $m \leq 8$, and $k \leq 10$ look promising as they are located in the upper left corner of the efficiency versus volume plots. It means those are designs with a high efficiency and a low volume, the objective is then to select the most optimal compromise between efficiency and volume.

5.4 Selected Design

5.4.1 Figure of Merit

In order to account for the volume as well as the efficiency of the system and to find the optimal solution, a figure of merit is introduced, as defined in (5.38), where a weight can be associated with the efficiency w_η and the volume w_V in order to account for the preference in one variable or the other in the choice of the design. As $\eta \in [0; 1]$ and the volume in the tenth of thousands cm^3 as used in the algorithm, a 10^{-5} multiplier is introduced in the equation to scale ψ_{design} and use simple weighting factors.

$$\psi_{\text{design}} = \frac{w_V \times \dfrac{V_{\text{design}}}{V_{\text{max}}}}{w_\eta \times \left(1 - \dfrac{P_{\text{losses}}}{P_{\text{out}}}\right)} \times 10^{-5} \tag{5.38}$$

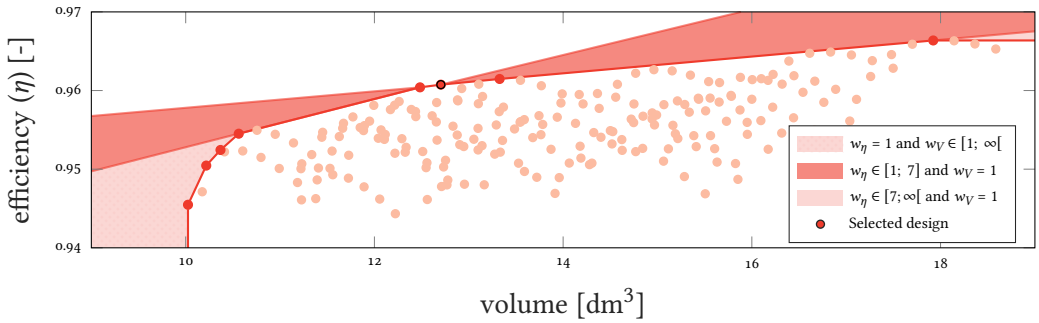


Fig. 5.17 Optimal designs front highlighted by the red line. Three areas are then filled depending on the weight given to the efficiency w_η and the volume w_V. On the one hand, when the focus is on the weight ($w_V > w_\eta$) the preferred designs are compact but their efficiency is 2 % lower than the most efficient designs. On the other hand, when the efficiency weight is preponderant ($w_\eta > w_V$), the designs are in the most efficient but almost two times larger than the most compact designs. The selected design is a compromise where the efficiency is slightly advantaged with $w_\eta = 2$ and $w_V = 1$. The numbers of the combinations is the combination and filter identifiers, a unique way to distinguish the designs.

As already highlighted in **Fig. 5.15(b)**, a selection of attractive designs with the MOSFET ④, $m \leq 8$, and $k \leq 10$ is located at the upper left corner of the efficiency versus volume plots. They are displayed in **Fig. 5.17**, where a front is defined thanks to the figure of merit ψ_{design} and the sweep of the associated coefficients w_η and w_V.

With $w_\eta = 2$ and the volume $w_V = 1$, a unique design can be selected. Out of the two competing solutions which are only differing by k, the one with the lower utilization factor is preferred. The combination circled in **Fig. 5.17** is the chosen design, where $m = 8$. Those eight parallel *branches* rely on the design detailed hereafter.

5.4.2 Branch Design

Narrowing down the universe of results from **Fig. 5.15** to **Fig. 5.17** allows to select a design, it is the most optimal in terms of volume and efficiency. Every part of this design is described hereafter, from the components, the *branch* and up to the *sub-converter* level, out of the two competing solution, the one with the lower utilization factor is preferred, they are only differing by k.

5.4.3 Full-Bridge Switching Cell

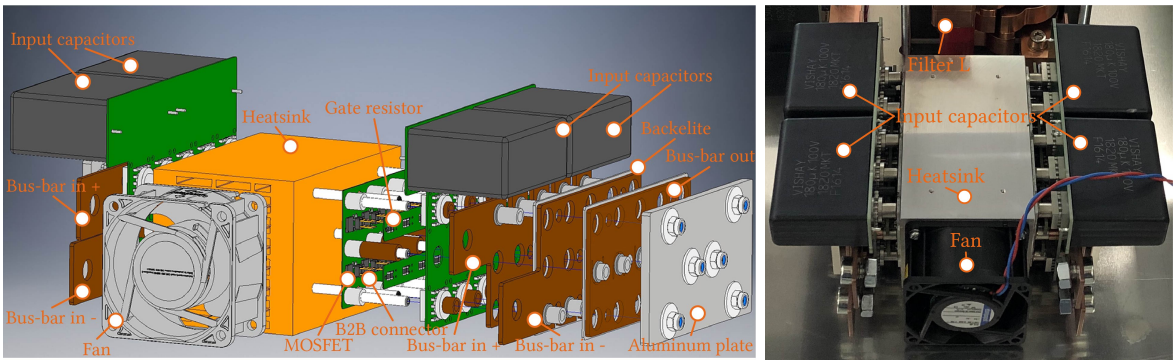
The design of the basic *branch* includes $k = 6$ MOSFETs devices in parallel, that are switched at 50 kHz and used at a conservative utilization factor, around 20 %. The summary of the semiconductor part of the design is given in **Tab. 5.5**. Unfortunately, at the time of the design, the MOSFET reference of the optimization was not available, imposing a change to a very similar one, whose characteristics are very close but differs for some parameters, *e.g.* $R_{\text{DS}_{\text{on}}}$ is 15 % larger. The heat-sink should dissipate the 90 W of losses produced by the semiconductor stage of the branch.

Additionally, some limitations in the availability of the film capacitors enforced some changes in the final implementation compared to the theoretical design. Nevertheless, the realized semiconductor module is a half-bridge and is represented in **Fig. 5.18**. The module is constituted of a stack comprised of (from left to right) the power PCB hosting the MOSFETs, the gate accessing PCB with the gate resistors and connectors, and the copper bus-bars for DC in and the middle point, isolated with Bakelite. The assembly is then pressed against the heat-sink with an additional aluminum plate that comes on top, as detailed in **Fig. 5.18(a)**.

The assembly of two semiconductor modules into the full-bridge topology of the *branch* is shown in **Fig. 5.18(b)**, where each of them is pressed on opposite sides of a square profiled heat-sink. An additional fan forces the air through the heat-sink, to bring the thermal resistance below $0.20\,\text{K}\,\text{W}^{-1}$. The full-bridge gate driver is not shown in this **Fig. 5.18**, but it is mounted on top of the assembly, sitting above the input film capacitors. It is the interface with the controller, embedding protection features, additional logic for the operation of the switches and that is connected through cables to the gate accessing PCB.

Tab. 5.5 Semiconductor characteristics of the selected *branch* design.

Device	Switching frequency	*branch* current	*branch* ripple	Parallel devices	Device current	Utilization factor
④	$f_{\text{sw}} = 50\,\text{kHz}$	$i_j = 250\,\text{A}$	$\Delta i_j = 16\,\text{A}$	$k = 6$	$i_{l,j} = 42\,\text{A}$	0.174



(a) (b)

Fig. 5.18 Detailed views of the semiconductor assembly (a) exploded view on the heat-sink and (b) realization of the full-bridge switching cell.

5.4.4 Filter Characteristics

The values of the *branch LC* filter in the design are: $L_{\text{fltr},j} = 8.3\,\mu\text{H}$ and $C_{\text{fltr},j} = 800\,\mu\text{F}$. The core, winding characteristics are gathered in **Tab. 5.6**, and the implemented capacitor part is detailed in **Tab. 5.7**. The capacitors are paralleled on a PCB which is directly interfaced to the output bus-bars of the branch.

For the inductor part, the windings are machined from a thick copper plate. Two standoff copper pieces allow the electrical connection between the turns, which are are linked to the base-plate through insulators. The assembly of cores is held together by aluminum clamps, and a sheet of Kapton isolates the windings from the core. Its overall volume is 1.45 l and a detailed representation is given in **Fig. 5.19**.

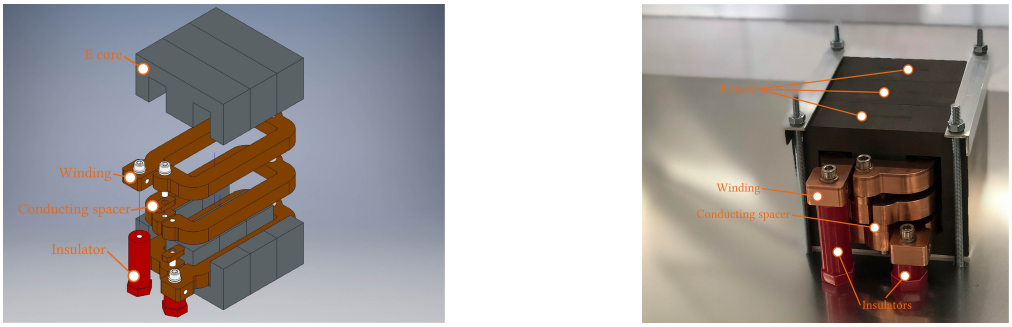
Tab. 5.6 Filter inductor characteristics of the selected *branch* design.

Core reference	Dimensions	Permeability	A_{L_0}	A_{L}	Core weight	Core stack
Magnetics 00K114LE060	$114.3 \times 46.18 \times 34.93\ \text{mm}^3$	60 μ	$445\,\text{nH/turns}^2$	$330\,\text{nH/turns}^2$	720 g	3

Number of turns	Inductance	Flat wire width	Flat wire thickness	Winding resistance	Peak flux density
$N = 3$	$L_{\text{eff}} = 8.9\,\mu\text{H}$	16.7 mm	14.3 mm	$R_{\text{dc}} = 80\,\mu\Omega$	$B_{\text{max}} = 0.22\,\text{T}$

Tab. 5.7 Filter capacitor characteristics of the selected *branch* design.

Capacitor reference	Dimensions	Capacitance	Parallel capacitors per *branch*	Total capacitance
Vishay MKT1820715065	$18.5 \times 35.5 \times 43.0\ \text{mm}^3$	150 µF	6	900 µF



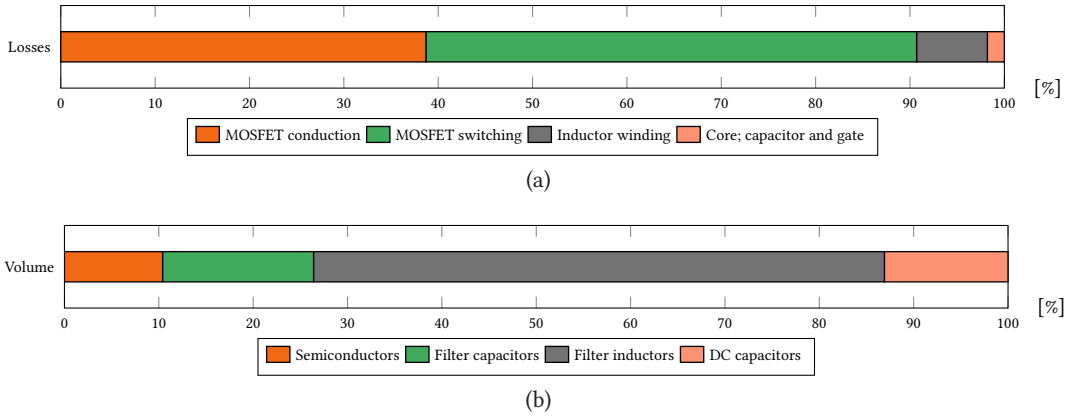
(a) (b)

Fig. 5.19 Details of the inductor implementation (a) exploded view and (b) isometric view of the final assembly.

5.4.5 Overall Losses and Volume

At the considered operating point applying 10 V on the load, the losses in the 2 kA converter sum up to 820 W, with a losses breakdown given in **Fig. 5.20** (a) considering semiconductor and filter losses, and resulting in an efficiency of 96 %. The adaptation of the gate resistance value is the key element to establish the ratio between conduction and switching losses [96]: the switching time is defined constant at 300 ns for the switch, then depending on the MOSFET characteristics and number in parallel k, the external gate resistor is computed to obtain such switching time. This method allows to compare semiconductors on a fair basis.

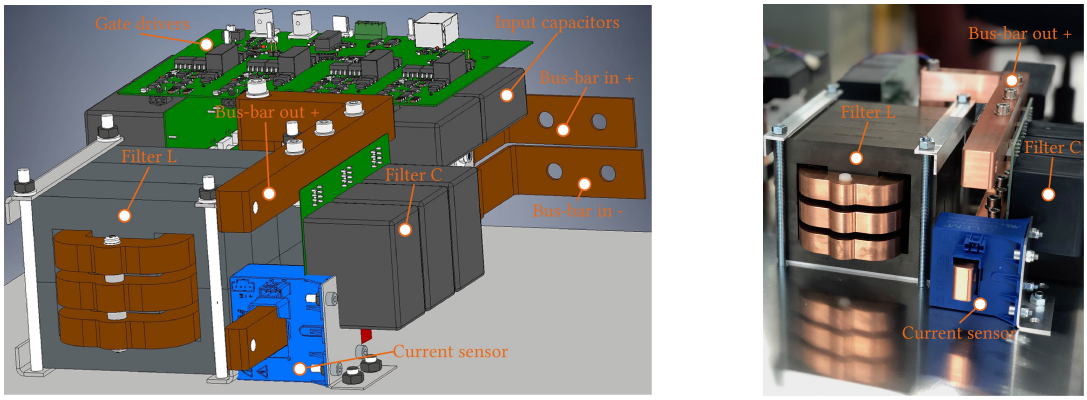
The total volume estimation of the components of the converter is around 13 l, with a sharing given in **Fig. 5.20(b)**. The main element of this design is the filter inductor which occupies 60 % of the total volume. With the adopted *branch* implementation, whose detailed assembly is given in **Fig. 5.21**, the global footprint of the *branch* is $210 \times 360 \times 115\text{mm}^3$, summing up to 70 dm^3 for the whole converter. That end result deviation from the original estimation comes from adding essential elements such as the appropriate heat-sink, some additional bus-bars to interconnect with the source and the load cables or mechanical pieces to keep the assembly together.



(a)

(b)

Fig. 5.20 Split of the *branch* (a) losses and (b) volume.



(a) (b)

Fig. 5.21 Details of the *branch* implementation (a) CAD rendering and (b) final implementation. It includes every element of the design and all the mechanics required to tied it to the base plate in a compact layout: it includes the gate driver, the output capacitor bank, the bus-bars and the current sensor.

5.4.6 Branch Driver

Each *branch* is driven by a dedicated circuit board, which is the interface between the power modules and the control platform (detailed further in **Sec. 6.5.1**). The driver needs to command the four switches of the full-bridge topology, from two controller generated digital command signal, one for each leg. An additional digital input used as an *enable* signal and two analogue outputs complete the I/Os of the driver. They are image of the output current and either a voltage or a temperature depending on the selected signal to transmit.

From the leg control signal, the complementary waveform is created locally on the board with a fixed dead-time, before being fed to an isolated driving stage that allows to match the resulting input capacitance and the peak current to be able to drive the six parallel MOSFETs. Another part of the board is dedicated to protection in order to have embedded safety at the *branch* level and signal conditioning to communicate with the controller using correctly scaled signals. Each driver is supplied with external auxiliary power supplies. The controller is depicted in **Fig. 5.22**.

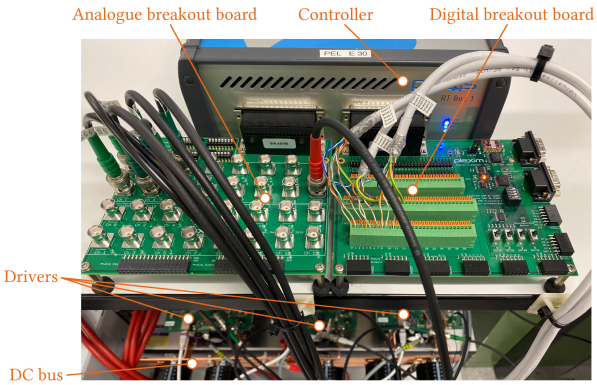


Fig. 5.22 Controller and breakout boards for communication with the drivers.

5.5 Experimental Results

5.5.1 Filter Inductor

Several tests are conducted to verify the performances of the prototyped branch. The first test consists in verifying the inductance value at 250 A. To this extent, the inductor is tested with the power choke tester *DPG10* [97]. The result of the test is provided in **Fig. 5.23**, where the measured inductance is 8.41 µH at the rated current for a target value of 8.9 µH, which is less than 10 % of deviation from target value.

5.5.2 Static Tests in Open-Loop

In order to test the *branch* at its nominal current and voltage, a load composed of several high-current air cooled inductors is wired with adequate cross section cables, for a total equivalent inductance around 254 µH, with a current rating above 750 A and different configurations with either an equivalent resistance of $R_{\text{loadA}} = 25\,\text{m}\Omega$, $R_{\text{loadB}} = 31\,\text{m}\Omega$ or $R_{\text{loadC}} = 44\,\text{m}\Omega$, it is depicted in **Fig. 5.24(a)**.

At the entry side of the branch, a DC power supply rated at a maximum of 20 V and 2250 A [98] is connected. Finally, in terms of instrumentation, a wide-band power analyzer *D6100* [99], with an external tri-axial shunt resistor rated for 300 A for the load side and 100 A for the source side, a 500 A current probe [100] in combination with a 500 MHz digital oscilloscope [101] are employed to obtain efficiency and waveforms from the functioning prototype.

The semiconductor stage is tested using an open-loop control, where the degree of freedom is the modulation index set by the controller, similar as the duty-cycle of the PWM modulating the switching leg. The set-point to reach the nominal current is defined considering the DC power supply at its 20 V maximum, a duty-cycle around 48 % for T_1, and using the load in configuration B with the low resistance $R_{\text{loadB}} = 31\,\text{m}\Omega$. It leads to an output voltage of 7.9 V and an output current of 255 A. The nature of the power supply makes the losses in the topology very current-driven, the voltage having only a lesser impact on them, that is why this operating point is legitimate to evaluate experimentally the prototyped design at its nominal current.

An infrared picture of the switching stage is captured during the test at this operating point and shown in **Fig. 5.24(b)**, where the semiconductors can be identified in the stack, still the temperature of their case remains in an acceptable range.

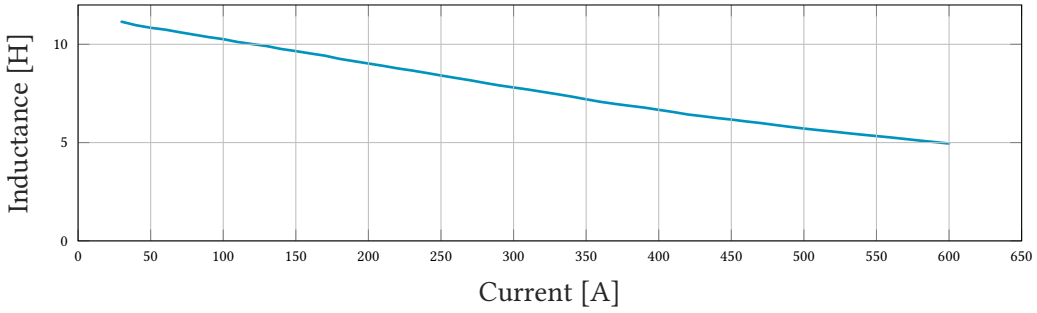
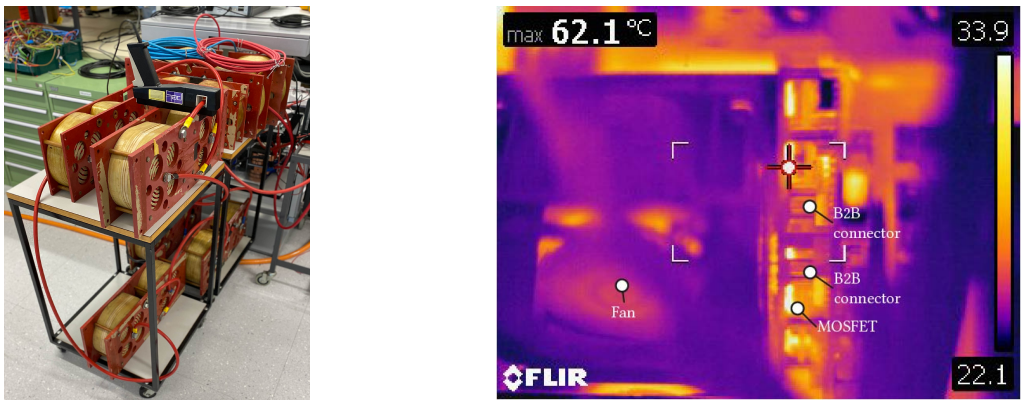


Fig. 5.23 Test result plot from the power choke tester, inductance L as a function of the current. The test sweep the current from 0 A to 600 A. The target value to be reached is 8.9 µH at 250 A.



(a) (b)

Fig. 5.24 Details of the test setup (a) inductive load and (b) infrared capture of the switching module at the operating point 6.5 V, 255 A. One of the switching MOSFET can be seen warmer where the target points.

Additionally, an outlook of the measured data at this operating point is provided in **Fig. 5.25**. The oscilloscope capture allows to visualize the evolution of the input voltage among others, where spikes can be identified when the switching events are happening, this is due to a weak DC bus capacitance, but their amplitude remains below 20 % of the 20 V input which is acceptable. Also, it can be seen that for the given operating conditions the peak-to-peak output current ripple is very low, and measure to be 1.9 A peak-to-peak thanks to the power meter, which is respecting the 1 % constraint given in the requirements.

The power meter allows to get a precise reading on the input and output power as well as a verification of the average values that can be read on the oscilloscope. For the 255 A operating point with the load C, the efficiency is $\eta_{\text{prototype}} = {}^{1993\,\text{kW}}/_{2330\,\text{kW}} = 86\,\%$.

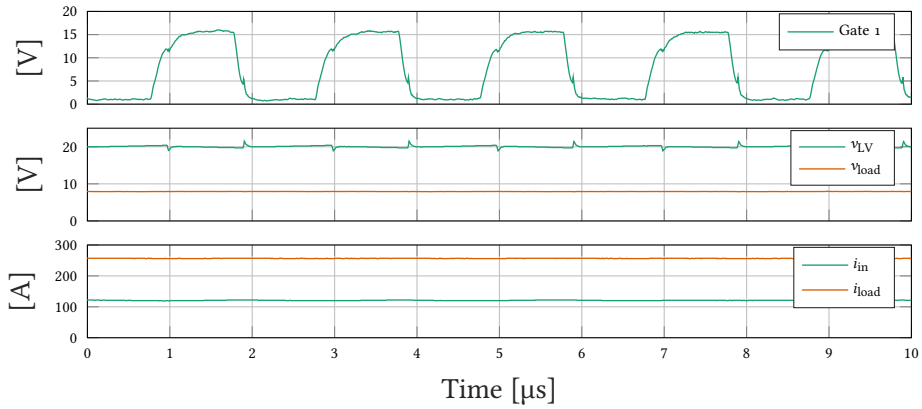


Fig. 5.25 Oscilloscope capture for the *branch* 1 operating with 7.9 V, 255 A at the output, operated with an open-loop control, where the set-point is defined as 48.4 % duty-cycle. i_{load} is measured with an external current probe.

In order to reach the nominal 10 V operation, the resistivity of the load should be increased. In this specific case, as only discrete elements are available for the wiring of the load, the reached value is $R_{\text{loadB}} = 44\,\text{m}\Omega$. This is not exactly matching the nominal current, leading to a second considered operating point at 10 V, 224 A. The waveforms are very similar to the one presented in **Fig. 5.25**, with the main change being the duty-cycle.

The data provided by the various load configurations is plotted in **Fig. 5.26**, based on the output current and voltage as well as the total losses of the system. The projections on the axis planes given on the plot show the trends whilst the experiment is performed on several loads.

This **Fig. 5.26** gathers lots of informations, the main part of it is the 3D plane of the total losses of the system that are collected for various loads. As expected, the losses increase with the load current or the load voltage. Regarding the projections, the v_{load} versus i_{load} is simply three lines corresponding to the three different resistance of the three loads.

There is quite a difference between the theory and the reality of implementation where the efficiency is lower than expected. This can be explained by several factors, the first one is the change in the selected MOSFET for the implementation: its $R_{\text{DS}_{\text{on}}}$ is 15 % higher than the one considered in the simulation. With this difference, the conduction losses are increased by the same ratio, bringing the efficiency down. The second one is the addition of five aluminum electrolytic capacitors on the DC bus, to help with the voltage stabilization, with an equivalent series resistance of several mΩ leading to another extra tenths of watt of losses, this is to be compared with the 100 W losses that should theoretically be released by the converter.

The investigations show that the difference comes from the parasitic resistance that were not taken into account in the optimization routine. Those parasitics comes from the bus-bars: they are unavoidable and mandatory for any implementation and would be equivalent for any design. By its nature, the

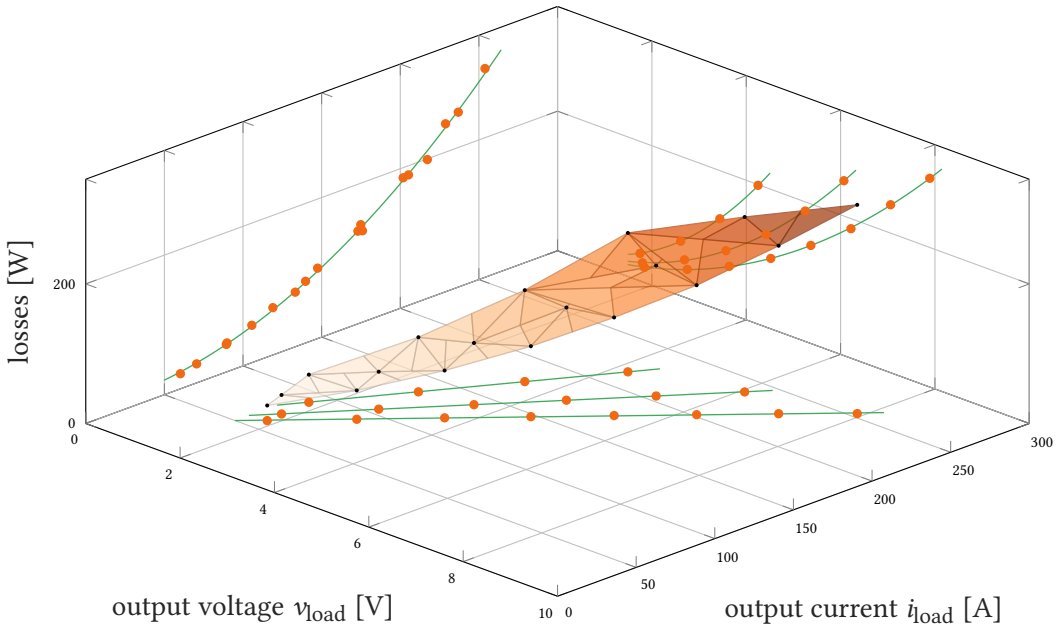


Fig. 5.26 Loss map for various load configurations and projection of the points of the axis planes where the dependence on the load can be highlighted.

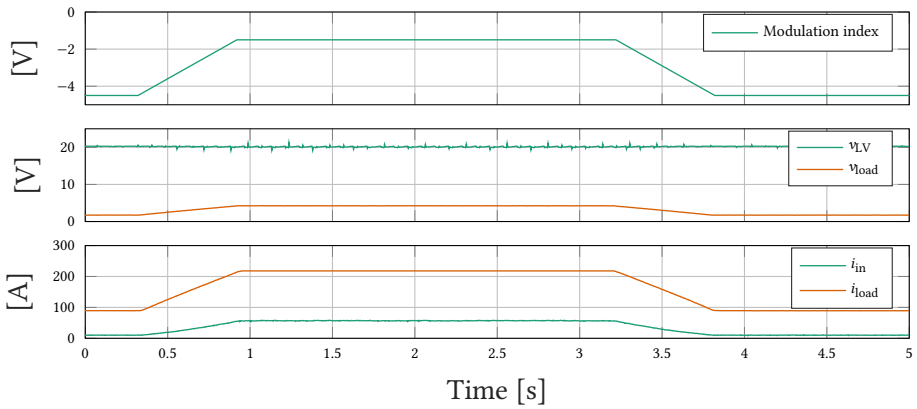


Fig. 5.27 Oscilloscope capture for the *branch* 1 operating in open-loop between 90 A and 225 A, where the set-point is defined as a change between 15 % and 29 % and a change rate limited around 200 A s^{-1}. The modulation index is set as an output of the controller and i_{load} is measured with an external current probe.

power supply with its high-current low-voltage output is very sensitive to any resistance: even the lowest when combined to high current leads to a measurable voltage drop. This would result in an offset of the entire design space solution towards the bottom of the plot. The main message is that the selected design would still remain the most optimal one.

5.5.3 Dynamic Tests in Open-Loop

A dynamic test can also be conducted, in a very primitive way to mimic the nominal cycle of the converter. A rate-limited change between 15 % and 39 % duty-cycle is performed and the waveforms are given in **Fig. 5.27**, it corresponds to a change between 72 A and 240 A in 20 ms.

The same parameters as before are kept for the acquisition, in order to get the key variations of the signals of interest that are the input and output voltages and currents. The response is as expected with a smooth transition between the two operating points.

5.6 Conclusions

The path from the specifications, to the practical realization of a high-current, low-voltage power converter elementary brick is defined. Once the requirements are defined, the adopted topology and modes of operation are established. Then, in order to define the most suited structure of the whole converter, the key elements are modeled and used within an optimization algorithm that defines a whole universe of designs, according to the range of swept parameters. From these multiple possibilities, a figure of merit is constructed to highlight the best design accommodating the volume and efficiency constraints. After the characterization of this optimal design, an implementation that takes into account the reality of component sourcing and machining capabilities is realized. Finally, tests are conducted in order to verify the implementation against the expectations, in a set of satisfying outcomes.

In order to reach the output ratings of 2000 A and ±10 V, the *sub-converter* is split into eight identical *branches* whose output ratings are 250 A and ±10 V. For an effective *branch* switching frequency of 50 kHz and a full interleaving of the eight branches, the output apparent switching frequency is

expected to be 400 kHz. Each *branch* is composed by four switches arranged in two half-bridges: one is switching while the other one is used as polarity inverter. The switches are themselves composed by six MOSFETs in parallel, the selected ones are rated for 60 V and used at 20 % of their nominal current to stay within the thermal capabilities of the device, because of its *PowerFLAT* package which requires to be integrated on a PCB. In the output of the switching leg is placed the *L* part of the output *LC* filter, designed as a three turns, powder EE core helical inductor. The output capacitor is composed of six standard film capacitor.

The results of the experiment show a promising electrical behavior where the output waveforms are matching the expectations. Nevertheless, some discrepancies in the efficiency number appear compared to the simulation, due to the parasitic resistances of the interfaces (bus-bars and connections).

6
Sub-Converter Interleaving and Control

This chapter presents the control of multiple modules in parallel, taking the optimal sub-converter *design previously determined, with eight* branches *in parallel. The control system design is carried out, implementing adequate controllers and tunning them to achieve required performances. The experimental results are collected from three realized* branches *operated in parallel, both in steady-state and dynamic operation of the system.*

6.1 Control Objectives

The control is introduced with the goal to track the current reference within the defined output range in an optimal manner, with limited delay and contained response. Namely, the goal of the control is to regulate the output voltage across the output capacitor to follow the current reference. According to the nature of the load, the current flowing through it is established accordingly, up to the limit of 2 kA for the sub-converter. To this extend, the voltage across the output filter capacitor is measured as well as the current at the output of each *branch* and the common input voltage. Variations are expected in the input voltage within the range of 24 V±6 V as well as in the value of the inductance filter because of manufacturing accuracy.

The control should keep the output stable even when the load, the input DC voltage and the reference change. The control scheme is detailed in the following section **Sec. 6.1.1**.

6.1.1 Control Scheme

The adopted topology is depicted in **Fig. 6.1(a)**. However, as the parallelization of voltage source is conflicting for the control, the output capacitance filters are merged into one as depicted in **Fig. 6.1(b)**.

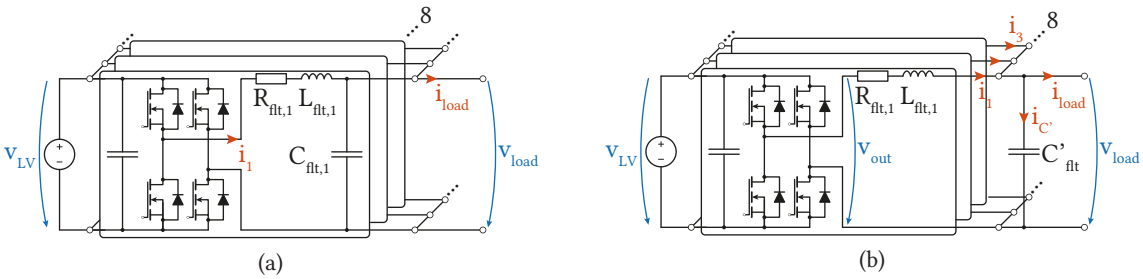


Fig. 6.1 *Sub-converter* electrical scheme: (a) C in the *branch* and (b) equivalent scheme for the control with a common C'.

The goal is to control the voltage across the output capacitance: the output voltage is the same for all branches, and decoupled by the *branch* filter inductor to control its current.

To control the voltage v_{load} across the capacitor C'_{flt} the current $i_{C'}$ through it needs to be controlled. The voltage and current of a capacitor are related as in (6.1).

$$i_{C'_{\text{flt}}} = C'_{\text{flt}} \times \frac{d\, v_{\text{load}}}{dt} \qquad \Rightarrow \qquad v_{\text{load}} = \frac{1}{C'_{\text{flt}}} \times \int_0^T i_{C'_{\text{flt}}}\, dt \tag{6.1}$$

Using the Laplace transform and considering the location of the capacitor in the circuit, the equation (6.2) is obtained.

$$v_{\text{load}} = \frac{1}{s\, C'_{\text{flt}}} \times (i_{\text{load}} - \sum_{j=1}^{8} i_j) \tag{6.2}$$

Finally, the transfer function linking the output v_{load} to the individual *branch* current i_j is given in (6.3). In order to control the output voltage, the averaged sum of the filter inductor currents i_j needs to be controlled.

$$G_{C'_{\text{flt}}}(s) = \frac{v_{\text{load}}}{i_{\text{load}} - \sum_{j=1}^{8} i_j} = \frac{1}{s\, C'_{\text{flt}}} \tag{6.3}$$

At the individual *branch* level, the voltage and current on the filter inductor are related as in (6.4).

$$v_{L_{\text{flt}}} = L_{\text{flt}} \times \frac{d\, i_j}{dt} \qquad \Rightarrow \qquad i_j = \frac{1}{L_{\text{flt}}} \times \int_0^T v_{L_{\text{flt}}}\, dt \tag{6.4}$$

The Laplace transform and Kirchhoff's laws in the *branch* , as detailed in (6.5) and (6.6), are used to obtain the transfer function.

$$i_j = \frac{1}{s\, L_{\text{flt}}} \times v_{L_{\text{flt}}} \tag{6.5}$$

$$v_{\text{out}} = i_j \times R_{\text{flt}} + s\, i_j \times L_{\text{flt}} + v_{\text{load}} \tag{6.6}$$

Finally, the transfer function linking the output i_j to the input $(v_{\text{out}} - v_{\text{load}})$ is given in (6.7). The control of i_j is made through v_{out} which is the *branch* output voltage.

$$G_{L_{\text{flt}}}(s) = \frac{i_j}{v_{\text{out}} - v_{\text{load}}} = \frac{1}{R_{\text{flt}} + s\, L_{\text{flt}}} = \frac{K_{\text{flt}}}{1 + s\, T_{\text{flt}}} \tag{6.7}$$

with $K_{\text{flt}} = 1/R_{\text{flt}}$ and $T_{\text{flt}} = L_{\text{flt}}/R_{\text{flt}}$.

Globally, the control scheme is done using two cascaded loops for the inductor current and the capacitor voltage, tuned according to the traditional magnitude and symmetrical optimum criteria [102].

6.1.2 Inner Control Loop - Inductor Current

The open loop transfer function of the inner system is written in (6.8)

$$H_{\mathrm{OL,i}}(s) = C_1(s) \times d_{\Sigma 1}(s) \times G_{L_{\mathrm{flt}}}(s) = \frac{1 + s\,T_n}{s\,T_i} \times \frac{K_{\Sigma 1}}{1 + s\,T_{\Sigma 1}} \times \frac{K_{\mathrm{flt}}}{1 + s\,T_{\mathrm{flt}}} \tag{6.8}$$

where $C_1(s)$, $d_{\Sigma 1}(s)$, $G_{L_{\mathrm{flt}}}(s)$ are transfer functions of the controller, the converter delay and the plant. In this case the plant is the series *RL* circuit. By choosing the controller time constant T_n to be equal to the plant time constant T_{flt}, the real zero of the controller cancels out the plants pole. Therefore, closed loop transfer function of the system becomes as in (6.9).

$$H_{\mathrm{CL,i}}(s) = \frac{H_{\mathrm{OL,i}}(s)}{1 + H_{\mathrm{OL,i}}(s)} = \frac{K_{\Sigma 1} \times K_{\mathrm{flt}}}{K_{\Sigma 1} \times K_1 + s\,T_i + s^2\,T_i \times T_{\Sigma 1}} = \frac{1}{1 + s\,\frac{T_i}{K_{\Sigma 1} K_{\mathrm{flt}}} + s^2\,\frac{T_i \times T_{\Sigma 1}}{K_{\Sigma 1} \times K_1}} \tag{6.9}$$

Applying the magnitude optimum design principle to the equation (6.9), leads to the controller gains given in (6.10).

$$T_n = T_{\mathrm{flt}} = \frac{L_{\mathrm{flt}}}{R_{\mathrm{flt}}} \qquad \text{and} \qquad T_i = 2\,K_{\Sigma 1} \times K_{\mathrm{flt}} \times T_{\Sigma 1} = 2 \times 1 \times \frac{1}{R_{\mathrm{flt}}} \times 1.5\,T_{\mathrm{sw}} \tag{6.10}$$

where the equivalent delay of the converter in terms of its current control is equal to $1.5\,T_{\mathrm{sw}}$, it is a product of the delay due to sampling ($0.5\,T_{\mathrm{sw}}$) and converter postponed action for a single switching period (T_{sw}).

For the design of the parameters of the current control, the small time constant used for the setting of the maximum bandwidth is not the apparent switching frequency. The apparent switching frequency only affects a part, in this case one eighth of the total energy flow. In order to account for the eight interleaved *branches* , the switching frequency is the considered to be the output apparent switching frequency, which is eight times higher than the effective switching frequency of each *branch* : $T_{\mathrm{sw}} = 1/f_{\mathrm{sw,\,app}}$.

6.1.3 Outer Control Loop - Capacitor Voltage

The plant to be controlled is a pure integrator since the objective is to control the voltage across the capacitor C'_{flt}. The inner control loop has to be represented in a simple way, so as to make the analysis of the outer control loop feasible. Since the current response is fast and well damped, it is considered as a good approximation if the inner control loop is represented as a first order delay system, as shown in (6.11). Open-loop and closed-loop transfer function of the outer control loop are provided in (6.12) and (6.13), respectively.

$$H_{\mathrm{CL,i}}(s) = \frac{1}{1 + s\,2 \times T_{\Sigma 1} + s^2\,2 \times T_{\Sigma 1}^2} \simeq \frac{1}{1 + s\,2 \times T_{\Sigma 1}} \tag{6.11}$$

$$H_{\mathrm{OL,v}}(s) = C_2(s) \times d_{\Sigma}(s) \times G_{C'_{\mathrm{flt}}}(s) = \frac{1 + s\,T_n}{s\,T_i} \times \frac{K_{\Sigma}}{1 + s\,T_{\Sigma}} \times \frac{1}{s\,C'_{\mathrm{flt}}} \tag{6.12}$$

$$H_{\mathrm{CL,v}}(s) = \frac{H_{\mathrm{OL,v}}(s)}{1 + H_{\mathrm{OL,v}}(s)} = \frac{1 + s\,T_n}{1 + s\,T_n + s^2\,\frac{T_i \times C'_{\mathrm{flt}}}{K_{\Sigma}} + s^3\,\frac{T_i \times C'_{\mathrm{flt}} \times T_{\Sigma}}{K_{\Sigma}}} \tag{6.13}$$

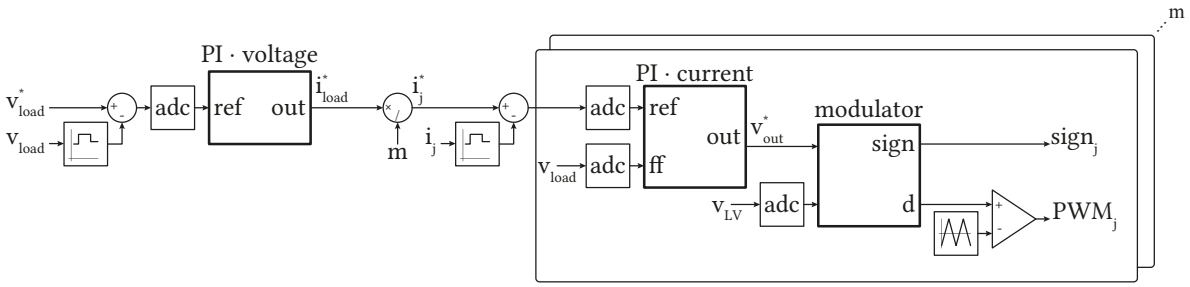


Fig. 6.2 Schematics of the complete *sub-converter* control model as implemented in the simulation.

Symmetrical Optimum Criterion is applied to the outer closed-loop transfer function. The controller gains are expressed in (6.14), according to their traditional definition.

$$T_n = 4 \times T_\Sigma \qquad \text{and} \qquad T_i = 8 \times K_\Sigma \times \frac{{T_\Sigma}^2}{C'_{\text{flt}}} \tag{6.14}$$

where the total delay T_Σ is partially due to slower sampling time of the outer loop ($T_{\Sigma 2}/2 = 5 \times T_{\text{sw}}$) and partially due to presence of the inner loop ($2 \times T_{\Sigma 1}$).

This control loop considers the input current to be the sum of all the *branches* currents: $\sum_{j=1}^{8} i_j$, the link with the individual currents is expressed in (6.15). The current in all the *branches* is measured and summed up to obtain the current that controls the equivalent filter capacitor voltage C'_{flt}, whose frequency is $f_{\text{sw, app}}$.

$$i_{\text{load}} = \frac{\sum_{j=1}^{8} i_j}{8} \tag{6.15}$$

6.2 Implementation in Simulation

The complete model of the discretized controller is implemented using PLECS as depicted in **Fig. 6.2**. The PI regulators are discretized and integrated with sampled measurements. The implementation of each part is described in the following **Sec. 6.2.1** to **Sec. 6.2.2**.

6.2.1 Modulator

The modulator implements the formula given in (6.16). Its inputs are the reference load voltage v^*_{load} and the measured v_{LV}, and returns two parameters: the sign of the reference current for the polarity leg and the duty-cycle to apply on the switching leg. The details of modulator implementation are given in **Fig. 6.3**. The duty-cycle is saturated to an upper and lower limit, which help in the zero-crossing of the voltage reference, actually corresponding to a change of operation mode by changing the state of the polarity leg.

Additionally, the modulator creates the adequate command signals for all the switches depending on the number of *branches* : the gate signal for the switching leg are created by comparing the duty-cycle to phase-shifted triangular carriers at the switching frequency; the gate of the polarity leg is given by the sign of the reference.

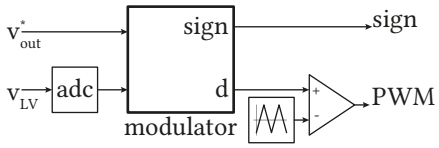


Fig. 6.3 Modulator implementation.

$$d_{T_1} = \begin{cases} \dfrac{v_{\text{load}}}{v_{\text{LV}}} & \text{if} \quad v_{\text{load}} \geq 0 \\ 1 - \dfrac{|v_{\text{load}}|}{v_{\text{LV}}} & \text{if} \quad v_{\text{load}} \leq 0 \end{cases} \tag{6.16}$$

6.2.2 Inner Control Loop - PI Current Controller

The inner loop consists in the control of the inductor current, and is implemented using a discrete PI controller with feed-forward from the load voltage and anti-windup, as depicted in **Fig. 6.4(a)**. The feed-forward comes from the measured load voltage and the reference is the *branch* current. To obtain the reference for a single *branch* , the load current is divided by the number of *branches m*, as shown in **Fig. 6.4(b)**.

The gain of the controller are obtain using the expressions given in (6.17).

$$k_i = \frac{1}{T_i} \qquad \text{and} \qquad k_p = T_n \times k_i \tag{6.17}$$

The control is tuned according to the magnitude optimum. The response to a step change is given in **Fig. 6.5**. The load is considered as an ideal voltage source.

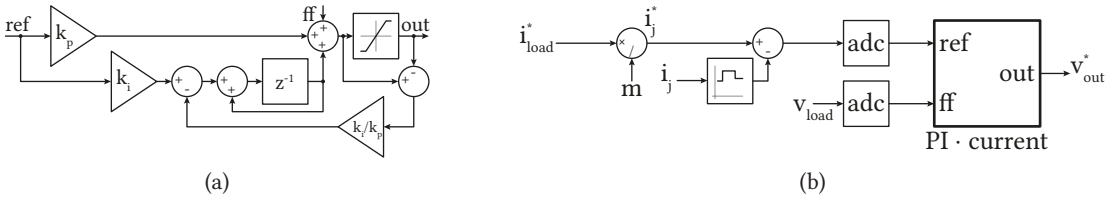


Fig. 6.4 PI current controller for the inner control loop with feed-forward (a) detailed implementation and (b) PI block with the references and feed-forward implementation.

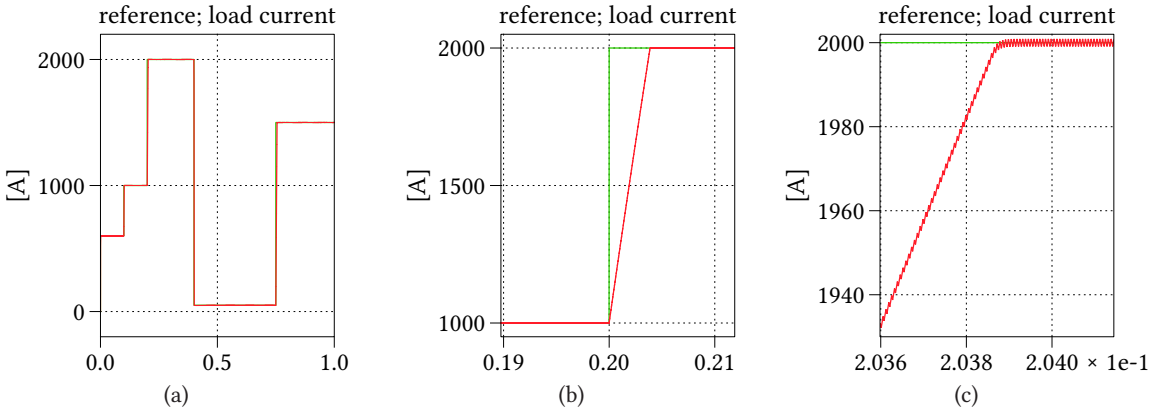


Fig. 6.5 Inner loop controller step response for $v_{\text{LV}} = 30\,\text{V}$ and $v_{\text{load}} = 9\,\text{V}$ (a) several steps, (b) zoom on one step and (c) details on one step with the ripple. The horizontal axis is time in [s] on all plots.

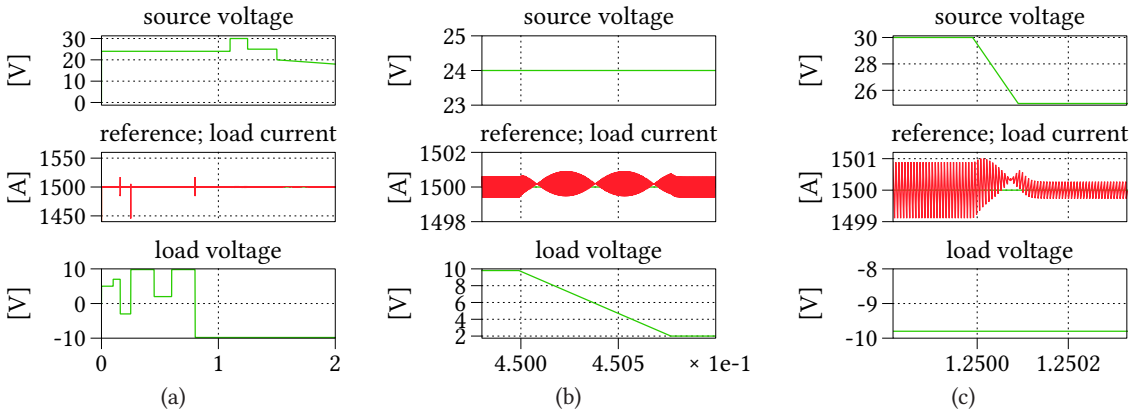


Fig. 6.6 Inner loop controller response to disturbances (a) on many changes, (b) zoom on one output voltage change where their is no mode change and (c) input voltage change. The horizontal axis is time in [s] on all plots.

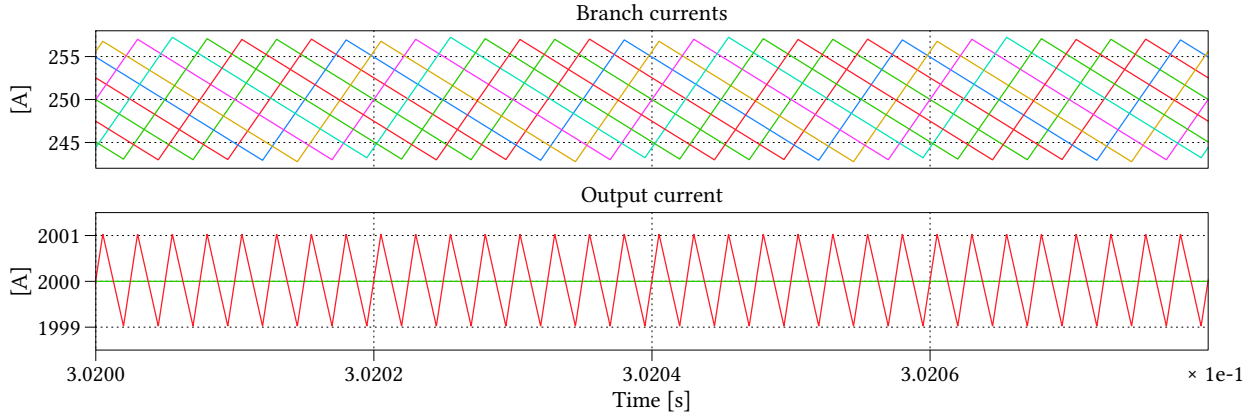


Fig. 6.7 Interleaved *branch* currents and the resulting output current of the *sub-converter*.

The output current ripple is considered at its worst when the input voltage is maximum ($v_{\mathrm{LV}} = 30\,\mathrm{V}$), the peak-to-peak ripple is at $\Delta i_{\text{pk-pk}} = 1.98\,\mathrm{A} < 2\,\mathrm{A}$: lower than the 0.1 % of 2000 A given by the specification.

To check the influence of the input voltage or change of load voltage another set of curve is derived in **Fig. 6.6**. Those disturbance are rate limited step changes in order to avoid too sharp edges.

The sharing of the current between the *m branches* is given in **Fig. 6.7**. This case is considered ideal where all the filter inductor are identical, so there is only one reference shifted by θ_8 angle for all the *branches* with no correction.

6.2.3 Outer Control Loop - PI Voltage Controller

As the response of the inner current loop is satisfying, the outer voltage controller is added in order to get the full picture of the control of the *sub-converter*. Its implementation is also a discrete PI, but this time without feed-forward as depicted in **Fig. 6.8**. The k_p and k_i gains are derived using the same equation as before (6.17). The load is modeled by an ideal current source.

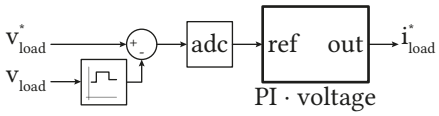


Fig. 6.8 PI voltage controller for the outer control loop.

The tuning of this controller is done according to the symmetric optimum criterion and the response to step changes is given in **Fig. 6.9**. The rate changes are limited to help with the zero-crossing when the sign of the load voltage changes.

Again, the response to the controller to disturbances is given in **Fig. 6.10** where the input voltage and output current vary. Those simulations results allow to get a good overview of the system behavior when the regulation is active and implemented according to the description.

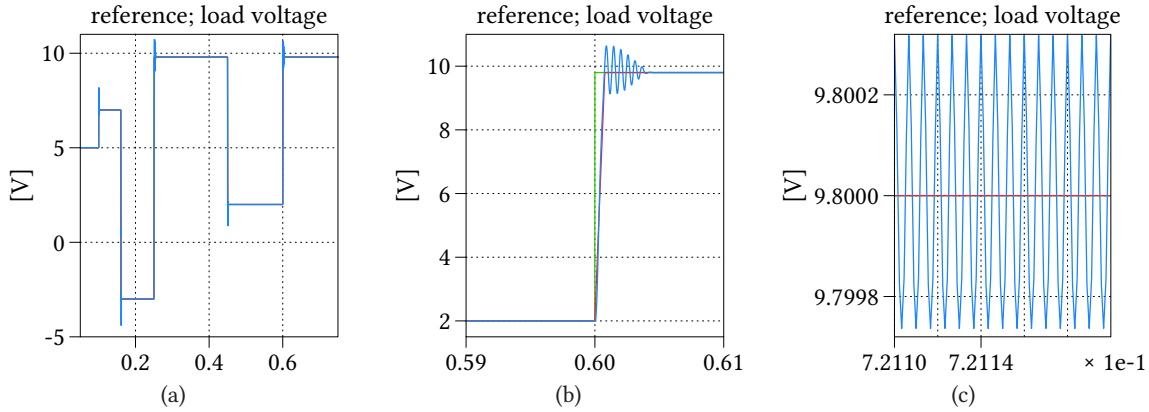


Fig. 6.9 Outer loop controller step response for $v_{\mathrm{LV}} = 30\,\mathrm{V}$ and $i_{\mathrm{load}} = 1500\,\mathrm{A}$ (a) several steps, (b) zoom on one step and (c) details on the ripple. The horizontal axis is time in [s] on all plots.

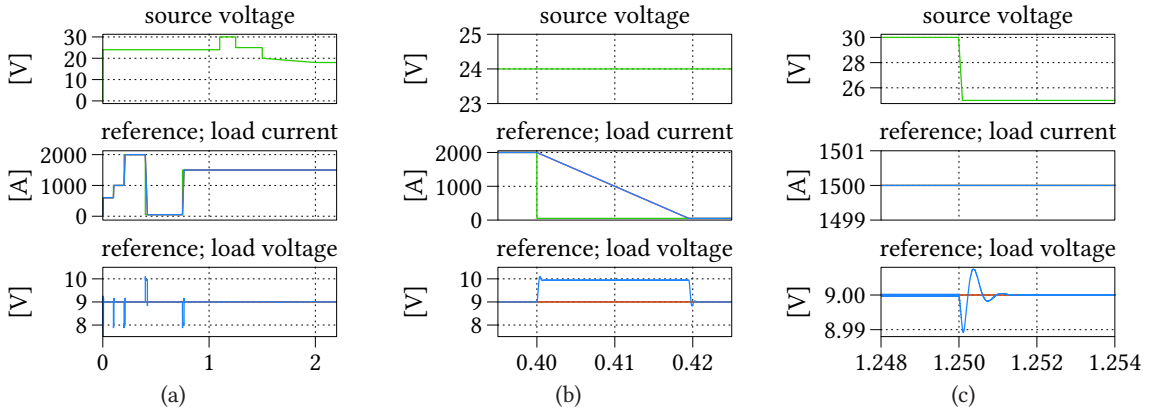


Fig. 6.10 Outer loop controller response to disturbances (a) on many changes, (b) zoom on one output voltage change and (c) input voltage change. The horizontal axis is time in [s] on all plots.

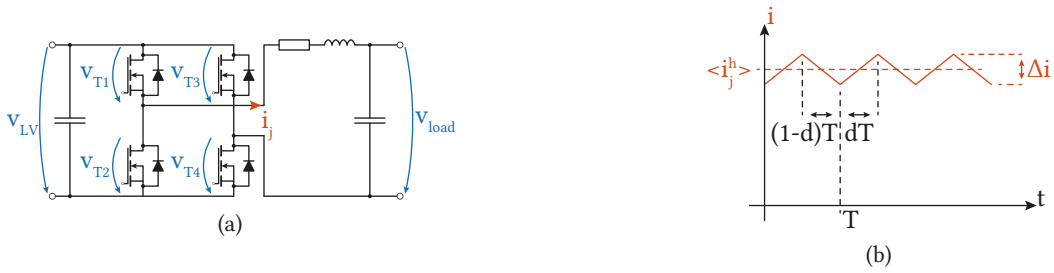


Fig. 6.11 (a) Details about the naming of the various quantities and (b) current waveform in inductance L_{flt}.

6.3 Sensitivity Analysis of the Parasitics on the Duty-Cycle

As the voltage drop is considered in the simulations, this part presents the way that the duty-cycle is influenced by the parasitics of the semiconductors.

In reality, ratings of the converters make every parasitic element a disturbance to the ideal case that has to be taken into account: high current makes every resistance a source of voltage drop, that cannot be neglected because of the low voltage rating. A model is defined taking into account output filter, voltage drop on the components and main parasitic elements such as the filter series resistance. The circuit with adequate naming convention is depicted in **Fig. 6.11(a)**. An analysis of the influence of those parasitics is conducted hereafter.

As can be noticed from the operational principle, the system strongly depends on the sign of the load voltage v_{load} with positive and negative output mode: the voltage that defines the boundary between modes is different from zero, as it is a combination of the various voltage drops.

Regardless of the load voltage sign, the current in L_{flt} presents a ripple that depends on the switching states, as can be seen in **Fig. 6.11(b)**. In this figure, $< i_j >$ is the current of L_{flt} averaged in a commutation period, which is equal to $<i_{\text{load}}>/m$. In the following, expressions for assessing the main parameters of operation are obtained; in the analysis, it is considered that the capacitor voltage is constant during a commutation period.

6.3.1 Positive Output Mode

For the positive output voltage mode, the configurations presented in **Fig. 6.12** are obtained. Under this condition, the voltage in L_{flt} is given in (6.19).

$$v^{+}_{L_{\text{flt}}} = v_{\text{LV}} - v_{T_1} - v_{T_4} - v_{\text{load}} = L_{\text{flt}} \times \Delta i^{+}/t_{\text{on}} = L_{\text{flt}} \times \Delta i^{+}/D{\times}T \tag{6.18}$$

$$v^{-}_{L_{\text{flt}}} = v_{T_2} - v_{T_4} - v_{\text{load}} \quad = L_{\text{flt}} \times \Delta i^{-}/t_{\text{off}} = L_{\text{flt}} \times \Delta i^{-}/(1-d){\times}T \tag{6.19}$$

where $v^{+}_{L_{\text{flt}}}$ and $v^{-}_{L_{\text{flt}}}$ are the voltage in L_{flt} when T_1 is ON and T_1 is OFF, respectively. Additionally, $v_T\#$ are the voltage drop on the MOSFET: $v_T = i_j \times R_{\text{DSon}}$.

In steady-state, $\Delta i^{+} = \Delta i^{-} = \Delta i$ and the average voltage on L_{flt} must be zero, leading to (6.22).

$$\int_0^{d\,T} v^{+}_{L_{\text{flt}}}\, dt = -\int_{d\,T}^{T} v^{-}_{L_{\text{flt}}}\, dt \tag{6.20}$$

$$\Rightarrow\ v^{+}_{L_{\text{flt}}} \times d\,T = -v^{-}_{L_{\text{flt}}} \times (1-d) \times T \tag{6.21}$$

Tab. 6.1 Summary of the switching states.

Output voltage	T_1	T_2	T_3	T_4	Current path
Positive voltage	switching	$\overline{T_1}$	OFF	ON	**Figs. 6.12(a)** and **6.12(b)**
Negative voltage	switching	$\overline{T_1}$	ON	OFF	**Figs. 6.13(a)** and **6.13(b)**

Fig. 6.12 Operation with positive load voltage with T_4 ON with (a) T_1 ON, T_2 OFF and (b) T_1 OFF, T_2 ON.

$$\Rightarrow (v_{\mathrm{LV}} - v_{T_1} - v_{T_4} - v_{\mathrm{load}}) \times d = -(v_{T_2} - v_{T_4} - v_{\mathrm{load}}) \times (1 - d) \tag{6.22}$$

Operating with (6.22), the relationship (6.23) between the load voltage and the DC bus voltage as a function of the duty-cycle can be obtained. It shows that if the voltage drop in the semiconductors are similar to v_{LV}, the load voltage is lower than in the ideal case, which must be compensated by an increase of duty-cycle.

$$\frac{v_{\mathrm{load}}}{v_{\mathrm{LV}}} = d - \frac{v_{T_1} \times d - v_{T_2} \times (1 - d) + v_{T_4}}{v_{\mathrm{LV}}} \tag{6.23}$$

An expression for the inductance L_{flt} as a function of switching frequency, current ripple and duty-cycle can be obtained using (6.19) and (6.23), and is given in (6.24).

$$L_{\mathrm{flt}} = \left[1 + \frac{v_{T_2} - v_{T_1}}{v_{\mathrm{LV}}}\right] \times \frac{v_{\mathrm{LV}} \times (1 - d) \times d}{f_{\mathrm{sw}} \times \Delta i} \tag{6.24}$$

6.3.2 Negative Output Mode

For the negative output mode of operation, the circuit configurations corresponds to those of **Fig. 6.13**.

Fig. 6.13 Operation with negative load voltage with T_3 ON with (a) T_1 ON, T_2 OFF and (b) T_1 OFF, T_2 ON.

Inspired from (6.23) for the positive mode of operation, the expression in (6.25) is obtained.

$$\frac{v_{\text{load}}}{v_{\text{LV}}} = -\left[1 - d + \frac{-v_{T_2} - v_{T_3} \times (1-d) + v_{T_4} \times d}{v_{\text{LV}}}\right] \tag{6.25}$$

Like in the case of the positive mode of operation, an expression of the inductance L_{flt} as a function of required current ripple and switching frequency is obtained in (6.26).

$$L_{\text{flt}} = \left[1 - \frac{v_{T_3} + v_{T_4}}{v_{\text{LV}}}\right] \times \frac{v_{\text{LV}} \times (1-d) \times d}{f_{\text{sw}} \times \Delta i} \tag{6.26}$$

Finally, the duty-cycle for each operation mode (positive and negative) is given by (6.27).

$$d = \begin{cases} \left[\frac{v_{\text{load}} - v_{T_2} + v_{T_4}}{v_{\text{LV}}}\right] \times \frac{1}{1 - (v_{T_2} + v_{T_1})/v_{\text{LV}}} & \text{if} \quad v_{\text{load}} \geq \frac{v_{T_2} - v_{T_4}}{v_{\text{LV}}} \\ \left[1 + \frac{v_{\text{load}} - v_{T_2} - v_{T_3}}{v_{\text{LV}}}\right] \times \frac{1}{1 - (v_{T_3} - v_{T_4})/v_{\text{LV}}} & \text{if} \quad v_{\text{load}} \leq \frac{v_{T_2} - v_{T_4}}{v_{\text{LV}}} \end{cases} \tag{6.27}$$

To be even more complete, taking into account the parasitic elements is necessary, the most obvious one is the resistive part of the filter inductance: R_{flt}, (6.28) is then obtained.

$$d = \begin{cases} \frac{v_{\text{load}} - v_{T_2} + v_{T_4} + i_j \times R_{\text{flt}}}{v_{\text{LV}}} \times \frac{1}{1 - (v_{T_2} + v_{T_1})/v_{\text{LV}}} & \text{if} \quad v_{\text{load}} > \frac{v_{T_2} - v_{T_4} - i_j \times R_{\text{flt}}}{v_{\text{LV}}} \\ \left[1 + \frac{v_{\text{load}} - v_{T_2} - v_{T_3} + i_j \times R_{\text{flt}}}{v_{\text{LV}}}\right] \times \frac{1}{1 + (v_{T_3} - v_{T_4})/v_{\text{LV}}} & \text{if} \quad v_{\text{load}} \leq \frac{v_{T_2} - v_{T_4} - i_j \times R_{\text{flt}}}{v_{\text{LV}}} \end{cases} \tag{6.28}$$

Regarding the case with non-zero voltage drop in the semiconductors, the analysis of (6.28) reveals that the maximum and minimum achievable values for v_{load} are shifted with respect to the ideal case: the maximum positive voltage that can be obtained (with $d_{T_1} = 1$) is lower than v_{LV}, since the voltage drops are opposite to the source (v_{LV}); on the other hand, the maximum negative voltage (with $d_{T_4} = 0$) is lower than $-v_{\text{LV}}$. The following expressions (6.29) present the maximum positive and negative voltages to be obtained.

$$\frac{v_{\text{load}}}{v_{\text{LV}}} = \begin{cases} 1 - \frac{v_{T_1} + v_{T_4} + i_j \times R_{\text{flt}}}{v_{\text{LV}}} & \text{Maximum positive} \quad d_{T_{1\text{max}}} = 1 \\ \frac{v_{T_2} - v_{T_4} + i_j \times R_{\text{flt}}}{v_{\text{LV}}} & \text{Boundary} \quad d_{T_{1\text{min}}} = 0,\ d_{T_{4\text{max}}} = 1 \\ -\left(1 - \frac{v_{T_2} + v_{T_3} - i_j \times R_{\text{flt}}}{v_{\text{LV}}}\right) & \text{Maximum negative} \quad d_{T_{4\text{min}}} = 0 \end{cases} \tag{6.29}$$

This analysis can be translated into functions for the MOSFETs duty-cycles as depicted in **Fig. 6.14**, to be recalled: $d_{T_2} = 1 - d_{T_1}$ and $d_{T_3} = 1 - d_{T_4}$. The difference between the ideal case and the real case is given by the change in maximum positive and negative voltages, boundary voltages and also in the slope of the function that relates duty-cycle to v_{LV}, as can be seen in (6.28). If the on-state voltage of

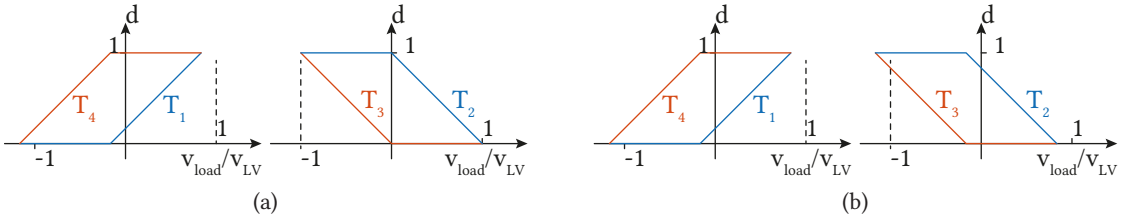


Fig. 6.14 Duty-cycles (a) in the ideal case and (b) when considering the voltage drop.

all semiconductors are the same and equal to a value v_{on}, the slope does not change and the curve is only shifted by a value given as $(2\times v_{on}+i_j\times R_{flt})/v_{LV}$.

The main message is that, depending on the components and parasitic elements, the voltage of the DC bus will have a minimum boundary that will allow safe operation of the converter - within the safe duty-cycle range. This is to be kept in mind for controllability aspects mainly.

6.4 Interleaving of Branches

Introducing interleaving between the parallel *branches* is a well-known way to improve the ripple and the apparent switching frequency at the output of the *sub-converter*.

To take the most out of the interleaving, the considered strategy is to phase shift each *branch* by a θ_m angle, defined by (6.30). Similarly, the output apparent switching frequency is increased by the same factor m, as expressed in (6.31).

$$\theta_m = \frac{2\pi}{m} \tag{6.30}$$

$$f_{\text{sw, app}} = m \times f_{\text{sw}} \tag{6.31}$$

Furthermore, for this specific kind of application, where the current ripple on the load should be controlled and very low, the interleaving is very beneficial.

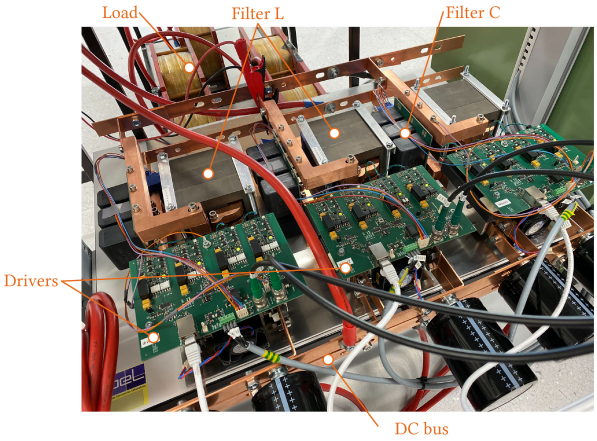


Fig. 6.15 Complete setup with three *branches* in parallel.

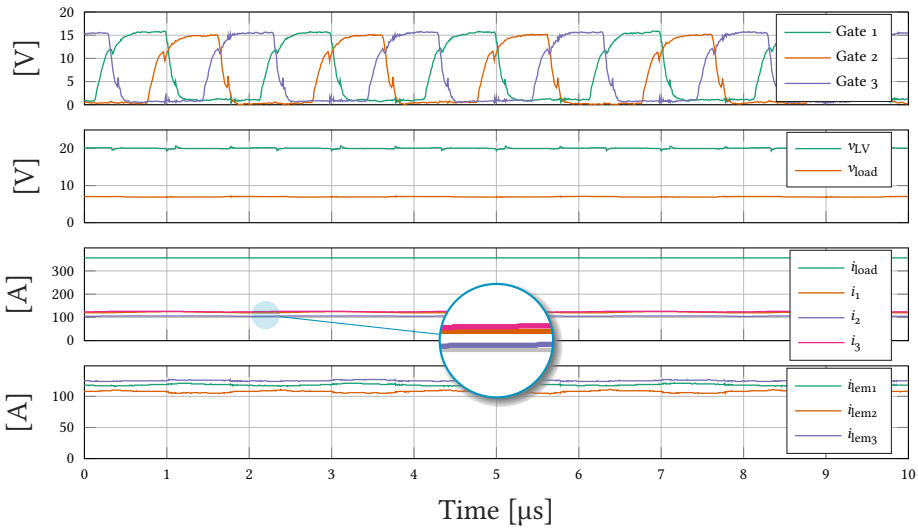


Fig. 6.16 Oscilloscope capture for the three *branches* providing the load with 5.85 V and 325 A, operated with an open-loop control, where the set-point is defined as 36 % duty-cycle. i_{load} and i_1 are measured with external current probes whereas i_{lem} is the image of the current obtain through the embedded current sensor at the output of each branch.

In order to get experimentally the waveforms and verify later on the control strategy, three *branches* previously described are implemented and assembled as depicted in **Fig. 6.15**. Their input and outputs are linked to a common power supply and load, respectively.

The structure is operated with an open-loop control at a set-point and with a load which allows an output of 5.85 V and 325 A where each *branch* contributes to a third, the waveforms of this operating point are given in **Fig. 6.16**. The interleaving also allows to reduce the voltage variations on the DC link, as can be seen on v_{LV} waveform compared to the single *branch* operation presented in the previous chapter.

As the operation is open-loop and the response of the driving stages are slightly different, there is a slight imbalance in the current provided by each branch. It can be seen in the current given by the *branch* sensors.

6.5 Closed-Loop Operation

The control strategy presented in the beginning of the chapter is implemented on the prototype. Some variations are expected in the input voltage within the range of 24 V±6 V, in the experimental setup only a fraction of this range could be explored as the source is limited to 20 V output. The dynamic of the system is explored whilst considering relevant scenario for the dedicated application, where a sudden change of load is not expected and the slope of the reference is limited.

6.5.1 Control Platform

The control scheme is established using a dedicated software which is linked with the control platform. This controller is a rapid control prototyping unit [103], that allows an easy access to the converter through analogue and digital breakout boards, as already presented in **Fig. 5.22**. The data coming

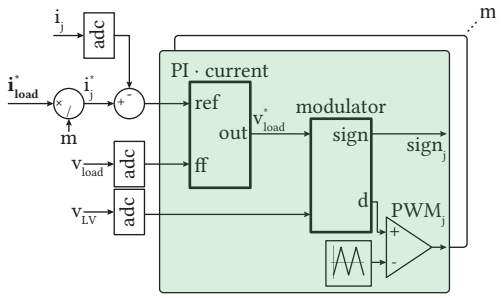


Fig. 6.17 Realized prototype regulation loop where the *branch* current regulator is highlighted in green. When considering the complete system, the load current i^*_{load} is regulated, with an equal share of current i_j from all the *branches* where $j \in [1; m]$ and m is the number of parallel operating branches. In the present case $m = 3$, if not specified otherwise.

from the driver are filtered digitally to remove noise as the controlled values are the mean ones. The cabled connections are either coaxial or twisted pairs in order to be immune to the ambient noise of the switching environment.

6.5.2 Regulation Loop

The established control structure for the *branch* current regulation is highlighted in green in **Fig. 6.17**, and is based on a traditional discrete PI controller and a dedicated modulator. The *branch* reference current is taken as input, the generated output returns two parameters: the sign of the reference current for the polarity leg and the PWM signal to apply on the switching leg.

The modulator takes care about the phase shifting and includes the transfer function of the real driver, as its output is not a 1:1 image of the input. In order to do so, it takes as input the voltage reference v^*_{load} and the DC link voltage v_{LV}.

The proportional-integral (PI) regulator is implemented with a feed-forward from the load voltage v_{load}, an anti-windup and tuned according to the magnitude optimum criterion.

To regulate the load current when several *branches* are paralleled, the individual current references are simply obtained by dividing the load current reference i^*_{load} by the number of active branches, so each contributes equally. The carriers of the PWM are shifted accordingly to provide the interleaving.

6.6 Experimental Results

The setup is operated under different scenarios, that remain consistent with the final use of the power supply: the load is a large inductance, the nominal operation cycle foresees a $16\,\text{A}\,\text{s}^{-1}$ ramp and the variations of the DC link are well defined but limited by the power supply capabilities.

6.6.1 Reference Tracking

A trapezoidal like reference is generated over a several seconds timescale in order to assess the performances of the prototype and the results are depicted in **Fig. 6.18**. The reference changes from the standby level of 75 A to a maximum of 500 A in order to remain within the limit of the external current probes used in the setup.

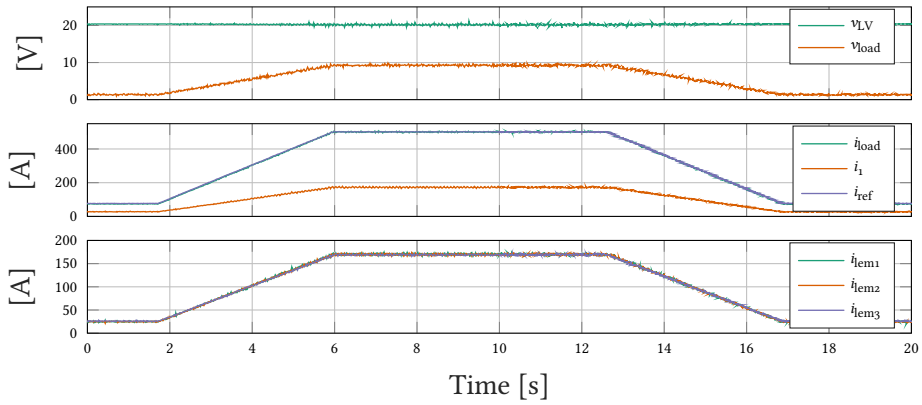


Fig. 6.18 Oscilloscope capture for the three *branches* operating with the current control regulator, where the set-point is defined as a cycle between 75 A and 500 A over a period of 15 s. i_{load} and i_1 are measured with external current probes whereas i_{lem} is the image of the current obtain through the embedded current sensor at the output of each branch.

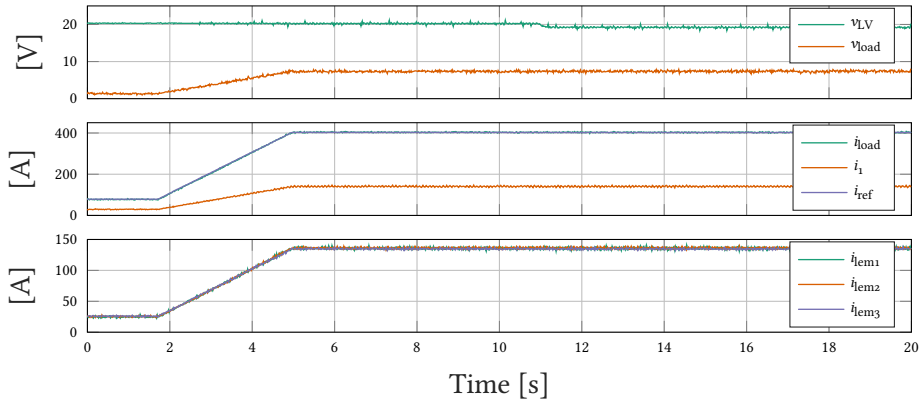


Fig. 6.19 Oscilloscope capture for the three *branches* operating with the current control regulator, where the set-point is defined as a ramp between 75 A and 400 A followed by a 1 V drop on the voltage DC link. i_{load} and i_1 are measured with external current probes whereas i_{lem} is the image of the current obtain through the embedded current sensor at the output of each branch.

The rate of the change is software limited to 100 A s^{-1}, leading to transitions around 4 s and a cycle flat-top duration of 5 s, the total acquisition time is limited in order to obtain meaningful visual data. The reference is tracked with precision and the balancing between the three stages is assured at all time as seen on the feedback from each *branch* current sensor.

Finally, the load cabled on the setup leads to an output voltage above 9 V. This corresponds to the operating point with the highest output power that can be reached with the present setup, as the source is at its maximum voltage, the current is the maximum that can be measured by the additional current probes and the output voltage of the *branch* is close to its maximal of 10 V. For this high-current tests, the power meter is removed from the circuit as the reached values are above the rating of its shunt resistors.

6.6.2 DC Link Disturbance

As mentioned before, the value of the DC link voltage can vary within a given range, the regulators should be able to cope with a such and change and maintain the balance between the three stages.

Even though in the final application no sudden change will happen, the test is done with a DC link voltage suddenly dropping by 1 V and is presented in **Fig. 6.19**. The drop is depending on the source output bandwidth, where the change is done in 150 ms. Neither the current output nor the current balancing among the *branches* are affected by this variation.

6.7 Conclusions

A set of simulations and analytical study are carried out to determine the response of the system and get a better understanding of the control strategy to be deployed on the system.

To augment the output current capabilities of the prototype, a set of three *branches* is paralleled and tested to verify its operation in a condition foreseen for the complete system. An extra layer of control is added with a load current controller deployed on the prototype and evaluated through relevant tests: steady-state and dynamic operation with disturbance from the input side. The results indicate that the proposed concept could be used to effectively realize a new generation of power supplies for superconducting magnets at CERN.

7
Conclusions and Future Works

This chapter concludes the work and highlights the learnings taken from the thesis, laying down the path for future development in what could be even larger particle accelerators.

7.1 Summary and Contributions

Powering a superconducting magnet is not only an electrical challenge, and within the CERN environment many other constraints should be taken into account such as the limited space for the integration or the management of the losses to be extracted from the system. The new family of 2-quadrant power converters is relying on the heritage of the existing 1- and 4-quadrant that are proven designs which already powered numerous cycles of the present LHC. In the HL-LHC project, the powering strategy is radically different because the equivalent resistance of the load, as seen from the output of the power supply, is reduced to its minimum. This means that the supply is located physically close to the superconducting interface, bringing the length of copper cable to its minimum. The main influence of this change is in the output voltage that the supply should deliver, with the ratings defined as ±10 V and 18 kA. The constraints specific to the thesis were presented in **Chap. 1** together with the CERN infrastructure and typical operating conditions.

The global overview of the high-current low-voltage power supplies given in **Chap. 2** allows to get a better understanding of the applications in which they are used, highlighting their very industrial focus. Narrowing down the study to the specific CERN applications and operating modes, a review of the existing topology demonstrates how the high currents are being practically reached, always using a parallel structure to reach the requirements.

In considering the new powering scheme proposed by the HL-LHC project, and fulfilling the constraints of limiting the rated power of the input stage and recovering locally the energy in the converter lead to the study of energy storage solutions of **Chap. 3**. The location of the storage in the system is critical for the sizing of the surrounding stages, and on the round trip efficiency of the energy recovery. Naturally the goal is to maximize the recovered energy, leading to the storage element integrated one conversion stage away from the load, directly on a DC bus. This choice is already framing the output DC/DC stage as the one to handle the high current and to provide the 2-quadrant operation by reversing the voltage on the load. Additionally, the storage technologies are reviewed, with a comparison between batteries and supercapacitors. The critical aspect for the storage is the charge/discharge phases of the cycle where the current should be within the limit of what it can give/accept. The volume criteria being the leading one for the decision, batteries and more precisely Li-Ion batteries are the most promising storage solution thanks to their good energy density and lifetime.

The second part of the thesis focuses on the core stage of the power supply which is the output DC/DC converter, the high current handling one. The adopted mode of operation is studied in **Chap. 4**, it allows to provide the voltage reversibility whilst lowering the losses in the structure. The topology is composed by a full-bridge semiconductor structure followed by a single stage *LC* filter. The question of the modularity and the component level details of the structure is determined in the following **Chap. 5**, where the multi-objective optimization routine is defined. This is the method that answers the question of the optimal structure to adopt in oder to have the best compromise between efficiency and volume for a *sub-converter* rated for 2 kA. This process consists at first of creating the different topology elements model considering their electrical, thermal and mechanical properties. Then the set of degrees of freedom is swept within the defined ranges in order to create a complete universe of solutions to be compared again one another to determine the optimal one. Every possible design that respect the constraint is present in this solution space and a figure of merit is introduced in order to determine the best compromising taking into account the volume and efficiency criteria. A single design is highlighted by this selection process, it is the most optimal solution for the design problem being solved. Namely, this design is composed by switches made of six parallel PCB mounted MOSFETs, switched at 50 kHz, and arranged in a 250 A rated *branches* and eight of those *branches* are composing a sub-converter. This optimal design is practically implemented and a series of test is performed to confirm its correct behavior. In this process the design of a high-current DC inductor based on powder cores is also performed and verified experimentally.

And last but not least, in the **Chap. 6** of the thesis, the control strategy and parallel operation of the *branches* are tackled. The interleaving allows to improve the waveform properties at the output of the converter. The performances are evaluated both in simulation and on the prototype based on three parallel branches.

7.2 Overall Conclusion

From the work presented in the thesis and the experience gained by the author, it can be concluded that the feasibility of the proposed solution to power superconducting magnets is demonstrated. The integration of an energy storage element inside the power supply allows to reduce the rating of the input stage, as well as acting as an energy buffer between the cycles is at the core of the 2-quadrant operation of this new family of converters. Furthermore, the design optimization of an elementary building block of the converter allow to adopt an innovative approach in the implementation including MOSFETs paralleling and high DC biased inductor. The overall implementation and control of the system also proved to be successful.

In this work, even if the experimental results differ in terms of numbers with what is predicted, the difference is found to come from the parasitic resistances. In terms of engineering, the interfaces and bus-bars are mandatory in the implementation and the consequence in a shift of the whole solution space towards lower efficiency, but it does not change the optimal design: the selected one remains on the optimal front and the only solution when using the defined figure-of-merit.

The optimization routine is especially tailored for this kind of high-current low-voltage power supply, in accordance with CERN requirements. The use of such method is known and generalized, nevertheless it is not trivial nor needed to build an optimization tool that could generate any kind of power supply, it would be sub-optimal in one way or another. In the present case, the libraries of components are made of low-voltage MOSFETs and magnetic core suited to high-DC bias and with

rather large mechanical dimensions. More generally, the optimization needs to already be customized for the end application as in [104]–[106].

7.3 Future Work

The work in this thesis opens up new possibilities in the development of power supplies in the CERN electrical power converter group when the operational constraints are following the same pattern as the one detailed in the thesis. The integrated energy storage element can be used to reduce the rated power of the input stage of the supply and consequently all its upstream infrastructure.

The power flow strategy between the grid, the storage and the load would be an interesting topic to be studied. For example, the advantage it could bring to operated the input side at constant power from the storage or grid point of view during the ramp-up phase. Once the sizing is done, various strategies could be compared to mitigate the power flow or extend the battery lifetime.

Finally from the realized prototype and the choice made in the design process of the elementary building block, there are some concepts that could be reused by the CERN engineering team that is working on the 18 kA project and whose role is to provide HL-LHC project with a fully functional power supply respecting the standards and being controlled by the CERN dedicated control platform.

Appendices

A Appendix

A.1 Inductive Power of Chap. 3

This paragraph provides an analysis regarding the energetic cycle in magnets, especially in the energy-power relation. The power transferred to the magnet system is composed of a resistive and an inductive component, as presented in (A.1).

$$P_{\text{magnet}}(t) = P_R(t) + P_L(t) = R \times I^2(t) + L \times \frac{d\,I(t)}{dt}\, I(t) \tag{A.1}$$

The inductive power of the magnet should not be confused with the reactive power, characteristic of an inductive component fed by an AC source. The inductive power is the $P_L(t)$ term in (A.1). It corresponds to the instantaneous power of an ideal inductor and is defined in the general case of AC or DC feeding of the magnet.

When the magnet is fed with a voltage whose DC-component is not zero, there is an energy accumulated over the time that is calculated through (A.2).

$$W_L(t) = \int_0^t L \times \frac{d\,I(t)}{dt}\, I(t)\, dt \tag{A.2}$$

This peculiar equation where a function is multiplied by its derivative can be found for different energy accumulating processes, such as the one involving the instantaneous powers expressed in (A.3).

$$\text{Capacitor:} \qquad P_C(t) = C \times \frac{d\,U(t)}{dt}\, U(t); \tag{A.3}$$

$$\text{Moving mass:} \qquad P_M(t) = M \times \frac{d\,v(t)}{dt}\, v(t); \tag{A.4}$$

$$\text{Rotating mass:} \qquad P_{\text{Mrot}}(t) = J \times \frac{d\,\omega(t)}{dt}\, \omega(t); \tag{A.5}$$

$$\tag{A.6}$$

For all those systems, the calculation of the accumulated energy over time is calculated through a similar expression as the inductance, namely (A.7), where $f'(t)$ is the time derivative of the function $f(t)$.

$$W(t) = K \times \int_0^t f(t)\, f'(t)\, dt \tag{A.7}$$

The integration is done using the calculus product rule the base of the relation describing the derivation of a product of two functions. As a consequence the energy accumulated in the systems listed above can be calculated as in (A.8).

$$\text{Inductor:} \qquad W_C(t) = L \times \frac{I^2(t)}{2}; \tag{A.8}$$

$$\text{Capacitor:} \qquad W_C(t) = C \times \frac{U^2(t)}{2}; \tag{A.9}$$

$$\text{Moving mass:} \qquad W_M(t) = M \times \frac{v^2(t)}{2}; \tag{A.10}$$

$$\text{Rotating mass:} \qquad W_{\text{Mrot}}(t) = J \times \frac{\omega^2(t)}{2}; \tag{A.11}$$

(A.12)

The initial conditions to respect are:

$$U(t_0) = 0; \qquad I(t_0) = 0; \qquad V(t_0) = 0; \qquad \omega(t_0) = 0; \tag{A.13}$$

The take home message is that the accumulated energy is independent from the profile or form of the function $f(t)$ that allows to reach its final value. The accumulated energy only depends on:

- a constant (C, L, M, J), characteristics of the system
- the square value of the variable reached at the considered time

A.2 Branch Optimization of Chap. 5

A.2.1 Devices List

The component map presented in **Fig. 5.1(b)** refers to the component of **Tab. A.1**.

Tab. A.1 Specifications of the sub-converter.

Identifier	Model	Manufacturer	V_{DS} V	I_D A	$R_{DS_{on}}$ Ω	$T_{j,max}$ °C
1	VMO1200-01F	IXYS	100	1220	0.001	150
2	IPT012N08N5	Infineon	80	300	0.001	175
3	IPT015N10N5	Infineon	100	300	0.0018	175
4	SKM111AR	Semikron	100	200	0.007	150
5	IRFP4468PbF	Infineon	100	195	0.002	175
6	IPB180N08S4-02	Infineon	80	180	0.0018	175
7	IRFB4310PbF	ST	100	130	0.0056	175
8	IPP052N08N5	Infineon	80	80	0.0046	175
9	IRF6668PbF	International Rectifier	80	55	0.012	150
10	MMIX1F520N075T2	IXYS	75	500	0.0012	175
11	IPT007N06N	Infineon	60	300	0.00066	175
12	STL220N6F7	ST	60	240	0.0012	175
13	AUIRF3805S	Infineon	55	160	0.0026	175
14	AUIRFP2907Z	International Rectifier	75	170	0.0035	175
15	IRFP7537PbF	International Rectifier	60	172	0.00275	175
16	STB160N75F3	ST	75	120	0.0035	175
17	SQJA62EP	Vishay	60	60	0.0037	175

A.2.2 Devices Package

The packages and mechanical mounting on a heat-sink of the MOSFET ① to ⑤ is depicted in **Fig. A.1**.

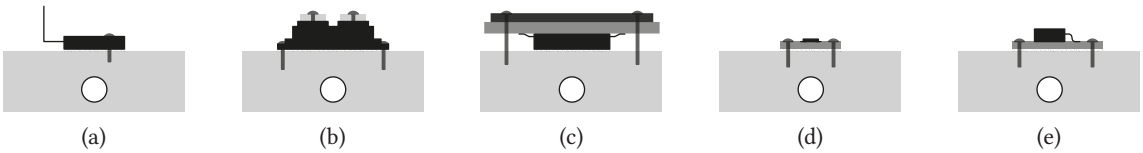


Fig. A.1 Mounting of the various packages on a cooling aggregate: (a) TO-247, (b) miniBLOC, (c) IXYSspecial, (d) PowerFLAT and (e) D2PAK.

A.2.3 Early Prototype - 200 A Half-Bridge Module

In this part of the appendix, the structure, design, implementation and realization of the early 200 A half-bridge module is detailed. The starting elements of the design process are the modularity numbers, $m = 10$ leading to the 200 A rating for the module, and $k = 10$ giving each device 20 A to process; the selected device is *FDMS86550* from *ON Semiconductor*.

A.2.3.1 Concept

The technical considerations tackled during the design process of the module should follow the requirements listed hereafter. The concept of the module is depicted in **Fig. A.2**.

Cooling: as the semiconductors are the main source of heat, the goal is to keep the junction temperature below 120 °C for a safe and durable operation. To this extend a CERN standard water cooled plate is used as the main heat exchanger; tests have shown its ability to dissipate up to 3 kW of power in normal condition of use.

Mechanical interface: the module is located on the cooling plate which is as well its mechanical base. To avoid any additional machining for the first prototype, a copper interface plate is used to fit the existing threaded holes to the module mechanical structure.

Electrical interface: the current processed in the module is 200 A, it requires the appropriate power connections and cables cross section. To be generic, the interface is a connection where a screw can be used to fasten cables terminations to the module, namely the bus-bar stack. Lighter interface is used for auxiliaries power supply as the consumption of the boards is known, it is integrated in the multi-pin connections between the boards.

Control signal level interface: the control signals are all electrical, as the PWM is coming from a waveform generator. The signals are transmitted between boards through cables assembly.

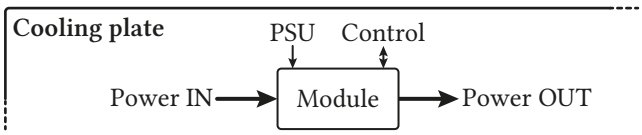


Fig. A.2 Conceptual definition of the module.

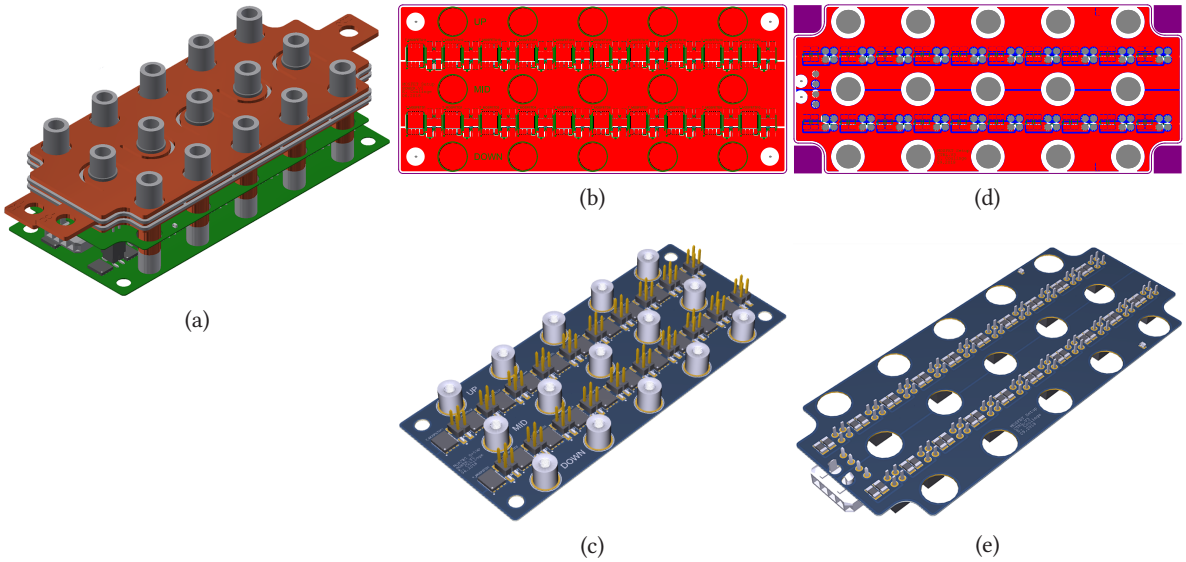
A.2.3.2 Design

The topology implemented in the module can be chosen to be a switch (composed by $k = 10$ parallel MOSFETs), a half-bridge (composed of two switches) or a full-bridge (composed of four switches). The half-bridge solution is adopted because it is a good compromise in terms of physical size, layout flexibility and control simplicity.

A.2.3.3 Power Part

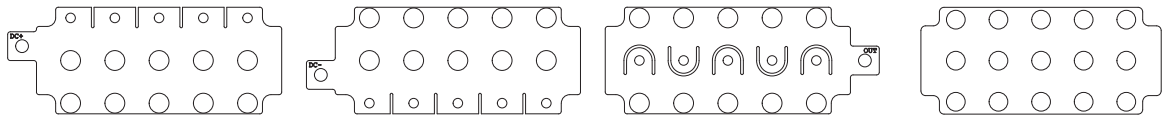
Power PCB The first designed board is the one where the power semiconductors sit and the design process can be summed-up in steps and depicted in **Figs. A.3(b)** and **A.3(c)**.

- As the Power PCB should be thermally efficient, it is chosen to go for IMS PCB which provide the best thermal performances: the FR4 core is replaced by aluminum. Nevertheless, it is quite limiting in terms of routing because it can only be single layer (in the standard pool of the selected PCB manufacturer) with no through hole components.
- The other limitation of the IMS technology is mechanical: only one 1.55 mm thickness is available, thus the board cannot withstand any mechanical stress and cannot be used as mechanical base.
- With the semiconductor device selected, and the module topology being adopted, the outline of the Power PCB is defined by the components that should sit on it: 20 devices arranged as 2×10 MOSFETs for each switch of the half-bridge plus the power and control interface.
- The physical size of this board defines the outline of all the others. For the Power PCB, dimensions are such that all the components can be tightly fitted onto it. Eventually, dimensions of the board are: 115 mm × 50 mm.
- All MOSFETs devices have to be driven through the gate pin which needs to be accessed directly. As no crossing is allowed by the single layer routing, it is chosen to have a direct connection to each gate with a Board-to-Board (B2B) connector. The smallest standard B2B connector is four positions, the other pins are used to share the Gate and Source voltage level of the MOSFET and then limit the area of the Gate-Source loop for a robust layout of the driver.
- The last item of this PCB is the power connection which allow the power to flow in and out of the board. The surface only mounting restrains the choice to simple internal blind-hole thread terminals. Rated for 50 A, five of them for DC+, DC- and OUT are required.
- Simplicity and symmetry of the layout of the Power PCB is key. MOSFETS are arranged in line and large polygons are used for Drain and Source connections.
- Adding any shunt resistor or current measuring device on the board destroys the switching performances of the module and imply quite a number of additional connections and signals for the ten parallel devices. Sensing is done indirectly using thermal probes underneath the PCB, below the center of each MOSFET.



(a) (b) (d) (c) (e)

Fig. A.3 (a) CAD rendering of the assembled power part, (b) layout of the Power PCB, (c) CAD rendering of the Power PCB, (d) layout of the Gate Routing PCB and (e) CAD rendering of the Gate Routing PCB.



(a) (b) (c) (d)

Fig. A.4 Bus-bar stack elements: (a) DC+, copper 1.5 mm thick, (b) DC-, copper 1.5 mm thick, (c) OUT, copper 1.5 mm thick and (d) isolation, Bakelite 1 mm thick.

Gate Routing PCB This boards sits on top of the Power PCB and its role is to spread the gate signal to all MOSFETs. Its input signal comes from the driver trough twisted cables and multi-pin wire-to-board connector. As this board is the final stage of the driving process but as its location is critical in the module, it is deported from the drivers boards. The schematics and layout design using Altium Designer are presented in **Figs. A.3(d)** and **A.3(e)**.

Bus-Bar Stack The power connections are extended in order to go above the Gate Routing board with a sufficient clearance. Then those connections need to be interfaced together and with the environment (cables), a classical approach for stacked planar bus-bars is used, layout is given in **Fig. A.4**.

A.2.3.4 Driver Part

The driver adopts the same stacked boards design philosophy because of the module area and volume constraints. It is depicted in **Fig. A.5**.

Driver Architecture The driver is divided into one pre-driver board which is the interface with the controller and two identical driver boards that takes PWM from the pre-driver and condition it to drive the upper and lower MOSFETs. It is chosen to create the complementary signal and dead-time locally. The other solution where the PWM and dead-time are generated by the controller and send (optically for isolation purposes) to the drivers is also considered but there are two main drawbacks:

the need for an integrity check of the signal on the driver side (which still requires some space on the board) and the use of two PWM channels from the controller. An advantage could be the very flexible dead-time: software based rather than programmed with a resistor on the driver chip - which is not useful in the purposed utilization of the module.

Pre-Driver The pre-driver is the interface with the outside, its role is to create two complementary PWM signals with the adequate dead-time when the enable signal is ON. The main parts of the board are: connectors (supply, PWM signal, enable,...), linear regulators for 5 V and 15 V, fault signal addition and driver to get the two PWMs signals for upper and lower switch of the half-bridge. The layout design using Altium Designer is presented in **Figs. A.5(b)** and **A.5(c)**.

Driver The drivers role is to amplify the PWM signal coming from the pre-driver. As there are ten MOSFETs in parallel, the gate capacitance becomes rather large, thus the need to amplify the signal, as one simple driver cannot handle that. It is why the topology of the driver features two MOSFETs that can drive larger currents using a bootstrap topology. A DC/DC power supply provides the galvanic isolation for the secondary floating stage. A small part of the circuitry is dedicated to the power supply monitoring and can return a fault in case of power failure. Signals are isolated with opto-couplers and the PWM signal is processed in order to correct the symmetry of the edges before reaching the driver. Protections against over-voltage are added in most of the circuits. The layout design using Altium Designer is presented in **Figs. A.5(d)** and **A.5(e)**.

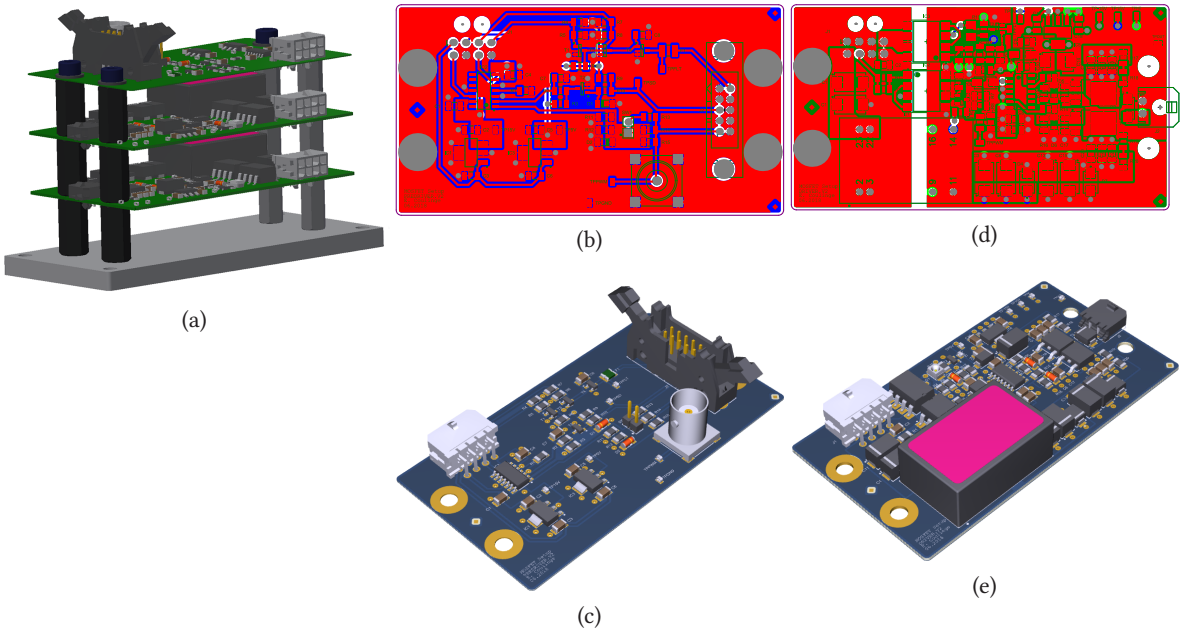


Fig. A.5 (a) CAD rendering of the assembled driver part, (b) layout of the Pre-driver PCB, (c) CAD rendering of the Pre-driver PCB, (d) layout of the Driver PCB and (e) CAD rendering of the Driver PCB.

A.2.3.5 Mechanical Assembly

The driver part is placed on top of the power part. The mechanical assembly takes into account the fact that heating mainly occurs on the power parts, thus vertical deformation should be possible on the different layers of the stack. To achieve that and to avoid over-constraining the whole assembly, it is decided to provide contact using pressure: the whole power module being compressed between plates with the adequate torque as in a press-pack assembly is depicted in **Fig. 5.12**.

- Elastic washers are added for the vertical tolerances at the bus-bar level.
- Galvanic insulation between the layers of the bus-bar stack is provided by the nylon columns that are the counter part of the power columns connection in the sandwiched assembly.
- To avoid extra machining on the used cooling plate, a thick copper plate is used to interface the module with the existing threaded holes of the plate. This interface plate is grooved to allow insertion of thermal probes right below each MOSFET. Additionally it can be used as the mechanical support for the whole module, being the lower part of the press-pack.
- The upper part of the press-pack is made out of a thick aluminum plate where the drivers sit.

Sensing The current sharing between the parallel MOSFETs is is only done in an indirect way using thermal probes that are located right below the center of each MOSFET, directly below the Power PCB, as indicated by the blue probes in **Fig. A.6(b)** (T_{MOSFET}). Sensing directly the current is worsening the dynamic performances of the converter.

A.2.3.6 Tests

Test Setup The module is tested in the lab as part of a complete test setup depicted in **Fig. A.6**. The temperatures monitoring using a eight channel data-logger and type *K* thermocouples. The cooling plate is connected to a cooling unit in a closed loop circuit. This unit is a thermostat that regulates temperature and circulate demineralized water at a $1.8\,\mathrm{L\,s^{-1}}$ flow rate. A standard laboratory Power Supply Unit (PSU) and waveform generator are used for auxiliaries and PWM generation respectively. The ratings of the power source are 0; 20 V, 0; 2250 A, model *TSD20* from *Magna-Power* with an air-core inductance rated 1000 A, 33 µH as a load.

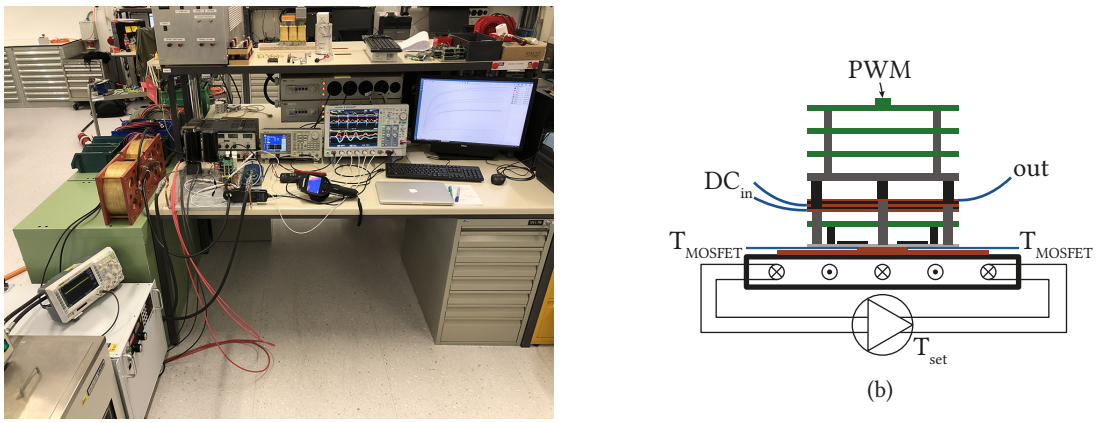


Fig. A.6 Test setup: (a) pictures and (b) integration scheme.

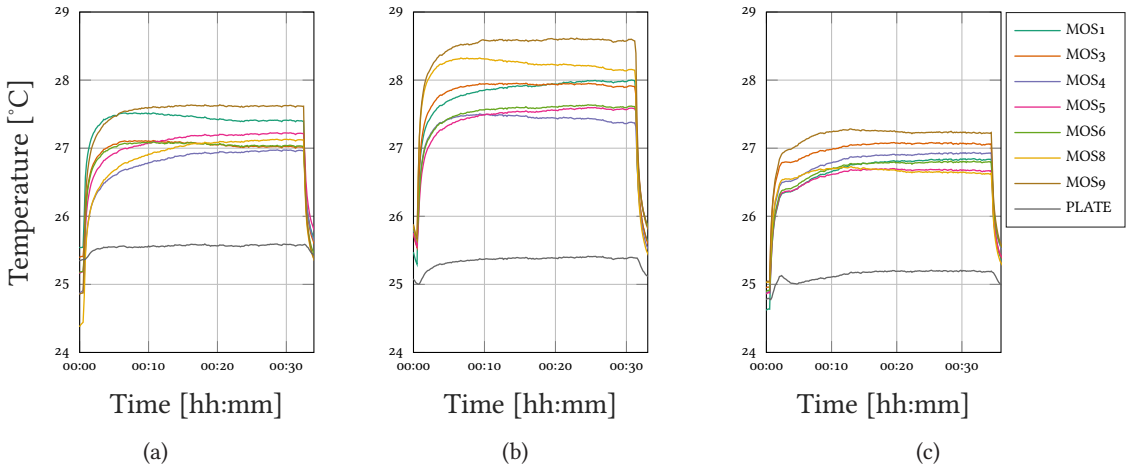


Fig. A.7 Static test results at 200 A and 25 °C water cooling: (a) upper switch MOSFET of the module, (b) lower switch MOSFET of the module and (c) lower switch MOSFET of a second module.

Static Tests They allow to verify the good balancing of the current among the MOSFETs. The results are provided in **Fig. A.7**, where a 3.5 % relative error is measured in permanent regime: 27.2 °C average measured temperature against 26.3 °C theoretical computed temperatures. The spread is contain within 1.2 °C

Switching Tests They allow to asses that the balancing of the current among the MOSFETs is good in the half-bridge module. Results are plotted in **Fig. A.8**. The tests show a spread of 2; 3 °C in the MOSFETs temperatures, which corresponds to a 6; 9 % temperature difference between the devices, which remain acceptable, below 10 %. The 200 A test is the most stressful for the test setup but still, it reaches thermal stability and the sharing remains good.

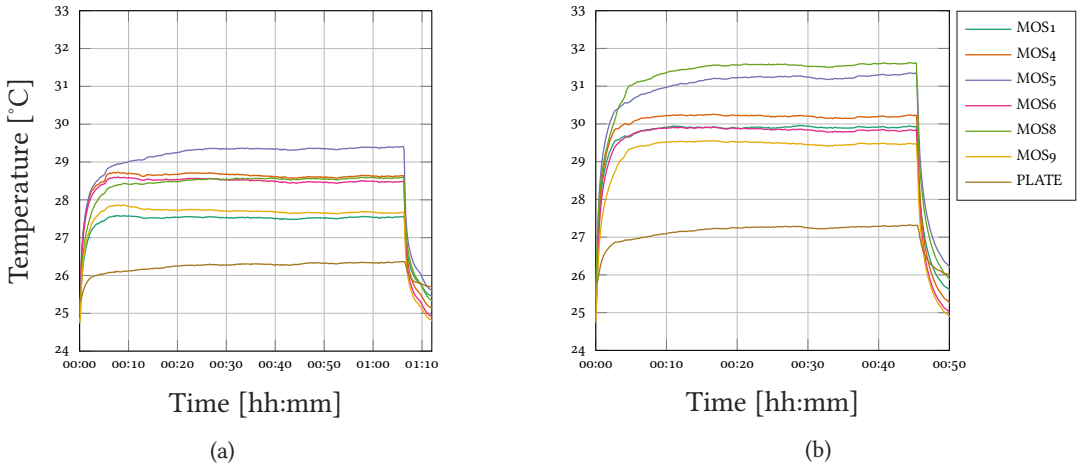


Fig. A.8 Switching test results with a 10 V source voltage and 25 °C water cooling: (a) at 100 kHz with a 24 % duty-cycle, leading to a current around 100 A and (b) at 25 kHz with a 22 % duty-cycle, leading to a current around 200 A.

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MSc thesis — *Power Electronics Building Block - Design*
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Power Electronics Laboratory, EPFL, Switzerland
Power Electronics Development
power electronics circuit development, hardware development, PCB prototyping, mechanical integration, commissioning and testing

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Electrical Power Converters Group, CERN, Switzerland
Evaluation of Thermal Cycling Effects on IGBT Lifetime: Case Study
AC/DC, DC/DC power converters electrical and thermal simulations, losses evaluation in semiconductors, lifetime estimation using Rainflow analysis and power stack data-sheets

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