EPFL

Thèse n° 7661

Modeling for Ultra Low Noise CMOS Image Sensors

Présentée le 10 septembre 2020

à la Faculté des sciences et techniques de l'ingénieur
Laboratoire de circuits intégrés
Programme doctoral en microsystèmes et microélectronique

pour l'obtention du grade de Docteur ès Sciences

par

Raffaele CAPOCCIA

Acceptée sur proposition du jury

Prof. E. Charbon, président du jury
Prof. C. Enz, directeur de thèse
Prof. A. Theuwissen, rapporteur
Prof. E. Fossum, rapporteur
Dr J.-M. Sallese, rapporteur

École
polytechnique
fédérale
de Lausanne

2020

Ma Nino non aver paura di sbagliare un calcio di rigore,
non è mica da questi particolari che si giudica un giocatore,
un giocatore lo vedi dal coraggio, dall'altruismo e dalla fantasia.
— Francesco De Gregori

To my family...

Acknowledgements

I would like to express my deep gratitude to my thesis advisor, Prof. Christian Enz. His guidance and support over the past few years helped me to expand my knowledge in the area of device modeling and sensor design. I am genuinely grateful for having taught me how important is to be methodical and to insist on the detail.

My grateful thanks are also extended to Dr. Assim Boukhayma for his contribution and for having introduced me to the fascinating world of image sensors. His help and encouragement over the entire time of my Ph.D. studies daily motivated me to improve the quality of the research.

I wish to thank Dr. Farzan Jazaeri for everything he taught me during my Ph.D. His passion for physics and device modeling has been a source of inspiration for the research.

I would also like to express my deepest gratitude to Prof. Edoardo Charbon, Prof. Jean-Michel Salles, Prof. Eric Fossum and Prof. Albert Theuwissen for being part of my jury, evaluating my thesis and providing comments and remarks about my work.

My gratitude also goes to Dr. Wei Gao for providing me with the opportunity to conduct an internship in an industrial environment and participate in projects beyond the scope of this thesis. In addition, I must also thank the whole sensor and camera team for giving me the possibility to join their team. I would like to thank Dr. Chiao Liu, Dr. Andrew Berkovich, Dr. Elliott Tsai, Dr. Ziyun Li, Dr. Syed Shakib Sarwar, Reid Pinkham, Tianyi Yang and Seth Hirsh.

I would like to thank Prof. Leblebici and Dr. Akin for their help and encouragement that inspired me during my master thesis to purse a Ph.D. degree. During my PhD, I had the opportunity to work together with two master students, Tijmen Spreij and Alban Morelle. I would like to thank them for the collaboration we had and for their work, which is partially included in this thesis. Thanks also to Dr. Althaus for helping me editing this manuscript.

Particular thanks go to all my colleagues from ICLAB, current and former, for making these past few years a memorable experience. I would like then to express my sincerest thanks to my office mates, Arnout Beckers and Chunmin Zhang, for all the support we always gave each other. I also want to thank all my lab mates: Mattia Cacciotti, Francesco Chicco, Vladimir Kopta,

Acknowledgements

Sammy Cerida, Alessandro Pezzotta, Huang Huaiqi, Raghavasimhan Thirunarayanan, Antonio D'Amico, Antonino Caizzone, Vincent Camus, Jérémy Schlachter, Minhao Yang, Daniel Bold, Marta Franceschini and Salvatore Collura for all the fun conversation we had.

I am also thankful to all the friends I met in Switzerland and the fun time we had outside of EPFL. I must acknowledge Mikhail, Navid, Gain, Jonathan, Pamela, Cosimo, Giorgio, Chiara, Michela, Eleonora, Selma e Marta. At the same time I want to acknowledge my friends outside Switzerland for their continuous support, so I thank Beppe, Giulio, Inger, Biagio, Ellis, Ruben, Andrea, Peppe and Fabio.

Finally, my deep gratitude to my family for their continuous love. I am grateful to my sister Marta for always being there for me as a friend, my brothers Francesco e Matteo for their unparalleled support, and my parents Paola and Arcangelo. I am forever indebted to them for giving me the opportunities that have made me who I am.

Neuchâtel, 2020 Raffaele Capoccia

Abstract

The low-light performance of a CMOS image sensor (CIS) is one of the most important performance metrics in a camera, whether it is used in products for consumer electronics or in an image-acquisition system for machine vision or the Internet-of-Things (IoT). At very low levels of illumination, the image sensors are limited by the noise generated by the readout circuits used to convert the information stored in the photodetector element, the pinned photodiode (PPD). Thanks to the development of efficient noise reduction techniques, modern CISs offer extremely interesting performance with sub-electron input-referred noise values. However, further noise reduction is needed to enable the single photon counting capability, which will allow new opportunities in a large variety of scientific applications.

This thesis focuses on the modeling of ultra-low noise CISs by exploring two main research topics. The first is the modeling of the PPD device together with the transfer gate (TG). The interface between these two structures limits performance in many advanced applications and requires a deep understanding of the charge transfer process. The core of the first compact model for the charge transfer in PPDs is reported here. The second evaluates the impact of different techniques on total noise reduction. In particular, the in-pixel source follower (SF) optimization, the combination of the column-level gain with the correlated multiple sampling (CMS) order and the effect of technology downscaling are analyzed and then verified by software simulations and experimental results.

The core of a physics-based compact model for the charge transfer in PPDs for CIS is presented in this dissertation. A set of analytical expressions is derived for the 2D electrostatic profile, the PPD capacitance, and the charge transfer current. The proposed model relies on the thermionic emission current mechanism, the barrier modulation and the full-depletion approximation to obtain the charge transfer current. The model is fully validated with stationary and opto-electrical technology computer-aided design (TCAD) simulations. The charge transfer model is validated experimentally by the expression of the total amount of the transferred charges derived from the charge transfer current and evaluated for different values of light intensity, TG voltage and transfer time. The result is a proven resource for CIS pixel designers in the analysis, simulation and optimization of PPD-based pixel in CISs.

The main circuit-level technique for noise reduction studied in this thesis is the CMS, which is used to reduce the thermal noise and the residual flicker noise originated in the in-pixel SF. To verify the impact of the combination of the column-level gain and the analog CMS on the readout noise, a readout chain with variable gain and variable CMS order has

been integrated in a standard 180 nm CIS process. The match between the measurement and the noise model results validates experimentally the model itself. Based on transient noise simulation results, the combination of an optimized pMOS source follower (SF), a column-level gain equal to 64 and a CMS of order 8 allows the noise to be reduced to the value of 0.20 e_{rms}, with a readout time of 43 µs.

Key words: Charge Transfer Current, CMOS Image Sensors (CIS), Compact Device Modeling, Correlated Double Sampling (CDS), Correlated Multiple Sampling (CMS), Flicker noise, Passive Switched Capacitor, Photon Shot Noise, Photon Transfer Curve (PTC), Pinned Photodiode (PPD), Readout Noise, Temporal Noise, Thermal noise, Thermionic Emission Theory.

Abstract

Le prestazioni a bassa luminosità dei sensori di immagini CMOS sono una delle metriche più importanti per la caratterizzazione di fotocamere utilizzate nell'elettronica di consumo o in sistemi per l'acquisizione di immagini processate da elaboratori o nell'internet delle cose (IdC o IoT). A livelli molto bassi di illuminazione, i sensori di immagini sono limitati dal rumore originato dai circuiti elettronici di lettura, utilizzati a loro volta per convertire l'informazione immagazzinata nel dispositivo fotosensibile, il fotodiodo pinned o pinned photodiode (PPD). Grazie allo sviluppo di efficienti tecniche di riduzione del rumore, i moderni sensori CMOS offrono performance estremamente interessanti con valori di rumore espresso in carica elettrica e riferito all'ingresso del circuito al di sotto del singolo elettrone. Tuttavia, una riduzione addizionale del rumore è necessaria per permettere il conteggio dei singoli elettroni generati durante l'illuminazione, il quale aprirebbe ad una serie di nuove opportunità in diverse applicazioni scientifiche.

Questa tesi si concentra sul modelllo dei sensori CMOS a bassa luminosità esplorando due ambiti principali di ricerca. Il primo è il modello del dispositivo PPD insieme al gate di trasferimento (o transfer gate (TG)). L'interfaccia tra queste due strutture limita le prestazioni in molte applicazioni avanzate e necessita di una comprensione profonda del processo di trasferimento di carica. Il nucleo del primo modello compatto per il trasferimento di carica nei PPD è presentato in questo dissertazione. Il secondo argomento valuta l'impatto delle diverse tecniche di riduzione del rumore. In particolar modo, l'ottimizzazione dell'inseguitore di tensione (o source follower (SF)) presente in ciascun pixel, la combinazione del guadagno in tensione applicato per ogni colonna dell'array del sensore con il campionamento multiplo correlato (Correlated Multiple Sampling (CMS)) e l'effetto dello scaling tecnologico sono analizzati e verificati con simulazioni software e risultati sperimentali.

Il nucleo del modello compatto qui presentato è basato sulla fisica del dispositivo e descrive il trasferimento di carica nei PPD usati nei CIS. Un insieme di espressioni analitiche è derivato partendo dal profilo elettrostatico in due dimensioni (2D), insieme alla capacità del PPD e alla corrente di trasferimento. Il modello proposto si basa sul meccanismo di corrente per emissione termoionica, la modulazione della barriera di potenziale all'interfaccia con il PPD e l'approssimazione di completo svuotamento. Il modello è interamente validato tramite simulazioni stazionarie e opto-elettriche effettuate con uno strumento software (TCAD) ed è in seguito validato sperimentalmente tramite l'espressione della quantità totale di cariche trasferite. Quest'ultima viene derivata direttamente dalla corrente di trasferimento e valutata

per diversi valori di intensità luminosa, tensione applicata al TG e tempo di trasferimento. Questo modello vuole essere una risorsa per i progettisti durante l'analisi, la simulazione e l'ottimizzazione di pixel basati sui dispositivi PPD.

La principale tecnica circuitale per la riduzione del rumore studiata in questa tesi è il CMS, utilizzato per ridurre il rumore termico e flicker originato nel SF, presente all'interno di ciascun pixel. Per verificare l'impatto della combinazione del guadagno a livello della colonna e del CMS analogico sul rumore, una catena di lettura con un guadagno variabile ed un ordine variabile per il CMS è stata implementata con un processo tecnologico 180 nm specifico per sensori di immagine. Il confronto tra le misure e i risultati del modello rappresentano una validazione sperimentale del modello stesso. Basandosi su delle simulazioni di rumore nel dominio del tempo, la combinazione di un pMOS SF ottimizzato nelle sue dimensioni e di un guadagno a livello della colonna uguale a 64 con un CMS di ordine 8 permette di ridurre il rumore ad un valore pari a 0.20 e_{rms}, con un tempo di lettura di 43 µs.

Parole chiave: Corrente di trasferimento della carica, sensori di immagine CMOS (CIS), modello compatto dispositivo, campionamento doppio correlato (CDS), campionamento multiplo correlato (CMS), rumore flicker, capacità commutate, rumore shot, fotodiodo pinned, rumore del circuito di lettura, rumore temporale, rumore spaziale, rumore termico, teoria ad emissione termoionica.

Contents

Acknowledgements **i**

Abstract (English/Italiano) **iii**

Acronyms **xi**

List of figures **xv**

List of tables **xxiii**

1 Introduction **1**

1.1 Brief History of CIS 1
1.2 CIS Market and Major Trends 4
1.3 Ultra-Low Noise CIS – an Overview 6
1.4 Thesis Motivation and Organization 8
References for Chapter 1 9

2 CMOS Image Sensors **17**

2.1 Silicon-based Photodetectors 17
2.1.1 Device Physics 17
2.1.2 Optical Absorption 18
2.1.3 Device Components 19
2.2 Pixel Architectures 23
2.2.1 PPS - 1T 24
2.2.2 APS - 3T 24
2.2.3 PPD/TG - 4T 25
2.3 Ultra-Low Noise CIS Architectures 26
2.3.1 Basic Block Diagram 26
2.3.2 Column-level Amplifier Architectures 28
2.3.3 Correlated Sampler Circuits 29
2.4 Summary 33
References for Chapter 2 33

3 Compact Modeling of Charge Transfer in PPDs for Low Light CIS **37**
3.1 Device Simulation . . . 38
3.2 Pinned Photodiode – Electrostatic Analysis . . . 38
3.3 Pinned Photodiode Capacitance . . . 43
3.4 Potential Barrier Modeling . . . 45
3.5 Charge Transfer Current . . . 50
3.6 Experimental Validation . . . 53
3.6.1 Validation Methodology . . . 53
3.6.2 Experimental Setup . . . 55
3.6.3 Measurement Results . . . 55
3.6.4 Model Comparison . . . 59
3.7 Summary . . . 60
References for Chapter 3 . . . 61

4 Noise Sources in CIS **65**
4.1 Photon Shot Noise . . . 65
4.2 Dark Current Shot Noise . . . 69
4.3 Charge Transfer Noise . . . 70
4.4 Readout Noise . . . 72
4.4.1 Thermal Noise . . . 73
4.4.2 Reset or kTC Noise . . . 74
4.4.3 Flicker Noise . . . 75
4.4.4 RTS Noise . . . 76
4.4.5 Leakage Current Shot Noise . . . 78
4.5 Fixed Pattern Noise . . . 80
4.6 Signal-to-Noise Ratio in CIS . . . 82
4.7 Summary . . . 83
References for Chapter 4 . . . 83

5 Readout Noise Analysis in Ultra-Low Noise CIS **87**
5.1 Ultra-Low Noise Readout Chains . . . 87
5.2 Noise Analysis . . . 89
5.2.1 Calculation Method . . . 89
5.2.2 Signal Transfer Functions . . . 91
5.2.3 Noise Transfer Functions . . . 94
5.2.4 Noise Analysis Results . . . 94
5.3 Summary . . . 101
References for Chapter 5 . . . 102

6 Noise Reduction Techniques in Ultra-Low Light CIS **105**
6.1 Noise Reduction Techniques . . . 106
6.2 Combination of SC CMS with Column-level Gain . . . 107
6.2.1 Readout Design . . . 109

6.2.2 Measurement Results . . . 117
6.3 Technology Downscaling Effects on Noise . . . 124
6.3.1 Impact of Technology Downscaling on Readout Noise . . . 124
6.3.2 Simulation setup . . . 126
6.3.3 Noise Simulation Results . . . 128
6.4 Combination of SC CMS with Downscaled Technology . . . 132
6.4.1 Simulation Setup . . . 132
6.4.2 Noise Simulations Results . . . 133
6.4.3 Photoelectron counting possibility . . . 135
6.5 Summary . . . 137
References for Chapter 6 . . . 138

7 Conclusion **141**
7.1 Summary of Achievements . . . 141
7.2 Main Findings . . . 142
7.3 Future Work . . . 143
References for Chapter 7 . . . 145

A Appendix **147**
A.1 Electrostatics in PPD device . . . 147
A.2 Electrostatics along path A . . . 148

List of Publications **149**

Curriculum Vitae **151**

Acronyms

ADC Analog-to-Digital Converter.

AI Artificial Intelligence.

APS Active Pixel Sensor.

AR Augmented Reality.

AZ Auto-Zero.

BCCD Buried Channel Charge-Coupled Device.

BER Bit error rate.

BSI Back-Side Illumination.

BSIM Berkeley Short channel IGFET Model.

BWI Bit-Wise Inversion.

CCD Charge-Coupled Device.

CDS Correlated Double Sampling.

CG Conversion Gain.

CIS CMOS Image Sensors.

CLA Column-Level Amplifier.

CMS Correlated Multiple Sampling.

CS Common Source.

CTI Charge Transfer Inefficiency.

CTIA Capacitive Trans-Impedance Amplifier.

DCSN Dark Current Shot Noise.

DR Dynamic Range.

DSNU Dark Signal Non Uniformity.

EFWC Equilibrium Full Well Capacity.

EMW Electromagnetic Wave Solver.

FPN Fixed Pattern Noise.

FPS Frames per Second.

FWC Full Well Capacity.

HDR High Dynamic Range.

IC Integrated Circuit.

LDD Low Doped Drain.

LTV Linear Time-Variant.

MI Moderate Inversion.

MOS Metal-Oxide-Semiconductor.

OTA Operational Transconductance Amplifier.

PCH Photon Counting Histograms.

PPD Pinned Photodiode.

PPS Passive Pixel Sensor.

PRNU Photo Response Non Uniformity.

PSD Power Spectral Density.

PSN Photon Shot Noise.

PT Photon Transfer.

PTC Photon Transfer Curve.

QE Quantum Efficiency.

QIS Quanta Image Sensor.

RMS Root Mean Square.

RS Row Select.

RST Reset Transistor.

RTS Random Telegraph Signal.

SF Source Follower.

SI Strong Inversion.

SN Sense Node.

SNR Signal-to-Noise Ratio.

SPAD Single Photon Avalanche Diode.

SRAM Static Random Access Memory.

SS Single-Slope.

STI Shallow Trench Isolation.

TCAD Technology Computer-Aided Design.

TG Transfer Gate.

ToF Time of Flight.

TRN Temporal Read Noise.

VCCS Voltage-Controlled Current-Source.

WI Weak Inversion.

List of Figures

1.1 A summary history of CIS with the crucial events reported in a timeline: from the early development stages of technology to modern designs. 2

1.2 CIS market growth in (a) from 2016 to 2019 with forecasts up to 2025. The positive trend is expected to continue in the upcoming years (source: Yole Développement). Worldwide number of shipped image sensors in (b) according to IC Insights. 4

1.3 Modern trends described in [14] that involve image sensors and camera designs: multi-camera systems in (a), high resolution arrays in (b), 3D sensing in (c) and biometric ID based on iris-scanner in (d) (source: Daiwa Capital Markets). . . . 5

1.4 Frames from advertisement in 2020 of the top smartphones of Apple and Samsung, respectively, involving good performances at low-light levels to appeal to consumers. 6

1.5 Values of input-referred read noise in articles published from 2003 to 2020 and reported in the references of this chapter. A large amount of research reached the sub-electron noise value, while the level for a photoelectron counting error lower than 0.1% (0.15 e^-_{rms}) is very close in recent publications. 7

2.1 Energy band diagram of semiconductor in (a). The absorption shown in (b) is one of the possible interactions between the light and the matters. 18

2.2 Absorption coefficient as a function of wavelength for silicon material. Below the cutoff wavelength, absorption increases gradually due to the fact that Si is an indirect gap material. 19

2.3 Cross-section of a pn-junction and its 2D equivalent representation. The electrostatic potential profile is depicted at equilibrium in (a), in reverse bias in (b) and in forward bias in (c). The I-V characteristic is shown in (d). 20

2.4 Cross-section of a MOS structure and its 2D equivalent representation. The gate electrode is on top of the silicon dioxide layer (SiO_2) and a p-type silicon structure. The potential distribution of the MOS structure is shown at various gate biases, V_G: for a flat-band condition in (a), for a negative V_G and a surface charge accumulation in (b), for a positive V_G and a shallow depletion in (c) and a surface inversion layer in (d). 21

2.5 Cross-sectional view of buried MOS structure in (a) and potential distribution under full depletion in (b). 22

2.6 Cross-sectional view of a buried photodiode or PPD in (a) and potential distribution in (c) under depletion. 23

2.7 Four pixel schematics: 1T PPS in (a), 3T in (b), 4T APS in (c) and 4T CTIA in (d). 24

2.8 Block diagram of a conventional low noise CIS composed of an array of 4T pixels. The Line Control enables the control signals for the pixel array according to the readout scheme. At column-level, the CLA, CDS and ADC blocks are generally implemented. 25

2.9 Rolling shutter readout mode in (a) with shifted reset, exposures and readout for each line. Global shutter mode in (b) with equal start and stop of the exposure for all lines. 26

2.10 Column amplifier architectures described in [18]: single-stage capacitive amplifier in (a), two-stage capacitive amplifier in (b) and dual single-stage capacitive amplifier in (c). 27

2.11 Column amplifier circuits described in [18]: single-ended MOS amplifier architectures in (a) and (b), differential MOS amplifier in (c). 28

2.12 Three different implementations for the CDS circuit described in [18]: the differential Track and Hold CDS in (a), the single-ended CDS with a voltage buffer in (b) and the single-ended CDS with transconductance amplifier in (c). 29

2.13 Analog implementation in (a) of CMS using a switched-capacitor integrator. Timing diagram in (b) of the control signals and voltages at the main internal nodes, during the reset and after the charge transfer from the PPD. 31

2.14 Digital implementation in (a) of CMS using a multiple-ramp single-slope ADC. Timing diagram in (b) of the control and main node signals during the reset and after the charge transfer from the PPD. 32

3.1 The suite of tools composing the TCAD Sentaurus Workbench are shown in the order of execution, from the process simulation to the output data visualization. 38

3.2 Pixel back-end in (a): the microlens, the color filter and the interconnections. Pixel front-end in (b): the pinned photodiode, the TG and the SN. 39

3.3 Sketches of the electrostatic potential of the PPD: (a) at equilibrium condition, showing two built-in potentials, V_{bi1} and V_{bi2}, and maximum potential, V_{max}; (b) the maximum value of the electrostatic potential increases until the empty condition is reached while transferring the charges from the PPD to the SN. The maximum variation of the electrostatic potential is the pinning voltage, V_{pin}, as defined in [5]; (c) the potential moves towards the flat-band condition due to the applied illumination. 40

3.4 Simplified cross-section of a PPD under the assumptions of full depletion and abrupt transition: $\rho(x)$ is the charge distribution, $\mathscr{E}(x)$ the electric field and $\psi(x)$ the electrostatic potential along the position x. x_n is the junction boundary between the p^+ and n layers, x_p the junction boundary between n and the substrate, x_{p1} and x_{p2} are the limits of the depletion regions on the p^+ and p regions of the two junctions, respectively. Expressions for the electric field and the electrostatic potential are given in Appendix A.1. 41

3.5 Electrostatic potential inside the PPD structure for Case 1, 2 and 3 reported in Table 3.1: the profile simulated in TCAD is compared with the expression derived in the proposed model. $x_{\max}$ is at 170 nm and $V_{\max}$ is 0.84 V at 300 K in case I, 305 nm and 0.76 V in case II, and 460 nm and 0.67 V in case III. 42

3.6 Opto-electrical transient simulations: the gate voltage applied to the TG, the intensity of the incident wave and the electrostatic potential inside the PPD. The changes in the electrostatic potential are proportional to the incident light and can be used to derive the PPD capacitance. 43

3.7 PPD capacitance as a function of the photogenerated electrons: TCAD simulations are compared with the proposed model. 44

3.8 Electrostatic Potential of the interface between the PPD and the TG when V_{TG} = 0 V. Evidence of a potential barrier between the n-well and the semiconductor beneath the TG. 45

3.9 Section of the interface between the TG and PPD with the 2D equivalent stretched version. Electrostatic potential at the interface between the PPD and the TG during the sweep of the gate voltage. The barrier voltage is changed by the TG and PPD voltage values. 46

3.10 In (a), the charge distribution, electric field, and electrostatic potential under the assumptions of full depletion and abrupt transitions. The interface region in (b) is fully depleted along the effective charge transfer path, for a V_{TG} = 2.5 V and V_{SN} = 2.5 V. 47

3.11 Electrostatic potential along the path B crossing the PPD well, the interface, the area beneath the TG and the SN, for different time instants. $t_1 - t_4$ corresponds to the rising edge of V_{TG} , while $t_5 - t_6$ refer to V_{TG} constant. 48

3.12 Value of the potential barrier during time along the charge transfer period. The behavior of the barrier is well predicted by the proposed model. 49

3.13 Current pulses in (a, b, c, d) representing the charge transfer from PPD to SN for four different V_{TG} values: TCAD simulations are compared with the proposed model. 51

3.14 Flow in (a) to evaluate the model based on the derived expressions. Proposed equivalent circuit in (b) for the PPD, TG, and SN, where the function f is given in (3.10). 52

3.15 TCAD transient simulation of the charge transfer current together with the TG pulse and the potential barrier. 53

3.16 Schematic in (a) of the implemented readout chain with a 4T pixel, the CLA and the passive CDS circuit. Timing diagram in (b) of the control signals and the main internal nodes: in order to obtain the measurement results, different values for the pulse width and the V_{TGH} are used. 56
3.17 Readout Photon Response with the Exposure A, B and C marked with red asterisks. 57
3.18 N_{tr} is plotted for different values of the transfer time versus the TG voltage for three different exposures (exposure A, B and C). This figure shows the values of V_{TGH} that allow a complete charge transfer. 57
3.19 N_{tr} is plotted for V_{TGH} equal to 1 V in (a) and 2.5 V in (b) versus the T_{tr} , together with the model results. the CTI for the two cases also is plotted with dashed lines. 58

4.1 A noiseless image in (a) and one affected by PSN with average number of photons per pixel equal to 1. 66
4.2 Histogram of the average number of photons per pixel assuming an average incident photon per pixel equal to 1, 10 and 20, respectively. A Gaussian distribution fits the Poisson distribution well at a large value of incident photons. 67
4.3 Block diagram of a CIS digital camera with an average number of photons as input and an analog output. Each block in between implements the transfer function related to the semiconductor, pixel and readout circuits. 68
4.4 Measured PTC curve from the readout chain detailed in Chapter 6. The main information that can be extracted from a PTC curve is indicated in the figure. . 69
4.5 Cross-section of the PPD together with the TG and the SN. The main sources of dark current are shown: the STI interface, the field-free area, the surface states and the interface between the semiconductor and the oxide. 70
4.6 Cross-section of the PPD together with the TG and the SN. The main sources of CTI are numbered as follows: (1) the diffusion inside PPD, (2) the potential barrier at the interface, (3) the charge trapping at interface states and (4) the spillback. 71
4.7 Simulated waveforms with a dominant thermal noise in (a), only 1/f and thermal noise in (b) and a dominant RTS noise in addition to thermal noise in (c). . . . 72
4.8 Equivalent circuit for thermal noise in a resistor: noise current generator in parallel to the resistor and noise voltage in series. 73
4.9 Equivalent circuit for noise of a MOS transistor: noise current generator between drain and source of the transistor and noise voltage referred to the gate. 74
4.10 RC circuit in (a) and equivalent circuit for noise calculation in (b). 75
4.11 RTS noise PSD with Lorentzian shape and corresponding drain current fluctuations in the time domain for a small-area MOSFET (reprinted from [15]). 77
4.12 Impact in (a) on a steady current of the shot noise and evolution in time of the number of cumulated charge carriers crossing the barrier (reprinted from [6]). In (b), noise spectrum and as a function of measured gate current of a MOSFET in 100 nm (reprinted from [22]). 78
4.13 Gate leakage current components flowing between the SF terminals. 79

4.14 Measurement methodology for Temporal and Fixed Pattern Noise (adapted from [24]). . . . 81
4.15 Plotted in red, the total SNR as a function of the input photoelectrons number, N. In dashed lines, the SNRs which take into account only the TRN, the PSN and the FPN. These lines show the range of photoelectrons where each noise source is dominant. . . . 82
5.1 Conventional CIS readout chain based on a intra-pixel source-follower amplifier in (a). Timing diagram of a low noise CIS readout chain in (b) with the noise contributions added to the signal. On the left, hydraulic model of a PPD with TG, SN and RST showing different readout steps. . . . 88
5.2 Block diagram for the noise analysis showing the signal and noise transfer functions. The expressions of the transfer functions are reported and sketched in each block. . . . 90
5.3 Small-signal equivalent in (a) for the CIS readout chain in Fig. 5.1(a) together with the different readout noise sources. Parasitic capacitances in (b) contributing to the SN node term C_{p}. . . . 91
5.4 The term $|H_{\mathrm{CMS}}(f)|^2$ as a function of the frequency normalized to the CMS sampling period T_{CMS}, for four different values of the CMS order. . . . 93
5.5 The parameter α_{th} is multiplied by $M/2$ and plotted as a function of $f_{\mathrm{c}} \cdot T_{\mathrm{CMS}}$ for different values of M. . . . 95
5.6 $\alpha_{1/\mathrm{f}}$ in (a) as a function of $f_{\mathrm{c}} \cdot T_{\mathrm{CMS}}$ for different values of M. The same parameter is plotted in (b) as a function of M to emphasize the plateau of the residual flicker noise reduction with M. . . . 97
5.7 The parameter α_{shot} is plotted as a function of M. . . . 99
5.8 α_{RTS} as a function of M for different values of $f_{\mathrm{RTS}}/f_{\mathrm{c}}$. . . . 101

6.1 Schematic in (a) of the implemented CIS readout chain with a 4T pixel, the capacitive amplifier and SC CMS. Timing diagram in (b) of the readout chain with all the control signals for the SC CMS for M equal to 8. . . . 108
6.2 SC CDS circuit implementation. . . . 111
6.3 Averager circuit in (a) for a SC CMS order equal to four in a minimum number of capacitors. Timeline in (b) of the CMS $M = 4$ with all the phases and the operations for each phase. . . . 112
6.4 Generic CMS order M splitted into two blocks of order M/2 and a simple averager. 113
6.5 Comparison between calculated results and PNOISE and transient noise simulation results for different values of the averager capacitor (a) and various CMS orders (b). . . . 114
6.6 Schematic of the implemented capacitive amplifier in (a). Layout in (b) of the pixels A and B with the PPD and the TG, RST, RS and SF transistors. . . . 115
6.7 Chip micrograph showing the main blocks of the readout chains with biasing circuits and buffers. . . . 116

6.8 Setup for the characterization and the noise measurements of the readout chains implemented on the chip. 117
6.9 PTCs of the readout chain for different values of the CLA gain (from 1 to 128), in order from (a) to (f). The overall CG is reported in each figure for both pixels. . 118
6.10 Input-referred noise for both pixels as a function of the CLA gain value. The expected trend for thermal noise reduction is plotted with a dashed line. 119
6.11 Input-referred total noise for Pixel A (a) and Pixel B (b) as a function of the CMS order M. The measurements are compared with the total noise expression proposed in (6.9). 120
6.12 The square root of the fitting parameters σ^2_{th} (on the left axis), $\sigma^2_{1/\text{f}}$ and σ^2_{floor} (on the right axis) is plotted for each value of the column-level gain for Pixel A (a) and Pixel B (b). 121
6.13 Measured values of the thermal noise excess factor against IC for L equal to 240 nm, 180 nm, 120 nm, 100 nm and 40 nm (reprinted from [21]). 123
6.14 Total, thermal and flicker RMS charge noise as a function of the SF IC coefficient. In order to generate these curves, the following values are used for the main parameters: $C_{ox} = 4.5\,\text{fF}\,\mu\text{m}^{-2}$, $I_{spec\square} = 500\,\text{nA}$, $C_{ex} = 0.45\,\text{fF}\,\mu\text{m}^{-1}$, $n = 1.2$, $C_P = 0.75\,\text{fF}$, $\gamma_A = 1$ and $G_{mA} = 30\,\mu\text{A}\,\text{V}^{-1}$ 124
6.15 Total, thermal and flicker RMS charge noise as a function of the SF width in (a) and length in (b). The following values are used for the main parameters: $C_{ox} = 4.5\,\text{fF}\,\mu\text{m}^{-2}$, $I_{spec\square} = 500\,\text{nA}$, $C_{ex} = 0.45\,\text{fF}\,\mu\text{m}^{-1}$, $n = 1.2$, $C_P = 0.75\,\text{fF}$, $\gamma_A = 1$ and $G_{mA} = 30\,\mu\text{A}\,\text{V}^{-1}$ 125
6.16 Schematic in (a) of the simulated low-noise CIS readout chains. Timing diagram in (b) of the simulated CIS readout chain. 127
6.17 Input-referred thermal noise of the CIS readout chain with nMOS2.5 in (a), pMOS2.5 in (b) and pMOS1.2 SF in (c), respectively, as function of the column-level gain. 129
6.18 Simulated and calculated input-referred flicker noise of the CIS readout chains with different type of in-pixel SFs. 130
6.19 Input-referred total noise in (a) of the readout chain with nMOS2.5, pMOS1.2 and pMOS2.5 SF, respectively. Input-referred total noise of the readout chain with pMOS2.5 SF as a function of the load capacitance in (b). 131
6.20 Schematic of the simulated low-noise CIS readout chains. 132

6.21 Input-referred thermal noise of the CIS readout chain with nMOS2.5 (a), pMOS2.5 (b) and pMOS1.2 (c) SF, respectively, as function of the column-level gain and the CMS order M. In (d) input-referred flicker noise of the CIS readout chain with different type of in-pixel SFs, as function of the CMS order M. 133
6.22 Input-referred shot noise in (a) of the CIS readout chain with pMOS1.2 SF. Input-referred total noise in (b) of the CIS readout chain with the NMOS2.5, PMOS2.5 and PMOS1.2 SF, respectively. 134

6.23 Simulated histogram from (a) to (d) showing the influence of different readout noise levels on the output of an image sensor for an average number of 2 photons per pixel. 136
6.24 Histogram of the output signal voltage for 6 different inputs: results from the transient noise simulations of the readout chain in 65 nm with pMOS2.5 SF. . . 136

List of Tables

3.1 Main Parameters for Three Cases of Pinned Photodiodes 42
3.2 Summary of Values for Model Parameters 59

6.1 Summary Table for Noise Reduction Techniques 107
6.2 Values of the Process and Design Parameters 122
6.3 Relevant parameters for noise estimation and calculated input-referred flicker noise 126

1 Introduction

This chapter begins with a brief history of CMOS Image Sensors (CIS), starting from the first work in the 1960s to modern achievements. The major trends in camera and camera systems are then presented and followed by an overview of the state-of-the-art in Ultra-Low Light CIS. Finally, the motivation for the work is provided and the organization of the manuscript outlined.

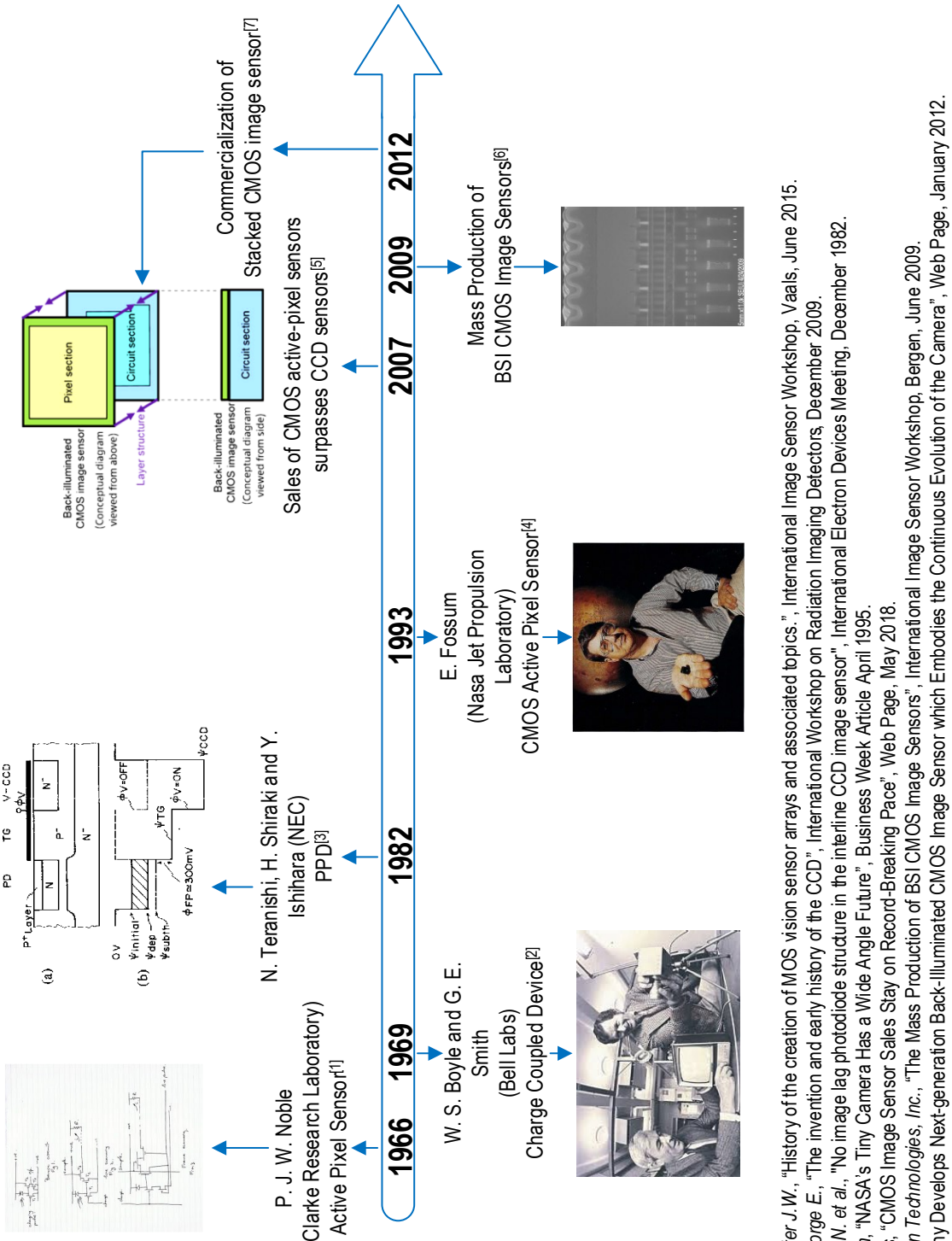
1.1 Brief History of CIS

The history of CIS is full of brilliant work and contributions from engineers and scientists all over the world [1]. This section aims to give a brief historical overview by mentioning some of the most important contributions to the development of modern sensors. A timeline with some ground breaking research is shown in Fig. 1.1.

Modern image sensors are based on metal-oxide-semiconductor (MOS) technology, a result of the MOS field-effect transistor (MOSFET) invented at Bell Labs in 1959 [2]. In the developed fabrication processes, two different type of MOS were available: the PMOS (p-type MOS) and the NMOS (n-type MOS).

In 1966, the first generation of optical sensor arrays was reported in the UK by Peter Noble of the Allen Clarke Research laboratory (Plessey), where the first self-scanned 10×10 sensor was implemented and the concept of an intra-pixel amplifier (active pixel) introduced [3]. At the new company set up by Noble, Integrated Photomatrix Ltd., a 64×64 array (4096 pixels) was implemented to be used in a monochrome camera for moving objects.

The development of semiconductor technology led to the invention of a charge-coupled device (CCD) in 1969 by Williard Boyle and George E. Smith at Bell Labs. While researching the use of MOS technology for electronic shift register [4], the basic building block of the CCD was created: the MOS capacitor. The two researchers realized in fact that a charge could be stored on a MOS structure. One of their colleagues, Michael F. Tompsett, noticed the potential of the CCD device for imaging applications [5]. For the imaging semiconductor circuit, Boyle and



[1] *Noble, Peter J.W.*, "History of the creation of MOS vision sensor arrays and associated topics.", International Image Sensor Workshop, Vaals, June 2015.
[2] *Smith, George E.*, "The invention and early history of the CCD", International Workshop on Radiation Imaging Detectors, December 2009.
[3] *Teranishi, N. et al.*, "No image lag photodiode structure in the interline CCD image sensor", International Electron Devices Meeting, December 1982.
[4] *E. Fossum*, "NASA's Tiny Camera Has a Wide Angle Future", Business Week Article April 1995.
[5] *IC Insights*, "CMOS Image Sensor Sales Stay on Record-Breaking Pace", Web Page, May 2018.
[6] *OmniVision Technologies, Inc.*, "The Mass Production of BSI CMOS Image Sensors", International Image Sensor Workshop, Bergen, June 2009.
[7] *Sony*, "Sony Develops Next-generation Back-illuminated CMOS Image Sensor which Embodies the Continuous Evolution of the Camera", Web Page, January 2012.

Figure 1.1: A summary history of CIS with the crucial events reported in a timeline: from the early development stages of technology to modern designs.

Smith were awarded the Nobel Prize Physics in 2009. CCDs had in fact an important impact on astronomy and were mounted on spacecraft to take images during robotic explorations of space [6].

Digital cameras and camcorders in the 1980s and 1990s embedded CCD sensors, which were industrialized and went into mass production in Japan [6]. The storing elements in CCDs are combined with electrodes positioned on top of an insulating material and on the surface of the semiconductor. They are used to apply a sequence of voltages and move the stored charges underneath from one element to the next. This image sensor works as a shift register for the photogenerated charge, until it reaches the corner of the chip where an amplifier is located. Based on their operational principle, CCDs require a nearly perfect charge transfer in order to avoid the so-called image lag. However, this property was difficult to obtain for large array sizes used at high frame rates and the electronics required to drive the sensor meant the final design was large and bulky.

The demand for more compact systems was one source of motivation for looking into new different solutions, and the integration in a CMOS process was the key to miniaturization. In order to achieve this goal, Eric Fossum at JPL built the first camera-on-chip in 1993 by replacing the multiple charge transfers with a single intra-pixel complete transfer and the output amplifier of a CCD with an intra-pixel one [7]. In this system, the output was sampled twice: once during the reset level and the other after the transfer of the photogenerated charge. The final output was the difference between the two measurements and the operation was called correlated double sampling (CDS). The technique was introduced to suppress the variance of transferred charges to a capacitor due to the Brownian motion of charge elements, also referred as kTC noise.

One of the key elements in modern CIS is the pinned photodiode (PPD), invented by Nobukazu Teranishi, Hiromitsu Shiraki and Yasuo Ishihara at the NEC Corporation in 1980 and published in 1982 [8]. The main advantages of this device were the lower lag, noise and dark current compared to conventional photodiodes, together with a higher quantum efficiency. At the beginning, the PPD was incorporated into CCD sensors in all consumer electronic cameras. By the time CMOS technology had surpassed CCD in the market sales [9], PPDs were being used in nearly all CISs.

The continuous growth in the camera industry led to the advent of large arrays in CIS with power consumption levels lower than CCD sensors. In 2009, Sony commercialized the CMOS back-side illumination (BSI) that further optimized the sensor in terms of quantum efficiency [10]. In 2012, the same company introduced the stacked CMOS BSI sensor opening to higher integration with electronic circuits [11]. The design of modern CISs is driven by the smartphone market and combines advanced chip stacking techniques with active pixels arrays embedding the latest 0.8 µm pixel generation into multiple camera systems [12].

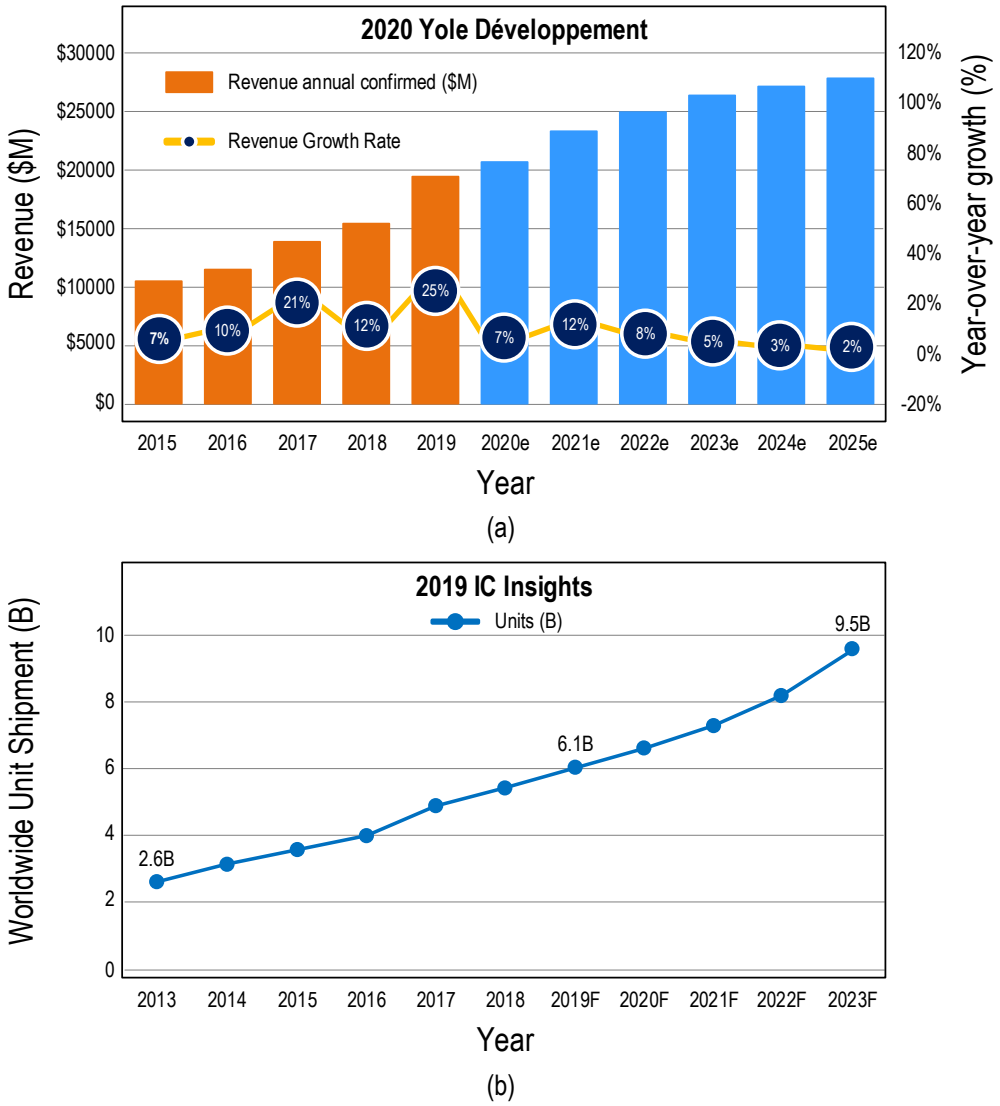


Figure 1.2: CIS market growth in (a) from 2016 to 2019 with forecasts up to 2025. The positive trend is expected to continue in the upcoming years (source: Yole Développement). Worldwide number of shipped image sensors in (b) according to IC Insights.

1.2 CIS Market and Major Trends

The considerable spread of CIS had a significant cultural impact: smartphone cameras and digital cameras are now part of our daily life. The rise of social media and selfie culture is linked to the spread of this technology, with social and political effects on people around the world.

In 2017, CMOS sensors accounted for 89% of the global image sensor market [9]. Yole Développement published the results of CIS market dynamics (Fig. 1.2(a)) with annual confirmed revenues from 2016 to 2019, and a forecast from 2020 to 2024 [13]. The continuous growth of

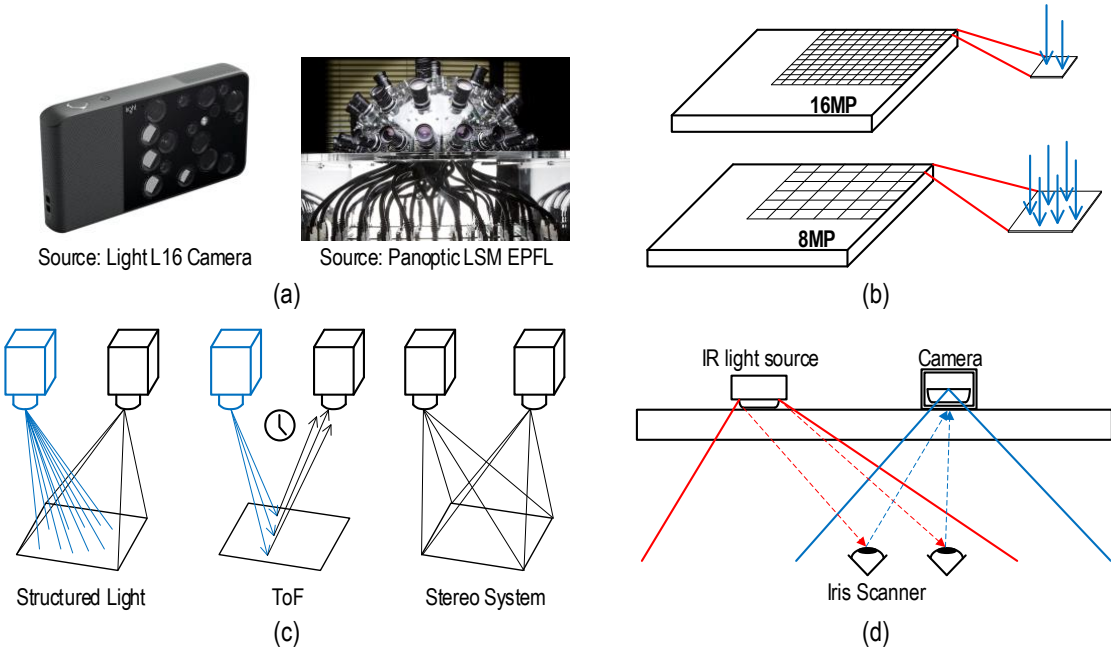


Figure 1.3: Modern trends described in [14] that involve image sensors and camera designs: multi-camera systems in (a), high resolution arrays in (b), 3D sensing in (c) and biometric ID based on iris-scanner in (d) (source: Daiwa Capital Markets).

CIS produced an annual revenue of US$ 19.3b in 2019, exceeding 4.6% of total semiconductor sales. The revenues are expected to continue growing and exceed US$ 27.5 billion in profits. According to IC Insights and as shown in Fig. 1.2(b), 6.1 billion image sensors are shipped worldwide each year (193 per second) [1, 9].

The smartphone sales (estimated global revenue of US$ 522 billion in 2018 [15]) is the main driving force of the CIS market. A summary of the main modern trends involving image sensors and camera designs is shown in Fig. 1.3 and extensively described in [14].

The multi-camera era represented in Fig. 1.3(a) started with the adoption of dual-cam smartphones and is now turning into triple and quad-cam systems with enhanced camera functions for image quality. The major benefits of multiple cams include higher optical zoom compared to dual-cams, broader angle, better image quality in low-light environment, enhanced functionality for Artificial Intelligence (AI) (e.g. face, objects and scenes detection and recognition) and auto adjustments of multiple parameters for optimum image output. As predicted in [14], a broader adoption of multiple cams in smartphones is expected during the course of 2020.

Smartphone cameras have also migrated towards higher resolution (from tens to hundreds of mega-pixels) incorporating pixels with a sub-micrometer distance from each other (pixel pitch) [12]. More imaging functions are possible by equipping phones with these state-of-the-art image sensors at the cost of a more complicated design. As shown in Fig. 1.3(b), the

Figure 1.4: Frames from advertisement in 2020 of the top smartphones of Apple and Samsung, respectively, involving good performances at low-light levels to appeal to consumers.

reduced pixel size allows in fact less light to be captured and longer focal length and results in a higher thickness for the camera module.

In addition, the leading companies in the market are developing 3D sensing modules to provide 3D features such as gesture or facial recognition [16]. The newly-developed modules consist of a receiver and a transmitter to project and receive light. Fig. 1.3(c) shows the main approaches to 3D sensing: structured light, time of flight (ToF) and stereo systems. Applications for this technology include augmented reality (AR), face and gesture recognition, 3D scanning and mobile payments.

Modern smartphone have adopted biometric ID technology for the iris recognition performed by an extra front camera processing the eye images, as drawn in Fig. 1.3(d) and detailed in [17].

1.3 Ultra-Low Noise CIS – an Overview

Ultra low noise CIS are fundamental to reaching high performance in low light imaging for applications such as surveillance, security, night vision and consumer electronics [18, 19, 20], where a good low light performance is crucial. The feature of high sensitivity is also very useful in applications like microscopy, high-precision scientific imaging and 3D vision based on indirect-Time-of-Flight (I-ToF) imagers [21, 22, 23]. As shown in Fig. 1.4, Apple and Samsung (who were reported to capture 56% of all smartphone industry revenues in 2019 [24]) use low-light performance (or night vision) as a key feature of their devices and advertising strategy to appeal to consumers. Hence, both industry and scientific institutions are interested in an image sensor that not only needs to exhibit an incredibly low value of noise, but also offers at the same time a high resolution and speed.

As shown in Fig. 1.5, the current state-of-the-art in low noise CIS exhibits sub-electron input-referred total noise, which represents a step towards the single photon detection capability for these sensors. The additive readout noise e.g. 1 or 2 e^-_{rms} was in fact responsible for the not

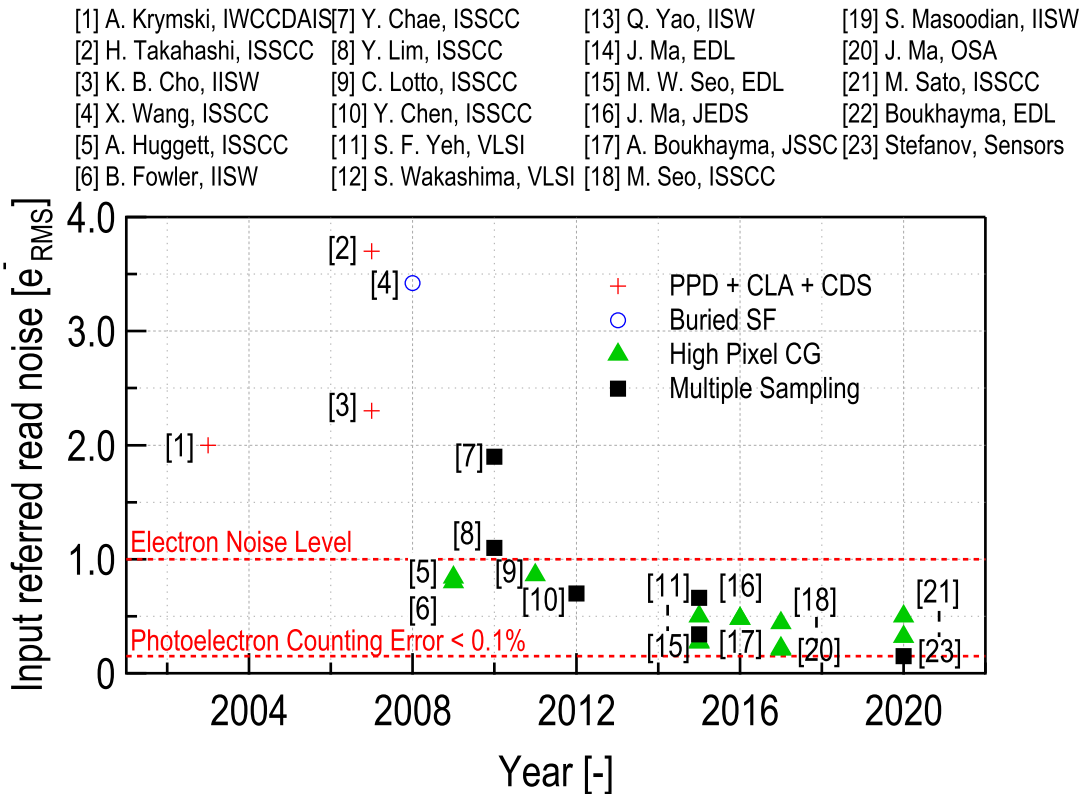


Figure 1.5: Values of input-referred read noise in articles published from 2003 to 2020 and reported in the references of this chapter. A large amount of research reached the sub-electron noise value, while the level for a photoelectron counting error lower than 0.1% (0.15 e^-_{rms}) is very close in recent publications.

visible quantized nature of the input light in a standard camera output.

In modern ultra low noise CISs, once the contribution of the column-level stages is reduced by using high column-level voltage gain and reduced bandwidth, the noise contribution from the pixel becomes the dominant noise source, particularly that generated by the in-pixel source follower (SF) [25]. To further decrease the input-referred noise, noise reduction techniques need to be implemented at different levels of the readout chain. At process level, changes in the standard flow are used in [26, 27, 28], whereas at pixel-level, where the degree of freedom left to designers is generally limited, optimizations and circuit techniques are used in order to reduce the sense node (SN) capacitance [29, 30, 31, 32]. The technology scaling of CIS processes and the associated reduction in the parasitic capacitances are often used to obtain a higher pixel gain, as reported in modern sensor design with a SN capacitance, C_{SN} , of less then 1 fF [33]. The main drawback in having a smaller C_{SN} is the reduction of the maximum amount of charges or full well capacity (FWC) that can be processed. Different circuit techniques compatible with different pixels are implemented instead at column-level [34, 35, 36, 37]. The research results on noise reduction shown in Fig. 1.5 define two main approaches: the increase in the conversion gain (CG) [38, 30, 39] and the correlated multiple sampling (CMS) [40, 41].

An alternative approach is proposed in Quanta Image Sensor (QIS), where the advance in pixel scaling is used to provide billions of elements (jots) that can be read at a very high rate (1000 fps) with a digital output [42]. The single photon-counting capability is combined with high temporal and spatial resolution to generate a series of images (cubicle) used for image reconstruction. The photon arrival rate described by a Poisson process is used in high-density QIS to obtain a higher non-linear interval of exposure (over-exposure latitude) compared to a linear image sensor. A SN capacitance lower than 0.5 fF is the key in QIS to reaching deep sub-electron performance and it is achieved by implementing the pump-gate jot device that minimizes the transfer gate (TG) to SN overlap capacitance [27]. Experimental data of quantized outputs ($0.175e^-_{rms}$) with low erroneous dark counts ($0.07e^-/s$) have been shown by means of Photon Counting Histograms (PCH) ultimately used to characterize the sensor in terms of read noise and conversion gain [33, 43]. The residual noise is attributed to the flicker noise originated in the in-pixel SF and characterized in [25]. The experimental results of a 1 Mjot QIS prototype has been shown in [42] with an input-referred noise equal to $0.22e^-_{rms}$ at 1040fps and for a power consumption of 17.6 mW.

Another major alternative for single photon detection is offered by Single Photon Avalanche Diodes (SPADs) that use avalanche multiplication for charge gain. This phenomenon is achieved when a high internal electric field is generated at the cost of a higher operating voltage (15-20V) and a larger pixel pitch in order to guarantee isolation. The photon detection time resolution of SPADs is currently the best among modern technologies and reaches sub-nanosecond range [44]. Unlike their CMOS counterpart, these sensors suffer from high dark count rates and a dead time during which the pixel is not active. Recent research has improved the fill factor and array sizes and become appealing for a wide variety of applications [45].

1.4 Thesis Motivation and Organization

The goal of the work presented here is to model ultra-low noise CIS with regard to further noise reduction. Because the developed models need to be a convenient tool for CIS designers, the aim is to produce a low level of complexity. Two research directions are described to achieve this, and will be discussed in the following chapters.

The first develops a compact physics-based model of a PPD-based pixel as a tool for CIS designers who need to optimize the sensor performance and look into device-level phenomena for further improvements. The main step conducted in this research is modeling the charge transfer mechanism of the photogenerated charges in the PPD. Simple analytical expressions based on simplified 2D equivalent structures will be derived and compared with software simulations and measurement results. The model verification becomes extremely useful to evaluate the validity of the assumptions and define the main trends related to the process and design parameters.

The second consists in evaluating the impact of different noise reduction techniques and comparing it with the available models for thermal, flicker and shot noise. Such a comparison

seeks to be extensive, hence different pixel designs and values of the main design parameters are evaluated. The comparison between the model and measurement results under various conditions becomes extremely useful to better define the effects and limitations of each technique.

The thesis is organized as follows:

Chapter 2 explains the fundamentals of photodetecting devices, pixel topologies and CIS architectures. An ultra-low noise CIS architecture is presented together with the main building blocks. Various possible implementations are described and compared to each other in terms of general performance metrics for an image sensor.

Chapter 3 presents the core of a compact model for the charge transfer between the PPD and TG. The analytical expressions derived from equivalent two-dimensional (2-D) structures are first used to match with software simulations and then compared with measurements from a readout chain implemented in a 180 nm CIS technology.

Chapter 4 describes the noise sources in CIS and defines their main properties by looking at the physical mechanisms. The statistical models of each source are then combined in order to evaluate the impact at different light levels. The dominant role of the readout noise at low-light illuminations is then established.

Chapter 5 presents a readout noise analysis for conventional low-noise CIS chains based on an in-pixel SF amplifier. A small-signal noise equivalent circuit is used to calculate the signal and noise transfer functions that allow the input-referred expressions for the thermal, flicker and leakage current shot noise to be derived.

Chapter 6 focuses on the noise reduction techniques evaluated in this work. The core of the chapter is the first analog implementation of the CMS with a passive SC circuit, and is used to show its impact on the total input-referred noise of the readout chain when combined to column-level voltage gain. The last section focuses on the effects of technology downscaling on noise when combined with other noise reduction techniques at circuit-level. The transient noise simulation results for a standard 65 nm process are used as a comparison with the model.

Chapter 7 concludes the dissertation, providing a summary of the results and contributions, and pointing to potential topics for future research.

References for Chapter 1

[1] E. R. Fossum, “The Invention of CMOS Image Sensors: A Camera in Every Pocket,” in *2020 Pan Pacific Microelectronics Symposium (Pan Pacific)*, pp. 1–6, 2020.

[2] R. K. Bassett, *To the Digital Age: Research Labs, Start-up Companies, and the Rise of MOS*

Technology. USA: Johns Hopkins University Press, 2002.

[3] P. J. Noble, "History of the creation of MOS vision sensor arrays and associated topics. And what does – or should - the future hold?," in *Proceedings of the International Image Sensor Workshop*, June 2015.

[4] G. E. Smith, "The invention and early history of the CCD," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 607, no. 1, pp. 1–6, 2009. Radiation Imaging Detectors 2008.

[5] M. Tompsett, "Charge transfer imaging devices," 1978. Patent US 4,085,456, Apr., 1978. Available on: https://www.google.com/patents/US4085456. Accessed on June 2020.

[6] J. Janesick, *Scientific Charge-Coupled Devices*. SPIE Press, 2001.

[7] E. R. Fossum, "Cmos image sensors: electronic camera-on-a-chip," *IEEE Transactions on Electron Devices*, vol. 44, no. 10, pp. 1689–1698, 1997.

[8] N. Teranishi, A. Kohno, Y. Ishihara, E. Oda, and K. Arai, "An Interline CCD Image Sensor with Reduced Image Lag," *IEEE Transactions on Electron Devices*, vol. 31, no. 12, pp. 1829–1833, 1984.

[9] IC Insights, "CMOS Image Sensor Sales Stay on Record-Breaking Pace," 2007. Available on: https://www.icinsights.com/news/bulletins/CMOS-Image-Sensor-Sales-Stay-On-RecordBreaking-Pace/. Accessed on May 2020.

[10] H. Yamanaka, "US patent 7521335," *Method and apparatus for producing ultra-thin semiconductor chip and method and apparatus for producing ultra-thin back-illuminated solid-state image pickup device*. Issued 2009-04-21. Assigned to Sony Corporation.

[11] H. Tsugawa, H. Takahashi, R. Nakamura, T. Umebayashi, T. Ogita, H. Okano, K. Iwase, H. Kawashima, T. Yamasaki, D. Yoneyama, J. Hashizume, T. Nakajima, K. Murata, Y. Kanaishi, K. Ikeda, K. Tatani, T. Nagano, H. Nakayama, T. Haruta, and T. Nomoto, "Pixel/dram/logic 3-layer stacked cmos image sensor technology," in *2017 IEEE International Electron Devices Meeting (IEDM)*, pp. 3.2.1–3.2.4, 2017.

[12] R. Fontaine, "The State-of-the-Art of Smartphone Imagers," in *Proceedings of the 2019 International Image Sensor Workshop*, Snowbird, Utah, June 24-27, 2019.

[13] Yole Développement, "Cis: Q4 2019 went way above forecast but this was before covid-192," 2020. Quarterly Market Monitor. Available on: http://www.yole.fr/iso_upload/News/2020/PR_CIS_QUARTERLY_MARKET_MONITOR_YOLE_March2020.pdf. Accessed on May 2020.

[14] Daiwa Capital Markets, "The more the merrier: multi-cameras are the next mega trend in smartphones," Mar. 2019. Available on: https://asiaresearch.hk.daiwacm.com/. Accessed on June 2020.

[15] Statista, "Global revenue from smartphone sales from 2013 to 2018," 2020. Available on: https://www.statista.com/. Accessed on June 2020.

[16] Ray Fontaine, Tech Insights, "Imaging + Sensing End-of-Year Highlights," 2007. Available on: https://www.techinsights.com/blog/imaging-sensing-end-year-highlights/. Accessed on June 2020.

[17] Calvin Hsieh, "Fingerprint-on-display adoptions increased to more than 200 million in 2019," 2020. Available on: https://technology.informa.com/. Accessed on June 2020.

[18] Y. Oike, K. Akiyama, L. D. Hung, W. Niitsuma, A. Kato, M. Sato, Y. Kato, W. Nakamura, H. Shiroshita, Y. Sakano, Y. Kitano, T. Nakamura, T. Toyama, H. Iwamoto, and T. Ezaki, "8.3M-Pixel 480-fps Global-Shutter CMOS Image Sensor with Gain-Adaptive Column ADCs and Chip-on-Chip Stacked Integration," *IEEE Journal of Solid-State Circuits*, vol. 52, pp. 985–993, April 2017.

[19] T. Takahashi, Y. Kaji, Y. Tsukuda, S. Futami, K. Hanzawa, T. Yamauchi, P. W. Wong, F. T. Brady, P. Holden, T. Ayers, K. Mizuta, S. Ohki, K. Tatani, H. Wakabayashi, and Y. Nitta, "A Stacked CMOS Image Sensor With Array-Parallel ADC Architecture," *IEEE Journal of Solid-State Circuits*, vol. 53, pp. 1061–1070, April 2018.

[20] Y. Développement, "Status of the CMOS Image Sensor Industry report." http://www.yole.fr/CIS_Markets_Applications.aspx#.W_V3t5NKiUk. Accessed on May, 2019.

[21] M. Seo, Y. Shirakawa, Y. Kawata, K. Kagawa, K. Yasutomi, and S. Kawahito, "A Time-Resolved Four-Tap Lock-In Pixel CMOS Image Sensor for Real-Time Fluorescence Lifetime Imaging Microscopy," *IEEE Journal of Solid-State Circuits*, vol. 53, pp. 2319–2330, Aug 2018.

[22] F. Acerbi, M. Moreno-Garcia, G. Köklü, R. M. Gancarz, B. Büttgen, A. Biber, D. Furrer, and D. Stoppa, "Optimization of Pinned Photodiode Pixels for High-Speed Time of Flight Applications," *IEEE Journal of the Electron Devices Society*, vol. 6, pp. 365–375, 2018.

[23] C. S. Bamji, P. O'Connor, T. Elkhatib, S. Mehta, B. Thompson, L. A. Prather, D. Snow, O. C. Akkaya, A. Daniel, A. D. Payne, T. Perry, M. Fenton, and V. Chan, "A 0.13 μm CMOS System-on-Chip for a 512x424 Time-of-Flight Image Sensor With Multi-Frequency Photo-Demodulation up to 130 MHz and 2 GS/s ADC," *IEEE Journal of Solid-State Circuits*, vol. 50, pp. 303–319, Jan 2015.

[24] Strategy Analytics, "Global smartphone wholesale revenue up +42019," 2020. Available on: https://www.strategyanalytics.com/. Accessed on June 2020.

[25] W. Deng and E. R. Fossum, "1/f noise modelling and characterization for cmos quanta image sensors," *Sensors*, vol. 19, p. 5459, Dec 2019.

[26] Y. Chen, X. Wang, A. J. Mierop, and A. J. P. Theuwissen, "A CMOS Image Sensor With In-Pixel Buried-Channel Source Follower and Optimized Row Selector," *IEEE Transactions on Electron Devices*, vol. 56, pp. 2390–2397, Nov 2009.

[27] J. Ma and E. R. Fossum, "A pump-gate jot device with high conversion gain for a quanta image sensor," *IEEE Journal of the Electron Devices Society*, vol. 3, pp. 73–77, March 2015.

[28] M. Seo, T. Wang, S. Jun, T. Akahori, and S. Kawahito, "A 0.44e$^{-}_{rms}$ read-noise 32fps 0.5Mpixel high-sensitivity RG-less-pixel CMOS image sensor using bootstrapping reset," in *2017 IEEE International Solid-State Circuits Conference (ISSCC)*, pp. 80–81, Feb 2017.

[29] S. Suh, S. Itoh, S. Aoyama, and S. Kawahito, "Column-Parallel Correlated Multiple Sampling Circuits for CMOS Image Sensors and Their Noise Reduction Effects," *Sensors*, vol. 10, no. 10, pp. 9139–9154, 2010.

[30] C. Lotto, P. Seitz, and T. Baechler, "A sub-electron readout noise CMOS image sensor with pixel-level open-loop voltage amplification," in *2011 IEEE International Solid-State Circuits Conference*, pp. 402–404, Feb 2011.

[31] A. Boukhayma, A. Peizerat, and C. Enz, "A Sub-0.5 Electron Read Noise VGA Image Sensor in a Standard CMOS Process," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 9, pp. 2180–2191, 2016.

[32] Jungwook Yang, K. G. Fife, L. Brooks, C. G. Sodini, A. Betts, P. Mudunuru, and Hae-Seung Lee, "A 3mpixel low-noise flexible architecture cmos image sensor," in *2006 IEEE International Solid State Circuits Conference - Digest of Technical Papers*, pp. 2004–2013, 2006.

[33] J. Ma, S. Masoodian, D. A. Starkey, and E. R. Fossum, "Photon-number-resolving megapixel image sensor at room temperature without avalanche gain," *Optica*, vol. 4, pp. 1474–1481, Dec. 2017. Publisher: Optical Society of America.

[34] R. J. Kansy, "Response of a correlated double sampling circuit to 1/f noise generated in CCD arrays," *IEEE Journal of Solid-State Circuits*, vol. 15, pp. 373–375, June 1980.

[35] G. R. Hopkinson and D. H. Lumb, "Noise reduction techniques for CCD image sensors," *Journal of Physics E: Scientific Instruments*, vol. 15, pp. 1214–1222, nov 1982.

[36] N. Kawai and S. Kawahito, "Effectiveness of a correlated multiple sampling differential averager for reducing 1/f noise," *IEICE Electronics Express*, vol. 2, pp. 379–383, 07 2005.

[37] A. Boukhayma, A. Peizerat, A. Dupret, and C. Enz, "Design optimization for low light CMOS image sensors readout chain," *New Circuits and Systems Conference (NEWCAS), 2014 IEEE 12th International*, pp. 241–244, June 2014.

[38] A. Huggett, C. Silsby, S. Cami, and J. Beck, "A dual-conversion-gain video sensor with dewarping and overlay on a single chip," in *2009 IEEE International Solid-State Circuits Conference - Digest of Technical Papers*, pp. 52–53,53a, Feb. 2009. ISSN: 2376-8606.

[39] M. Sato, Y. Yorikado, Y. Matsumura, H. Naganuma, E. Kato, T. Toyofuku, A. Kato, and Y. Oike, "5.8 A 0.50e$^-_{rms}$ 1.45micrometer-Pitch CMOS Image Sensor with Reference-Shared In-Pixel Differential Amplifier at 8.3Mpixel 35fps," in *2020 IEEE International Solid- State Circuits Conference - (ISSCC)*, pp. 108–110, Feb. 2020. ISSN: 2376-8606.

[40] Q. Yao, B. Dierickx, B. Dupont, G. Ruttens, and H. Consciencestraat, "CMOS image sensor reaching 0.34 e$^-_{rms}$ read noise by inversion-accumulation cycling," in *Proceedings of the International Image Sensor Workshop*, p. 4, June 2015.

[41] K. D. Stefanov, M. J. Prest, M. Downing, E. George, N. Bezawada, and A. D. Holland, "Simulations and Design of a Single-Photon CMOS Imaging Pixel Using Multiple Non-Destructive Signal Sampling," *Sensors*, vol. 20, p. 2031, Jan. 2020. Number: 7 Publisher: Multidisciplinary Digital Publishing Institute.

[42] S. Masoodian, J. Ma, D. Starkey, Y. Yamashita, and E. R. Fossum, "A 1Mjot 1040fps 0.22e-rms Stacked BSI Quanta Image Sensor with Cluster-Parallel Readout," in *Proceedings of the International Image Sensor Workshop*, p. 4, June 2017.

[43] D. A. Starkey and E. R. Fossum, "Determining conversion gain and read noise using a photon-counting histogram method for deep sub-electron read noise image sensors," *IEEE Journal of the Electron Devices Society*, vol. 4, no. 3, pp. 129–135, 2016.

[44] C. Bruschini, H. Homulle, I. Antolovic, S. Burri, and E. Charbon, "Single-photon avalanche diode imagers in biophotonics: review and outlook.," in *Light Sci Appl 8, 87.*, 2019.

[45] K. Morimoto, A. Ardelean, M.-L. Wu, A. C. Ulku, I. M. Antolovic, C. Bruschini, and E. Charbon, "Megapixel time-gated spad image sensor for 2d and 3d imaging applications," *Optica*, vol. 7, pp. 346–354, Apr 2020.

[46] N. Teranishi, A. Kohono, Y. Ishihara, E. Oda, and K. Arai, "No image lag photodiode structure in the interline ccd image sensor," in *1982 International Electron Devices Meeting*, 1982.

[47] E. Fossum, "Nasa's tiny camera has a wide-angle future," 1995. Business Week Article. Available on: http://ericfossum.com/Articles/Cumulative%20Articles%20about%20EF/Business%20Week%201995.pdf. Accessed on May 2020.

[48] OmniVision Technologies, Inc., "The Mass Production of BSI CMOS Image Sensors," in *Proceedings of the International Image Sensor Workshop*, 2009.

[49] Sony Global, "Sony Develops Next-generation Back-Illuminated CMOS Image Sensor which Embodies the Continuous Evolution of the Camera," 2012. Available on: http://www.sony.net/SonyInfo/News/Press/201201/12-009E/index.html. Accessed on May 2020.

[50] A. Krymski, N. Khaliullin, and H. Rhodes, "A 2 e$^-$ Noise 1.3Megapixel CMOS Sensor," in *IEEE Workshop on Charge-Coupled Devices and Advanced Image Sensors*, p. 6, 2003.

[51] B. Fowler, C. Liu, S. Mims, J. Balicki, W. Li, H. Do, and P. Vu, "Wide Dynamic Range Low Light Level CMOS Image Sensor," in *Proceedings of the International Image Sensor Workshop*, p. 4, June 2009.

[52] K.-B. Cho, C. Lee, S. Eikedal, H. Yan, T. Cho, T.-M. Miao, J. Song, C. Zeleznik, A. Mokhnatyuk, and S. Barna, "A 2.3e$^-$ Read Noise 1.3Mpixel CMOS Image Sensor with Per-Column Amplifier," in *Proceedings of the International Image Sensor Workshop*, p. 3, June 2007.

[53] X. Wang, M. F. Snoeij, P. R. Rao, A. Mierop, and A. J. Theuwissen, "A CMOS Image Sensor with a Buried-Channel Source Follower," in *2008 IEEE International Solid-State Circuits Conference - Digest of Technical Papers*, pp. 62–595, Feb. 2008. ISSN: 2376-8606.

[54] Y. Chen, Y. Xu, Y. Chae, A. Mierop, X. Wang, and A. Theuwissen, "A 0.7e$^-_{\text{rms}}$ temporal readout-noise CMOS image sensor for low-light-level imaging," *2012 IEEE International Solid-State Circuits Conference (ISSCC)*, pp. 384–386, Feb 2012.

[55] Y. Lim, K. Koh, K. Kim, H. Yang, J. Kim, Y. Jeong, S. Lee, H. Lee, S.-H. Lim, Y. Han, J. Kim, J. Yun, S. Ham, and Y.-T. Lee, "A 1.1e$^-$ temporal noise 1/3.2-inch 8Mpixel CMOS image sensor using pseudo-multiple sampling," in *2010 IEEE International Solid-State Circuits Conference - (ISSCC)*, pp. 396–397, Feb. 2010. ISSN: 2376-8606.

[56] S. Yeh, K. Chou, H. Tu, C. Y. Chao, and F. Hsueh, "A 0.66e$^-_{\text{rms}}$ Temporal Readout Noise 3-D-Stacked CMOS Image Sensor With Conditional Correlated Multiple Sampling Technique," *IEEE Journal of Solid-State Circuits*, vol. 53, pp. 527–537, Feb 2018.

[57] H. Takahashi, T. Noda, T. Matsuda, T. Watanabe, M. Shinohara, T. Endo, S. Takimoto, R. Mishima, S. Nishimura, K. Sakurai, H. Yuzurihara, and S. Inoue, "A 1/2.7 inch Low-Noise CMOS Image Sensor for Full HD Camcorders," in *2007 IEEE International Solid-State Circuits Conference. Digest of Technical Papers*, pp. 510–618, Feb. 2007. ISSN: 2376-8606.

[58] S. Wakashima, F. Kusuhara, R. Kuroda, and S. Sugawa, "A linear response single exposure CMOS image sensor with 0.5e$^-$ readout noise and 76ke$^-$ full well capacity," in *2015 Symposium on VLSI Circuits (VLSI Circuits)*, pp. C88–C89, June 2015. ISSN: 2158-5636.

[59] J. Ma, L. Anzagira, and E. R. Fossum, "A 1 micrometer-Pitch Quanta Image Sensor Jot Device With Shared Readout," *IEEE Journal of the Electron Devices Society*, vol. 4, pp. 83–89, Mar. 2016. Conference Name: IEEE Journal of the Electron Devices Society.

[60] J. Ma and E. R. Fossum, "Quanta Image Sensor Jot With Sub 0.3e$^-_{\text{rms}}$ Read Noise and Photon Counting Capability," *IEEE Electron Device Letters*, vol. 36, pp. 926–928, Sept. 2015.

[61] M. W. Seo, S. Kawahito, K. Kagawa, and K. Yasutomi, "A 0.27 e^-_{rms} Read Noise 220 μV/e- Conversion Gain Reset-Gate-Less CMOS Image Sensor with 0.11 μm CIS Process," *IEEE Electron Device Letters*, vol. 36, no. 12, pp. 1344–1347, 2015.

[62] A. Boukhayma, A. Caizzone, and C. Enz, "A CMOS Image Sensor Pixel Combining Deep Sub-electron Noise with Wide Dynamic Range," *IEEE Electron Device Letters*, pp. 1–1, 2020. Conference Name: IEEE Electron Device Letters.

[63] Y. Chae, J. Cheon, S. Lim, D. Lee, M. Kwon, K. Yoo, W. Jung, D.-H. Lee, S. Ham, and G. Han, "A 2.1Mpixel 120frame/s CMOS image sensor with column-parallel delta-sigma ADC architecture," in *2010 IEEE International Solid-State Circuits Conference - (ISSCC)*, pp. 394–395, Feb. 2010. ISSN: 2376-8606.

2 CMOS Image Sensors

This chapter reviews the background knowledge of CIS. The main concepts behind silicon-based photodetectors are introduced and include the energy gap and light absorption spectra. Several devices used in image sensors are described: the pn-junction, the MOS or photogate, the buried MOS used in CCDs and the PPD in modern CIS. Their physical structures are defined and the operational principles compared. The CIS architecture is then shown and explained by using a generic block and timing diagram. Various implementations for each building block are presented.

2.1 Silicon-based Photodetectors

The knowledge developed for imaging is one of the most fascinating chapters in the history of physics and engineering and involved the greatest minds, starting from the sixteenth and seventeenth centuries. An image sensor constructs a map in space and time of the light intensity reaching its photosensitive array. Related topics such as the physical nature of light and light-matter interactions are behind each image formation. The physical nature of light is not discussed here, but textbooks such as [1, 17] give detailed explanations. The basics of semiconductor physics and optical properties of silicon are recalled in this section.

2.1.1 Device Physics

One of the main concepts in semiconductor device physics is the energy band, introduced in order to explain how mobile charges are distributed in crystal structures [21]. As shown in Fig. 2.1(a), for silicon (lattice constant equal to 5.43 Å) it is possible to distinguish two allowed energy regions, respectively the valence and conduction bands, and a forbidden one, whose height is defined as the energy gap or band-gap, E_g (1.12 eV at 300 K and 1.17 eV at 0 K for silicon (Si)). Within each allowed band, from the lowest to the higher, the energy states are occupied by electrons. The band-gap prevents mobile charges from rising to the conduction band, which at equilibrium and for a temperature, T, equal to 0 K, contains no mobile charge

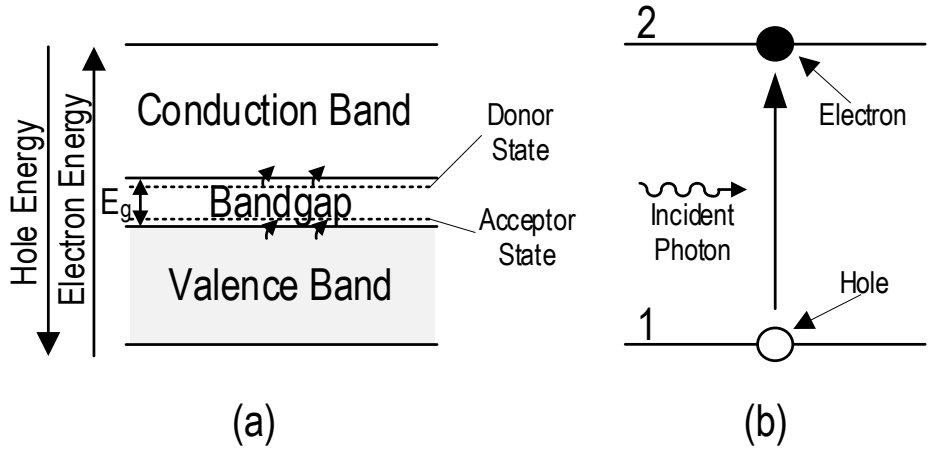


Figure 2.1: Energy band diagram of semiconductor in (a). The absorption shown in (b) is one of the possible interactions between the light and the matters.

and determines a zero electric current flowing in the material.

By only looking at the energy band diagrams, an insulator differs from a semiconductor in that it possesses a higher energy gap. However, the electrical conductivity of semiconductor devices can be drastically increased by the doping technique, which introduces impurities into the intrinsic material [20]. Although the inserted atoms are electrically neutral, the thermal excitation at room temperature is enough for electrons to become free from the bound state. The remaining atoms are ionized: donor impurities are charged positively by releasing electrons into the conduction band, while acceptors become negatively charged due to electrons from the valence band. The *n*-type semiconductors have therefore a higher population (majority carriers) of electrons as mobile charges, while a *p*-type semiconductor refers to the positively charged holes. Holes in *n*-type semiconductors and electrons in *p*-type are called minority carriers [21].

2.1.2 Optical Absorption

Since photons are directly transduced into electric charges, the interaction between light and matter is a fundamental topic. Fig. 2.1(b) shows the basic principle of absorption when the matter is modeled as a system of two energy levels, a basic and an excited one. The absorbed photon gives its energy to an electron moving from the basic to the excited state.

The formulation based on two discrete levels of energy can be extended to semiconductor materials, where the basic state is replaced by the valance band and the excited state with the conduction band. The absorbed photons causing a charge to move from one band to the other need to have an equal or higher energy compared to the band-gap of the semiconductor material. Due to the band-gap of silicon, photons have a minimum energy to be absorbed,

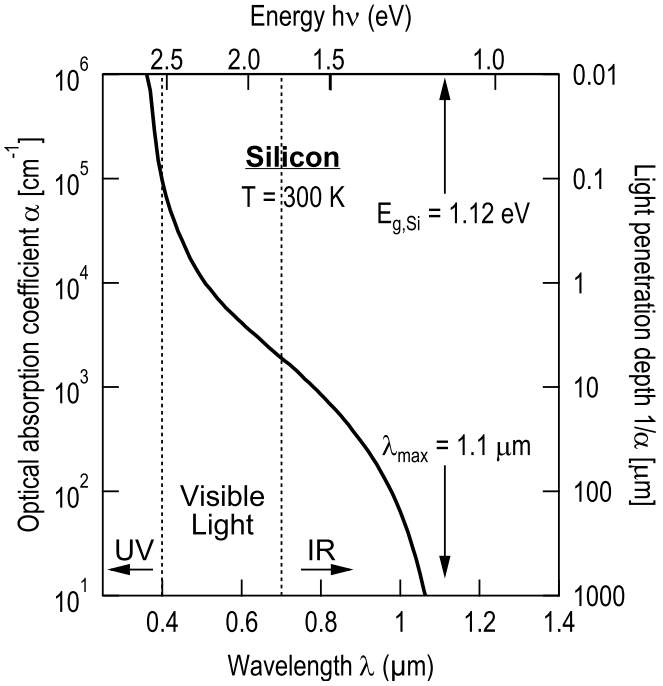


Figure 2.2: Absorption coefficient as a function of wavelength for silicon material. Below the cutoff wavelength, absorption increases gradually due to the fact that Si is an indirect gap material.

which can be translated into a cut-off wavelength, λ_{max}, above which light is not absorbed (1.1 µm for silicon). As shown in Fig. 2.2, the particular value of the silicon band-gap allows photons within the range of visible light to be absorbed and to generate an equivalent number of charges within the device.

When light hits the sensor, part of the incident power is reflected, while the remainder propagates inside the material. Due to absorption, the transmitted energy decreases exponentially with the distance from surface. This phenomenon determines how far into a material light of a particular wavelength can penetrate. In order to define the amount of absorbed photons at each centimeter and the light penetration depth, the absorption coefficient, α, is defined and expressed in cm^{-1}. At a particular distance from surface, the generation rate (number of carriers per second and distance) is given by multiplying the number of photons per second at a specific distance inside the material by the value of α. In Fig. 2.2, α is plotted against the light wavelength, λ, showing the sharp edge in the absorption and a lower penetration depth for photons with higher energy.

2.1.3 Device Components

The main device components used in image sensors are briefly explained in this section. The energy band diagrams are drawn when the device is under equilibrium condition and when an external voltage is applied. The main electrical and optical properties of each device are

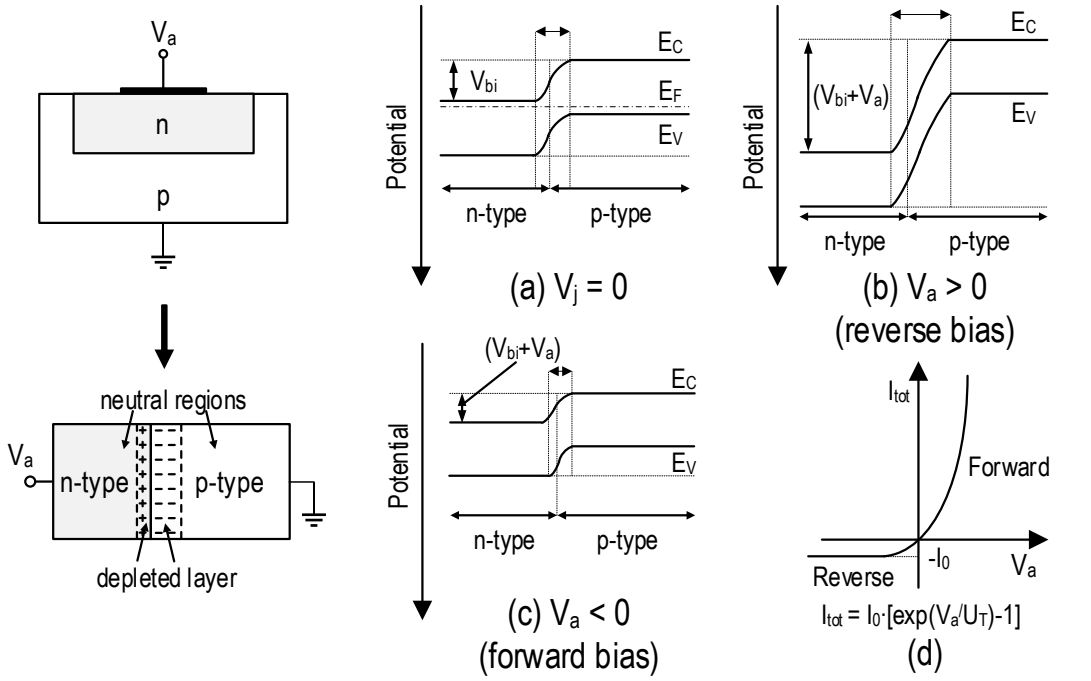


Figure 2.3: Cross-section of a pn-junction and its 2D equivalent representation. The electrostatic potential profile is depicted at equilibrium in (a), in reverse bias in (b) and in forward bias in (c). The I-V characteristic is shown in (d).

therefore defined.

pn-Junction (Photodiode)

Fig. 2.3 shows a pn-junction and its 2D equivalent structure. When the two doped regions are connected, electrons in the n-type and holes in the p-type diffuse from the borders of the junction toward opposite areas. Being minority carriers in a neutral region, during this operation electrons and holes recombine, while the left impurities become ionized and form an electric field at the interface to balance out the diffusion process. Near the junction, ionized donors in the n-type region and acceptors in the p-type are spatially fixed charges and, since no mobile charge remains, this area is called the depletion layer. Under a fully-depleted approximation, the transition between neutral and depleted regions is assumed to be abrupt.

From the energy diagram at thermal equilibrium in Fig. 2.3(a), it is possible to derive the potential profile characterized by the barrier between the two regions, where its height is typically defined as the junction built-in potential, V_{bi}.

When V_a is applied, the device operates out of equilibrium and the external voltage applies directly to the junction potential. Due to a reverse bias ($V_a > 0$ V) and as shown in Fig. 2.3(b), the barrier and width of the depleted region increase, while Fig. 2.3(c) illustrates their decrease when a forward bias ($V_a < 0$ V) is given. The different profiles for the energy diagrams are

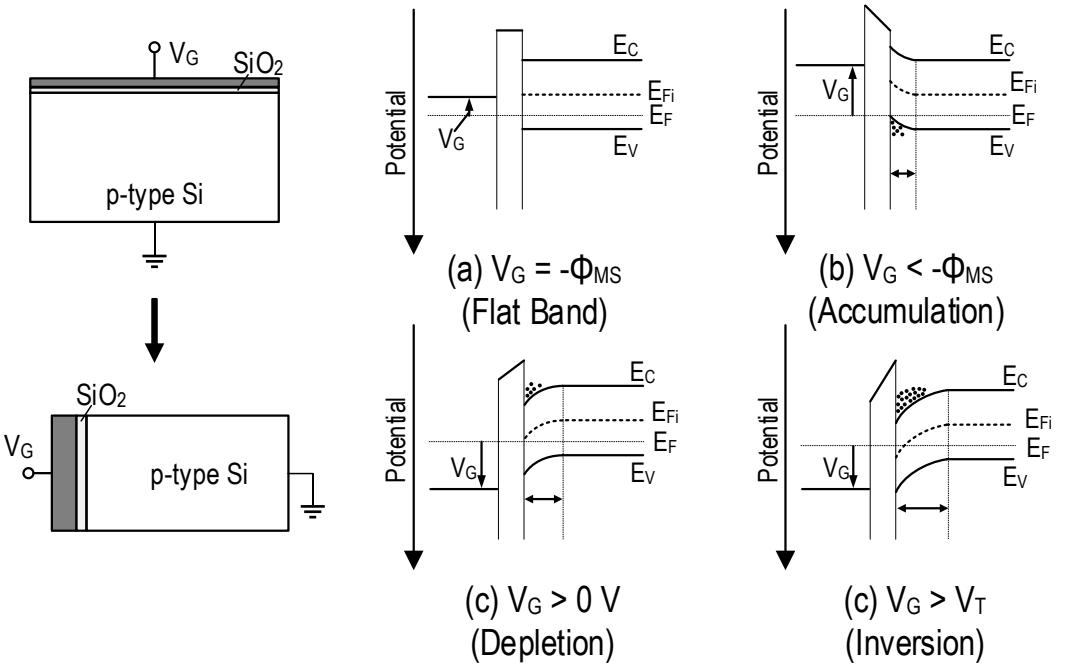


Figure 2.4: Cross-section of a MOS structure and its 2D equivalent representation. The gate electrode is on top of the silicon dioxide layer (SiO_2) and a p-type silicon structure. The potential distribution of the MOS structure is shown at various gate biases, V_G: for a flat-band condition in (a), for a negative V_G and a surface charge accumulation in (b), for a positive V_G and a shallow depletion in (c) and a surface inversion layer in (d).

responsible for a small reverse saturation current, I_0, and for a forward current, which depends exponentially on V_a [21]. Both currents are shown in the plot of the total current, I_{tot}, against V_a depicted in Fig. 2.3(d).

The structure of a conventional photodiode is the same as that of the pn-junction. The presence of a gate electrode attenuates the absorbed light intensity. When charges need to be generated by incident light, the reverse bias condition is particularly useful. A larger and fully-depleted region guarantees that charges can be generated without immediately recombining. Photogenerated electrons are forced to flow into the highly potential node where the operation of readout can be performed, while holes flow towards the substrate and are discharged.

MOS structure (Photogate)

The cross-sectional view of a MOS structure is shown in Fig. 2.4 with the gate electrode, silicon dioxide (SiO_2) and p-type silicon. Fig. 2.4(a) depicts the band diagram when the gate voltage, V_G, is equal to the difference between the gate metal and semiconductor workfunctions, $-\phi_{MS}$. The workfunction is defined as the minimum energy needed to extract an electron from a solid to the closest energy level in the vacuum and is equal to the difference between the vacuum level, E_0, and the Fermi-level, E_F [21]. The applied voltage determines the flat-band condition,

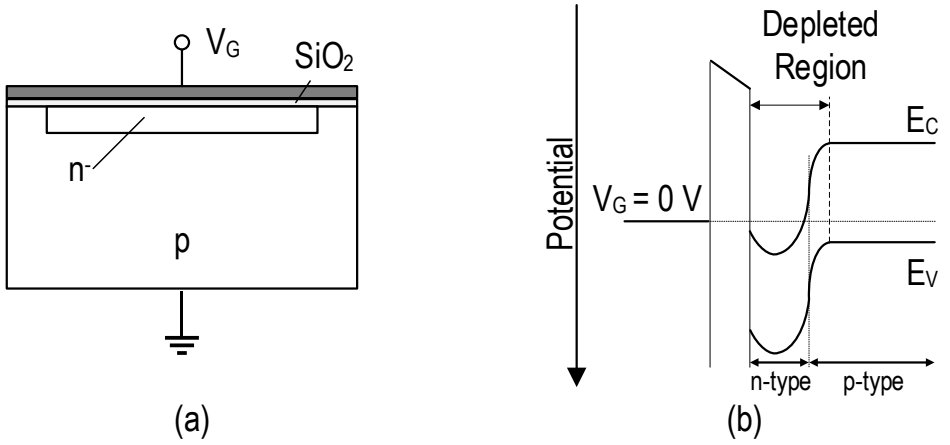


Figure 2.5: Cross-sectional view of buried MOS structure in (a) and potential distribution under full depletion in (b).

where there is no potential difference between the silicon and gate electrode and the charge distribution is equal to zero.

As shown in Fig. 2.4(b) for V_G more negative than $-\phi_{MS}$, the vertical shift in the energy diagram forces the majority carriers (the hole in a p-type semiconductor) to accumulate at the interface between the oxide and silicon (accumulation).

Fig. 2.4(c) and Fig. 2.4(d) depict the bending of the energy diagram when a positive value of V_G is applied. This leads first to a depletion at the interface with the oxide and then to an accumulation of the minority carriers (electrons in a p-type semiconductor) called inversion.

The photogate used in image sensors is a MOS structure, where the depletion layer due to a positive voltage applied to the gate is exploited. The maximum potential in the depletion region is located at the surface, where the electric field spatially separates the photogenerated pair consisting of one electron and one hole. As explained earlier for conventional photodiodes, the electrons are collected at the surface while holes move to the substrate. Even though a reduced sensitivity to blue light is observed due to higher absorptions for shorter wavelengths, a polysilicon gate is commonly used to allow light to pass through.

Buried MOS (Buried CCD)

The buried MOS structure is used in the buried channel CCDs (BCCDs) and in the buried MOSFETs. As shown in Fig. 2.5(a) and in contrast with the MOS structure, for a buried MOS structure an n-type layer is formed in the channel area under the gate electrode.

Under the hypothesis of thermal equilibrium, the inserted pn-junction at the silicon surface determines a built-in potential and a depletion layer between both sides of the junction. If electrons in the n-type layer are withdrawn by means of a high reset voltage, the n-type area

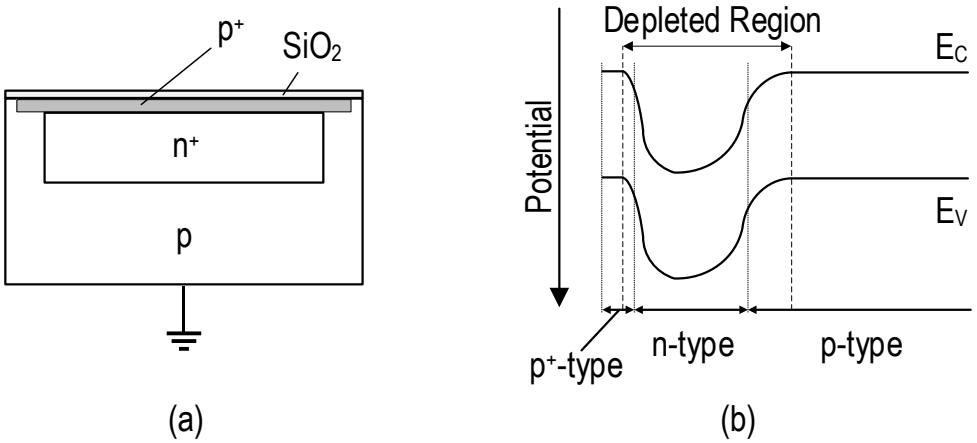


Figure 2.6: Cross-sectional view of a buried photodiode or PPD in (a) and potential distribution in (c) under depletion.

becomes fully depleted and only the positively-charged and spatially-fixed ionized donors remain.

As indicated in Fig. 2.5(b), the resulting potential profile becomes a convex downward quadratic curve. The position of the maximum potential is inside the silicon and separated from the silicon–oxide interface. Since the photogenerated electrons can flow without touching the interface, they avoid the influence of the state traps.

Pinned Photodiode

The PPD shown in Fig. 2.6(a) is used in most modern CISs for high image quality applications and its study is a central topic of this dissertation. The device is made of a buried n-well and a highly doped p^+ shallow layer, which implements a potential well for the photoelectrons to be stored [8, 2]. As shown in Fig. 2.6(b), the potential is in fact pinned in the depleted region as with a buried MOS structure.

The existence of a highly-doped p^+ layer at the interface substantially reduces the dark current generated by the electrons, which are thermally excited to the conduction band through the interface state with silicon oxide. The absorption of light and the integration of photogenerated charges are the same as in conventional photodiodes.

2.2 Pixel Architectures

The electronic devices shown in the previous section are the photodetecting elements that are integrated in image sensor and represent the core element of every pixel of the array. In this section, a brief description of the main pixel architectures is given, from the ones including conventional photodiodes to that based on PPDs.

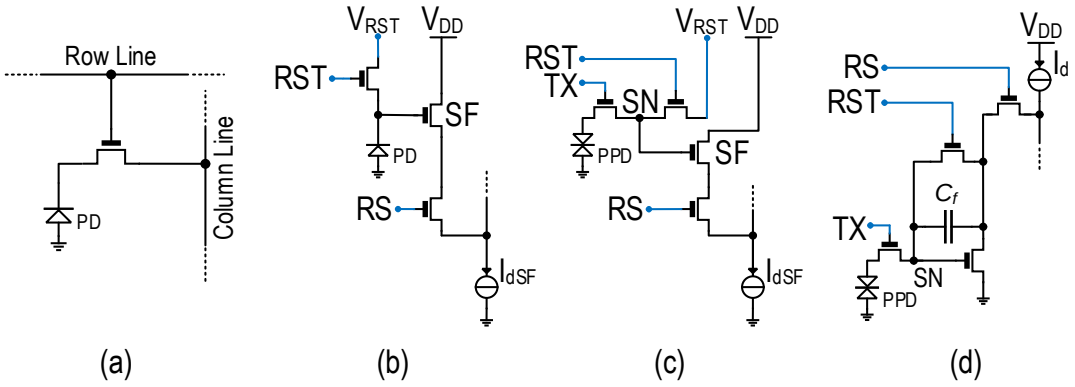


Figure 2.7: Four pixel schematics: 1T PPS in (a), 3T in (b), 4T APS in (c) and 4T CTIA in (d).

2.2.1 PPS - 1T

The passive pixel sensor (PPS) is shown in Fig. 2.7(a) and integrates one transistor (1T) to connect the photo-detecting surface diode to the bit line [12, 8, 9]. This pixel replaced the CCD photosensitive element used to sense the light in the CCD camera scheme. The basic structure of the CCDs was based on vertical and horizontal shift registers [11], that are replaced by metal lines in a PPS-based architecture. While the single in-pixel transistor is used as a selector, two additional transistors for each column are used to reset the photodiode and to select the specific column. An output SF-based amplifier is used to convert the charge in the output voltage [11].

2.2.2 APS - 3T

As shown in Fig. 2.7(b), a SF and a reset transistor (RST) are added to the pixel leading to an active pixel sensor (APS). This pixel was introduced to improve the performance which were limited by the output SF amplifier. When the charge-to-voltage conversion is implemented with a SF, both the conversion and reset noise (kTC) are optimized by minimizing the input capacitor to this stage, C_{in}. For a given amount of charge, ΔN, the change in voltage output is in fact given by $\Delta V_{\text{out}} = (q\Delta N)/C_{in}$ and the charge noise variance by $\sigma^2[Q_{\text{in}}] = (kTC_{in})/q^2$, where Q_{in} is the charge stored on C_{in}. In a CIS based on a PPS, the long metal connections add a large capacitive component limiting the sensor performance to values that are not acceptable in most applications.

The solution to this problem is to introduce a SF inside each pixel in order to separate the conversion capacitance from the column, at the cost of an increased complexity and reduced pixel photosensitive area (fill factor). Once the floating diffusion node is isolated from the bit line capacitance, it can be reduced to much smaller values, increasing the overall pixel gain. Even though this technique was introduced in late 1960s [3, 4], it became practical in the early 1990s because of CMOS process scaling [16].

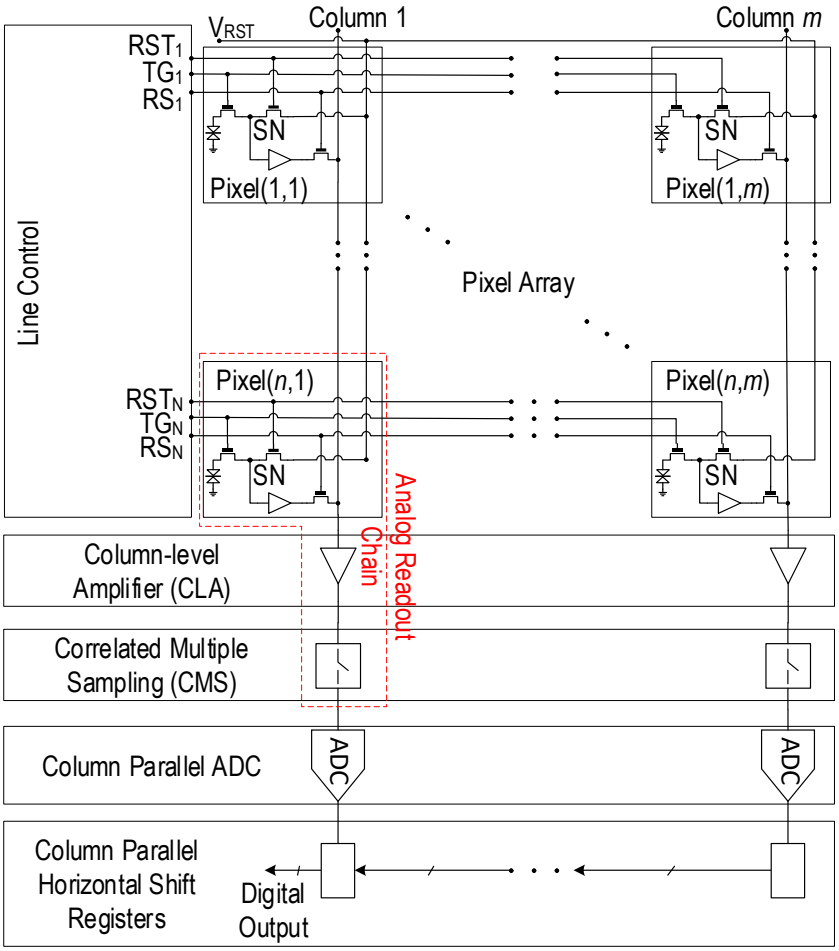
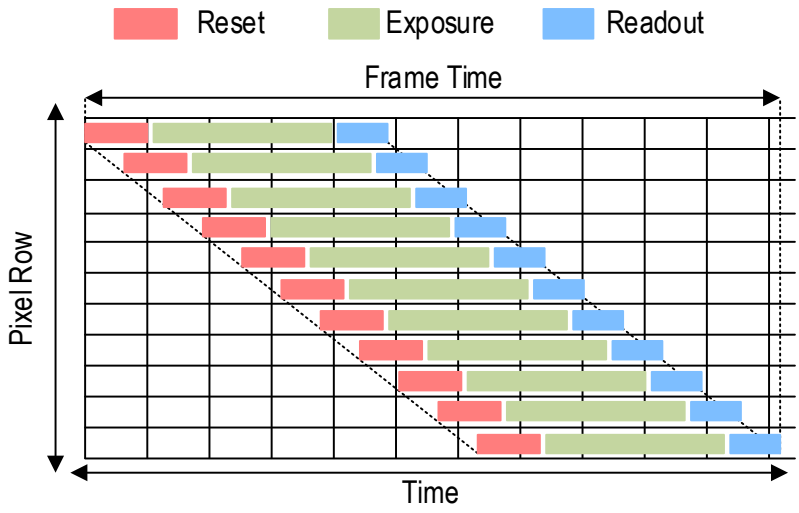


Figure 2.8: Block diagram of a conventional low noise CIS composed of an array of 4T pixels. The Line Control enables the control signals for the pixel array according to the readout scheme. At column-level, the CLA, CDS and ADC blocks are generally implemented.

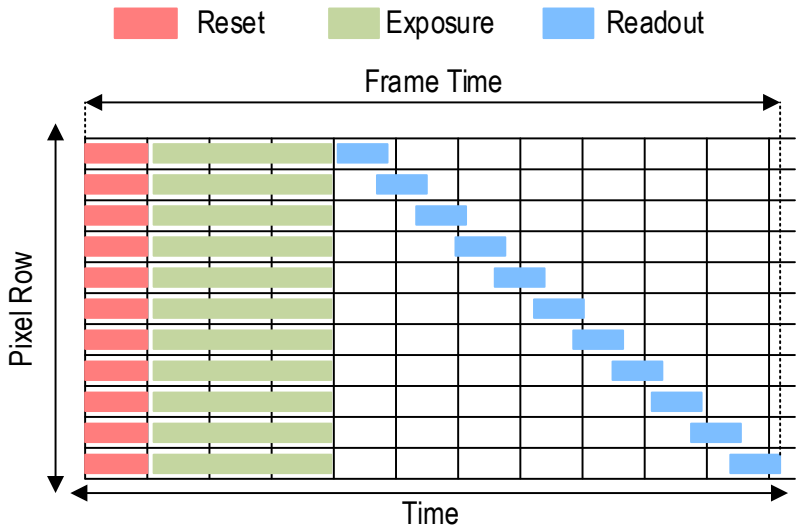
2.2.3 PPD/TG - 4T

In the four transistors (4T) APS shown in Fig. 2.7(c), the photodiode and conversion capacitances are separated. The pixel embeds a PPD as photodetector and a TG to move the charge from the PPD to the SN. The voltage change at the input of SF, ΔV_{SN}, is in this case equal to $(q\Delta N)/C_{SN}$, where C_{SN} is the SN capacitance of the pixel. If $C_{SN} = 1\,\text{fF}$ then each electron will cause a 160 µV change at the input of the SF and, if a voltage swing at the SF input equal to 1 V is assumed, it is obtained a maximum SN FWC of 6250 electrons and a dynamic range (DR) of 75.9 dB.

As shown in Fig. 2.7(d), an increased gain at pixel level can be also introduced with a capacitive trans-impedance amplifier (CTIA) [15, 22]. In this circuit, assuming the transistor's voltage gain is much greater than the ratio of C_{SN}/C_f, the feedback capacitance C_f controls the gain and output voltage of the amplifier, given by $q\Delta N/C_f$.



(a)



(b)

Figure 2.9: Rolling shutter readout mode in (a) with shifted reset, exposures and readout for each line. Global shutter mode in (b) with equal start and stop of the exposure for all lines.

2.3 Ultra-Low Noise CIS Architectures

2.3.1 Basic Block Diagram

In a top-down approach, an overview of a low noise CIS is formulated in this section. Fig. 2.8 shows the block diagram of a conventional low noise CIS. At the center of the diagram, the pixel array contains all pixels in a number of n rows and m columns. Each one is made up of a PPD together with four transistors: the TG, the RST, the row select (RS) and the in-pixel amplifier.

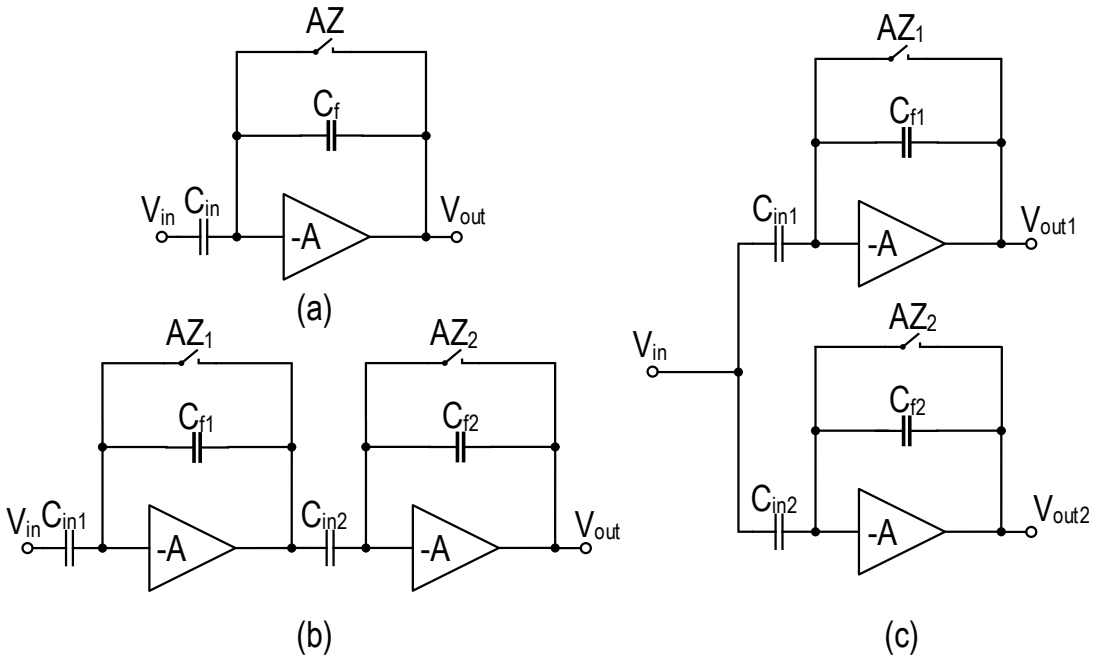


Figure 2.10: Column amplifier architectures described in [18]: single-stage capacitive amplifier in (a), two-stage capacitive amplifier in (b) and dual single-stage capacitive amplifier in (c).

The Line Control block in Fig. 2.8 controls each row and enables the signals according to the array readout scheme. At the bottom of each column, a column-level amplifier (CLA) is generally implemented before the CDS and analog-to-digital converter (ADC).

The readout schemes define the different timing diagrams used to control the array and therefore determine how an image is built from individual information stored in each line and pixel. In order to speed up the readout operation, a column parallel readout scheme is usually performed.

As shown in Fig. 2.9(a) for a rolling shutter, the readout operation is performed line by line and the frame time corresponds to that required to read each one. In order to obtain the same integration time, the reset pulses of each line are time-shifted, resulting in a different starting time of light integration for each line. In this scheme, a line integrates light, while two others either start the readout operation or already finish their exposure. This is not an issue when static objects are captured, but when fast movements compared to the row readout time are captured, a strong distortion of the obtained image is unavoidable.

To avoid the distortion with moving objects, it is necessary to take a "snapshot" with the beginning and end of the integration phase equal for all lines. This readout mode is called global shutter and is depicted in Fig. 2.9(b). It consists of a shared phase of reset (global reset), followed by the exposure and readout as performed in rolling shutter sensors.

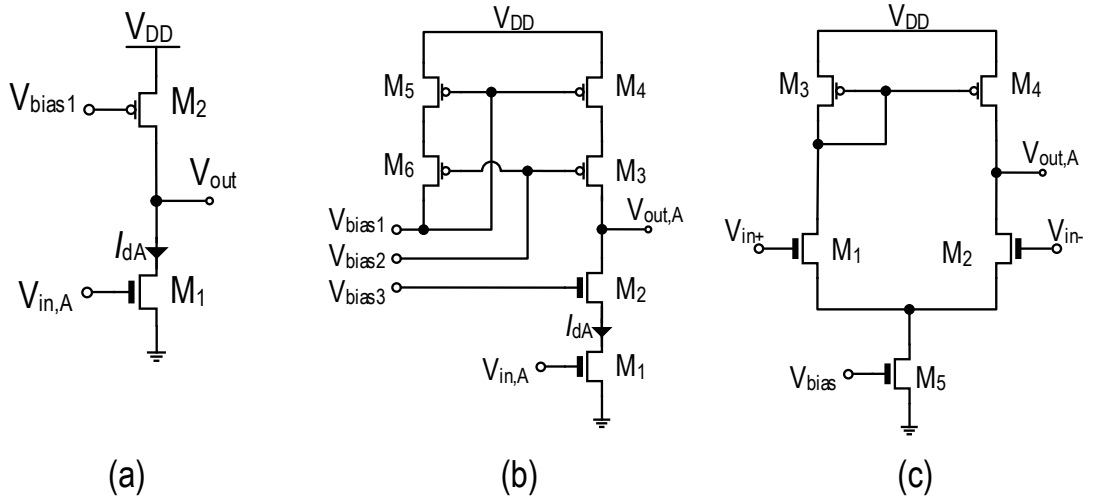


Figure 2.11: Column amplifier circuits described in [18]: single-ended MOS amplifier architectures in (a) and (b), differential MOS amplifier in (c).

2.3.2 Column-level Amplifier Architectures

Since the early 1990s, CLAs have been used to improve CIS performance and, when they achieved a small noise contribution of a few e^-_{rms}, became practically essential in ultra-low noise CIS [13]. The CLA limits the signal and noise bandwidth at the high end by low-pass filtering and decreases the impact of the following blocks on the input-referred noise. The filtering-induced noise reduction needs to be balanced with the circuit complexity, leading in most designs to a single pole low-pass filter CLA. In order to minimize the thermal noise contribution, the bandwidth of the CLA is usually set between 2 and 10 times the row readout rate. Since a too-low value will prevent the amplifier from settling during the sampling period and an overly-high one will not optimize the noise performance, the bandwidth of the CLA is often adjusted by the correct sizing of an output load capacitor, C_L. Even though a high value for the CLA gain is desirable, the signal amplification is always distributed between the pixel and amplifier in order to balance with other design requirements such as read noise, dark current, fill factor, quantum efficiency (QE), FWC, die size, and cost. Even though many different CLA architectures are possible, the typical design constraints in an image sensor limits the choice to a few commonly-used options. Three main CLA architectures are described in [18] and shown in Fig. 2.10: the first is a single-stage capacitive amplifier, the second a two-stage and the third a pair of single-stages [10].

The single-stage CLA in Fig. 2.10(a) is composed of a MOS amplifier, two capacitors and a reset switch across the feedback capacitor, C_f. Due to the use of the few active components, it achieves the lowest noise performance and is therefore the most commonly used architecture in CIS. The limited gain-bandwidth and higher power dissipation compared to a two-stage amplifier are the main limitations of this solution.

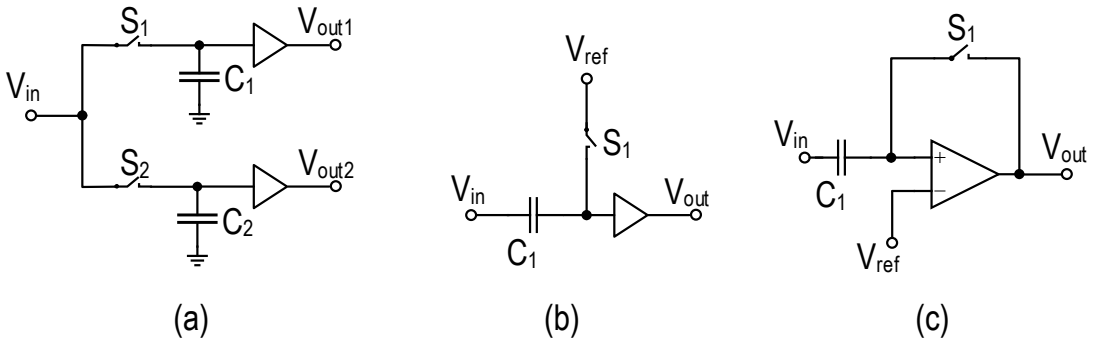


Figure 2.12: Three different implementations for the CDS circuit described in [18]: the differential Track and Hold CDS in (a), the single-ended CDS with a voltage buffer in (b) and the single-ended CDS with transconductance amplifier in (c).

The capacitive CLA in Fig. 2.10(b) is the cascade of two single-stage capacitive amplifiers with lower voltage gain. When required by the design specifications, such a solution is used in order to achieve a higher gain and/or bandwidth compared to a single-stage amplifier. The lowest power dissipation for a given bandwidth is usually achieved by this architecture, at the cost of a higher silicon area. Its noise performance can be optimized to be similar to the single-stage architecture.

When both high and low gain values for the CLA are required simultaneously, a pair of single-stage CLAs operating in parallel is used, as shown in Fig. 2.10(c). Since one amplifier is set to have a high-gain and the other a low, this solution maximizes the sensor DR. The high-gain amplifier is used to reduce noise, while the low-gain allows the effective sensor FWC to be maximized. The main disadvantage of this solution is the required power consumption, which is almost twice as high as the single stage CLA.

The circuit schematics for the commonly used MOS amplifiers in CLAs are detailed in [18] and shown in Fig. 2.11 with two single-ended solutions and one differential one. The simple two transistor amplifier in Fig. 2.11(a) has the lowest gain but the largest output swing, while the opposite applies to the fully cascode amplifier in Fig. 2.11(b). The differential in Fig. 2.11(c) has the same performance as the single-ended amplifiers, but a better power supply rejection and the possibility to be operated either in inverting or non-inverting mode. For the same available silicon area and/or power budget, single-ended amplifiers can achieve lower noise and larger swing than differential amplifiers.

2.3.3 Correlated Sampler Circuits

Overview of CDS circuits

In order to minimize noise, the control of the readout chain bandwidth is combined with signal amplification in ultra-low noise CIS. A low-end limitation of the signal bandwidth is

given by the CDS circuit. This operation differentiates between a reset and a signal voltage sample, respectively taken after resetting the SN and transferring the photogenerated charge to the SN. The output difference removes both the SN and CLA reset kTC noise and high-pass filters the 1/f and RTS noise that affect the signal, while increasing the thermal noise power by a factor of two [7].

Fig. 2.12 illustrates the three typical CDS circuits described in [18]. A differential track and hold (T&H) circuit is shown in Fig. 2.12(a), where the output of the CLA is tracked when switches S_1 and S_2 are closed, and sampled on a capacitor when a switch opens. After sampling, the difference between the two voltages, V_{out1} and V_{out2}, is the CDS signal. The CDS circuit in Fig. 2.12(b) samples the reset level of the CLA when S_1 is opened and then subtracts this value from the signal when the same switch is closed, in a single-ended buffered output. The CDS circuit in Fig. 2.12(c) operates similarly to the previous one, but replaces the voltage buffer with an auto-zero operational transconductance amplifier (OTA), often used as the first stage of a comparator in a column-level ADC and to cancel the additional offset voltages and low noise fluctuations.

Overview of CMS circuits

When compared to a simple CDS, the CMS consists in averaging M samples after the reset and M samples after the transfer with a sampling period, T_{CMS}, and then calculating the difference between the two averages. This technique is used in ultra-low noise CIS to reduce thermal noise by averaging multiple samples and reduce slightly further the residual 1/f noise. Different implementations of CMS are reported in the literature, including analog and digital techniques [19, 6].

The schematic of a typical analog implementation of CMS is shown in Fig. 2.13(a) with the two main blocks (the analog multiple sampler and CDS) and corresponding timing diagram in Fig. 2.13(b). An active switched-capacitor integrator cumulates on the feedback capacitor, C_{f}, the sum of M consecutive values of the input voltage, V_{col}, sampled on the input capacitor, C_{in} [19]. The CDS block is used to store the values of the cumulated reset and the signal levels and implement the final difference. As shown in the timing diagram, when the S_1 switches are opened V_{col} is sampled M times at the capacitor C_{in} after the reset of the SN and the auto-zeroing of the amplifier. The S_2 switches are used instead to transfer the sampled charge from C_{in} to C_{f}. After M iterations, the output voltage of the integrator. V_{sc}, is equal to the sum of M consecutive samples of the reset-level. The switch S_{SR} is opened at the end of the reset sampling in order to hold the final value of V_{sc} on C_1. The samples of the signal-level are similarly taken after the photogenerated charges are transferred from the PPD to the SN. The switch S_{SS} is then opened to hold the final value of V_{sc} on C_2 for the signal-level. The difference between the values stored on C_1 and C_2 is the final output of the CMS circuit. The main drawback of this implementation is the reduction in DR by a factor M. An alternative solution involves the introduction of a folding integration scheme with digitally assisted feedback to prevent the integrator from saturating [19]. This solution is obtained at the cost of additional

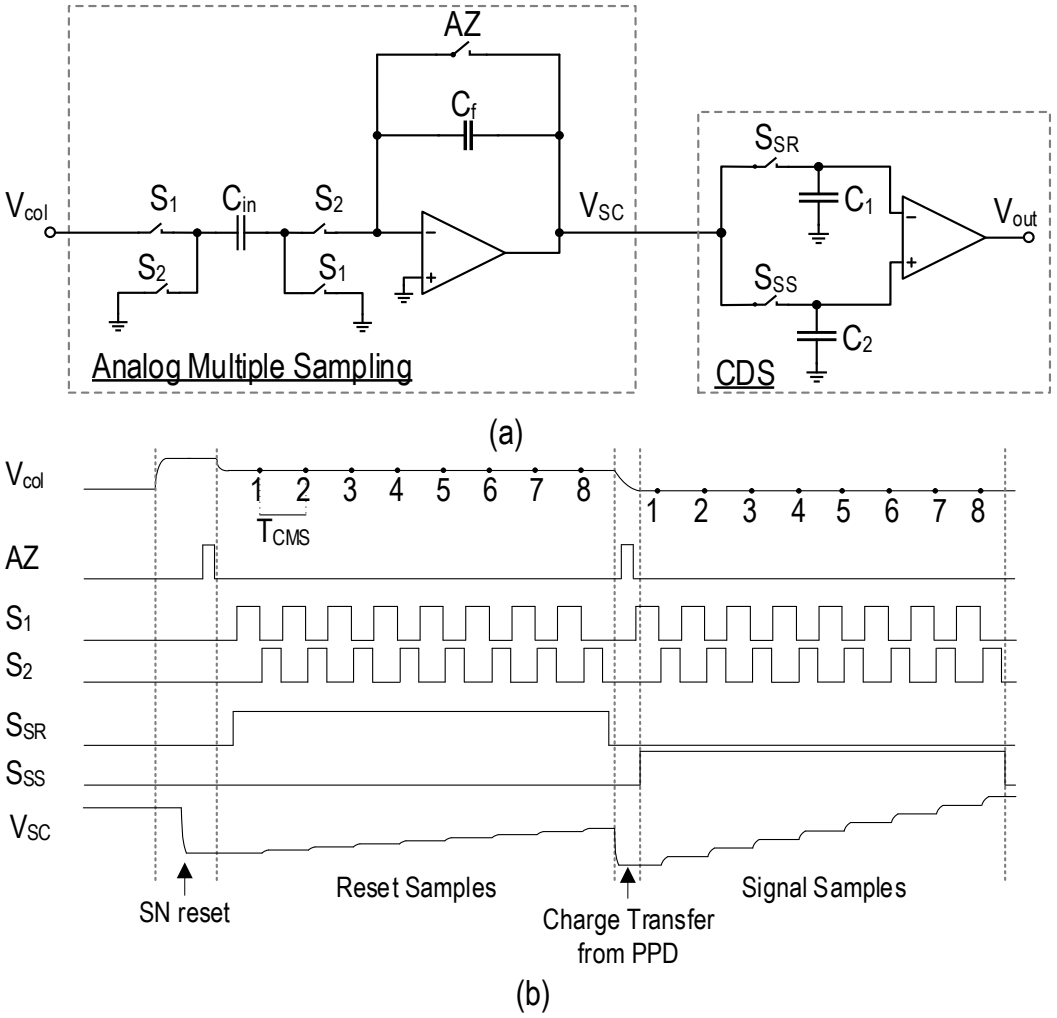


Figure 2.13: Analog implementation in (a) of CMS using a switched-capacitor integrator. Timing diagram in (b) of the control signals and voltages at the main internal nodes, during the reset and after the charge transfer from the PPD.

circuitry and complexity.

Fig. 2.14(a) shows the typical digital implementation of CMS [6, 14, 5]. A multiple-ramp single-slope (SS) ADC is used to sample the input voltage, V_{in}, usually connected to the CLA output and perform multiple analog-to-digital conversions. The SS-ADC consists of a comparator, driven by a ramp voltage and a bit-wise inversion (BWI) counter. The analog-to-digital conversion is performed by the BWI cell counting the number of clock cycles until the comparator output changes. The corresponding timing diagram of the main signals is shown in Fig. 2.14(b). The SN and comparator are reset, while the CLA is auto-zeroed. Given enough time to settle, V_{in} is equal to the reset-level and can be compared with a ramp voltage, V_{ramp}, while the BWI counter counts up synchronously. When V_{ramp} is equal to the other input of the comparator, V_{c}, it toggles from high to low and the counter stops. The digital output

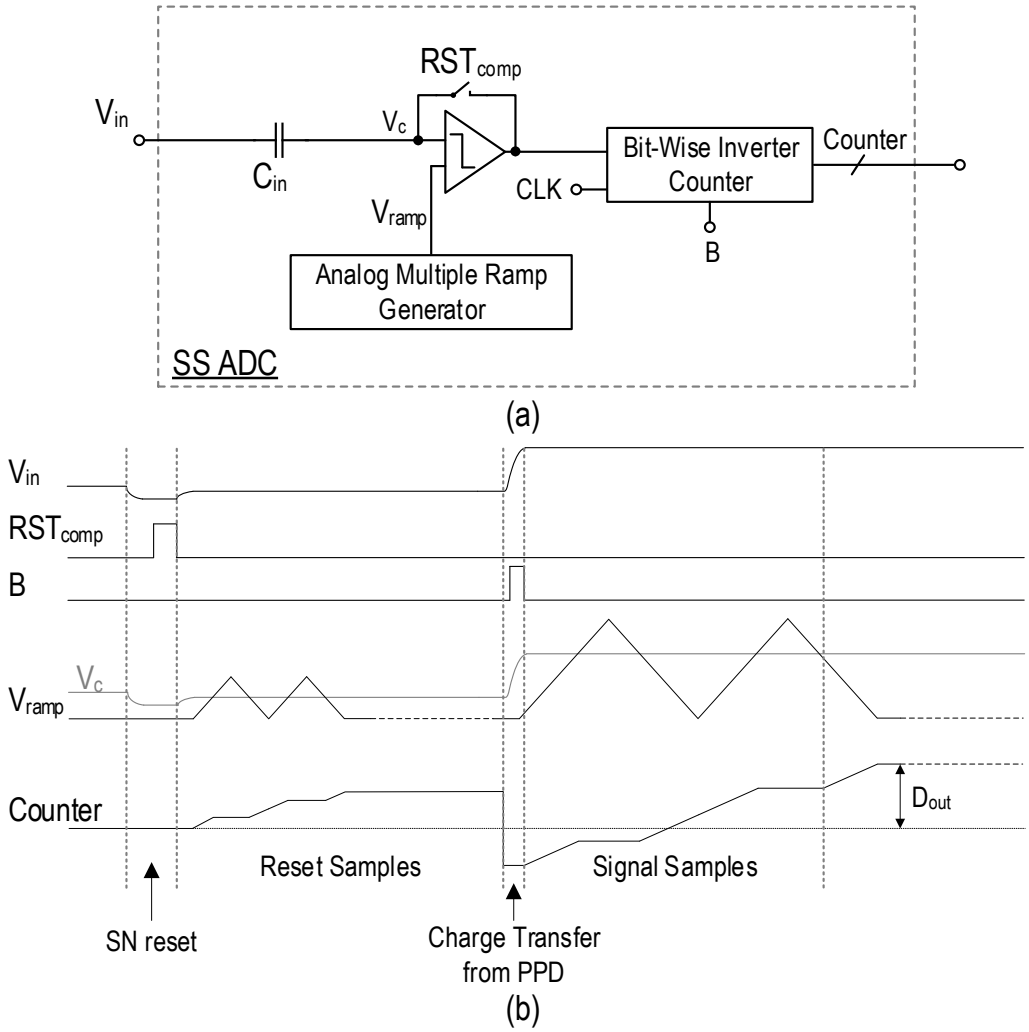


Figure 2.14: Digital implementation in (a) of CMS using a multiple-ramp single-slope ADC. Timing diagram in (b) of the control and main node signals during the reset and after the charge transfer from the PPD.

of the counter is now equivalent to the input reset-level. By ramping V_{ramp} up and down a number of times equal to M with the counter still increasing, M samples of the reset-level are cumulated. The charge is then transferred from the PPD to the SN and V_{c} increases to the amplified signal-level. The inversion, B, is now activated in order to 1's complement all the output bits and store the negative digital value corresponding to M -times the reset-level. Starting from this negative digital value, the counter once again begins counting for M samples of the pixel signal-level. The difference between the two final conversions of the reset and signal samples and the averaging are finally implemented in the digital domain. A digital implementation of CMS requires multiple analog-to-digital conversions, which translates into faster ADC and higher power consumption.

2.4 Summary

Designing modern CIS requires detailed knowledge of semiconductor devices, CMOS circuits and system architectures, with additional experience in the field of physics of light and properties of solid-state materials. This chapter aimed to present a brief summary of notions that are fundamental to later sections.

The first part of the chapter describes silicon-based photodetectors and defines the main optical properties of silicon for CIS. The semiconductor devices used in imaging are briefly described: the *pn*-junction for conventional photodiodes, MOS structure for photogates, buried MOS in BCCD and PPD for modern CISs.

In the second part, various pixel architectures are explained and the main reasons for their development are indicated, following the historical evolution of pixel designs from the 1T pixel, to 3T and 4T.

In the last part of the chapter, the ultra-low noise CIS is described at system-level, with a focus on the main building blocks and readout schemes. Each block is then reviewed by analyzing and pointing out the advantages and limitations of different implementations commonly reported in the literature.

References for Chapter 2

[1] Max Born and Emil Wolf. *Principles of Optics: Electromagnetic Theory of Propagation, Interference and Diffraction of Light (7th Edition)*. Cambridge University Press, 1999.

[2] R. Capoccia, A. Boukhayma, F. Jazaeri, and C. Enz. Compact Modeling of Charge Transfer in Pinned Photodiodes for CMOS Image Sensors. *IEEE Transactions on Electron Devices*, pages 1–9, 2018.

[3] S. G. Chamberlain. Photosensitivity and scanning of silicon image detector arrays. *IEEE Journal of Solid-State Circuits*, 4(6):333–342, 1969.

[4] S. G. Chamberlain and V. K. Aggarwal. Photosensitivity and characterization of a solid-state integrating photodetector. *IEEE Journal of Solid-State Circuits*, 7(2):202–204, 1972.

[5] N. Chen, S. Zhong, M. Zou, J. Zhang, Z. Ji, and L. Yao. A Low-Noise CMOS Image Sensor With Digital Correlated Multiple Sampling. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 65(1):84–94, Jan 2018.

[6] Y. Chen, Y. Xu, Y. Chae, A. Mierop, X. Wang, and A. Theuwissen. A $0.7e^-_{rms}$ temporal readout-noise CMOS image sensor for low-light-level imaging. *2012 IEEE International Solid-State Circuits Conference (ISSCC)*, pages 384–386, Feb 2012.

[7] C. Enz and G. Temes. Circuit techniques for reducing the effects of op-amp imperfections:

autozeroing, correlated double sampling and chopper stabilization. *Proceedings of the IEEE*, 84(11):1584–1614, 1996.

[8] E. R. Fossum and D. B. Hondongwa. A Review of the Pinned Photodiode for CCD and CMOS Image Sensors. *IEEE Journal of the Electron Devices Society*, 2(3):33–43, 2014.

[9] Eric R. Fossum. Active pixel sensors: are CCDs dinosaurs? In *Charge-Coupled Devices and Solid State Optical Sensors III*, volume 1900, pages 2–14. International Society for Optics and Photonics, July 1993.

[10] B. Fowler, X. Liu, S.Mims, J. Balicki, W. Li, H. Do, and P. Vu. Wide dynamic range low light level CMOS image sensor. In *Proceedings of 2009 Internation Image Sensor Workshop*, June 2009.

[11] J.R. Janesick. *Scientific Charge-Coupled Devices*. SPIE Press, 2001.

[12] L. J. Kozlowski, J. Luo, W. E. Kleinhans, and T. Liu. Comparison of passive and active pixel schemes for CMOS visible imagers. In *Infrared Readout Electronics IV*, volume 3360, pages 101–110. International Society for Optics and Photonics, September 1998.

[13] Alex Krymski, Nail Khaliullin, and Howard Rhodes. A 2 e- Noise 1.3Megapixel CMOS sensor. In *Proceedings of 2003 IEEE Workshop on CCDs and AIS*, May 2003.

[14] Y. Lim, K. Koh, K. Kim, H. Yang, J. Kim, Y. Jeong, S. Lee, H. Lee, S. Lim, Y. Han, J. Kim, J. Yun, S. Ham, and Y. Lee. A 1.1e- temporal noise 1/3.2-inch 8Mpixel CMOS image sensor using pseudo-multiple sampling. *2010 IEEE International Solid-State Circuits Conference (ISSCC)*, pages 396–397, Feb 2010.

[15] C. Lotto, P. Seitz, and T. Baechler. A sub-electron readout noise CMOS image sensor with pixel-level open-loop voltage amplification. In *2011 IEEE International Solid-State Circuits Conference*, pages 402–404, Feb 2011.

[16] Sunetra K. Mendis, Sabrina E. Kemeny, Russell C. Gee, Bedabrata Pain, Quiesup Kim, and Eric R. Fossum. Progress in CMOS active pixel image sensors. In Morley M. Blouke, editor, *Charge-Coupled Devices and Solid State Optical Sensors IV*, volume 2172, pages 19 – 29. International Society for Optics and Photonics, SPIE, 1994.

[17] F. Pedrotti and L. Pedrotti. *Introduction to Optics, 3rd edition*. Prentice-Hall International, Inc., 2017.

[18] P. Seitz and A. Theuwiseen. *Single-Photon Imaging*. Springer Series in Optical Sciences, 2011.

[19] Sungho Suh, Shinya Itoh, Satoshi Aoyama, and Shoji Kawahito. Column-Parallel Correlated Multiple Sampling Circuits for CMOS Image Sensors and Their Noise Reduction Effects. *Sensors*, 10(10):9139–9154, 2010.

[20] S.M. Sze and M.K. Lee. *Semiconductor Devices: Physics and Technology, 3rd Edition*. Wiley, 2012.

[21] S.M. Sze and K.K. Ng. *Physics of Semiconductor Devices*. Wiley, 2006.

[22] Jungwook Yang, K. G. Fife, L. Brooks, C. G. Sodini, A. Betts, P. Mudunuru, and Hae-Seung Lee. A 3Mpixel Low-Noise Flexible Architecture CMOS Image Sensor. In *2006 IEEE International Solid State Circuits Conference - Digest of Technical Papers*, pages 2004–2013, Feb 2006.

3 Compact Modeling of Charge Transfer in PPDs for Low Light CIS

Different CIS designs in the literature report sub-electron read noise levels and frame rates in the order of hundreds of thousands of frames per second (fps) [1, 2]. The non-ideal effects influencing the charge transfer mechanism from the PPD to the SN are among the main limitations to further improve the sensor performances. This acts as a motivation to look more deeply into device-level phenomena and develop a physics-based compact model for the PPD together with the TG.

In this chapter, the core of a compact model of the PPD device and the TG is proposed based on analytical expressions derived from equivalent two-dimensional (2-D) structures. After introducing the PPD device structure and its typical principle of operation, the analytical derivation starts with an electrostatic analysis of the PPD structure, where the main electrical parameters are defined. When the TG is added, a second electrostatic analysis is carried out and the potential barrier between the PPD and the TG expressed as a function of the PPD and TG voltages and other physical parameters. The concept of modulation of the potential barrier by the TG voltage is highlighted and verified by Synopsys® TCAD [3] simulation results. The expression of the potential barrier at the interface is used to derive an expression of the charge transfer current, which is then used to evaluate the amount of transferred charges at each transfer. An experimental validation methodology that relies on the amount of transferred charges is proposed in order to verify the model under different values for the light illumination, the TG voltage and the transfer time.

The derived expressions reasonably match with the simulation and measurement results, and are fundamental to understanding the main design trade-offs with respect to the process, electrical and geometrical parameters. Ultimately, the goal of this compact model is to be a tool for CIS designers to simulate, design and optimize PPD-based pixels.

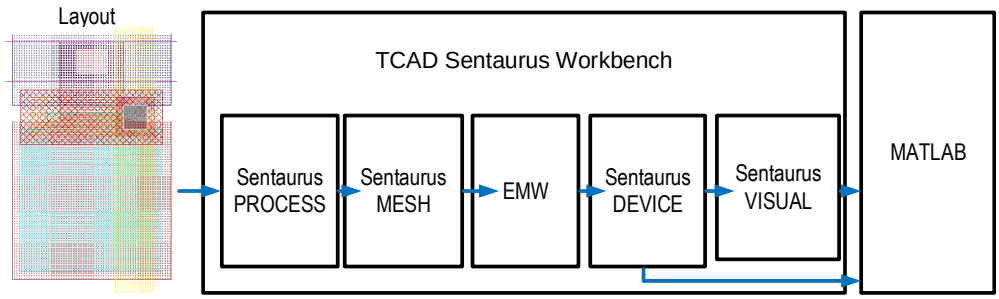


Figure 3.1: The suite of tools composing the TCAD Sentaurus Workbench are shown in the order of execution, from the process simulation to the output data visualization.

3.1 Device Simulation

In order to verify the analytical expressions derived during the model development, software simulations are required. As shown in Fig. 3.1, Synopsys® TCAD Sentaurus is used, comprising a suite of different tools that allows computer simulations of semiconductor devices, from the fabrication steps to the opto-electrical characterization.

In order to simulate the fabrication process used for making PPD devices [4], Sentaurus Process combines a set of models to create a realistic device structure and Sentaurus Mesh adds an optimized grids of points for device simulation. The optical simulation is performed by the Electromagnetic Wave Solver (EMW), a finite-difference time-domain solver, which calculates the optical field and optical generation rate in the device, accounting for the properties of the incident light. Sentaurus Device calculates the electrical device response based on a set of carrier transport models and on the results from EMW, while Sentaurus Visual is used together with Matlab in order to visualize and process the simulation results [3].

The developed model aims to explain the charge transfer in a generic PPD-TG structure, hence the simulated device is not calibrated towards a specific process. A general purpose flow is used, while static and transient simulations from a three-dimensional structure validate the derived analytical expressions.

3.2 Pinned Photodiode – Electrostatic Analysis

As mentioned in the previous chapter, a PPD is a device made by a n-well buried in a p-substrate and, on top of this well, a thin layer of highly p-doped semiconductor takes place. Even though the structure does not differ greatly from a standard pn photodiode, the working principle is quite different. A PPD operates as a unipolar charge accumulator, where the photogenerated electrons, N_{PPD}, can be stored. Lowering the energy barrier (below the energy at the PPD well), by imposing a positive voltage to the TG next to the PPD, allows the accumulated charge to be moved towards the SN. This node is initially set to a positive reset voltage, e.g. 2.5 V. As explained for the 4T pixel, the TG isolates the PPD and SN capacitances,

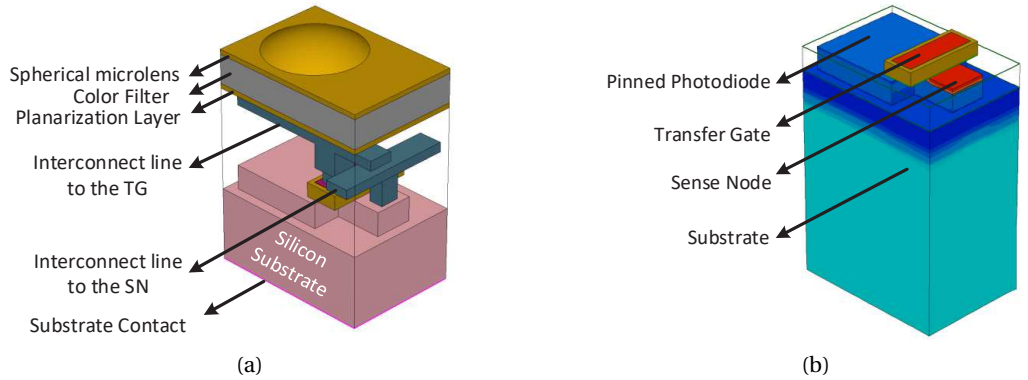


Figure 3.2: Pixel back-end in (a): the microlens, the color filter and the interconnections. Pixel front-end in (b): the pinned photodiode, the TG and the SN.

leading to a lower capacitance at the SN. Due to the fact that the SN capacitance, C_{SN} , is lower than the PPD capacitance, C_{PPD} , the transferred electrons cause a higher voltage variation that can be processed by the readout circuitry $\left[\Delta V_{\mathrm{SN}} = \left(q \cdot N_{PPD}\right) / C_{\mathrm{SN}}\right]$.

The 3D geometry of the back-end is depicted in Fig. 3.2(a), including the silicon at the bottom, the two metal interconnects, connected through a via to the TG and the SN contacts. As illustrated, a color filter is sandwiched between a layer of deposition on the bottom and a spherical microlens on the top. The color filter is chosen according to the wavelength used for the input light. In the simulations shown in this chapter, an ideal red color filter is used centered at a wavelength equal to 650 nm. Fig. 3.2(b) is a 3D view of the front-end of the device, including the photodiode, the TG made in polysilicon and surrounded by an insulating material, and the SN diffusion. Blue, red and light blue correspond to the p^+ type, n^+ type regions and p substrate, respectively.

At the top of Fig. 3.3, the simplified cross-section of a PPD is shown, made by a p^+np structure. The electrostatic potentials of the PPD are also shown under different conditions. Fig. 3.3(a) corresponds to the equilibrium condition, while the impact of charge transfer is sketched in Fig. 3.3(b) and that of light in Fig. 3.3(c). At the equilibrium condition, the n-well region is partially neutral and the electrostatic potential remains almost constant. The two built-in potentials, V_{bi1} and V_{bi2} , are illustrated in Fig. 3.3(a). The doping concentration in the p^+ layer is typically higher than in the p substrate. Hence, the built-in potential of the pn junction, V_{bi2} , is lower than that with the p^+ layer, V_{bi1} . After the free carriers are transferred from the PPD, the maximum value of the electrostatic potential increases and allows the n-well to be almost completely emptied of carriers. In Fig. 3.3(b), V_{pin} is retrieved as the maximum variation of the PPD electrostatic potential, in consistency with the definition given in [5]. On the other hand, when the photodiode is exposed to light, the entire electrostatic potential moves towards the flat-band condition as shown in Fig. 3.3(c).

In this chapter, the electrostatic analysis of the PPD is performed for the structure depicted

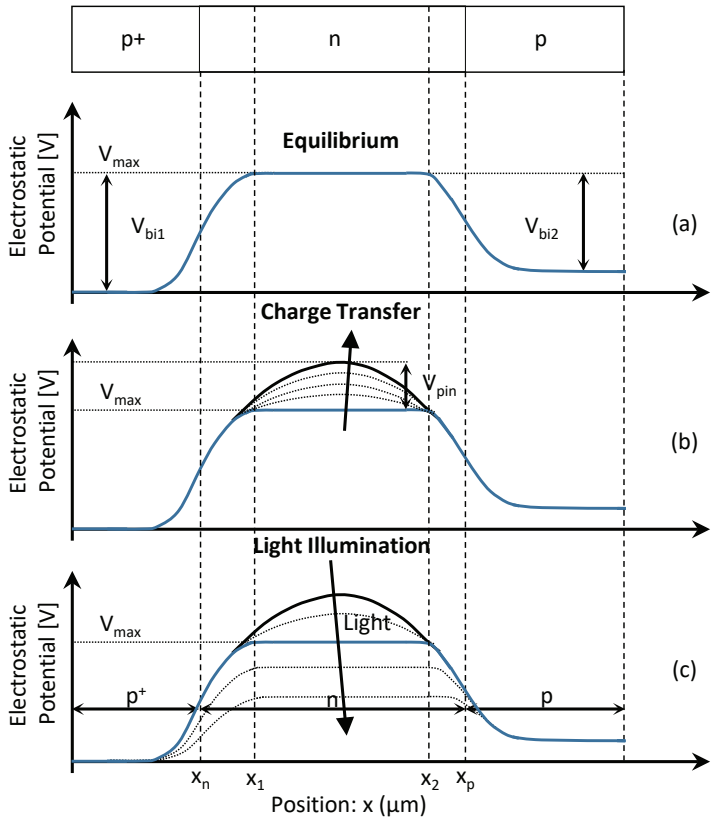


Figure 3.3: Sketches of the electrostatic potential of the PPD: (a) at equilibrium condition, showing two built-in potentials, V_{bi1} and V_{bi2}, and maximum potential, V_{max}; (b) the maximum value of the electrostatic potential increases until the empty condition is reached while transferring the charges from the PPD to the SN. The maximum variation of the electrostatic potential is the pinning voltage, V_{pin}, as defined in [5]; (c) the potential moves towards the flat-band condition due to the applied illumination.

in Fig. 3.4, characterized by a fully depleted n-well. The full-depletion of the n-well can be achieved as soon as all the accumulated charges are transferred to the SN during the reading operation. Since a full-depletion approximation is assumed along the device, the free carrier concentrations are negligible compared to the fixed charge density. In TCAD simulations the full-depletion is reached by a proper choice of the physical parameters, hence the two depleted regions intersects in one point. This is a particular case where the maximum of the electrostatic potential, V_{max} , is equal to the highest built-in potential, namely that p^+n junction, V_{bi1} . If the length of the n-well is further reduced, the structure is still pinned, but V_{max} is lower than V_{bi1} .

In the simplified cross-section of a PPD illustrated in Fig. 3.4, the left side corresponds to the top of the structure shown in Fig. 3.2(c). To simplify the analysis, the following assumptions are added: a) an abrupt transition between the neutral and the depleted region is used for both junctions; b) both the applied voltages in the substrate and at the pinned layer are set to

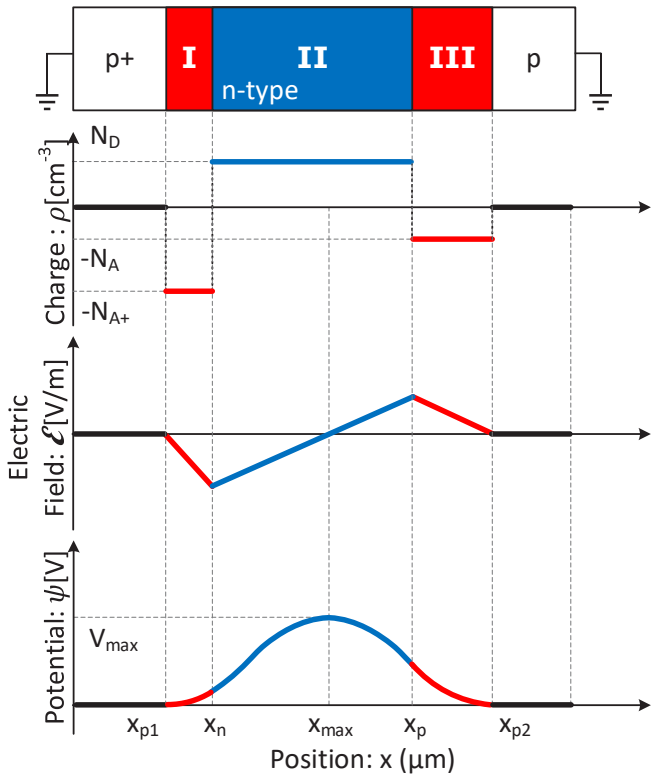


Figure 3.4: Simplified cross-section of a PPD under the assumptions of full depletion and abrupt transition: $\rho(x)$ is the charge distribution, $\mathscr{E}(x)$ the electric field and $\psi(x)$ the electrostatic potential along the position x. x_n is the junction boundary between the p^+ and n layers, x_p the junction boundary between n and the substrate, x_{p1} and x_{p2} are the limits of the depletion regions on the p^+ and p regions of the two junctions, respectively. Expressions for the electric field and the electrostatic potential are given in Appendix A.1.

zero. This condition is required to impose the boundary conditions. Under these assumptions, the total charge density $\rho(x)$ along the PPD is plotted in Fig. 3.4.

Solving the Poisson equation, $\nabla^2\psi(x) = -\rho(x)/\varepsilon_s$, analytical expressions of the electric field, $\mathscr{E}(x)$, and electrostatic potential, $\psi(x)$, are derived (Appendix A.1). The $\mathscr{E}(x)$ and $\psi(x)$ are depicted in Fig. 3.4.

The maximum of the electrostatic potential, V_{max}, and its corresponding position, x_{max}, are obtained, and given by the following expressions

$$x_{\text{max}} = x_{\text{n}} + \frac{N_{\text{A}^+}}{N_D}(x_n - x_{\text{p1}}) = x_{\text{p}} - \frac{N_{\text{A}}}{N_D}(x_{\text{p2}} - x_p), \tag{3.1}$$

and

$$V_{\text{max}} = \frac{qN_{\text{A}^+}}{2\varepsilon_{\text{Si}}} \cdot \frac{N_{\text{A}^+} + N_{\text{D}}}{N_{\text{D}}}(x_n - x_{\text{p1}})^2, \tag{3.2}$$

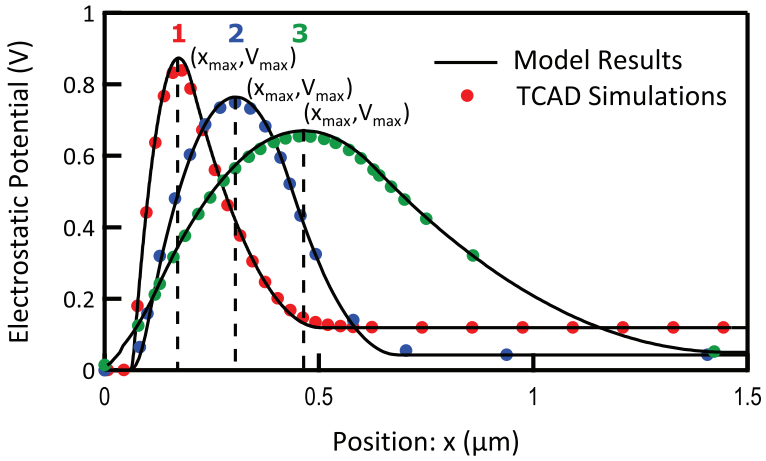


Figure 3.5: Electrostatic potential inside the PPD structure for Case 1, 2 and 3 reported in Table 3.1: the profile simulated in TCAD is compared with the expression derived in the proposed model. x_{max} is at 170 nm and V_{max} is 0.84 V at 300 K in case I, 305 nm and 0.76 V in case II, and 460 nm and 0.67 V in case III.

Table 3.1: Main Parameters for Three Cases of Pinned Photodiodes

	Case 1	**Case 2**	**Case 3**
$\mathbf{N_{A^+}}$ (cm^{-3})	10^{18}	10^{17}	10^{16}
$\mathbf{N_D}$ (cm^{-3})	10^{17}	2×10^{16}	5×10^{15}
$\mathbf{N_A}$ (cm^{-3})	10^{16}	10^{15}	10^{15}
$\mathbf{x_n}$ (nm)	70	100	120
$\mathbf{x_p}$ (nm)	200	430	630
$\mathbf{x_{max}}$ (nm)	170	305	460
$\mathbf{V_{max}}$ (V)	0.84	0.76	0.67

where N_{A^+} and N_D are the doping concentrations in the p^+ and the n-well regions, q the electron charge and ε_s the absolute permittivity of silicon. The maximum of the potential occurs at x_{max}, corresponding to the point where the electric field is equal to zero. The term x_{max} is therefore obtained by solving $\mathscr{E}(x) = 0$ in the depleted n region, resulting in (3.1).

Imposing the charge neutrality between the depleted p and n regions, given by

$$N_A x_{p2} - N_{A^+} x_{p1} = (N_A + N_D)\, x_p - (N_{A^+} + N_D)\, x_n \tag{3.3}$$

leads to the RHS of (3.1). The two derived expressions of (3.1) confirm that x_{max} is situated between x_n and x_p. Inserting x_{max}, obtained from (3.1), into the expression of the electrostatic potential (A.1.2) leads to the expression for its maximum, V_{max}, given by (3.2).

Fig. 3.5 shows the TCAD simulation results for the electrostatic potential profile along the device for different values of the geometrical parameters, reported in Table 3.1. Together with

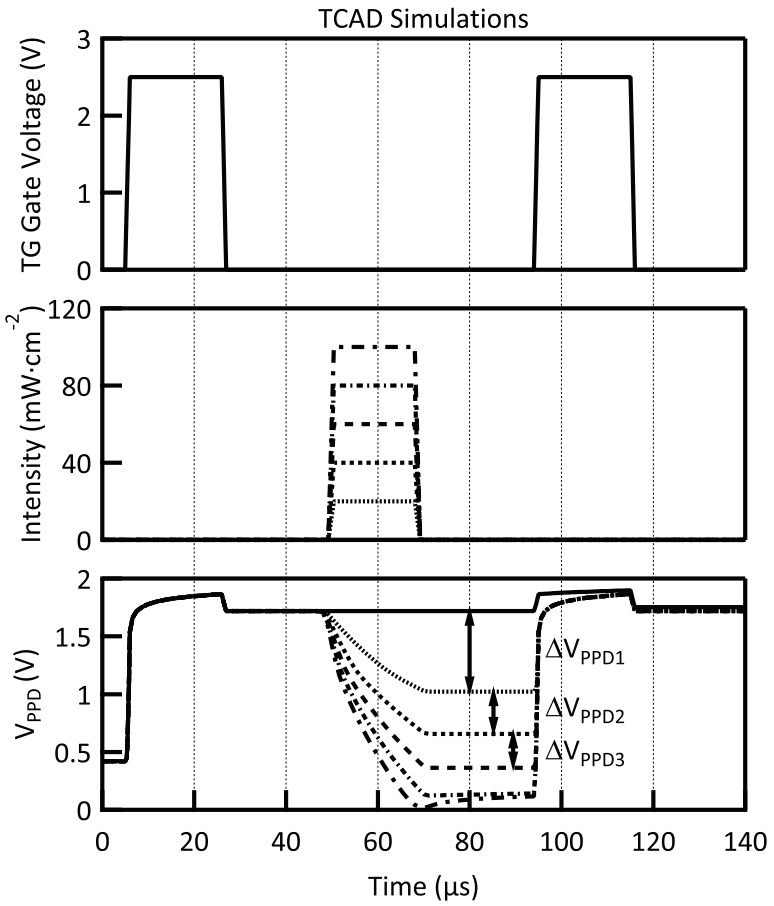


Figure 3.6: Opto-electrical transient simulations: the gate voltage applied to the TG, the intensity of the incident wave and the electrostatic potential inside the PPD. The changes in the electrostatic potential are proportional to the incident light and can be used to derive the PPD capacitance.

the potential profile of this device obtained with TCAD simulations, the model results are plotted. A very good agreement is observed between the model and TCAD simulations.

The Equilibrium Full Well Capacity (EFWC) is defined in [6] as the maximum photogenerated charges that can be accumulated in the PPD in dark conditions and neglecting the TG leakage current. Following this definition, the EFWC can be accurately estimated by the number of electrons stored in the PPD at equilibrium condition. The full well number of photogenerated electrons in the PPD volume between x_2 and x_1 (defined in Fig. 3.3) is given by $N_{\text{PPD,EFWC}} = A_{\text{PPD}}(x_2 - x_1)N_D$, where A_{PPD} is the area of the PPD.

3.3 Pinned Photodiode Capacitance

During illumination, the electrostatic potential inside the n-well decreases proportionally to the intensity of the light [7]. The ratio of the accumulated charges and the voltage variation

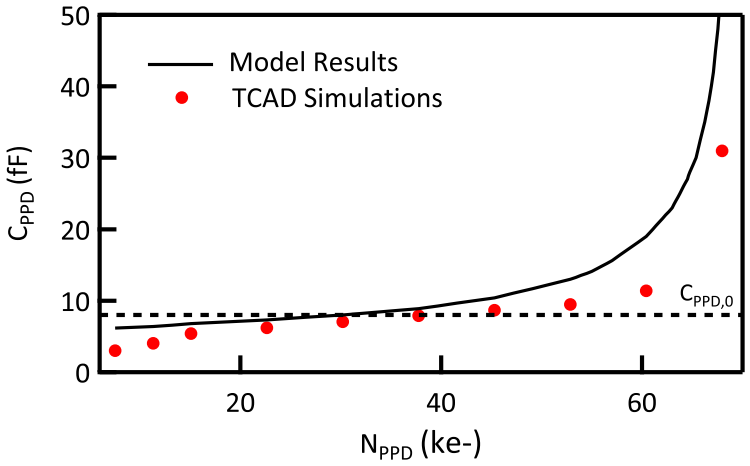


Figure 3.7: PPD capacitance as a function of the photogenerated electrons: TCAD simulations are compared with the proposed model.

corresponds to the capacitance $C_{\mathrm{PPD}} = (q\,N_{\mathrm{PPD}})/\Delta V_{\mathrm{PPD}}$. Whereas a detailed analytical model has been proposed in [8], the well-known expression of the junction capacitance [9] has been used in [10] and [11] to obtain an analytical expression of C_{PPD} . C_{PPD} can therefore be expressed as

$$\left(\frac{C_{\mathrm{PPD}}}{A_{\mathrm{PPD}}}\right)^2 = \frac{q\,\varepsilon_{\mathrm{s}}}{2\,(V_{\mathrm{max}} - \Delta V)}\,\frac{N_{\mathrm{D}} \cdot N_{\mathrm{A^+}}}{N_{\mathrm{D}} + N_{\mathrm{A^+}}}\,, \tag{3.4}$$

where q is the elementary charge, ε_{s} the permittivity of silicon, ΔV the variation of the electrostatic potential due to photo-generation. Typically for PPDs, $N_{\mathrm{A^+}} \gg N_{\mathrm{D}}$ while ΔV can be expressed as a function of N_{PPD}, equal to $N_{\mathrm{PPD}}/C_{\mathrm{PPD}}$. After some mathematical manipulations, the derived expression is

$$\left(\frac{C_{\mathrm{PPD}}}{A_{\mathrm{PPD}}}\right)^2 \approx \frac{q\,\varepsilon_{\mathrm{s}}\,N_{\mathrm{D}}}{2\,V_{\mathrm{max}}\left(1 - \dfrac{N_{\mathrm{PPD}}}{N_{\mathrm{PPD,FWC}}}\right)}\,, \tag{3.5}$$

where N_{PPD} and $N_{\mathrm{PPD,FWC}}$ are respectively the number of photogenerated electrons and the amount of electrons in the n-well at the full well condition, equal to $C_{\mathrm{PPD}} \cdot V_{\mathrm{max}}$.

In order to validate the proposed formula of C_{PPD} , a TCAD transient simulation with different values of light intensity is carried out. The light is represented by a linearly polarized plane wave for which the intensity, wavelength and angle of incidence can be properly set. In TCAD simulations, the illumination is set to a wavelength of 650 nm and a normal angle with respect to the surface of the device. The voltage applied to the TG, the pulses of light and the PPD voltage with respect to time are depicted in Fig. 3.6. First, to deplete the PPD from the charges a positive potential is applied to the gate. The PPD is then exposed to a pulse of light which generates an amount of photoelectrons. Increasing the light intensity leads to an increase of

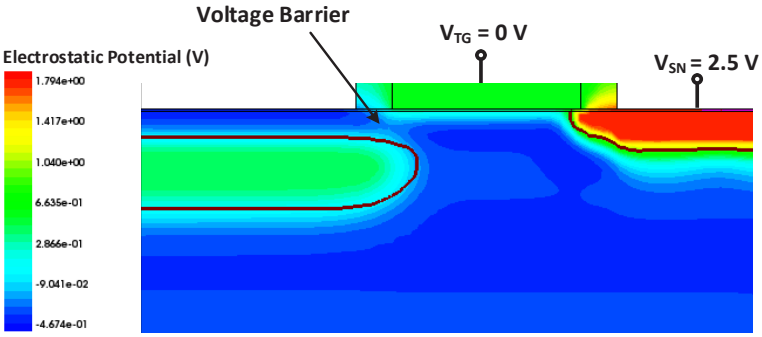


Figure 3.8: Electrostatic Potential of the interface between the PPD and the TG when $V_{TG} = 0$ V. Evidence of a potential barrier between the n-well and the semiconductor beneath the TG.

the PPD voltage variation.

To evaluate the $C_{PPD} = N_{PPD}/\Delta V_{PPD}$, N_{PPD} and the maximum voltage variation, ΔV_{PPD}, must be extracted properly using TCAD simulations. The ΔV_{PPD} can be readily determined from Fig. 3.6 for each value of the light intensity. In addition, N_{PPD} is estimated in TCAD simulations using the optical generation parameter, providing information about the semiconductor charge density. The parameter is integrated over the active volume and then multiplied by the integration time. To validate the proposed model the equivalent capacitance of the PPD is obtained through (3.5) and compared to TCAD simulations in Fig. 3.7. A good agreement is found for the numerical calculation and the model.

3.4 Potential Barrier Modeling

The np junction between the PPD n-well and the TG results in a potential barrier between the charge accumulation region and the semiconductor beneath the gate, as shown in Fig. 3.8. This barrier has been already reported in [12] and measurements performed in [13].

The proposed model for the charge transfer from the PPD to the SN is based on the prediction of the barrier's behavior with respect to the applied voltage to the TG and PPD voltage. The transfer mechanism is also assumed to be limited by the interface properties between the PPD and TG. This assumption is verified for relatively short devices which are not limited by internal diffusion mechanism [14]. The model covers the case where the SN voltage remains constant and always higher than the PPD maximum voltage and the TG channel voltage.

In order to derive an expression of the potential barrier, an equivalent 2D structure of all the regions crossed by path A is shown in Fig. 3.9. The proposed structure is a stretched version of the effective charge transfer path from the PPD to the SN and contains the MOS part, the p^+ layer, the n-well, and the p substrate. Path A is used to perform an electrostatic analysis deriving the potential barrier from Fig. 3.10(a) and illustrating the impact of the TG voltage. On the other hand, Path B corresponds to the current path and it is introduced to derive the

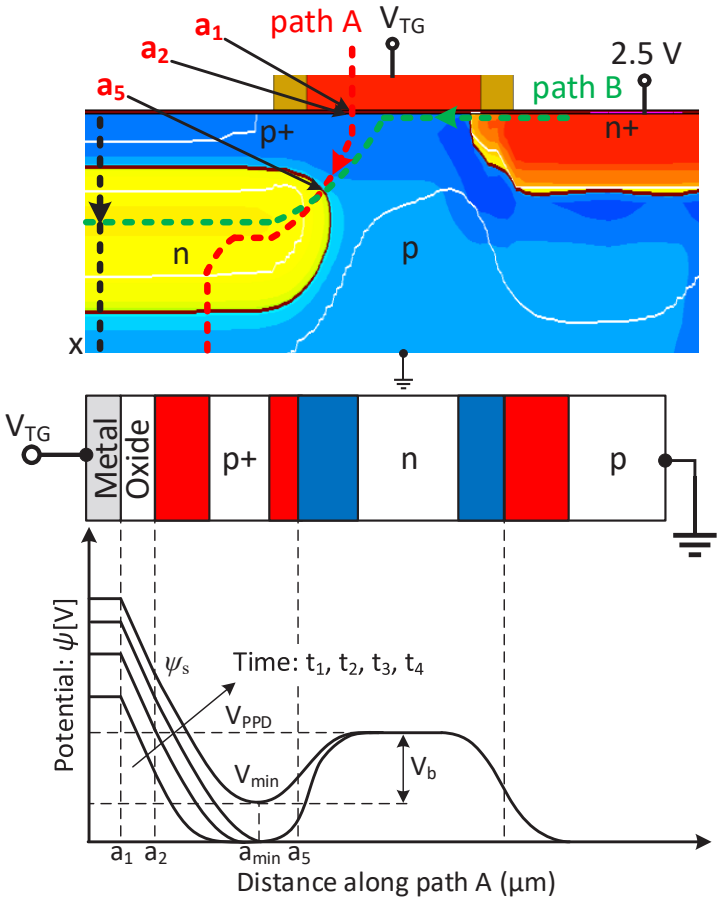
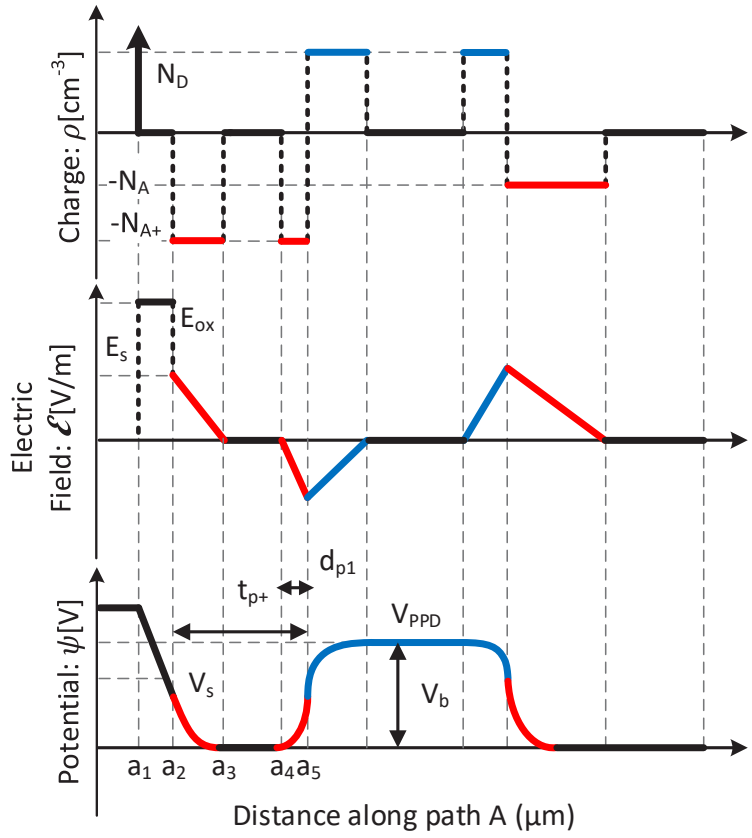


Figure 3.9: Section of the interface between the TG and PPD with the 2D equivalent stretched version. Electrostatic potential at the interface between the PPD and the TG during the sweep of the gate voltage. The barrier voltage is changed by the TG and PPD voltage values.

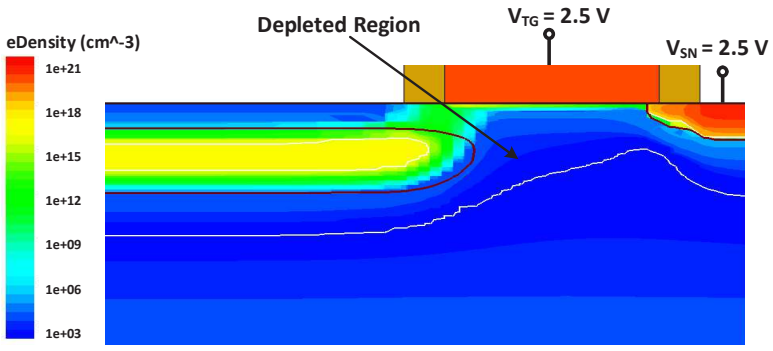
proposed model of the transferred charges, validated by TCAD simulation results.

As shown in Fig. 3.10(b), the region beneath the TG is almost completely emptied of electrons along the effective charge transfer path. The SN is biased to the value of 2.5 V, leading to the fully depleted region of the carriers around this node due to the high shift in the quasi-Fermi potential. In such a configuration, with a positive voltage applied to TG, there is no inversion layer under the gate. The presence of mobile charges under the transfer gate can impact the barrier height. However, in this particular case where the SN is kept to a high voltage value and the substrate to ground, any mobile charge under the transfer gate will move towards the corresponding contact. Moreover, it is assumed that the SN voltage is constant, which allows the impact of its variation on the charge transfer to be neglected [12].

The workfunction difference between the metal and the semiconductor together with the voltage applied to TG determine the surface potential, ψ_s. During the rising edge of the $V_{TG}(t)$, all the electrostatic potential of the MOS structure shifts up, as illustrated in Fig. 3.9. On the



(a)



(b)

Figure 3.10: In (a), the charge distribution, electric field, and electrostatic potential under the assumptions of full depletion and abrupt transitions. The interface region in (b) is fully depleted along the effective charge transfer path, for a $V_{TG} = 2.5\,V$ and $V_{SN} = 2.5\,V$.

other hand, we define the potential barrier $V_b(t)$ as the voltage difference between the voltage inside the n-well, V_{PPD}, and the minimum voltage in the p-doped semiconductor beneath the transfer gate, V_{min}. This allows the behavior of the barrier to be predicted throughout the

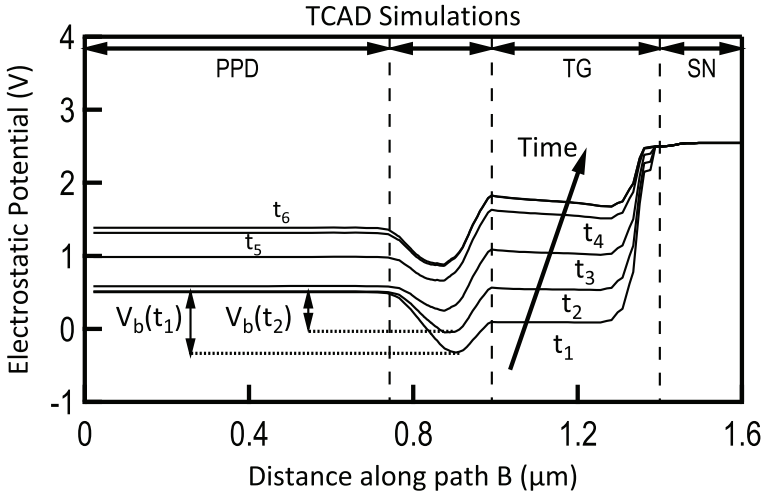


Figure 3.11: Electrostatic potential along the path B crossing the PPD well, the interface, the area beneath the TG and the SN, for different time instants. $t_1 - t_4$ corresponds to the rising edge of V_{TG}, while $t_5 - t_6$ refer to V_{TG} constant.

transfer time and leads to the following definition for the potential barrier

$$V_{\mathrm{b}}(t) = V_{\mathrm{PPD}}(t) - V_{\mathrm{min}}(t). \tag{3.6}$$

The term $V_{\mathrm{PPD}}(t)$ can be derived by the following expression

$$V_{\mathrm{PPD}}(t + \Delta t) = V_{\mathrm{PPD}}(t) + \frac{i(t) \cdot \Delta t}{C_{\mathrm{PPD}}}, \tag{3.7}$$

where $i(t)$ is the charge transfer current and Δt the time interval between two consecutive instances along the discretized time axis. Starting from the initial value, $V_{\mathrm{PPD},0}$, the values of $V_{\mathrm{PPD}}(t)$ are calculated at each iteration by the potential variation due to the amount of transferred charges, $i(t) \cdot \Delta t$.

On the other hand, Fig. 3.9 depicts the potential along path A at different instants during the rise of V_{TG}(t) . The figure clearly shows that the potential barrier V_{b}(t) is reduced due to the increase of the TG gate voltage, which enables the transfer of the charges to the SN. Using again the full-depletion approximation, the charge distribution, electric field and electrostatic potential along the proposed path are derived and plotted in Fig. 3.10(a). The expressions for the electric field and electrostatic potential are presented in Appendix A.2. Starting from a_2, the solution of the Poisson equation is equal to

$$\psi(a) = \psi_{\mathrm{s}} - E_{\mathrm{s}}(a - a_2) + \frac{qN_{\mathrm{A}^+}}{2\varepsilon_{\mathrm{s}}}(a - a_2)^2. \tag{3.8}$$

The increase in the gate voltage will increase the depletion region beneath the gate, until merging with the depleted region around the n-well. Under this assumption, $\rho(a)$ can be con-

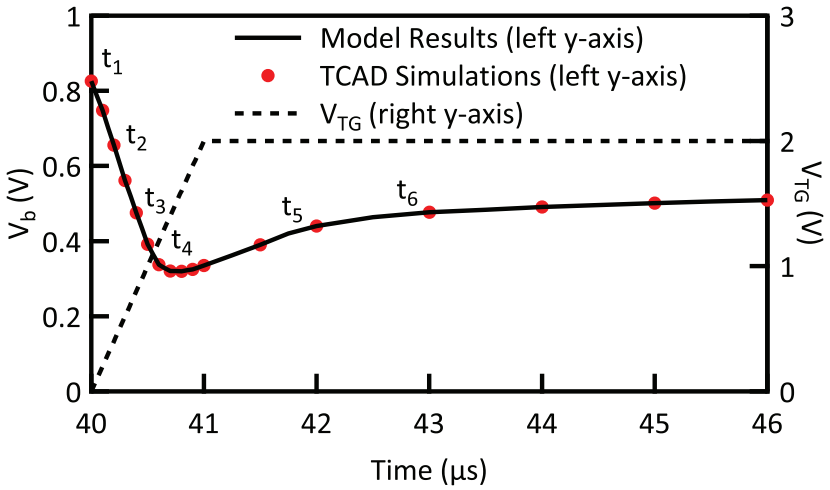


Figure 3.12: Value of the potential barrier during time along the charge transfer period. The behavior of the barrier is well predicted by the proposed model.

sidered to be equal to $-qN_{A^+}$ for $a_2 \leq a \leq a_5$. $V_{\min}(t)$ is the minimum value of the electrostatic potential in the region between the PPD and the semiconductor beneath the TG, while $a_{\min}$ is the position of $V_{\min}$ ($V_{\min} = \psi(a_{\min})$). Since in this point the value of the electric field must be zero, $a_{\min}$ is equal to $a_2 + t_{p^+} - d_{p1}$, where t_{p^+} is the thickness of the p^+ layer and d_{p1} the width of the depletion region of the p^+n junction in the p^+ region (see Fig. 3.10(a)). The solution to the Poisson equation allows an analytical expression of the barrier to be obtained, which includes the effect of V_{TG} .

By using the expression of the depletion region in a metal-oxide-semiconductor as a function of the applied gate voltage (reported in Appendix A.2) and after some mathematical manipulations, $V_{\min}$ results in

$$
\begin{aligned}
&V_{\min}(t) = \\
&\frac{qN_{A^+}}{2\varepsilon_s}\left(t_{p^+} - d_{p1}\right)^2 - \left(t_{p^+} - d_{p1}\right)\frac{qN_{A^+}}{C_{ox}}\left[1 - \sqrt{1 + \frac{C_{ox}^2}{2q\varepsilon_s N_{A^+}}V_{TG}(t)}\right] + \\
&+ \frac{q\varepsilon_s N_{A^+}}{2C_{ox}^2}\left[1 - \sqrt{1 + \frac{C_{ox}^2}{2q\varepsilon_s N_{A^+}}V_{TG}(t)}\right]^2 .
\end{aligned}
\tag{3.9}
$$

From the proposed formula, it can be seen that the height of the potential barrier is a function of V_{TG}(t) , the doping concentration in the semiconductor and the thickness of the p^+ layer t_{p^+} , which defines the position of the n-well.

To verify the validity of the proposed analytical expression of the potential barrier and its variation over time, a transient simulation in TCAD is performed. This simulation decouples the illumination from the charge transfer, by having first a pulse of light and then a pulse of voltage applied to the TG. The light therefore does not affect the potential barrier during the

transfer and its impact is not taken into account in the proposed model of $V_{\mathrm{b}}(\mathrm{t})$. To guarantee a full charge transfer, the width of the TG pulse is set to be longer than needed. In the specific case in which the transfer time is set to be shorter, i.e. high-speed applications such as ToF, the dynamic effects of the charge transfer, which are not considered in this derivation, have to be included. During this simulation, the SN is kept at a constant voltage of 2.5 V and a constant value equal to 7 fF is used as a good approximation of C_{PPD} within the range of interest.

The potential profile along the path B (Fig. 3.9) is plotted during different instants of time in Fig. 3.11. The simulation results show that this potential barrier is modulated by the gate voltage, as predicted by (3.6). All different values of $V_{\mathrm{b}}(\mathrm{t})$ are calculated from each potential profile and plotted as a function of the simulation time in Fig. 3.12. Initially, the barrier decreases following the linear slope of the V_{TG} rising edge. Once the gate voltage reaches the maximum value and remains constant, the potential barrier also starts to saturate and, due only to the charge transfer, slowly undergoes a slow change. As shown in Fig. 3.12, the simple model given by (3.6) is in agreement with the TCAD simulation results.

Increasing $V_{\mathrm{TG}}(\mathrm{t})$ lowers $V_{\mathrm{b}}(\mathrm{t})$ until V_{TG} reaches the threshold voltage of the MOS structure, above which the surface potential, ψ_{s}, only increases logarithmically with V_{TG} and most of the voltage drop occurs across the oxide [15]. This means that above the threshold, the surface potential will almost not be influenced by V_{TG} and no additional potential barrier reduction is achieved. On the other hand, a higher voltage will force the surface p^+ layer to be further depleted. Once this has occurred, the pinned structure is no longer present and the potential inside the n-well is then determined by the V_{TG} voltage.

3.5 Charge Transfer Current

Once the analytical expression of the potential barrier is developed and validated with TCAD simulations, it can be used to derive an expression of the charge transfer current. Relying on the thermionic emission mechanism, the transfer current crossing a potential barrier is obtained.

The thermionic emission theory states that the electrons which have enough thermal velocity in the transfer direction will cross the barrier on the charge transfer path [9] and has been used to model the charge transfer between the PPD and the SN [16, 12]. In TCAD simulations, path A is chosen as that with the minimum barrier and therefore the highest current density. In the model, the assumption is that all the current flows along the minimum barrier path, path A. Based on this transportation mechanism, the expression of the charge transfer current that embeds the effects of both the PPD and TG voltages and the other physical parameters on $V_{\mathrm{b}}(\mathrm{t})$ is derived.

The charge transfer current is given by

$$i(t) = I_0 \cdot \exp\left[-\frac{V_{\mathrm{b}}(t)}{U_T}\right] = I_0 \cdot \exp\left[-\frac{V_{\mathrm{PPD}}(t) - V_{\mathrm{min}}(t)}{U_T}\right], \tag{3.10}$$

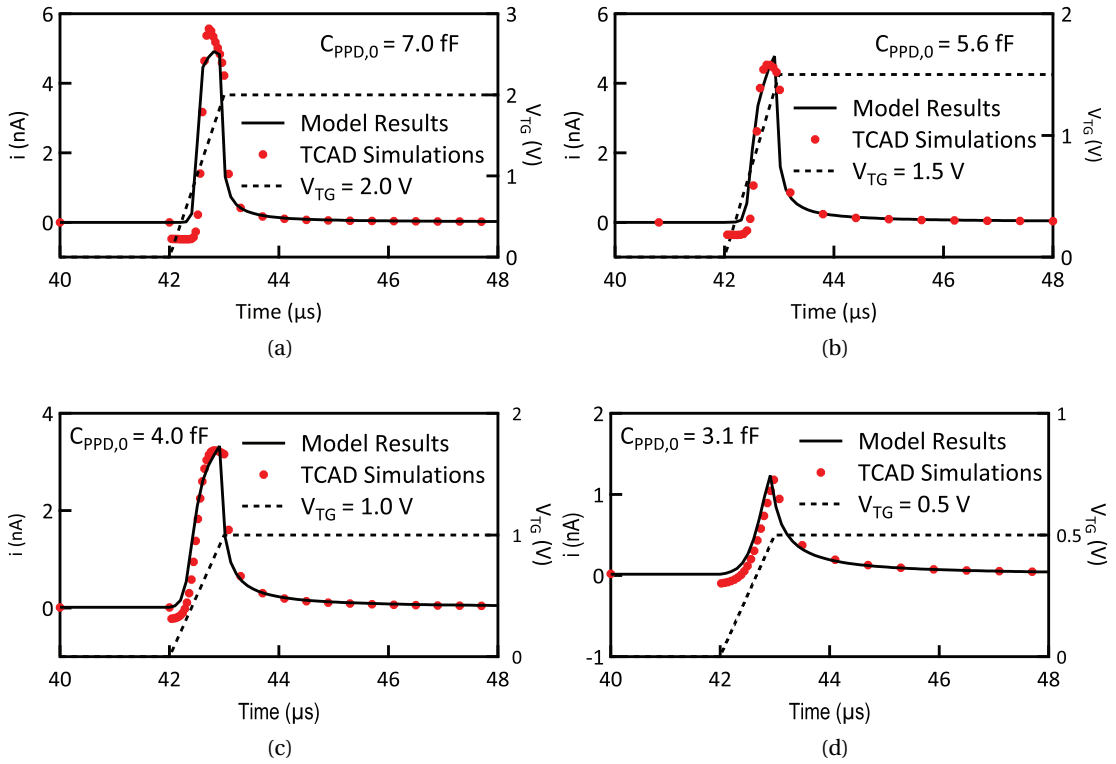


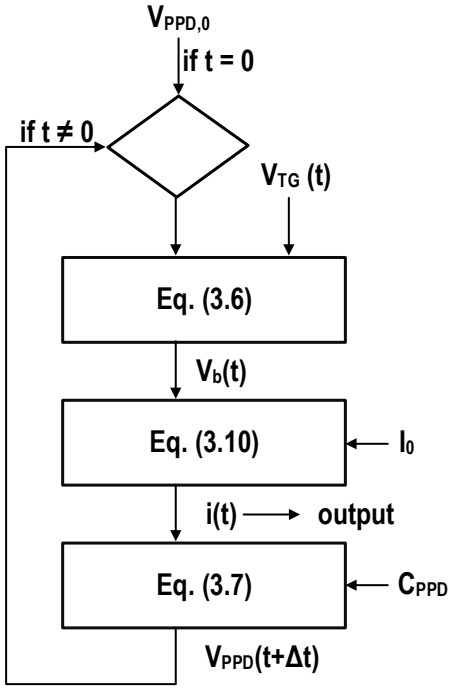
Figure 3.13: Current pulses in (a, b, c, d) representing the charge transfer from PPD to SN for four different V_{TG} values: TCAD simulations are compared with the proposed model.

where $V_b(t)$ is given by Equations (3.6) and (3.9) and I_0 is equal to $A\,S_A\,T^2$, with A equal to the Richardson constant [9], and S_A the area of the cross-section on the charge transfer path at the barrier position.

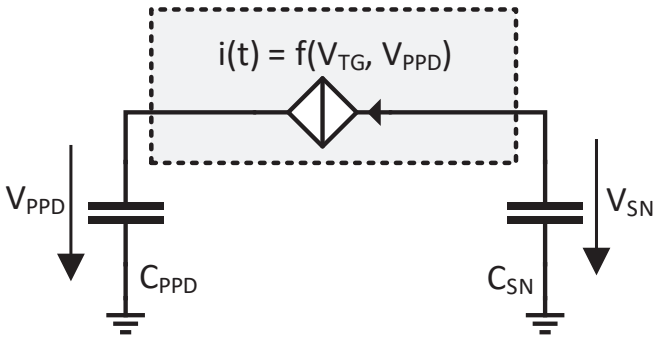
To validate this expression, the total current that flows through the SN can be extracted from the transient TCAD simulation results. The latter is shown in Fig. 3.13(a)-(d) for different values of V_{TG} : 2.0 V, 1.5 V, 1.0 V and 0.5 V. The simulation results obtained during the charge transfer can be compared with (3.10). The agreement between TCAD simulation results and the proposed model is good and confirms that the derived expression predicts the characteristic of the charge transfer from the PPD to the SN.

The exact values of the cross-section S_A have to be extracted from TCAD by looking at the current density distribution during the charge transfer. Based on the analysis of C_{PPD} shown in Section 3.3, we initially considered C_{PPD} as a constant parameter of the model, $C_{PPD,0}$, for the specific value of light used during simulation. The value of $C_{PPD,0}$ is equal to 7 fF and is shown in Fig. 3.7.

However, to obtain such an agreement between TCAD simulations and the proposed model, the constant value $C_{PPD,0}$ has been used as a fitting parameter. Thus, the value of $C_{PPD,0}$ has been reported for each simulated case in Fig. 3.13(a)-(d). This variation is reasonably predicted



(a)



(b)

Figure 3.14: Flow in (a) to evaluate the model based on the derived expressions. Proposed equivalent circuit in (b) for the PPD, TG, and SN, where the function f is given in (3.10).

in Fig. 3.7, where the value of C_{PPD} is not independent of the number of electrons stored in the photodiode. The dynamic modeling of C_{PPD} is investigated in [17, 18], and its use as a fitting parameter allows the proposed expression for the charge transfer current to be verified.

Until the TG voltage reaches a precise value, all the current pulses in Fig. 3.13(a)-(d) exhibit almost zero transferred charges. The voltage beneath the gate has to be higher than the PPD voltage in order to allow an efficient transfer of the integrated charge. The delayed charge transfer with respect to the TG voltage is consistent with [12]. When the final value of V_{TG} is below V_{PPD}, it results in an incomplete charge transfer. The latter is shown in the last two cases

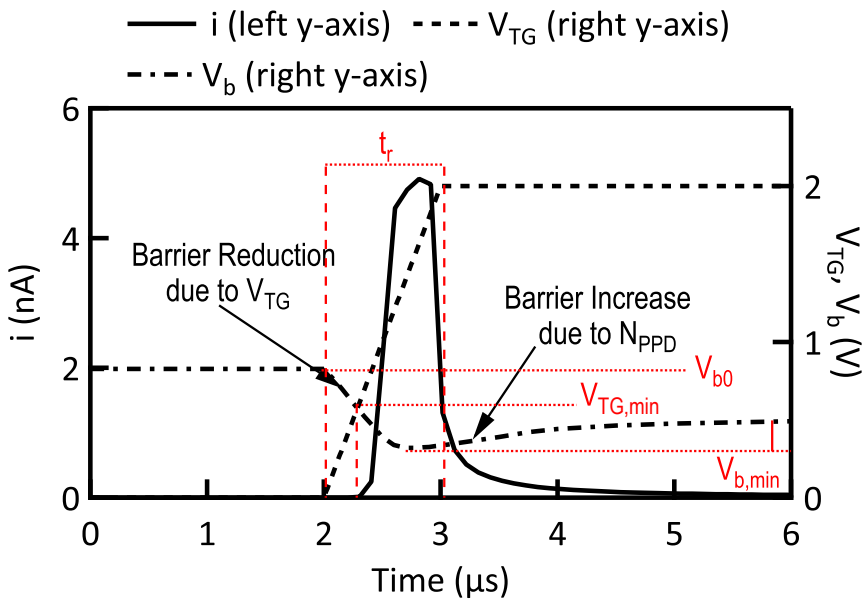


Figure 3.15: TCAD transient simulation of the charge transfer current together with the TG pulse and the potential barrier.

in Fig. 3.13(c)-(d), where the current pulse is considerably smaller than Fig. 3.13(a)-(b). On the other hand, the current initially exhibits negative values in transient simulations which can be explained as a capacitive coupling (overlap) between the TG and the SN. The calculated current through the proposed model does not include this phenomenon, hence the two curves substantially differ in this time interval.

In order to simulate the transient behavior with the proposed model, a quasi-static assumption together with equations (3.7), (3.6) and (3.10) are used. The evaluation flow of the model is summarized in the diagram in Fig. 3.14(a).

An equivalent circuit for the charge transfer from the PPD to the SN is given in Fig. 3.14(b). The PPD and the SN are replaced by two equivalent linear and time invariant capacitors, C_{PPD} and C_{SN}. The TG is replaced by a voltage-controlled current-source (VCCS). Since in a $\mathrm{p^+np}$ PPD the electrons are transferred to the SN, the VCCS indicates a current flowing from the SN to the PPD. Relying on the proposed model, the transfer current is expressed as function of V_{TG} and V_{PPD} according to (3.10).

3.6 Experimental Validation

3.6.1 Validation Methodology

Since the direct measurement of $i(t)$ is practically difficult, the validation of the model is performed through the measurement of the total amount of transferred charges, N_{tr} , which can be estimated from the readout output, V_{out} .

The expression of the thermionic emission current is used in [12] to derive an expression of N_{tr} as a function of the pulse width, T_{tr}, applied to the TG. The proposed experimental verification also includes the impact of the gate voltage, V_{TG}, embedded in the value of the potential barrier.

Fig. 3.15 shows the charge transfer current together with the TG pulse and the potential barrier. Since a value of 1 µs is used for the rising edge of the TG pulse, t_r, the two phases for the transfer process can be distinguished. The first phase takes place during the edge, and only starts when V_{TG}(t) reaches a value high enough ($V_{TG,min}$ in the figure), which depends on the initial PPD voltage; the second follows when V_{TG}(t) settles to its final value, V_{TGH}. During the first phase and due to the increase in V_{TG}(t), the initial value of the barrier, V_{b0}, linearly decreases to V_{min}, while during the second, the increase in V_{PPD} with a reduced number of electrons inside the PPD is responsible for a higher value of the barrier.

Since a voltage offset due to V_{PPD} needs to be taken into account during t_r, which is usually smaller than T_{tr}, the charge transferred during the rising edge of the TG pulse can be considered a small fraction of the one transferred when the gate voltage is set to V_{TGH}. Even though a zero charge is assumed to be transferred during the first phase, during the first phase V_{b0} is reduced to $V_{b,min}$.

If the time origin ($t = 0$) corresponds to the instant at which V_{TG}(t) becomes constant and the expression for barrier height correction derived in [12] is used, the potential barrier can be expressed as

$$V_b(t) = V_{b,min} + \frac{q}{2\cdot\varepsilon_{\mathrm{s}}}\cdot N_D\cdot d^2\cdot\left(1-\frac{N_{PPD}}{N_D\cdot\Lambda_{PPD}}\right)^2 = V_{b,min}+\Delta V_b\cdot\left(1-\frac{N_{PPD}}{N_D\cdot\Lambda_{PPD}}\right)^2, \quad (3.11)$$

where q is the elementary charge, ε_{s} the permittivity of silicon, N_D the doping concentration of the PPD n-well region, Λ_{PPD} the PPD volume, d is half of the PPD undepleted depth in a full well condition and $\Delta V_b = \frac{q}{2\cdot\varepsilon_{\mathrm{s}}}\cdot N_D\cdot d^2$. A parabolic relationship is found in [12] for the change in the potential barrier due to the number of electrons inside the PPD, while the term $N_D\cdot\Lambda_{PPD}$ represents the maximum number of electrons that can be stored in the n-well region.

When the expression of the potential barrier for the electrons inside the PPD is replaced in the thermionic emission current, it is possible to obtain a differential equation, given by

$$\exp\left[\frac{\Delta V_b}{U_{\mathrm{T}}}\cdot\left(1-\frac{N_{PPD}}{N_D\cdot\Lambda_{PPD}}\right)^2\right]\cdot N_{PPD}^{-1}\frac{dN_{PPD}}{dt} = -\frac{I_0}{qN_C\Lambda_{PPD}}\cdot\exp\left(-\frac{V_{b,min}}{U_{\mathrm{T}}}\right), \quad (3.12)$$

where $N_C = 2\cdot\left(\frac{2\pi\cdot m_n^*\cdot kT}{h^2}\right)^{3/2}$ is the conduction band effective density of states, m_n^* the effective mass of the electron in silicon and h the Planck constant. Due to the term on the left side of the equation, it is difficult to achieve an analytical solution when the modulation of the barrier is included.

However, N_{PPD} is lower than the full well in a working PPD and, when a small amount of transferred charge is considered, the change in the potential barrier due to N_{PPD} can be neglected. The barrier can therefore be assumed to remain constant and equal to $V_{b,min}$ throughout the charge transfer. This simplification allows the analytical solution for the differential equation to be found, given by

$$N_{tr}(t) = N_{PPD0} \cdot \left[1 - \exp\left(-\frac{I_0}{qN_C\Lambda_{PPD}} \cdot \exp\left(-\frac{V_{b,min}}{U_T}\right) \cdot t\right)\right], \tag{3.13}$$

where N_{PPD0} is the initial number of electrons in the PPD. The latter is the same expression found in [12] and can be expressed as

$$N_{tr}(t) = N_{PPD0} \cdot \left[1 - \exp\left(-\frac{t}{\tau \cdot \exp\left(\frac{V_{b,min}}{U_T}\right)}\right)\right], \tag{3.14}$$

where $\tau = \frac{qN_C\Lambda_{PPD}}{I_0}$ is a time constant related to the thermionic emission phenomenon. The higher potential barrier exponentially increases the transfer time. If enough time is given, the exponential term in (3.14) approximates to zero, and the charge transfer is complete. This expression is compared with measurement results in the next section.

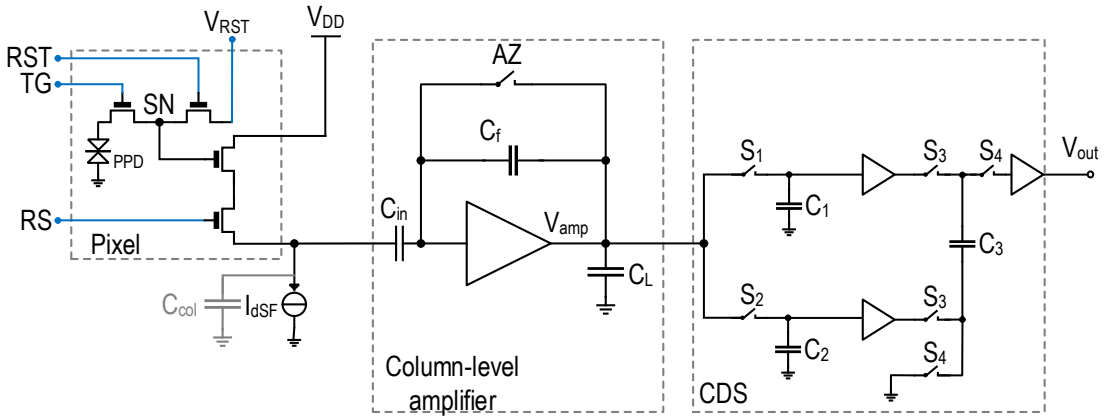
3.6.2 Experimental Setup

The schematic of the CIS readout chain implemented in a 180 nm CIS technology is shown in Fig. 3.16(a). The main blocks of the chain are a four transistor (4T) pixel, a CLA and a passive CDS circuit [19]. The pixel includes a PPD with a pitch of 12 µm, the TG, the RST, the in-pixel SF and the RS. The TG gate voltage amplitude and duration, T_{tr}, can be controlled externally.

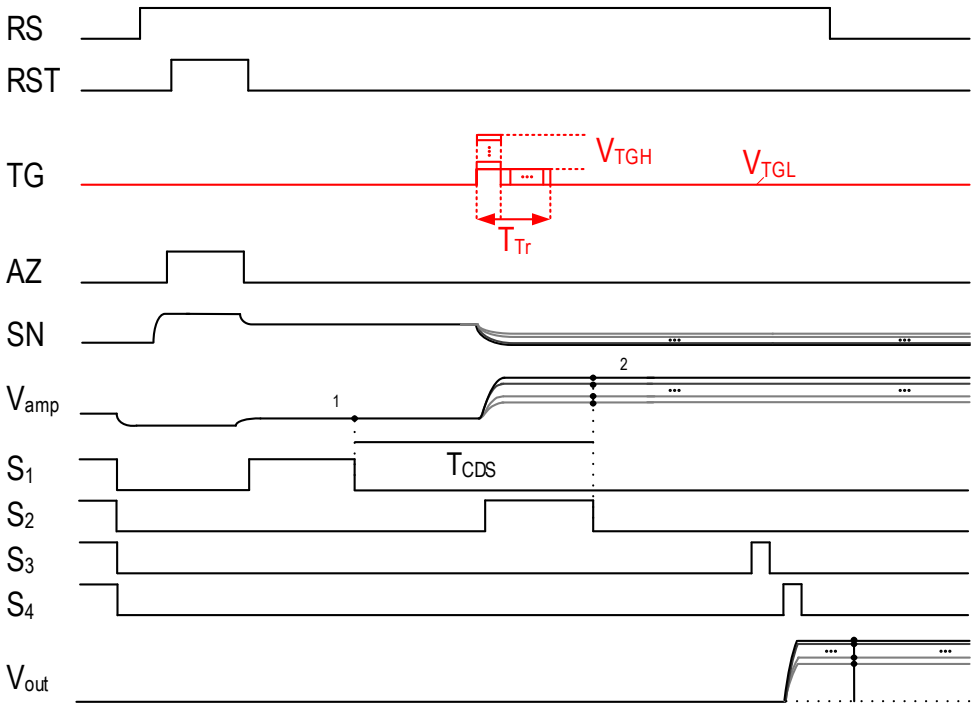
As shown in Fig. 3.16(b), the TG pulse features a low, V_{TGL}, and a high value, V_{TGH}. In the measurements shown in this section, the value of V_{TGL} is set to 0 V. Fig. 3.16(b) indicates that the amount of transferred charges will modify the SN voltage, the output voltage of the CLA, V_{amp}, and the readout output, V_{out}. The CDS block samples the amplifier output before and after the charge transfer in C_1 and C_2, respectively. The difference is then sampled on C_3 following the timing diagram in Fig. 3.16(b). When the column-level gain is set to unity, the CG of the readout chain is 75 µV/e$^-$, which is measured by using the PTC method [20]. The CG value is used directly to convert the output voltage to the number of electrons transferred from the PPD to the SN.

3.6.3 Measurement Results

Eq. (3.14) is validated by measuring N_{tr} for different values of V_{TGH} and T_{tr}. Three different exposure conditions are chosen for validation, from the lowest (exposure A) to the highest



(a)



(b)

Figure 3.16: Schematic in (a) of the implemented readout chain with a 4T pixel, the CLA and the passive CDS circuit. Timing diagram in (b) of the control signals and the main internal nodes: in order to obtain the measurement results, different values for the pulse width and the V_{TGH} are used.

(exposure C).

As shown in Fig. 3.17, the three exposures lie on the linear part of the sensor response and correspond respectively to an illumination power of 163 nW cm^{-2}, 565 nW cm^{-2} and 942 nW cm^{-2}. For these three conditions, the maximum amount of transferred charges are 520e^-, 1800e^- and

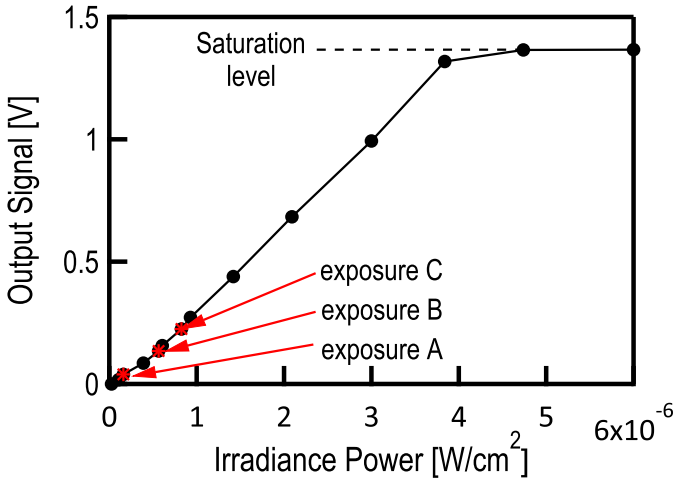


Figure 3.17: Readout Photon Response with the Exposure A, B and C marked with red asterisks.

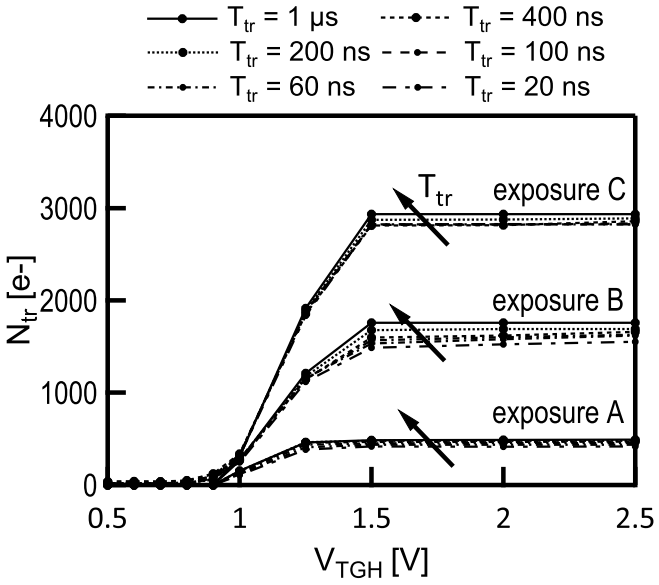
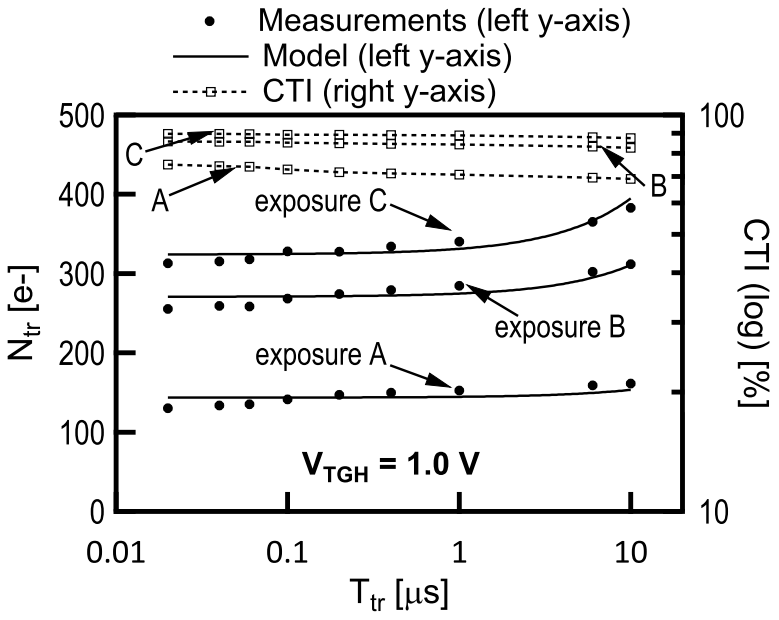


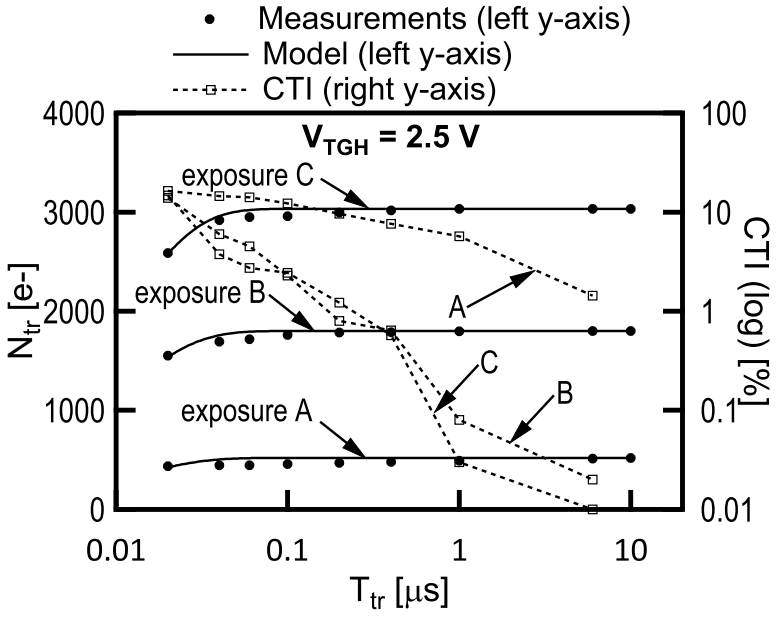
Figure 3.18: N_{tr} is plotted for different values of the transfer time versus the TG voltage for three different exposures (exposure A, B and C). This figure shows the values of V_{TGH} that allow a complete charge transfer.

$3000e^-$. In order to limit the variation of the SN voltage and neglect the impact of V_{SN} on the charge transfer current, the transferred charges are limited to a small fraction of the FWC.

Fig. 3.18 shows N_{tr} versus V_{TGH} for the three different exposures and for six different values of T_{tr}, ranging from 20 ns to 1 µs. The range for V_{TGH} goes from 0.5 V to 2.5 V. From 0 V to about 0.9 V there is almost no charge transfer. From 0.9 V to almost 1.5 V, all the curves show a transition region, where the charge transfer can be considered incomplete. Finally, above 1.5 V, the charge transfer saturates and is then complete. This figure has been used to select two different values of V_{TGH}, one for an incomplete and the other for a complete charge transfer. The two different scenarios are then compared with the analytical model results.



(a)



(b)

Figure 3.19: N_{tr} is plotted for V_{TGH} equal to 1 V in (a) and 2.5 V in (b) versus the T_{tr} , together with the model results. the CTI for the two cases also is plotted with dashed lines.

Fig. 3.19(a) and Fig. 3.19(b) show N_{tr} versus T_{tr} in a lin-log plot for the same exposure and for a V_{TGH} equal to 1.0 V and 2.5 V, respectively. The value of CTI is also computed at each point by dividing the value of the transferred charge by its maximum value, which is taken from the measurement at V_{TGH} equal to 2.5 V and T_{tr} equal to 10 µs. As shown in Fig. 3.19(a) and (b)

Table 3.2: Summary of Values for Model Parameters

		Exposure A	**Exposure B**	**Exposure C**
N_{PPD0}	$[e^-]$	520	1800	3033
A	$[\text{A cm}^{-2}\text{K}^{-2}]$		120	
S_{A}	$[\text{cm}^2]$		5×10^{-8}	
T	[K]		300	
I_0	[A]		0.54	
N_{C}	$[\text{cm}^{-3}]$		2.82×10^{19}	
Λ_{PPD}	$[\text{cm}^3]$		5×10^{-11}	
q	[C]		1.6×10^{-19}	
τ	[ns]		0.41	
t_{ox}	[cm]		1×10^{-5}	
C_{ox}	$[\text{F cm}^{-1}]$		3.45×10^{-8}	
$t_{p+} - d_{p1}$	[cm]		1×10^{-5}	
N_{D}	$[\text{cm}^{-3}]$		2.4×10^{15}	
$N_{\text{A+}}$	$[\text{cm}^{-3}]$		5×10^{16}	
d	[cm]		2.5×10^{-5}	
V_{b0}	[V]		0.71	
$V_{b,min}$ @ V_{TGH} = 1.0V	[V]		0.36	
$V_{b,min}$ @ V_{TGH} = 2.5V	[V]		0.07	

with dashed lines, the value of the CTI is high (from 70 % to 90 %) for V_{TGH} equal 1.0 V, while it substantially decreases (until values lower than 1 %) when V_{TGH} is 2.5 V. The measurement results, shown with markers, are compared with the proposed expression in (3.14), drawn with solid lines.

3.6.4 Model Comparison

To obtain a good agreement between the measurements and (3.14), the values of the model parameters shown in Table 3.2 are used.

The initial number of electrons stored in the PPD for each exposure is equal to the total transferred charge when a complete transfer is obtained, hence for a V_{TGH} equal to 2.5 V and T_{tr} of 10 µs. As it is done for Λ_{PPD}, the value of the cross-section S_A is estimated from the size of the photodiode, which ultimately affects the obtained values for I_0 and τ. In order to estimate the values of $V_{b,min}$ for a specific value of V_{TGH}, first the value of the potential

barrier at equilibrium, V_{b0}, is estimated by using the formula of the built-in potential of a n-p$^+$ junction [9], given by

$$V_{b0} = U_T \cdot \ln\left(\frac{N_D \cdot N_{A^+}}{n_i^2}\right), \tag{3.15}$$

where n_i is the intrinsic carrier density in silicon (1×10^{10} cm^{-3} at 300 K) and reasonable values have been assumed for the doping concentrations, N_D and N_{A+}. The values for $V_{b,min}$ are then estimated by using (3.9) for the two different values of V_{TGH} . Based on reported values for the model given in [21], an assumption have been made on the TG oxide, t_{ox}, and the undepleted region in the p^+ layer thicknesses, $t_{p+} - d_{p1}$.

Even though the technological parameters would need to be aligned with more accurate information from the specific process, the reported values are the one that minimize the error between the measurement and model results, and prove that the used formula can well predict the transferred charge under different illumination and transfer conditions.

3.7 Summary

The core of a compact physics-based model for the PPD together with the TG has been obtained by deriving an analytical expression of the charge transfer current. The 2D equivalent structures of the PPD and the charge transfer path have been used under full-depletion approximation to derive an expression of the main model parameters.

This model is first validated by static and transient opto-electrical simulations in TCAD and then experimentally verified by measuring the equivalent number of transferred electrons in a CIS readout chain under different light illumination, TG voltage and transfer times.

A good agreement with experimental data has been observed. The proposed model is developed as a tool for the analysis, design and optimization of PPD-based pixels in low light CISs.

State-of-the-Art Advancements

The pinning voltage model parameter, V_{pin} , was introduced in [22] and a comparison of the main estimation methods given in [23]. As reported in [5], the definition of the pinning voltage can be controversial. In this work, the derivation based on Fig. 3.4 is a simple analysis of the PPD structure, where the values of the PPD electrostatic potential are expressed in terms of the main physical and process parameters. Supported by TCAD simulation results, the proposed derivation aims to clarify the definition of the pinning voltage.

The PPD capacitance, C_{PPD} , was modeled as a depletion capacitance in [11] and the reported models in [6] and [24] assumed a constant value, independent of the operating conditions.

However, a highly nonlinear and voltage dependent behavior close to the full well condition was observed in the measurement results reported in [17]. In this work, an expression is proposed that relates C_{PPD} to the amount of charge stored in the PPD. By evaluating this expression and by comparing with the Q-V TCAD simulation results based on optical illumination, an interval of the PPD stored charges is estimated where it is reasonable to assume a constant value for C_{PPD} .

The main contribution described in this chapter is the modeling of the interface potential barrier, $V_b(t)$. The evidence of a potential barrier was reported in [12] and in [5]. However, an expression of the potential barrier that includes the impact of the PPD and the TG potentials was still missing. The expressions in (3.6), (3.7) and (3.9) allow to predict the instantaneous value of the potential barrier as a function of the optical and electrical operating conditions and to take into account the values of the physical and process parameters.

When combined to the expression based on the thermionic emission theory proposed in [12], this work shows how the instantaneous value of the charge transfer current can be predicted. Since it opens to the implementation of the model as a Verilog-A code, the obtained match between the analytical expression and the complex 3D TCAD simulations is an important achievement of this work.

Experimental results for the charge transfer model were presented in [12], where the expression of the total amount of transferred charges in (3.13) was derived and different PPD designs were used to verify the model trends. A contribution of this work is the direct comparison between the compact model and the experimental results under different operating conditions. The obtained match with reasonable values of the extracted parameters is a fundamental step along the model development.

References for Chapter 3

[1] Y. Tochigi, K. Hanzawa, Y. Kato, R. Kuroda, H. Mutoh, R. Hirose, H. Tominaga, K. Takubo, Y. Kondo, and S. Sugawa, "A global-shutter CMOS image sensor with readout speed of 1Tpixel/s burst and 780 Mpixel/s continuous," in *2012 IEEE International Solid-State Circuits Conference*, 2012.

[2] Z. Cao, Y. Zhou, Q. Li, L. Liu, and N. Wu, "Design of pixel for high speed CMOS image sensor," in *Proceedings of the International Image Sensor Workshop*, 2013.

[3] Synopsys.com, "Technology computer aided design (TCAD)," Available on:https://www.synopsys.com/silicon/tcad.html. Accessed on May 2020.

[4] E. R. Fossum and D. B. Hondongwa, "A Review of the Pinned Photodiode for CCD and CMOS Image Sensors," *IEEE Journal of the Electron Devices Society*, vol. 2, no. 3, pp. 33–43, 2014.

[5] A. Pelamatti, *Estimation and Modeling of Key Design Parameters of Pinned Photodiode*

CMOS Image Sensors for High Temporal Resolution Applications. PhD thesis, Université de Toulouse, 2015.

[6] A. Pelamatti, V. Goiffon, M. Estribeau, P. Cervantes, and P. Magnan, "Estimation and Modeling of the Full Well Capacity in Pinned Photodiode CMOS Image Sensors," *IEEE Electron Device Letters*, vol. 34, no. 7, pp. 900–902, 2013.

[7] Y. Xu, X. Ge, and A. Theuwissen, "Investigating Transfer Gate Potential Barrier by Feed-Forward Effect Measurement," in *Proceedings of the International Image Sensor Workshop*, 2015.

[8] H. Alaibakhsh and M. A. Karami, "A New Analytical Pinned Photodiode Capacitance Model," *IEEE Electron Device Letters*, vol. 39, no. 3, pp. 379–382, 2018.

[9] S. Sze and K. Ng, *Physics of Semiconductor Devices*. Wiley, 2006.

[10] V. Goiffon, M. Estribeau, J. Michelot, P. Cervantes, A. Pelamatti, O. Marcelot, and P. Magnan, "Pixel Level Characterization of Pinned Photodiode and Transfer Gate Physical Parameters in CMOS Image Sensors," *IEEE Journal of the Electron Devices Society*, vol. 2, no. 4, pp. 65–76, 2014.

[11] C. Cao, B. Shen, B. Zhang, L. Wu, and J. Wang, "An Improved Model for the Full Well Capacity in Pinned Photodiode CMOS Image Sensors," *IEEE Journal of the Electron Devices Society*, vol. 3, no. 4, pp. 306–310, 2015.

[12] L. Han, S. Yao, and A. J. P. Theuwissen, "A Charge Transfer Model for CMOS Image Sensors," *IEEE Transactions on Electron Devices*, vol. 63, pp. 32–41, Jan 2016.

[13] C. Chen, Z. Bing, W. Junfeng, and W. Longsheng, "Measurement of charge transfer potential barrier in pinned photodiode CMOS image sensors," *Journal of Semiconductors*, vol. 37, no. 5, p. 054007, 2016.

[14] A. Pelamatti, V. Goiffon, A. Chabane, P. Magnan, C. Virmontois, O. Saint-Pé, and M. B. de Boisanger, "Charge Transfer Speed Analysis in Pinned Photodiode CMOS Image Sensors based on a Pulsed Storage-Gate Method," in *45th European Solid State Device Research Conference*, 2015.

[15] C. Enz and E. Vittoz, *Charge-Based MOS Transistor Modeling: The EKV Model for Low-Power and RF IC Design*. Wiley, 2006.

[16] E. R. Fossum, "Charge Transfer Noise and Lag in CMOS Active Pixel Sensors," in *Proceedings IEEE Workshop Charge-Coupled Devices and Advanced Image Sensors*, 2003.

[17] U. Khan and M. Sarkar, "Dynamic capacitance model of a pinned photodiode in cmos image sensors," *IEEE Transactions on Electron Devices*, vol. 65, pp. 2892–2898, July 2018.

[18] U. Khan and M. Sarkar, "Dynamic capacitance variations due to barrier modulation in pinned photodiode of cmos image sensor," *IEEE Transactions on Electron Devices*, vol. 66, pp. 5202–5208, Dec 2019.

[19] R. Capoccia, A. Boukhayma, and C. Enz, "Experimental Verification of the Impact of Analog CMS on CIS Readout Noise," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 67, pp. 774–784, March 2020.

[20] J. Janesick, *Photon Transfer*. SPIE Press, 2007.

[21] J. Xu, R. Wang, L. Han, and Z. Gao, "Analysis and modeling of spill back effect in high illumination cmos image sensors," *IEEE Sensors Journal*, vol. 20, no. 6, pp. 3024–3031, 2020.

[22] A. Krymski and K. Feklistov, "Estimates for scaling of Pinned Photodiodes," in *Proceedings of the International Image Sensor Workshop*, 2005.

[23] A. Pelamatti, V. Goiffon, A. de Ipanema Moreira, P. Magnan, C. Virmontois, O. Saint-Pé, and M. B. de Boisanger, "Comparison of Pinning Voltage Estimation Methods in Pinned Photodiode CMOS Image Sensors," *IEEE Journal of the Electron Devices Society*, vol. 4, no. 2, pp. 99–108, 2016.

[24] M. Sarkar, B. Buttgen, and A. J. P. Theuwissen, "Feedforward Effect in Standard CMOS Pinned Photodiodes," *IEEE Transactions on Electron Devices*, vol. 60, pp. 1154–1161, March 2013.

4 Noise Sources in CIS

The signal in a CIS is corrupted by numerous noise sources injected at different levels: during the photoelectron generation at the PPD, during the charge transfer to the SN or at the level of the readout circuit. The mechanisms behind these sources are also different: the photon shot noise (PSN) is for example due to the nature of the light, whereas the dark current shot noise (DCSN) and the transfer noise depend on device defects; the fixed pattern noise (FPN) is caused by pixel-to-pixel or column-to-column non-uniformities, and the thermal, the flicker and the shot noise sources are generated by electronic devices. Some, such as the PSN and the FPN, are also signal-dependent noise sources and their variance therefore depends on the level of the input light [14].

This chapter describes each noise source and provides a brief theoretical background of the main physical mechanism and statistical models. The expressions of variance and power spectral density (PSD) are also derived for each noise component. The PSDs are used later during the readout noise analysis and are fundamental in order to establish the role of readout noise in low-light CIS. The total signal-to-noise ratio (SNR) is derived and plotted at the end of the chapter against the number of photogenerated electrons, N, in order to highlight the dominant role of the readout noise at low light conditions.

4.1 Photon Shot Noise

The PSN is a fundamental noise component connected to the way photons arrive in space and time on a detector. Even if the incident light is modeled as a particle flux with a constant rate in time, the average number of interacting photons per pixel is not uniform. The PSN is defined by the standard deviation (or root mean square (RMS)) of the photon distribution. Two 300×300 pixels images in Fig. 4.1 show the difference between noiseless (a) and noisy scenarios when the average number of photons per pixel is equal to 1.

The shot noise is a statistical phenomenon resulting from a series of independent events occurring with the same probability. When a photon flux with an average rate constant in

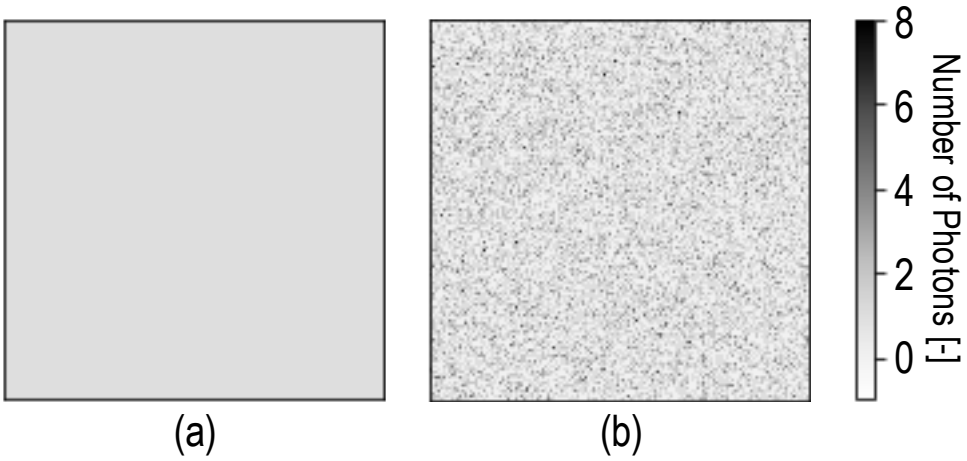


Figure 4.1: A noiseless image in (a) and one affected by PSN with average number of photons per pixel equal to 1.

time is considered, the arrival of each particle on the sensor is a series of independents event occurring with the same probability and therefore obeys to a Binomial Law [18]. When the probability of incidence is close to unity, the Binomial Laws tends to a Poisson distribution [18]. Based on a Poisson statistics, the probability distribution to receive a number equal to i of particles assuming an average number of incident particles equal to N_{ph} can be expressed by

$$p_i = \frac{N_{ph}^i}{i!} e^{-N_{ph}}, \tag{4.1}$$

The expression above is evaluated for N_{ph} equal to 1, 10 and 20, respectively, and the resulting histograms are plotted in Fig. 4.2 against the effective number of photons per pixel. A 300×300 array for the detector is assumed and a Gaussian fit is also drawn for each distribution.

As shown in Fig. 4.2, the Gaussian curve approximates accurately a Poisson distribution when the number of photons per pixel is large: a near-perfect fit is observed for an average number of photons per pixel equal to 20. The Gaussian distribution is characterized by a probability function given by

$$p_i = \frac{1}{\sqrt{2\pi\sigma_N^2}} e^{-\frac{(i-\mu_N)^2}{2\sigma_N^2}}, \tag{4.2}$$

where μ_N and σ_N^2 are the average and variance values, respectively.

One of the main properties of the PSN following a Poisson statistics is that the noise variance simply reduces to

$$\sigma_{Sh}^2 = N_{ph}. \tag{4.3}$$

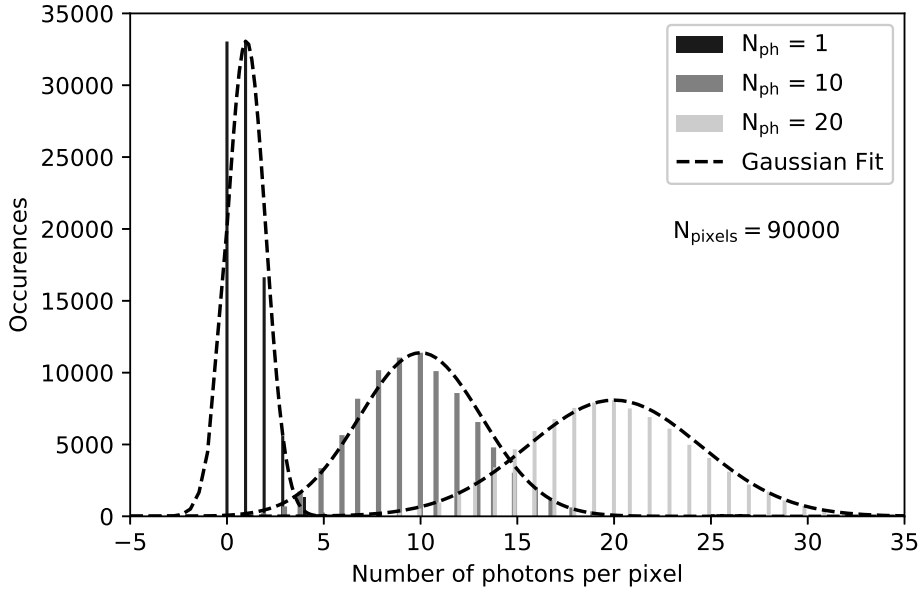


Figure 4.2: Histogram of the average number of photons per pixel assuming an average incident photon per pixel equal to 1, 10 and 20, respectively. A Gaussian distribution fits the Poisson distribution well at a large value of incident photons.

The variance of the received number of photons per pixel is equal to the incident average: a higher amount of photons hitting the sensors translates into a broader distribution for the effective number of photons per pixel.

The property of CMOS cameras to be photon shot-limited is often used to characterize the sensor. Excluding the ADC at the end of the chain and assuming an in-pixel SF amplifier, a CMOS camera can be modeled by the block diagram shown in Fig. 4.3. Each stage of the chain represents a transfer function related to the semiconductor, pixel and readout circuit, with different signal and noise terms defined in between. The input to the camera is the average number of incident photons, N_{ph}, while the analog output is the output of the CDS block, V_{out}. The output can be expressed as a function of the input in

$$V_{out}(N_{ph}) = N_{ph} \cdot QE \cdot A_{SN} \cdot A_{SF} \cdot A_{col} \cdot A_{CDS}, \tag{4.4}$$

where QE is the number of photogenerated electrons per number of photons, while A_{SN}, A_{SF}, A_{col} and A_{CDS} are respectively the transfer functions for the SN, SF, CLA and CDS blocks. Assuming $QE = 1$ and introducing the overall camera transfer function or conversion gain, CG, (4.4) can be rewritten as

$$V_{out}(N_{ph}) = N_{ph} \cdot CG. \tag{4.5}$$

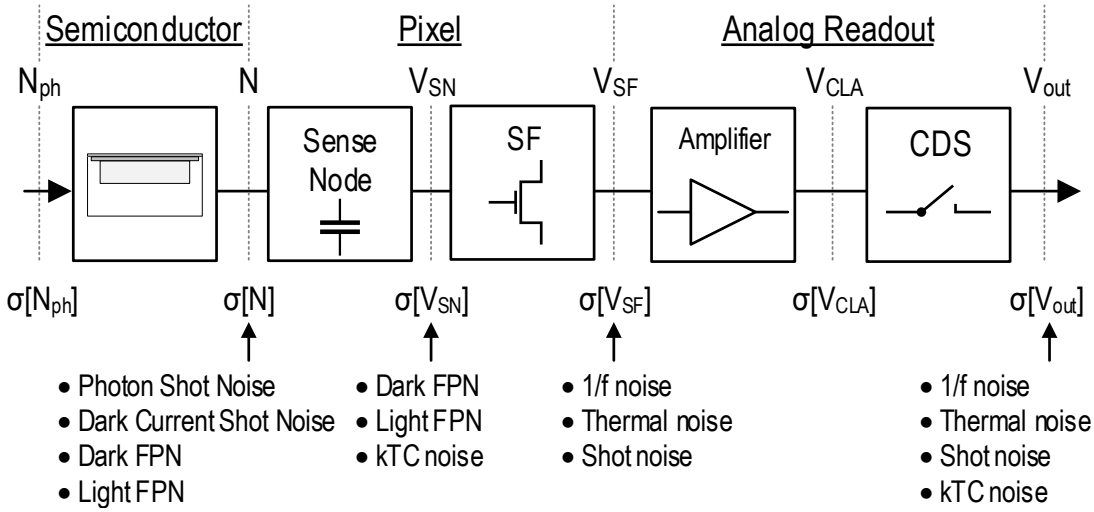


Figure 4.3: Block diagram of a CIS digital camera with an average number of photons as input and an analog output. Each block in between implements the transfer function related to the semiconductor, pixel and readout circuits.

Each individual transfer function is rather difficult to measure, while the Photon Transfer (PT) method provides a solution to evaluate CG. Thanks to the latter, the RMS output voltage, $\sigma[V_{out}(N_{ph})]$, can also be expressed as

$$\sigma\left[V_{out}(N_{ph})\right] = \sigma\left[N_{ph}\right] \cdot CG. \tag{4.6}$$

Replacing the variance and signal mean in (4.3) by the expressions given respectively by (4.5) and (4.6), the CG can be expressed as

$$CG = \frac{\sigma^2[V_{out}(N_{ph})]}{V_{out}(N_{ph})}. \tag{4.7}$$

The above expression is called the PT relation and shows that it is possible to evaluate CG by measuring the output voltage statistics and dividing the output variance by the average value, without knowing the individual camera transfer functions. For given values of $\sigma^2[V_{out}(N_{ph})]$ and $V_{out}(N_{ph})$, a unique value of CG will satisfy the condition given in (4.3) for the input. It is also important to notice that a similar law does not apply to the output voltage: in such a case, CG would in fact be forced to be always equal to one.

The curve for the output variance versus average is called the Photon Transfer Curve (PTC) [14]. Fig. 4.4 shows the measured PTC obtained with the column readout circuit designed in this work and later explained in detail. The conversion gain CG can be measured as the slope of the linear part, while the average signal for which the PTC curve collapses corresponds to the full well capacity of the sensor. This saturation point could be due to the saturation of the electronic readout circuit or to that of the photodiode if the DR of the readout chain is high enough. The noise variance in dark conditions (for an average signal equal to zero)

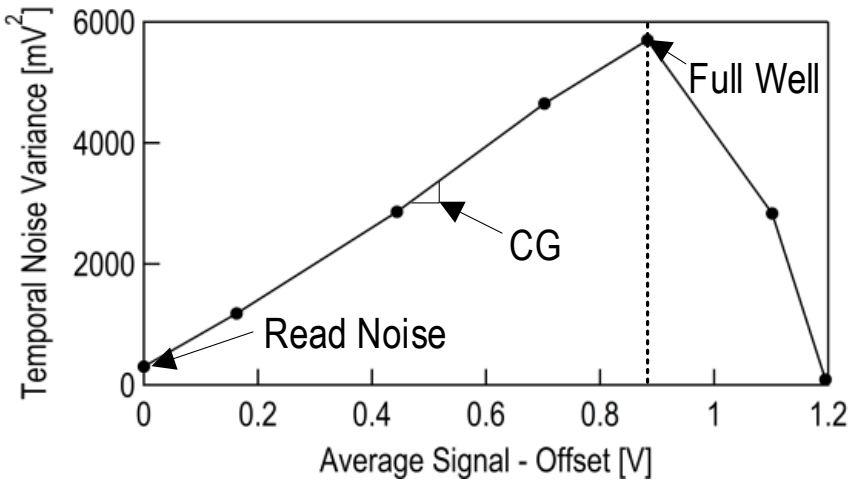


Figure 4.4: Measured PTC curve from the readout chain detailed in Chapter 6. The main information that can be extracted from a PTC curve is indicated in the figure.

corresponds to the readout noise.

4.2 Dark Current Shot Noise

The leakage current due to thermally generated carriers determines a nonzero output for a total absence of light. The so-called dark current, I_{dark}, generally expressed as the number of electrons per second or as a current density per unit area of the PPD device, is often problematic because it corrupts the signal value and limits the maximum integration time of the sensor, t_{int}. Even though this undesirable phenomenon depends on several different design aspects (e.g. the technology, layout, electrical or mechanical stresses and metal contacts), the device's active and/or passive cooling was for many years the only effective solution to substantially decrease it, exploiting the exponential dependence with temperature [13]. However, modern imagers embedding PPD devices have lowered the dark current to typical values in the order of a few $e^- \cdot s^{-1} \cdot \mu m^{-2}$ (or $pA \cdot cm^{-2}$) at room temperature.

The physical model commonly used to explain the dark charge generation is the trap-assisted generation-recombination, which is based on additional energy states in the bandgap introduced by impurities. These energy levels in fact facilitate the transition of a mobile charge from the conduction to valence band.

Fig. 4.5 shows the different dark current sources located respectively at (1) the level of the depleted area of the PPD, (2) the field free bulk area, (3) the surface and (4) the interface with different materials. Since the density of charge traps increases with impurities and process defects, every interface is a potential source of dark current (e.g. the TG Si-SiO_2 and shallow

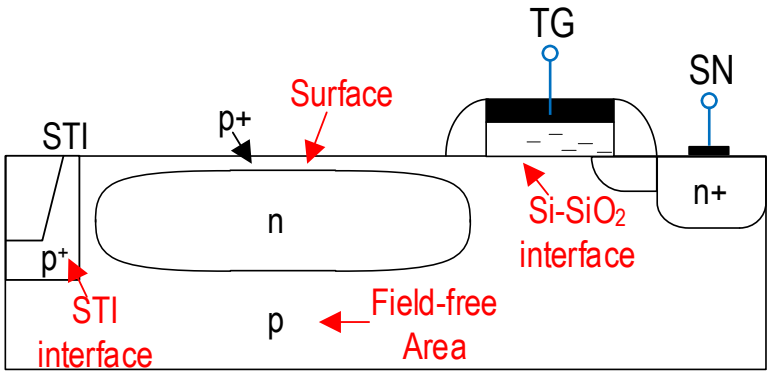


Figure 4.5: Cross-section of the PPD together with the TG and the SN. The main sources of dark current are shown: the STI interface, the field-free area, the surface states and the interface between the semiconductor and the oxide.

trench isolation (STI) interfaces). Dark current centers can be located in depleted regions, where the electric field will move the charges towards the photodetectors, and in field-free regions, where a diffusion process will take place.

The DCSN is the statistical variation of the dark current value resulting in a shot noise component. When described by Poisson statistics, the DCSN variance after integration, σ_D^2, is equal to the average number of electrons generated in the dark inside the PPD for a given integration time, N_D. The latter can be expressed as the product of I_{dark} and t_{int}. The resulting expression is also divided by the elementary charge, q , to express the signal as a number of electrons. The DCSN variance is therefore given by

$$\sigma_D^2 = N_D = \frac{I_{dark} \cdot t_{int}}{q}, \tag{4.8}$$

4.3 Charge Transfer Noise

When the photogenerated charges are transferred from the PPD to SN, the transfer can be incomplete and affect the signal with an additional noise component. The efficiency of charge transfers have already been extensively studied for CCDs [13] and growing importance is reported in ultra-low noise CISs working at sub-electron noise levels [7].

The main sources of CTI in PPDs are shown in Fig. 4.6 and include (1) the internal diffusion inside PPD, (2) the potential barrier at the interface, (3) the charge trapping due to interface states and (4) the spill-back from the SN to the PPD [1]. Even though it is not easy to measure the impact of each event, some phenomena are more important than others according to the device geometry and the transfer time.

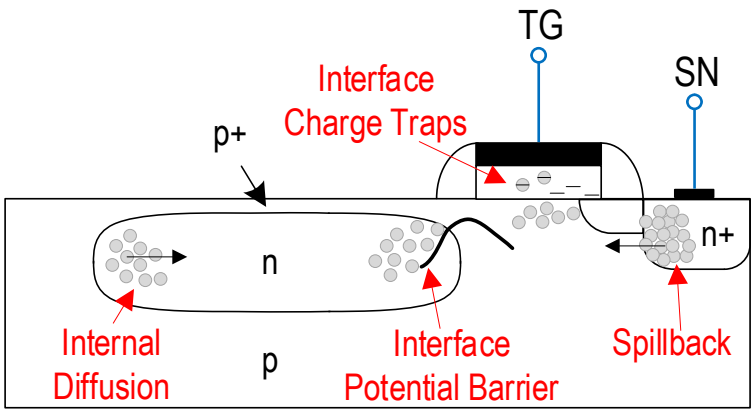


Figure 4.6: Cross-section of the PPD together with the TG and the SN. The main sources of CTI are numbered as follows: (1) the diffusion inside PPD, (2) the potential barrier at the interface, (3) the charge trapping at interface states and (4) the spillback.

The diffusion speed of electrons moving from the extremities of the PPD to the interface with the TG can limit the charge transfer in large PPDs and is crucial in devices with a length greater than a few tens of µm [19]. Process-level techniques are exploited to obtain an internal electric field that allows electrons to drift towards the TG and accelerate the transfer [11].

The potential barrier at the interface between the PPD and the region beneath the TG, $V_b(t)$, is described as the main cause of CTI in PPDs with a length of a few µm [19]. Its presence slows down the charge transfer preventing the full charge transfer from being arbitrarily fast. In addition, once the TG pulse is lowered some charges located at the center of the transfer path can go back to the PPD [10, 23].

At very long transfer times, the CTI is limited by charge trapping at the Si-SiO_2 interface of the TG [1]. The positive voltage applied to the TG attracts the electrons to the interface: when the TG voltage is high, the charge traps may become activated with trapped electrons until the voltage goes down. Other possible charge traps, for example surface and bulk, are less important in modern CMOS processes due to the presence of the pinning layer in a PPD.

Finally, when the PPD or the SN accumulate an overly-high number of photoelectrons or the SN reset voltage is too low, a reverse current or spill-back from the SN to the PPD can occur. A correct sizing of the SN capacitance can lower this phenomenon [21].

The CTI quantifies the percentage of charges left in the potential well of the PPD after each readout, and is defined as the average residual charge normalized with respect to the total charge stored in the PPD before the transfer, Q_{PPD}. It is expressed in [19] as

$$CTI = 1 - \frac{Q_{out}}{Q_{PPD}} \tag{4.9}$$

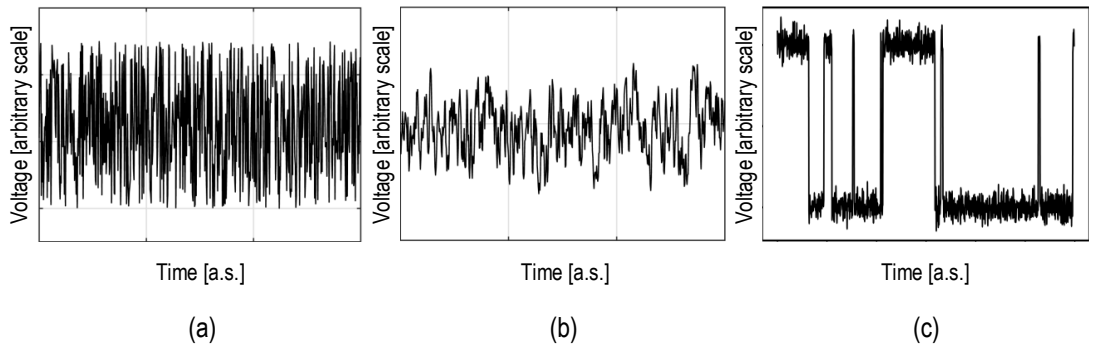


Figure 4.7: Simulated waveforms with a dominant thermal noise in (a), only 1/f and thermal noise in (b) and a dominant RTS noise in addition to thermal noise in (c).

where Q_{out} is the equivalent number of charges measured at the output. This formula is used to evaluate the quantity in technology computer-aided design (TCAD) and in Montecarlo simulations in order to define the impact of the geometrical, physical and design parameters [19].

Similarly to buried-channel CCDs [13], the charge transfer noise variance behaves as a shot noise [7] and its variance, σ_T^2, is given by

$$\sigma_T^2 = CTI \cdot N. \tag{4.10}$$

In modern CIS based on 4T pixels, values of CTI as low as 0.1% have been reported. Thus the charge transfer noise is usually lower than readout noise in ultra-low light CIS.

4.4 Readout Noise

The readout noise refers to the fluctuations injected into the signal at the level of the readout circuit and include the thermal, 1/f (or flicker), random telegraph signal (RTS) and shot noise associated with the leakage current noise.

Fig. 4.7 shows three simulated waveforms, where one of these sources is dominant: in (1) the thermal noise is characterized by fast fluctuations, in (2) the 1/f by slow fluctuations and in (3) the RTS switching between two or more voltage levels. The mechanism behind each noise source is briefly explained in order to derive the noise PSD.

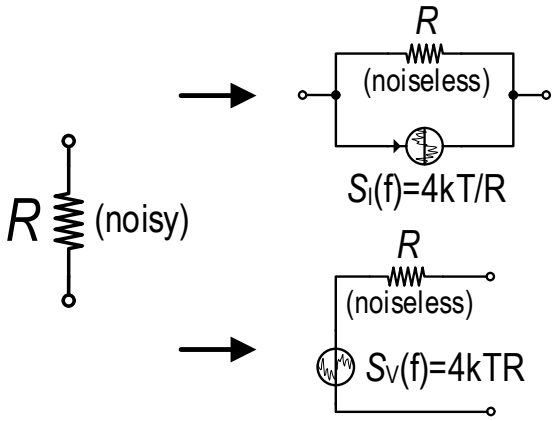


Figure 4.8: Equivalent circuit for thermal noise in a resistor: noise current generator in parallel to the resistor and noise voltage in series.

4.4.1 Thermal Noise

Thermal Noise in Resistors

Thermal or Johnson–Nyquist noise is a fundamental physical phenomenon observed in all conducting devices at a positive absolute temperature and independently of the conducting device material. It originates from the fluctuation of the charge carriers' velocity due to thermal excitation. A simplified microscopic model of thermal noise consists in assimilating the carriers in a conducting device to a Maxwell-Boltzmann idealized gas where particles exchange energy only by mutual collisions or thermally and the resulting random motion is called Brownian.

By applying the equipartition theorem [5], the unilateral expression of the current thermal noise PSD crossing the resistance R is expressed as

$$S_{\mathrm{I}}(f) = \frac{4kT}{R} \cdot \frac{1}{1+(2\pi f \tau_c)^2}, \tag{4.11}$$

where τ_{c} is the relaxation time related to the collisions. For conventional electronic circuits $f\tau_c << 1$, which simplifies the expression into *4kT/R*. The corresponding voltage fluctuation has a PSD given by

$$S_{\mathrm{V}}(f) \approx 4kTR, \tag{4.12}$$

and a noise variance, σ_V^2, expressed as

$$\sigma_V^2 = 4kTR\Delta f, \tag{4.13}$$

where Δf is the bandwidth. As shown in Fig. 4.8, the thermal noise of a resistor is modeled at the circuit level by a noise current source in parallel to the ideal resistor, with a current noise

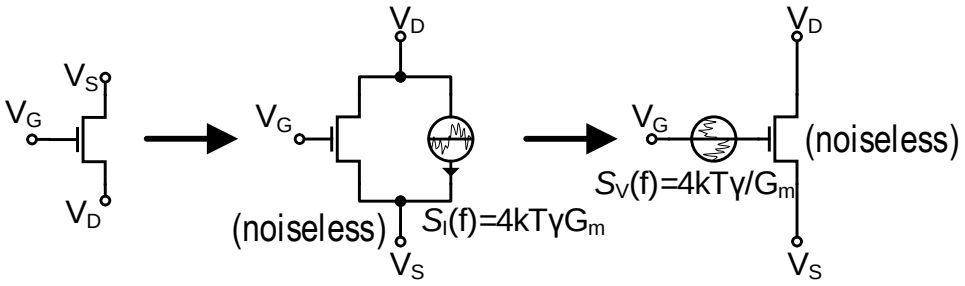


Figure 4.9: Equivalent circuit for noise of a MOS transistor: noise current generator between drain and source of the transistor and noise voltage referred to the gate.

PSD of $\frac{4kT}{R}$ or a series voltage source with a noise PSD of $4kTR$.

Thermal Noise in MOS transistors

In the EKV model [5], the thermal noise is derived by considering each slice Δx of the MOS transistor channel to have a local resistance, ΔR, and a noise current source δI_n^2 to model the thermal noise contribution. The total current noise PSD is obtained by integrating the noise contribution of each slice over the entire MOSFET channel, leading to the following expression for the current PSD

$$S_{I_D}(f) = 4kT\gamma G_m, \tag{4.14}$$

where G_m is the gate transconductance of the transistor and γ is defined as the thermal noise excess factor and shows how much noise is generated at the drain for a given G_m. The latter is given by

$$\gamma = \begin{cases} \frac{n}{2} & \text{in weak inversion and saturation,} \\ \frac{2n}{3} & \text{in strong inversion and saturation,} \end{cases} \tag{4.15}$$

where n is the EKV model parameter named the slope factor [5].

4.4.2 Reset or kTC Noise

The kTC noise is the uncertainty of charge stored on a capacitor after charging (or discharging) through a resistor. The resistive component in fact generates a thermal noise responsible for the charge fluctuation.

An RC circuit and its equivalent for noise are shown in Fig. 4.10. A voltage noise source, V_n, with a PSD equal to $4kTR$ is used to model the thermal noise of the resistor. The noise variance

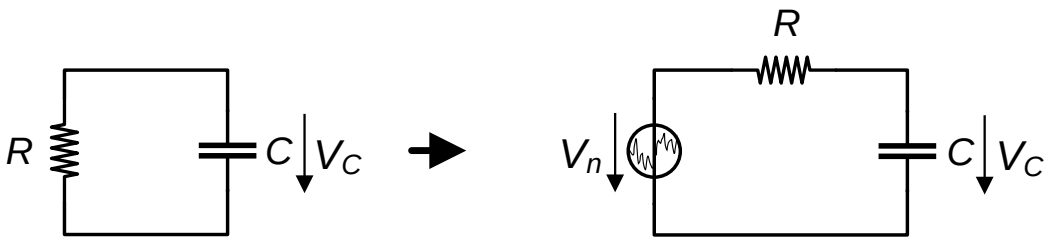


Figure 4.10: RC circuit in (a) and equivalent circuit for noise calculation in (b).

of the charge stored on the capacitor, $\overline{Q_C^2}$, can be calculated as

$$\overline{Q_C^2} = C^2 \cdot \overline{V_C^2} = C^2 \cdot \int_0^\infty \frac{4kTR}{1+(2\pi fRC)^2} = C^2 \cdot \frac{kT}{C} = kTC, \tag{4.16}$$

where V_C is the voltage across the capacitor. The noise spectrum is low-pass filtered by the RC circuit and the total output noise is independent of the value of R. Larger values of R determines at the same time a higher noise per unit bandwidth and a lower circuit bandwidth, canceling each other in the total integrated noise.

The kTC noise is often called reset noise in a CIS and expressed in terms of number of electrons by using the expression $\sqrt{kTC}/q$. At room temperature and for typical values of C_{SN} , the kTC is very large (tens of electrons) and compromises the overall image sensor. The CDS is the fundamental technique used to cancel the kTC noise in CISs.

4.4.3 Flicker Noise

In addition to thermal noise, a MOS transistor also exhibits flicker or 1/f noise, which is characterized by a PSD inversely proportional to frequency and which dominates at low frequency. Because the flicker noise scales inversely proportional to the gate area, it is a major issue in modern integrated circuit (IC) design. The most obvious technique to reduce this low-frequency noise is to increase the gate area at the expense of higher capacitances, which require a higher current to maintain the same performances. There are three 1/f noise models: Mc Worther's model based on carrier number fluctuations [16], Hooge's model based on mobility fluctuations [17], and the Berkley unified model [12]. The current PSD is derived in all models by relating the fluctuations of the channel carriers' number or mobility to the drain current.

In McWhorter's model, the 1/f noise origin is the fluctuation of the number of conduction carriers due to the trapping/de-trapping phenomenon at the Si-SiO_2 interface. The normalized

PSD of 1/f noise is given by [8]

$$\frac{S_{I_D}(f)}{I_D^2} = \frac{k^\star}{f} \frac{2}{C_{ox}^2 \cdot W \cdot L} \frac{1}{(V_{GS} - V_{th})^2}, \tag{4.17}$$

where I_D is the bias current, $k^\star$ a coefficient that defines the possibility of tunneling between channel and gate oxide traps [4], C_{ox} the oxide capacitance, W and L the transistor width and length, respectively, V_{GS} the gate-source voltage and V_{th} the threshold voltage.

In Hooge's model, the mobility fluctuations of the mobile charges at the level of the bulk is considered the 1/f noise origin. The mobility gives an average velocity of carriers in response to an electric field, and its variance can be related to a Brownian-motion or to variances in scattering. The normalized PSD of 1/f noise of a transistor biased in the saturation region, due to mobility fluctuations, is given by

$$\frac{S_{I_D}(f)}{I_D^2} = \frac{\alpha_H}{f} \frac{2q}{C_{ox} \cdot W \cdot L} \frac{1}{(V_{GS} - V_{th})}, \tag{4.18}$$

where q is the elementary charge and α_H the Hooge's parameter [8].

The Berkley unified model and EKV consider both phenomena as the origin of 1/f noise, with the scattering-induced mobility fluctuation correlated to the trapped or surface charges near the Si-SiO_2 interface. In the EKV model, the gate-referred noise expression for flicker noise is expressed as

$$S_{V_g}(f) = \frac{1}{f} \frac{K_\mathrm{G} \cdot k \cdot T \cdot q^2 \cdot \lambda N_\mathrm{t}}{C_{ox}^2 \cdot W \cdot L}, \tag{4.19}$$

where K_G is a bias-dependent parameter close to unity when the transistor is operating in the weak and moderate inversion regime and increases with the inversion coefficient, I_C [5], λ is the tunneling attenuation distance (≈ 0.1 nm) [9] and N_t the oxide trap density.

4.4.4 RTS Noise

When the process of capture and release of carriers is due to a single trap, the resulting fluctuations are commonly named as RTS noise. As shown in (4.20), this noise manifests itself as a drain current switching between two or more discrete values. Technology scaling is responsible for MOS transistors with deep sub-micron gate widths and lengths featuring single traps.

When a single trap is considered, the MOS transistor drain current switches between two states denoted as capture and release, respectively. As explained in [2], they are characterized by two relaxation times, τ_c and τ_r, with a uniform probability density per unit time to switch from one state to the other. The transitions between capture and release states cause the number of trapped carriers, $N(t)$, to switch between 0 (in release state) and 1 (in capture state). The bias

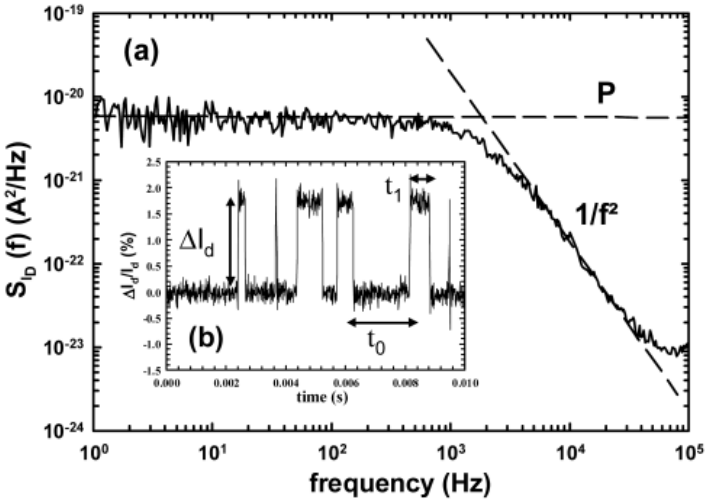


Figure 4.11: RTS noise PSD with Lorentzian shape and corresponding drain current fluctuations in the time domain for a small-area MOSFET (reprinted from [15]).

voltage dependence of this phenomenon allows the distance of the channel from the traps to be measured [3].

By expressing the autocorrelation of this random process and using the Wiener-Khinchin theorem [18], it is possible to derive the RTS current noise PSD, $S_{RTS}(f)$, due to a single trap as

$$S_{RTS}(f) = \frac{P}{1+\left(\frac{f}{f_{RTS}}\right)^2} = \frac{4A\Delta I_d^2 \cdot \tau_{RTS}}{1+(2\pi f \tau_{RTS})^2}, \tag{4.20}$$

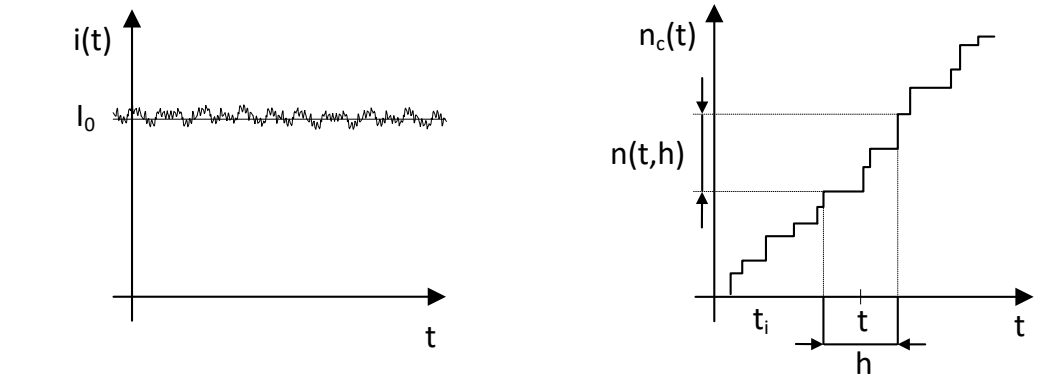
where P is the constant plateau, $f_{RTS} = 1/2\pi\tau_{RTS}$ the corner frequency, A the loading factor related to the trap occupation probability given in [15] and τ_{RTS} the characteristic time constant. The term τ_{RTS} is given by

$$\frac{1}{\tau_{RTS}} = \frac{1}{\tau_c} + \frac{1}{\tau_r}, \tag{4.21}$$

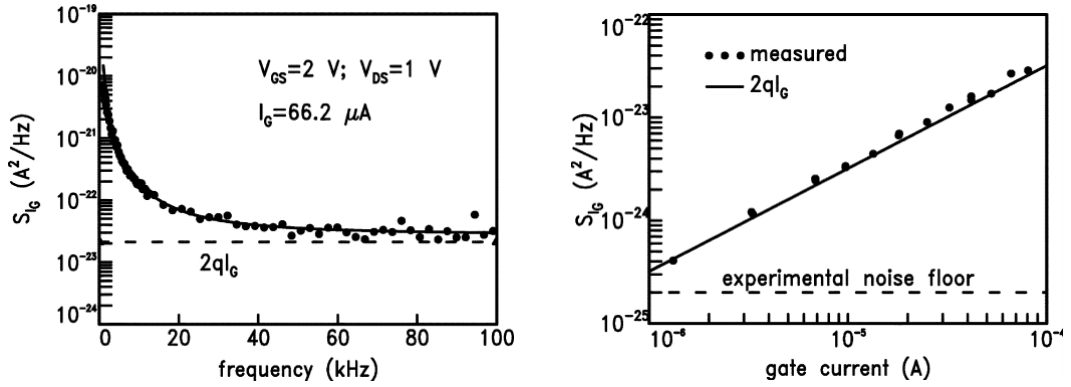
while the associate RTS noise PSD or so-called Lorentzian spectra is shown in (4.20).

The RTS is considered as a possible microscopic origin of 1/f noise. The PSD of the noise caused by all the traps in the silicon oxide can in fact be obtained by integrating (4.20) over all the energies, E, and τ_c in the gate oxide volume. Assuming a uniform spatial and energy distribution of the traps between two depths in the oxide, the resulting total noise PSD density per unit area of the gate oxide results into

$$S_{\Sigma RTS}(f) = k \cdot T \cdot \lambda \cdot N_t \cdot \frac{2}{\pi} \cdot \frac{\arctan\left(2\pi f \tau_2\right) - \arctan\left(2\pi f \tau_1\right)}{f} \approx \frac{k \cdot T \cdot \lambda \cdot N_t}{f}. \tag{4.22}$$



(a)



(b)

Figure 4.12: Impact in (a) on a steady current of the shot noise and evolution in time of the number of cumulated charge carriers crossing the barrier (reprinted from [6]). In (b), noise spectrum and as a function of measured gate current of a MOSFET in 100 nm (reprinted from [22]).

where λ is the tunneling attenuation distance (≈ 0.1 nm [9]), N_t the oxide trap density (typical values in the range of 10^{16} to 10^{17} eV^{-1} m^{-3} at room temperature) and $\tau_{1/2}$ are the capture time constant corresponding to the two depth levels. When frequencies inside the interval defined by the two time constants are considered in (4.22), the noise PSD becomes proportional to 1/f.

4.4.5 Leakage Current Shot Noise

When an independent and discrete-number of charge carriers cross a potential barrier due to two adjacent different materials, a fluctuation in the steady current appears, called shot noise, as shown in Fig. 4.12(a)(left). Since charges have a quantized nature, as discussed for the PSN, the number of particles per unit time crossing the barrier follows a Poisson process and its variance is therefore given by the average number.

As shown in Fig. 4.12(a)(right), charge carriers cross the barrier between the regions of the device at random instants t_i and the time evolution of the number of cumulated charge

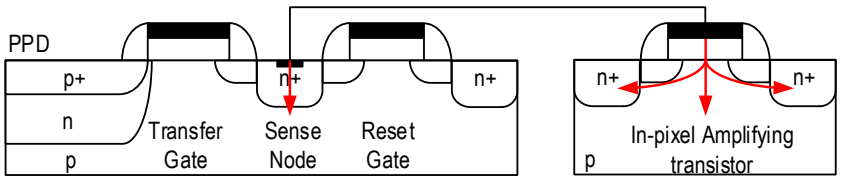


Figure 4.13: Gate leakage current components flowing between the SF terminals.

carriers crossing the barrier, $n_c(t)$, shows a behavior similar to the drunk man walk [18].

Following a Poisson statistics, the number of charges crossing the barrier at an instant t and during a period h can be expressed [2]. This allows the autocorrelation of the current to be calculated and used in order to define the bilateral noise PSD when h goes to zero, given by

$$S_I(f) \approx 2 \cdot q \cdot I_0, \tag{4.23}$$

where I_0 is the mean current crossing the device.

An experimental verification of the white noise spectrum of the gate current for a 100 nm technology is shown in [22] and reported in Fig. 4.12(b). When the white noise level is plotted against the DC gate current, the theoretical expression in (4.23) well predicts the observed noise levels, demonstrating the shot noise of the gate leakage current.

The SN in CIS is sensitive to the leakage current from depleted regions or through insulators. As shown in Fig. 4.13, two main leakage current mechanisms can be distinguished at the level of the SN: one is the generation-recombination of the pn junctions connected to the SN (similar to dark current generation in PPDs), and the other the charge tunneling through the gate oxide of the readout transistor which has a small thickness in modern CMOS processes. While the first flows between the SN and the bulk, the second separates in three components flowing between the gate and each one of the other terminals.

These leakage currents correspond to individual charge carriers crossing a barrier between two materials and result in a shot noise. As explained earlier, the shot noise variance is directly linked to the leakage current mean value. As reported in [2], the simulated average leakage current at the level of the SN for technology nodes above 130 nm and a readout time of 10 µs is negligible (below $0.001e^-$). As shown later in this manuscript, in more advanced technologies the leakage current increases by several orders of magnitude and the leakage current shot noise can become dominant.

4.5 Fixed Pattern Noise

The noise sources presented above are random fluctuations in time, also called temporal noise. As shown in Fig. 4.14, in order to measure this noise a number of frames equal to k are collected and the standard deviation, $\sigma_{temp,j}$, is computed for the j-th pixel, as follows

$$\sigma_{temp,j} = \sqrt{\frac{1}{k} \cdot \sum_{i=1}^{k} \left(s_{j,i} - \mu_j\right)^2}, \tag{4.24}$$

where $s_{j,i}$ is the j-th pixel value at the i-th frame and μ_j the j-th pixel average. The average value over all the n pixels results into the pixel temporal noise value, as given by

$$\sigma_{temp} = \frac{1}{n} \cdot \sum_{j=1}^{n} \sigma_{temp,j}, \tag{4.25}$$

If the average is performed in time and the standard deviation computed across pixels, information on the variation in the spatial-domain is obtained. The formula for FPN is given by

$$\sigma_{FPN} = \sqrt{\frac{1}{n} \cdot \sum_{j=1}^{n} \left(\mu_j - \mu\right)^2}, \tag{4.26}$$

where μ is the global pixel average, thus the mean value of all pixel averages.

The pixel-to-pixel variations due to the dark current and/or gain and offset of the in-pixel amplifier cause the dark fixed-patter noise or dark signal non-uniformity (DSNU). In order to distinguish them, the temperature and exposure time are usually changed, taking advantage of the fact that the in-pixel amplifier is practically independent of these two factors. The spatial variation is random from chip to chip but correlated in time for each chip, which means that it can be compensated by image post processing (dark frame subtraction).

The opposite of the DSNU is the light fixed patter noise or photon response non-uniformity (PRNU), which originates from pixel-to-pixel photon response non uniformities and column-level spatial variations. The first can be traced to spatial variations of the PPD QE, pinning voltage and FWC.

As shown in [2], the light FPN variance, σ_F^2, can be defined by a gain and an offset term, and rewritten as

$$\sigma_F^2 = \sigma_{CG}^2 \cdot N^2 + \sigma_{V_{off}}^2, \tag{4.27}$$

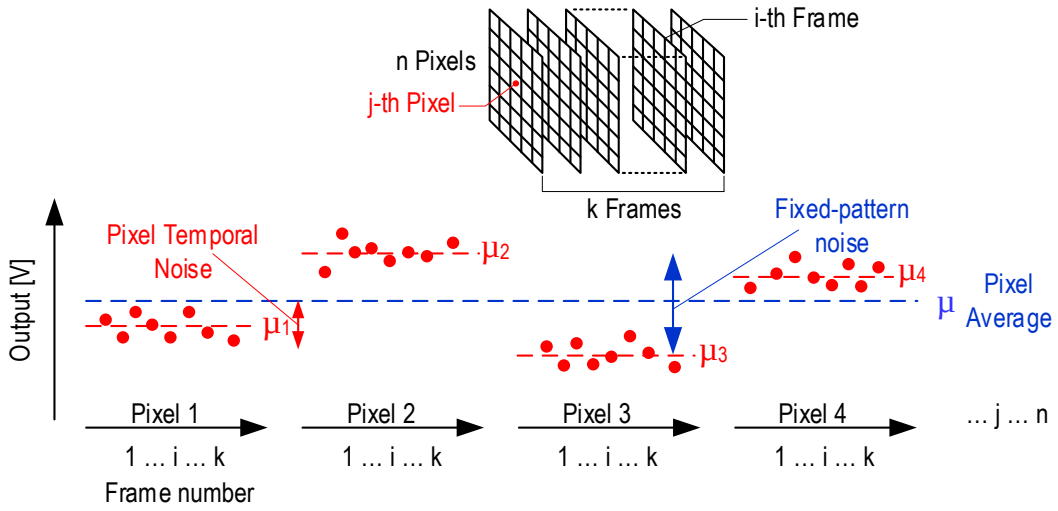


Figure 4.14: Measurement methodology for Temporal and Fixed Pattern Noise (adapted from [24]).

The spatial gain standard deviation, σ_{CG}, is expressed as

$$\sigma_{CG} = \sqrt{\frac{\sigma^2(CG)}{CG^2}} \tag{4.28}$$

and includes a column and a pixel-to pixel gain mismatch.

The vertical gain mismatch originates from the gain variation of the CLAs and results in vertical lines on the image, towards which the human eye is very sensitive. Since small feedback components are used in order to implement high gain levels, the gain spatial variation in a switched-capacitor CLA is mainly due to capacitors mismatch. Typical values of this mismatch standard deviation are of the order of 0.1% [20].

The pixel-to-pixel gain mismatch is the pixel conversion factor mismatch and, unlike the previous one, is not visually distinguishable from the PSN and TRN. The main sources are the SN capacitance variation together with the RST and TG overlap capacitances [5]. Typical values of this standard deviation are of the order of 0.5% [20].

The main sources of offset are the in-pixel transistors and the CLA. CDS and CLA auto-zeroing efficiently reduce the offset of the in-pixel SF as well as the CLA. An offset can also be generated by the nonidealities (clock feed-through and charge injection) of the switches connected to the SN.

The injected charge, ΔQ, at the SN can be generally expressed as

$$\Delta Q = \frac{C_{ov} \cdot C_{SN}}{C_{ov} + C_{SN}} \Delta V_G \approx C_{ov} \Delta V_G, \tag{4.29}$$

where C_{SN} is the total SN capacitance, C_{ov} the overlap or coupling capacitance between the

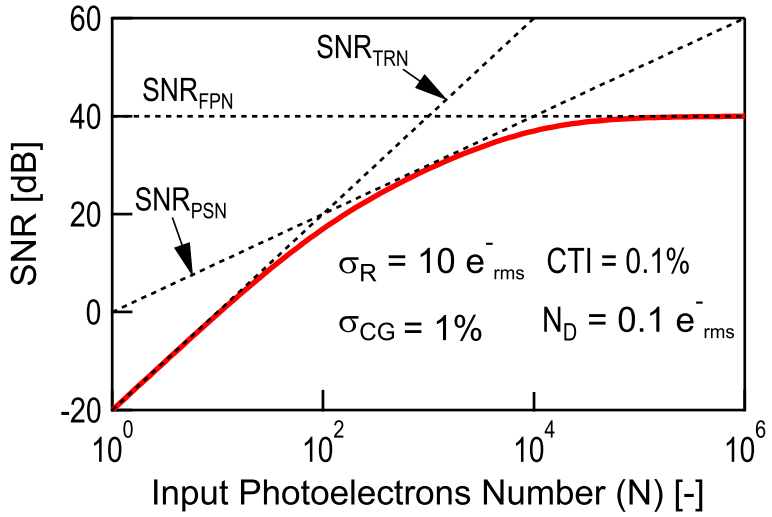


Figure 4.15: Plotted in red, the total SNR as a function of the input photoelectrons number, N. In dashed lines, the SNRs which take into account only the TRN, the PSN and the FPN. These lines show the range of photoelectrons where each noise source is dominant.

TG or RST transistor and the SN, and ΔV_G the pulse amplitude applied at the level of the transfer or reset gates.

Since the charge injected by the TG at the rising edge is compensated by the one injected during the opposite transition and that of the RST is canceled by CDS, the offset variations are neglected compared to these of the gain.

4.6 Signal-to-Noise Ratio in CIS

To evaluate the role of each noise source in different applications, the signal-to-noise ratio (SNR) can be expressed as

$$SNR = 10\log\left[\frac{N^2}{\sigma_{\mathrm{Sh}}^2+\sigma_{\mathrm{D}}^2+\sigma_{\mathrm{T}}^2+\sigma_{\mathrm{F}}^2+\sigma_{\mathrm{R}}^2}\right], \tag{4.30}$$

where N is the average number of photoelectrons stored in the PPD, σ_{Sh}^2 the PSN variance, σ_{D}^2 the DCSN variance, σ_{T}^2 the transfer noise variance, σ_{F}^2 the FPN variance and σ_{R}^2 the total input-referred read noise, which includes the thermal, 1/f and shot noise contributions generated by the readout circuit and can be assumed to be signal independent.

Fig. 4.15 shows the SNR as a function of the photoelectron number N, for typical values of $N_{\mathrm{D}} = 0.1\, e^-_{rms}$, a CTI of 0.1% and a $\sigma_{\mathrm{CG}} = 1\%$ for the FPN. σ_{R} is assumed to be equal to $10\, e^-_{rms}$ in Fig. 4.15 and the definitions given in this chapter for each signal-dependent noise are used.

The SNR which includes only the TRN is named SNR_{TRN}, and, in the same way, SNR_{PSN} is introduced for the PSN and SNR_{FPN} for the FPN. These quantities are plotted in dashed lines to highlight the contribution of each noise source in different ranges of illumination. The figure shows that the signal-dependent noise sources dominate the noise at high signal level, the PSN at mid range and the FPN at higher signal levels, whereas at low signal level the TRN is the dominant noise source. This shows the importance of minimizing the TRN for low light imaging.

4.7 Summary

Image sensors deal with many different types of noise characterized by various physical mechanisms and statistical properties. In order to show the important role of the temporal readout noise in ultra-low light CIS, this chapter provides a description of the noise sources together with their PSDs and noise variances.

It begins by showing the temporal noise sources with fluctuations in the input signal (photon shot noise), the shot noise of the dark current and charge transfer. In order to define the noise sources introduced by the readout circuits, the theories behind the thermal, flicker and shot noise are briefly recalled. To conclude, the spatial noise (or fixed pattern noise) due to the non-uniformities at the levels of pixel and column are included in the derivation. An expression for the total SNR is obtained and then evaluated for different signal values.

References for Chapter 4

[1] L. E. Bonjour, N. Blanc, and M. Kayal. Experimental Analysis of Lag Sources in Pinned Photodiodes. *IEEE Electron Device Letters*, 33(12):1735–1737, Dec 2012.

[2] A. Boukhayma. *Ultra Low Noise CMOS Image Sensors*. Springer Theses, 2018.

[3] Z. Celik-Butler, P. Vasina, and N. Vibhavie Amarasinghe. A method for locating the position of oxide traps responsible for random telegraph signals in submicron MOSFETs. *IEEE Transactions on Electron Devices*, 47(3):646–648, 2000.

[4] Wei Deng and Eric R. Fossum. 1/f noise modelling and characterization for cmos quanta image sensors. *Sensors*, 19(24):5459, Dec 2019.

[5] C.C. Enz and E.A. Vittoz. *Charge-Based MOS Transistor Modeling: The EKV Model for Low-Power and RF IC Design*. Wiley, 2006.

[6] Christian Enz. Fundamentals of Noise in Electronic Devices. *Lecture notes from Techniques for Handling Noise and Variability in Analog Circuits, Mead course*, 2020.

[7] Eric R. Fossum. Charge Transfer Noise and Lag in CMOS Active Pixel Sensors. In *Proceedings IEEE Workshop Charge-Coupled Devices and Advanced Image Sensors*, 2003.

[8] Tze-Ching Fung, Gwanghyeon Baek, and Jerzy Kanicki. Low frequency noise in long channel amorphous In–Ga–Zn–O thin film transistors. *Journal of Applied Physics*, 108:074518 – 074518, 11 2010.

[9] G. Ghibaudo. Low-frequency noise and fluctuations in advanced CMOS devices. *Proc. SPIE*, 5113:16–28, May 2003.

[10] L. Han, S. Yao, and A. J. P. Theuwissen. A Charge Transfer Model for CMOS Image Sensors. *IEEE Transactions on Electron Devices*, 63(1):32–41, Jan 2016.

[11] S. Han, T. Takasawa, K. Yasutomi, S. Aoyama, K. Kagawa, and S. Kawahito. A Time-of-Flight Range Image Sensor With Background Canceling Lock-in Pixels Based on Lateral Electric Field Charge Modulation. *IEEE Journal of the Electron Devices Society*, 3(3):267–275, May 2015.

[12] K. K. Hung, P. K. Ko, C. Hu, and Y. C. Cheng. A unified model for the flicker noise in metal-oxide-semiconductor field-effect transistors. *IEEE Transactions on Electron Devices*, 37(3):654–665, 1990.

[13] J.R. Janesick. *Scientific Charge-Coupled Devices*. SPIE Press, 2001.

[14] J.R. Janesick. *Photon Transfer*. SPIE Press, 2007.

[15] C. Leyris, F. Martinez, M. Valenza, A. Hoffmann, J. C. Vildeuil, and F. Roy. Impact of Random Telegraph Signal in CMOS Image Sensors for Low-Light Levels. In *2006 Proceedings of the 32nd European Solid-State Circuits Conference*, pages 376–379, 2006.

[16] A. L. McWhorter. *1/f Noise and Related Surface Effects in Germanium*. PhD Thesis, MIT, Cambridge, MA, USA, 1955.

[17] Hooge F. N. 1/f is no surface effect. In *Physics Letter A*, volume 29, pages 139–140. Elsevier, March 1969.

[18] Athanasios Papoulis and S. Unnikrishna Pillai. *Probability, Random Variables, and Stochastic Processes, Fourth Edition*. McGraw Hill, 2002.

[19] Alice Pelamatti. *Estimation and Modeling of Key Design Parameters of Pinned Photodiode CMOS Image Sensors for High Temporal Resolution Applications*. PhD thesis, Université de Toulouse, 2015.

[20] D Sackett. Cmos pixel device physics. In *2005 ISSCC Advanced Circuit Design Forum: Characterization of Solid-State Image Sensors*, 2005.

[21] M. Sarkar, B. Buttgen, and A. J. P. Theuwissen. Feedforward Effect in Standard CMOS Pinned Photodiodes. *IEEE Transactions on Electron Devices*, 60(3):1154–1161, March 2013.

[22] A. J. Scholten, L. F. Tiemeijer, R. van Langevelde, R. J. Havens, A. T. A. Zegers-van Duijnhoven, and V. C. Venezia. Noise modeling for RF CMOS circuit simulation. *IEEE Transactions on Electron Devices*, 50(3):618–632, 2003.

[23] Seiji Takahashi, Yi-Min Huang, Jhy-Jyi Sze, Tung-Ting Wu, Fu-Sheng Guo, Wei-Cheng Hsu, Tung-Hsiung Tseng, King Liao, Chin-Chia Kuo, Tzu-Hsiang Chen, and et al. A 45 nm Stacked CMOS Image Sensor Process Technology for Submicron Pixel. *Sensors*, 17(12):2816, Dec 2017.

[24] Albert Theuwissen. Noise: You Love It or You Hate it! *Solid-State Circuits Society*, 2018. Available on:https://resourcecenter.sscs.ieee.org/webinars/SSCSWEB3030.html. Accessed on June 2020.

5 Readout Noise Analysis in Ultra-Low Noise CIS

In the previous chapter, the dominant role of the readout noise is proven to be the bottleneck for sensitivity at ultra-low light level. A noise analysis is presented in this chapter for conventional ultra-low noise CIS readout chains based on an in-pixel SF amplifier, a CLA and a CMS block. The various noise sources that affect the signal are considered in a small-signal equivalent circuit, which allows to derive the input-referred charge noise variances for thermal, flicker and leakage current shot noise. The pixel, CLA and CMS transfer functions for the signal and noise are used in order to propagate all noise PSDs to the output, which are then input-referred by dividing by the square magnitude of the overall transfer function. The derived expressions are fundamental for evaluating the impact of the process and design parameters on the overall noise performance.

5.1 Ultra-Low Noise Readout Chains

The conventional analog readout chain for ultra-low noise CIS based on a 4T-pixel is shown in Fig. 5.1(a) with the timing diagram of the control and output signals in Fig. 5.1(b). On the left part of Fig. 5.1(b), a cross-sectional view of the PPD, TG and RST is shown in order to draw the corresponding hydraulic model for different readout steps.

The chain is composed of a 4T pixel followed by a switched-capacitor CLA and a CDS/CMS block. In this work, a SF amplifier is used inside each pixel in order to take advantage of the large voltage swing and the robustness against the reset switch nonidealities and process spatial variations [1]. As shown in the complete block diagram in Fig. 2.8, after the stage for correlated sampling, a column-parallel analog-to-digital conversion is performed. The outputs of the various ADCs are shifted in an horizontal shift register in order to have a single digital output for the image sensor. The noise analysis presented here focuses on the analog part of the readout chain and, due to the presence of the high-gain CLA, the noise contributions of the ADC and output buffers can be neglected [2].

First, the sensor integration time, T_{int}, starts when the PPD is reset by applying a positive

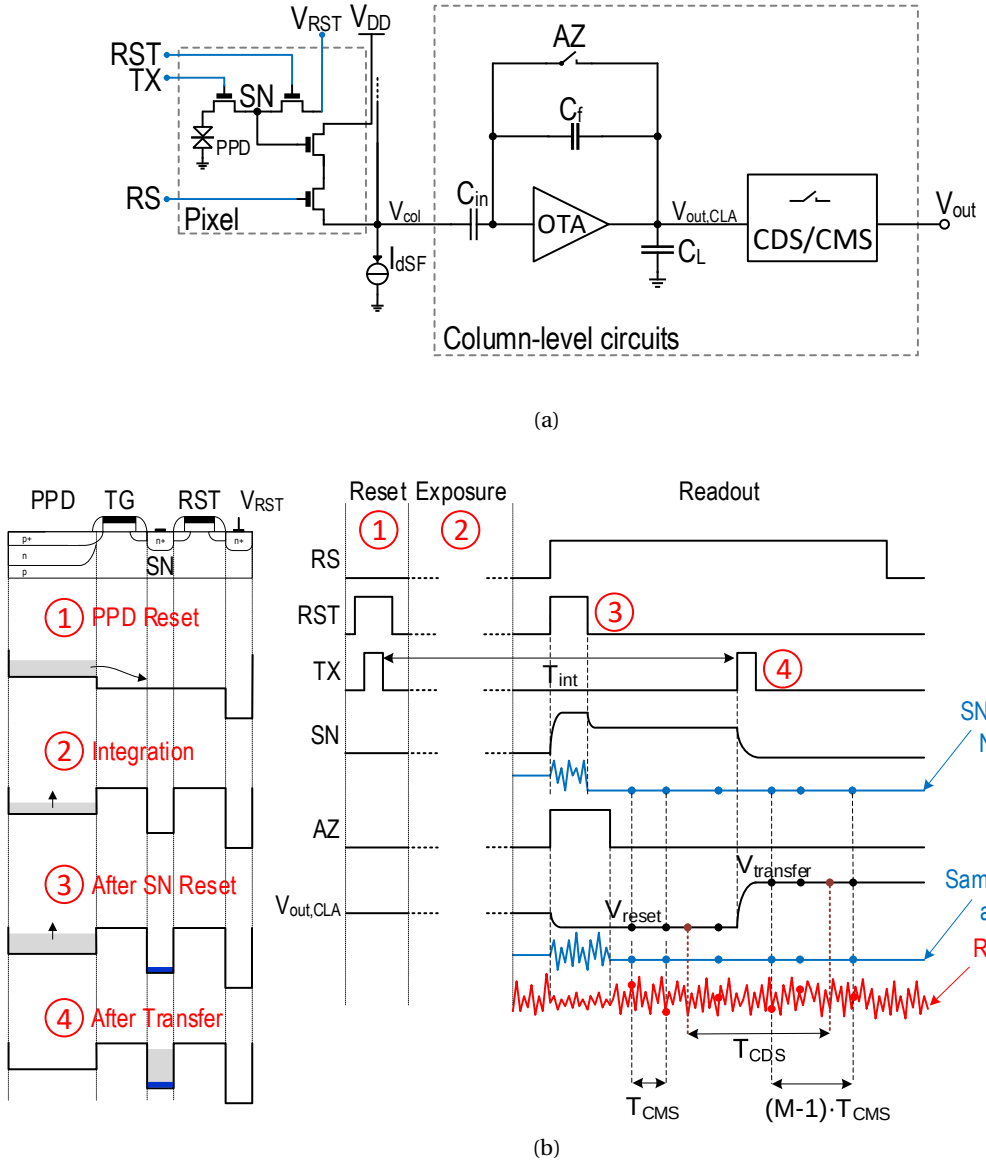


Figure 5.1: Conventional CIS readout chain based on a intra-pixel source-follower amplifier in (a). Timing diagram of a low noise CIS readout chain in (b) with the noise contributions added to the signal. On the left, hydraulic model of a PPD with TG, SN and RST showing different readout steps.

pulse to both the TG and RST transistors. The stored charges are in fact drained out of the photodiode thanks to the high voltage, V_{RST} , applied to the PPD. After the exposure phase, where the PPD is storing the photogenerated charges, the readout operations can take place. The pixel is selected during the entire readout by the high value of the RS signal. A pulse on RST allows to set the SN voltage to V_{RST}, while an AZ operation is performed on the CLA. The AZ allows the feedback capacitor, C_f , to be reset and a voltage value including the offset and low frequency noise of the amplifier itself to be stored on the input capacitance of the

amplifier, C_{in} [3]. Once stored, this value is subtracted from the signal applied at the input. This is a simple and common way to reduce the offset and the low frequency fluctuations in a voltage amplifier stage [3]. The output of the pixel is connected to the column line, which connects to the input of the CLA. The latter introduces a certain amount of voltage gain in order to increase the overall conversion gain, *CG*, which is also fundamental to decrease the impact of the blocks following the amplifier on the input-referred noise [2]. After the SN and the output of the amplifier are settled, the first sample, V_{reset}, of a CDS can be stored.

At the end of the light integration time, the photogenerated electrons in the PPD are transferred to the SN by applying a pulse to TX. When the SN and the amplifier settle to a value proportional to the amount of transferred charges, a second sample of the output, $V_{transfer}$, is stored. The difference between these two samples is performed and the obtained value is passed to the following stage. Thanks to the correlated sampling operation, the *kTC* noise sampled at the SN after the reset operation can be canceled. In fact, both samples involved in the difference embed the same frozen *kTC* component [4].

The timing diagram also depicts the noise sources corrupting the signal during the readout, while the effects of the dark current and incomplete charge transfer are neglected. The low values reported in the literature [5] (a few e^-/s for the dark current and values as low as 0.1% for the image lag) combined with exposure times below hundreds of ms, confirm in fact the dominant role of the read noise at low light.

The noise components shown in Fig. 5.1(b) are: the *kTC* noise due to the SN reset and readout chain contributions from the pixel (in-pixel SF, noise coupling to the SN through the TG or RST lines, power supply fluctuations) and from column-level circuits. As explained earlier, the SN reset noise can be extremely high due to the low SN capacitance e.g. 18 e^-_{rms} for a C_{SN} equal to 2 fF and is canceled by the CDS operation. The CLA also reduces the noise contribution of the CDS block itself.

5.2 Noise Analysis

5.2.1 Calculation Method

In order to derive the expressions of the input-referred charge noise variances for the thermal, flicker and leakage current shot noise, a detailed noise analysis for a low noise CIS readout chain was presented in [6]. The total noise variance in a readout chain composed by a single pixel, a CLA and a generic CMS circuit is derived by calculating all the transfer functions and by defining the PSD of each noise source. In this analysis, the noise sources coming from the different devices are assumed to be statistically independent. These expressions make use of the EKV formalism, which is described in [7] and are fundamental to evaluate the impact of process and design parameters on CIS noise performance.

Fig. 5.2 shows the block diagram for the noise analysis where each transfer function is sketched.

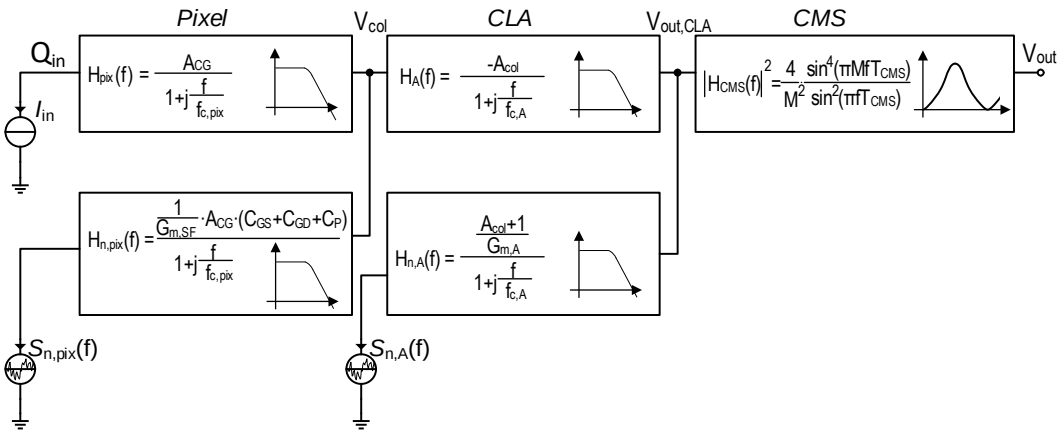


Figure 5.2: Block diagram for the noise analysis showing the signal and noise transfer functions. The expressions of the transfer functions are reported and sketched in each block.

The input signal of the CIS readout chain is modeled as a current pulse, I_{in}, which represents the charge accumulated during the integration phase and transferred to the SN when TG is pulsed. The pixel signal transfer function, $H_{pix}(f)$, relates the input charge to the column-level voltage and its DC gain is the pixel conversion gain, A_{CG} (in *V/e*$^-$). The transfer functions of the CLA and the CMS are respectively $H_A(f)$ and $H_{CMS}(f)$. The readout noise is calculated at the output as a voltage using the noise transfer functions and then is referred to the input as a charge after division by the gain of the signal path, namely the product between A_{CG} and the in-bandwidth CLA gain, A_{col}.

Thus, the variance of the input-referred noise originating from the pixel, $\overline{Q^2_{\text{n,pix}}}$, can be expressed as

$$\overline{Q^2_{\text{n,pix}}} = \frac{1}{A^2_{\text{CG}} \cdot A^2_{\text{col}}} \cdot \int_0^{\infty} S_{n,pix}(f) \cdot |H_{n,pix}(f)|^2 \cdot |H_A(f)|^2 \cdot |H_{CMS}(f)|^2 df, \tag{5.1}$$

where $S_{n,pix}(f)$ is the current PSD of the pixel-level noise sources and $H_{n,pix}(f)$ the pixel noise transfer function, which goes from the source to V_{col} (see Fig. 5.2).

Similarly, the variance of the input-referred noise originating from the CLA, $\overline{Q^2_{\text{n,A}}}$, can be expressed as

$$\overline{Q^2_{\text{n,A}}} = \frac{1}{A^2_{\text{CG}} \cdot A^2_{\text{col}}} \cdot \int_0^{\infty} S_{n,A}(f) \cdot |H_{n,A}(f)|^2 \cdot |H_{CMS}(f)|^2 df, \tag{5.2}$$

where $S_{n,A}(f)$ is the current PSD of the column-level noise sources and $H_{n,A}(f)$ the noise transfer function from that source to the output of the CLA. Since these noise sources are independent, the total input-referred noise charge variance of the readout chain, $\overline{Q^2_{\text{n,tot}}}$, can

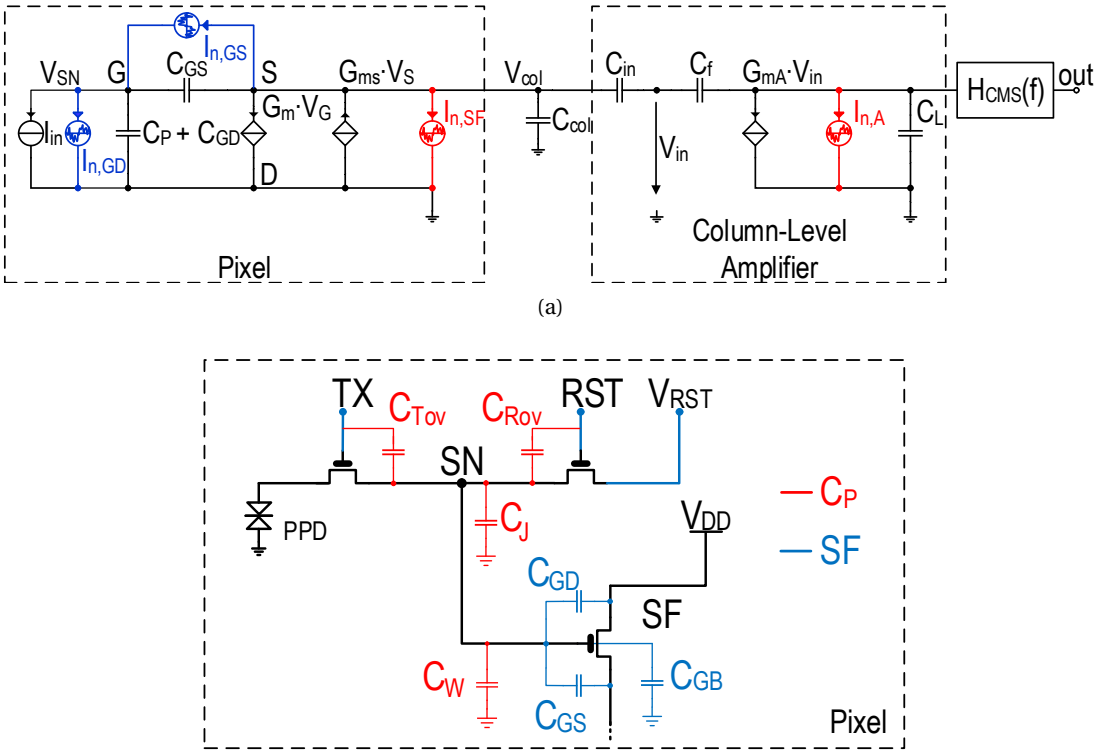


Figure 5.3: Small-signal equivalent in (a) for the CIS readout chain in Fig. 5.1(a) together with the different readout noise sources. Parasitic capacitances in (b) contributing to the SN node term C_{p}.

be expressed as

$$\overline{Q^2_{\mathrm{n,tot}}} = \overline{Q^2_{\mathrm{n,pix}}} + \overline{Q^2_{\mathrm{n,A}}}. \tag{5.3}$$

5.2.2 Signal Transfer Functions

Based on the small-signal circuit in Fig. 5.3(a), the signal transfer functions can be derived. The pixel transfer function is given by

$$H_{\mathrm{pix}}(f) = \frac{V_{col}}{Q_{in}} = \frac{A_{CG}}{1 + j\frac{f}{f_{c,pix}}}, \tag{5.4}$$

where $Q_{\mathrm{in}} = j \cdot 2\pi f I_{in}$, and

$$f_{\mathrm{c,pix}} = \frac{1}{2\pi} \frac{G_{m,SF}}{C_{col} \cdot A_{CG} \cdot (C_{GS} + C_{GD} + C_P)}, \tag{5.5}$$

is the cut-off frequency of the in-pixel SF stage, C_{col} the column-level capacitance, C_{GS} and C_{GD} the gate-to-source and gate-to-drain SF capacitances, and n is the slope factor of the SF. When the SF is biased in saturation, the latter is equal to the ratio between the source transconductance, $G_{ms,SF}$, and gate transconductance, $G_{m,SF}$ [7]. C_{p} is the sum of the parasitic capacitances at the SN shown in Fig. 5.3(b) and is defined in [1] as

$$C_P = C_{Tov} + C_{Rov} + C_J + C_W, \tag{5.6}$$

where C_{Tov} and C_{Rov} are the overlap capacitances of the TG and RST gates, C_J the SN junction capacitance and C_W the parasitic capacitance related to metal wires.

The conversion gain corresponds to the DC gain of the pixel transfer function $H_{pix}(f)$ and is given by

$$A_{CG} = \frac{\frac{1}{n}}{C_P + C_{GD} + \left(1 - \frac{1}{n}\right) C_{GS}}. \tag{5.7}$$

This expression can be further detailed assuming the SF is biased in strong inversion (SI), by expressing the capacitances C_{GD} and C_{GS} in terms of the SF gate size and oxide capacitance density per unit area, C_{ox}, resulting in

$$A_{CG} = \frac{\frac{1}{n}}{C_P + C_e \cdot W + \left(1 - \frac{1}{n}\right)\left(C_e \cdot W + \frac{2}{3} C_{ox} \cdot WL\right)}, \tag{5.8}$$

where C_e is the extrinsic capacitance per unit width of the in-pixel SF transistor and consists of the overlap and the fringing field capacitances.

Regarding the CLA, since the noise frozen on C_{in} after auto-zeroing is transferred to C_f and to the output during the amplification phase and canceled by the CDS, only the direct output noise during the amplification phase needs to be considered for the noise calculation. Moreover, since $A_{col} \ll \frac{G_{m,A}}{g_{out,A}}$, where $G_{m,A}$ and $g_{out,A}$ are the transconductance and the output conductance of the column-level OTA in Fig. 5.1(a), the column-level gain is given by $A_{col} = \frac{C_{in}}{C_f}$. The transfer function of the CLA when the AZ switch is opened can be derived from the small-signal circuit shown in Fig. 5.3(a) and is given by

$$H_A(f) = \frac{-A_{col}}{1 + j\frac{f}{f_{c,A}}}, \tag{5.9}$$

where

$$f_{c,A} = \frac{1}{2\pi} \frac{G_{m,A}}{(A_{col} + 1)C_L + C_{in}}. \tag{5.10}$$

The zero in the transfer function given by the input capacitor and equal to $\frac{1}{2\pi} \frac{A_{col} \cdot G_{m,A}}{C_{in}}$ is much higher than $f_{c,A}$ and its impact has been neglected.

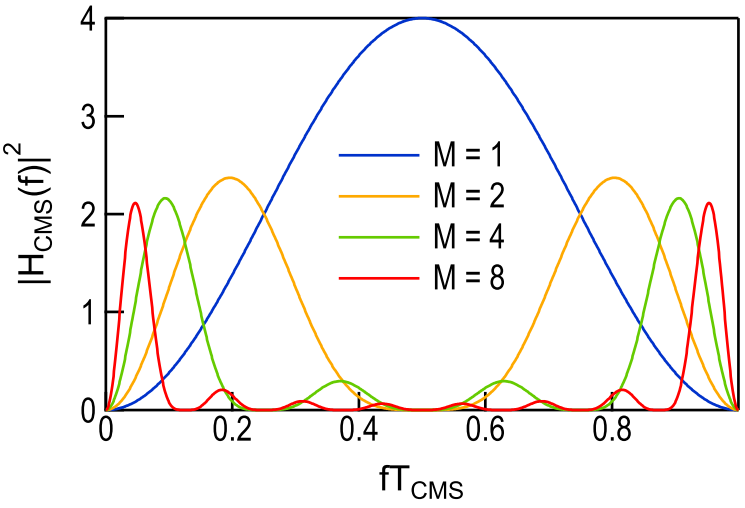


Figure 5.4: The term $|H_{\mathrm{CMS}}(f)|^2$ as a function of the frequency normalized to the CMS sampling period T_{CMS}, for four different values of the CMS order.

The CMS output is the difference between the reset level, V_{reset}, and the signal level, V_{transfer}, averages, and can be expressed as

$$V_{\mathrm{CMS}} = \frac{1}{M}\sum_{i=1}^{M} V_{\mathrm{transfer,i}} - \frac{1}{M}\sum_{i=1}^{M} V_{\mathrm{reset,i}}. \tag{5.11}$$

A detailed analysis of the analog CMS has been derived in [1, 8] giving the PSD of the analog CMS output noise as

$$S_{\mathrm{n,CMS}}(f) = \sum_{n=-\infty}^{+\infty} |H_{\mathrm{n}}(f)|^2 \cdot S_{\mathrm{n}}\left(f - \frac{n}{2MT_{\mathrm{CMS}}}\right), \tag{5.12}$$

where $|H_{\mathrm{n}}(f)|^2$ is given by

$$|H_{\mathrm{n}}(f)|^2 = sinc^2(\pi f \cdot 2MT_{\mathrm{CMS}}) \cdot \left|H_{\mathrm{CMS}}\left(f - \frac{n}{2MT_{\mathrm{CMS}}}\right)\right|^2. \tag{5.13}$$

and $sinc(x) = sin(x)/x$ accounts for the hold of each sample over a full period $2M \cdot T_{\mathrm{CMS}}$. The square magnitude of the CMS transfer function $|H_{\mathrm{CMS}}(f)|^2$ in (5.13) is given by

$$|H_{\mathrm{CMS}}(f)|^2 = \left(\frac{2}{M}\right)^2 \cdot \frac{\sin^4(\pi f \cdot M \cdot T_{\mathrm{CMS}})}{\sin^2(\pi f \cdot T_{\mathrm{CMS}})}, \tag{5.14}$$

which is plotted in Fig. 5.4 versus the normalized frequency $f \cdot T_{\mathrm{CMS}}$ for different values of M ranging from 1 to 8.

The variance of the CMS output voltage is obtained by integrating the PSD given by (5.12) over

frequency. Thanks to power conservation in the CMS circuit, it is shown in [1] that this integral is actually equal to the integral of the signal before sampling, resulting in

$$\int_{-\infty}^{+\infty} S_{\mathrm{n,CMS}}(f) = \int_{-\infty}^{+\infty} |H_{\mathrm{CMS}}(f)|^2 \cdot S_{\mathrm{n}}(f)\, df. \tag{5.15}$$

This means that the CMS output variance only depends on the square magnitude of the CMS transfer function (5.13) and the input noise PSD $S_{\mathrm{n}}(f)$. For a white noise input PSD, the CMS output variance is therefore proportional to the area below the curves shown in Fig. 5.4.

The impact of CMS on thermal and 1/f noise variances has first been investigated in [4], as early as 1982 and for CDS ($M = 1$). The same year, in [9] the noise reduction techniques were studied in CCD, extending the work in [4] to various implementations and to $M > 1$. In 2005, the PSD of the noise at the output of a digital CMS were derived in [10].

5.2.3 Noise Transfer Functions

Based on the small-signal circuit in Fig. 5.3(a) and the derivation shown in [1], the noise pixel transfer function to the output column-level is given by

$$H_{\mathrm{n,pix}}(f) = \frac{\frac{1}{G_{m,SF}} A_{CG} \cdot (C_{GS} + C_{GD} + C_P)}{1 + j\frac{f}{f_{c,pix}}}, \tag{5.16}$$

while the noise transfer function for the CLA referred to its output is given by

$$H_{n,A}(f) = \frac{\frac{A_{col}+1}{G_{m,A}}}{1 + j\frac{f}{f_{c,A}}}. \tag{5.17}$$

5.2.4 Noise Analysis Results

By combining the signal and noise transfer functions with the expression of the noise PSDs as defined in (5.1) and (5.2), it is possible to obtain the analytical expression for the noise variances.

Thermal Noise

The total input-referred noise charge variance for the thermal noise is

$$\overline{Q_{\mathrm{th}}^2} = \alpha_{\mathrm{th}} \cdot \frac{k\,T}{A_{\mathrm{col}}\,C}\left[\frac{\gamma_{\mathrm{SF}}\, G_{\mathrm{mA}}(C_P + C_{GD} + C_{GS})^2}{G_{\mathrm{mSF}}} + \frac{\gamma_{\mathrm{A}}}{A_{\mathrm{CG}}^2}\right], \tag{5.18}$$

where k is the Boltzmann constant, T the temperature expressed in Kelvin; C is equal to $C_{\mathrm{L}} + C_{\mathrm{in}}/(A_{\mathrm{col}} + 1)$, where C_{L} is the amplifier load capacitance, γ_{SF} and γ_A are the excess noise

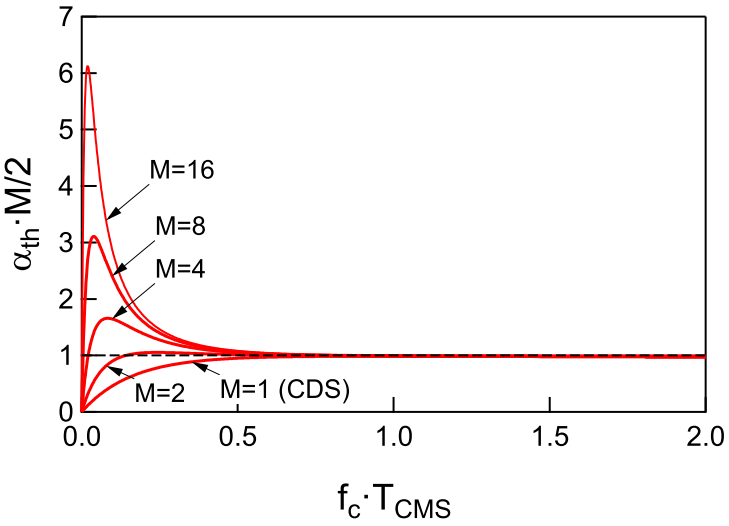


Figure 5.5: The parameter α_{th} is multiplied by $M/2$ and plotted as a function of $f_c \cdot T_{\text{CMS}}$ for different values of M.

factors of the in-pixel SF stage (including the amplifier and load transistors) and the CLA [7].

In [1], (5.18) is expressed under the assumption that the SF is a long-channel transistor biased in SI [7], resulting in

$$\overline{Q_{\text{th}}^2} = \alpha_{\text{th}} \cdot \frac{k\,T}{A_{\text{col}} \cdot C} \left[\frac{\gamma_{\text{SF}}\, G_{\text{mA}} \left(C_{\text{p}} + \frac{2}{3} C_{\text{ox}} WL + 2\, C_{\text{ex}} W \right)^2}{G_{\text{mSF}}} + \frac{\gamma_{\text{A}}}{A_{\text{CG}}^2} \right], \tag{5.19}$$

where W and L are the SF width and length, respectively.

The impact of the CMS process on thermal noise is evaluated in (5.19) with the help of the parameter α_{th}. A low-pass filtered white noise with a bandwidth f_c is given by

$$S_{\text{n}}(f) = S_{\text{n,th}}(f) = \frac{S_0}{1 + \left(\frac{f}{f_c}\right)^2}. \tag{5.20}$$

α_{th} is defined as the CMS output noise variance $V_{\text{n,CMS,th}}^2$ due to this white noise, normalized to the total white noise power at the input $\pi f_c \cdot S_0$

$$\alpha_{\text{th}} \triangleq \frac{V_{\text{n,CMS,th}}^2}{\pi f_c \cdot S_0} = \frac{2}{\pi f_c} \int_0^\infty \frac{|H_{\text{CMS}}(f)|^2}{1 + \left(\frac{f}{f_c}\right)^2}\, df. \tag{5.21}$$

Eq. (5.21) can be integrated analytically for $M = 1$, resulting in

$$\alpha_{\text{th}}|_{\text{M=1}} = 2e^{-\pi f_c \cdot T_{\text{CMS}}} \cdot \sinh(\pi f_c \cdot T_{\text{CMS}}) \tag{5.22}$$

and for $M = 2$, leading to

$$\alpha_{\text{th}}|_{\text{M=2}} = \frac{1}{2} e^{-6\pi f_c \cdot T_{\text{CMS}}} \cdot \left[e^{4\pi f_c \cdot T_{\text{CMS}}} \cdot \left(1 + 4\sinh(2\pi f_c \cdot T_{\text{CMS}})\right) - 1 \right]. \tag{5.23}$$

Unfortunately, no simple closed-form expressions can be obtained for $M \geq 3$ and (5.21) needs to be computed numerically, which shows that α_{th} is actually proportional to $2/M$. Indeed, the factor 2 comes from the subtraction of two uncorrelated averages and the factor $1/M$ is due to the noise averaging in each half period of the CMS process.

This property is illustrated in Fig. 5.5 which shows the product $\alpha_{\text{th}} \cdot M/2$ versus $f_c \cdot T_{\text{CMS}}$ for different values of M ranging from 1 to 16. As expected, $\alpha_{\text{th}} \cdot M/2$ tends to unity for $f_c \cdot T_{\text{CMS}} > 1/2$ and for all values of M.

As shown in Fig. 5.4, the area delimited by $|\text{H}_{\text{CMS}}(\text{f})|^2$ reduces when increasing the value of M, hence the thermal noise variance at the output of the CMS is inversely proportional to M. This clearly illustrates quantitatively the reduction of the thermal noise thanks to the noise averaging provided by the CMS process.

Flicker Noise

On the other hand, the input-referred 1/f noise charge variance leads to the following expression

$$\overline{Q_{1/\text{f}}^2} = \alpha_{1/\text{f}} \cdot \frac{K_{\text{F}} \left(C_{\text{p}} + C_{\text{GD}} + C_{\text{GS}}\right)^2}{{C_{\text{ox}}}^2 \cdot W\,L}, \tag{5.24}$$

where the parameter K_{F} is expressed in [7] as

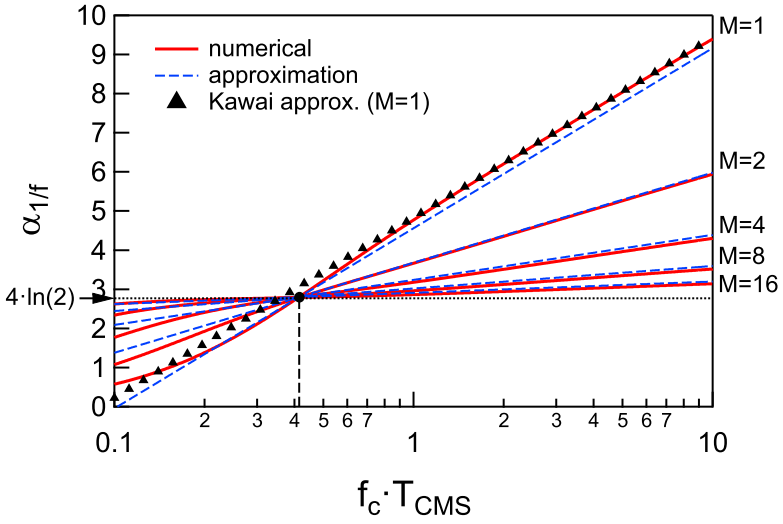
$$K_{\text{F}} = K_{\text{G}} \cdot k \cdot T \cdot q^2 \cdot \lambda\, N_{\text{t}}. \tag{5.25}$$

In (5.25), K_{G} is a bias-dependent parameter close to unity when the transistor is operating in the weak and moderate inversion [7], q the electron charge, λ is the tunneling attenuation distance (≈ 0.1 nm) [11] and N_{t} the oxide trap density.

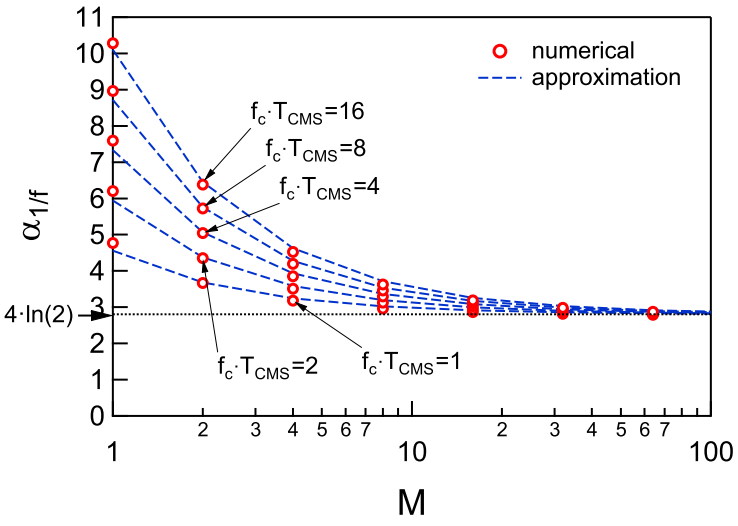
Under the assumption of a long-channel SF biased in SI, the flicker noise charge variance is expressed in [1] as

$$\overline{Q_{1/\text{f}}^2} = \alpha_{1/\text{f}} \cdot \frac{K_{\text{F}} \left(C_{\text{p}} + 2\,C_{\text{ex}}\,W + \frac{2}{3} C_{\text{ox}} \cdot W\,L\right)^2}{{C_{\text{ox}}}^2\,W\,L}. \tag{5.26}$$

The reported input-referred flicker noise variance takes only into account the dominating flicker noise contribution generated by the in-pixel SF, whereas the flicker noise of the CLA



(a)



(b)

Figure 5.6: $\alpha_{1/f}$ in (a) as a function of $f_c \cdot T_{CMS}$ for different values of M. The same parameter is plotted in (b) as a function of M to emphasize the plateau of the residual flicker noise reduction with M.

featuring larger devices can be neglected [3].

Based on Fig. 5.4, the CMS has a high-pass characteristic since it introduces a zero in the transfer function which cancels the 1/f noise. However, the maximum of $|H_{CMS}(f)|^2$ decreases and at the same time moves to lower frequencies when increasing M.

In order to evaluate the impact of CMS on the 1/f noise, the parameter $\alpha_{1/f}$ is defined and numerically calculated for different values of M. A low-pass filtered 1/f noise has a PSD given

by

$$S_{\mathrm{n,1/f}} = \frac{K_{\mathrm{f}}}{|f|} \cdot \frac{1}{1+\left(\frac{f}{f_c}\right)^2}. \tag{5.27}$$

The parameter $\alpha_{1/\mathrm{f}}$ is defined as

$$\alpha_{1/\mathrm{f}} \triangleq \frac{V^2_{\mathrm{n,CMS,1/f}}}{K_{\mathrm{f}}} = \int_0^\infty \frac{1}{f} \cdot \frac{|H_{\mathrm{CMS}}(f)|^2}{1+\left(\frac{f}{f_c}\right)^2} df, \tag{5.28}$$

where $V^2_{\mathrm{n,CMS,1/f}}$ is the CMS output variance due to the low-pass filtered 1/f input noise. There is unfortunately no simple closed-form expression for the integral given by (5.28).

The latter has been computed numerically and is plotted in Fig. 5.6(a) versus $f_{\mathrm{c}} \cdot T_{\mathrm{CMS}}$ for different values of M ranging from 1 to 16. Choosing a log scale for the x-axis in Fig. 5.6(a) shows that $\alpha_{1/\mathrm{f}}$ actually scales linearly with $\ln(2\pi f_{\mathrm{c}} \cdot T_{\mathrm{CMS}})$ for $f_{\mathrm{c}} \cdot T_{\mathrm{CMS}} > 4.15$ and that the slope is inversely proportional to M. A simple approximation of (5.28) in the case of CDS ($M = 1$) was proposed in [9] and [10] as

$$\alpha_{1/\mathrm{f}} \cong 2\gamma + 2\ln(2\pi f_{\mathrm{c}} \cdot T_{\mathrm{CDS}}), \tag{5.29}$$

where $\gamma \cong 0.577$ is the Euler constant and T_{CDS} the time between the two CDS samples. The CDS approximation given by (5.29) is plotted in Fig. 5.6(a) with the triangle symbol which shows a good match for $f_{\mathrm{c}} \cdot T_{\mathrm{CDS}} > 1$. Unfortunately, today no simple approximation of (5.28) has been derived for $M > 1$. As already observed in [9] and [10], for very large values of M (actually $M \to \infty$), $\alpha_{1/\mathrm{f}}$ saturates to $4\ln(2) \cong 2.77$, which corresponds to the dotted horizontal line in Fig. 5.6(a). Having a closer look at Fig. 5.6(a), we see that all the curves computed numerically for $M = 1, 2, 4, 8, 16$ cross roughly at a point given by $f_{\mathrm{c}} \cdot T_{\mathrm{CMS}} \cong 4.15$ and $\alpha_{1/\mathrm{f}} = 4\ln(2) \cong 2.77$. A simple approximation can then be derived from this observation and from the fact that the lines in the lin-log plot scale as $2/M$. This results in the newly proposed approximation given by

$$\alpha_{1/\mathrm{f}} \cong 4\ln(2) + \frac{2}{M} \cdot \ln\left(\frac{f_{\mathrm{c}} \cdot T_{\mathrm{CMS}}}{0.415}\right), \tag{5.30}$$

which fits the numerical values reasonably well for M ranging from 1 to 16 as shown by the dashed lines in Fig. 5.6(a). The interesting new feature of the approximation given by (5.30) is that it captures the scaling of the 1/f noise reduction with the CMS order M as illustrated in Fig. 5.6(b) for different values of $f_{\mathrm{c}} \cdot T_{\mathrm{CMS}}$. It also shows that no substantial 1/f noise reduction is achieved when choosing M larger than 16.

Fig. 5.6(a) shows that $\alpha_{1/\mathrm{f}}$ increases logarithmically with $f_{\mathrm{c}}\, T_{\mathrm{CMS}}$ for each value of M. This means that the time between the samples should be kept at the minimum value that ensures the signal to settle ($f_{\mathrm{c}}\, T_{\mathrm{CMS}} = 1$). This figure illustrates that the residual 1/f noise can be

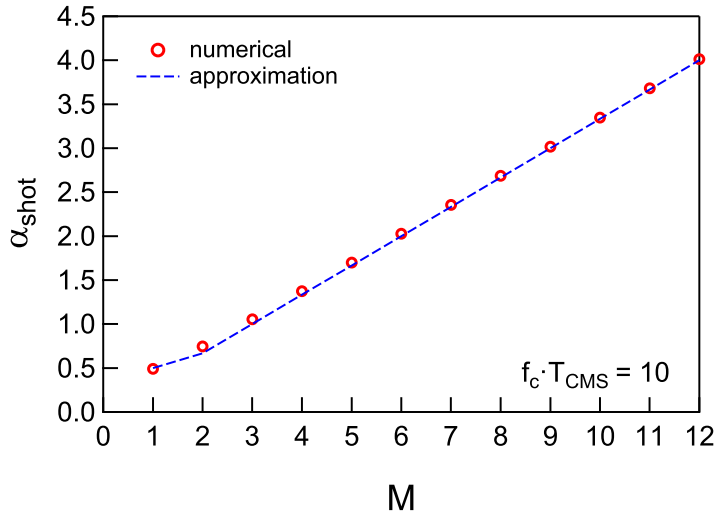


Figure 5.7: The parameter α_{shot} is plotted as a function of M.

reduced by the CMS up to $M = 16$, above which the aforementioned plateau corresponding to $4\ln(2) = 2.77$ is reached. This figure also shows that higher CMS orders make $\alpha_{1/f}$ less dependent on $f_c\, T_{CMS}$.

Leakage Current Shot Noise

As shown in the small signal equivalent of Fig. 5.3(a), the leakage current shot noise can be modeled by two noise current sources: $I_{n,GD}$ and $I_{n,GS}$ featuring the same transfer function towards the output. The former is the shot noise of all the leakage currents flowing between the SN and ground e.g. the SN junction leakage and the SF gate oxide tunneling current into the bulk and drain, while the latter is the shot noise from the SF gate oxide tunneling current that flows to the source. $I_{n,GS}$ can be split into one component from gate to drain and another from source to drain.

The pixel leakage current shot noise transfer function can hence be expressed as

$$H_{shot,pix}(f) = \frac{A_{CG}^2}{(2\pi f)^2} \frac{1}{1 + j\frac{f}{f_{c,pix}}}. \tag{5.31}$$

The input-referred charge noise variance due to the total leakage current shot noise, $\overline{Q_{\text{shot}}^2}$, can be expressed as

$$\overline{Q_{\text{shot}}^2} = 2 \cdot \alpha_{shot} \cdot q \cdot I_L, \tag{5.32}$$

where I_L is the DC leakage current and

$$\alpha_{\text{shot}} = \int_0^{\infty} \frac{1}{(2\pi f)^2} \cdot |H_{\text{CMS}}(f)|^2 \cdot \frac{1}{1+\left(\frac{f}{f_c}\right)^2} df. \tag{5.33}$$

A numerical evaluation of α_{shot} as a function of the CMS order M is shown in Fig. 5.7 together an approximation function equal to $\frac{M}{3}$ for $M \geq 2$ and to $\frac{1}{2}$ for $M = 1$.

α_{shot} is independent of the readout chain cut-off frequency and, when integrated in the SN capacitance, the white PSD of the shot noise current give rise to a Wiener process [12]. The variance of this noise is thus expected to increase linearly with the readout time, M and T_{CMS}.

Random Telegraph Signal Noise

CISs embedded in modern smartphones feature pixels with a 0.8 µm pitch [13, 14], where transistors have deep sub-micron gate widths and lengths. As explained in Section 4.4.4, discrete current fluctuations at a fixed bias condition are generally observed for these devices. This phenomenon is mainly due to the trapping of an individual carrier in a single oxide trap or to the presence of a scattering center in the proximity of an inversion layer [15]. The associated noise, named as random telegraph noise or RTS, can be described by a current noise PSD, $S_{RTS}(f)$, expressed by

$$S_{RTS}(f) = \frac{k_{RTS} \cdot \tau_{RTS}}{1 + (2\pi f \tau_{RTS})^2}, \tag{5.34}$$

where k_{RTS} is the RTS noise coefficient [16] and τ_{RTS} the characteristic time constant for a single trap.

In order to evaluate the impact of CMS on the RTS noise, the parameter α_{RTS} is defined and calculated for different values of M and the RTS corner frequency, $f_{\text{RTS}} = 1/2\pi \cdot \tau_{\text{RTS}}$. Following a similar derivation to the one used for the thermal and flicker input PSDs, a low pass filtered Lorentzian noise PSD is given by

$$S_{\text{n,RTS}} = \frac{k_{RTS} \cdot \tau_{RTS}}{1 + (2\pi f \tau_{RTS})^2} \cdot \frac{1}{1+\left(\frac{f}{f_c}\right)^2}, \tag{5.35}$$

while the parameter α_{RTS} is defined as

$$\alpha_{RTS} \triangleq 2\pi \cdot \frac{V^2_{\text{n,CMS,RTS}}}{k_{\text{RTS}}} = \int_0^{\infty} \frac{\frac{1}{f_{RTS}}}{1+\left(\frac{f}{f_{RTS}}\right)^2} \cdot \frac{|H_{\text{CMS}}(f)|^2}{1+\left(\frac{f}{f_c}\right)^2} df, \tag{5.36}$$

where $V^2_{\text{n,CMS,RTS}}$ is the CMS output variance due to the low-pass filtered RTS input noise.

The latter has been computed and plotted in Fig. 5.8 versus the CMS order, M, for different

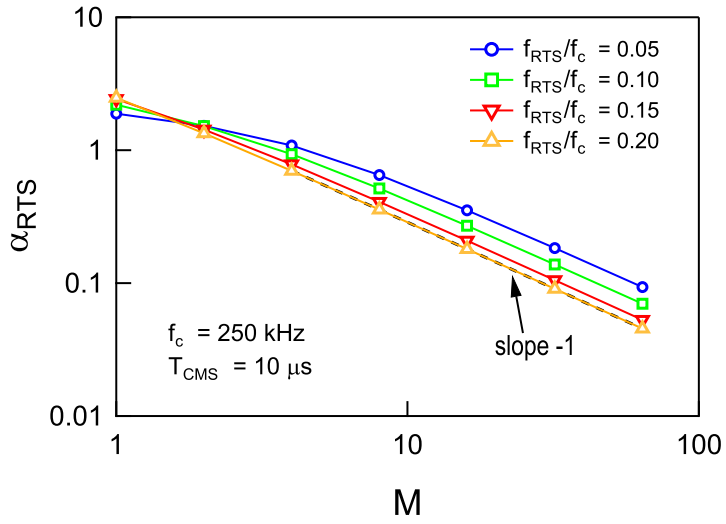


Figure 5.8: α_{RTS} as a function of M for different values of f_{RTS}/f_c.

values of f_{RTS}/f_c. Under the assumption that the CMS sampling period is longer than the characteristic time constant of the RTS trap, a noise reduction is achieved when M is increased. Choosing a log scale for the both axis in Fig. 5.8 shows that α_{RTS} scales inversely to M and the slope for the noise reduction approaches -1. Similar results for the impact of CMS on RTS have been presented in [16], while a theoretical model is compared with measurement results in [17], where it is shown that the CMS is also an efficient technique for reducing RTS noise under the above assumptions.

5.3 Summary

A readout noise analysis is shown in this chapter in order to derive the expression of the input-referred charge noise variances for thermal, flicker and leakage current shot noise. The noise PSDs are first propagated to the output and then input-referred dividing by the overall readout chain gain. The process and design parameters are then included in order to evaluate the impact of each component on the noise.

This chapter starts with the detailed description of the ultra-low noise readout chain and its corresponding timing diagram. The noise components corrupting the signal at different levels are shown together with the main signals. A small-signal equivalent circuit is used in order to derive the signal and noise transfer functions. The noise analysis results are shown separately for each type of noise.

The description of different noise reduction techniques shown in the following chapter is based on the expressions here derived.

State-of-the-Art Advancements

A detailed readout noise analysis was presented in [1], leading to the derivation of the charge noise variances reported in (5.19), (5.26) and (5.32), while the effectiveness of the CMS for reducing 1/f noise was described in [10].

In the work presented in this chapter, a newly proposed approximation of the flicker noise factor, $\alpha_{1/f}$, is given in (5.30). The latter fits the numerical values reasonably well and captures the scaling of the 1/f noise reduction with the CMS order. The proposed expression also highlights that no substantial 1/f noise reduction is achieved when choosing M larger than 16, which is a fundamental result used during the noise characterization of the low-noise readout chain described in the following chapter.

References for Chapter 5

[1] A. Boukhayma, *Ultra Low Noise CMOS Image Sensors*. Springer Theses, 2018.

[2] B. Razavi, *Design of Analog CMOS Integrated Circuits*. McGraw-Hill, first ed., 2001.

[3] C. Enz and G. Temes, "Circuit techniques for reducing the effects of op-amp imperfections: autozeroing, correlated double sampling and chopper stabilization.," *Proceedings of the IEEE*, vol. 84, no. 11, pp. 1584–1614, 1996.

[4] R. J. Kansy, "Response of a correlated double sampling circuit to 1/f noise generated in CCD arrays," *IEEE Journal of Solid-State Circuits*, vol. 15, pp. 373–375, June 1980.

[5] A. Boukhayma, A. Peizerat, and C. Enz, "A Sub-0.5 Electron Read Noise VGA Image Sensor in a Standard CMOS Process," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 9, pp. 2180–2191, 2016.

[6] A. Boukhayma, A. Peizerat, and C. Enz, "Temporal Readout Noise Analysis and Reduction Techniques for Low-Light CMOS Image Sensors," *IEEE Transactions on Electron Devices*, vol. 63, pp. 72–78, Jan 2016.

[7] C. Enz and E. Vittoz, *Charge-Based MOS Transistor Modeling: The EKV Model for Low-Power and RF IC Design*. Wiley, 2006.

[8] C. Enz and A. Boukhayma, "Recent trends in low-frequency noise reduction techniques for integrated circuits," in *2015 International Conference on Noise and Fluctuations (ICNF)*, pp. 1–6, June 2015.

[9] G. R. Hopkinson and D. H. Lumb, "Noise reduction techniques for CCD image sensors," *Journal of Physics E: Scientific Instruments*, vol. 15, pp. 1214–1222, nov 1982.

[10] N. Kawai and S. Kawahito, "Effectiveness of a correlated multiple sampling differential averager for reducing 1/f noise," *IEICE Electronics Express*, vol. 2, pp. 379–383, 07 2005.

[11] G. Ghibaudo, "Low-frequency noise and fluctuations in advanced CMOS devices," *Proc. SPIE*, vol. 5113, pp. 16–28, May 2003.

[12] A. Papoulis and S. U. Pillai, *Probability, Random Variables, and Stochastic Processes, Fourth Edition*. McGraw Hill, 2002.

[13] Y. Lee, J. Park, B. Kim, J. Kim, H. Yoo, S. Nah, D. Park, T. Lee, B. Kim, D. Keum, H. Jeong, H. Kwon, M. Kim, S. Jung, Y. Kim, C. Moon, and Y. Park, "World first mass productive 0.8um pixel size image sensor with new optical isolation technology to minimize optical loss for high sensitivity ," in *Proceedings of the 2019 International Image Sensor Workshop*, Snowbird, Utah, June 24-27, 2019.

[14] D. Jang, D. Park, S. Cha, H. Kwon, M. Kim, S. Lee, H. Lee, S. Kim, N. Lee, J. Han, D. Lee, K. Oh, M. Lee, I. Yun, H. Lee, S. Hong, Y. Kim, C.-R. Moon, and Y. Park, "0.8um-pitch CMOS Image Sensor with Dual Conversion Gain Pixel for Mobile Applications," in *Proceedings of the 2019 International Image Sensor Workshop*, Snowbird, Utah, June 24-27, 2019.

[15] E. Simoen and C. Claeys, "Random telegraph signal: a local probe for single point defect studies in solid-state devices," *Materials Science and Engineering: B*, vol. 91-92, pp. 136 – 143, 2002.

[16] S. Suh, S. Itoh, S. Aoyama, and S. Kawahito, "Column-Parallel Correlated Multiple Sampling Circuits for CMOS Image Sensors and Their Noise Reduction Effects," *Sensors*, vol. 10, no. 10, pp. 9139–9154, 2010.

[17] C. Y.-P. Chao, S.-F. Yeh, M.-H. Wu, K.-Y. Chou, H. Tu, C.-L. Lee, C. Yin, P. Paillet, and V. Goiffon, "Random Telegraph Noises from the Source Follower, the Photodiode Dark Current, and the Gate-Induced Sense Node Leakage in CMOS Image Sensors," *Sensors*, vol. 19, p. 5447, Dec 2019.

6 Noise Reduction Techniques in Ultra-Low Light CIS

In the previous chapter, the noise analysis of a single readout chain is shown in order to derive the expressions for the input-referred charge noise variances for the thermal, flicker and leakage current shot noise. Based on them, the main readout noise reduction techniques can be defined, involving process and design parameters at different levels of the readout chain. Process-level modifications and optimizations of the column-level blocks and pixel, where designers are more constrained in their choices, can be applied to reduce the thermal and 1/f noise.

This chapter describes the first analog implementation of the CMS with a passive SC circuit in a 180 nm CIS technology and shows its impact on the total input-referred noise of the readout chain when combined to the column-level gain. The schematic and timing diagram for the control signals of the SC CMS is described and followed by a charge-based noise analysis for a generic CMS order, M, which aims to prove the fixed noise contribution of this circuit equal to kT/C, regardless of the value of M. This noise analysis is supported by periodic noise (PNOISE) and transient noise simulation results. The readout chain used to evaluate this circuit technique embeds two different pixels, a programmable-gain CLA and the SC CMS. The obtained measurement results allow the further noise reduction due to this circuit to be verified and to evaluate the impact of the combination of multiple noise reduction techniques.

The effects of technology downscaling on the read noise are also investigated and the simulation results are shown for a 65 nm technology combining different circuit-level noise reduction techniques. The opportunities of noise reduction with technology downscaling are exploited and the role of the shot noise associated to the gate tunneling current is emphasized. The input-referred total noise of $0.37\,e^-_{rms}$ is obtained in ELDO transient noise simulations for a readout chain in a standard 65 nm process using only circuit techniques and optimal device choices and sizing. The simulation results have been favorably compared with analytical noise calculations and opened to opportunities of photoelectron counting in this process. When combined to CMS and a proper sizing of the SF, a sub-electron noise level is obtained in simulation results for the same technology. The obtained noise value in ELDO transient noise simulations is $0.20\,e^-_{rms}$ for a single row readout time of 43 µs.

6.1 Noise Reduction Techniques

The main noise reduction techniques are summarized in this section thanks to the derived expressions shown in (5.19) and (5.26) that allow the evaluation of the impact of design and process parameters on the input-referred readout noise.

Regarding thermal noise, at column-level it is possible to implement a high-gain amplifier and a precise bandwidth, together with a CDS or a CMS circuit. The input-referred thermal noise variance is in fact inversely proportional to the product of the column level gain, A_{col}, the capacitance C and the CMS order, M, having all equivalent impacts on the noise reduction and the readout time. Even though it negatively affects the dynamic range, the high gain reduces the bandwidth and the total integrated thermal noise, and mitigates the noise contribution of the stages following the amplifier. The noise contribution of the CLA itself is defined by its excess factor, γ_A, which can be optimized by choosing an amplifier capable to provide enough voltage gain when used in closed loop with a minimum number of transistors [1, 2]. Since the noise contributions of cascode transistors are negligible, a cascode amplifier is often used and can be further optimized by a proper ratio of the transistors' transconductances [3].

By looking at pixel-level, the term expressed in (5.19) can be reduced by a higher pixel conversion gain, A_{CG}, that can be achieved with a small SN capacitance. As explained earlier, C_{SN} includes the parasitic capacitances included in C_{p} and the SF capacitors, and its reduction can be achieved by a careful layout and using minimum size transistors [3]. The thermal noise contribution of the SF stage itself can be reduced by optimizing its excess noise factor, γ_{SF}, which is usually achieved with proper values for the transistor transconductances [3].

Once the thermal noise is minimized, the flicker noise originated from the SF becomes the dominant noise source in the readout circuit [4]. At column-level and since they are outside the pixel, the transistors can be designed with a gate area large enough in order to exhibit low flicker noise, and the CMS order can be used to have an additional noise reduction.

At pixel-level, the degrees of freedom left to designer are very much reduced. Based on (5.26), the reduction of C_P mentioned for thermal noise reduction, also decreases the input-referred 1/f noise by means of a higher pixel conversion gain.

Process improvements are able to reduce C_P in a more efficient way than layout optimizations. For example in [5], an effective reduction (about 47%) is obtained by removing the low doped drains (LDDs) used in standard CMOS transistors and by increasing the depletion depth under the floating diffusion with a lower doping concentration. In [6], a potential profile that isolates the SN from the TG (virtual phase) is used to reduce the overlap capacitance between the TG and the SN. Furthermore, the overlap between the RST gate and SN is reduced by controlling the doping profile. The higher conversion gain is obtained at the cost of a low pixel FWC and a relatively higher lag. In [7], the overlap capacitance between the TG and the SN is reduced by introducing a special implant, while the overlap capacitance between the RST and the SN is reduced by omitting the reset transistor and by using an off-chip high voltage clock of 25 V

Table 6.1: Summary Table for Noise Reduction Techniques

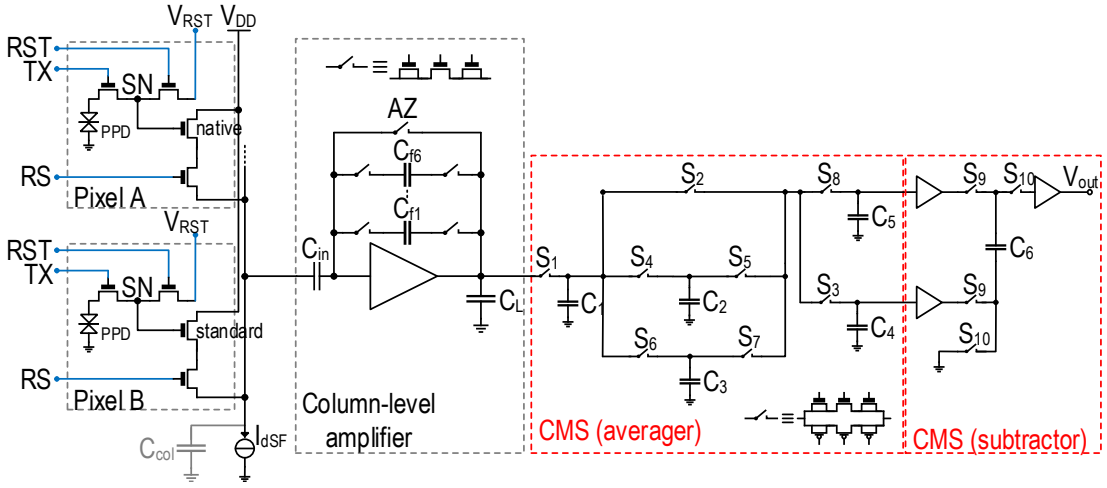
	Thermal Noise	Flicker Noise
Pixel-level Techniques	• Reduce C_{SN}	• Reduce the 1/f noise process parameter N_t • Reduce C_{SN} • Minimum W_{SF} and optimal L_{SF} • Increase C_{ox}
Column-level Techniques	• Column-level Gain • Bandwidth Limitation • CMS order M	• Large Gate Area Device • CMS order M

connected directly to an implant close to the SN, which resets the SN by a punch-through effect.

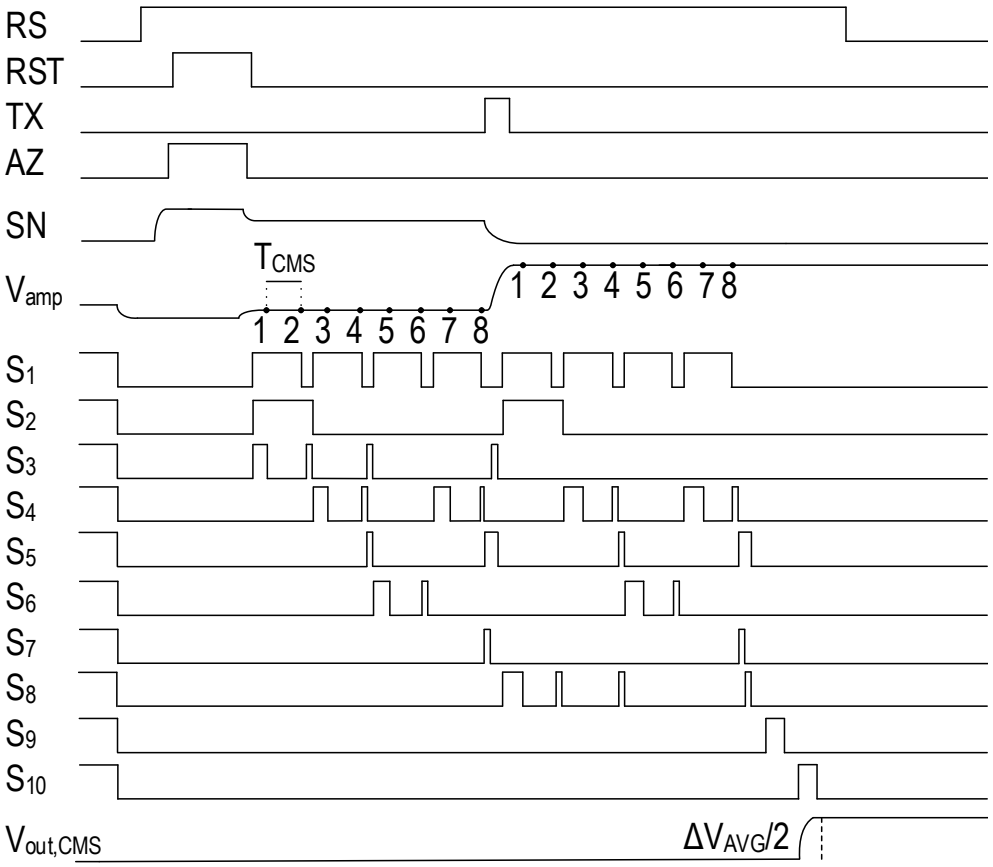
On the other hand, only pixel-level optimizations and circuit techniques are used in [8, 9]. For the SF transistor, the optimized gate dimensions, together with the highest oxide capacitance per unit area, C_{ox}, and the lowest flicker noise parameter, K_{F}, are the solutions to minimize the noise. Based on [4], the lowest input-referred 1/f noise corresponds to a minimum SF gate width and an optimal length, while a higher C_{ox} is expected to lower the noise when the SN capacitance is not dominated by C_P. In [10], a minimum width and an optimal length are shown to give the minimal 1/f noise and an in-pixel thin oxide pMOS SF is used in [11]. The process dependent parameter related to the 1/f noise mechanism is K_F which is proportional to the oxide trap density N_t and can be reduced by a device choice in the standard library or through process-level improvements. The main techniques for thermal and flicker noise reduction are summarized in Table 6.1 and separated into pixel and column-level.

6.2 Combination of SC CMS with Column-level Gain

The CMS is the only technique that is independent from the pixel design and process parameters and can further reduce the flicker noise [10]. For this reason, this work aims to precisely analyze the impact of the combination of the column-level gain and the CMS on the input-referred noise and to validate the theoretical model with measurements.



(a)



(b)

Figure 6.1: Schematic in (a) of the implemented CIS readout chain with a 4T pixel, the capacitive amplifier and SC CMS. Timing diagram in (b) of the readout chain with all the control signals for the SC CMS for M equal to 8.

6.2.1 Readout Design

The CIS readout chains used in this work embed two different pixels, a CLA and a passive SC analog CMS. The schematic and the timing diagram of the CIS readout chain are shown in Fig. 6.1(a) and Fig. 6.1(b). For the sake of simplicity, the two different pixels in the circuit schematic refer to the same readout chain, but in the actual implementation each pixel has a separate one.

Passive Switched-Capacitor CMS – Implementation and Noise Analysis

The SC CMS was introduced for the first time in [12] and takes advantage of a simple SC circuit to average the reset and the signal output samples and perform the CMS, without the need for any additional circuits, feedback loops or multiple analog-to-digital conversions. In the SC CMS, the operation of averaging is performed by taking advantage of the charge sharing principle between equal capacitors. If the initial voltages of two equal capacitors are respectively V_1 and V_2, when connected together the final voltage across them will be equal to $(V_1 + V_2)/2$. This is due to the charge sharing between the two capacitors. If M consecutive samples with a sampling period, T_{CMS}, are stored on M different capacitors, connecting them all together at the instant $M \cdot T_{CMS}$ results in averaging the M samples. As seen earlier, in a low noise CIS the two averages correspond respectively to the reset and the signal-levels, after the transfer of the photogenerated charge from the PPD to the SN [4].

If the average is calculated progressively and the intermediate results are stored in re-usable capacitors, the minimum number of capacitors can be optimized. Based on [12], $n+1$ capacitors are needed for averaging 2^n samples. Compared to more traditional CMS implementations, the proposed circuit does not need any additional active circuits.

Fig. 6.1(a) shows the implemented CMS circuit, composed of an averaging and a subtractor block. The former consists of five equal capacitors for averaging 8 samples of the reset and signal-levels, before and after the charge transfer, and to store the two averages on capacitors C_4 and C_5, respectively. The maximum CMS order of 8 is chosen according to the theoretical limit of the 1/f noise reduction, discussed in the previous chapter. The latter, based on SF buffers and a bootstrap capacitor, C_6, is used to subtract the two averages and to obtain the final output value.

The circuit is explained with the help of the timing diagram of Fig. 6.1(b), which assumes $M = 8$. Initially, switches S_1, S_2 and S_3 are closed. A first sample, V_1, is then stored in C_4 as S_3 opens. After time T_{CMS}, from the last event, S_1 is also opened to store the next sample, V_2, in C_1. After the two samples are taken, S_2 and S_3 are closed, while S_1 is opened and the first two samples are averaged, the result being held on C_4. The same operations are repeated between capacitors C_1 and C_2, as shown in the timing diagram. The average between fours samples is then stored on C_4 by closing S_3 and S_5. The two other iterations on C_3 and on C_2 allow the average of eight samples to be stored on C_4.

During the averaging of the signal-level, the charges injected by switches on C_4 and C_5 are a possible issue. It is therefore crucial to design the complementary switches with dummy transistors in series, as used in the SC CMS and shown in Fig. 6.1(a) [2].

A T_{CMS} equal to 1 µs is chosen in order to ensure the settling of the output after charge transfer and to minimize the introduced latency, and the values of 400 fF and 1 pF are used for the averaging capacitors and the bootstrap capacitor, respectively. As explained later in this chapter, the logic circuit to control the switches is implemented externally with an FPGA. Since these signals are common to all the implemented readout columns, the required additional circuit area can be considered negligible in an on-chip implementation.

SC circuits require only capacitors, switches and digital control circuits. Their main limitations are the analog switches non-idealities, the charge injection, the mismatch and the *kTC* noise. As explained in Chapter 4, the latter is the charge noise variance on a capacitor due to thermal noise, where k is the Boltzmann constant, T the temperature expressed in Kelvin and C the value of the capacitor. The theoretical estimation of this SC noise can be arduous, since these circuits are linear time-variant (LTV) systems and the noise transfer functions for each noise source have to be recalculated during each phase [13]. The result is a difficult derivation for many SC circuits.

A complete analysis of the total output noise of the SC CMS circuit is here based on a method that defines all the noise terms involved in the charge domain. A similar method was presented in [14] as an extension of the Bode Theorem applied to *RLC* networks [15] and was used for estimating the thermal noise voltage variance in SC circuits using OTAs with capacitive feedback. The thermal noise estimation method is also applied to SC filters in [16] and to a passive SC low pass filter and a N-path filter in [10].

In periodic SC networks, each capacitor can be either connected to a voltage source or to another capacitor, through a switch. When connected to a voltage source, the switch resistance, R_{on}, is responsible for the thermal noise injected into the capacitor, from which originates kT/C noise voltage variance. When connected to another capacitor, a phenomenon of charge sharing between the two components takes place. The thermal noise is an uncorrelated type of noise, hence each generated noise term is independent of the others. Each noise contribution can be considered separately, from the generation during the voltage sampling to the propagation, where all operations are ideal since no extra noise is added.

In this method, all the different phases in a SC circuit are first determined. All the noise terms are then distinguished and propagated in time through all the phases in order to be added up and obtain the final output noise variance. The derivation is first proposed for a CDS circuit and then for a CMS of order four, before a general theory is obtained. The derived analytical formulas from this analysis are verified with noise simulations performed with the Spectre® circuit simulator.

The schematic of the SC CDS is shown in Fig. 6.2, where the difference between two input

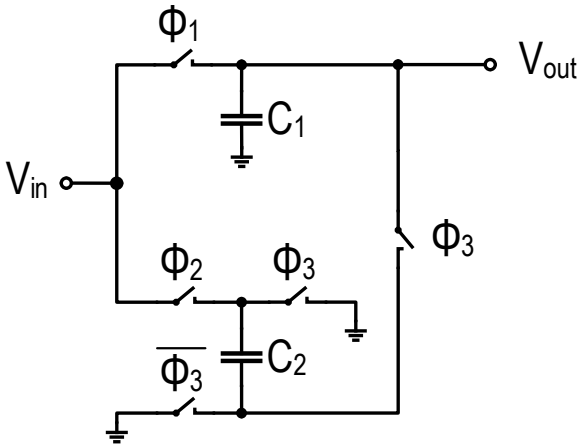


Figure 6.2: SC CDS circuit implementation.

voltage samples is implemented [17]. In this circuit, it is possible to define three phases: ϕ_1, where the first sample is stored on C_1, ϕ_2, to store the second sample on C_2, and ϕ_3, to implement the difference between the two samples.

The noise charge variance on C_1 at the end of ϕ_1, $\overline{Q^2_{\phi_1}}$, is equal to kTC_1. When expressed in terms of voltage noise variance, $\overline{V^2_{\phi_1}}$, is equal to kT/C_1. This noise value will not be influenced by ϕ_2, while in ϕ_3 the charge sharing between C_1 and C_2 will lead to

$$\overline{V^2_{\phi_1}} = \frac{\overline{Q^2_{\phi_1}}}{(C_1+C_2)^2} = \frac{kTC_1}{(C_1+C_2)^2}. \tag{6.1}$$

Similarly, the voltage noise variance due to the noise contribution generated during ϕ_2 and shared during ϕ_3, $\overline{V^2_{\phi_2}}$, can be written by swapping C_1 and C_2 in $\overline{V^2_{\phi_1}}$. Finally, the last noise contribution is generated during ϕ_3 and can be expressed as

$$\overline{V^2_{\phi_3}} = \frac{kT}{C_1+C_2}. \tag{6.2}$$

All the computed terms can be added up to give the total output noise voltage variance, $\overline{V^2_{n,out}}$, given by

$$\overline{V^2_{n,out}} = \frac{kTC_1}{(C_1+C_2)^2} + \frac{kTC_2}{(C_1+C_2)^2} + \frac{kT}{C_1+C_2} = \frac{2kT}{C_1+C_2}. \tag{6.3}$$

In the typical case where C_1 and C_2 are both equal to C is considered, the total voltage variance results in kT/C.

The schematic of the SC averager circuit for a CMS order equal to four implemented with a minimum number of capacitors is shown in Fig. 6.3(a). The minimum number of phases for sampling and averaging is equal to six (ϕ_1 to ϕ_6) and are described in Fig. 6.3(b).

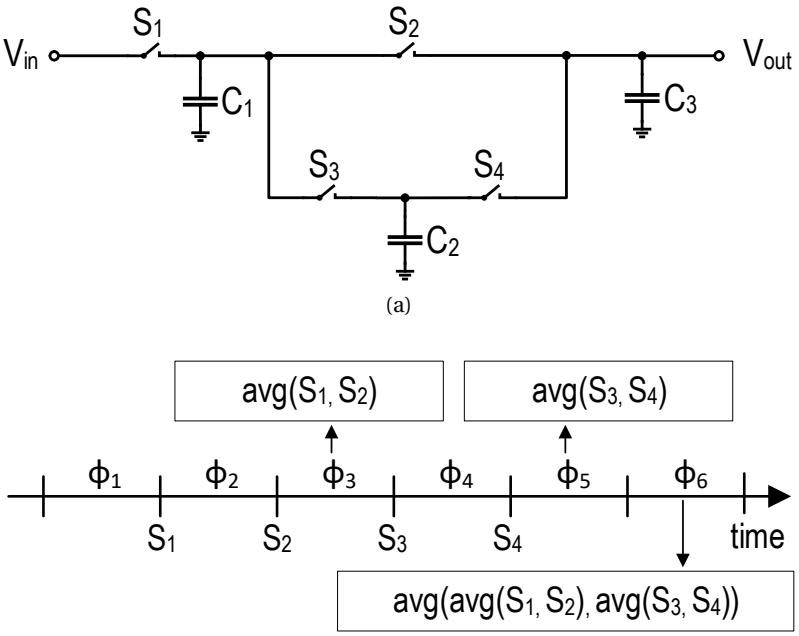


Figure 6.3: Averager circuit in (a) for a SC CMS order equal to four in a minimum number of capacitors. Timeline in (b) of the CMS $M = 4$ with all the phases and the operations for each phase.

The noise generated in ϕ_1 is equal to kT/C_3 and the charge sharing between C_1 and C_3 will determine a voltage variance equal to $kTC_3/(C_1+C_3)^2$. By multiplying the previous expression with ${C_3}^2$, it is possible to define a charge noise variance. This noise term will then go through a second operation of averaging, which will lead to the following expression

$$\overline{Q^2_{\phi_1}} = \frac{\frac{kTC_3^3}{(C_1+C_3)^2}}{(C_2+C_3)^2} C_3^2. \tag{6.4}$$

If all capacitors are considered to be equal to C, $\overline{Q^2_{\phi_1}}$ is equal to $kTC/16$. The same noise contributions can be obtained for the other three samples, generated during ϕ_2, ϕ_3 and ϕ_4. In ϕ_3 and ϕ_5, two different averages are generated, which are averaged a second time during ϕ_6. The two additional noise contributions, $\overline{Q^2_{\phi_3}}$ and $\overline{Q^2_{\phi_5}}$, can be written as

$$\overline{Q^2_{\phi_{3(5)}}} = \frac{kTC^2_{1(3)}}{C_{1(3)}+C_{2(4)}} \cdot \frac{C^2_{1(3)}}{(C_1+C_3)^2}. \tag{6.5}$$

In the case of equal capacitors, both of these variances are equal to $kTC/8$. The last noise contribution to be taken into account is the one generated by the average implemented during ϕ_6, which results in

$$\overline{Q^2_{\phi_6}} = \frac{kTC_1^2}{C_1+C_3}. \tag{6.6}$$

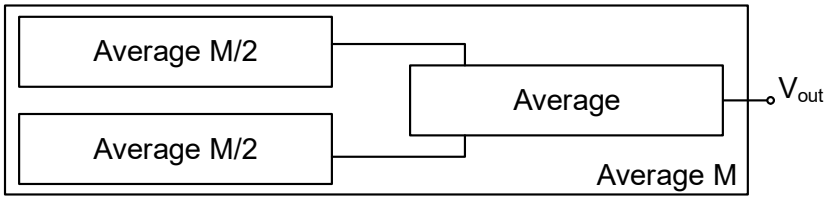


Figure 6.4: Generic CMS order M splitted into two blocks of order M/2 and a simple averager.

The latter is equal to $kTC/2$ when $C_1 = C_3$ is assumed. All the noise terms can be added up to obtain the total output charge noise variance, which is equal to kTC.

The noise analysis for the SC averager can now be generalized for an order M of the CMS. As shown in Fig. 6.4, every averager in a CMS of order M can be divided into the average of two averagers of order $M/2$. Based on the previous examples, if this process is iterated, each averager can be considered to generate a noise voltage variance equal to kT/C. Under these assumptions, the total noise output voltage, $\overline{V_{n,avg}^2}$, is given by

$$\overline{V_{n,avg}^2} = \frac{1}{4}\left(\frac{kT}{C} + \frac{kT}{C}\right) + \frac{kT}{2C} = \frac{kT}{C}. \tag{6.7}$$

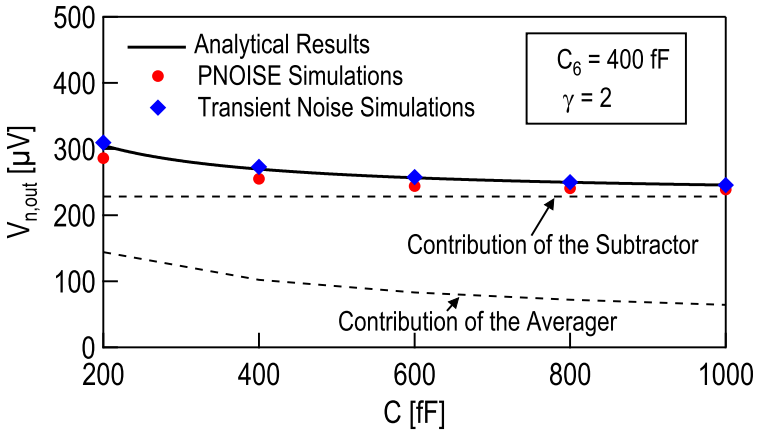
The first noise term in (6.7) originates from the noise charge sharing, while the second is the contribution of the average block. $\overline{V_{n,avg}^2}$ is equal to kT/C independently of the order M of the passive SC CMS circuit. The output noise contribution of the averager is independent of the number of input voltage samples processed.

To derive a formula for the total output voltage noise of the SC CMS circuit, the impact of the subtractor and the noise generated by the subtractor itself have to be added. The operation of subtraction doubles the input noise variance, while each voltage buffer will contribute with a noise variance equal to $\gamma kT/C_6$, where γ is the noise excess factor [1]. The latter assumes a low output impedance equal to $1/G_m$ for the voltage buffers. Finally, the contribution from the switching operation is equal to kT/C_6, and the final output voltage variance results in

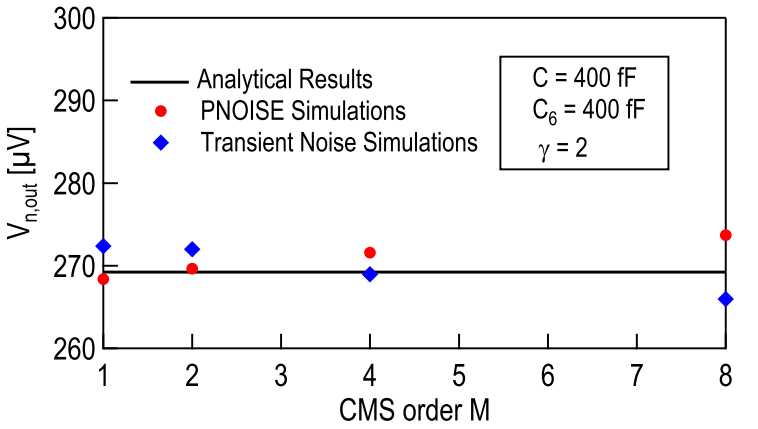
$$\overline{V_{n,out}^2} = \frac{2kT}{C} + \frac{(2\gamma+1)kT}{C_6}. \tag{6.8}$$

The proposed formula for the output voltage noise of the SC CMS is verified with PNOISE and transient noise simulations in the Spectre® circuit simulator. The simulations are performed assuming a sampling period, T_{CMS}, equal to 1 µs.

Fig. 6.5(a) and Fig. 6.5(b) show the RMS value of the CMS output voltage, $V_{n,out}$. In Fig. 6.5(a), $V_{n,out}$ is computed for four different values of the averager capacitor, C, from 200 fF to 1 pF. The noise contributions from the averager and the subtractor are shown separately and in



(a)



(b)

Figure 6.5: Comparison between calculated results and PNOISE and transient noise simulation results for different values of the averager capacitor (a) and various CMS orders (b).

dashed lines. The averager noise reduction with an increase in C is predicted by the kT/C term in (6.8). However, the noise of the subtractor is not influenced by the value of C. In Fig. 6.5(b), the output voltage noise is evaluated for four different CMS orders. The simulation results confirm that the noise contribution of the SC CMS is independent of M, and hence is not influenced by the required number of samples. The PNOISE and transient noise simulations results show a good match and validate the noise analysis results.

Column-level Amplifier Design

As shown in Fig. 6.1(a), the CLA is implemented with an adjustable gain. The closed-loop gain of this amplifier is set by the ratio between C_f and C_{in}: a different value of C_f can be

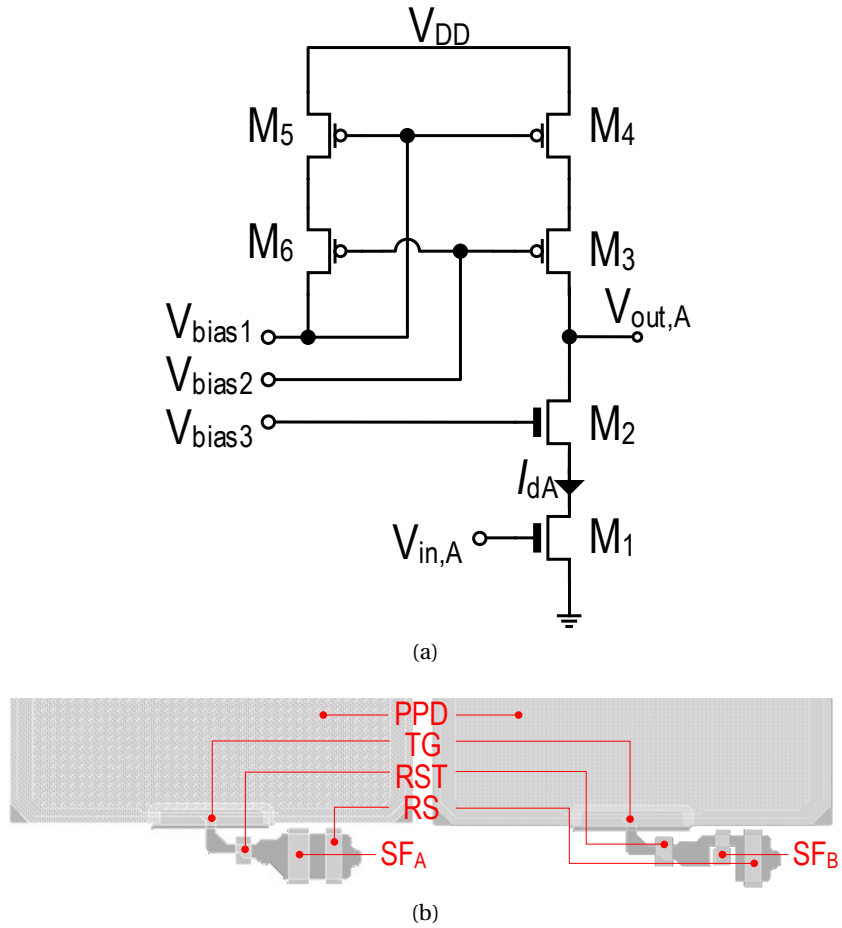


Figure 6.6: Schematic of the implemented capacitive amplifier in (a). Layout in (b) of the pixels A and B with the PPD and the TG, RST, RS and SF transistors.

chosen thanks to the two selection switches in series with each capacitor from C_{f1} to C_{f6}. The programmable value of C_f allows A_{col} to be changed between 1 and 128.

The CLA is implemented as a single-ended transconductance gain stage and its schematic is shown in Fig. 6.6(a). Since there is enough voltage headroom, cascode transistors are used to maximize the DC gain without increasing the noise. By choosing $G_{m1} > G_{m4}$, the noise contribution of the current source M_4 is made negligible compared to that of the driver transistor M_1.

The flicker noise contribution of the CLA is strongly reduced thanks to the autozero [17] and the transistor area of the CLA is made much larger than the in-pixel SF. As discussed earlier, this is a reasonable choice due to the relaxed constraint on the area at column-level compared to the tight area constraint set for the pixel. When the high closed-loop gains are used, the charge injection coming from the AZ transistor becomes critical because it can dramatically decrease the dynamic range of the amplifier. This phenomenon is compensated by the use of

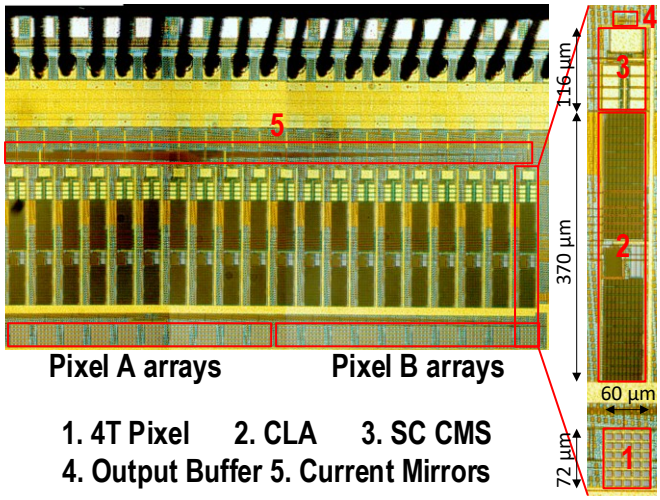


Figure 6.7: Chip micrograph showing the main blocks of the readout chains with biasing circuits and buffers.

properly-sized dummy transistors in series with the switches [17], as shown in Fig. 6.1(a).

Pixel Design

The layout of the two pixels implemented in a 180 nm CIS technology is shown in Fig. 6.6(b). They differ in the size and type of the nMOS SF transistor: in Pixel A, the SF is a n-channel native transistor featuring an aspect ratio of 1.2 µm/0.6 µm, while Pixel B features a standard nMOS SF with an aspect ratio of 0.22 µm/0.35 µm. The bias current of each pixel is named I_{dSF} and it is set by an external current reference to 2 µA. Both pixels have about the same value of parasitic capacitance at the SN, C_p, which is estimated at 3 fF. To asses the impact of the SF sizing on noise, the aspect ratio of Pixel B is more than three times smaller than that of Pixel A. As discussed in the previous section, the reduction of the W and the use of an optimal L for the SF transistor is one of the solutions proposed to achieve the lowest 1/f noise [10]. Based on this analysis, a better noise performance is expected from Pixel B. The compact layout for the two pixels results in a fill factor of 80% with a pixel pitch of 12 µm.

Chip Micrograph

In Fig. 6.7, a chip micrograph with a lateral zoom of a single readout chain is shown. The red rectangles are numbered to define the different implemented blocks, which consist of the two pixels, the CLA, the SC CMS, the output buffers and the current mirrors. The height and width of each block are reported directly in the figure.

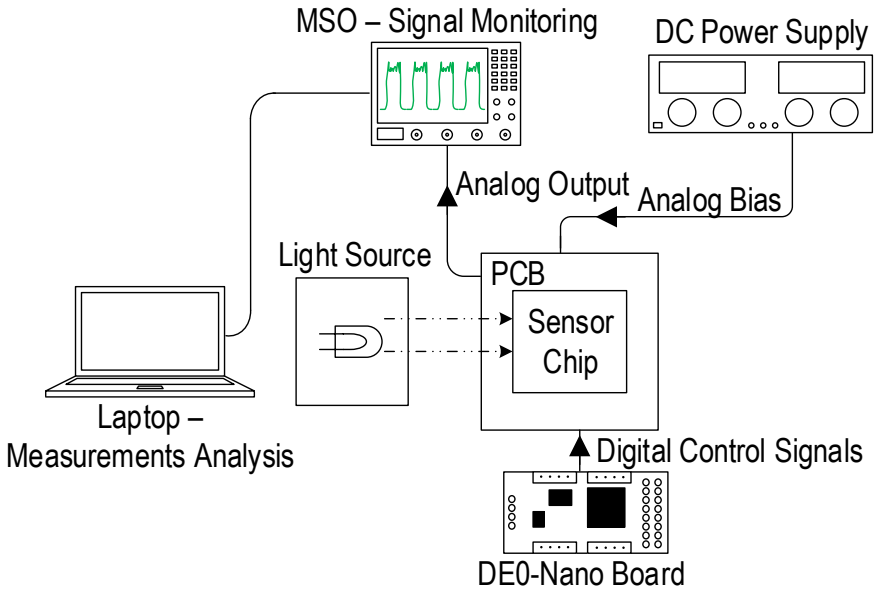


Figure 6.8: Setup for the characterization and the noise measurements of the readout chains implemented on the chip.

6.2.2 Measurement Results

Experimental Setup

The measurement setup is shown in Fig. 6.8. The sensor chip is packaged and mounted on a PCB, where all connectors and power supply filters for low noise requirements are placed. All the control signals for the readout and the SC CMS are generated by the Cyclone-V FPGA of the DE0-Nano Board [18]. The analog voltage and current references are generated externally, as is the 3.3 V voltage supply, and the output of each readout chain is selected directly on the PCB. The output signal is monitored on the MSO-S 804A oscilloscope and the data acquisition performed with a Visual Basic script executed on a laptop. The input of the oscilloscope has an integrated 10 bit ADC. The PTC measurements require a variable input light, which is implemented with a voltage tunable LED source attached to the top of the sensor. Data require averaging, a step which is performed during data processing in the Matlab® environment and which reduces the impact of the quantization noise of the scope ADC.

Conversion Gain Measurement

As explained in Chapter 4, the PTC technique is used to obtain the value of the readout conversion gain, *CG* [19]. When the sensor is limited by the PSN, the variance of the output is proportional to the average output value and the coefficient of proportionality corresponds to *CG*. The latter was therefore extracted from the output noise variance versus input signal strength for values of the CLA gain ranging from 1 to 128 by estimating the slope of the linear

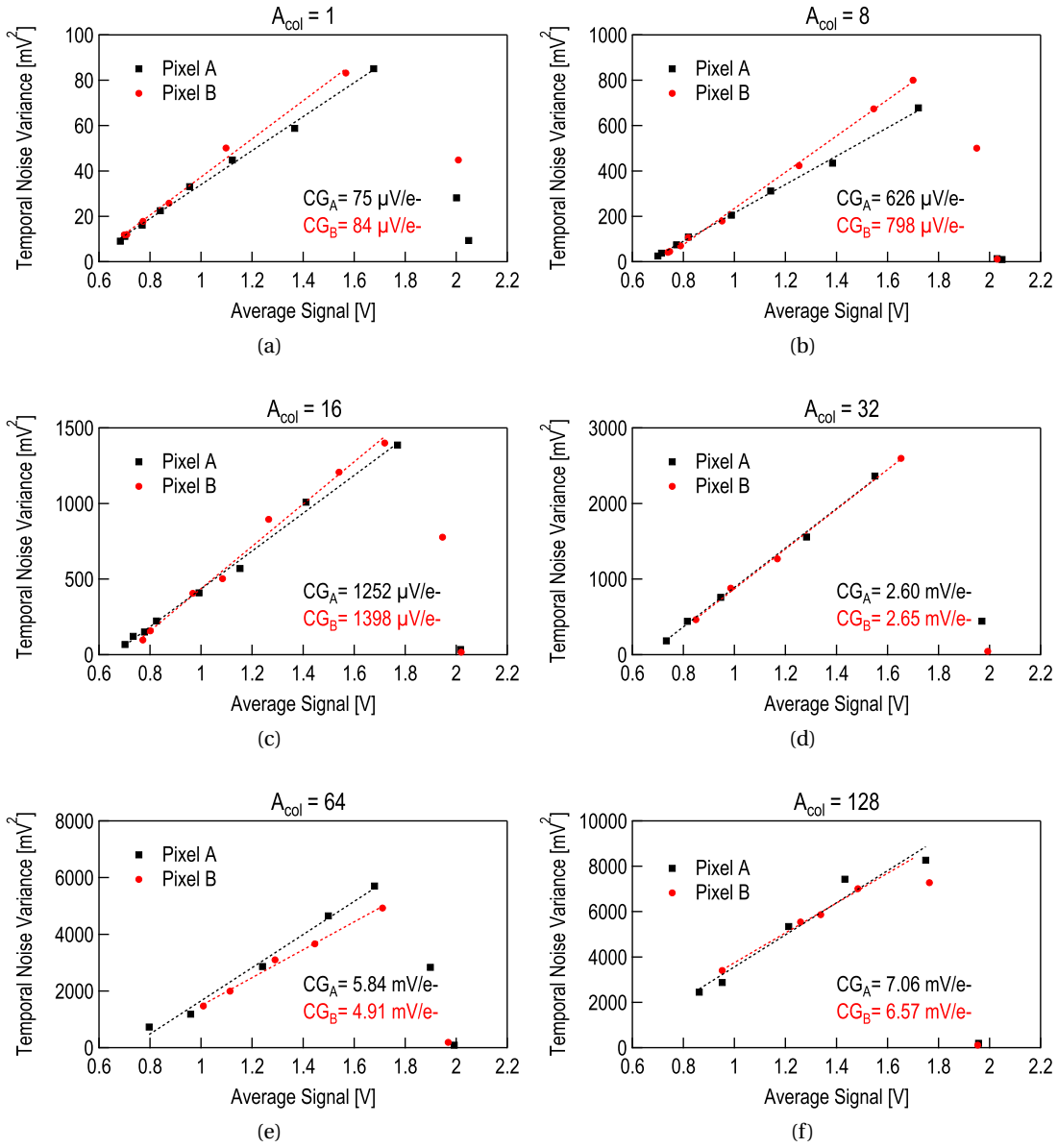
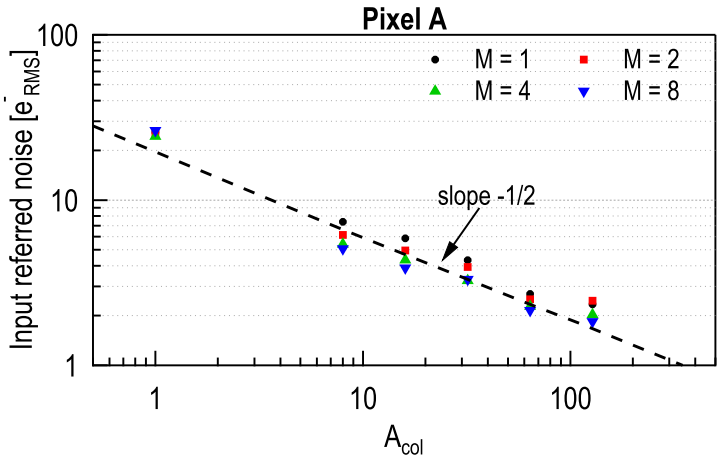


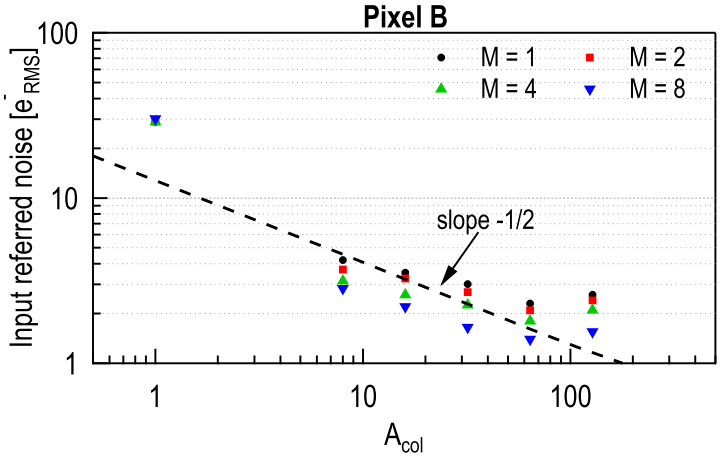
Figure 6.9: PTCs of the readout chain for different values of the CLA gain (from 1 to 128), in order from (a) to (f). The overall *CG* is reported in each figure for both pixels.

part of the PTC before saturation, as shown in Fig. 6.9.

During the performed measurements, the sensor is exposed to a uniform input light and a voltage source allows the illumination level to be increased. The obtained *CG* values for each A_{col} gain value are reported inside the corresponding figure, while the dashed lines are the linear approximation of the measured values, indicated with markers. When the CLA gain is equal to one, the readout conversion gain, *CG*, corresponds to the pixel conversion gain, A_{CG}, used in (5.19). The measured pixel conversion gain for Pixel A is 75 µV/e$^-$ and 84 µV/e$^-$



(a)

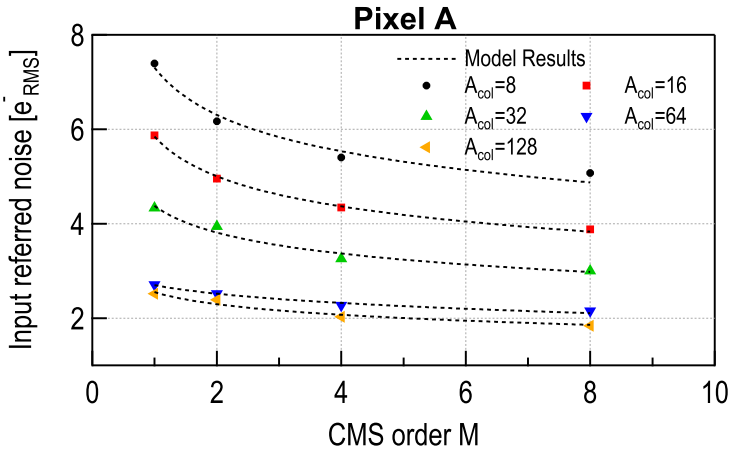


(b)

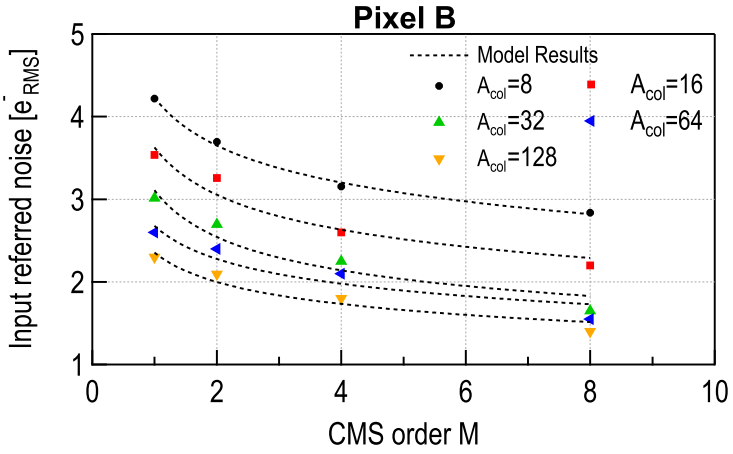
Figure 6.10: Input-referred noise for both pixels as a function of the CLA gain value. The expected trend for thermal noise reduction is plotted with a dashed line.

for Pixel B. The small difference in the pixel conversion gain is due to the different sizes of the SF transistors and means that the total SN capacitance is dominated by C_p in this particular design. The contributions of the in-pixel SF to the SN capacitance only slightly influence the value of A_{CG}.

At about 1.8 V, almost all the curves in Fig. 6.9 deviate from the linear behavior, because the readout chain reaches saturation at the level of the amplifier. This shows that the dynamic range in all configurations is limited by the readout chain and not by the full-well capacity of the PPD. For $A_{col} = 1$, the fact that the PTC collapses around 1.8 V allows the readout handling capacity to be estimated, which results in 18 200 e^-. This value is suitable for applications requiring high dynamic range (HDR) imaging.



(a)



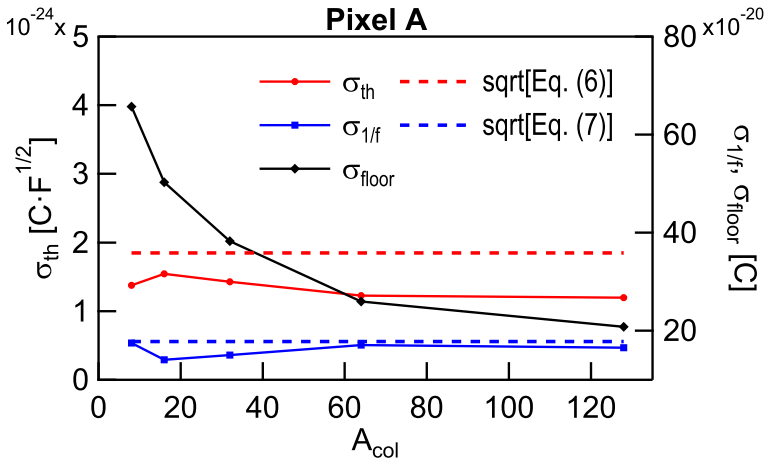
(b)

Figure 6.11: Input-referred total noise for Pixel A (a) and Pixel B (b) as a function of the CMS order M. The measurements are compared with the total noise expression proposed in (6.9).

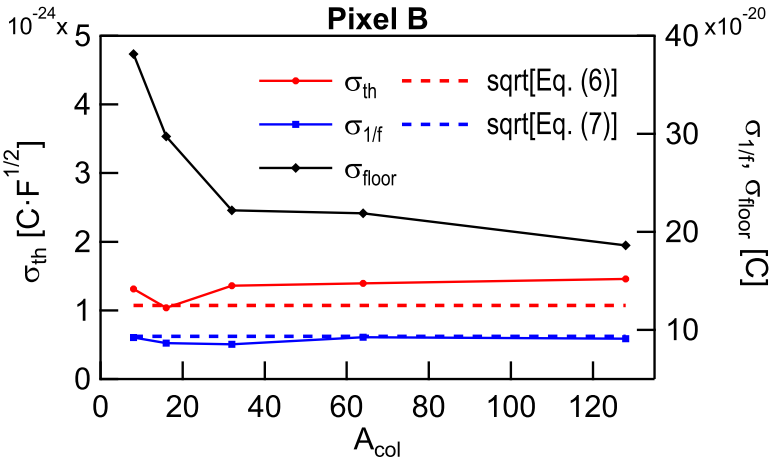
Temporal Read Noise

The input-referred noise is calculated from the measured output noise voltage variance and the extracted *CG*. The output voltage samples are stored after performing 1000 readout operations with a T_{CMS} of 1 µs. The TG remains off throughout the measurement procedure. The CLA gain is varied along six different values and the implemented CMS orders are 1, 2, 4 and 8. At the column-level gain of 32, the amplifier limits the bandwidth to about 250 kHz. As mentioned earlier, this is key for limiting the thermal noise contribution.

Fig. 6.10(a) and Fig. 6.10(b) show the impact of the CLA gain on the total input-referred noise. Unlike the simulation results shown in [20], the noise contributions originating from different noise mechanisms (thermal, flicker and shot) can not be completely separated.



(a)



(b)

Figure 6.12: The square root of the fitting parameters σ^2_{th} (on the left axis), $\sigma^2_{1/f}$ and σ^2_{floor} (on the right axis) is plotted for each value of the column-level gain for Pixel A (a) and Pixel B (b).

For unity CLA gain value, the noise contributions of the stages following the amplifier (e.g. kT/C noise of the CMS network, voltage buffers and ADC) are not reduced and add to the noise of the SF and the CLA. This explains the discrepancy between the measurements and the ideal $1/A_{col}$ interpolation observed for $A_{col} = 1$ and $A_{col} = 8$.

Based on (5.19) and unlike 1/f noise, the thermal noise is expected to decrease following the $1/\sqrt{A_{col}}$ "law". In log scale, this translates to a linear trend with -1/2 slope, plotted with a dashed line in Fig. 6.10(a) and Fig. 6.10(b). A similar behavior is observed in Pixel A for A_{col} between 8 and 64 and in pixel B between 8 and 32. This suggests that the thermal noise is the dominating noise mechanism for these gain values.

For higher gain values, the thermal noise is reduced to a value close to or below the 1/f noise.

Table 6.2: Values of the Process and Design Parameters

		Pixel A	**Pixel B**
C_{ox}	[fF µm^{-2}]	4.5	4.5
C_{in}	[pF]	1	1
C_L	[fF]	400	400
γ_{SF}	[-]	5	5
γ_A	[-]	5	5
W	[µm]	1.2	0.22
L	[µm]	0.6	0.35
I_{dSF}	[µA]	2	2
I_{dA}	[µA]	10	10
C_{ex}	[fF µm^{-1}]	0.45	0.45
C_p	[fF]	1.6	1.6
T_{CMS}	[µs]	1	1
$C_{1...5}$	[fF]	400	400
C_6	[pF]	1	1
N_t	[eV^{-1} cm^{-3}]	$3 \cdot 10^{17}$	$5 \cdot 10^{16}$
σ_{th}	[C F$^{1/2}$]	$1.85 \cdot 10^{-24}$	$1.07 \cdot 10^{-24}$
$\sigma_{1/f}$	[C]	$1.78 \cdot 10^{-19}$	$9.35 \cdot 10^{-20}$

According to (5.26), 1/f noise does not scale as $1/A_{col}$, since it accounts for the 1/f noise of the SF only, which is injected before the CLA. This explains the limitation of the noise reduction for A_{col} above 32.

In Fig. 6.11(a) and Fig. 6.11(b), the same measurements are plotted for both pixels as a function of the CMS order and for different values of A_{col}. The measurement results are compared with the following proposed expression for the total noise

$$\overline{Q_{n,tot}} = \sqrt{\frac{\sigma_{th}^2}{M\,A_{col}\,C} + \alpha_{1/f}\sigma_{1/f}^2 + \sigma_{floor}^2}, \tag{6.9}$$

which is based on (5.19) and (5.26). In the proposed formula, the thermal and the flicker noise parameters, σ_{th}^2 and $\sigma_{1/f}^2$, are introduced, as well as the noise floor, σ_{floor}^2. σ_{th}^2 and $\sigma_{1/f}^2$ depend only on process and design parameters and, by using (5.19) and (5.26), they can be expressed as

$$\sigma_{th}^2 = 2\,k\,T\left[\frac{\gamma_{SF}\,G_{mA}\left(\frac{2}{3}C_{ox}WL + 2\,C_{ex}W + C_p\right)^2}{G_{mSF}} + \frac{\gamma_A}{A_{CG}^2}\right] \tag{6.10}$$

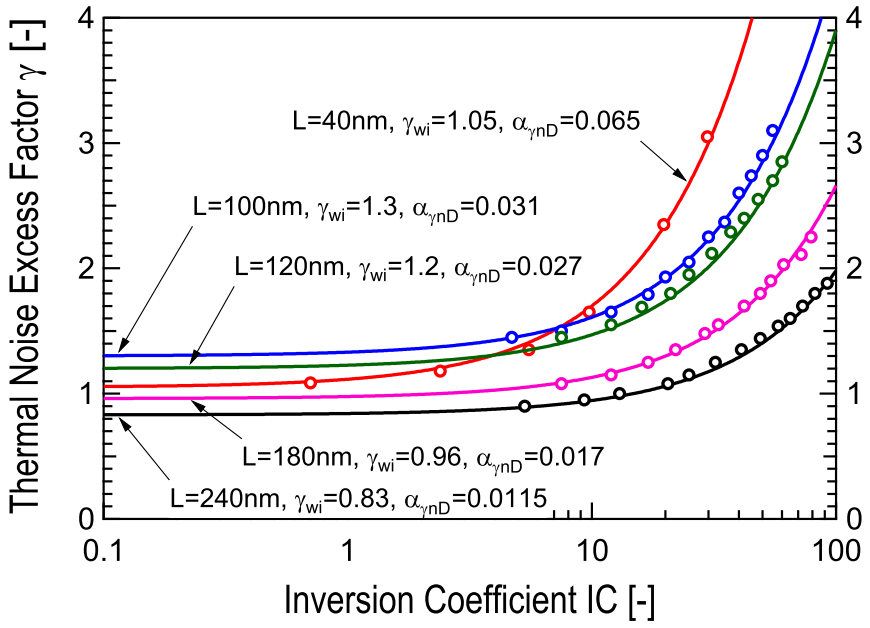


Figure 6.13: Measured values of the thermal noise excess factor against IC for L equal to 240 nm, 180 nm, 120 nm, 100 nm and 40 nm (reprinted from [21]).

and

$$\sigma_{1/f}^2 = \frac{K_F \left(C_p + 2\, C_{ex}\, W + \frac{2}{3} C_{ox}\, W\, L \right)^2}{{C_{ox}}^2\, W\, L}. \tag{6.11}$$

The noise floor is introduced to model all noise sources which are not included in (5.19) and (5.26) but still need to be accounted for. It mainly corresponds to the noise introduced after the CMS subtractor of Fig. 6.1(a), which includes the noise of the measurement electronics. To achieve a match between the measurements and the model results, σ_{th}^2, $\sigma_{1/f}^2$ and σ_{floor}^2 are used as fitting parameters. Table 6.2 reports the estimated values of the process and design parameters used to match with the measurement results as well as the expected values for σ_{th} and $\sigma_{1/f}$.

As shown in Fig. 6.12 for each value of A_{col}, a good match between the measured noise and the one calculated using (6.9) is obtained for the values of σ_{th}, $\sigma_{1/f}$ and σ_{floor}. In the same figure, σ_{th} and $\sigma_{1/f}$ are compared with the expected values from the model, which are plotted with dashed lines, and a good match is obtained. This validates the theoretical results on the impact of the gain and the CMS on the noise, as well as the use of the process and the design parameters involved in (5.19) and (5.26). As expected from (6.10) and (6.11), the values of σ_{th} and $\sigma_{1/f}$ obtained from the numerical fitting are only slightly influenced by A_{col}. The value of σ_{floor}^2 is indeed reduced under the effect of a higher gain, in agreement with the earlier statement.

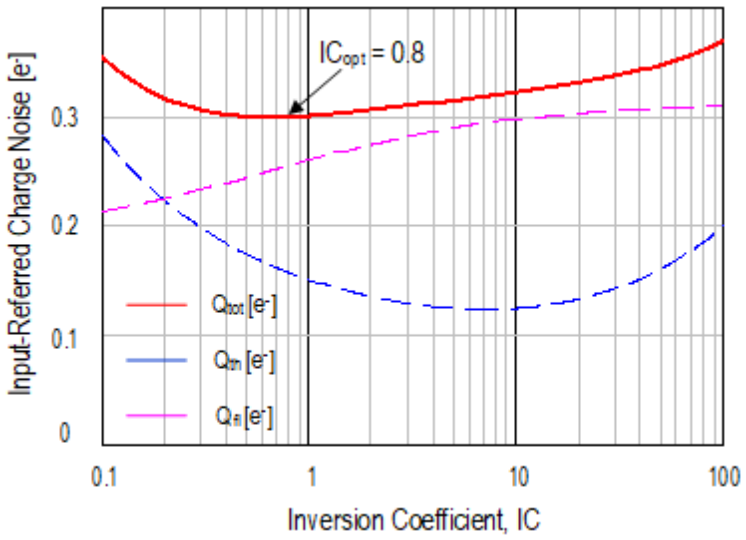


Figure 6.14: Total, thermal and flicker RMS charge noise as a function of the SF IC coefficient. In order to generate these curves, the following values are used for the main parameters: $C_{ox} = 4.5\,\text{fF}\,\mu\text{m}^{-2}$, $I_{spec\square} = 500\,\text{nA}$, $C_{ex} = 0.45\,\text{fF}\,\mu\text{m}^{-1}$, $n = 1.2$, $C_P = 0.75\,\text{fF}$, $\gamma_A = 1$ and $G_{mA} = 30\,\mu\text{AV}^{-1}$

6.3 Technology Downscaling Effects on Noise

6.3.1 Impact of Technology Downscaling on Readout Noise

More advanced technology nodes e.g. under 100 nm have been introduced for CISs [22, 23, 24, 25] and a possible read noise reduction due to technology downscaling was analytically predicted in [26]. The better noise performance is based on a higher C_{ox}, a lower SF width and overlap capacitances often reported for thin oxide transistors in downscaled processes. In [26], a thin oxide pMOS is used as an in-pixel SF and lower values of the oxide trap density, N_t, compared to nMOS transistors were shown for different foundries and technology nodes.

Regarding thermal noise in more advanced technologies, the noise excess factor, γ, against the inversion coefficient (IC) is shown in Fig. 6.13 for different channel lengths, L, from 40 nm to 240 nm [21, 27, 28]. The parameter IC is defined in [1] as

$$IC = \frac{I_{Dsat}}{I_{spec}}, \tag{6.12}$$

where I_{Dsat} it the MOSFET saturation current and I_{spec} being the specific current given by

$$I_{spec} = I_{spec\square} \cdot \frac{W}{L} = 2n\beta U_T^2, \tag{6.13}$$

where $\beta = \mu C_{ox} W/L$ is the transfer parameter, $I_{spec\square} = 2n\mu C_{ox} U_T^2$ and μ the mobility of carriers. IC is a metric for the inversion level of a transistor, with $IC < 0.1$ defining weak

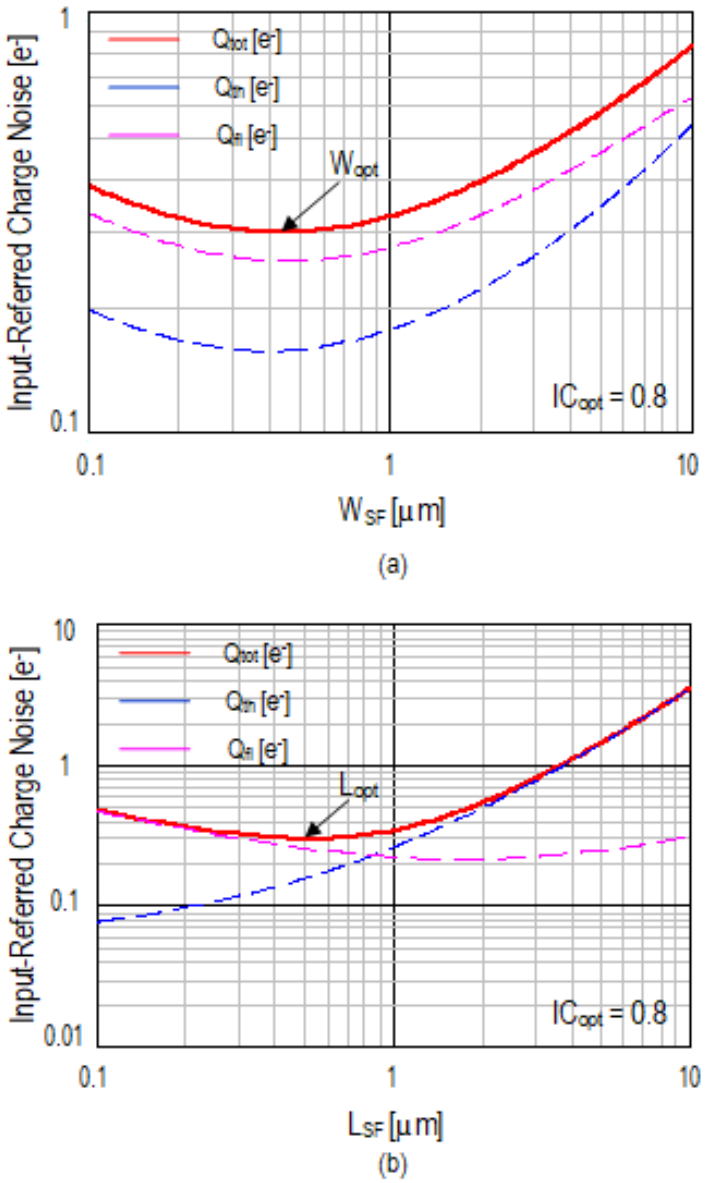


Figure 6.15: Total, thermal and flicker RMS charge noise as a function of the SF width in (a) and length in (b). The following values are used for the main parameters: $C_{ox} = 4.5\,\text{fF}\,\mu\text{m}^{-2}$, $I_{spec\square} = 500\,\text{nA}$, $C_{ex} = 0.45\,\text{fF}\,\mu\text{m}^{-1}$, $n = 1.2$, $C_P = 0.75\,\text{fF}$, $\gamma_A = 1$ and $G_{mA} = 30\,\mu\text{AV}^{-1}$

inversion (WI), $IC > 10$ strong inversion (SI) and $0.1 < IC < 10$ moderate inversion (MI) region [1]. In Fig. 6.13, the measured results are compared with the empirical expression used in [27] and given by

$$\gamma = \gamma_{wi} + \alpha_{\gamma nD} \cdot IC, \tag{6.14}$$

where the values for $\alpha_{\gamma nD}$ are directly reported in the figure. From moderate to strong inver-

Table 6.3: Relevant parameters for noise estimation and calculated input-referred flicker noise

	nMOS2.5	**pMOS2.5**	**pMOS1.2**
V_{dd} [V]	2.5	2.5	1.2
N_t [$eV^{-1} \cdot cm^{-3}$]	$8 \cdot 10^{16}$	$2.4 \cdot 10^{16}$	$9.5 \cdot 10^{16}$
C_{ox} [$fF/\mu m^2$]	6.2	5.9	12.0
t_{ox} [nm]	5.6	5.9	2.8
N_t/C_{ox}^2 [$eV^{-1}\,\mu m\,fF^{-2}$]	2081	689	660
$\overline{Q_{1/f}^2}$ [e^-_{rms}]	0.80	0.35	0.43

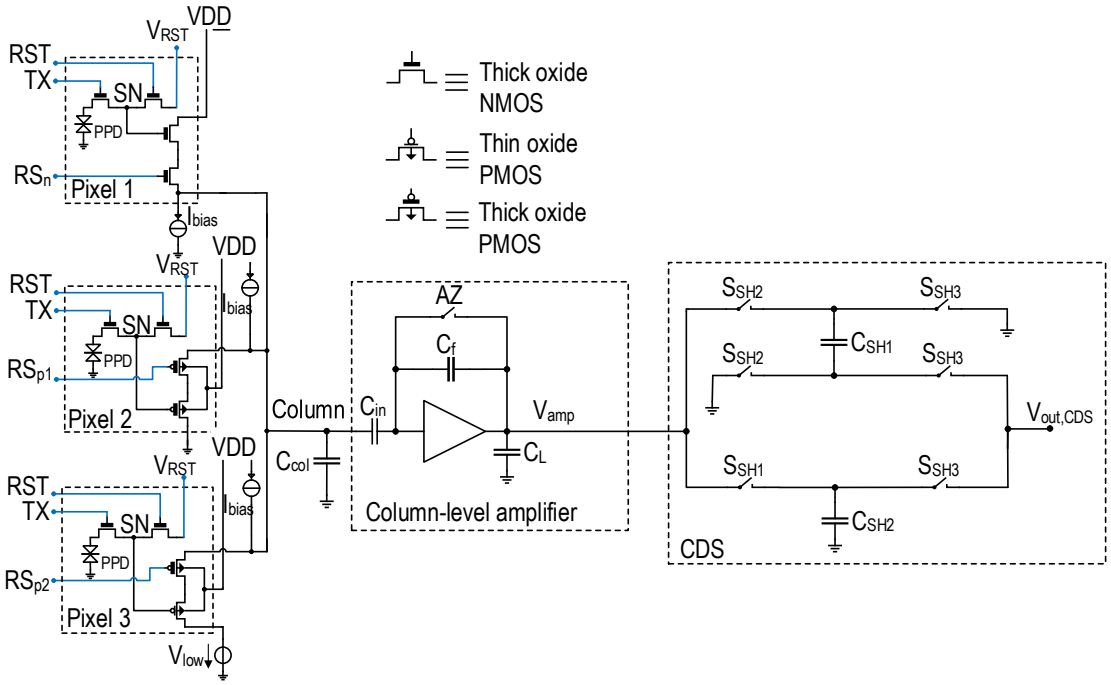
sion, the thermal noise excess factor significantly increases (from ~ 1 to 3). For lower transistor lengths, a higher value of γ is reported due to short channel effects e.g. velocity saturation and carrier heating [1, 28]. When the dependence on IC and the short channel effects are taken into account in (5.18) for γ_{SF}, G_{mSF} and the SF capacitances, the thermal noise optimization of the SF indicates an optimum point on the upper side of MI and for a minimum length, as shown with a blue dashed lines respectively in Fig. 6.14 and Fig. 6.15(b).

The dependence of the input-referred noise charge variance due to flicker noise on IC comes from the gate-to-source intrinsic capacitance, C_{GS}, in (5.24), but as shown in Fig. 6.14 it is rather small. The latter is also not affected by velocity saturation. Contrary to what is shown in [3] for a 180 nm technology and as predicted in [29], with lower transistor sizes an optimum SF width, W_{opt}, and length, L_{opt}, are found when optimizing the flicker noise contribution. The latter is shown in Fig. 6.15(a) and Fig. 6.15(b) for $IC = IC_{opt} = 0.8$. The optimum design point corresponds to the minimum flicker noise knowing that the conversion gain increases with a lower SF area, while the 1/f noise increases. The total input-referred charge noise against IC in Fig. 6.14 illustrates that the optimum bias for the SF, IC_{opt}, is located in the MI region.

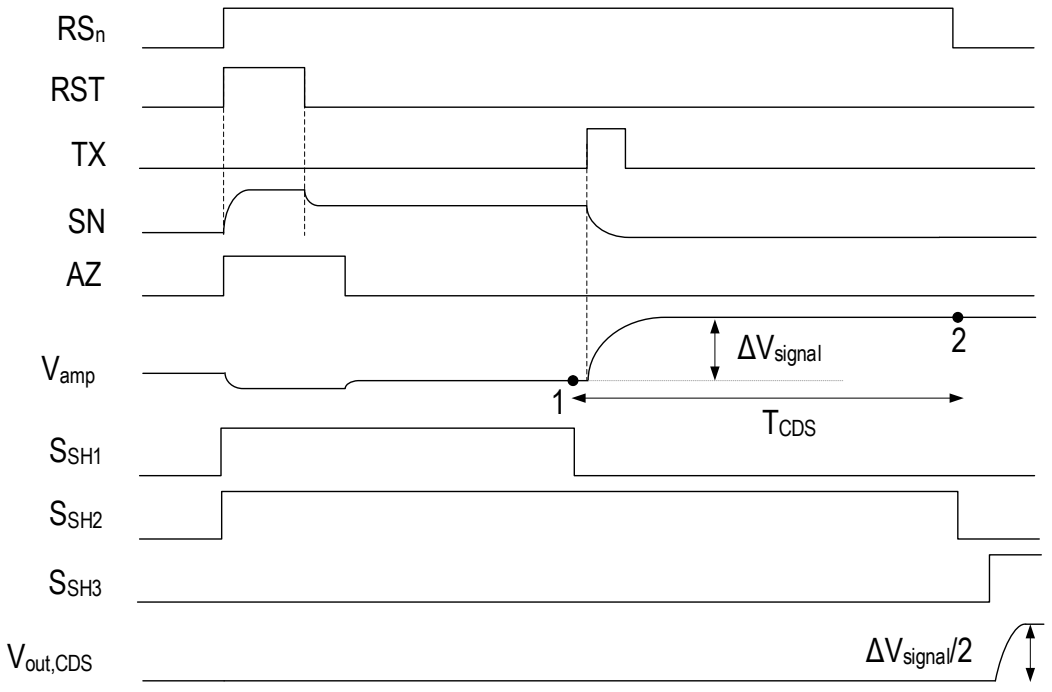
6.3.2 Simulation setup

In this section, the read noise of a CIS readout chain integrated in a 65 nm process is investigated. The transistors in the simulated 65 nm process that can be used as the in-pixel SF are shown in Table 6.3, with their parameters relevant to this analysis. From the flicker noise expression in (5.26), a lower 1/f noise can also be obtained with a higher C_{ox}, a lower minimum gate width and a constant N_t. The 3.3 V in-pixel SF traditionally used in a 180 nm CIS process feature a C_{ox} of about 4 $fF/\mu m^2$ with a N_t of $1.5 \cdot 10^{17}\,eV^{-1} \cdot cm^{-3}$ for nMOS and $3 \cdot 10^{17}\,eV^{-1} \cdot cm^{-3}$ for pMOS [3]. All the transistors shown in Table 6.3 feature a higher C_{ox} and a lower N_t with respect to the 3.3 V nMOS from a typical 180 nm CIS process. Consequently, based on (5.26), a better 1/f noise performance can be expected from this 65 nm process.

Specifically, the pMOS2.5 has the best N_t/C_{ox}^2 ratio, which makes it the best candidate for low-1/f-noise performance, followed by the pMOS1.2 and the nMOS2.5. The input-referred



(a)



(b)

Figure 6.16: Schematic in (a) of the simulated low-noise CIS readout chains. Timing diagram in (b) of the simulated CIS readout chain.

flicker noise calculated from (5.26) with the parameters given in Table 6.3 are shown in the last row of the table. For the nMOS2.5 the result is 0.8 e^-_{rms}, for the pMOS1.2 0.43 e^-_{rms} and for the pMOS2.5 0.35 e^-_{rms}. As shown later in this section, transient noise simulations can verify the assumption of deep sub-electron read noise performance with this 65 nm process.

Fig. 6.16(a) shows the schematic of the simulated low-noise CIS readout chains. Each pixel is based on a different source follower: nMOS2.5, pMOS2.5 and pMOS1.2. The pMOS based pixels use pMOS2.5 row selectors. For the pMOS1.2 transistor, the bulk and the drain are shifted in order to keep the voltage between its terminals below 1.2 V. The three pixels are sharing the same column-level readout chain made of a fully cascoded single-ended CLA and CDS. The bandwidth of the CLA has been set to 256 kHz, for a gain of 64 and a load capacitance of 200 fF, to 512 kHz for a gain of 16. Consequently, the minimum time interval T_{CDS} for a sufficient signal settling is about 4 µs. The CDS is implemented with an analog circuit. The corresponding readout chain timing diagram is shown in Fig. 6.16(b). In an analog CDS, a first sample is held in a capacitor after resetting the pixel; then, the TG is turned-on and after a time equal to T_{CDS}, a second sample is stored in an other capacitor. The two samples are differentiated after the rising edge of the signal S_{SH3}. As before, the AZ is performed in order to reset the feedback capacitor [17].

6.3.3 Noise Simulation Results

Given that the readout chain is a time variant system, the most realistic way of simulating the noise is the transient noise simulation [30]. In this work, the circuit simulator Eldo is used since it also allows to separate the analysis of the thermal and 1/f noise. Transient noise simulations have shown a good match with experimental results in [11] for both thermal and flicker noise.

A parametric simulation is first performed in order to evaluate the overall conversion gain of each readout chain. The noise voltage, evaluated at the output, is then referred to the input as an equivalent noise charge. The simulated pixel conversion gain are 145 $\mu V/e^-$ for the *n*MOS2.5, 140 $\mu V/e^-$ for the *p*MOS2.5 and 162 $\mu V/e^-$ for the *p*MOS1.2. Here, thermal, flicker and leakage current shot noise are analyzed separately.

Thermal noise

The input-referred thermal noise, obtained from transient noise simulations, as a function of the column-level gain A_{col} is shown for each of the three SF configurations, in Fig. 6.17. The latter curves show how the column-level gain decreases the thermal noise, as expected analytically by (5.19). The contributions of the pixel and the CLA have similar values. For a column-level gain of 64, a C_L of 200 fF and a bandwidth of 256 kHz, the input-referred thermal noise of each configuration is below 0.3 e^-_{rms}, as for the 180 nm from [11]. In fact, at $A_{col} = 64$ both the readout chain based on pMOS2.5 and nMOS2.5 feature an input-referred thermal

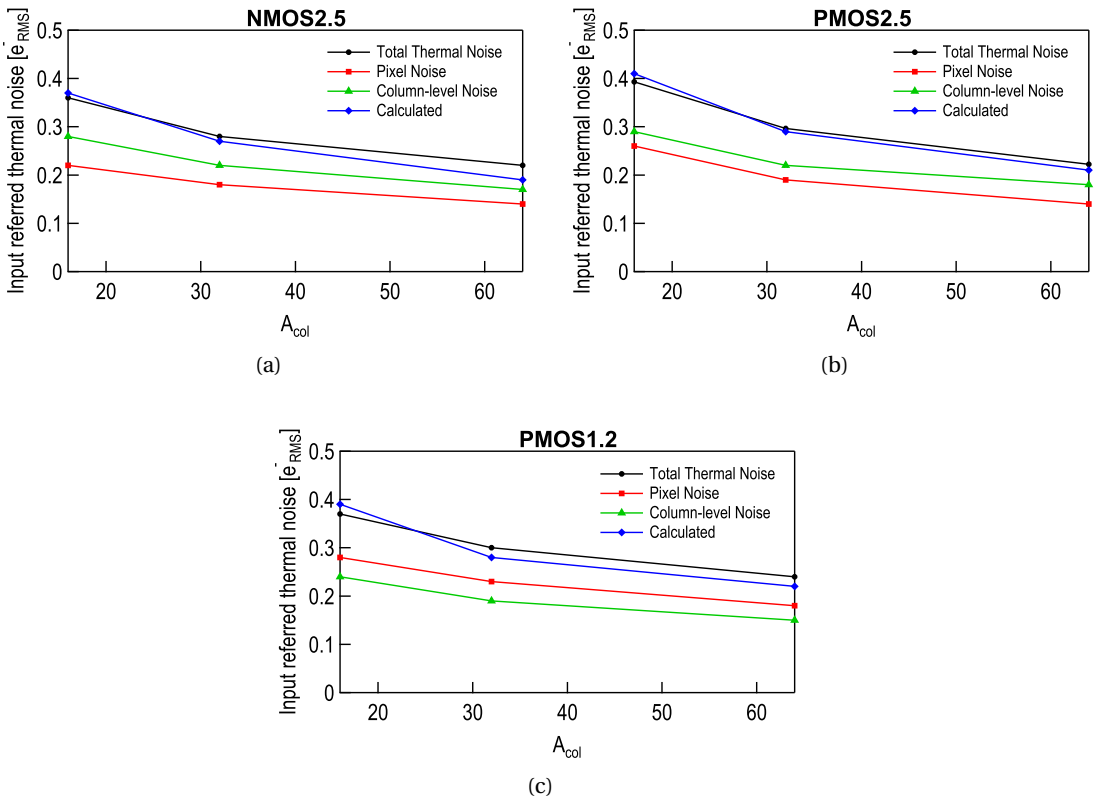


Figure 6.17: Input-referred thermal noise of the CIS readout chain with nMOS2.5 in (a), pMOS2.5 in (b) and pMOS1.2 SF in (c), respectively, as function of the column-level gain.

noise of 0.22 e^-_{rms}, while the pMOS1.2 features a noise level of 0.24 e^-_{rms}. These simulation results are compared with the input-referred noise calculated using (5.19), showing a good match. For the noise calculation, both noise excess factor γ_{SF} and γ_A are considered to be equal to 1, C_P has been obtained by simulation as 0.72 fF, C_e has been considered to have a value of one tenth of C_{ox}, $G_{m,A}$ is equal to 30 µS and $G_{m,SF}$ 13 µS for pMOS2.5, 30 µS for nMOS2.5 and 23 µS for pMOS1.2.

The pMOS2.5 and nMOS2.5 feature a minimum gate width of 0.4 µm and a minimum length of 0.28 µm, while the pMOS1.2 features a width of 0.2 µm and a length of 0.3 µm. All the width and length values were chosen to optimize the input-referred total noise.

The simulation and calculation results show that the downscaling does not increase the thermal noise and the analysis leading to (5.19) is still valid for this 65 nm process. The result of this analysis is that the thermal noise of the readout chains with all type of SFs could efficiently be reduced using column gain and bandwidth control. As it will be shown in next section, the 1/f noise is confirmed to be dominant.

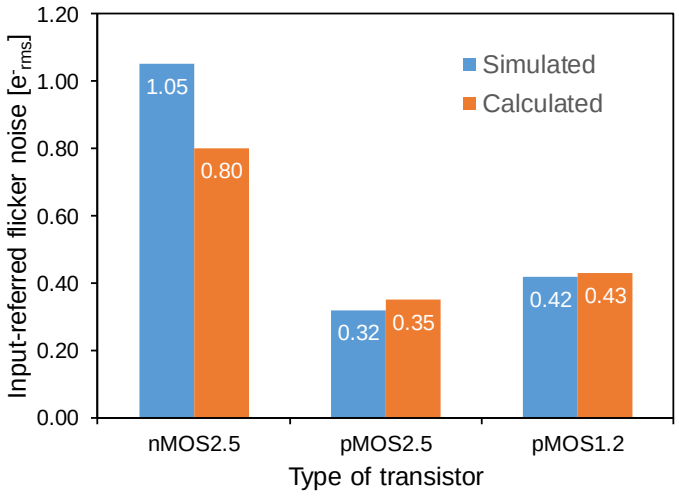


Figure 6.18: Simulated and calculated input-referred flicker noise of the CIS readout chains with different type of in-pixel SFs.

1/f noise

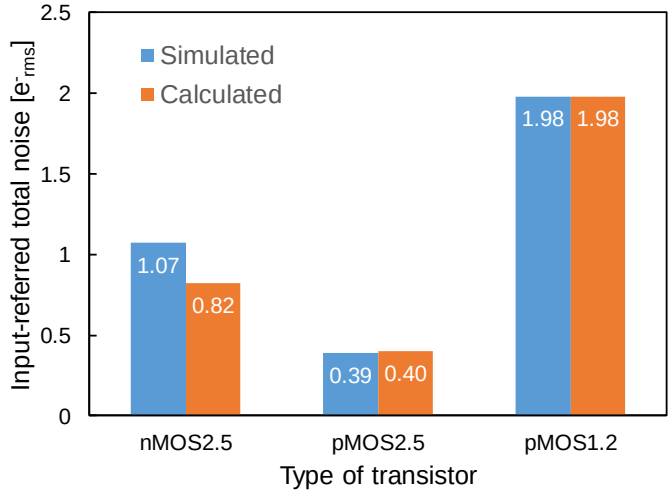
The input-referred flicker noise obtained by transient noise simulations for the three different configurations are shown in Fig. 6.18. The 1/f noise of the pMOS2.5, pMOS1.2 and nMOS2.5 is calculated for a column-level gain of 64, a C_L of 200 fF and a bandwidth of 256 kHz, and behaves as expected theoretically.

The mismatch between the simulated and the calculated values can be explained with the different values of the parameter K_G, which has been considered constant and equal to unity in calculation. Indeed, K_G depends on the inversion coefficient [1], which is not the same for the three types of transistors. The nMOS2.5 shows a high N_t and low C_{ox}, hence it features the highest noise level. The pMOS1.2 features approximately the same N_t as the nMOS2.5 but a C_{ox} twice as large, resulting in a twice better RMS noise performance. But for the pMOS2.5, even if its C_{ox} is not as high as the pMOS1.2, it features a much lower N_t, which makes it the lowest noise device with an input-referred 1/f noise of 0.32 e^-_{rms}.

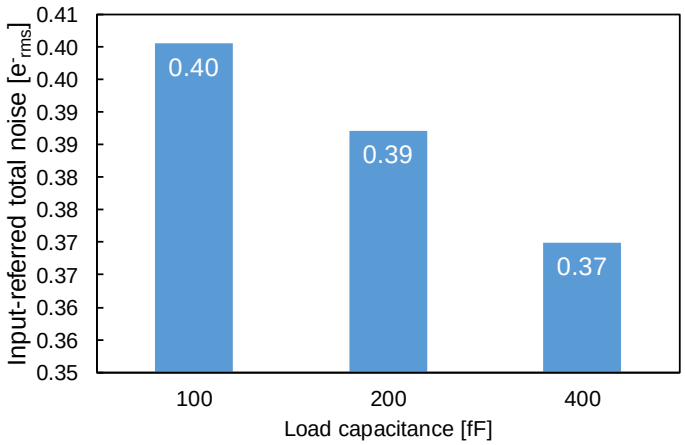
Leakage Current Shot Noise

With a gate oxide scaled down to 3 nm and below, the gate leakage current due to the carrier direct tunneling becomes important [31]. From Table 6.3, it can be observed that this is indeed the case for pMOS1.2. As it was shown in Chapter 4, in BSIM4, the gate tunneling current components include the tunneling current between gate and substrate and the current between gate and channel, which is partitioned between the source and drain terminals. Since these leakage currents are due to barrier control processes, they give rise to shot noise.

The input-referred charge variance due to the total leakage currents shot noise is expressed



(a)



(b)

Figure 6.19: Input-referred total noise in (a) of the readout chain with nMOS2.5, pMOS1.2 and pMOS2.5 SF, respectively. Input-referred total noise of the readout chain with pMOS2.5 SF as a function of the load capacitance in (b).

in (5.32). The shot noise current sources feature a white PSD and when integrated in the SN capacitance, they give rise to a variance increasing linearly with T_{CDS} [26]. The BSIM4 model parameters $igcMod$ and $igbMod$ allow the activation of the gate leakage current components. This makes possible the separation between thermal noise and gate tunneling current shot noise in the simulation.

The simulation shows that this shot noise is completely negligible for thick oxide transistors nMOS2.5 and pMOS2.5 and for the thin oxide pMOS1.2, with a column-level gain of 64, a C_L of 200 fF and a bandwidth of 256 kHz, the input-referred charge noise variance increases dramatically to reach 1.88 e^-_{rms}.

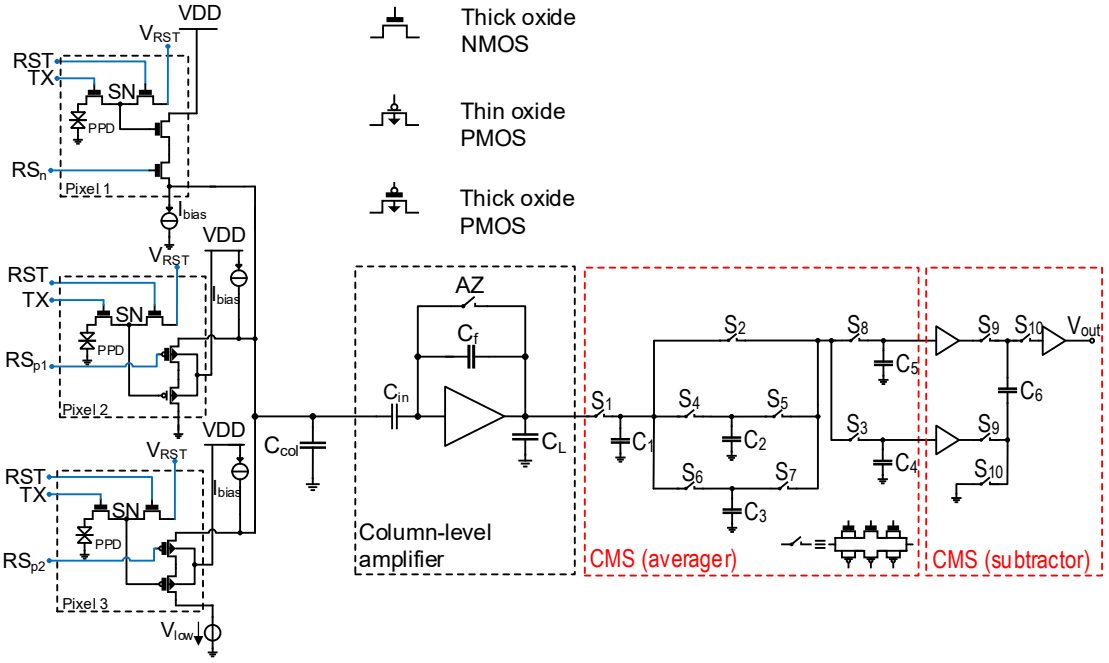


Figure 6.20: Schematic of the simulated low-noise CIS readout chains.

The input-referred total noise is shown in Fig. 6.19(a). It appears clearly that the pMOS2.5 features the best noise performance of $0.39\,e^-_{rms}$, as expected theoretically. This noise relays between the photoelectron counting ($0.3\,e^-_{rms}$) and the photoelectron detection limit ($0.4\,e^-_{rms}$). In order to further reduce the thermal noise of the readout chain, the increase of C_L is used in addition to the A_{col}. This results in a lower bandwidth and high T_{CDS}. Fig. 6.19(b) shows that the simulated total input-referred noise can be further reduced to reach $0.37\,e^-_{rms}$.

6.4 Combination of SC CMS with Downscaled Technology

The optimal design of the SF and column-level amplification previously described for a 65 nm technology can be combined with the analog CMS. Transient noise simulations in ELDO for the readout chains based on the same three different in-pixel SFs can be used as a tool for validation.

6.4.1 Simulation Setup

Fig. 6.20 shows the three low-noise CIS readout chains with the SF transistors featuring the same parameters reported in Table 6.3. As expected before, transistors PMOS2.5 and PMOS1.2 should exhibit the best 1/f noise performance due to their lower N_t/C_{ox}^2 ratio [11]. The CMS is

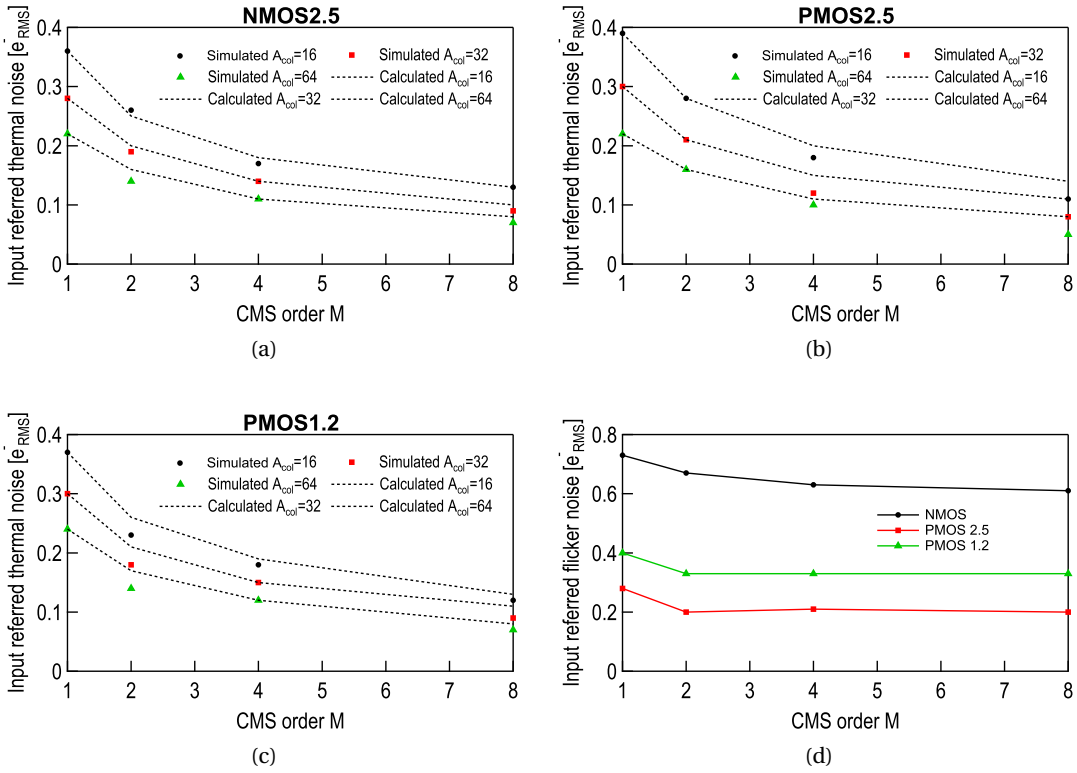


Figure 6.21: Input-referred thermal noise of the CIS readout chain with nMOS2.5 (a), pMOS2.5 (b) and pMOS1.2 (c) SF, respectively, as function of the column-level gain and the CMS order M. In (d) input-referred flicker noise of the CIS readout chain with different type of in-pixel SFs, as function of the CMS order M.

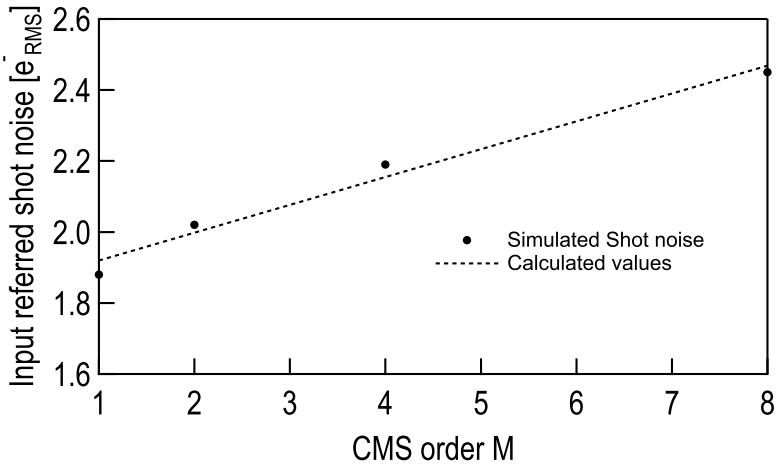
implemented with the same SC circuit described above and the timing diagram of Fig. 6.1(b) can be used as a reference. The line readout times corresponding to each CMS order range between 22 µs and 43 µs.

6.4.2 Noise Simulations Results

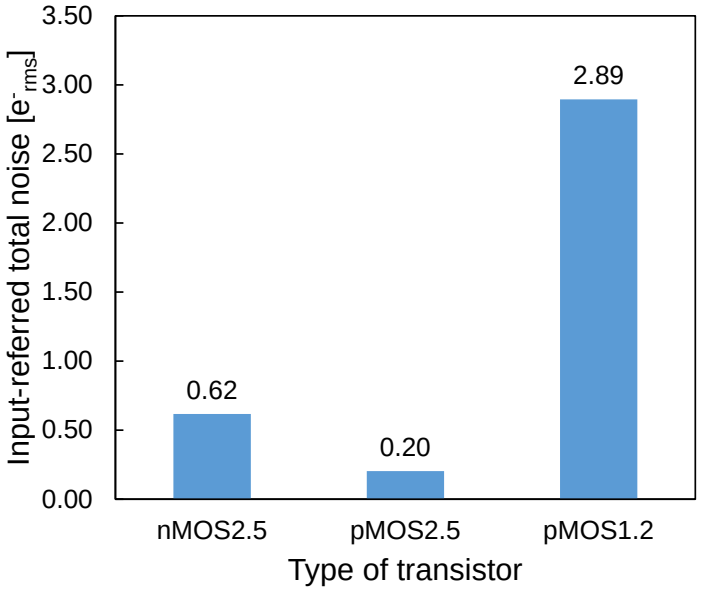
Thermal noise

The input-referred thermal noise, obtained from transient noise simulations performed with the ELDO circuit simulator, is shown in Fig. 6.21(a),(b) and (c), as a function of the CMS order M and the column-level gain A_{col}, for each of the three pixel configurations. The curves show that both the column-level gain and an increased CMS order reduce the thermal noise. The decrease in the input-referred thermal noise due to the CMS is proportional to $\sqrt{\mathrm{M}}$, as predicted by (5.19).

The mismatch between simulated and expected values can be explained by the additional



(a)



(b)

Figure 6.22: Input-referred shot noise in (a) of the CIS readout chain with pMOS1.2 SF. Input-referred total noise in (b) of the CIS readout chain with the NMOS2.5, PMOS2.5 and PMOS1.2 SF, respectively.

bandwidth limitation that the SCs introduce at the output of the column amplifier, further reducing the thermal noise contribution. For a column-level gain of 64, a C_L of 200 fF and a CMS order equal to 8, the input-referred thermal noise of each configuration is well below 0.1 e^-_{rms}. In fact, the readout chain based on both *n*MOS2.5 and *p*MOS1.2 feature an input-referred thermal noise of 0.07 e^-_{rms}, while the *p*MOS2.5 features a noise level of 0.05 e^-_{rms}. This confirms that, under this condition, the 1/f noise analyzed in the next section is dominant.

1/f Noise

Fig. 6.21(d) shows the results of 1/f noise simulations for each of the three readout chains shown in Fig. 6.20(a). As expected in the previous section, the pMOS1.2 and the pMOS2.5 exhibit the lowest input-referred flicker noise. The impact of CMS can be appreciated from the trend shown in Fig. 6.21(d) for the three readout chains. As expected theoretically, the 1/f noise reduction, as a function of CMS order, reaches a plateau after CMS of order 4.

The step in the input-referred flicker noise between simple CDS ($M = 1$) and CMS of orders 2 or 4 depends on the ratio between the sampling interval (T_{CDS} and T_{CMS}) and the signal settling time (τ). On the other hand, when various CMS orders are compared, the input-referred flicker noise is less influenced by the different T_{CMS}/τ ratios.

Fig. 6.21(d) shows that combining the pMOS2.5 as SF and using CMS of order 2 or higher, an input-referred flicker noise as low as 0.20 e^-_{rms} is reached, in contrast to 0.32 e^-_{rms}, obtained in the previous section when simple CDS is used with a T_{CDS} of 7 μs.

Leakage Current Shot Noise

As shown in the previous section, in the simulated 65 nm process, the pMOS1.2 transistor is the only one particularly concerned by the leakage current shot noise, due to its low oxide thickness (below 3 nm). In Chapter 5, it has been shown that the variance of the leakage current shot noise at the level of the SF increases linearly with the CMS order, starting from $M = 2$. Hence, the input-referred shot noise is expected to increase with $\sqrt{M}$. Fig. 6.22(a) shows the simulated input-referred gate leakage shot noise together with the theoretical values based on [26]. The input-referred shot noise appears to dominate the other noise sources for this thin oxide transistor.

Based on the shown results, the input-referred total noise has been calculated and shown in Fig. 6.22(b), for a A_{col} of 64 and a CMS of order 8. The pMOS2.5 transistor appears to be the best choice as in-pixel SF.

6.4.3 Photoelectron counting possibility

As explained in Chapter 4, the number of photoelectrons collected by each pixel can be modeled by a Poisson distribution. When the residual readout noise dominated by the in-pixel SF flicker noise is described by a Gaussian distribution [32] and added to the photon shot noise component, the quantization of the photon number disappears.

This phenomenon is shown in Fig. 6.23(a) to Fig. 6.23(d), where the noise levels of 0.5 e^-_{rms}, 0.3 e^-_{rms}, 0.2 e^-_{rms} and 0.1 e^-_{rms} are added to the histogram generated from an average number of 2 photons per pixel. The effect of the readout noise on the signal histogram is to broaden each peak and force each distribution to merge. An error in the photoelectron counting is

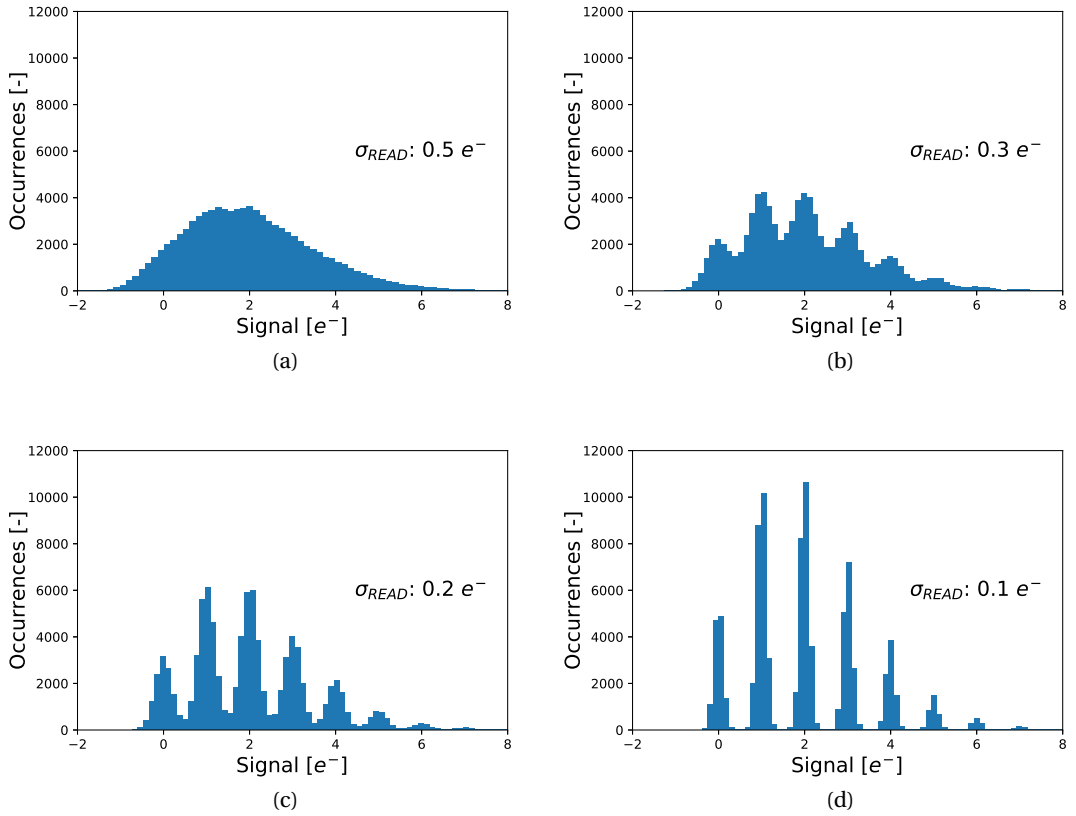


Figure 6.23: Simulated histogram from (a) to (d) showing the influence of different readout noise levels on the output of an image sensor for an average number of 2 photons per pixel.

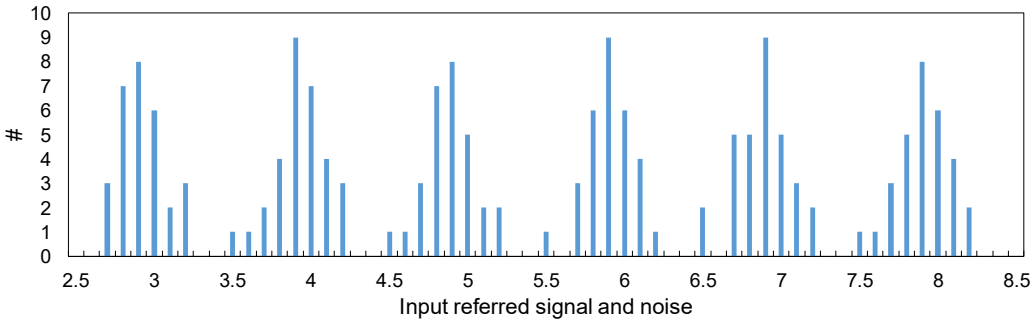


Figure 6.24: Histogram of the output signal voltage for 6 different inputs: results from the transient noise simulations of the readout chain in 65 nm with pMOS2.5 SF.

therefore made. As derived in [33] and shown in Fig. 6.23(d), to achieve a photoelectron counting error less than 0.1%, the readout noise needs to be reduced to values lower than 0.15 e^-_{rms}.

In the simulated 65 nm technology, the pMOS2.5 transistor appears to be the best choice as

in-pixel SF. Thanks to the combination of an advanced process, an optimized pixel, a high column-level gain (64) and CMS (order 8), the total noise of the readout chain based on the pMOS2.5 SF is reduced to the extremely low value of 0.20 e^-_{rms}. The noise performance of the readout chain based on PMOS2.5 SF is on the edge of true photoelectron counting at room temperature. Fig. 6.24 is the histogram of the input-referred signal when injecting into the SN a number of electrons ranging from 3 to 8. The histogram shows that the number of electrons can be easily quantified, thanks to the values of the valleys descending to zero.

6.5 Summary

This chapter describes a passive SC analog implementation of the CMS. After presenting the operation principle and giving a detailed noise analysis, this circuit is used to further reduce the total input-referred noise in CIS readout chains. The impact of the combination of the column-level gain and the CMS is validated experimentally with CIS readout chains in 180 nm embedding two different pixels, a variable gain CLA and a passive SC CMS circuit.

The noise measurements include PTCs for different gains and pixels and they show reasonably well that CMS reduces the 1/f noise by about 33% for order 8. This confirms the possibility to further reduce the total input-referred readout noise in CIS by making a proper use of CMS and at the same time validates the analytical formula for thermal and flicker noise in CIS readout chains.

This circuit noise reduction technique is also combined with an optimized choice for the SF in a downscaled 65 nm technology. The transient noise simulation results exhibits the low value of 0.20 e^-_{rms}, which opens up future possibilities in photoelectron counting.

State-of-the-Art Advancements

The passive SC implementation of the CMS was presented for the first time in [12], while this work shows its first implementation in silicon. One contribution of this work is the detailed noise analysis of the SC CMS circuit for a generic order M, which is based on the time propagation of the charge noise terms. Being validated by noise simulation results, this analysis confirms the noise performance of the SC CMS. The latter only depends on the values of the capacitors used for the averaging and the subtraction operations.

The main contribution of this work is the extensive validation of the noise model derived for an ultra-low noise readout chain. Since they play complementary roles, column-level amplification and CMS need to be combined and the described work aims to show the role of each noise reduction technique in order to define the optimum design configuration.

The technology downscaling effects on the CIS readout noise were predicted in [26]. Based on the transient noise simulations of an ultra-low noise readout chain in a 65 nm technology embedding an optimized pixel, a CLA and a SC CMS circuit, this work shows that ultra-low

noise CIS can benefit from downscaled technologies. The possible dominant role of the SF leakage current shot noise also is verified.

The temporal readout noise analysis were presented in [4] and [34]. The IC-based analysis shown in this chapter is based on the EKV formalism and can be used as a design methodology for a generic CIS technology. Compared to the previous noise models, the bias dependency of the model parameters is introduced e.g. the SF noise excess factor and the intrinsic capacitances. Contrary to previous models where a SI operation was assumed for the SF, this analysis shows that the optimum bias is in the MI region. This is an interesting result for CIS implementations in advanced technology nodes, where the bias in SI is rather difficult to achieve due to the reduced supply voltage [1].

References for Chapter 6

[1] C. Enz and E. Vittoz, *Charge-Based MOS Transistor Modeling: The EKV Model for Low-Power and RF IC Design*. Wiley, 2006.

[2] B. Razavi, *Design of Analog CMOS Integrated Circuits*. McGraw-Hill, first ed., 2001.

[3] A. Boukhayma, *Ultra Low Noise CMOS Image Sensors*. Springer Theses, 2018.

[4] A. Boukhayma, A. Peizerat, and C. Enz, "Temporal Readout Noise Analysis and Reduction Techniques for Low-Light CMOS Image Sensors," *IEEE Transactions on Electron Devices*, vol. 63, pp. 72–78, Jan 2016.

[5] F. Kusuhara, S. Wakashima, S. Nasuno, R. Kuroda, and S. Sugawa, "[paper] analysis and reduction technologies of floating diffusion capacitance in cmos image sensor for photon-countable sensitivity," *ITE Transactions on Media Technology and Applications*, vol. 4, no. 2, pp. 91–98, 2016.

[6] J. Ma and E. R. Fossum, "A pump-gate jot device with high conversion gain for a quanta image sensor," *IEEE Journal of the Electron Devices Society*, vol. 3, pp. 73–77, March 2015.

[7] M. Seo, T. Wang, S. Jun, T. Akahori, and S. Kawahito, "A 0.44e^-_{rms} read-noise 32fps 0.5Mpixel high-sensitivity RG-less-pixel CMOS image sensor using bootstrapping reset," in *2017 IEEE International Solid-State Circuits Conference (ISSCC)*, pp. 80–81, Feb 2017.

[8] S. Suh, S. Itoh, S. Aoyama, and S. Kawahito, "Column-Parallel Correlated Multiple Sampling Circuits for CMOS Image Sensors and Their Noise Reduction Effects," *Sensors*, vol. 10, no. 10, pp. 9139–9154, 2010.

[9] C. Lotto, P. Seitz, and T. Baechler, "A sub-electron readout noise CMOS image sensor with pixel-level open-loop voltage amplification," in *2011 IEEE International Solid-State Circuits Conference*, pp. 402–404, Feb 2011.

[10] A. Boukhayma, A. Peizerat, A. Dupret, and C. Enz, "Design optimization for low light CMOS image sensors readout chain," *New Circuits and Systems Conference (NEWCAS), 2014 IEEE 12th International*, pp. 241–244, June 2014.

[11] A. Boukhayma, A. Peizerat, and C. Enz, "A Sub-0.5 Electron Read Noise VGA Image Sensor in a Standard CMOS Process," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 9, pp. 2180–2191, 2016.

[12] A. Boukhayma, A. Peizerat, and C. Enz, "A correlated multiple sampling passive switched capacitor circuit for low light CMOS image sensors," in *2015 International Conference on Noise and Fluctuations (ICNF)*, pp. 1–4, June 2015.

[13] B. Murmann, "Thermal noise in track-and-hold circuits: Analysis and simulation techniques," *IEEE Solid-State Circuits Magazine*, vol. 4, pp. 46–54, Spring 2012.

[14] C. Enz, A. Caizzone, A. Boukhayma, and F. Krummenacher, "Simple Thermal Noise Estimation of Switched Capacitor Circuits Based on OTAs–Part I: Amplifiers with Capacitive Feedback," *arXiv preprint arXiv:1908.08099*, 2019.

[15] H. Bode, "Network Analysis and Feedback Amplifier Design," 01 1945.

[16] C. Enz, S. C. Rengifo, A. Boukhayma, and F. Krummenacher, "Simple Thermal Noise Estimation of Switched Capacitor Circuits Based on OTAs–Part II: SC Filters," *arXiv preprint arXiv:1908.08109*, 2019.

[17] C. Enz and G. Temes, "Circuit techniques for reducing the effects of op-amp imperfections: autozeroing, correlated double sampling and chopper stabilization.," *Proceedings of the IEEE*, vol. 84, no. 11, pp. 1584–1614, 1996.

[18] Terasic, "DE0-Nano Development and Education Board." https://www.terasic.com.tw/cgi-bin/page/archive.pl?No=593. Accessed on May, 2019.

[19] J. Janesick, *Photon Transfer*. SPIE Press, 2007.

[20] R. Capoccia, A. Boukhayma, and C. Enz, "Analysis of CMS noise reduction for 65 nm CIS," *2017 IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1–4, 2017.

[21] C. Enz, "Fundamentals of Noise in Electronic Devices," *Lecture notes from Techniques for Handling Noise and Variability in Analog Circuits, Mead course*, 2020.

[22] "STMicroelectronics Imaging Technology," Available on:https://www.st.com/content/st_com/en/about/innovation---technology/imaging.html. Accessed on June 2020.

[23] S. Takahashi, Y.-M. Huang, J.-J. Sze, T.-T. Wu, F.-S. Guo, W.-C. Hsu, T.-H. Tseng, K. Liao, C.-C. Kuo, T.-H. Chen, and et al., "A 45 nm Stacked CMOS Image Sensor Process Technology for Submicron Pixel," *Sensors*, vol. 17, p. 2816, Dec 2017.

[24] J. Ma and E. R. Fossum, "Quanta Image Sensor Jot With Sub 0.3e- r.m.s. Read Noise and Photon Counting Capability," *IEEE Electron Device Letters*, vol. 36, no. 9, pp. 926–928, 2015.

[25] Jung-Chak Ahn, Chang-Rok Moon, Bumsuk Kim, Kyungho Lee, Y. Kim, M. Lim, Wook Lee, Heemin Park, Kyoungsik Moon, Jaeryung Yoo, YongJei Lee, ByungJun Park, Sangil Jung, Junetaeg Lee, Tae-Hun Lee, YunKi Lee, Junghoon Jung, Jin-Hak Kim, Tae-Chan Kim, Hyunwoo Cho, Duckhyung Lee, and Yonghee Lee, "Advanced image sensor technology for pixel scaling down toward 1.0μm (Invited)," in *2008 IEEE International Electron Devices Meeting*, pp. 1–4, 2008.

[26] A. Boukhayma, A. Peizerat, and C. Enz, "Noise reduction techniques and scaling effects towards photon counting cmos image sensors," *Sensors*, vol. 16, p. 514, Apr 2016.

[27] C. Enz, F. Chicco, and A. Pezzotta, "Nanoscale MOSFET Modeling: Part 2: Using the Inversion Coefficient as the Primary Design Parameter," *IEEE Solid-State Circuits Magazine*, vol. 9, no. 4, pp. 73–81, Autumn 2017.

[28] M. A. Chalkiadaki, "Characterization and modeling of nanoscale MOSFET for ultra-low power RF IC design," *Ph.D. dissertation, EPFL, Dissertation 7030*, 2016.

[29] W. Deng and E. R. Fossum, "1/f noise modelling and characterization for cmos quanta image sensors," *Sensors*, vol. 19, p. 5459, Dec 2019.

[30] P. Bolcato and R. Poujois, "A new approach for noise simulation in transient analysis," in *[Proceedings] 1992 IEEE International Symposium on Circuits and Systems*, vol. 2, pp. 887–890 vol.2, 1992.

[31] BSIM (Berkeley Short-channel IGFET Model) Group, "BSIM4 4.8.2 MOSFET Model," Jan. 10, 2020 (BSIM4 4.8.2). Available on:http://bsim.berkeley.edu/models/bsim4/. Accessed on May 2020.

[32] D. M. Fleetwood, "1/f noise and defects in microelectronic materials and devices," *IEEE Transactions on Nuclear Science*, vol. 62, no. 4, pp. 1462–1486, 2015.

[33] E. R. Fossum, "Modeling the performance of single-bit and multi-bit quanta image sensors," *IEEE Journal of the Electron Devices Society*, vol. 1, no. 9, pp. 166–174, 2013.

[34] N. Kawai and S. Kawahito, "Noise analysis of high-gain, low-noise column readout circuits for cmos image sensors," *IEEE Transactions on Electron Devices*, vol. 51, no. 2, pp. 185–194, 2004.

7 Conclusion

CMOS image sensors performance in low light conditions is mainly affected by the read noise and the efficiency of the charge transfer process from the PPD to the SN. With the aim of improving ultra low light performance, the focus of this work is focused on two research directions: the charge transfer mechanism in Chapter 3 and the noise reduction techniques in Chapter 6. In this chapter, a summary is given for the main achievements and one for the main findings of this research, while at the end an overview of possible future work is presented.

7.1 Summary of Achievements

As discussed previously, ultra-low light CISs have reached extremely low values of total input-referred noise. When it comes to an additional noise reduction, a better understanding of the fundamental aspects of image sensors inevitably has a crucial role. The work presented here continues the effort in modeling ultra-low noise CISs. The journey, from the analytical derivation on a piece of paper, through the device and circuit simulations to the measurement results, brought many challenges but also resulted in some interesting ideas. The most important ones are summarized here:

- The potential barrier at the interface between the PPD and the region beneath the TG was reported in [1]. In this work, the concept of modulation of the barrier due to the TG voltage and the PPD charge allowed to match the model results of the charge transfer current with the TCAD simulations of a 3D structure. If coded by using a device descriptive language, the model might be included in a SPICE-like circuit simulator for simulations of the pixel together with the readout chain (mixed-mode simulations).
- The measurements of different pixel designs were compared with model trends in [2] and [3]. In this work, the experimental verification in Chapter 3 is a direct comparison for specific sensor operating conditions. The obtained match between the analytical model and measurements with reasonable values of the model parameters is an essential step towards the inclusion in the model of additional levels.

- The empirical expression for the flicker noise reduction factor, $\alpha_{1/f}$, introduced in Chapter 5 is able to capture the scaling of the 1/f noise reduction with the CMS order for different values of the readout cut-off frequency and the CMS sampling period. It also shows the plateau reached in the 1/f noise reduction for CMS orders larger than 16.

- The column-level gain and the correlated multiple sampling are well-known noise reduction techniques used in ultra-low noise CISs [4]. The extensive validation of the noise model shown in this work in Chapter 6 highlights their complementary roles and the need to combine them in order to achieve the minimum input-referred noise.

- The additional readout noise reduction due to the CIS technology downscaling was predicted in [5]. This work uses the transient noise simulation results of a 65 nm technology in order to verify the possibility of photoelectron counting in CISs and to warn about a possible new dominant noise source given by the SF leakage current shot noise.

- The temporal readout noise analysis were presented in [6] and [7]. The novel design methodology based on the IC coefficient shown in Chapter 6 is based on the EKV formalism and can be used for optimum design in a generic CIS technology. Compared to previous ones, the proposed noise model includes the bias dependency of the parameters involved e.g. the SF noise excess factor and the intrinsic capacitances, and predicts an optimum bias of the SF in MI.

7.2 Main Findings

Regarding the compact modeling of charge transfer in PPDs

- The electrostatic analysis of the PPD structure defines the main parameters of the device and illustrates how the potential well for the photogenerated electrons is obtained.

- The electrostatic analysis of the charge transfer path is carried out in order to model the potential barrier between the charge accumulation region and the semiconductor beneath the TG. This barrier limits the charge transfer in terms of minimum required transfer time and voltage applied to the TG.

- When the transfer is only limited by the potential barrier between the PPD and TG, the proposed model is able to predict the charge transfer current. The thermionic emission current mechanism, full-depletion approximation and barrier modulation due to V_{TG} and V_{PPD} are the key elements to express the charge transfer current.

- An analytical expression of the transferred charges from the PPD to the SN is derived from the TCAD validated model and it is used to experimentally validate the model as a function of the initial charge stored in the PPD, the transfer time and the voltage applied to the TG. The output measurements from a readout chain in a 0.18 µm CIS technology are used to compare with the model results, where a good match is obtained.

Regarding the temporal readout noise reduction techniques

- Measurement results confirm that column-level amplification, A_{col}, reduces thermal noise following a $1/\sqrt{(A_{col})}$ trend and plays the key role of mitigating the noise contribution of the following stages in the CIS readout chain.
- The CMS reduces thermal noise in the same way the column-level amplifier does, but unlike amplification, it can not reduce the noise originating from next stages in the readout chain. Based on analytical and simulation results, CMS further reduces 1/f noise.
- The CMS noise reduction is validated by implementing the CMS as a passive SC circuit. Based on the derived analytical expression for the output noise and simulation results, the contribution of the SC CMS to the total noise is not influenced by the CMS order, M.
- When column-level amplification and CMS are combined, they play complementary roles. With a moderate column-level gain, the CMS reduces both the thermal and the residual 1/f noise without an impact on the dynamic range and the readout time.
- The model for the input-referred thermal and flicker noise charge variances is validated by the obtained good match with the measurement results from readout chains exploiting two different pixel types, a conventional CLA and a passive SC CMS circuit are implemented in a 0.18 µm CIS technology.
- The 1/f noise reduction can benefit from a higher value of C_{ox} in downscaled technologies. However, the best choice does not correspond directly to the highest C_{ox}, but the value of the charge trap density, N_{t}, needs to be taken into consideration. Transistor-level simulations show promising results but point out also the serious challenges regarding the gate tunneling leakage current.
- When the pixel SF optimization and column-level gain in an advanced process is combined with CMS, transient noise simulations show that an input-referred noise as low as $0.20\,\mathrm{e^-_{rms}}$ can be reached with a thick oxide pMOS SF, $M = 8$ and $A_{\mathrm{col}} = 64$, and photoelectron counting can therefore be envisaged.
- The analysis of the total input-referred charge noise against the inversion coefficient, IC, predicts that in downscaled technologies the optimum bias for the SF shifts to the MI region. Since in previous models the SF is assumed to operate in SI, this result is interesting for future CIS implementations. Due to the reduced supply voltage, the bias in SI is in fact difficult to achieve in advanced technologies [8].

7.3 Future Work

Due to time and resources, the scope of this work is limited and does not look into all the different paths that appeared during the research. A list of possible future directions is provided

below.

Regarding the compact modeling of charge transfer in PPDs

- The modeled charge transfer in PPDs is derived and verified under the assumption that the SN voltage is constant throughout the entire transfer process. This assumption limits the transfer mechanism only to the properties of the PPD and TG and considerably reduces the complexity of the model. This assumption is reasonable for low illumination levels, where the amount of transferred charges is a fraction of the photodiode full well capacity. The variation of the SN voltage is considerable when the amount of transferred charges is high, and could result in signal charges spilling back to PPD when the TG pulse returns to a low value [9]. The impact of the SN voltage variations on the charge transfer must be added to the model shown in this manuscript in order to extend the model to high illumination levels [3].
- The TCAD simulation results are obtained from a structure based on generic steps of fabrication, with specific parameters that are not calibrated to any particular process. Even though such information are very difficult to obtain, the developed model for the charge transfer current must be extensively verified for different implementations of the PPD.
- The experimental verification of the model presented in this manuscript was implemented by using only the available test equipment. More emphasis should be placed on verifying the model for different pixel designs and fabrication process.

Regarding the temporal readout noise reduction techniques

- The SC CMS circuit can be integrated in a full image sensor. The reason for an implementation as a single readout chain was to simplify the experimental characterization. The main goal in this work was the extensive validation of the noise model. An implementation as a full sensor would give the opportunity to evaluate this circuit technique with fuller statistics based on the number of pixels and to evaluate the circuit performance with captured frames.
- Advanced technology nodes for CISs are already available on the market, but their accessibility for academic researchers is still very limited due to the cost and currently more industrial orientation. This work predicts and verifies with simulation results that technology scaling can potentially improve sensor noise performances and possibly novel dominant source of noise needs to be considered.

References for Chapter 7

[1] E. R. Fossum and D. B. Hondongwa, "A Review of the Pinned Photodiode for CCD and CMOS Image Sensors," *IEEE Journal of the Electron Devices Society*, vol. 2, no. 3, pp. 33–43, 2014.

[2] A. Pelamatti, *Estimation and Modeling of Key Design Parameters of Pinned Photodiode CMOS Image Sensors for High Temporal Resolution Applications*. PhD thesis, Université de Toulouse, 2015.

[3] L. Han, S. Yao, and A. J. P. Theuwissen, "A Charge Transfer Model for CMOS Image Sensors," *IEEE Transactions on Electron Devices*, vol. 63, pp. 32–41, Jan 2016.

[4] P. Seitz and A. Theuwiseen, *Single-Photon Imaging*. Springer Series in Optical Sciences, 2011.

[5] A. Boukhayma, A. Peizerat, and C. Enz, "Noise reduction techniques and scaling effects towards photon counting cmos image sensors," *Sensors*, vol. 16, p. 514, Apr 2016.

[6] A. Boukhayma, A. Peizerat, and C. Enz, "Temporal Readout Noise Analysis and Reduction Techniques for Low-Light CMOS Image Sensors," *IEEE Transactions on Electron Devices*, vol. 63, pp. 72–78, Jan 2016.

[7] N. Kawai and S. Kawahito, "Noise analysis of high-gain, low-noise column readout circuits for cmos image sensors," *IEEE Transactions on Electron Devices*, vol. 51, no. 2, pp. 185–194, 2004.

[8] C. Enz and E. Vittoz, *Charge-Based MOS Transistor Modeling: The EKV Model for Low-Power and RF IC Design*. Wiley, 2006.

[9] J. Xu, R. Wang, L. Han, and Z. Gao, "Analysis and modeling of spill back effect in high illumination cmos image sensors," *IEEE Sensors Journal*, vol. 20, no. 6, pp. 3024–3031, 2020.

A Appendix

A.1 Electrostatics in PPD device

By solving the Poisson equation, the electric field and the potential profiles in the PPD device are respectively given by

$$\begin{aligned}
\mathscr{E}(x) = & \\
& -\frac{qN_{\mathrm{A}^+}}{\varepsilon_{\mathrm{s}}}(x-x_{\mathrm{p1}})\left[u(x-x_{\mathrm{p1}})-u(x-x_{\mathrm{n}})\right]+ \\
& +\left[\frac{qN_{\mathrm{D}}}{\varepsilon_{\mathrm{s}}}(x-x_{\mathrm{n}})+\mathscr{E}(x_{\mathrm{n}})\right]\left[u(x-x_{\mathrm{n}})-u(x-x_{\mathrm{p}})\right]+ \\
& +\left[-\frac{qN_{\mathrm{A}}}{\varepsilon_{\mathrm{s}}}(x-x_{\mathrm{p2}})+\mathscr{E}(x_{\mathrm{p}})\right]\left[u(x-x_{\mathrm{p}})-u(x-x_{\mathrm{p2}})\right],
\end{aligned} \tag{A.1.1}$$

$$\begin{aligned}
\psi(x) = & \\
& +\frac{qN_{\mathrm{A}^+}}{2\varepsilon_{\mathrm{s}}}(x-x_{\mathrm{p1}})^2\left[u(x-x_{\mathrm{p1}})-u(x-x_{\mathrm{n}})\right]+ \\
& \left[-\frac{qN_{\mathrm{D}}}{2\varepsilon_{\mathrm{s}}}(x-x_{\mathrm{n}})^2+\frac{qN_{\mathrm{A}^+}}{\varepsilon_{\mathrm{s}}}(x_{\mathrm{n}}-x_{\mathrm{p1}})\,x+\psi(x_{\mathrm{n}})\right] \\
& \left[u(x-x_{\mathrm{n}})-u(x-x_{\mathrm{p}})\right]+ \\
& +\left[\frac{qN_{\mathrm{A}}}{2\varepsilon_{\mathrm{s}}}(x-x_{\mathrm{p2}})^2+\psi(x_{\mathrm{p}})\right]\left[u(x-x_{\mathrm{p}})-u(x-x_{\mathrm{p2}})\right],
\end{aligned} \tag{A.1.2}$$

where $u(x-x_0)$ is the step function and is equal to unity when $x>x_0$ and zero elsewhere.

A.2 Electrostatics along path A

Solving Poisson equation under full-depletion approximation leads to the electric field $\mathscr{E}(a)$ and electrostatic potential $\psi(a)$ along the path A between a_2 and a_5, given by the following expressions

$$\begin{aligned}
&\mathscr{E}(a) = \\
&\quad \left[E_{\mathrm{s}} - \frac{qN_{\mathrm{A}^+}}{\varepsilon_{\mathrm{s}}}(a-a_2)\right][u(a-a_2)-u(a-a_5)]\,, \\
&\psi(a) = \\
&\quad \left[\psi_{\mathrm{s}} - E_{\mathrm{s}}(a-a_2) + \frac{qN_{\mathrm{A}^+}}{2\varepsilon_{\mathrm{s}}}(a-a_2)^2\right] \\
&\quad [u(a-a_2)-u(a-a_5)]\,,
\end{aligned} \tag{A.2.1}$$

where ψ_{s} is the surface electrostatic potential and E_{s} the electric field at the surface, obtained by $\psi_{\mathrm{s}} = x_{\mathrm{d}}^2 q\, N_{\mathrm{A}^+}/2\,\varepsilon_{\mathrm{s}}$ and $E_{\mathrm{s}} = -x_{\mathrm{d}} q\, N_{\mathrm{A}^+}/\varepsilon_{\mathrm{s}}$.

Moreover, to obtain (3.9), the following expression for the depletion region, x_{d}, in a metal-oxide-semiconductor is used

$$x_{\mathrm{d}} = -\frac{\varepsilon_{\mathrm{s}}}{C_{\mathrm{ox}}} + \sqrt{\left(\frac{\varepsilon_{\mathrm{s}}}{C_{\mathrm{ox}}}\right)^2 + \frac{\varepsilon_{\mathrm{s}}}{2qN_{\mathrm{A}^+}}V_{\mathrm{TG}}}\,. \tag{A.2.2}$$

This has been derived by solving Poisson equation of the TG MOS structure [1].

References for Appendix

[1] J. Janesick, *Scientific Charge-Coupled Devices*. SPIE Press, 2001.

List of Publications

Journal Papers

- **R. Capoccia**, A. Boukhayma, F. Jazaeri and C. Enz, "Compact Modeling of Charge Transfer in Pinned Photodiodes for CMOS Image Sensors," in IEEE Transactions on Electron Devices, vol. 66, no. 1, pp. 160-168, Jan. 2019.
- **R. Capoccia**, A. Boukhayma and C. Enz, "Experimental Verification of the Impact of Analog CMS on CIS Readout Noise," in IEEE Transactions on Circuits and Systems (TCAS) I: Regular Papers, vol. 67, no. 3, pp. 774-784, March 2020.
- **R. Capoccia**, T. Spreij, A. Boukhayma and C. Enz, "Experimental Verification of Charge Transfer Model in Pinned Photodiode for CMOS image sensors," to be submitted to IEEE Transactions on Electron Devices (in preparation).

Conference Papers

- **R. Capoccia**, A. Boukhayma and C. Enz, "Sub-electron CIS noise analysis in 65 nm process," 2016 IEEE International Conference on Electronics, Circuits and Systems (ICECS), Monte Carlo, 2016.
- **R. Capoccia**, A. Boukhayma and C. Enz, "Analysis of CMS noise reduction for 65 nm CIS," in IEEE International Symposium on Circuits and Systems (ISCAS), Baltimore, 2017.
- **R. Capoccia**, A. Boukhayma and C. Enz, "A kTC Noise Analysis in a Passive Switched-Capacitor Correlated Multiple Sampling Circuit for CIS," 2019 International Conference on Noise and Fluctuations (ICNF), Neuchâtel, 2019.
- A. Boukhayma, A. Caizzone, **R. Capoccia** and C. Enz, "Design and Optimization of Low Power and Low Light Sensor: (Invited)," 2020 IEEE Custom Integrated Circuits Conference (CICC), Boston, 2020.
- F. Chicco, **R. Capoccia**, A. Pezzotta and C. Enz, "Linear analysis of phase noise in LC oscillators in deep submicron CMOS technologies," 2017 International Conference on Noise and Fluctuations (ICNF), Vilnius, 2017.

Raffaele CAPOCCIA

Electronic Engineer

Date of Birth: July 24th, 1990
Nationality: Italian
Address: Rue des Saars 2, Neuchâtel 2002, Neuchâtel (Switzerland)

raffaele.capoccia@epfl.ch

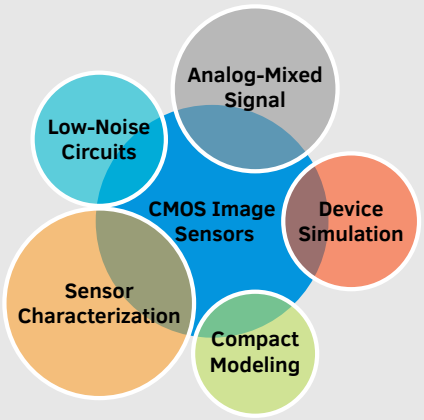
CH: +41 (0)77 990 54 66

linkedin.com/in/raffaele-capoccia-124977103

live:capoccia.raffaele

https://goo.gl/GMW7tB

Skills



Interests

- Image Sensor Design
- Analog-Mixed Signal Design
- Opto-Electrical Device Simulations
- Novel Pixel Design
- Experimental Characterization

References

- Christian Enz
  christian.enz@epfl.ch
- Assim Boukhayma
  assim.boukhayma@epfl.ch
- Farzan Jazaeri
  farzan.jazaeri@epfl.ch

Summary

My PhD in Microelectronics focuses on the modeling of pinned photodiodes and design of low-noise CMOS image sensor readout chains. During my Phd, I learned the basic skills in device modeling and simulation, low-noise readout chain design and image sensor characterization. Before starting my PhD, I also worked on the hardware implementation of a multiple camera image processing algorithm for depth mapping. I take the most work satisfaction from working in a multidisciplinary team.

Experience

Oct 2015 - Now — **PhD** — **ICLAB - EPFL**, Neuchâtel, Switzerland
Actions implemented:
Performed bibliographic research on low noise CMOS image sensors. Simulated the impact of downscaled technology and analog noise reduction techniques on CIS readout noise. Developed the core of a compact model for the charge transfer in Pinned Photodiodes and verified the theory with TCAD simulations. Designed and characterized a tape out of low noise CIS readout chains with pixels optimized for noise.

July 2019 - Dec 2019 — **Intern** — **Facebook - Oculus**, Redmond, USA
Actions implemented:
Implemented an environment for image sensor characterization. Fully characterized the novel image sensor developed for AR/VR application.

Dec 2014 - Apr 2015 — **Intern** — **LSM - EPFL**, Lausanne, Switzerland
Actions implemented:
Simulated the hardware implementation of a disparity estimation algorithm for depth mapping. Tested on FPGA the real-time Full HD trinocular depth map estimator.

Education

Sept 2012 - Oct 2014 — **MSc, Electronic Engineering** — **Polytechnic of Turin**, Italy
Specialization: Electronic Systems
Grade: 110/110 cum Laude
Thesis Title: Real Time Hardware Implementation of Multiple Camera Depth Map Estimation
Major: Analog Circuit Design, Digital System Design, Integrated Circuits and Architectures, Microelectronics, Low Power Electronic Systems.

Sept 2009 - Oct 2012 — **BSc, Electronic Engineering** — **Polytechnic of Turin**, Italy
Grade: 110/110 cum Laude
Major: Circuit Theory, Analog Electronics, Digital Electronics, Semiconductor Devices Physics and Technology, Control Theory, Programming.

Extra-curricular activities and interests

Reviewer	Reviewed articles for IEEE conferences.
Volunteer	European Solid State Circuits Conference 2016. International Conference on Noise and Fluctuations 2019.
Student Association	IEEE Student Branch at EPFL.
Other	Soccer and guitar player.

Computer Skills

- Cadence Virtuoso, Calibre
- Synopsys TCAD
- VHDL, Verilog, Modelsim
- Matlab, Python, C
- Latex, MS Office, Igor Pro

Languages

- **Italian:** Mother Tongue
- **English:** C1 level
- **French:** B1 level