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par

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It is about how hard you can get hit and keep moving forward,
how much can you take and keep moving forward.
That's how winning is done!

Nessuno può colpire duro quanto può colpire la vita,
perciò andando avanti non è importante come colpisci,
l'importante è come sai resistere ai colpi,
a come incassi e se finisci al tappeto hai la forza di rialzarti!
(Doppiaggio italiano)

— Rocky Balboa (Sylvester Stallone)

Alla mia famiglia…

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Lausanne, 2 December 2019 Giovanni Santoruvo

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Abstract

Gallium Nitride (GaN) and all III-Nitride compounds have revolutionized the world with the development of the blue light emitting diode (LED). In addition, GaN-based epi-structures, such as AlGaN/GaN, enable the fabrication of high electron mobility transistors (HEMTs) for several applications handling high power. In the radio frequency (RF) domain, power amplifiers (PAs) based on GaN HEMTs are currently used for base stations, radars and, in the future, will replace low power amplifiers, currently made with silicon, ensuring much smaller footprint and reduced cost.

Despite the presence of several commercial GaN HEMT-based devices, performances, especially in frequency, are quite far from the predicted theoretical limits. A lot of research focuses in using etched AlGaN/GaN HEMT nanowires (NWs) as channel for ultrascaled metal semiconductor field-effect transistors (MESFETs) to reduce short channel effects, arising when shrinking the gate length to increase the operating frequency, and linearity issues.

In this thesis, we perform a transverse study of AlGaN/GaN NWs starting from the investigation of electron transport and ending with the proposal of new device architectures for improved device performance.

Electron transport is studied in mesoscopic devices based on GaN HEMT NWs. Ballistic transport is observed even at room temperature and at large bias, thanks to the high mobility of electrons and large optical phonon energy. Quenched Hall effect and quantum physics phenomena due to phase coherence are observed at cryogenic temperature under a strong magnetic field. Finally, the sidewall depletion width, an important parameter for designing devices based on NWs, of AlGaN/GaN is extracted, resulting in one of the smallest values (19.5 nm) among all III-V HEMTs.

Due to the increased parasitic capacitance in NW-based MESFETs, we also explored more exotic gating techniques consisting of side and in-plane gates (IPGs). IPGFETs and metal IPGFETs (M-IPGFETs) are fabricated, characterized and simulated. A record current density of 1.4 A/mm and transconductance of 665 mS/mm are measured, together with a breakdown voltage larger than 300 V. Simulations of the device capacitance yield values as low as few aF, resulting in possible cut-off frequencies up to 0.89 THz. Such value, together with the large breakdown voltage, push GaN IPGFETs beyond the theoretical limit of GaN for RF applications and paves the way for future device architectures.

NWs are also used to noticeably improve performance of zero-bias RF detectors. We developed for the first time a field-effect rectifier (FERs) where the channel is constituted by an array of GaN-HEMT etched NWs. The much better gate control over NWs resulted in a current curvature

(30.1 V^{-1}) close to the theoretical limit of Schottky diodes (38.7 V^{-1}). The cut-off frequency of these devices is up to 140 GHz, which, together with the large measured responsivity (3000 V/W), make NW-FERs very promising for stand-alone applications as well as for integration in GaN Monolithic Microwave Integrated Circuits (MMICs) for improving overall performance and add new applications.

Key words: HEMT, Ballistic transport, III-Nitride, Microwave detection, Nanowires, Quantum effect, RF transistor, Side gate

Riassunto

Il nitruro di gallio (GaN) e tutti i nitruri basati su elementi appartenenti alla quinta colonna della tavola periodica hanno rivoluzionato il mondo con lo sviluppo dei LED (in inglese light emitting diode) blu. In aggiunta, strutture epitassiali basate sul GaN, hanno permesso la realizzazione di transistor con elettroni ad elevata mobilità (in inglese high electron mobility transistors, HEMT) per diverse applicazioni ad alta potenza. Nel campo delle radio frequenze (RF), gli amplificatori di potenza basati su GaN HEMT sono attualmente utilizzati nelle stazioni radio, radar e, in futuro, sostituiranno anche gli amplificatori a più bassa potenza, attualmente fabbricati in silicio, assicurando dimensioni e costi ridotti.

Nonostante la presenza sul mercato di diversi dispositivi basati su GaN HEMT, le prestazioni, specialmente in frequenza, sono ancora lontane dai valori predetti teoricamente. Molta ricerca è focalizzata sull'uso di nanowire (NW, letteralmente fili di dimensioni nanometriche) incisi partendo da dei wafer di AlGaN/GaN HEMT. Questi NW costituiscono il canale per transistor a effetto di campo basati su giunzioni metallo-semiconduttore, con lo scopo di ridurre gli effetti di canale corto, necessario per aumentare la massima frequenza operativa, e ridurre i problemi di non linearità.

In questa tesi, abbiamo studiato trasversalmente i nanowire basati su AlGaN/GaN iniziando con lo studio di trasporto di elettroni in queste strutture e finendo con delle proposte riguardanti nuove architetture al fine di migliorarne le prestazioni di dispositivi operanti nel campo RF.

Il trasporto degli elettroni è stato studiato in dispositivi mesoscopici basati sui NW di GaN HEMT. Il moto balistico degli elettroni è stato osservato sia a temperature criogeniche (4 K o -269.15 °C) che a temperatura ambiente a elevate tensioni di alimentazione, grazie all'alta mobilità degli elettroni e alla notevole energia richiesta per generare fononi ottici. L'appiattimento dell'effetto Hall (Quenched Hall effect) e fenomeni quantistici legati alla correlazione di fase degli elettroni sono stati osservati a temperature criogeniche e sotto l'effetto di forti campi magnetici. Per concludere, la larghezza di deplezione laterale, un importante parametro per progettare dispositivi basati sui nanowire, è stata estratta ottenendo uno dei valori più piccoli (19.5 nm) ottenibile in qualsiasi HEMT.

Per ridurre le capacità parassite e problemi di trappole nel semiconduttore quando si usano nanowire, abbiamo esplorato la possibilità di controllare il canale lateralmente. Lo studio è iniziato da dispositivi a singolo nanowire con gate complanare (in-plane gate field-effect transistors IPGFETs). Valori record sia di corrente, 1.4 A/mm, che di transconduttanza, 665 mS/mm, sono stati misurati per questi dispositivi. Inoltre, considerando i valori di capacità simulati (pochi aF), delle frequenze di taglio fino 0.89 THz dovrebbero essere raggiungibili. A

ciò si aggiunge anche un valore estremamente alto per la tensione di rottura del dispositivo di 300 V. Questi parametri sono stati in seguito migliorati tramite trattamenti chimici e usando gate metallici (metal-IPGFET). Questi ultimi, in particolare, permettono anche di ridurre la resistenza di gate e rendono i M-IPGFET ideali per fabbricare dispositivi con più nanowire in parallelo, al fine di aumentare la potenza in uscita.
I nanowire sono stati anche utilizzati per migliorare le prestazioni di rilevatori di potenza RF non polarizzati (nessuna alimentazione è richiesta per il funzionamento). Abbiamo creato per la prima volta un rettificatore a effetto di campo (field-effect rectifier, FER) che utilizza una stringa di nanowire incisi su un wafer di GaN-HEMT. Grazie al miglior controllo della corrente nei nanowire, abbiamo raggiunto valori di curvatura di corrente (30.1 V^{-1}) vicini al limite teorico previsto per i diodi Schottky (38.7 V^{-1}). La frequenza di taglio di questi dispositivi arriva fino a 140 GHz insieme a un'elevata responsività misurata di 3000 V/W. Tale combinazione di prestazioni rende questi dispositivi molto promettenti sia per applicazioni semplici che per l'integrazione in circuiti monolitici a microonde (Monolithic Microwave Integrated Circuits, MMICs) basati su GaN per migliorarne le prestazioni e aggiungere nuove funzionalità.

Symbols and Acronyms

Symbols

Symbol	Quantity	Measurement unit or value
a	Lattice constant	Å
B	Magnetic field	T
β	Responsivity	V/W
Bw	Frequency bandwidth	Hz
CTE	Coefficient of thermal expansion	K^{-1}
Δa	Lattice mismatch	%
$\Delta\lambda$	Thermal mismatch	%
$DIBL$	Drain induced barrier lowering	mV/V
E_{OP}	Optical phonon energy	eV
E_F	Fermy energy	J
ϵ	Relative dielectric constant	
ϵ_0	Vacuum dielectric constant	8.85×10^{-12} F/m
f_c	Cutoff frequency	Hz
G_0	Conductance quantum	~80 μS
γ	Current curvature	V^{-1}
γ_0	Current curvature at 0 V	V^{-1}
g_m	Transconductance	S
h	Plank constant	6.62×10^{-34} m^2kg/s
$\hbar$	Cut Plank constant	2.1×10^{-34} m^2kg/s
I_r	Reverse current	A
$JFoM$	Johnson figure of merit	MV/s
J	Current density	A/m
k_bT	Boltzmann constant	1.38×10^{23} $m^2kg/\ s^2/K$
λ	Thermal coefficient	W/cm/K
l_c	Cyclotron radius	nm
L_G	Gate length	nm
l_m	Mean free path	nm
l_ϕ	Phase coherence length	nm
M	Number of modes	
m^*	Effective mass	kg
μ	Mobility	cm^2/Vs

NEP	Noise equivalent power	$\mathrm{pW}\sqrt{\mathrm{Hz}}$
n_s	Sheet carrier concentration	cm^{-2}
$P_\text{in-RF}$	RF input power	dBm
p_x,p_y	Momentum in x and y	m^2/s
q	Electronic charge	$1.602\mathrm{X}10^{-19}$ C
R_0	Resistance quantum	~12.5 kΩ
R_d	Differential resistance	Ω
R_d0	Differential resistance at 0 V	Ω
RT	Room temperature	300 K
SS	Subthrehsold slope	mV/dec
τ	Mean free time	s
V_br	Breakdown voltage	V
v_f	Fermi velocity	cm/s
V_Jn	Johnson (thermal) noise voltage	V
V_on	Turn-on voltage	V
v_sat	Saturation velocity	cm/s
V_t	Thermal voltage	V
W_NW	Nanowire width	nm
w_sd	Sidewall depletion width	nm

Acronyms

Abbreviation	Full name
2DEG	2-Dimensional Electron Gas
AC	Alternate Current
BOE	Buffered Oxide Etch
CMOS	Complementary Metal Oxide Semiconductor
DC	Direct Current
DI	Deionezed water
DUT	Device under test
EBL	Electron-Beam Lithography
GND	Ground
HCl	Cloridric acid
HEMT	High Electron Mobility Transistor
HSQ	Hydrogen Silsesquioxane
ICP RIE	Inductive coupled plasma reactive-ion
KOH	Potassium hydroxide
MESFET	Metal-Semiconductor Field-Effect Transistor
MMIC	Monolithic Microwave Integrated Circuits
MOSFET	Metal Oxide Semiconductor Field-Effect Transistor
NW	Nanowire
PA	Power Amplifier
PMMA	Polymethyl methacrylate
RF	Radio Frequency
RT	Room Temperature
RTP	Rapid thermal process
SCE	Short Channel Effect
TMAH	Tetramethylammonium hydroxide
UCF	Universal Conductance Fluctuations
VNA	Vector Network Analyzer
WL	Weak Localization

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1 Introduction

Internet of Things IoT is a network superstructure where different objects (“things”), humans, and computing devices are identified by a UID (unique identifier) and data communication can also happen without any human action [1].

IoT is supposed to revolutionize our lives in the near future leading to autonomous cars, smart homes, improvements in healthcare and in many fields of human activities. The basic idea behind IoT is that every element in the network can communicate with others once an internet access is granted (Fig. 1.1).

The fifth generation of mobile communication (also known as 5G) will ensure a network access to mobile phones and remote embedded systems with unprecedented data rate (to enable 4K and 8K streaming), extremely small latency (very important for autonomous driving and telesurgery, for example) and high connection density (billions of devices are expected to be connected). Fig. 1.2 quantitatively describes the performance of 5G and the comparison with its predecessor (4G).

The 5G infrastructure is based on a large number of cells with different dimensions, power, and

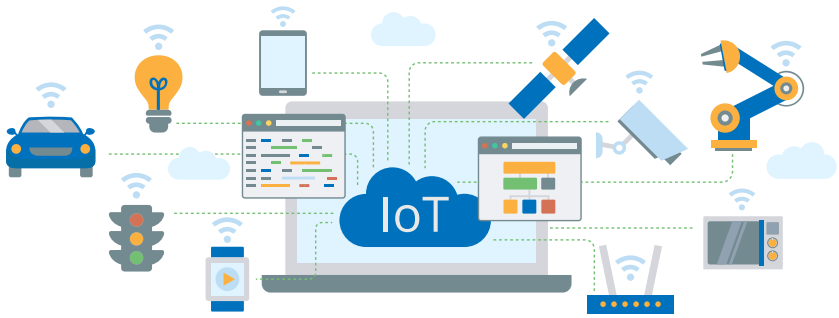


Figure 1.1 – Schematic (from ScienceSoft) showing the concept of the internet of things. Every object, from home appliances and wearable objects to industrial machines and city facilities, is connected to the cloud, which can be accessed from several devices and allows both monitoring and remote control in real-time.

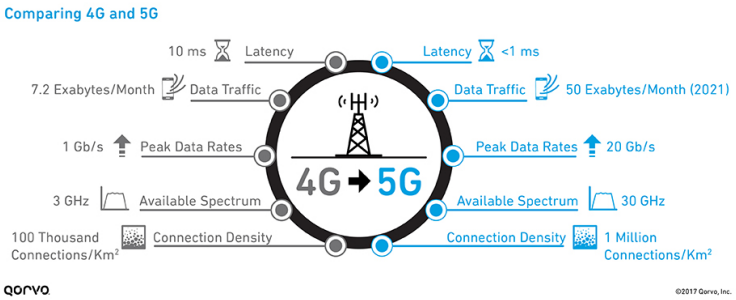


Figure 1.2 – Illustration (from Qorvo) of the main differences between the fourth and fifth generation of mobile communications. All the improvements are essential for the real development of IoT. For example, the small latency is necessary for autonomous driving and remote control (e.g., telesurgery), while the 10X larger connection density is the basement for connecting several "things".

numbers of user capabilities [2]. For low-power cells (femto and pico cells), the required power can be easily delivered from low-doping metal oxide semiconductor (LDMOS) technology on silicon. For larger cells, the higher power demand (up to tens of watts) makes devices based on Si and GaAs very inefficient and space-consuming.

Gallium Nitride (GaN) and the entire family of III-Nitride semiconductors, thanks to their physical properties (which will be later discussed), are more favorable for high power applications; thus, they do and will play a more and more relevant role. In addition, GaN-based devices will also have an impact on low power applications since they can deliver the same power in a smaller footprint, besides the reduced device resistance also allows an easy matching with the antenna yielding in a strong, and further, reduction of the overall required footprint (thus cheaper and more economical appealing systems) [3] .

In the next sections, we will discuss GaN and other III-Nitride compounds, together with the physical properties that make these materials very favorable for 5G applications and several more. Later we will review the state of the art of GaN devices for RF applications and we will highlight some issues in current technologies. Finally, we will talk about the use of nanowires (NWs) to enhance performance for the next generation of GaN electronic devices.

1.1 Physical properties of Gallium Nitride for RF applications

Gallium Nitride is the most known binary compound of the family of III-Nitrides, where we can also find Indium Nitride (InN), Aluminum Nitride (AlN) and Boron Nitride (BN, though it is investigated more as 2D material than bulk).

One of the main advantages of III-Nitrides is the property to tune the band gap from 0.6 eV of InN up to 3.39 eV of GaN and 6.1 eV of AlN. Intermediate values are obtained by using ternary

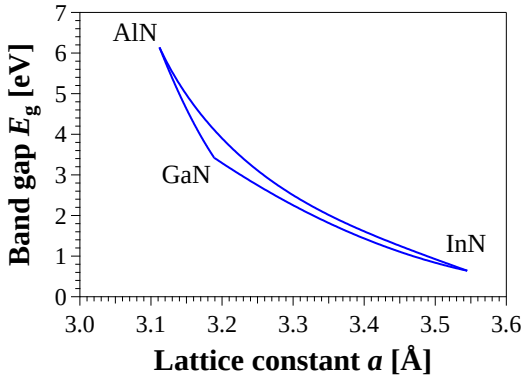


Figure 1.3 – Band gap versus lattice constant for the three main nitride compounds (AlN, GaN, and InN) and their ternary alloys, namely $Al_xGa_{1-x}N$, $In_xGa_{1-x}N$, and $Al_xIn_{1-x}N$.

or quaternary alloys, mainly based on Ga, Al, and In. In Fig. 1.3, we report the variation of band gap when creating ternary alloys using the three main Nitride compounds (e.g. $Al_xGa_{1-x}N$, $In_xGa_{1-x}N$ and $Al_xIn_{1-x}N$ with x varying from 0 to 1). The models used for determining E_g and a are the bowling model (quadratic) and linear model, respectively [4–6].

The capability of tuning the band gap using almost lattice-matched alloys is crucial for band structure engineering since it enables the growth of different epistructures for specific purposes. For example, the famous blue light-emitting diode (LED) is based on a multi-quantum-well (MQW) formed with layers of GaN and InGaN: carrier recombination for generating light happens in the InGaN layers having band gaps engineered to emit in the blue spectrum.

GaN and AlN (including AlGaN) belong to the family of large band gap semiconductors, which are very desirable for applications related to engine electrification and the high power telecommunications systems. A large band gap translates in higher breakdown voltage (V_{br}) for the fabricated devices, that is to say, more considerable power capabilities than narrow gap semiconductor (e.g., Si). Specifically for RF amplification, the breakdown voltage sets the maximum bias voltage for devices, which directly influences the maximum output power.

The saturation velocity (v_{sat}) is another crucial property since it determines the speed at which electrons cross the gate or base region (according to the type of transistor). The saturation velocity has a direct influence on the device cut-off frequency (f_c), which, for a lateral field-effect transistor (FET) having a gate length L_g, is equal to:

$$f_c = v_s / 2\pi L_g \tag{1.1}$$

Both high saturation velocity and large breakdown are fundamental in defining the device performance, and the Johnson Figure of Merit ($JFoM$) is usually used to describe the trade-off

Table 1.1 – Main semiconductors for RF applications and their physical properties together with the Johnson figure of merit (normalized with respect to the Si one). Values comes from Ref. [7]

Material	E_g [eV]	ϵ_r	E_{BR} [MV/cm]	μ [cm^2/Vs]	v_{sat} [cm/s]	$JFoM$
Si	1.1	11.8	0.3	1350	1.0×10^7	1
SiC	3.26	10	3.0	700	2.0×10^7	20
Diamond	5.5	5.5	5.6	1900	2.7×10^7	50
GaN	3.39	9.0	3.3	1200	2.5×10^7	27.5
GaAs	1.42	13.1	0.4	8500	1.0×10^7	2.7

between the two properties:

$$JFoM = \frac{E_{BR}\, v_{sat}}{2\pi} = V_{BR} f_c \tag{1.2}$$

In Tab. 1.1, we collect the values of the main physical properties influencing the RF behavior for materials which have or will have a substantial impact on the RF domain. Despite the very high $JFoM$ for diamond, this material is still at an embryonic stage in both growth (wafer size, cost, and quality) and fabrication process; in addition, it does not allow the formation of heterostructures which can ensure higher carrier mobility. The second most favorable candidate is then GaN, which has also other significant features: very high quality material thanks to growth developments for the fabrication of blue LEDs, large variety of wafers on which GaN can be grown, better thermal conductivity than GaAs, high mobility and carrier concentration in GaN-based high electron mobility transistors (HEMTs).

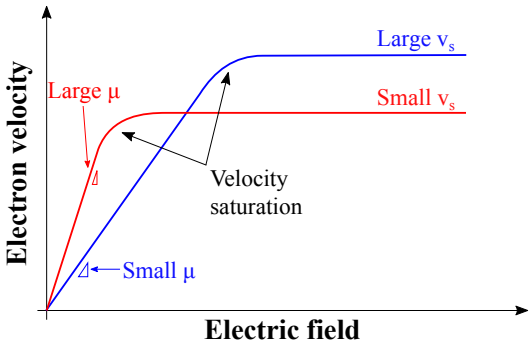


Figure 1.4 – Electron velocity in two different semiconductors: one has low mobility and high saturation velocity (blue line) and the other the opposite (red line). Such independence between electron mobility and velocity can be observed comparing GaAs and SiC (Tab. 1.1).

Despite the common thought, we believe that the role of the mobility for RF devices depends on the application and might be secondary. For example, amplifiers designed in class from A

to C work with a drain (or collector) bias causing the saturation of electron velocity, which is uncorrelated from the mobility (e.g. SiC has twice the saturation velocity of GaAs, yet its mobility is more than 10x smaller) and determines the cut-off frequency (Eq. 1.1). In this perspective, high mobility becomes useful only for low power applications since a small drain bias is needed for reaching the saturation velocity (Fig. 1.4); moreover, also noise performances are improved. In the case of RF power amplifiers (PAs), an increase of mobility reduces the voltage at which the saturation happens by a few volts, which is not an impressive improvement considering that operating bias voltage values are in the range of tens of volt.

1.2 Polarization and 2DEG formation

The common property of III-Nitrides is the wurtzite structure of the elementary cell (Fig. 1.5). The asymmetric position of the nitrogen ion with respect to the electrostatic centroid of the pyramid defined by the four gallium ions generates a dipole moment. When forming the crystal structure, dipoles of each cell sum together producing an electric field in between two layers (at the top and the bottom surfaces) of fixed charges (with opposite sign). This phenomenon is called spontaneous polarization (the same name also defines the charge density of the two layers), which generates an electric field in the order of MV/cm. Since III-Nitrides are piezoelectric materials, a polarization field is also generated when growing a binary or ternary compound on top of another with a different lattice constant. The lattice mismatch strains the thinner layer (the strain in the thick layer can be neglected if the ratio of the thicknesses is large) originating a piezoelectric polarization.

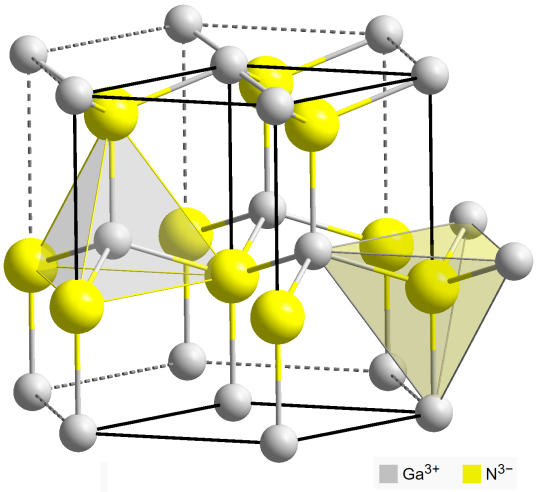
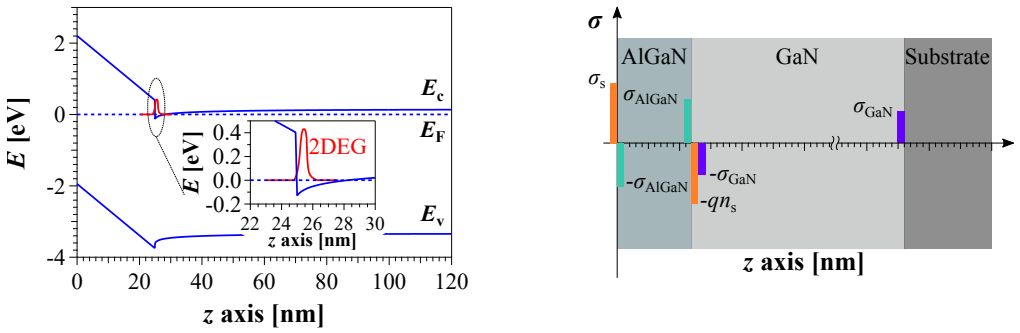


Figure 1.5 – Illustration of the combination of some GaN elementary crystal cells. Each cell is constituted by four Ga atoms, defining the four edges of the triangular-base pyramid, and a N atom in the center. The ionic bonds produce the formation of a nitrogen anion and four gallium cations per cell.



(a) Band diagram of an AlGaN/GaN HEMT.

(b) Fixed and mobile charge distribution in an AlGaN/-GaN HEMT.

Figure 1.6 – (a) and (b) Simulated band diagram and qualitative charge distribution of an AlGaN/GaN HEMT along its growth direction .

Both the spontaneous and piezoelectric polarization are essential in the formation of a 2-dimension electron gas. The most common HEMT structure is formed by using an AlGaN barrier on top of a GaN channel. Fig. 1.6a shows the band structure for an $Al_xGa_{1-x}N$/GaN heterostructure while Fig. 1.6b shows the charge distribution. When putting together the channel and the barrier, the total electric field (which is the sum of both the spontaneous and piezoelectric polarization) produces an accumulation of electrons at the interface between the two materials (more precisely in the GaN channel) while a fixed layer of positive charge is left at the interface with the air. Due to the accumulation of electrons, the conduction band bends down forming a triangular-shaped quantum well where electrons are confined, thus forming a 2-dimensional electron gas (2DEG) layer. The carrier concentration (n_s) of this layer depends on the material used for the barrier and its thickness, since both influences the total electric field due to piezoelectric and spontaneous polarization. Usual values are in the range of 1×10^{13} cm^{-2} (higher values, up to 6×10^{13} cm^{-2} have been also demonstrated [8]), which are at least one order of magnitude larger than those in other HEMT structures [9, 10]. The mobility of electrons in GaN-HEMT can be as high as 2200 V/cm^{2}s [11], exceeding the value reachable in bulk GaN (1200 V/cm^{2}s). Such improvement is produced by a screening effect of the high-density 2DEG with respect to charged centers in the barrier, e.g. dislocations, thus actively reducing scattering sources [4].

1.3 GaN growth and substrates

GaN epistructures (e.g. p-i-n, MQW, HEMT, etc.) can be grown with different techniques. Metal oxide chemical vapor deposition (MOCVD) is the most used in the LED and HEMT industry since it ensures relatively good material properties and quality with a large throughput. Molecular beam epitaxy (MBE) is generally employed in the academic field since it gives much better control of the growth parameters, thus enabling the formation of very complex epistructure, yet with a very small growth rate. Hybride phase epitaxy (HVPE), instead, is used to fabricate GaN

Table 1.2 – List of the most common substrates on which GaN can be grown. Physical properties such as the lattice constant (a), the thermal conductivity (λ), solid electrical resistance (ρ) and the coefficient of thermal expansion (CTE) are reported together with the lattice mismatch (Δa) and thermal mismatch (ΔCTE) with respect to GaN [12].

Substrate	GaN	Sapphire	6H-SiC	Si (111)
a [Å]	3.189	4.758	3.08	3.84
λ [W/cm/K]	1.3	0.5	3.0–3.8	1–1.5
ρ [Ωcm]	10^6	10^{14}	10^5	10^3-10^4
CTE in-plane [10^{-6} K^{-1}]	5.59	7.5	4.2	2.59
Δa [%]	–	16	3.5	-16.9
ΔCTE [%]	–	-34	25	54
Advantages	• Homoepitaxy • Large ρ	• Inexpensive • Simple growth • Large ρ	• High λ • Small ΔCTE • Large ρ	• Inexpensive • Very scalable • Si industry support
Disadvantages	• Expensive • Poor scalability • Up to 2”	• Large wafer bowing • Large Δa • Small λ	• Expensive • Limited wafer size	• Large Δa and bowing • Complex growth • Small ρ

substrates due to the fast growth rate.

GaN can be grown on different substrates with very noticeable differences in material properties, quality, and costs. In Tab. 1.2 we report the four main substrates usually used for GaN growth. The lattice constant of the substrate determines the presence of strain, either compressive (e.g. GaN on sapphire) or tensile (e.g. GaN on silicon), the density of dislocations and the growth complexity to alleviate such defects (for example, a thick, up to several μm, buffer is usually grown on Si).

Strain also arises when the coefficient of thermal expansions (CTE), particularly the in-plane one, of the substrate is different from that of GaN. Growths usually happen at temperatures higher than 1000 °C, then, when cooling down the growth chamber, both GaN and the used substrate shrink by different amounts, if the CTE is different, and strain or bowing result as effects.

The last aspects to consider in choosing the substrate are its thermal conductivity and solid electrical resistivity. Independently from the application, highly thermal conductive substrates (e.g. SiC) are more desirable since the generated heat can be easily dissipated, allowing higher power operation than in low thermally conductive wafers. A good electrical conductivity is more favorable for high power low frequency (up to few MHz) applications, while high resistive substrates are preferred for RF ones.

The highest material quality for any epistructure is obtained using GaN substrates; however,

they are costly (especially high resistive wafers) and strongly limited in size. Foreign substrates, presenting small lattice and thermal mismatch with respect to GaN are generally used and they include 6H-SiC, Si (111), and sapphire.The growth of GaN on foreign substrates can yield to the formation of cracks, high dislocation density, and large wafer bowing.

For RF applications, the two most suitable candidates are SiC and Si, since sapphire wafers are not ideal for dissipating considerable power due to the poor thermal properties. GaN on SiC is, so far, the best choice for RF devices where high-frequency operation and large power (i.e. large dissipated power) are needed. SiC ensures good thermal conductivity together with extremely good electrical insulation (which results in reduced RF losses with respect to more conductive substrates), though at the expense of higher material cost and size limitations.

High resistive (HR) silicon wafers can be used for applications where the handled power is not high (otherwise, there would be several thermal issues) and the operating frequency is below 10 GHz. The latter is caused by poor insulation capability of HR silicon which generates significant RF losses at high frequency. The advantages of using Si instead of SiC are the lower price and the larger wafer size (GaN can be grown on up-to-8" Si wafers) as well as the possibility to convert old Si manufacturing chains to produce GaN devices. All these factors contribute to actively reduce the cost (of course at the expense of the performance); thus, they target more mass commercial applications. Another advantage, which is still under research, is the monolith integration of logic circuits (for which 100 Si is needed) and RF circuits [13]. A similar trend is followed for GaN-based power devices using the silicon on insulator (SOI) technology [14].

1.4 MESFET based on GaN HEMTs: structure and operation

The most known device structure for a transistor based on a GaN HEMT is the MEtal-Semiconductor field-effect transistor (MESFET). Fig. 1.7 shows a device based on an AlGaN/GaN HEMT, where the source and drain are formed by fabricating ohmic contacts while a Shottky contact is used as gate to control the channel underneath. The device is usually isolated either by mesa etching or by ion implantation.

Ohmic contacts are usually realized by depositing and annealing, by a rapid thermal process (RTP), a stack of metals, which can varies from a simple Au-free Ti/Al stack [15] to 6-layer stacks using more exotic metals and also semiconductors (generally Si or Ge with the intent to perform a n-doping of the barrier)[16]. The used metal stack and RTP conditions (temperature, annealing time, chamber gas) strongly influence the morphology of the contacts (generally annealed ohmic contacts are quite rough), the contact resistance with the 2DEG (down to 0.21 Ωmm [16]) and lateral diffusion of the metals (very important for MESFET with short source-drain distance). Much better contacts can be achieved by partially etching the epistructure underneath the desired contact regions and regrowing heavily n-doped (up to 10^{19} cm^{-3}) GaN. The growth is usually performed by MBE and allows achieving ohmic contact resistance in the order 0.085 Ωmm [17]. In this case, the metal is deposited on top of the regrown regions and no annealing is required,

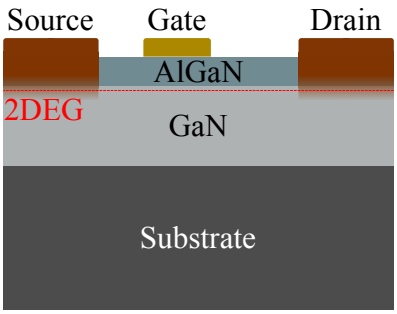


Figure 1.7 – Schematic of a MESFET based on an AlGaN/GaN HEMT structure.

thus this technology, despite being more complex, is the best choice for ultra scaled devices.

The Schottky gate is realized by using a metal with a high working function, since such value determines, in the case of a thick barrier where the tunneling current can be neglected, the gate leakage current. Nickel is the most common choice and it is generally followed by a thick gold layer that ensures very low gate contact resistance (not to be confused with the gate conductance, which takes into account the leakage current through the gate).

The working principle of a MESFET is based on the modulation of the 2DEG carrier density by applying a negative voltage to the Schottky gate. Further accumulation of electrons in the 2DEG is strongly limited by the reduction of the Schottky barrier height for positive gate voltage, which results in a considerable gate leakage. This problem can be solved by using a MOS-HEMT structures, which also allow the fabrication of normally-off devices (no 2DEG at equilibrium under the gate).

1.5 State of the art of RF devices based on GaN HEMT

1.5.1 Commercial GaN HEMT devices

The main RF application for GaN-based HEMT is for PAs, thanks to the large breakdown voltage which allows increasing the supplied bias, so the maximum output power. Commercial GaN PAs are already available and they can reach power up to 100 W in a single stage (e.g. the Qorvo's TGA2813-CP PA).

The large band gap makes GaN also less susceptible to noise and capable of working at high temperatures (some hundreds of Celsius), thus very appealing for low noise amplifiers (LNAs). A further advantage in using GaN for LNAs is strong robustness to excess of input power, indeed commercial devices can resist to up 10 W exceeding power (e.g. Qorvo's TGA2227-SM) and such capability is not present in any other competing technology.

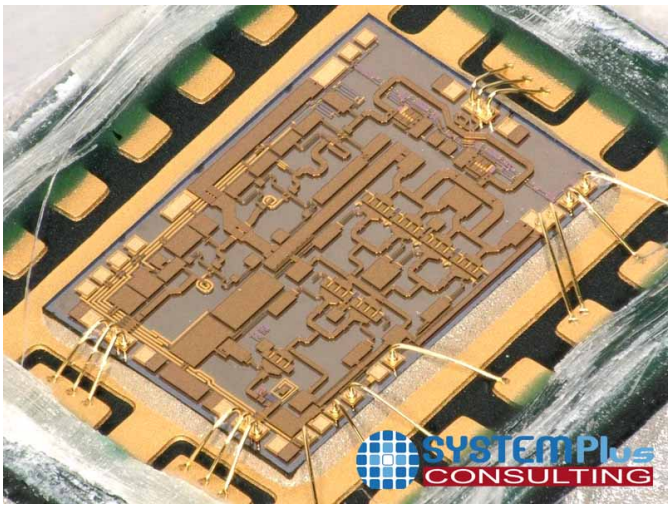


Figure 1.8 – Qorvo GaN MMIC unveiled by System Plus Consulting [18]. The MMIC targets 5G base stations and includes a high linearity LNA, a low insertion-loss TR switch and a high gain PA.

Another, less mainstream, commercial application involves the fabrication of RF switches (e.g. the United Monolithic Semiconductors CHS8618-99F GaN reflective single pole double trows). The large breakdown voltage allows operations with high power signals while the high current capabilities, due to the large saturation velocity and high carrier concentration, ensures very small insertion losses (1.3 dB).

Thanks to the lateral structure of devices based on GaN-HEMTs, the fabrication of microwave monolithic integrated circuits (MMICs) is feasible and very promising. MMICs, in general, allow reducing parasitic components due to the proximity of the devices which coexists on the same die, hence losses are reduced and the frequency operation is increased; furthermore, the total cost of the system is strongly diminished. Fig. 1.8 shows a front end module for 5G base stations wholly built on a GaN on SiC chip. The MMIC contains a high linearity LNA, a low insertion-loss Transmit Receive (TR) switch and a high gain PA.

1.5.2 GaN HEMT research activity

Despite the availability of excellent and competitive commercial devices, there is a lot of research activities which aim to improve some device properties, expand the fields of application of GaN-HEMT devices and mitigate some issues.

While commercial devices can work up to several tens of GHz, researchers are developing scaling technologies to approach the theoretical limit predicted for GaN. This process involves the reduction of the gate length (down to a few tens of nm) and the reduction of parasitic capacitance and resistance contributions. Ultrascaled GaN HEMTs require the fabrication of the T-shaped gate, which helps to reduce both the gate length and resistance, regrown contacts to reduce the

overall device resistance and optimization of the passivation layer. Tang et al. [19] demonstrated the best ever reported frequency performance in a 20 nm-long gate device (Fig. 1.9a) with a cut-off frequency (f_c) of 454 GHz.

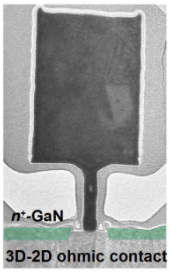
Ultra-short gate devices, though, present two main disadvantages: reduction of break down voltage and increase of short channel effects (SCE). The latter includes poor channel control which translates in very high subthreshold slope (SS), far from the ideal 60 mV/dec, and large drain induced barrier lowering (DIBL). Previous works have shown that short channel effects start to be dominant when the ratio between the gate length and the gate-to-DEG distance (e.g. the barrier thickness in case of a Schottky gate) is smaller than 7.5 (average values between two different papers investigating short channel effects [20, 21]). For example, a GaN HEMT with a gate length of 20 nm would require a barrier thickness of about 3 nm.

The reduction of the barrier thickness under the gate is achievable either by growing HEMT wafers with thinner barriers or by using the gate recess technique. The former usually requires to use different materials than AlGaN for the barrier to ensure the formation of the 2DEG (the average AlGaN barrier thickness is around 25 nm and smaller values would strongly reduce the carrier concentration, yielding an increase of resistance). For example, the barrier thickness can be reduced down to 6 nm using InAlN [22] or to 4 nm using AlN [19] while still maintaining an average carrier density around 1×10^{13} cm^{-2}.

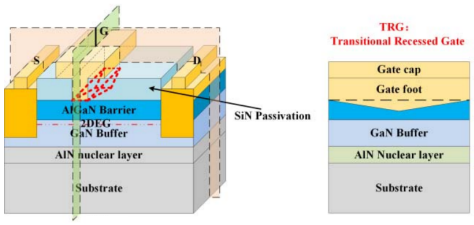
Gate recess, instead, requires a very precise etching of a portion of the barrier under the gate region. In this case, the research is mainly focused on improving the etch speed control and reduce etch damages. For this purpose, digital etching is one of the most common techniques and involves cycles of oxidation of the barrier by O_2 plasma and removal by acid (usually hydrochloric acid). For each cycle, a constant number of atomic layers are removed ensuring very good control; however, such technique, widespread in the academic field, would be challenging to use in the industry. Atomic layer etching (ALE), already developed for narrow-gap III-V semiconductors and just released for III-Nitrides, can be a good substitute for digital etching since it still works by oxidation-removal cycles but everything happens inside the reacting chamber of the tool, hence it is very promising for mass production.

Despite the used techniques and material to achieve thin barriers, electron tunneling cannot be neglected and this strongly deteriorates the operating power range [23].

Linearity over input voltage is another important feature of PAs. The modulation scheme implemented for 5G communications produces signals with a high peak-to-average power ratio, thus the amplitude of the signal to be amplified has a wide dynamic range. A linear modulation can be ensured either by using pre-distortion techniques, which use complex algorithms and require further hardware, or by using high-linearity PAs. A flat transconductance of transistors over the gate voltage ensures good linear behavior and this can be achieved by properly tuning the transistor threshold voltage along the device width [25]. This solution can be implemented by using different techniques; for example, by a transitional-recess gate technology (Fig. 1.9b) [24].



(a) 20 nm T-gate MESFET with an AlN/GaN HEMT.



(b) Schematic of MESFET with a transitional-recessed gate.

Figure 1.9 – (a) Cross section of a MESFET with a 20 nm long T-gate and regrown ohmic contact [19]. The reported frequency performance ($f_c \sim 450$ GHz) is the best realized with any III-Nitride HEMT. (b) Schematics of a MESFET with transitional-recess along the gate width for improving the device linearity thanks to a smooth variation of the threshold voltage [24, 25].

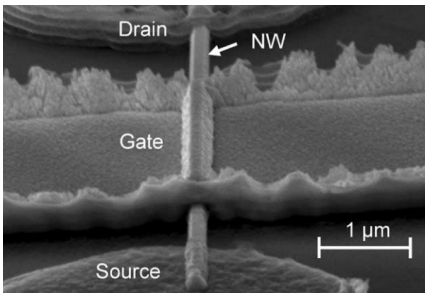
1.5.3 GaN nanowires

GaN nanowires (NWs) might be a solution to both linearity problems and short channel effects. Growth and etching of GaN nanowires are the two possible fabrication techniques.

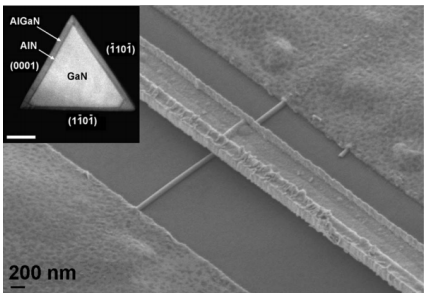
NWs can be grown on different substrates using catalysts or the selective area growth technique inside either MOCVD or MBE chambers. Fig.1.10a shows a MESFET based on an n-type NW which was grown on Si (111) and then transferred on SiO_2 over Si wafer, while Fig. 1.10b illustrate a metal insulator semiconductor FET (MISFET) relying on a radially grown AlGaN/GaN epistructure [26].

The second approach starts using a wafer with the desired epi-structure, which can be n-p-n for vertically devices (Fig. 1.10c [28]) or HEMT for lateral ones (Fig. 1.10d [29]), and perform a dry-etching with an hard mask or metals defining the NW diameter or width for vertical or lateral NWs, respectively. In this case, ad especially for vertical NWs, which are used to create gate all around (GAA) MOSFETs, the interface is very important and a wet etching process, based either on hot potassium hydroxide (KOH) or hot tetramethylammonium hydroxide (TMAH), is performed to heal dry-etching damages on the sidewalls.

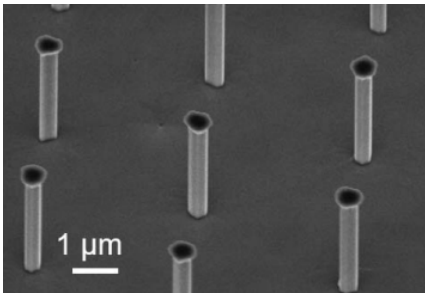
Top-down NW HEMTs are very promising because they help to solve the previously listed issues, such as linearity and short channel effects, without a strong degradation of the material and 2DEG properties. For example, Joglekar et al. [25] have demonstrated that by using an array of GaN HEMT NWs with different widths, it is possible to obtain a more flat transconductance, indicating a more linear behavior of the device. Short channel effects can also be sharply reduced as shown by Ture et al., indeed the subthreshold slope improved from 200 mV/dec in the planar MESFET to 75 mV/dec in the NW-based one [29].



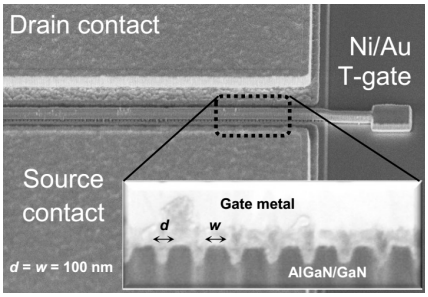
(a) MESFET based on a grown GaN NW.



(b) MISFET based on a grown AlGaN/GaN NW.



(c) Vertically etched GaN NWs.



(d) MESFET with T-gate based on NWs etched from a GaN HEMT wafer.

Figure 1.10 – (a) MESFET based on a MBE grown n-type *c*-axis GaN NW [27]. (b) MISFET based on a MOCVD grown *c*-axis AlGaN/GaN NW [26]. In the inset, a cross section of a NW with a scale bar of 50 nm. (c) Vertical NWs etched from a n-p-n GaN wafer [28]. (d) MESFET with a T-gate which wraps the three sides of NWs etched from an AlGaN/GaN HEMT on SiC [29].

1.6 Thesis outline

The use of GaN HEMT NWs is becoming more common and favorable for several applications, from high power [30, 31] to RF [32–34], and a lot of research is still going on.

In this thesis, we deeply investigate GaN HEMT NWs under different aspects to have more physics insights about these structures and offer new applications and architectures.

In chapter 2, we report electron transport studies performed in a mesoscopic device, called electron filter cross, which is based on two crossing NWs. This study reveals fascinating phenomena, such as ballistic transport at RT, quenched Hall effect, and quantum phase coherence, as well as it gives some practical information about NWs, e.g. a very accurate measurement of the sidewall depletion width. The reported results mainly come from Ref. [35].

In chapter 3, we discuss unconventional gating techniques for GaN HEMT NWs which should

alleviate the increase of parasitic capacitance, a drawback present for any NW-based transistors. This chapter is based on results published in Ref. [36] and other unpublished results of our group.

In chapter 4, we investigate a new architecture for RF power detectors working at zero bias, which is based on field-effect rectifiers having a channel constituted by an array of etched GaN HEMT NWs. This chapter is based on results published in Ref. [37].

Chapter 5 concludes the thesis and ends with some future work projects.

2 Ballistic transport in GaN nanowires

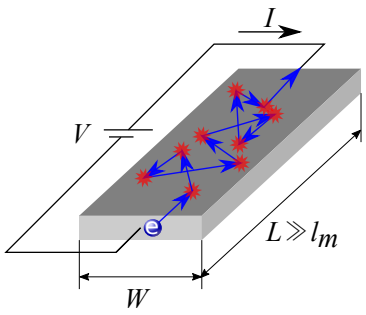
2.1 Introduction

In this chapter, we will discuss about electron transport studies performed by fabricating and measuring mesoscopic devices using III-Nitride HEMTs. The chapter first gives a theoretical overview of ballistic transport and quantum phenomena associated with the wave nature of electrons. Most of the material for this section comes from the book of S. Datta [38] and the review article about mesoscopic devices of T. J. Thornton [39]. Then we report about the measurements performed in our lab using GaN-based mesoscopic devices by varying several parameters (device dimensions, bias, temperature, magnetic field, etc.). Finally, we conclude with a small summary of the chapter. The shown results are from Ref. [35].

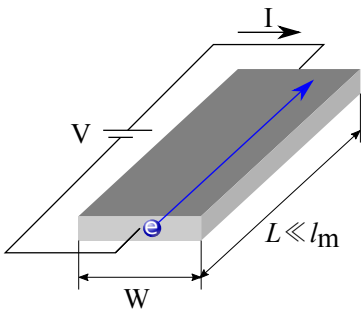
2.2 From diffusive to ballistic transport

Considering a 2D conducting layer with a length L and a width W, if we apply a voltage (V), as shown in Fig. 2.1a, then the measured current I is equal to $\frac{V}{R} = V\frac{L}{\sigma_0 W}$, where $\sigma_0 = n_s q^2 \tau / m^*$ is the Drude conductivity (with q and m^* being the elementary charge and the effective mass of the carrier, respectively) [38]. n_s represents the number of available carriers (electrons or holes) per unit of area while τ is the mean free time, which is the average time between two consecutive collisions of a carrier. The sources of these collisions are numerous and depend on both the material and the applied electric field [40]. The product between τ and the average speed of electron (v_F) defines the mean free path (l_m), that is to say the average distance between two consecutive collisions.

For $L \gg l_m$ electrons scatter multiple times before reaching the other terminal and this transport regime is called diffusive (Fig. 2.1a). On the other hand, ballistic transport is achieved for $L \ll l_m$, in which case electrons do not suffer any collision over the length L (Fig. 2.1b). In these conditions, the overall resistance does not reach 0 Ω but $h/2q^2 \sim 12.5k\Omega$ (h is the Plank constant), known as resistance quantum (R_0, or conductance quantum $G_0 = 1/R_0$) which is



(a) Diffusive transport.



(b) Ballistic transport.

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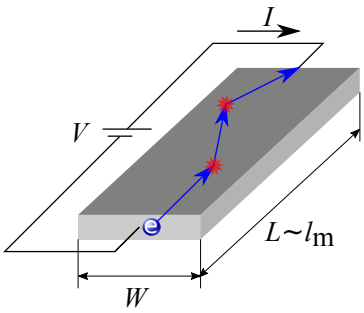


(c) Quasi-ballistic transport.

Figure 2.1 – (a) Diffusive transport of an electron between two terminals, which is characterized by several collisions along the path. (b) Ballistic transport of an electron with a transmission probability equal to 1. (c) Quasi-ballistic transport in which case electrons suffer scattering with a probability to directly reach the other terminal between 0 and 1.

defined as the resistance of a 1D semiconductor where only one energy level (mode) is available. The number of modes (M) can be increased by enlarging the semiconductor width, for instance, and this was experimentally observed in 1988 [41, 42]. The result of the experiments was the quantization of conductance by *quanta* equal to G_0, though the width of the channel was smoothly increased by the applied electric field. In the case of ballistic transport, the resistance associated with each mode is 0 Ω, since there is no scattering, and the voltage drops only at contacts and equally by $IR_0/2$ for each mode; thus the total measurable resistance is R_0/M.

In the case of $L \sim l_\mathrm{m}$ (Fig. 2.1c), there are two resistance contributions, namely the contact resistance R_c and the channel resistance R_ch (Fig. 2.1c), with the latter caused by a few collisions along the path L. This situation is used to define a common expression for the resistance in a semiconductor (Fig. 2.2), independently from the size and the transport regime [38]:

$$R = R_\mathrm{ch} + R_\mathrm{c} = \frac{L}{\sigma_0 W} + \frac{l_\mathrm{m}}{\sigma_0 W} \tag{2.1}$$

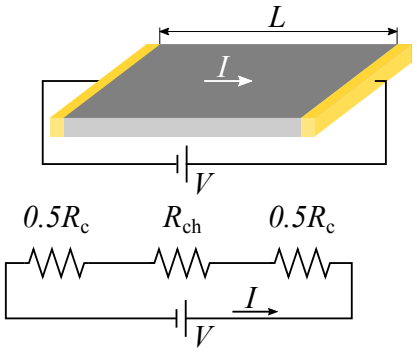


Figure 2.2 – General resistance representation, which is independent of the transport nature, of a semiconductor sample with two ohmic contacts.

For $L \gg l_m$, R_c is negligible, the transport is diffusive and the Eq.2.1 becomes simply $\frac{L}{\sigma W}$, whereas, in the opposite case, the transport is ballistic and the only resistance contribution is from contacts and Eq. 2.1 reduces to $\frac{l_m}{\sigma W} = R_0/M$. Eq. 2.1 can also be written as a function of the number of modes and the transmission coefficient $T = l_m/(L + l_m)$, which indicates the probability for an electron to reach the other terminal without collisions, obtaining the Landauer formula:

$$R = \frac{h}{2q^2}\frac{1}{MT} \tag{2.2}$$

2.3 Electrons as waves

At the beginning of the XX century, De Broglie suggested the idea, which was later demonstrated by the Davisson-Germer experiment in 1927, that electrons, as light, have a dual nature; in particular, they can behave either as a wave or as a particle in according to the surround conditions. The study the wave nature of electrons in semiconductors is possible if the applied bias is lower than E_F/q (E_F is the Fermi energy) and one or more dimensions are smaller than the phase coherence (or phase-relaxation) length (l_ϕ), which is referred as the average distance over which the phase associated to the wavelength of an electron is maintained. In these conditions, quantum interference phenomena can happen and the value of l_ϕ can be extracted, which depends on temperature and material properties. The main difference between l_m and l_ϕ comes from the nature of electron collisions, which can be elastic (no loss in energy and phase) or inelastic. Both scattering mechanism influences the mean free path since both produce a change of momentum (direction of electrons), thus the transition from ballistic to diffusive transport. On the other hand, the phase-coherent length will be sensitive only to the inelastic collisions, which can be neglected at cryogenic temperatures leading to the manifestation of interference effects.

Weak localization (WL) is one of the most important consequences of the wave nature of electrons

and it explains the decrease of conductivity in a narrow channel (width much smaller than the phase coherence length) of a NW HEMT at cryogenic temperature[38, 43, 44]. Considering an etched NW from any HEMT structure, by reducing the temperature, the conductivity increases in according to the Drude model (larger mean free time due to increased mobility); however, below a specific temperature, the conductivity starts to decrease. The more resistive behavior can be explained as the result of destructive interference between the forward and backward waves associated with elastic electron scattering centers. As soon as a magnetic field is applied, the time-reversal invariance is lost and this reduces the probability of destructive interference, hence the conductivity augments [38, 43, 44].

Another phenomenon caused by wave interference is called universal conductance fluctuations (UCF) [45, 46]. In particular, by measuring the resistance versus magnetic field using any couple of voltage probes connected to a NW with a width smaller than l_ϕ, fluctuations are observable due to interference effects.

2.4 Mesoscopic devices

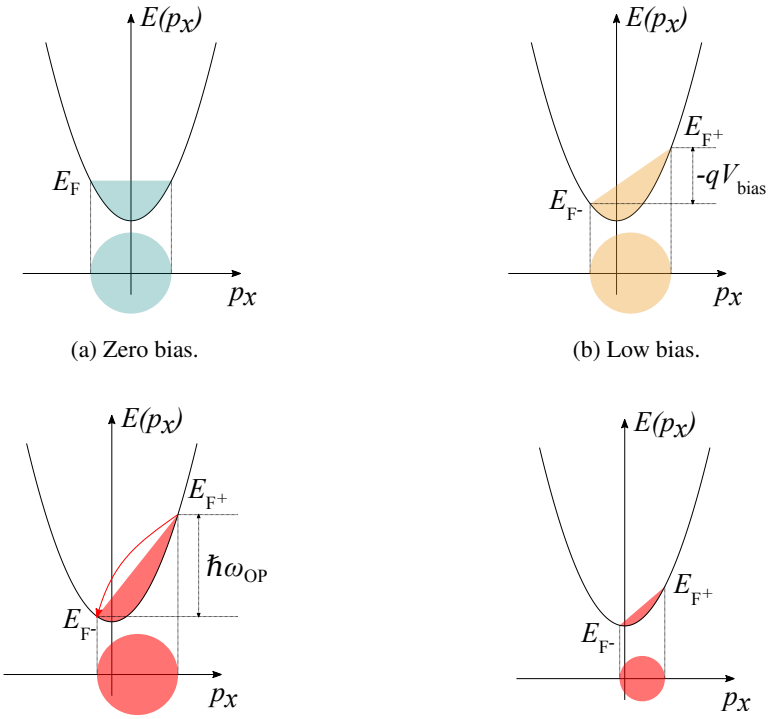
The conditions required for either ballistic transport or interference phenomena are usually satisfied in devices with dimensions from a few nm up to one μm. For ballistic transport, devices with very high mobility (μ) are more desirable, since $l_\mathrm{m} = \frac{m^* \mu(T) v_\mathrm{F}}{q}$, to avoid the fabrication of extremely small features and to ensure room temperature operation. In this perspective, HEMTs are a common platform to study electron transport. Devices having one or more dimensions smaller or comparable with either l_m or l_ϕ are called mesoscopic devices, which can be used for transport studies and might overcome issues in classic electronic devices [39].

Mesoscopic devices for the investigation of electron transport and quantum phenomena have been usually realized by using narrow-gap semiconductor HEMTs, such as InGaAs/ InP [47], GaAs/AlGaAs[48], InSb/AlInSb[10], InAs[49] and Si/SiGe[50]. At cryogenic temperatures, quantized conductance in a point contact [42, 51], negative bend resistance [52, 53], electron focusing [54], quantum interference [43], and quantum Hall effect [55] have been demonstrated. Mesoscopic devices exploiting ballistic transport have been reported, such as ballistic deflection transistors [56], logic gates based on quantum point contacts [57], ballistic rectifiers, and functional materials [47].

2.5 Ballistic transport in mesoscopic GaN devices

2.5.1 Advantages of GaN-HEMTs for ballistic transport studies and devices

III-Nitride HEMTs offer an interesting platform for studying electron transport because of the up-to-four time large optical phonon energy (E_OP) with respect to other HEMT structures. Optical phonons are vibrations of the crystal lattice which require higher energies than acoustic phonons



(a) Zero bias.

(b) Low bias.

(c) High bias.

(d) Large bias with reduced n_s.

Figure 2.3 – 1D energy-momentum plot at zero bias (a), low bias (b), high bias (c) and reduced n_s in high bias (d). At zero bias (a), the Fermi level is constant and the number of electrons having positive and negative momentum is the same, so there is no net flux. When a bias is applied, the Fermi level splits into two quasi-Fermi levels separated by a quantity equal to $-qV_{bias}$; furthermore, the momentum balance is broken and there is a current flowing. (c) When the difference between the quasi-Fermi levels is equal to the E_{OP}, optical phonons are emitted and the momentum is inverted in sign, meaning that electrons start to scatter. (d) In the case of reduced carrier concentration (e.g. by applying a gate voltage), the generation of optical phonons is drastically reduced.

and cause the saturation of the electron velocity. Furthermore, as it will be described in the next lines, if the transport of electrons is ballistic, the generation of optical phonons causes the transition to diffusive transport.

Considering a 2D conductive layer in the xy plane, the electron energy and momentum components (p_x and p_y) are linked by a parabolic relation $E = (p_x^2 + p_y^2)/2m^*$. Along the x direction, the cross-section is the parabola shown in Fig. 2.3a, where the Fermi level is constant and the amount of electron having positive p_x and negative p_x is the same; consequently the net momentum is 0 (so the average velocity) as well as the net current (as expected since there is no applied bias). As soon as a bias (V_{bias}) is applied along the x direction, we can define quasi-Fermi energy levels (E_{F+} and E_{F-}) which are spaced by qV_{bias}. The distribution of electrons shifts toward positive values of p_x (Fig. 2.3b), thus the net momentum is different from 0 along with

Table 2.1 – Electron mobility, saturated drift velocity and optical phonon energy for some of the most currently used semiconductors. The reported values are from NSM archive. The reported mobility for GaN refers to HEMT structures.

Property	Si	Ge	GaAs	GaN	4H-SiC	InP	InSb
Electron mobility (cm^2/Vs)	1500	3900	8500	2200	900	5400	77 k
Optical phonon energy (meV)	63	37	33.81	92	104.2	42.6	25

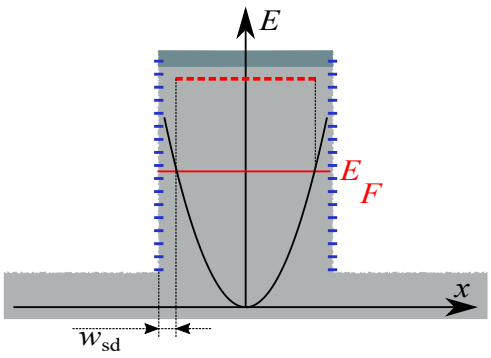
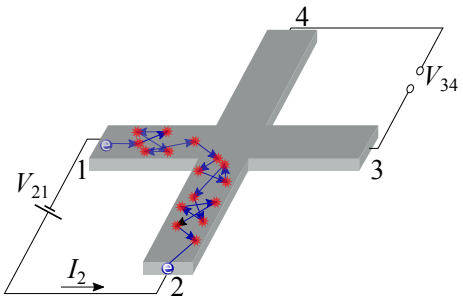


Figure 2.4 – Representation of a NW after an etching process. Dangling bonds are usually present on the sidewalls and they deplete the channel by pinning the Fermi level at lower energy. The sidewall depletion width is defined as half of the reduction of the effective channel width.

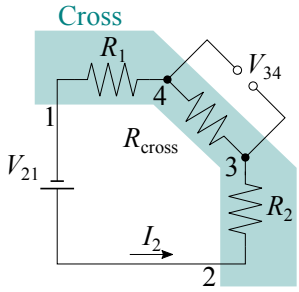
the electrical current. When the difference $E_{F+} - E_{F-}$ is equal to E_{OP}, electrons will start emitting optical phonons, losing energy and falling in the lowest available energy levels on the $E(p_x)$ curve (Fig. 2.3c). A negative p_x is associated with such levels implying that electrons start to move in the opposite direction, i.e. the electron scatters. For semiconductors having large optical phonon energy, the mobility (thus the mean free path) is not limited by optical phonon emission at low bias; however, other sources of scattering might be limiting ballistic transport. From this point of view, III-Nitride HEMTs offer one of the best compromises between long mean free path (high mobility) and high optical phonon energy (Tab. 2.1). Despite the small optical phonon energy (which is mitigated by a less efficient phonon emitting process) and because of the extremely high mobility, also InSb is a promising material for ballistic transport at room temperature, though the growth of such material is still challenging [58].

As shown by Fang et al.[59], the optical phonon generation can also be strongly reduced for smaller values of the carrier concentration in the channel (Fig. 2.3d). Bajaj et al. [60] demonstrated an enhancement of the electron velocity from $\sim 1\times10^7$ cm/s to $\sim 1.75\times10^7$ cm/s when reducing the carrier concentration from 7.4×10^{-12} cm^{-2} to 7.4×10^{-11} cm^{-2}.

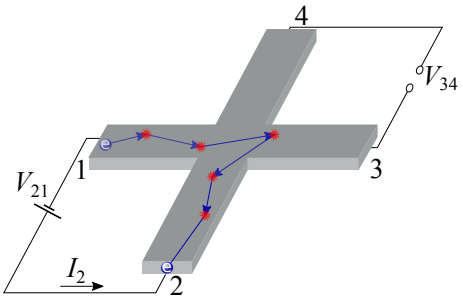
Another advantage of III-Nitride HEMTs is a larger carrier density, which allows having more carriers in etched NWs together with a much-reduced sidewall depletion. The etching process required to etch NWs in any material, especially if it is dry etching, produces damages on the



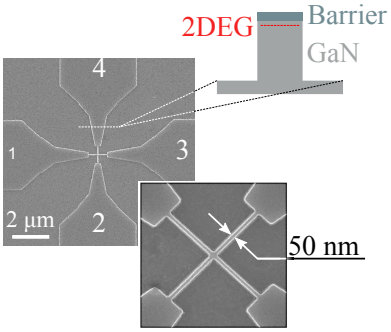
(a) Electron-filter cross under diffusive transport.



(b) Equivalent circuit of an electron-filter cross.



(c) Electron-filter cross under ballistic transport.



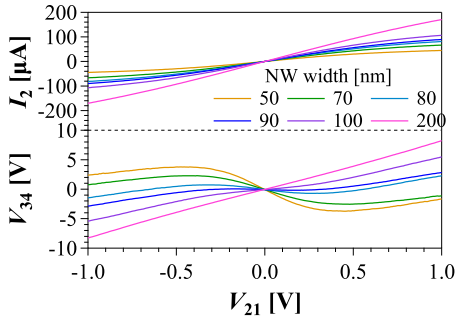
(d) SEM image of a cross based on 50 nm-wide NWs.

Figure 2.5 – (a) Representation of an electron moving diffusely under the applied bias in the electron-filter cross. The probability for electrons to reach the lead 3 is close to 0. (b) Equivalent circuit of the cross for electrons moving under diffusive transport. (c) Representation of an electron crossing the center of the cross without collisions, thus reaching lead 3. (c) SEM image of a cross based on 50 nm-wide HEMT NWs fabricated by dry etching.

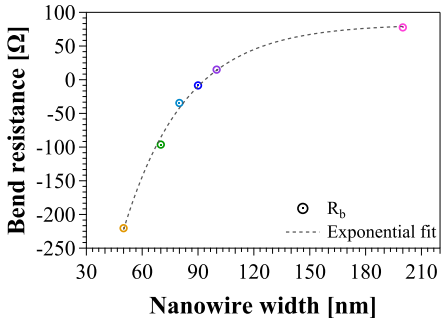
sidewalls and leaves unbounded negative ions (dangling bonds) that act as a negative gate voltage reducing the extension of the conductive channel. This conductive width reduction depends on the amount of these sidewall charges and the carrier concentration in the channel. Supposing that etching processes create about the same amount of dangling bonds independently from the material, the reduction in conductive width (also known as sidewall depletion width w_{sd}) will be less severe for highly carrier-populated NWs. Previous work have shown that the sidewall depletion width can be in the order of few hundreds of nm in narrow-gap semiconductor [9, 10] while in III-Nitrides HEMT NWs it is in the order of few tens of nm [35, 61], since the latter have more than 10X larger carrier concentration (up to 2-3$\times 10^{13}$ cm^{-2} [62, 63]).

2.5.2 Ballistic transport at room temperatures

One of the most interesting devices for investigating the nature of electron transport is the electron-filter nanowire cross shown in Fig. 2.5a [9, 50, 61, 64]. When a voltage is applied



(a) Electron-filter crosses with different Nw widths.



(b) Bend resistance versus Nw width.

Figure 2.6 – (a) I_2 and V_{34} versus V_{21} for crosses based on NWs with a width from 50 nm to 200 nm. (B) R_b versus NW width together with the exponential fit used to extract l_b [61].

between terminals 1 and 2 (V_{21}) and in the case of diffusive transport, electrons move from lead 1 to lead 2 suffering several collisions and the measured voltage between terminals 3 and 4 (V_{34}) is positive and it represents the voltage drop in the center of the cross (Fig. 2.5a and 2.5b). On the other hand, in the case of ballistic transport, electrons can cross the center of the cross and reach lead 3 (Fig. 2.5a). This yields a more negative potential in lead 3 than in lead 4, as a result V_{34} is negative (to be more general, opposite in sign with respect to V_{21}).

We fabricated crosses having a nanowire length of 1 μm and widths from 50 nm (2.5d) to 200 nm (the process flow shown in Appendix A.1 is used until step) using an AlInN/GaN HEMT structure. The width of the NWs also represents the minimum distance that electrons need to cross without collisions to produce a sign inversion of V_{34}. The bias voltage V_{21} is applied in the push-pull configuration ($V_1 = -V_2$, hence $V_{21} = 2V_2$) and Fig. 2.6a shows the measured V_{34} for all the NW widths. A fully diffusive behavior is noticeable for the 200 nm-wide NW devices since V_{34} has the same sign of V_{21}, whereas a firm signature of ballistic transport is presented for the 50 nm devices due to the inverted sign of V_{34}. Intermediate-width devices show a smooth transition from diffusive to ballistic transport as soon as the NW width decreases, which can also be interpreted as an increase of the transmission coefficient from lead 1 to lead 3 (for positive V_{21}) if we refer to the Büttiker and Landauer formalism [38]. Such coefficient (T_{31}) is proportional to the ratio l_m/L, where L is the distance to be crossed, hence crosses based on narrow NWs yield larger T_{31}.

The bend resistance (R_b), defined as $\frac{\partial V_{34}}{\partial I_2}$, is calculated around zero bias and its dependence versus the NW width is illustrated in Fig. 2.6b. The negative value of R_b indicates that the transport is mainly ballistic in the center of the cross with a probability for electrons to move under ballistic regime larger for more negative R_b. Matioli and Palacios [61] defined the ballistic length as a quantity similar to the mean free path, which results to be ~33 nm for the discussed devices (the value of R_b for 200 nm wide NWs is not considered in according to the assumption of the authors).

2.5.3 Ballistic transport under magnetic field at 4.2 K

A ballistic cross formed by 87 nm-wide NWs based on an AlGaN-barrier HEMT was used to investigate the effect of a magnetic field perpendicular to the 2DEG on the electron transport. The study was performed at 4.2 K and under a magnetic field up to 10 T.

In Fig. 2.7 we report the behavior of V_{34} and $J_2 = I_2/W_{NW}$ versus $V_{wire} = V_{21} - I_2 R_{acc}$ (with R_{acc} being the total access resistance which takes into account both the ohmic contact resistance and the resistance of the access regions) at 4.2 K and with no applied magnetic field. For small V_{wire}, V_{34} and J_2 have a linear behavior with a negative slope for the former, indicating that the electron transport is mainly ballistic. This is also highlighted by the negative sign of the bend resistance shown in the inset of Fig. 2.7. When V_{wire} reaches V_{knee} =100 mV, the current saturates while V_{34} reaches its maximum. At this point, optical phonons start to be emitted, causing the saturation of the velocity, thus J_2, and the reduction of electrons moving in the ballistic regime. The effect of optical phonon is more evident at 4.2 K than at room temperature due to the drastic reduction of all the other sources of scattering, which also leads to an increase of more than six times in mobility. The bend resistance crossing the 0 Ω ordinate at V_{knee} shows more clearly this transition from full ballistic transport to semi-ballistic one. This voltage value is very close to the optical phonon energy in GaN (92 meV), confirming the theory concerning the effect of optical phonons on the ballistic transport of electrons.

The absence of collisions in the ballistic transport regime resembles the motion of electrons in vacuum tubes, where either magnetic or electric field can change their trajectories. This similarity drove us to investigate the response of "ballistic" electrons in the presence of a strong magnetic field (B) between -9.9 T and 9.9 T and perpendicular to the conductive plane. Fig. 2.8 shows the 2D map of V_{34} as function of bias and magnetic field at 4.2 K. The straight trajectory of an electron moving without collision can be easily modified into a circular one by applying a magnetic field. This generates a Lorenz force which is proportional to the electron velocity ($\vec{v}_e$) and the applied electric ($\vec{E}$) and magnetic ($\vec{B}$) field ($\vec{F}_L = q\vec{E} + q\vec{v}_e \times \vec{B}$). The vectorial product between $\vec{v}_e$ and $\vec{B}$ produces the bending of the electron trajectories which is maximized when the

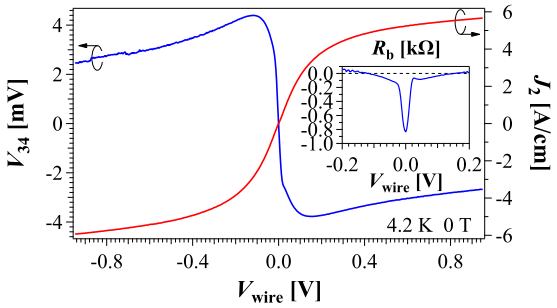


Figure 2.7 – V_{34} and J_2 versus V_{wire} for a crosses based on NWs with a width from 87 nm. In the inset R_b is shown for values of V_{wire} close to 0 V.

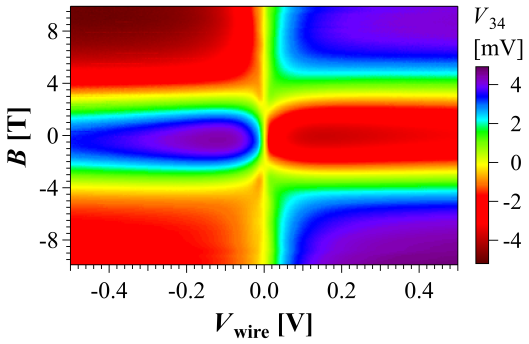


Figure 2.8 – V_{34} versus V_{wire} (x axis) and B (y axis) at 4.2 K.

two vectors are perpendicular ($\vec{v}_e \perp \vec{B}$).

The 2D map can be divided in three regions with respect to the magnetic field (curves for each region are collected in Fig. 2.9):

- inverting region for B below 2 T: V_{34} still exhibits a negative slope but with a reduction in amplitude as B increases;
- semi inverting region for B between 2 T and 3.6 T: an interesting behavior occurs for 0 < V_{wire} < V_{knee}, where the slope of V_{34} changes from positive to negative defining sharp transition points V_{tp}, as shown in Fig. 2.9;
- non-inverting region for B above 3.6 T: V_{34} has the same sign of V_{21}(positive slope).

In absence of collisions and under a potential difference (V_{wire}), electrons move with a velocity $\vec{v} = -q\vec{E}t/m^*$ (where the electric field magnitude (E) is proportional to V_{wire} and t is the time) [65] while in the presence of a magnetic field, electrons follow a circular orbit with radius l_c=

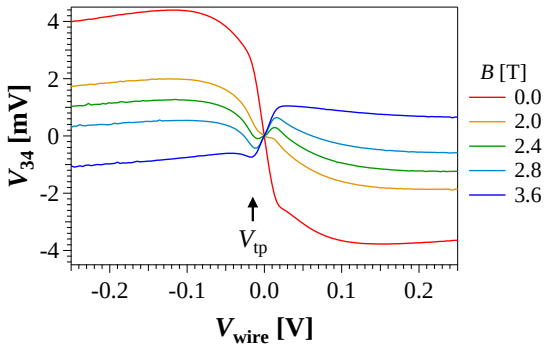


Figure 2.9 – V_{34} versus V_{wire} for some values of B at 4.2 K.

$m^* v_e / qB$. For $B > 2$ T and small bias, the small v of electrons yields small l_c ($l_c \ll W_{NW}$), forcing electrons in a circular ballistic motion, and resulting in a positive slope of V_{34}. As V_{wire} increased above V_{tp} for a given B, l_c becomes large enough to allow electrons to travel across the center of the cross and reach the opposite lead 3 ($l_c \gg W_{NW}$), leading to a negative slope of V_{34}. This effect fades either with the saturation of v_e when $V_{wire} > V_{knee}$ or with $B > 3.6$ T, when the electron velocity is not high enough to ensure a large l_c before it saturates. Hence the turning points reflect the equilibrium between the straight motion towards lead 3 and circular motion towards lead 2 of electrons. The relation between l_c and W_{NW} also explains the behavior in the inverting and non-inverting region, since for the former l_c is always much larger than W_{NW}, i.e. electrons can reach the opposite lead, while for the latter is always smaller.

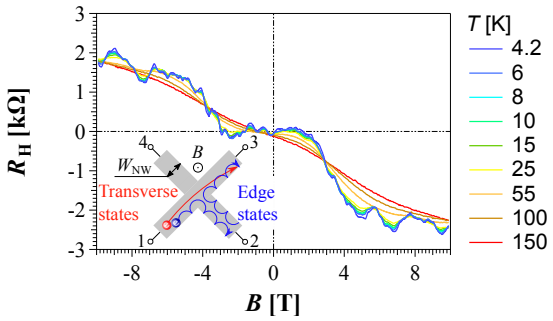
2.6 Quenched Hall effect, UCF and WL

Electron transport is also investigated at low bias conditions ($V_{bias} \ll E_f / q$), where semi-classical and quantum phenomena can be observed thanks to the wave nature of electrons. For this purpose, Hall measurements are performed with two synchronized single-output lock-in amplifiers: the first applies a bias of 100 μV between leads 1 and 3 and measures the current I_{13}, the second measures the Hall voltage between contacts 2 and 4 (V_{24}).

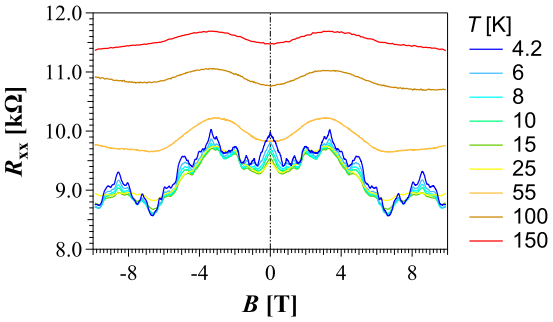
Fig. 2.10a shows the measured Hall resistance $R_H = \frac{V_{24}}{I_{13}}$ in the device, where we observe its quenching for $|B| \lesssim 2.25$ T until relatively high temperatures (55K). This is a direct consequence of ballistic transport of electrons at the center of the nanoscale cross. Electrons moving without collisions across the device present a probability to end up in lead 3 much higher than in leads 2 and 4, even if the Lorentz force exercised by the magnetic field imposes a preferential direction [66]. In the Büttiker and Landauer formalism $R_H = \frac{h}{q^2} \frac{(T_2 - T_4)}{[2T_3(T_3+T_2+T_4)+T_2^2+T_4^2]}$, where T_i is the transmission probability to the i-th lead [64]. The ballistic injection of electrons results in $T_3 \gg T_2 \simeq T_4 = 0$, hence $R_H = 0\ \Omega$. In these conditions, electrons move along transverse states [66] (inset of Fig. 2.10a), where the Lorentz force does not induce a significant change in transmission probability with respect to $B = 0$ T (inset of Fig. 2.10a).

Beyond B ~ ±2.25 T, the force exercised by the magnetic field is strong enough to inject electrons to a transverse lead (2 or 4 depending on the sign of B), which breaks the symmetry, raising R_H towards a second plateau. This so-called "last plateau" is a consequence of the absence of back-scattering due to the guiding of electrons through edge states when $l_c \leqslant W_{NW}^{eff}$ (where $W_{NW}^{eff} = W_{NW} - 2W_{sd}$ is the effective width of the nanowire). This occurs for $B < B_0 = \frac{\hbar k_F}{q W_{NW}^{eff}}$ (with k_F being the Fermi wavevector), when the Hall resistance saturates at $R_{H_0} = \frac{h}{2q^2} \frac{\pi}{k_F W_{NW}^{eff}}$, which is the quantum resistance of a quasi-1D nanowire [67]. The independence of the R_H on B holds until $2l_c < W_{NW}$, thus for $B_0 < B < 2B_0$.

To evaluate B_0 and R_{H_0}, W_{NW}^{eff} is determined from the plot of the longitudinal resistance $R_{xx} = V_{13} / I_{13}$ versus B (Fig. 2.10b). The shoulders observed in R_{xx} at $B_s = \pm 3.34$ T are a consequence of back-scattering of electrons, a geometrical phenomenon responsible for the observed peaks



(a) Hall resistance versus magnetic field.



(b) Longitudinal resistance versus magnetic field.

Figure 2.10 – R_H (a) and R_{xx} (b) versus magnetic field when a bias voltage of 100 μV is applied.

in R_{xx} when $W_{NW}^{eff} \sim 0.55 l_c$ [68, 69]. This relationship results in $W_{NW}^{eff} = \hbar k_F / q B_s = 48$ nm, $B_0 = 6.1$ T and $R_{H_0} = 1.92$ kΩ, in excellent agreement with our experimental results (Fig. 2.10a). We cannot observe the end of the last plateau since $2B_0 = 12.2$ T is not achievable with our experimental set-up.

From W_{NW}^{eff}, we estimate a small sidewall depletion of 19.5 nm in AlGaN/GaN, which highlights another advantage of this material for the study of ballistic transport in top-down etched nanoscale devices. The fluctuations observed in R_{xx} and in R_H, as well as the peak observed in R_{xx} at 0 T are signatures of universal conductance fluctuations [45, 46] and weak localization [43, 44], respectively. The variance of UCF was used to extract a phase coherence length (l_ϕ) of 190 nm [45, 46]. The much larger l_ϕ compared to W_{NW} supports quantum interference observed up to ~ 25 K which resulted in WL and UCF (Fig. 2.10a and 2.10b). At larger temperatures, the thermal energy smeares out all these magneto-anomalies resulting in classic-like Hall behavior. Hall measurements also allow us to determine the carrier density in the 2DEG in the nanoscale cross. In classical Hall effect, the Hall resistance depends on B as $R_H = B/(q n_s)$ yielding $n_s = 3.1 \times 10^{12}$ cm^{-2} at 4.2 K (in this case a larger bias of 300 mV was used to avoid the presence of quantum fluctuations) and 2.78×10^{12} cm^{-2} at 300 K. The smaller values of n_s in the nanoscale cross compared to bulk values were due to sidewall depletion and strain relaxation of the AlGaN barrier in narrow structures [70]. The estimated l_m using these values of n_s was 51 nm at 300 K

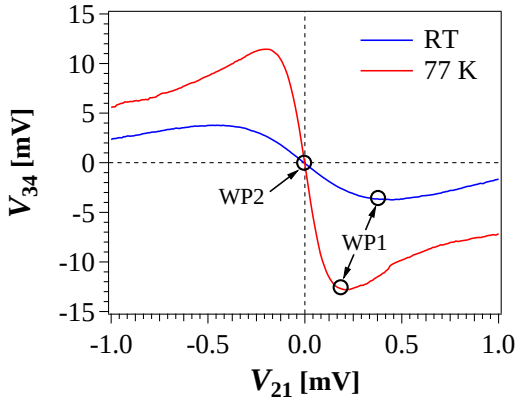


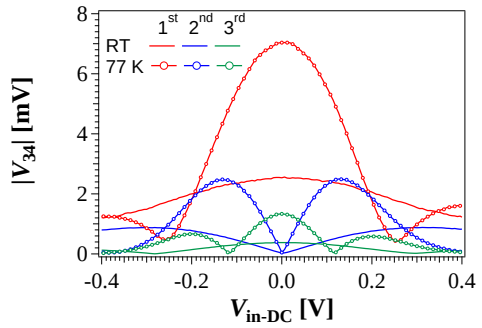
Figure 2.11 – V_{34} versus V_{21} at room temperature and 77 K. Two working points are identified for both curves which will be analyzed during the harmonic generation study.

and 313 nm at 4.2 K.

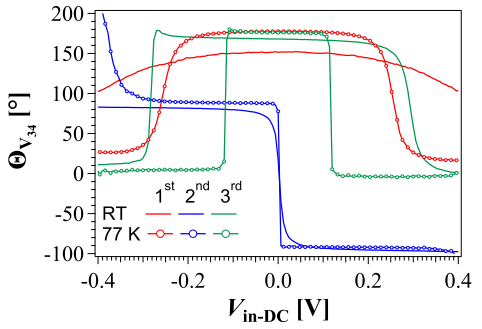
2.7 From physics to applications: frequency multiplication

The high speed of ballistic electrons combined to the non-linear behavior of V_{34} versus V_{21} was used to generate higher-order harmonics at RT and 77 K. Fig. 2.11 show V_{34} versus V_{21} for a 50 nm-wide NW-based cross etched from an AlInN-barrier HEMT at room temperature and at 77 K. In both cases, we observe the inverting behavior in V_{34}, which is the consequence of the ballistic transport of electron; moreover, the amplitude of such voltage is 3X larger at 77 K because of the larger mobility of electrons (which translates in a reduced probability to be scattered). The knee voltage is also different in the two curves and this is associated with the reduction of access resistance at 77 K and to the fact that in this measurement we report V_{21} and not V_{wire}. For the illustrated curves, we identify two interesting working points, WP1 at the knee voltage and WP2 at the inverting region, to perform AC measurements using a high-frequency 2-input locking amplifier from Zurich Instruments (HF2LI). The measurement consists of supplying a sinusoidal signal with an offset between lead 2 and 1 and measuring the voltage between leads 3 and 4.

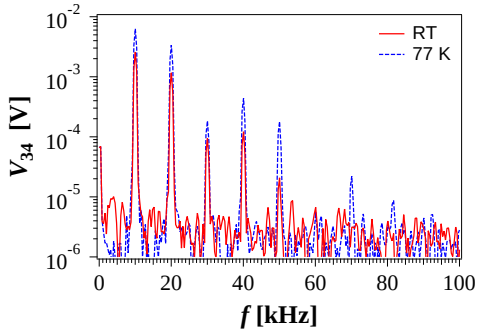
The study of the harmonic generation process starts by sweeping $V_{\text{in-DC}}$ and measuring the magnitude and phase of the first three harmonics. For $V_{\text{in-DC}} \sim 0$ V and at 77 K, the inverting behavior due to ballistic transport yields a fundamental harmonic shifted by 180° with respect to the input signal, in addition, also the 3$^{\text{rd}}$ harmonic unexpectedly appears with the same phase shift of the fundamental. For larger values of $V_{\text{in-DC}}$, both the 1$^{\text{st}}$ and 3$^{\text{rd}}$ fade whereas the 2$^{\text{nd}}$ becomes more dominant with a peak in magnitude for $V_{\text{in-DC}}$ close to the knee voltage (WP2 in Fig. 2.11), as a consequence of the quadratic behavior observed in the DC measurements. A further increase of $V_{\text{in-DC}}$ produces the attenuation of the 2$^{\text{nd}}$ harmonic while the fundamental magnitude starts to rise again. Similar results are reported for the measurement at RT, even



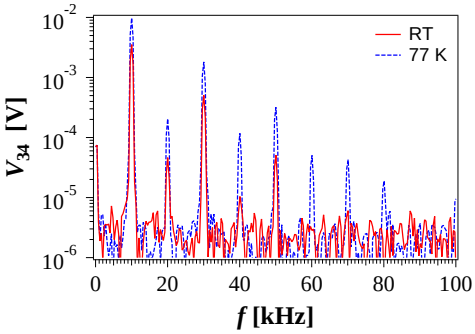
(a) Magnitude of V_{34} for the first three harmonic versus $V_{\text{in-DC}}$.



(b) Phase of V_{34} for the first three harmonic versus $V_{\text{in-DC}}$.



(c) Spectrum of V_{34} at the working point 1.



(d) Spectrum of V_{34} at the working point 2.

Figure 2.12 – $|V_{34}|$ (a) and $\Theta_{V_{34}}$ (b) of the first three harmonic versus $V_{\text{in-DC}}$ at RT and 77 K. (c) and (d) Spectrum of V_{34} at RT and 77 K for the working points optimized to generate the 2nd and 3rd harmonics, respectively.

though the magnitude of all harmonics at any $V_{\text{in-DC}}$ is 2-3 times smaller than at 77 K and the phase behaviors are less sharp.

An optimization process with respect to V_{21}^{AC} and V_{21}^{DC} is run to improve the efficiency and spectral ratio of the 2nd and 3rd harmonics over the fundamental harmonic. Higher-order harmonics are not considered since it is challenging to produce them individually; therefore, the obtained spectral purity is inferior. The efficiency for the i$^{\text{th}}$ harmonic, defined as $\eta^{\text{i}^{\text{th}}} = V_{34}^{\text{i}^{\text{th}}} / V_{21}^{\text{AC}}$, reflects the harmonic generation process with respect to the input signal, while the spectral ratio, defined as $R_{\text{S}}^{\text{i}^{\text{th}}/1^{\text{st}}} = V_{34}^{\text{i}^{\text{th}}} / V_{34}^{1^{\text{st}}}$, reflects the amplitude ratio of the i$^{\text{th}}$ harmonic over the fundamental harmonic. The input signal frequency was set at 10 kHz to avoid distortion and attenuation caused by the impedance mismatch in the nanoscale device and loading effect of the measurement instrument, which limited the frequency measurements to less than 100 kHz. The results of the optimization process for the generation of the 2nd and 3rd harmonics are summarized in Tab. 2.2. The harmonic generation process is very promising for the 2nd harmonic with a spectral ratio of more than 50 % at both RT and 77 K, while it is less strong for the 3rd harmonic. Fig. 2.12c and 2.12d show

Table 2.2 – Efficiency ($\eta^{i^{th}}$) and spectral ratio over the fundamental harmonic ($R_S^{i^{th}/1^{st}}$) for the 2nd and 3nd at the optimized working points (WPs) (V_{21}^{AC}, V_{21}^{DC}) at RT and 77 K.

WP	$V_{in\text{-}AC}$ [mVpp]		$V_{in\text{-}DC}$ [mV]		$\eta^{i^{th}}$ ‰		$R_S^{i^{th}/1^{st}}$ [%]	
	RT	77 K	RT	77 K	RT	77 K	RT	77 K
1	200	100	282	125	2.2	12.5	52.9	53.1
2	200	100	0	0	0.9	6.7	14.9	18.9

the spectrum of V_{34} at the two optimized working points for the 2nd and 3rd harmonic generation, where we also observe the presence of higher-order harmonics. In both cases, the amplitude of the two harmonics (2nd and 3rd in the respective WPs) is more than ten times larger than the others, which ensures a good spectral purity (better at RT). These measurements showed that ballistic devices can be promising to generate higher-order harmonics even at RT, even though the present devices were passive with a low differential output power.

2.8 Conclusion

In conclusion, we report the use of an electron filter based on two crossing etched NWs for investigating different transport regimes. Ballistic transport is observed even at room temperature thanks to the high mobility of III-Nitrides HEMTs together with the high optical phonon energy. Ballistic transport of electrons is also analyzed under a transverse magnetic field to manipulate the trajectory of electrons. In high-bias condition, a strong dependence of V_{34} on both magnetic field and bias voltage results in transition points (for 2 T < B < 3.6 T) with a pronounced non-linear behavior revealing the equilibrium between straight and circular trajectories of ballistic electrons.

We also correlate the ballistic behavior with semiclassical and quantum effects by measuring the same device in a Hall configuration, which highlights the interaction of the scattering-less ballistic transport with Lorentz forces in bending the electron trajectory and creating edge states for electron propagation. Hall measurements revealed the quenching of Hall resistance and the manifestation of the last plateau (saturation of the Hall resistance) in excellent agreement with the theoretical value of the quasi-1D resistance R_{H0}. A long measured phase coherence length of 190 nm allowed the observation of universal quantum fluctuations and weak localization due to quantum interference up to ~25 K.

Finally, we investigated the non-linear behavior of the ballistic crosses to generate high order harmonics at both room temperature and 77 K, demonstrating a 50% energy transfer from the fundamental harmonic to the 2nd one; besides with the generation of the 3rd harmonic, both with high spectral purity in the respective optimized working points.

3 New gating techniques

3.1 Introduction

In this chapter, we will discuss different gating techniques to improve the performance of RF transistors based on etched HEMT NWs with sub-micron gate length. In particular, we investigate side-gate control to replace tri-gate and reduce parasitic capacitance contributions and trapping mechanisms. First, we propose in-plane-gate FETs, to study side gating, demonstrating very good control which can be improved by healing dry etching damages with TMAH treatment. Then we present metal IPGFETs (M-IPGFETs) as the evolution of IPGFETs, which can ensure better control, low gate resistance, and better scalability. Finally, we conclude with a small summary of the chapter. Most of the shown results are from Ref. [36].

3.2 From planar gate to tri-gate

One of the most important geometrical features of lateral transistors (e.g. MOSFETs, MISFETs, MOS-HEMTs, etc.) is the gate length (L_g), which defines the length of the conductive channel whose carrier concentration is modulated by the applied gate voltage. Independently from the application, usually switches or amplifiers, the gate length directly influences the maximum frequency at which a lateral device can work. Shorter lengths result in higher operating frequencies since carriers need to cross a shorter path before reaching the drain terminal. The process of reducing the gate length is called gate scaling and, conventionally, a technological node includes all the technology, tools and fabrication process required to fabricate a device with a gate length defined by the node (e.g. the 9 nm node, or process, refers to the realization of devices with a gate length of 9 nm).

Gate scaling is a very complicated operation since it requires a lot of innovation from the technological point of view (new micro and nanotechnology tools, as well as improvements in the fabrication process flows) and an in-depth study of the effect of shorter gate lengths on other device parameters such as the threshold voltage (V_{th}), the on/off current ratio, the leakage

current, the gate current, and the breakdown voltage. Furthermore, when reducing the gate length, especially in the sub-micrometer range, new physical phenomena may happen, such as ballistic transport, and gate control weakens with the manifestation of short-channel effects.

The strength of the gate action can be quantified by the transconductance (in the linear region, $I_d \sim g_m V_{gs}$) and by the subthreshold slope (SS) in the exponential region ($I_d \propto \exp\frac{V_{gs}}{V_t}$) of a device. The most known reference value for SS is 60 mV/dec, which is the smallest and best value obtainable in any later field-effect transistor with common materials (more exotic materials, such as ferroelettric ones, can replace the oxide layer in MOSFETs to reduce SS below 60 mV/dec yet using a FET device [71]).

In HEMT based devices, the reduction of SCE is guaranteed if the ratio between the gate length and the gate-to-2DEG distance is in the range from 5 [20] to 15[21], depending on the materials. Considering the optimistic value of 5 for the ratio and neglecting any technological issue, this would imply that, for a gate length of some tens of nm, the distance between the channel (2DEG) and the gate should be few nm. At this scale, the tunneling gate current can be considerable, reducing the gate control and other parameters such as the operating power.

This sets an important limit for devices (called planar), where the gate is parallel to the conductive channel, and the entire structure can be seen as a parallel plate capacitor.

The most known solution to this issue is to increase the gate surface over the channel surface by exploiting 3D structures. NWs fulfil this function since the rectangular cross-section allows up-to-4 times increase of the gate surface with strong improvements in gate control [72–75]. The drawback of 3D structuring is an increase in parasitic capacitance, which can strongly limit the frequency capabilities.

3.3 Gated NWs

3.3.1 From planar gate to side gates

Fig. 3.1a shows the cross-section of a planar MESFET based on a HEMT structure. The electric field interaction between the gate and the 2DEG (black arrows in the figure) is similar to that of a parallel plate capacitor. The same situation is also illustrated in the case of a top-gated NW (Fig. 3.1b); in particular, the fringe electric field (arrows outside the NW region) starts to play an important role in modulating the 2DEG density. The electrostatic interaction between the gate and the 2DEG can be modeled by the gate capacitance (C_g), whose expression per unit of length can be approximated to $C'_g = \epsilon_0 \epsilon_b \frac{W_{NW}}{t_b}$ (where ϵ_b and t_b are the relative dielectric constant and thickness of the barrier, respectively). Such expression is identical to that of a parallel plate capacitor and holds until $W_{NW} \gg t_b$, while, if the two dimensions get comparable, the fringe electric field is not negligible anymore. The tri-gate technology better exploits the NW geometry by controlling the channel also from the two sides (Fig. 3.1c). However, for narrow NWs (few t_b

(a) Planar MESFET. (b) Top gate NW. (c) Tri-gate NW. (d) Side gate NW.

Figure 3.1 – (a) to (d) Cross-section schematic of a planar MESFET, top gate NW, tri-gate NW, and side gate NW, respectively, with black arrows representing the electric field interaction between the gate and the 2DEG channel.

large), the main control of the channel originates from the sides of the gate, while the top part has a negligible influence. Moreover, especially in the cases of barriers with several defects and traps (such as in the case of AlGaN barriers for GaN HEMT), the top gate produces electron trapping and more parasitic capacitance.

Side-gate technology (Fig. 3.1d) becomes more suitable for narrow NWs since it allows direct and effective control of the NWs in an efficient area, hence reducing both trapping phenomena and parasitic capacitance. Unfortunately, the geometry proposed in Fig. 3.1d is not easy to realize and the topic of this chapter is to show a pathway toward side gating.

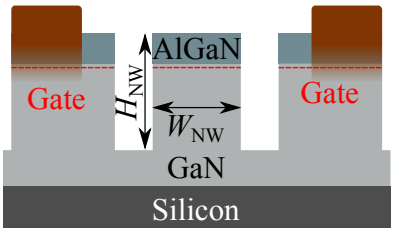
3.3.2 In-plane gate field-effect transistor

The investigation of side gating can be performed by using in-plane gate field-effect transistors (IPGFETs). Fig. 3.2a shows the schematic of an AlGaN/GaN IPGFET where air trenches separate the channel from the gates, which are also based on the 2DEG and connected to the gate terminals by ohmic contacts. The working principle is based on modulating the carrier concentration of the NW 2DEG by laterally applying an electric field trough the 2DEG layers in the two side gates.

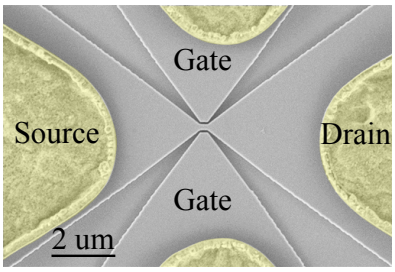
2DEG of the two in-plane gates which are usually separated from the central NW by etched trenches.

The fabrication process of IPGFETs is relatively simple and consists of two major steps: the definition of a NW channel and in-plane gates, and the formation of ohmic contacts for every terminal (gates included). The first step can be achieved using e-beam lithography, followed by dry etching, or by direct etching employing focused ion beam. In the case of etched trenches, air serves as dielectric removing a lot of uncertainties related to the use of dielectric layers. Both the simple process flow and the absence of dielectric layers make the IPGFET architecture ideal for studying side gating as well as to be used as a starting point for scaling up side gate devices.

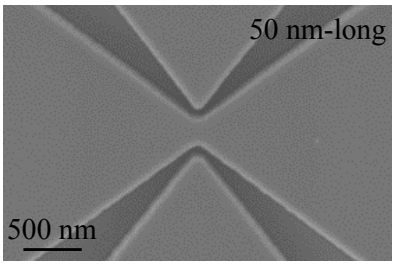
The study of IPGFETs started in the 90s by using narrow-gap III-V HEMTs such as AlGaAs/GaAs



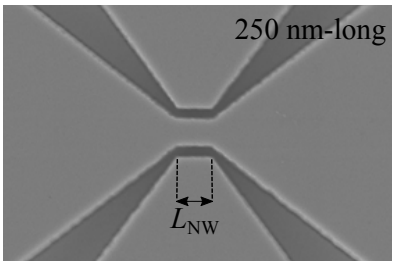
(a) Schematic of an IPGFET cross section.



(b) SEM of an IPGFET.



(c) SEM of a 50 nm-long IPGFET.

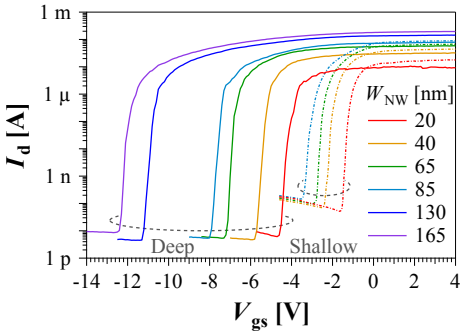


(d) SEM of a 250 nm-long IPGFET.

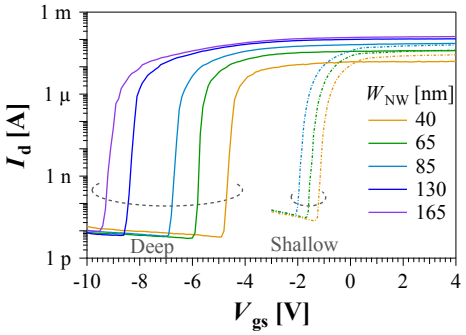
Figure 3.2 – (a) Schematic of the cross-section of an IPGFET. (b) False-colored SEM image of an AlGaN/GaN IPGFET. (c) and (d) Magnified SEM images of a 50 nm-long and 250 nm-long IPGFETs, respectively.

at 300 K [76–81], GaAs/InGaAs/AlGaAs at 300 K [82], InGaAs/InP at 4 K [83] and InAlAs at 300 K [84]. Interesting phenomena have been observed in these structures, such as negative differential resistance [84] and quantum ballistic transport [85]. Although a good gate control has been demonstrated for IPGFETs in the literature, the relatively small electron density in the 2DEG and the very low critical breakdown field of narrow-gap III-V semiconductors have yielded small output current and breakdown voltage, and consequently limited output power. Furthermore, the low carrier concentration set a limitation on the geometrical size of NWs and the effectiveness of the gate control when performing a dry-etching process. As deeply explained in Sec. 2.5.1, the sidewall depletion in many III-V HEMTs can be as large as hundreds of nm, implying NW widths relatively large for which side gating is not efficient. Besides, since there is no 2DEG close to the gate edges facing the NW, the side gating action is weakened even more.

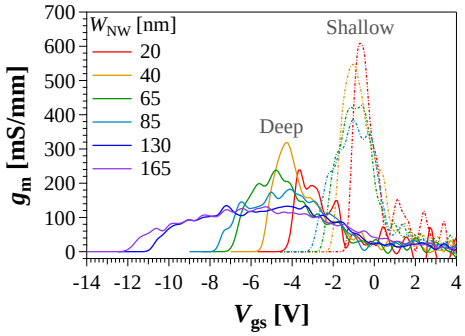
On the other hand, III-Nitride HEMTs are known to have a sidewall depletion width in the range of few tens of nm (Sec. 2.6), which allows fabricating IPGFETs with very narrow NWs and better control. In the following sections, we will discuss the first high-performance AlGaN/GaN IPGFETs which overcome, both in current density and transconductance, any other IPGFET in the literature. Then we will talk about the optimization of device performance and its evolution into the metal IPGFETs (M-IPGFETs) to meet the requirements for RF devices (such as small gate resistance).



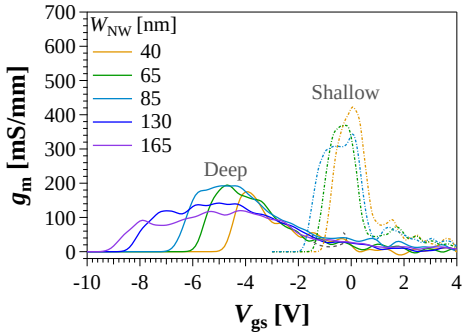
(a) Transfer curves of 50 nm-long IPGFETs.



(b) Transfer curves of 250 nm-long IPGFETs.



(c) Transconductance of 50 nm-long IPGFETs.



(d) Transconductance of 250 nm-long IPGFETs.

Figure 3.3 – (a) and (b) I_d versus V_{gs} in logarithmic scale for IPGFETs based on 50 nm-long and 250 nm-long NWs, respectively. (c) and (d) g_m versus V_{gs} for IPGFETs based on 50 nm-long and 250 nm-long NWs, respectively. For all the figures, solid curves refer to Deep IPGFETs while dashed curves refer to Shallow ones.

3.4 AlGaN/GaN IPGFETs

IPGFETs are fabricated on $Al_{0.25}Ga_{0.75}N$ (23.5 nm)/AlN (8 nm)/GaN (300 nm) followed by a 3.75 μm-thick buffer on a silicon substrate. The electron mobility (μ_e), carrier concentration (n_s) and sheet resistance (R_{sh}) of the epitaxial structure measured at 300 K are 1.05×10^{13} cm^{-2}, 1690 cm^2/Vs and 350 $\Omega/\square$, respectively. The fabrication process is the one reported in the Appendix A.1 (but it ends at step 6) and Fig. 3.2b shows a completed IPGFET. We fabricate devices with channel lengths (L_{NW}) of 50 nm (Fig. 3.2c) and 250 nm (Fig. 3.2d) and widths (W_{NW}) varying from 20 nm to 165 nm. 60 nm-wide isolation trenches were etched with two nominal trench depths (H_{NW}) of 140 nm (Shallow) and 210 nm (Deep) as measured in the mesa regions (the depth within the narrow trenches may be smaller than these values). For simplicity, when comparing IPGFETs based on nanowires having different dimensions, we will characterize IPGFETs with adjectives referring to the NW, e.g. a short IPGFET is an IPGFET with a short NW.

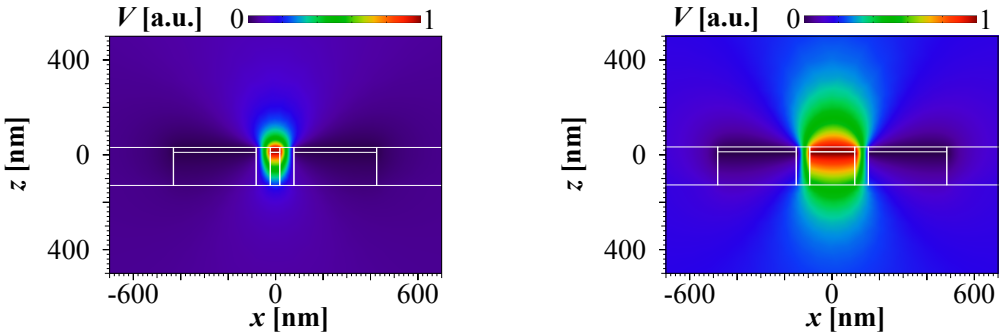
3.4.1 Transfer characteristics and capacitance simulations

Fig. 3.3a and 3.3b show the transfer characteristics for L_{NW} of 50 nm and 250 nm, both for the Shallow and Deep samples. For a fixed L_{NW} and H_{NW}, I_d decreases for narrower channel devices, due to the higher resistance. In addition, the more pronounced strain relaxation of the AlGaN barrier in NWs with smaller width causes a decrease of 2DEG carrier concentration [70, 86], thus reducing I_d and $|V_{th}|$. These devices present a large on-off ratio up to 10^7 with a small leakage current of less than 10 pA for the Deep and 100 pA for the Shallow devices, revealing an excellent channel control from the in-plane gate with air dielectric. For a fixed W_{NW}, an increase in I_d along with a more negative V_{th} is observed by reducing the length of the nanowires from 250 nm to 50 nm (Fig. 3.3a), which is again expected due to the smaller resistance of the wire and the reduced strain relaxation in the 50 nm-long devices. The subthreshold slope ranges from 60 mV/dec, for small W_{NW}, to 100 mV/dec for larger NWs, indicating poorer control for the latter and confirming that side gating is efficient for narrow NWs mainly. Double-sweep transfer characteristic measurements (not shown) reveal a ΔV_{th} of about 0.2 V - 0.3 V, which is independent of device geometry and channel sizes. Such ΔV_{th} can be associated with the presence of traps in the AlGaN barrier and on the etched sidewalls, which can be mitigated by passivating the device.

The depth of the etched trenches that isolate the gate and channel regions has an important impact on the device performance. By reducing H_{NW} while maintaining W_{NW} constant, we observed a significant positive shift in V_{th} for all device widths, which reveals an increase in gate capacitance for the shallower trenches (discussed in more details later).

Fig. 3.3c and 3.3d show the normalized transconductance (over the NW width) of the 50 nm-long and 250 nm-long IPGFETs at V_{ds}= 1 V, revealing larger and broader g_m for wider nanowires. IPGFETs based on shorter NWs have 20% larger transconductance. In first approximation, we can write $g_m \sim \frac{I_{d\text{-}max}}{|V_{th}|}$, where both $I_{d\text{-}max}$ and V_{th} increase for shorter NWs. Since g_m is larger for shorter NWs, this suggests a stronger dependence of the $I_{d\text{-}max}$ versus the L_{NW} then V_{th} versus the same. A significant increase of transconductance, together with a less flat behavior, was observed for the Shallow devices. The normalized (with respect to W_{NW}) g_m was larger for smaller NW widths, due to the improved modulation over the narrower channels, and ranging from 335 mS/mm for 85 nm-wide channel to 665 mS/mm for the 20 nm-wide channel, which is nearly 5x-larger than the best IPGFET [82].

The NW width, as well as the trench width and depth, strongly determine the type of control and the gate capacitance. Fig. 3.4a and 3.4b show the COMSOL simulated electric potential distribution for two IPGFETs having a narrow (40 nm) and a wide (200 nm, roughly 10X larger than the barrier thickness) NW, respectively. The potential is strongly localized for the narrow NW, resulting in an electric field that is mainly confined around it, whereas the potential spreads much more for the wider IPGFET. In such case, the generated electric field extends deeply into the buffer, where traps can be activated, possibly resulting in a trap-control based device instead of a field-effect control [87]. A similar consideration can be done also in the case of IPGFETs



(a) Potential distribution for a narrow IPGFET.

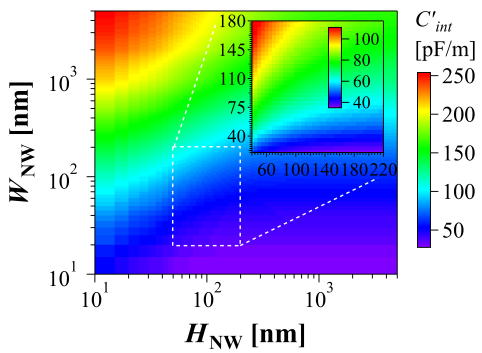
(b) Potential distribution for a large IPGFET.

Figure 3.4 – (a) and (b) Potential distribution in IPGFETs based on a narrow ($W_{NW} \sim t_b$) and a wide ($W_{NW} \gg t_b$) NW, respectively.

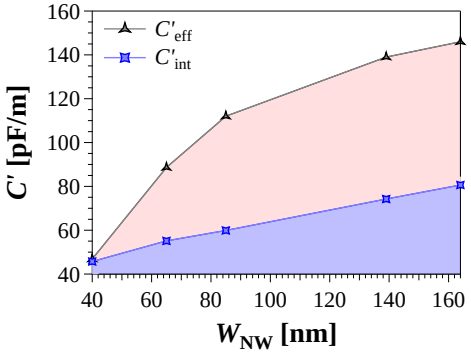
with larger trench widths; in particular, this parameter should be reduced to allow larger NWs or improved control (e.g. smaller *SS*). IPGFETs with zero trench width, called by the authors three-terminal nanojunction [88], have also been fabricated and they have shown *SS* below 60 mV/dec (at low V_{ds}).

Concerning the gate capacitance, we differentiate two contributions, namely the intrinsic and extrinsic (or parasitic) capacitance. The former represents the electrostatic interaction between the charges into the NW and the applied gate voltage, while the latter refers to the interaction between the gates and the 2DEG in the rest of the IPGFET. Fig. 3.5a shows the intrinsic capacitance per unit of length (C'_{int}) simulated using the same structure of Fig. 3.4a and 3.4b while changing the NW width and trench depth, both between 10 nm and 5000 nm. On average, the intrinsic capacitance increases for wider nanowires (similarly to what happens in a parallel plate capacitor but with a sublinear dependence) and for shallower trenches. The latter is caused by a larger overlap of the electric field lines over the semiconductor with respect to deeper trenches, where the electric field spread mainly in air. Since GaN has a dielectric constant about 10X bigger than the air (vacuum) one, this yields a larger capacitance. In the inset of Fig. 3.5a, we vary both W_{NW} and H_{NW} in the range of the fabricated devices (since we do not know exactly the trench depth, we consider values smaller than 140 nm due to the load effect during the dry-etching). The inset emphasizes more the increase of intrinsic capacitance for shallower trenches, especially for very narrow or very wide NWs. In first approximation, we can write that $V_{th} \sim \frac{-qn_s}{C_{int}}$, thus larger capacitance values result in more positive threshold voltage (smaller in absolute value) and larger transconductance values (considering the approximation $g_m \sim \frac{I_{d\text{-}max}}{|V_{th}|}$), with the latter indicating a stronger channel control. Such relation explains the more positive V_{th} and larger g_m measured for shallow IPGFETs than for deep ones. Other effects may also influence the channel for deeper etchings, such as a larger strain relaxation of the barrier that reduces n_s and further shifts V_{th} towards positive values.

In Fig. 3.5b we report the intrinsic capacitance simulated from COMSOL and the total capacitance



(a) Simulated intrinsic capacitance of IPGFETs.



(b) Capacitance contributions in IPGFETs.

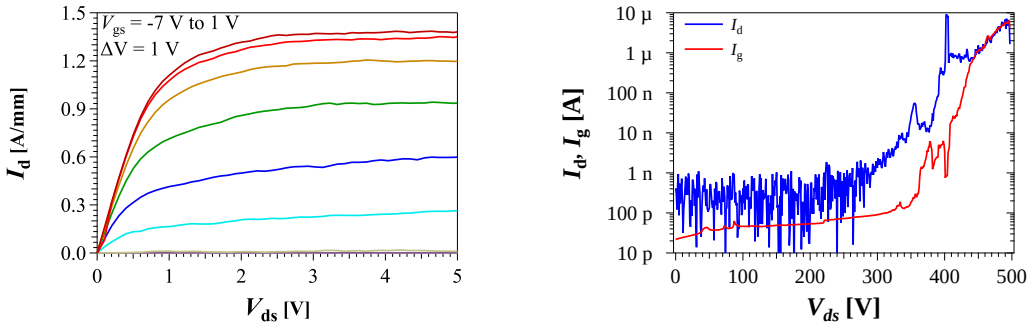
Figure 3.5 – (a) Simulated intrinsic capacitance per unit of length versus NW width and height. (b) Effective capacitance, calculated as $\frac{-qn_s}{V_{th}}$, and intrinsic capacitance for IPGFETs. The difference between the two curves can be associated with the extrinsic capacitance.

Table 3.1 – Characteristics of the 50 nm-long Shallow and Deep IPGFETs. f_T was estimated as $f_T \approx g_m/2\pi C_{eff}$.

	w [nm]	n_s [$e12$ cm^{-2}]	C_{eff} [aF]	g_m [μS]	f_T [THz]
Shallow	20	1.9	2.2	12.4	0.89
	40	3.1	4.6	22.1	0.77
	65	4.0	8.5	27.9	0.53
	85	4.3	9.4	33.2	0.56
Deep	20	1.9	0.7	3.9	0.89
	40	3.1	1.8	9.3	0.82
	65	4.0	3.1	14.4	0.75
	85	4.3	3.9	14.7	0.60

extracted from measurements, which can be interpreted as the sum of the extrinsic and intrinsic capacitance. The latter is calculated using the relation $C'_{eff} = \frac{-qn_s}{V_{th}} W_{NW}$, where n_s is obtained from measuring, as Hall bars, electron-filter crosses fabricated on the same chip (same procedure described in Sec. 2.6) while V_{th} is extracted from the transfer characteristics at I_d= 1 nA. The light red region in the plot represents the difference between the effective and simulated capacitance, thus the extrinsic capacitance of IPGFETs.

The total effective capacitance for short IPGFETs (50 nm-long NWs) estimated as $C_{eff} = C'_{eff} L_{NW}$ was in the range of 0.7 aF (20 nm-wide) to 3.9 aF (85 nm-wide) for the Deep, and 2.2 aF (20 nm-wide) to 9.4 aF (85 nm-wide) for the Shallow devices (Tab. 3.1). These are extremely small values of gate capacitance, which are very promising for high frequency applications. The estimated cut-off frequencies $f_c \approx g_m/2\pi C_{eff}$ for IPGFETs are up to 0.89 THz. Tab. 3.1 summarizes the characteristics of the 50 nm-long IPGFETs.



(a) Output characteristic.

(b) Breakdown measurement.

Figure 3.6 – (a) I_d versus V_{ds} for a 50 nm-long and 85 nm-wide IPGFET for V_{gs} varying from -7 V to 1 V. (b) I_d and I_g versus V_{ds} in the off-state.

3.4.2 Output characteristic and breakdown test

Fig. 3.6a shows the output characteristics of a 50 nm-long 85 nm-wide shallow IPGFET. A large current density of 1.4 A/mm was observed, which is over 9x-larger than the best IPGFET [82] based on an InGaAs quantum well, due to the much larger carrier density and very small sidewall depletion in III-Nitrides [35, 61].

Fig. 3.6b shows the breakdown voltage measurement for the 165 nm-wide 250 nm-long IPGFET in off-state (V_{gs} = -11 V), revealing a small drain I_d and gate I_g leakage currents, below 1 nA and 100 pA respectively, even at 300 V, along with a very high breakdown voltage of 500 V (regardless of the width of the devices). The similar behavior of I_d and I_g suggests that at large voltages the leakage current flows entirely through the semiconductor buffer layers, not through the nanowires, since both the drain and gate contacts are ohmic. Furthermore, the device performance and breakdown characteristics are not hindered by the dielectric quality, since air trenches serve as dielectric in these IPGFETs.

3.4.3 Healing of dry-etching damages on the sidewalls

Top-down NWs require a dry-etching process, which results in damages on sidewalls, depending on the process parameters. These defects make sidewalls rough, reducing the mobility in the channel, and full of traps, which may lead to not optimal dynamic behavior.

Two of the most common techniques to heal dry-etching damages are the cycled treatment and wet etching. The former is similar to the digital etching explained in Sec. 1.5.2, while the latter is an anisotropic wet etching process. In general III-Nitride compounds are very difficult to be wet etched due to the strong chemical stability. Base solutions, such as sodium hydroxide (NaOH) and potassium hydroxide (KOH) [89], have been demonstrated as possible solutions; however, they result also in an alkali metal contamination which may induce threshold voltage

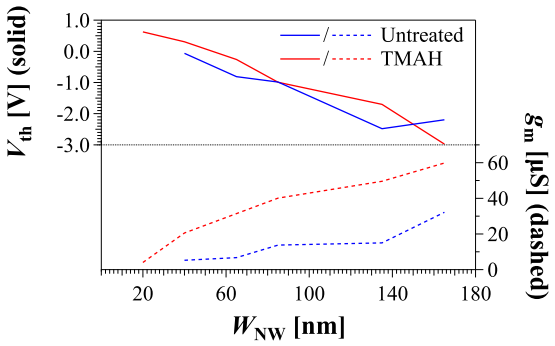


Figure 3.7 – V_{th} and g_m versus NW width for untreated and TMAH-treated IPGFETs.

instability [90]. Tetramethylammonium hydroxide (TMAH) etching, instead, does not produce any contamination, thus it is more suitable for devices based on NWs. The etch rate of TMAH depends on the solution concentration (from 2% to 25%), temperature (up to 80-90 °C) and exposed material face; in particular, the etch rate is very slow with all the faces aligned with the c-plane (which implies very slow vertical etching) and a-plane.

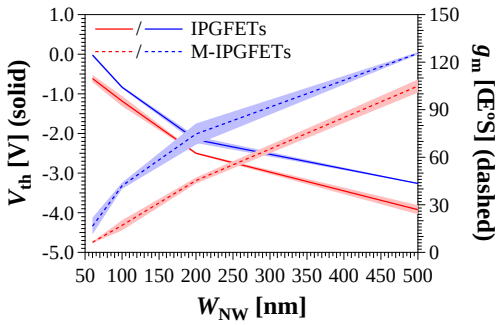
Despite the common knowledge, the etch rate of faces aligned with the a- and c-plane is not negligible, especially when etching NWs. Tests performed using TMAH 5% at 80 °C show a very difficult control, yielding in a complete etch of crystal-aligned NWs after few minutes. Besides, we also observed that the etch rate changes even with respect to the aluminum composition with more Al-reach compounds being etched faster. After several optimizations, a temperature of 40 °C and a treatment time of 1-2 minutes are found to be the best parameters for the process.

Fig. 3.7 shows V_{th} and g_m for both untreated and TMAH-healed IPGFETs, where the reported values are obtained from transfer characteristics at V_{ds} = 1V. On average, the threshold voltage is not strongly affected by the treatment; however, it allows achieving working normally-off devices while this is not possible with untreated IPGFETs. Despite the e-beam technology enables the definition of very narrow NWs, the etching process strongly damages them and their reliability is quite low unless treated. As a further advantage of the TMAH treatment, IPGFETs are characterized by an up-to-3X larger transconductance.

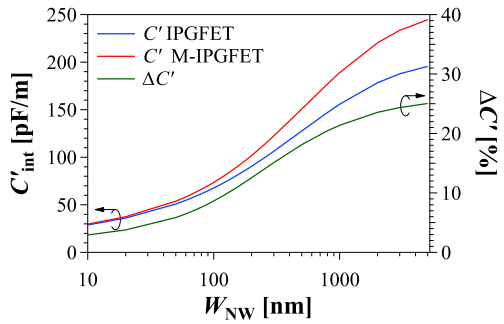
3.5 Metal-IPGFETs: a step towards scaled-up devices

IPGFETs have shown extremely good gate control capabilities which path the way for side gating. The next step is the optimization of other parameters that strongly influence the RF behavior of lateral FETs, as well as to find a scaling-up technology.

A fundamental requirement for RF transistors is a small gate resistance, which led to the development of several procedures for the fabrication of T-shaped gates (shortly T-gates). The control of the gate can be interpreted as the charge and discharge of the gate capacitance by the



(a) V_{th} and g_m for IPGFETs and M-IPGFETs.



(b) C'_{int} for IPGFETs and M-IPGFETs.

Figure 3.8 – (a) Threshold voltage and transconductance versus NW width for IPGFETs and M-IPGFETs (the shadows represent the standard deviation). (b) Intrinsic capacitance, for the same devices, and relative difference ($\Delta C' = \frac{C'_{\text{M-IPGFET}} - C'_{\text{IPGFET}}}{C'_{\text{IPGFET}}} 100$) versus NW width.

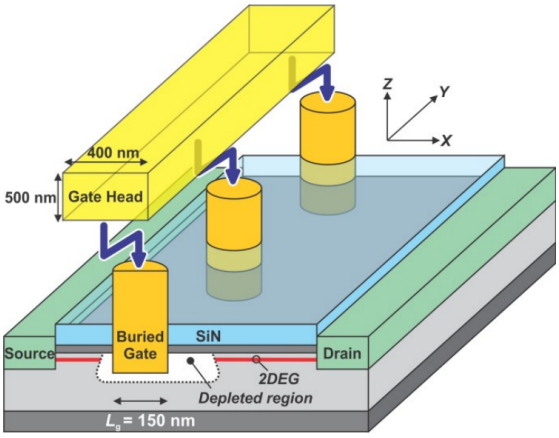
gate resistance (neglecting all the parasitic components) with a time constant $\tau_g = R_g C_g$. Since the gate capacitance should be relatively large to ensure proper control of the device (which translates in higher g_m, thus power gain), only R_g can be reduced to make the gate control faster. The idea of the T-gate is to have a small gate foot to minimize the source-drain distance (achieving larger f_c) and a large head to reduce the gate resistance.

Considering IPGFETs, the gate resistance is determined by the sheet resistance of the 2DEG and by the gate dimensions. The advantage of using III-Nitrides for such devices is the 10x larger carrier concentration of the 2DEG with respect to narrow-gap III-V HEMTs; nevertheless, such value is not enough to ensure a small gate resistance. Besides, considering the geometry of IPGFETs, higher current and gain values would require more devices connected in parallel, yielding a considerable increase of parasitic components due to the interconnections.

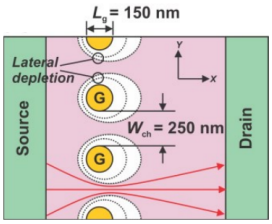
In metal IPGFETs, we replace the two side gates, made with the same structure as the channel, with two metallic gates. The metallic in-plane gates are much less resistive than 2DEG-based ones, besides interconnections among all the gates are easier to be fabricated.

We compare IPGFETs and M-IPGFET, which are both treated with TMAH and having the same dimensions. Fig. 3.8a shows V_{th} and g_m for IPGFETs and M- IPGFETs. The threshold voltage is more positive for metallic gates thanks to a larger capacitive coupling between the gates and the 2DEG of the channel. This also results in the 2x larger transconductance, which is very promising for RF applications. Other parameters, such as the off-current and subthreshold slope, are also improved in M-IPGFETs.

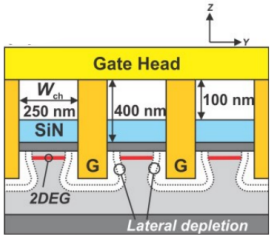
In Fig. 3.8b we show the simulated intrinsic capacitance versus W_{NW} for IPGFETs and M-IPGFETs with the same geometrical parameters. For any NW width, the capacitance is larger for M-IPGFET; more specifically, considering the relative increase ($\Delta C' = \frac{C'_{\text{M-IPGFET}} - C'_{\text{IPGFET}}}{C'_{\text{IPGFET}}} 100$) and the useful range of W_{NW}, the increase is between 5% and 15%. However, this does not explain



(a) 3D schematic of a BRIDGE FET.



(b) Schematic of the top view.



(c) Schematic of the gate cross section.

Figure 3.9 – (a) 3D schematic of the BRIDGE FET proposed in Ref. [91]. (b) Top view of the proposed device. (c) Cross section schematic at the gate section.

the doubling of transconductance, which can be associated with the absence of traps and defects on the gate sidewall. In usual IPGFETs, gates are made with the HEMT epistructure itself, thus they are sensitive to traps, especially those close to the sidewalls facing the NW channel since they can produce a screening action reducing the gate control effectiveness.

3.5.1 Scaled-up side-gate FETs

Metal IPGFETs demonstrate that side-control by metallic gates is achievable and very promising. A scaled-up version of M-IPGFETs is demonstrated by Shinohara et al. with their buried dual gates FET (BRIDGE FETs) [91]. Fig.3.9a and 3.9b show the the 3D schematic and the top view of the proposed devices, while Fig. 3.9c illustrates the cross-section at the gate in the y-direction. Considering an individual channel, this is controlled by the metallic gates at its two sides, similarly to M-IPGFET. The authors compared BRIDGE FET with planar T-gate HEMT having the same geometrical dimensions and they reported a flatter g_m, very promising for linear amplifiers, and a negligible drain-induced barrier lowering of 3 mV/V, resulting in a very small (and desired) drain conductance (g_d). Thanks to the flat g_m and small g_d, the authors demonstrate a much more uniform gain in BRIDGE FETs than in planar FETs.

3.6 Conclusion

In this chapter, we propose the side-gating technology as an alternative to the tri-gate one to control NWs etched from an AlGaN/GaN HEMT. Though the tri-gate technology is very efficient in controlling NWs with widths up to hundreds of nm, it increases the parasitic capacitance for very narrow NWs. In this case, side gating can be a better option since by removing the top gate, whose control capabilities over the 2DEG channel are weaker than the side gates due to the presence of the barrier (more than 20 nm), we can reduce both parasitic elements and trapping happening in the barrier. To demonstrate the effectiveness of side gating we investigated AlGaN/GaN IPGFETs. Devices show a much higher current (1.7 A/mm) and transconductance (660 mS/mm) than any other IPGFETs reported in the literature (considering any material). Very good control is also confirmed by an extremely small off current, a close to 60 mV/dec subthreshold slope and a breakdown voltage of more than 300 V over a single NW.

With M-IPGFET, we moved toward the requirements for RF transistors, since, thank the use of metal gates, we could sharply reduce the gate resistance. Also, we observed a doubling of the transconductance thanks to the absence of trapping effect in the gates (no more made with the same HEMT structure used for the channel).

As confirmation of this work, scaled-up devices based on metal side gating have been published, showing auspicious performance for RF applications.

4 GaN-HEMT zero-bias RF detectors

4.1 Introduction

In this chapter, we will discuss RF detection achieved in NW based field-effect rectifiers (NW-FERs) fabricated using a commercial RF GaN-HEMT wafer. The chapter starts with an overview of RF detectors, together with their figures of merit and state of the art about zero-bias RF detectors based on semiconductors. Then, we introduce the NW-FER concept and a full characterization, both in DC and RF, is given. Finally, we conclude with a small summary of the chapter. The shown results are from Ref. [37].

4.2 Radio-frequency detectors

A radio-frequency (or microwave) power detector is a device capable of generating an output DC voltage which is function of the RF power at the input of the device.

RF detection can be achieved in macroscopic and microscopic devices. The most famous bulky detector is the bolometer, which transforms the impinging energy (from radiation, photons, ionizing particle, etc.) into thermal energy that is sensed by a resistor whose resistance changes according to the temperature, thus the incident power into the device. Very high precision and sensitivity are achievable with bolometers, though the time constant related to the measurement process is quite large (because of the conversion of radiation power into heat) thus limiting the application of such devices in cases where the power is constant or changing slowly.

Microscopic RF detectors are based on semiconductor devices (usually Schottky diodes). The detection relays on rectifying the AC signal at the input and then extracting the DC value, which is proportional to the input power (Fig. 4.1). Diodes are usually much faster and smaller than bolometers, though they are less sensitive.

The detection law of the incident power varies substantially among microwave detectors [92]. The most used detectors are here listed:

- root mean square (RMS) power detectors: the DC voltage is directly proportional to the logarithmic of the RMS of the power at the input;
- peak (or envelope) detectors: the detector tracks the envelope (either positive or negative) of the AC input signal;
- square-law detectors: the DC output voltage is proportional to the square of the input voltage, thus linearly proportional to the input power.

Diodes can work either as envelope or square-law detectors depending on the input power $P_{\text{in-RF}}$ [93]:

- $P_{\text{in-RF}}$ < -20 dBm: square law region [94];
- -20 dBm < $P_{\text{in-RF}}$ < 20 dBm: transition region;
- $P_{\text{in-RF}}$ > 20 dBm: linear region which can be used in envelope detectors.

Applications for both detectors include power tracking for PAs [95–97], simple receivers for amplitude modulated signals [98–100] or more complex receiving systems, such as the six-port receivers [101–104]. Thanks to their capability to detect low power, square-law detectors with very good frequency performance can be also used as terahertz detectors for imaging applications.

In this chapter, we will focus on zero-bias detectors, a subfamily of square-law detectors, which are capable of detecting RF signals without any DC biasing voltage. This results in two significant advantages: no need for DC bias network involving bulky chokes as well as the reduction of the flicker noise (also known as 1/f noise) [105].

Another important aspect is the monolithic integrability of detectors with other devices since in many cases they are implemented in systems where, for example, also RF transistors are present. Considering the advantages of MMICs [106] and the continuous development of such technology, having integrable zero-bias detectors can lead to overall system improvements.

4.3 Figures of merit

In this section, a description of the most important figures of merit of square-law detectors is given before discussing state of the art devices (in the next section). Square-law detectors are usually characterized both in DC and in RF. The current curvature (or simply curvature) γ is one of the most important DC parameter and defined by Eq.4.1[107]:

$$\gamma = \frac{\frac{\partial^2 I}{\partial V^2}}{\frac{\partial I}{\partial V}} \tag{4.1}$$

The physical meaning of the current curvature is to describe how well the device can detect the input RF power, thus large values are greatly desired. Another important parameter is the device differential resistance $R_d = (\frac{\partial I}{\partial V})^{-1}$, which also influences the device detection capabilities as it will be shown in the next lines. Both γ and R_d are strongly influenced by the applied bias; however, since the topic of the chapter concerns zero-bias detectors, we will usually refer to their values at 0 V, namely γ_0 and R_{d0}.

The responsivity (or voltage sensitivity) $\beta = \frac{V_{\text{out-DC}}}{P_{\text{in-RF}}}$ of a detector is defined as the DC output voltage $V_{\text{out-DC}}$ over the input RF power $P_{\text{in-RF}}$, besides it can be estimated from the DC figures of merit or from the RF measurements (the setup will be later described). Considering values of R_{d0} up to few kΩ, the responsivity is equal to $\beta = 0.5 R_{d0} \gamma (1 - |\Gamma|^2)$, where $\Gamma = \frac{R_{d0} - R_{so}}{R_{d0} + R_{so}}$ is the reflection coefficient and R_{so} is the resistance of the source (signal generator or antenna, in both cases usually 50 Ω). The term in parentheses is always smaller than 1 (so it reduces the responsivity) and takes into account the amount of power reflected back to the source. Since R_{d0} is up to few kΩ, a matching network can be used and an optimal responsivity $\beta_{opt} = 0.5 R_{d0} \gamma_0$ can be achieved. For $R_{d0} \gg R_{so}$, usual matching networks become complex, narrowband and lossy and the maximum responsivity is equal to $0.5 R_{so} \gamma_0$ [108].

In real detectors, a noise voltage is present in addition to the desired DC voltage at the output of the device. The major noise contributions are thermal (or Johnson), flicker and shoot; however, since we are considering zero-bias detectors, the last two can be neglected. The thermal noise voltage (V_{Jn}) at the output has an effective value of $\sqrt{4 k_B T \Delta f R_{d0}}$, where Δf is the input bandwidth (in the case of no input filter or matching network, Δf includes all the frequency from DC up to the maximum frequency at which the device can operate). The thermal noise voltage can be seen as the voltage detected for a noise power at the input of the device equals to $P_{\text{in-Jn}} = \frac{V_{Jn}}{\beta}$, which can be normalized with respect to $\sqrt{\Delta f}$ obtaining a quantity known as noise equivalent power $NEP = \beta^{-1} \sqrt{4 k_B T R_{d0}}$.

R_{d0} has a strong effect on both responsivity and NEP. Fig. 4.2a shows the influence of the differential resistance (where 3 kΩ is the upper limit that we set to be able to perform a

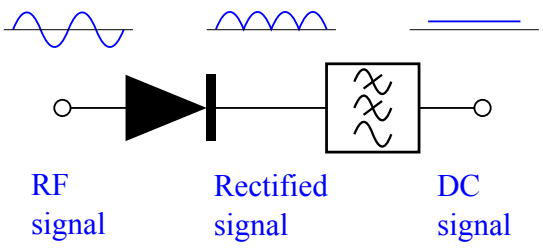
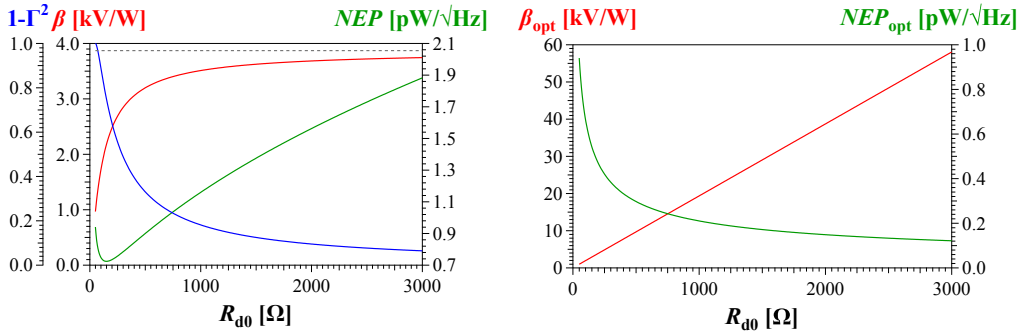


Figure 4.1 – A simplified schematic for RF power detection by using a diode.



(a) Detection performance for unmatched detectors.

(b) Detection performance for matched detectors.

Figure 4.2 – (a) Responsivity and NEP versus R_{d0} for an unmatched detector with a curvature of 38.7 V^{-1} at 0 V, together with the correction coefficient $1-\Gamma^2$ which takes into account the amount of power going through the device. (b) The same parameters are reported in the case of a matched detector ($\Gamma^2 = 0$ thanks to an impedance matching network between the source and the device).

good impedance matching) on both parameters using the expressions previously described and assuming a curvature of 38.7 V^{-1} (which is the ideal value for a Schottky diode, more information will be given later in the chapter). The responsivity increases for larger values of R_{d0} up to some hundreds of Ohm, next it saturates due to the decrease of the power effectively going through the device (defined by $1-\Gamma^2$). The noise figure of merit first decreases, reaching a minimum at ~150 Ω, then increases for larger resistance values indicating that a trade-off between responsivity and NEP needs to be found for this solution. In the unmatched case, the highest possible responsivity is equal to 3870 V/W, which is achieved for $R_{d0} \gg R_s$ at the expense of poor noise performance (which is not always a problem).

The situation changes noticeably by using an impedance matching network obtaining the results shown in Fig. 4.2b, where the responsivity linearly increases with R_{d0} reaching values more than 10X larger than in the unmatched cases. Furthermore, also NEP improves with larger resistance values and limitations only come from the maximum impedance that can be matched (usually few kΩ). The drawback of such solution is the impedance matching itself since the design requires a trade-off between complexity (which usually influences the chip area required for the implementation), the bandwidth and residual reflection coefficient. In other words, the improved detection performance will cost in either a larger area or a reduced working bandwidth.

RF characterization usually involves measurements of the responsivity and the S-parameter of devices. The first consists of supplying an RF signal and measuring the DC output voltage when either the power or the frequency of the RF input signal are swept. Such measurements allow extracting the responsivity as well as the dynamic range (from the input power sweep measurement). The latter indicates the input power range in which the device works as a square-law detector. This value can be obtained by plotting together the measured $V_{out\text{-}DC}$ (in dBmV)

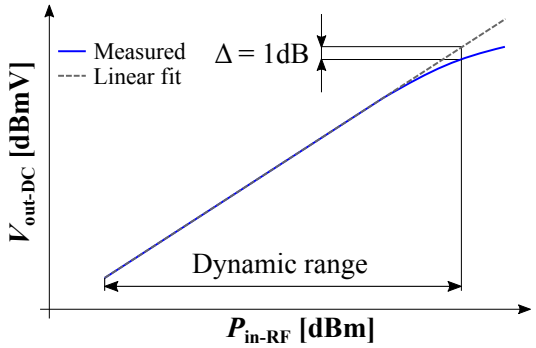


Figure 4.3 – Measured (solid line) output DC voltage (in dBmV) versus RF input power (in dBm) for a generic square-law detector. The coefficients for the linear fit are extracted in the linear region and the 1-dB compression point identifies the input power at which the difference between the fit and the measured voltage is equal to 1 dB. The difference between this point and the minimum detectable power determines the dynamic range.

versus $P_{\text{in-RF}}$ (in dBm) and the "ideal" one obtained by extracting the linear coefficients from the linear region of the measured one (Fig. 4.3). The input power at which the difference between the "ideal" linear plot and the measured one becomes equal to 1 dB defines the 1-dB compression point, so the dynamic range of the device. Usual square-law detectors have a dynamic range of at least 30 dB, which implies that they can detect signal down to - 50 dBm (10 nW), considering that they work with input power lower than -20 dBm.

S-parameter measurements allow obtaining the value of the parameters of the device equivalent circuit, which are used to calculate both NEP and the cut-off frequency (f_c). From the RF point of view, the device can be designed as a single port or dual port device. In the former case, the anode of the device is connected to the signal connector of a vector network analyzer (VNA) port and the cathode is connected to ground, besides the device can be fully characterized by only measuring S_{11}. In the dual port case, the cathode and the anode of the DUT are connected to the signal of two ports of a VNA, thus the device does not have any reference to GND. In this case, all the four S-parameters can be measured to characterize the device fully; furthermore, the linear operation of the device (essential for a correct measurement and parameter extraction) can be confirmed by checking that $S_{xx} \simeq S_{yy}$ and $S_{xy} \simeq S_{xy}$ (with x and y equal to 1 and 2).

Considering that most of the square-law detectors can be seen as diodes, the equivalent circuit is the one reported in Fig. 4.4, with:

- R_s is called series resistance and takes into account both the access and contact resistance;
- R_j is the junction resistance;
- C_j is the junction capacitance.

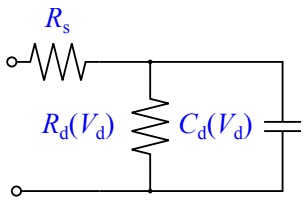


Figure 4.4 – Equivalent circuit of a square-law detector based on a diode.

Both R_j and C_j depends on the bias voltage or the input power, while R_s can be considered almost constant. The expression of NEP can now be improved by replacing R_{d0} with the device resistance generating thermal noise and using the value of β obtained from responsivity measurements, hence obtaining $NEP = \beta^{-1}\sqrt{4k_B T(R_j + R_s)}$.

The cut-off frequency is defined as the frequency at which half of the power is dissipated on R_s and half on R_j. The expression of f_c can be obtained by calculating the voltage drop on R_j as function of the input voltage v_{in}:

$$v_{R_j} = \frac{v_{in}}{Rs + R_j//(i\omega C_j)} R_j//(i\omega C_j) \quad \text{where} \quad R_j//(i\omega C_j) = \frac{R_j}{1 + i\omega R_j C_j} \tag{4.2}$$

Then, the ratio $\frac{v_{R_j}}{v_{in}}$ is equal to:

$$\frac{v_{R_j}}{v_{in}} = \frac{1}{(1 + \frac{R_s}{R_j}) + i\omega C_j R_s} \tag{4.3}$$

Consecutively, we can define the power ratio and set it to 0.5 to extract f_c:

$$\frac{P_{R_j}}{P_{in}} = \left|\frac{v_{R_j}}{v_{in}}\right|^2 = \frac{1}{(1 + \frac{R_s}{R_j})^2 + (2\pi f_c C_j R_s)^2} = \frac{1}{2} \tag{4.4}$$

Usually the junction resistance (especially at low bias or low input power) is much larger than the series resistance, so Eq. 4.4 can be reduced to Eq. 4.5 and a simple expression of f_c can be obtained:

$$\frac{P_{R_j}}{P_{in}} \approx \frac{1}{1 + (2\pi f_c C_j R_s)^2} = \frac{1}{2} \Rightarrow f_c = \frac{1}{2\pi C_j R_s} \tag{4.5}$$

Eq.4.5 suggests that the frequency performance can be improved either by reducing the junction capacitance or the series resistance. For the latter, this is usually achieved by improving the ohmic contact or reducing the access region resistance.

In conclusion, good zero-bias detectors should have large as well as broadband responsivity and

small NEP, together with a wide dynamic range and high cutoff frequency.

4.4 State of the art of solid state zero-bias RF detectors

Zero-bias RF rectifiers have been demonstrated based on several materials, principles and geometries. The first devices relied on intensively optimized Schottky contacts on n/n$^+$ GaAs epitaxial structures [109, 110], showing good frequency response up to 170 GHz with large responsivity up to about 3900 V/W. Exceptional performance has been achieved with tunnel junctions resulting in β up to about 5000 V/W and an estimated f_c of 805 GHz [111–113]. However, these devices require customized epitaxial structures that are not compatible with that of any other semiconductor-based RF device.

2D materials offer an approach for integration with other devices since they can be transferred on several substrates. Device structures based on graphene [114, 115] have been demonstrated with β up to 200 V/W. Excellent performance has been recently reached in MoS_2 Schottky diodes [116]; however, with a limited frequency response up to 10 GHz due to the low electron mobility of MoS_2 layers.

Device integration can also be achieved by transferring bottom-up grown III-V NWs. Pitanti et al. [117] and Vitiello et al. [118] have demonstrated diode and transistor-based detectors, respectively, by transferring InAs-based NWs on high-resistive Si substrates. Vitiello et al. [118] reported excellent frequency performance, with RF detection at 293 GHz with a bow-tie antenna connected to a NW-based transistor, nonetheless, requiring biasing to both gate and drain to maximize its responsivity, which was still low at 1V/W (this value needs to be taken with care since it represents the total system responsivity as it also accounts for the antenna coupling and radiation losses).

Self-switching devices (SSDs) are another option for zero-bias rectifiers, which can be widely implemented on a large range of materials and epitaxial structures [119]. These devices are based on a simple top-down NW fabrication, fully compatible with HEMT based devices, and have shown very good frequency response up to 300 GHz but with a relatively small β up to 200 V/W[120–123].

Field-effect rectifiers (FERs) are an alternative to SSDs, being both based on HEMTs, and they were first proposed as low-V_{on} power diodes [124, 125], then as zero-bias RF detectors [105, 126, 127] and mixer [128]. The measured responsivity for these devices is in the other of thousands of V/W, thus much larger than the values for SSDs, yet with frequency performances limited to a few GHz.

4.5 Field-effect rectifiers

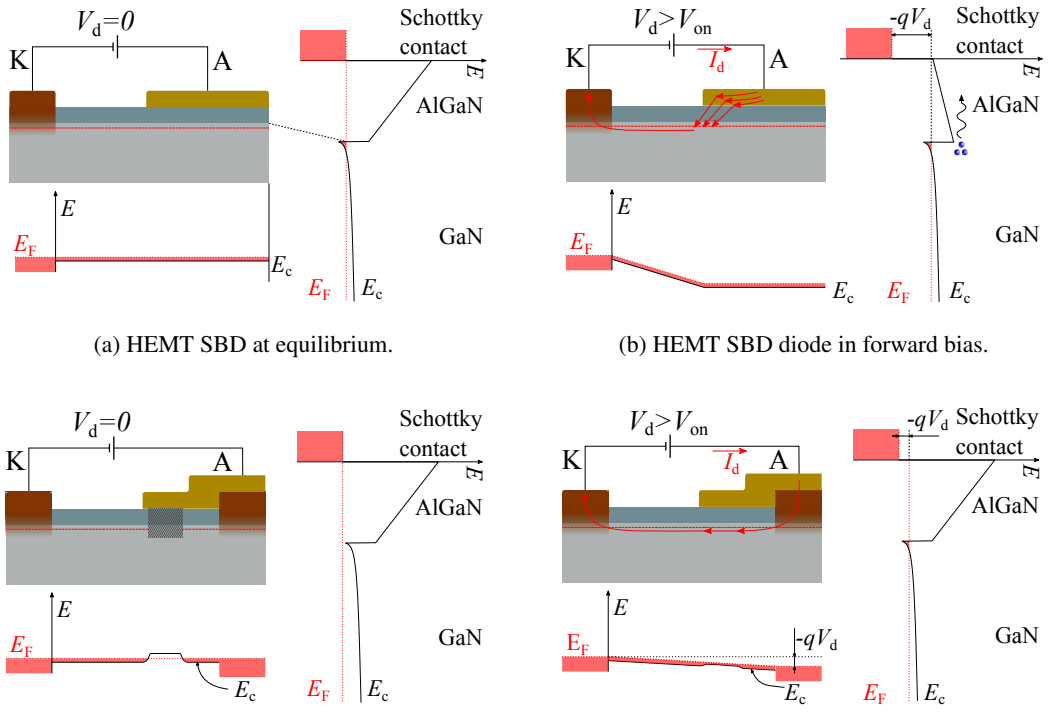
4.5.1 Field-effect rectifiers and Schottky diodes

Schottky barrier diodes (SBDs) and field-effect rectifiers are two different device topologies allowing the fabrication of a rectifier by using almost any HEMT structure. The formation of a Schottky junction is the most known method to achieve rectification in a HEMT; in particular, the anode is formed by depositing a high work function (larger than the electron affinity of the used semiconductor) metal while the cathode requires an ohmic contact (Fig. 4.5a). If the applied voltage $V_d = V_A - V_K$ is smaller than the turn-on voltage V_{on}, then no current flows due to the potential barrier of the Schottky junction. On the other hand, for $V_d > V_{on}$ the barrier is lowered and electrons, coming from the cathode, can flow from the 2DEG to the anode contact through the barrier (Fig. 4.5b) [129].

FERs are actually a quite well know concept in CMOS technology since it is possible to fabricate a diode by simply connecting the drain with the gate (such connection scheme is also known as diode configuration of a transistor). This connection can also be realized for a HEMT-based transistor; however, since the channel is already present at equilibrium, a normally-off technique needs to be used under the gate to remove the 2DEG (stripe region in Fig.4.5c). Later, we will focus on how to achieve the normally-off behavior and the impact of the channel V_{th} on the reverse current I_r. For $V_d < V_{on}$, the current cannot flow between the two ohmic contacts because the 2DEG channel is interrupted in the normally-off region. In the case of $V_d > V_{on}$, the 2DEG is restored and the current flows only in the channel between the two ohmic contacts (Fig. 4.5d). For a further increase of V_d and in the absence of any dielectric material between the gate and the barrier, the Schottky barrier is reduced (for which we can define a $V_{on\text{-}Sb}$) and the current starts to flow also through the gate (as in a conventional Schottky diode). For GaN HEMTs, usual values of $V_{on\text{-}Sb}$ are in the range 1.5 V - 2 V, while FER V_{on} is in the range of few hundreds of mV, implying that for $V_{on} < V_d < V_{on\text{-}Sb}$ (usual working range) the current only flows through the 2DEG channel and not trough the barrier as for Schottky diode. This is one of the most essential differences between Schottky diodes and FERs based on HEMTs.

4.5.2 Effect of V_{th} on V_{on} and I_r for field-effect rectifiers

The main reason for developing FERs for III-Nitride HEMTs was to reduced V_{on} of Schottky diodes since this translates in better efficiency in power circuits [124, 125]. The advantage of FERs is an easier control of V_{on} which can be reduced to values close to 0 V by adjusting the threshold voltage of the channel. In first approximation $V_{th} \sim= -qn_s/C_g$ (where C_g is the gate capacitance), thus V_{th} can be tailored by modifying the carrier concentration (if we consider the same C_g). The effect of V_{th} on both the turn-on voltage and reverse current can be estimated by following the same procedure shown by Westlund [108] for SSDs. The current flowing in a HEMT in the sub-threshold regime (which is the one of interest to determine both V_{on} and I_r)



(a) HEMT SBD at equilibrium.

(b) HEMT SBD diode in forward bias.

(c) FER at equilibrium.

(d) FER in forward bias.

Figure 4.5 – (a) and (b) Band diagram of a Schottky diode at equilibrium and in forward bias, respectively. Current flows when the Schottky barrier is lowered enough ($V_d > V_{on}$) to allow electrons to move from the 2DEG to the Schottky contact. (c) and (d) Band diagram of a FER at equilibrium and in forward bias, respectively. Current flows when the "gate" voltage (equal to the applied bias) is large enough to restore the 2DEG in the normally-off region, so electrons can move from the cathode to the anode ohmic contact.

can be assumed similar to the one for MOSFETs (Eq. 4.6).

$$I_d^{\text{sub-th}} = I_s \exp\left(\frac{V_{gs} - V_{th}}{n V_t}\right)\left[1 - \exp\left(-\frac{V_{ds}}{V_t}\right)\right] \tag{4.6}$$

V_t is the thermal voltage ($k_B T/q$) while the quantity n represents the ideality of the field control with $n = 1$ being the ideal case and $n > 1$ indicating a poorer control. Considering that gate and drain are connected together ($V_{gs} = V_{ds} = V_d$, with V_d the applied diode voltage), and supposing an ideal gate control, the sub-threshold current in the diode can be defined as:

$$I_d^{\text{sub-th}} = I_s \left[\exp\left(\frac{V_d - V_{th}}{V_t}\right) - \exp\left(-\frac{V_{th}}{V_t}\right)\right] \tag{4.7}$$

By setting $I_s^{FER} = I_s \exp\left(-\frac{V_{th}}{V_t}\right)$, Eq. 4.7 can be rewritten as:

$$I_d^{sub\text{-}th} = I_s \exp\left(-\frac{V_{th}}{V_t}\right)\left[\exp\left(\frac{V_d}{V_t}\right) - 1\right] = I_s^{FER}\left[\exp\left(\frac{V_d}{V_t}\right) - 1\right] \tag{4.8}$$

For $V_a \ll V_{th}$ (reverse bias), Eq. 4.8 reduces to $-I_s^{FER} = -I_s \exp\left(-\frac{V_{th}}{V_t}\right)$, which is the reverse current. If V_{th} is negative (normally-on channel), the exponent is positive and large resulting in a OFF current in the same order of the ON one and constant with respect to the applied bias, that is to say that the diode is never switched off. On the other hand, for positive value of V_{th} (normally-off channel), the argument of the exponent is negative and the reverse current sharply decreases for larger values of V_{th}. Despite the small I_r, large and positive values of V_{th} yield an increase of V_{on}, considering that the current is proportional to $\exp\left(-\frac{V_{th}}{V_t}\right)$. For zero-bias detectors, both low V_{on} and strong control of I_r are required, so the techniques used for controlling V_{th} has a relevant impact on the device detection capabilities.

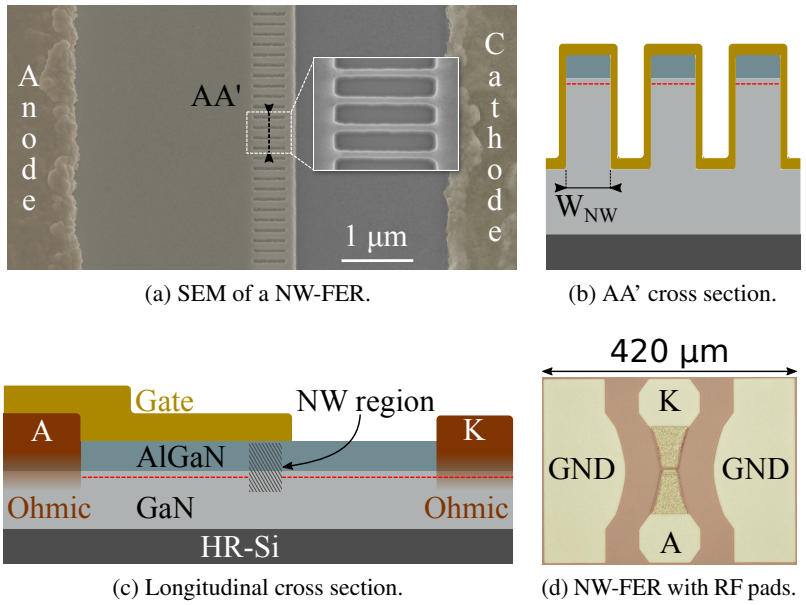
4.5.3 Comparison of curvature

The maximum curvature at zero bias for a FER can be calculated by using Eq. 4.7 in Eq. 4.1 resulting in $V_t^{-1} = \frac{q}{k_b T}$; in particular, at room temperature (300 K) $\gamma_{0\text{-max}}$ is equal to 38.7 V^{-1}. This is the maximum value achievable in any FER independently from geometry, material, and fabrication process.

Considering a Schottky diode with a current $I_d = I_s\left[\exp\left(\frac{qV_d}{\eta k_b T}\right) - 1\right]$, where η is the ideality factor of the diode ($\eta \geq 1$ and $\eta = 1$ means ideal diode), $\gamma_{0\text{-max}}$ is equal to $\frac{q}{\eta k_b T}$. This expression is similar to the FER one; in particular, a field-effect rectifier with γ_0 equals to γ_{0max} can be considered as an ideal Schottky diode.

The reported maximum value of curvature can be exceeded only by using physical effects different from electric field control (for FERs and SSDs) or Schottky barrier modulation. Backward tunneling diodes are an example, indeed the reported maximum curvature can be as large as 58 V^{-1} [130]; however, a strongly optimized epi-structure is used which cannot be used for the fabrication of any other semiconductor device.

Despite the existence of reports with γ_0 exceeding 38.7 V^{-1} in FERs [127, 131], the authors did not provide any explanation for such values; furthermore, the characterization of the devices is not complete (e.g. frequency measurements are missing). Since γ_0 is extracted by performing twice the numerical derivative on the measured diode current versus the applied bias, sources of errors might be an insufficient amount of points or a wrong measurement setup.



(a) SEM of a NW-FER.

(b) AA' cross section.

(c) Longitudinal cross section.

(d) NW-FER with RF pads.

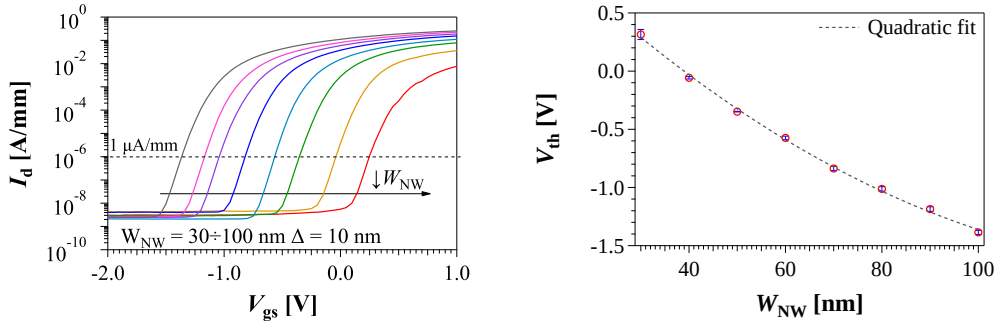
Figure 4.6 – (a) False colored SEM image of a NW-FER based on 45 nm-wide NWs. (b) Schematic of the AA' cross-section. (c) Schematic of the longitudinal cross-section, from anode (A) to cathode (K), of a NW-FER. (d) Picture of a NW-FER in the dual port configuration for RF measurements.

4.6 Nanowire Field-Effect Rectifiers (NW-FERs): device concept

The channel threshold voltage strongly impacts the detection performance of FERs, so the technology used to tune such parameter plays a key role. For III-Nitride HEMTs, the fluorine treatment was firstly used for this purpose [105, 124–126], which consisted of performing a fluorine-based plasma to implant negative ions into the barrier to deplete the 2DEG. The reduction of the barrier (known as barrier recess) can also be used to control V_{th} [127] since it drops the polarization electric field in the barrier which generates the 2DEG, yielding a reduced carrier density [132].

The etching of NWs from normally-on HEMT structures is another technique to change the carrier concentration, thus V_{th}, into the NWs [31, 133, 134]. We use such technique in FERs demonstrating for the first time nanowire based field-effect rectifiers (Fig. 4.6a to 4.6d), showing better performance than planar (or lateral) FERs (shortly L-FERs) both in curvature, so responsivity, and frequency. This result is also achieved because the "gate" of FERs wraps the NWs ensuring a much-improved control than in the planar case, thus better rectification performance.

A standard commercial AlGaN/GaN HEMT on high-resistive Si substrate is used to demonstrate such concept and process flow is described in Appendix A.1. The exact epi-structure of the wafer consists of GaN (2.7 nm)/ AlGaN (25 nm)/GaN (500 nm) followed by a 1.7 μm-thick buffer on high-resistive silicon substrate. The electron mobility (μ_e), carrier concentration (n_s) and sheet



(a) Transfer curves of Schottky tri-gate transistors.

(b) Threshold voltage versus NW width.

Figure 4.7 – (a) Transfer characteristics in logarithmic scale of Schottky tri-gate transistors with NW width from 30 nm to 100 nm. (b) Extracted V_{th} (at 1 μA/mm) versus NW width, together with a quadratic fit.

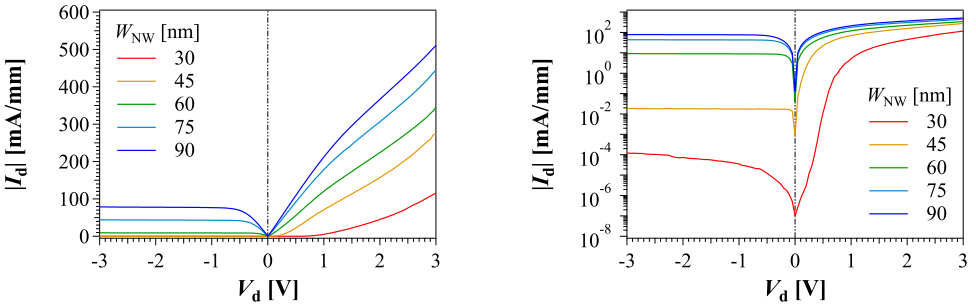
resistance (R_{sh}) of the epitaxial structure measured at 300 K were 1917 cm^2/Vs, 1.06×10^{13}cm^{-2} and 300 Ω/□, respectively.

The influence of the NW width (W_{NW}) on the threshold voltage is investigated by fabricating Schottky tri-gate transistors on the same wafer with W_{NW} varying from 30 nm to 100 nm. Transfer characteristics are shown in Fig. 4.7a and in Fig. 4.7b we report V_{th}, extracted at 1 μA/mm, versus W_{NW} including error bars. The threshold voltage reduces from about -1.4 V (normally-on) for 100 nm-wide NWs to 0.3 V (normally-off) for 30 nm with a quadratic dependence. The influence of the NW width on the threshold voltage, also shown by Jun et al. [135], is produced by the sidewall depletion of carriers [136], strain relaxation of the barrier layer in narrow NWs [31] and the enhanced gate control from the tri-gate structures [30]. Fig. 4.7b shows that the use of top-down NWs is a very precise method to properly tune the channel V_{th}, besides also ensuring a very good reproducibility as highlighted by the very small error bars.

4.7 DC characterization of NW-FERs

We fabricated NW-FERs composed of 240 NWs with length of 500 nm and widths (W_{NW}) varying from 30 nm to 90 nm with a constant NW spacing of 100 nm. This is equivalent to varying the NW filling factor from 23% to 47%. The device current was normalized by the width of the entire device footprint (not by the NW width).

Fig. 4.8a shows the absolute value of the diode current versus bias voltage for all NW-FERs. The increase of the NW width from 30 nm to 90 nm produces a larger ON current, a smaller turn-on voltage and a worsening of the current blocking capabilities. For almost all devices, a change of slope is present in the forward IV, which is related to the turn-on of the Schottky barrier. Since there is no oxide between the "gate" and the barrier of the HEMT, large values of voltage on



(a) Linear plot of IV curves of NW-FERs.

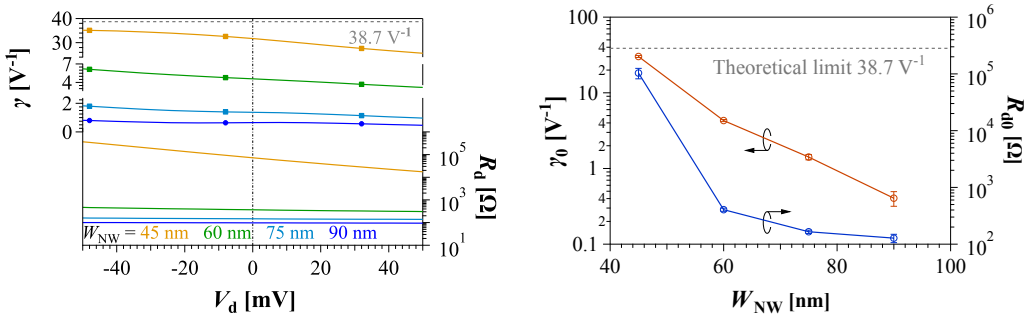
(b) Logarithmic plot of IV curves of NW-FERs.

Figure 4.8 – (a) and (b) Linear and logarithmic plots of the absolute current versus applied bias in NW-FERs with NW widths from 30 nm to 90 nm.

the anode terminal are able to reduce the Schottky barrier height, resulting in a current which becomes comparable to the one flowing into the 2DEG. Fig. 4.8b better illustrates the blocking capabilities of NW-FERs as well as the sub-threshold behavior. The reverse current augments by six orders of magnitude when increasing the NW width, as expected from the used model defined by Eq. 4.7 and the dependence of the threshold voltage on the NW width. Devices with W_{NW} between 60 nm and 90 nm have a negative V_{th} (Fig. 4.7b), thus the term $-I_s \exp\left(-\frac{V_{th}}{V_t}\right)$ in Eq. 4.7 is very large, yielding a reverse current which is independent of the applied bias and in the same order of the ON current. 45 nm-wide NW-FERs have a channel threshold voltage around 0 V, thus the reverse current is in the order of I_s. Finally, for 30-nm wide NW-FERs the exponential term becomes very small ($\sim 10^{-5}$) because the channel threshold voltage is positive and much larger than V_t . By defining the diode turn-on voltage at 10 mA/mm (usually 1 mA/mm is a more common value; however, this would not allow extracting V_{on} for the 45 nm-wide NW-FERs, which still show good blocking capabilities with an ON/OFF ratio larger than 10^3), 30 nm-wide NW-FERs have a V_{on} of ~0.55 V while it reduces to almost 0 V for 45 nm-wide NW-FERs.

Fig. 4.9a shows the calculated values of curvature and differential resistance from IV curves Because of the numerical differentiation and errors from measurements (e.g. measurement autorange, offset, integration time), it is very important to use a large number of points, together with a long integration constant and a measurement delay (0.16 s and 0.1 s are set, respectively), due to the low current level, to obtain reasonable values of curvature (wrong setup can lead to an overestimation with values larger than the theoretical limit). 30 nm-wide NW-FERs have a large V_{on}, thus the characterization as zero-bias detectors, which includes also the estimation of γ and R_d, is not reported.

Both the curvature and the diode resistance are almost constant with respect to the applied bias for large NW-based devices, while they change substantially for the 45 nm-wide NW-FERs, which is the signature of much better blocking capabilities. Such difference is better shown in Fig. 4.9b, where the value of γ and R_d are taken at zero bias and plotted versus NW widths.



(a) γ and R_{d} versus V_{d}.

(b) γ_0 and R_{d0} versus W_{NW}.

Figure 4.9 – (a) Curvature and differential resistance of NW-FERs versus applied bias for different NW widths. (b) Curvature and differential resistance at 0 V versus NW width.

The curvature reaches 30.1 V^{-1} for the 45-nm wide NW-FERs and quickly decreases to 0.4 V^{-1} for the 90 nm-wide NW-FERs. The variation of R_{d0} is even more drastic, with a difference of three orders of magnitude. The strong dependence of both parameters with respect to the NW width is related to the variation of channel threshold voltage, which determines the working point of the devices. The model previously described in this chapter refers for FERs working in the sub-threshold region; in particular, this can be achieved if V_{th} is close to 0 since the "applied bias" is 0 V. Devices with negative V_{th} values, instead, work in the triode-region of the transistor where the current can be modeled as [108]:

$$I_{\mathrm{d}} = \kappa \left(\frac{V_d}{2} - V_{\mathrm{th}} \right) V_d \tag{4.9}$$

κ is a constant which is proportional to the transconductance of the transistor used to realize a FER with its drain and gate contacts disconnected. The curvature can be obtained by inserting Eq. 4.9 in Eq. 4.1 resulting in V_{th}^{-1}. The transition between FERs working in the triode and sub-threshold region is not abrupt; however, if we set a V_{th} of about -0.25 V as limit for the triode region, the maximum γ_0 achievable in this region is ~4 V^{-1}, which is about ten times smaller than the value achievable in sub-threshold. When the NW width decreases from 90 nm to 45 nm, FER operating points move from the triode region to the sub-threshold region yielding a strong improvement of the curvature. On the other hand, also the resistance increases and this negatively affects the noise performance, whose analysis will be conducted later in the chapter.

4.8 RF characterization of NW-FERs

The RF characterization of NW-FERs involves the measurement of the responsivity and the S-parameters of devices.

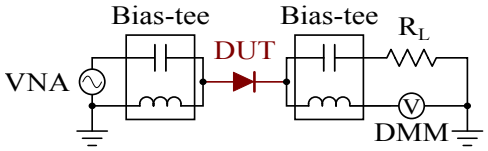


Figure 4.10 – Setup for measuring the responsivity of NW-FER involving a VNA as signal source and a digital multimeter to measure the DC output voltage.

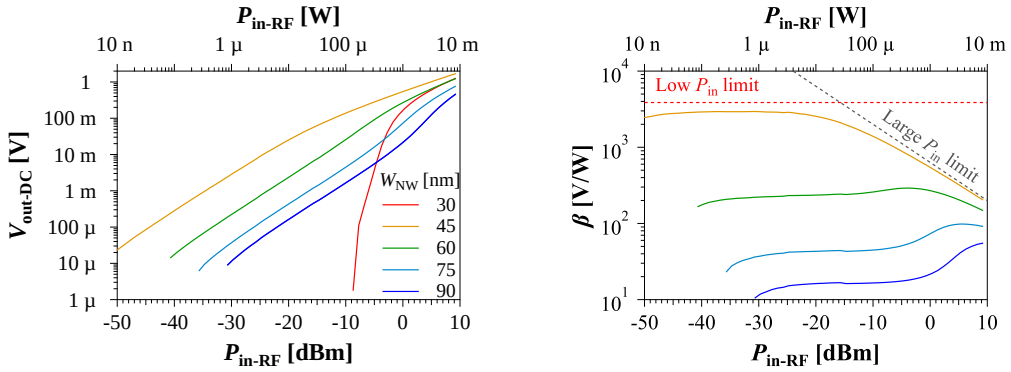
4.8.1 Responsivity measurement

The setup to measure the responsivity is shown in Fig. 4.10, where a VNA is used to supply an RF signal to the anode and a digital multimeter (DMM) to read the output DC voltage from the cathode. For the connections, two bias-tees are used because of the dual-port pad configuration. The losses between the VNA and the device under test due to interconnections are calibrated by performing a S-parameter measurement on a "thru"; in particular, the power at the input of the device can be calculated as $P_{\text{in-RF}} = P_{\text{VNA}} + S_{21}^{\text{cable}}/2$ (power values in dBm and S_{21}^{cable} in dB) . Since cables are lossy, S_{21}^{cable} is negative and the power at the device input is smaller; moreover, the measured value is divided by two because it refers to two cables, whereas only one is used in the responsivity measurement. A power sensor was also used to validate the performed calibration.

V_{out} has a linear behavior for a large range of P_{in}, in agreement with the “square-law” of diodes ($V_{\text{out}} \propto V_{\text{in}}^2 \propto P_{\text{in}}$) [94]. At larger P_{in} the impedance of diodes starts to depend on P_{in} causing the sub-linear behavior observable in Fig. 4.11a [94]. The minimum detectable power generating a stable V_{out} was -50 dBm for 45 nm-wide NW-FERs, which was degraded for wider NWs devices. The dynamic range was about 30 dBm (calculated from the 1 dB compression point) independently from the NW widths.

Fig. 4.11b shows $\beta = V_{\text{out}}/P_{\text{in}}$ for all devices versus P_{in}, revealing a significant increase of up to 2 orders of magnitude for narrow NW FERs, which is a consequence of the much larger γ_0 (Fig. 4.9b). The 45 nm-wide NW-FERs present a maximum β of 3000 V/W, which is very close to the theoretical value of $2R_{\text{so}}\gamma_0 = 3010\ \text{V}^{-1}$, defined in the case of complete mismatch between the device impedance (~ 100 kΩ) and the source impedance R_{so} (50 Ω of the VNA port) [108]. The responsivity approaches the maximum responsivity achievable in unmatched FERs ($2R_{\text{so}}\gamma_0^{\text{max}} =$ 3870 V/W) at low power and the theoretical value of $2\sqrt{2Z_0/P_{\text{in}}}$ at large power, which considers a capacitive load connected to an ideal diode in off-state ($I_{\text{r}} = 0$ A), for which the entire reflected power causes the doubling of input voltage.

Fig. 4.12 shows the measured frequency response of β at P_{in} = -20 dBm (square law region for all devices) for a large frequency range, up to 50 GHz. The 45 nm-wide NW FERs is characterized by a large and flat β over almost the entire measured range, which corresponds to an improved frequency performance compared to other lateral FERs [105, 126, 128] together with a very good



(a) $V_{\text{out-DC}}$ versus $P_{\text{in-RF}}$ at 1 GHz.

(b) β versus $P_{\text{in-RF}}$ at 1 GHz.

Figure 4.11 – (a) Output DC voltage versus input RF power at 1 GHz for NW-FERs with widths from 30 nm to 90 nm with no bias voltage. (b) Responsivity versus input RF power at 1 GHz. The measurement for the 30 nm-wide NW-FERs is not reported since the device does not work as zero-bias detector.

responsivity. The oscillations seen in Fig. 4.12 are due to impedance mismatches between the devices and the VNA.

4.8.2 S-parameter measurement

The frequency behavior of 45-nm wide NW-FERs, which are the most promising devices, is also characterized by performing the measurements of the four S-parameters (further details about the measurement procedure are shown in Appendix B.3). In Fig. 4.13 we report only S_{11} and S_{21} since S_{22} and S_{12} are respectively identical, hence satisfying the conditions $S_{xx} \simeq S_{yy}$ and $S_{xy} \simeq S_{xy}$ required to neglect any non-linear effect of the device. This allows using the model previously introduced in the chapter (Fig. 4.4), for which the component values were extracted

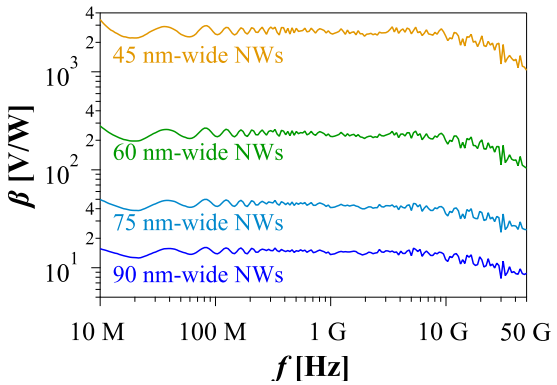


Figure 4.12 – Responsivity versus the frequency of the input signal with a power of -20 dBm.

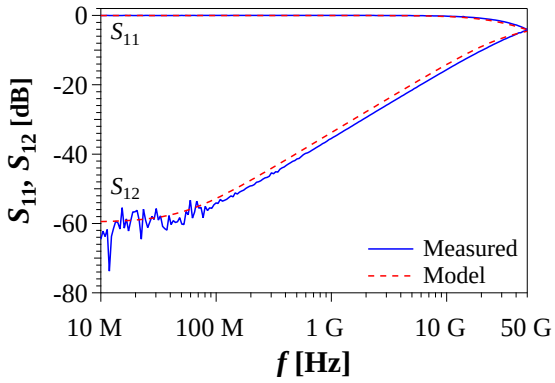


Figure 4.13 – Measured (solid) and simulated (dashed) S_{11} and S_{12} versus input signal frequency at -20 dBm.

from the measured S-parameters yielding in R_s of 37.9 ±1.6 Ω, R_j of 101 ±17.5 kΩ (similar to the DC $R_d = R_s + R_j \sim R_j$ since $R_j \gg R_s$) and C_j of 30.6 ±1.7 fF.

The simulation of the S-parameters based on the model is performed using the Advanced Design System (ADS) simulation software and the results are reported in Fig. 4.13, which show a very good agreement between the experimental and simulated results.

The model parameters also allow determining the cut-off frequency (Eq. 4.5) which is equal to 140 GHz. Such value can be significantly improved by reducing R_s and C_j with an optimized geometry, smaller anode and cathode access regions and reduced contact resistances (e.g. by using regrowth contact such resistance can drop from 0.7 Ωmm down to 0.23 Ωmm [137]).

Finally, the noise equivalent power was calculated $\sqrt{4k_B T R_s + R_j}/\beta$ yielding a value of 18.7 ± 2.3 pW/$\sqrt{\text{Hz}}$, which is slightly larger than recommended values (less than 10 pW/$\sqrt{\text{Hz}}$). To reduce the value of NEP, the device resistance $R_{d0} \sim R_s + R_j \sim R_j$ needs to be reduced. A first approach involves the scaling up of devices which translates in a larger number of NWs, indeed NEP reduces from 27 pW/$\sqrt{\text{Hz}}$ to 18.7 pW/$\sqrt{\text{Hz}}$ when increasing the number of NW from 120 to 240. The second solution requires the increase of the reverse current by tuning V_{th}, so the NW width. R_{d0} can be derived from the expression of current 4.8 as:

$$R_{d0} = \left(\frac{\partial I_d}{\partial V_d}\right)^{-1} = \frac{k_b T}{q I_s^{FER}} = \frac{k_b T}{q I_s \exp(-\frac{V_{th}}{V_t})} \tag{4.10}$$

Smaller values of R_{d0} requires an increase of I_s, which depends on the epistructure (e.g. buffer thickness and doping), or a reduction of V_{th}. While larger values of I_s are desirable for NW-FERs, they may cause issues for other devices, such as RF switches or amplifiers, that might be potentially fabricated together, thus limiting the overall integrability. As a consequence, the

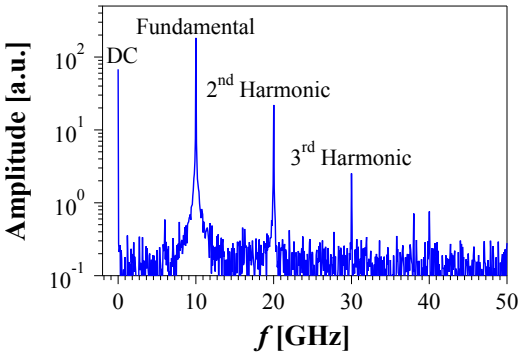


Figure 4.14 – FFT spectrum of the signal at the cathode of a 45 nm-wide NW FER when stimulated by a 10 GHz sine wave with a power of 0 dBm.

tuning of V_{th} is a more suitable solution, thought its exponential influence together with its role in defining the operating region of the device (triode or sub-threshold region, with latter being more favorable) makes the design very difficult. The technology used to adjust the threshold voltage is crucial and we have demonstrated that the design of the width of etched NWs is a meticulous technique ensuring both high control and reproducibility (Fig. 4.7b). Future works should focus on an optimization of the width between 45 nm and 60 nm, which should result in smaller resistance and devices still working in the sub-threshold region (large curvature).

4.9 Other applications: frequency multiplication

The high-frequency capabilities of NW-FERs together with their strong non-linearity are used to demonstrate frequency multiplication in a measurement setup consisting of a VNA and a Keysight UXR1102A Infiniium oscilloscope (110 GHz). The VNA is used to supply the RF signal at the anode of the device while the cathode is connected to the input of the oscilloscope. Then Fast Fourier Transform (FFT) is performed to obtain the output signal spectrum and identify the generated harmonics. Fig 4.14 shows the FFT spectrum of the voltage at the cathode of the device when a 10 GHz 0 dBm input sine wave is supplied at the anode of the 45 nm-wide NW-FER. A strong DC component is observed, confirming the good rectification capabilities of the device, along with intense peaks at 20 GHz and 30 GHz, corresponding to the 2nd and 3rd harmonics, which are only 9 dB and 20 dB smaller than the fundamental, respectively. Therefore these devices could be used as passive frequency multipliers and mixers for a low-power low-noise coherent (de)modulation.

4.10 Chapter conclusion

In conclusion, we demonstrated high-performance zero-bias RF rectifiers based on NW-FERs fabricated on a commercial AlGaN/GaN HEMT. The use of NWs offered a flexible design tool and much-improved rectification capabilities. By adjusting the width of NWs, V_{th} could be properly designed, with very high reproducibility, which resulted in a normally-off channel with low V_{on} (required for zero-bias operation in FERs). The tri-gate structure wrapping the NWs yielded a much better channel control than in planar FERs, resulting in a curvature coefficient of 30.1 V^{-1}, which is close to the theoretical limit of 38.7 V^{-1}. NW-FERs showed a large responsivity of 3000 V/W, as predicted by the used model, with flat frequency response, and a high f_{c} of 140 GHz. Such value can be significantly improved by reducing R_{s} and C_{j} with an optimized geometry and which opens opportunities for high-frequency detectors. The large responsivity reported together with the good frequency response shows that NW-FERs are an excellent alternative to GaN-HEMT-based SSDs and lateral FERs, thus further expanding the device portfolio compatible with GaN MMICs.

5 Conclusion and future directions

In this thesis, we deeply investigated nanowires etched from III-Nitride HEMTs, mainly based on AlGaN/GaN heterostructures, to better understand electron transport at nanoscale and to create new device architectures or improve current ones.

The nature of electron transport was explored by fabricating NW-based crosses, which can filter electrons moving under ballistic regime from those under diffusive one. Ballistic transport was observed at room temperature and under large bias thanks to the high mobility of electrons and the large optical phonon energy in III-Nitrides. Semi-classical and quantum effects have been noticed at cryogenic temperature and under strong magnetic fields. The carrier concentration in NWs and the sidewall depletion width, which are usually challenging to be experimentally measured but very important when designing devices based on NWs, have been extracted using these crosses. Future works would consist of fabricating these mesoscopic devices with different III-Nitride HEMTs (e.g., N-polar HEMTs, quaternary-barrier HEMTs, multi-channel HEMTs, etc.) to analyze both variations of transport behavior and physical parameters.

NWs allow a large variety of gate geometries which can noticeably influence the overall device performance. In particular, we propose side gating for all those devices based on NWs with a width in the order of the barrier thickness. We demonstrated, using transistors with gates on the same plane of the NW channel (called IPGFETs), that side gates can effectively control the 2DEG in NWs yielding extremely large transconductance and subthreshold slope close to 60 mV/dec. In such perspective, we studied in-plane gates made with the HEMT structure itself and metal IPGs, with the latter resulting in much better performance and better scaling capabilities.

Further research is needed to reduced parasitic elements and to optimize the device fabrication process and geometry. A more exotic development of IPGFETs would require the fabrication of BRIDGE FETs with n-GaN replacing the metal gate. Such solution might be particularly useful for devices operating in harsh environments, especially at temperatures of several hundreds of degrees Celsius. GaN is one of the most promising materials for these applications, thanks to the large band gap, and having transistors which use GaN to form both channel and gate would provide a very promising architecture.

Finally, we demonstrated that by using an array of etched NWs, we could noticeably improve the performance of field-effect rectifiers used as RF zero-bias detectors. NWs offer an excellent tool to meticulously design the threshold voltage of the channel, which is a crucial parameter for designing these rectifiers. The tri-gate geometry provides much better control than planar gates, which, together with the optimization of V_{th}, allowed to reach a very high curvature value (resulting in large responsivity with no need for any impedance matching network) combined with a wide frequency operation.

Future work on NW-FERs can be oriented either on the optimization of the fabrication process or on the applications. The combination of NWs with other known techniques used for controlling the carrier concentration in GaN HEMTs, such as p-GaN gate and barrier recess, could yield to larger optimal width for NWs. Commercial RF GaN devices are usually based on 0.15-0.25 μm process; thus, NW widths in this range would facilitate the integration of NW-FERs with other RF devices in MMICs without demanding high-resolution tools (such as e-beam lithography). NW-FERs might be potentially used also for RF energy harvesting; in this case, devices should be optimized to reduce the differential resistance to improve the matching with the antenna. The advantage of using GaN HEMT is that devices would be more electrically robust than those based on other materials, similarly to what discussed in Sec. 1.5.1 about LNAs based on GaN. Frequency multiplication, or more generally frequency mixing, is another important application which we just started to explore in this thesis. The non-linear behavior required for these applications is ensured by NW-FERs without any DC bias, thus strongly improving noise performance. A better and more complete characterization for this application would help to understand if NW-FERs might offer a different architecture to perform such functions. The frequency scaling of NW-FERs will require the use of regrown contacts, reduction of the anode-to-cathode distance, and reduction of parasitic components. Scaled NW-FERs will be able to work in the terahertz range, where a large number of applications demand very sensitive devices as the NW-FERs demonstrated in this thesis.

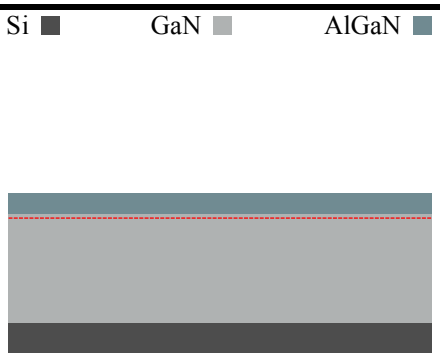
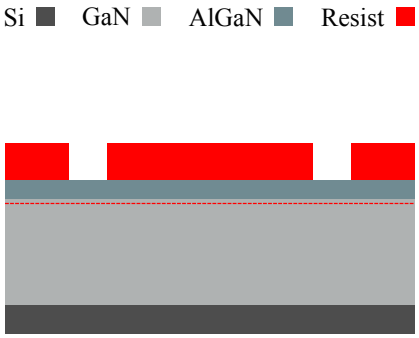
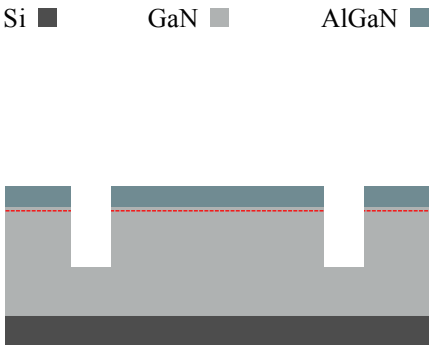
A Fabrication process

The fabrication of the devices presented in this thesis is entirely performed in the clean room facilities of the EPFL, namely the *Center of Micronanotechnology* (CMi) and the *III/V lab* of the Physics department. In this appendix, the fabrication process flow is described together with some important details about e-beam lithography (EBL).

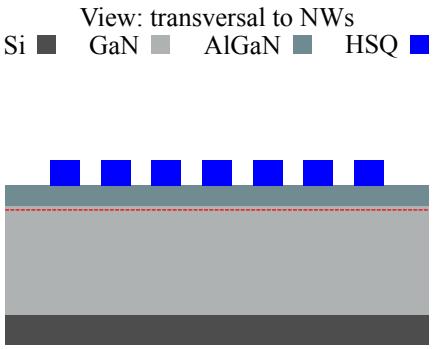
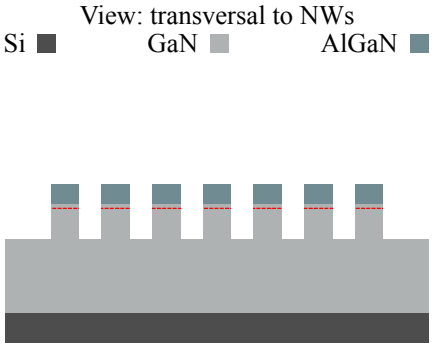
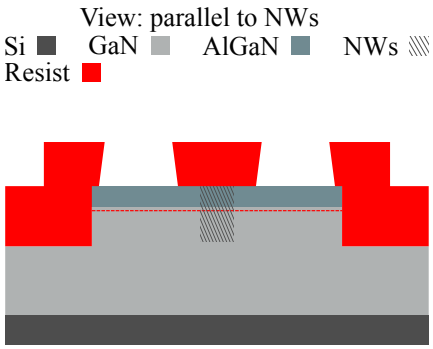
A.1 Process flow

The process flow for the fabrication of the devices reported in this thesis is quite similar for all them, except for some variations such as substrate, presence of gate and pads.

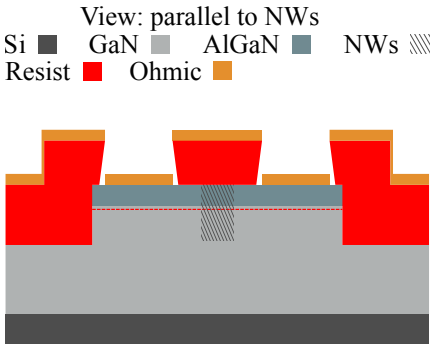
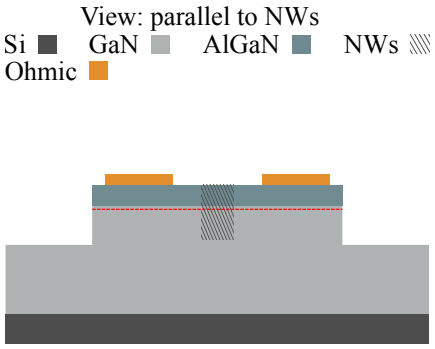
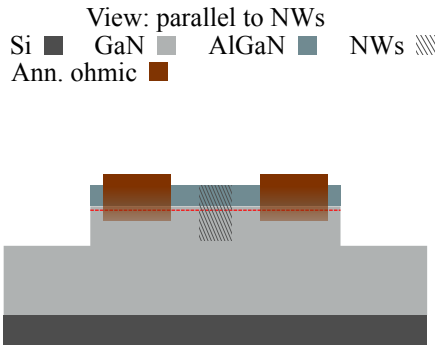
Tab. A.1 describes the process flow for the fabrication of the alignment marks, which consist in 10 μm-large or 20 μm-large etched squares, used for the EBL alignment. The fabrication of EBL alignment mark is required if the process flow presents multiple EBL steps or if different electron beam current values are used for a single step. Concerning the latter and depending on the used tool, the reference position of the e-beam for a certain current value can be quite different from the same for another current value. Such difference is proportional to the difference between the used currents and it causes a shift of the features written with one beam current with respect to those written with another. The alignment procedure allows almost eliminating such shift, which can be as large as hundreds of nm.

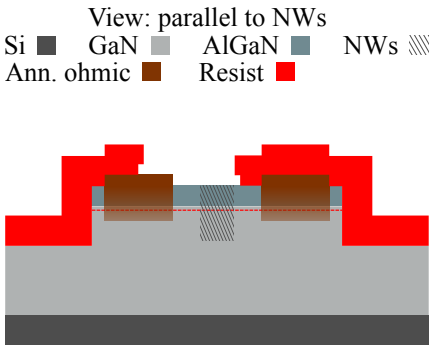
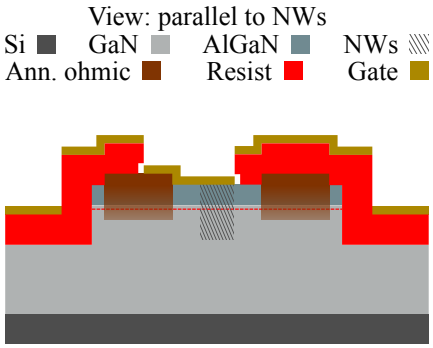
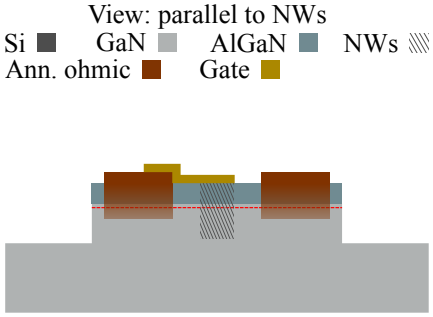
Step	Process description	Cross-section after process
1	Sample cleaning 1.1 SVC-14: MP sonic, 5' 1.2 IPA: MP sonic, 3' 1.3 Drying: N_2 gun	
2	Alignment mark lithography 2.1 Dehydration: 135°C, 5' 2.2 AZ1512 coat: 6 krpm, 30" 2.3 Soft bake: 100°C, 1'30" 2.4 Exposure: MLA150, dose 42 mJ/cm^2, defocus 0 2.5 Development: 2.5.1 Dev.: AZ726, 22"-25" 2.5.2 Rinsing: 2X DI H_2O 2.5.3 Drying: N_2 gun 2.6 O_2 Plasma Descum: Tepla GigaBatch, high power, 30"	
3	Alignment mark etching 9.1 Etching Sentech ICP-RIE 500 9.1.1 Cleaning 1 : O_2, 5' 3.1.2 Cleaning 2: Cl_2/Ar, 5' 3.1.3 Etching: Cl_2/Ar, ~ 600 nm 3.4 Resist stripping: 3.4.1 SVC-14: MP sonic, 5' 3.4.2 IPA: MP sonic, 1' 3.4.3 Drying: N_2 gun 3.5 O_2 Plasma: Tepla GigaBatch, high power, 3'	

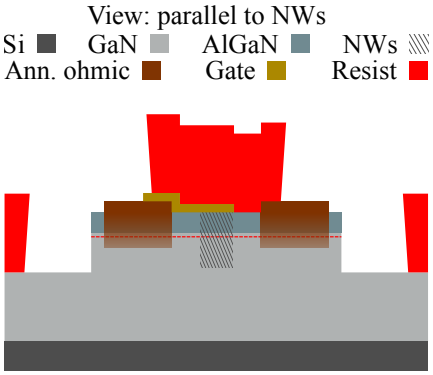
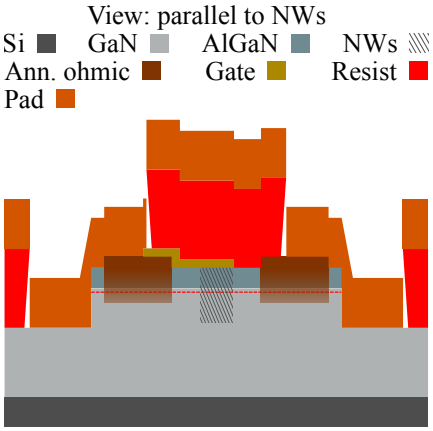
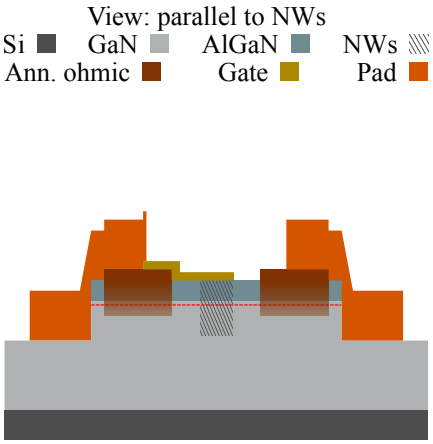
Tab. A.2 shows the process flow for the fabrication of NW-FERs. The process flow for the other devices described in the thesis is usually a shorter version of this, for example the process flow for the fabrication of the electron-filter cross ends at step 6 of Tab. A.2.

Step	Process description	Cross-section after process
1	Mesa and NW e-beam lithography 1.1 O_2 plasma cleaning: Tepla GigaBatch, high power, 1' 1.2 HSQ 2% coat: 3 krpm, 1' 1.3 Exposure: Raith EBPG5000, dose 1650 μJ/cm^2 1.4 Development: 1.4.1 Dev.: TMAH 25%, 2'30" 1.4.2 Rinsing: 2X DI H_2O 1.4.3 Drying: N_2 gun 1.5 O_2 plasma HSQ hardening: Tepla GigaBatch, high power, 2'	
2	Mesa and NW etching 2.1 Etching Sentech ICP-RIE 500 2.1.1 Cleaning 1 : O_2, 5' 2.1.2 Cleaning 2: Cl_2/Ar, 5' 2.1.3 Etching: Cl_2/Ar, ~250 nm 2.2 HSQ removal: 2.2.1 Etching: BOE 7:1 3' 2.2.2 Rinsing: 2X DI H_2O 2.2.3 Drying: N_2 gun	
3	Ohmic contact lithography 3.1 Dehydration: 135°C, 5' 3.2 AZ nLOF 2020 coat: 6 krpm, 30" 3.3 Soft bake: 110°C, 1'15" 3.4 Exposure: MLA150, dose 80 mJ/cm^2, defocus 0 3.5 Post-exposure bake: 110°C, 1'15" 3.6 Development: 3.6.1 Dev.: AZ726, 1' 3.6.2 Rinsing: 2X DI H_2O 3.6.3 Drying: N_2 gun 3.7 O_2 Plasma Descum: Tepla GigaBatch, low power, 30"	

Appendix A. Fabrication process

Step	Process description	Cross-section after process
4	Ohmic contact evaporation 4.1 Evaporation EVA760: 4.1.1 Ti: 5 Å/s, 200 Å 4.1.2 Al: 5 Å/s, 1200 Å 4.1.3 Ti: 5 Å/s, 400 Å 4.1.4 Ni: 5 Å/s, 600 Å 4.1.5 Ti: 5 Å/s, 500 Å	
5	Ohmic contact lift-off 5.1 Lift-off: 5.1.1 PR strip: SVC-14, 70°C, >6 h 5.1.2 Eventual manual metal peeling by tweezers 5.1.3 PR cleaning: SVC-14, LP sonic, 70°C, 3' 5.1.4 Rinsing: IPA, LP sonic, 1' 5.1.4 Drying: N_2 gun	
6	Ohmic contact annealing 7.1 Annealing: RTP AS-ONE, N_2, 780°C, 30"	

Step	Process description	Cross-section after process
7	Gate e-beam lithography 7.1 Dehydratation: 180°C, 5' 7.2 Double PMMA coat: 7.2.1 PMMA 495A8 coating, 7 krpm, 1' 7.2.2 Bake: 180°C, 7'30" 7.2.3PMMA 950A8 coating: 4.5 krpm, 1' 7.2.4 Bake: 180°C, 7'30" 7.3 Espacer coating: 2krpm, 1' 7.4 Exposure: Raith EBPG5000, dose 600 μJ/cm^2 7.5 Espacer removal: 7.5.1 Removal: DI H_2O, 1' 7.5.2 Drying: N_2 gun 7.6 Development: 7.6.1 Dev.: MiBK:IPA 1:3, 3' 7.6.2 Rinse: IPA, 1'	
8	Gate evaporation 8.1 Evaporation LAB 600H: 8.1.1 Ni: 2 Å/s, 500 Å 8.1.2 Au: 2 Å/s, 1300	
9	Ohmic contact lift-off 9.1 Lift-off: 9.1.1 PR strip: 1165, 70°C, >6 h 9.1.2 Eventual manual metal peeling by tweezers 9.1.3 PR cleaning: 1165, LP sonic, 70°C, 3' 9.1.4 Rinsing: IPA, LP sonic, 1' 9.1.4 Drying: N_2 gun	

Step	Process description	Cross-section after process
10	Pad lithography 101 Dehydration: 135°C, 5' 112 AZ nLOF 2020 coat: 2 krpm, 30" 10.3 Soft bake: 105°C, 1' 10.4 Exposure: MLA150, dose 150 mJ/cm^2, defocus 0 10.5 Post-exposure bake: 105°C, 1' 10.6 Development: 10.6.1 Dev.: AZ726, 1' 10.6.2 Rinsing: 2X DI H_2O 10.6.3 Drying: N_2 gun 10.7 O_2 Plasma Descum: Tepla GigaBatch, low power, 30"	
11	Pad contact evaporation 11.1 Evaporation EVA760: 11.1.1 Cr: 5 Å/s, 200 Å 11.1.2 Cu: 5 Å/s, 8000 Å	
12	Pad contact lift-off 12.1 Lift-off: 12.1.1 PR strip: SVC-14, 70°C, >6 h 12.1.2 Eventual manual metal peeling by tweezers 12.1.3 PR cleaning: SVC-14, LP sonic, 70°C, 3' 12.1.4 Rinsing: IPA, LP sonic, 1' 12.1.4 Drying: N_2 gun	

Tab. A.3 explains abbreviation and acronyms used in Tab. A.2.

Table A.3 – List of abbreviations and acronyms used in the process flow.

Abbreviation or acronym	Explanation
BOE	Buffered oxide etch
DI	Deionezed water
HP	High power
HSQ	Hydrogen silsesquioxane
ICP RIE	Inductive coupled plasma reactive-ion etching
LP	Low power
MP	Medium power
PR	Photoresist
PMMA	Polymethyl methacrylate
RTP	Rapid thermal process
Sonic	Sonication

A.1.1 Proximity error correction for EBL

EBL steps, especially those involving the definition of NWs and mesa, are the most critical in the process flow. Despite the small dimension of the beam spot (down to almost 4 nm), the effective e-beam resolution is limited by several factors and, among them, the proximity effect is one of the most important. During e-beam writings electrons suffer two main scattering mechanisms:

- electron-electron scattering: electrons scatter among them-self inside the e-beam and in the resist, causing an increase of the e-beam spot size
- backscattering: a large number of electrons, which depends on the operating electric field (up to 100 KV), can pass through the resist, reach the substrate and then scatter back to the resist exposing regions which are not supposed to be exposed

The two contributions are taken into account in a mathematical model consisting of the superposition of two Gaussian curves, one for each scattering mechanism, which results in the point spread function (PSF) [138]:

$$PSF(r) = \frac{1}{1+\eta}\left[\frac{1}{\alpha^2}\exp\left(-\frac{r^2}{\alpha^2}\right) + \frac{\eta}{\beta^2}\exp\left(-\frac{r^2}{\beta^2}\right)\right] \tag{A.1}$$

Here the list of variables in Eq. A.1:

- $r = \sqrt{x^2 + y^2}$ is the radial distance
- η represents the ratio of the backscattered to forward scattered energies;
- α is the forward scattering parameter;
- β is the backward scattering parameter.

Eq. A.1 describes the probability for an electron to scatter at a distance r from the point where the beam is directed, that is to say the broadening of the electron beam. If a high electric field is used, α is very small and the forward-scattering associated Gaussian goes rapidly to 0 as soon as r increases, this means that the contribution of such mechanism in broadening the e-beam spot is negligible while the backscattering is the most dominant.

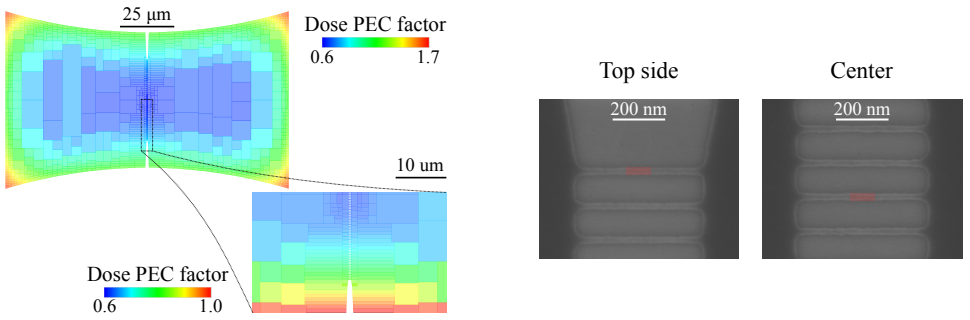
Since the Raith EBPG5000, present in CMi, works at 50 kV, the forward scattering is not considered as the primary source of beam broadening; hence, only β and η are the parameters usually considered for the proximity error correction (PEC) procedure. In particular, β depends mainly by the substrate while η by the used resist.

The values of these two parameters are found experimentally by performing tests with specific patterns. Without going into details about the theory behind, the procedure usually consists of performing a dose test with different values of β and η. Since this study would require a lot of combinations, during our tests, we perform a fine tune of the dose, while just a few values of β and η are tested. This choice is motivated by the fact that usually good guest values for the parameters are known, therefore the variation for each combination of material and resist is small.

In devices such as NW-FERs (Ch. 4), a large array of NWs is present (up to 240 NWs) and the EBL should ensure the same width for all of them. Since HSQ (negative resist) is used for the lithography, if NWs are exposed without PEC, they would be much larger in the center of devices (in the worst case they might also merge) than on the sides. The HSQ in the center of devices receives a much larger electron dose because of backscattering happening while exposing the nearby regions, whereas, on the sides, the amount of backscattered electrons is up to 50 % smaller. The proximity error correction locally changes the dose, by a correction factor close to 1 (e.g. from 0.1 to 2, with 1 meaning no change in the dose), during the device writing to compensate the proximity effect: the dose is usually larger closer to device borders and lower toward their center (Fig. A.1a). Thanks to optimized PEC parameters, we manage to get an array of 240 30 nm-wide NWs with constant width, as can be seen in Fig. A.1b.

A.2 E-beam writing on transparent and low conductive substrates

Another issue limiting the resolution of e-beam lithography is the electrical charging of exposed substrates. Once the electrons of the e-beam pass through the resist and substrate, they might get trapped in the latter or pass trough it reaching the sample bottom, which is usually connected to ground, avoiding electron accumulation. Electrons reaching the ground is the ideal situation which happens if conductive substrates are used (e.g. n- or p-doped silicon). For semi-insulating (e.g. high-resistive silicon substrates) or insulating (e.g. silicon carbide or sapphire substrates), electrons instead get trapped close to the surface and start to create an electric field which is directed in the opposite direction of the e-beam one. Also in this case the effect is a broadening of the e-beam spot size and the cause is shortly called substrate charging. Depending on the



(a) PEC for a 240 NW-FER.

(b) SEM images of 30 nm -wide NWs in a 240 NW-FER.

Figure A.1 – (a) Real design of a 240 NW-FER with PEC coefficients defined by color. (b) SEM images of 30 nm-wide NWs in the top side and central part of the 240 NW array of a NW-FER. Two red identical semitransparent rectangles are overlapped on both figures to show that the width of the NW is maintained constant along the array thanks to proximity error correction.

resistivity of the substrate and the used resists, different solutions can be employed to strongly reduce this problem.

The transparency of substrates to light is also another issue for e-beam lithography, since these machines use laser interferometers to locally measure at which height the sample is and then adjust the e-beam focus; therefore, a wrong focus position can result in e-beam spot broadening.

Substrate charging and transparency are quite often linked problems since insulating substrates frequently are also transparent. The wafers used for the fabrication of the devices of this thesis are composed of a GaN-HEMT epi-structure grown on different substrates: p-doped silicon, high-resistive silicon, and silicon carbide (double polished, thus completely transparent). Considering the small thickness of the epi-structure (up to 5-6 μm) and the electric field of the e-beam, the substrate is the main actor in the charging problem. In Tab. A.4, we reported the solutions that we used to mitigate both issues when using different substrates and resists.

Table A.4 – Adopted solution to alleviate charging and transparency problems in insulating or transparent substrates.

Substrate	Resist	Solution
HR-Si	HSQ	Since the conductivity of the substrate is not very small, a copper tape is glued on top of the sample before coating and then it is attached to the e-beam sample holder (which is connected to ground). Such solution takes advantage of the HEMT 2DEG to create an escape path for electrons.
HR-Si	PMMA	For this configuration, the 2DEG has been partially etched (considering the process flow of Tab A.2), thus it cannot be used to reduce charging. The solution adopted in this case is to coat a conductive layer (ESPACER or Electra92) to create a conductive path for electrons. Once the sample is loaded on the holder, a copper tape connects the conductive layer to the holder.
Double-polished SiC	HSQ	This wafer is both insulating and transparent. Considering the process flow in Tab. A.2, prior to step 1.2, 200 Å of Ti are evaporated. Then a Cu tape is used as in the case for HR-Si wafer. Before step 2.1.3, the titanium layer is etched (the recipe is based on Cl_2/BCl_3 chemistry and at high power). Finally, while performing step 2.2.1, also the Ti layer is etched by the BOE [139].

B RF measurements with VNA

B.1 Introduction

One of the most useful measurement tools for characterizing RF devices is the vector network analyzer. Any electronic device can be seen as a black box with a certain number of terminal pairs (called ports) allowing the connection to the external world. The measurement of the scattering matrix (the element of such matrix are called S-parameters), whose dimension depends on the number of port, allows extracting a lot of information about the device electrical behavior. Considering a dual-port device (Fig. B.1), the S-matrix consists in four elements (2X2) which related the input (a) and output (b) power for each port and they are defined as follow:

$$\begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \begin{pmatrix} a_1 \\ a_2 \end{pmatrix}; \quad \text{with} \quad S_{11} = \frac{b_1}{a_1}, \quad S_{12} = \frac{b_1}{a_2}, \quad S_{21} = \frac{b_2}{a_1}, \quad S_{22} = \frac{b_2}{a_2}. \tag{B.1}$$

The physical meanings of S-parameters are the amount of power going from one port to another (S_{xy}) and the power reflected (S_{xx}) from the same port. Once the S-matrix is known, it is possible to extract other known matrices such as the impedance, admittance, and hybrid ones. All together, they allow obtaining a lot of knowledge about the device under test.

The vector network analyzer (VNA) is an instrument that measures S-parameters, both in magnitude and phase, for a device. On-wafer measurements can be realized by connecting the fabricated devices with a VNA through an RF probe station (Fig. B.2), which allows contacting devices directly, without any wire bond or macroscopic connection, after proper RF pads are

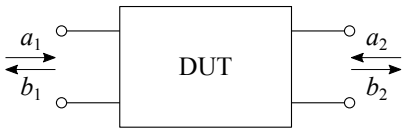


Figure B.1 – Dual-port representation of a DUT. a_i and b_i (with i equals 1 or 2) are the input and output power for the i-th port, respectively.

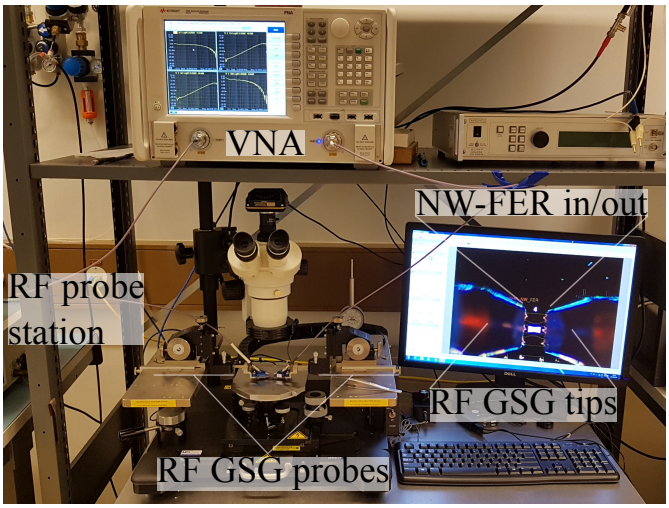


Figure B.2 – Used RF setup with a VNA connected to the RF probes which are landed on the input and output of a NW-FER.

designed.

B.2 On-wafer SOLT calibration

One of the main advantages of using S-matrices is the possibility to represent the behavior of a cascade of black boxes with the product of their transfer matrices, which can be derived by S-matrices. Such property is fundamental to remove the systematic errors during an RF measurements, which are caused by non-ideal VNA behaviors and the measurement setup, especially in the case of probe stations. These errors are predictable and repeatable, thus can be measured and compensated, though a complete error removal is impossible due to different reasons, such as: imperfection in the calibration standard, connector interface, interconnecting cable, instrumentation, device contact, etc.

The procedure to measure systematic error and perform a compensation is called calibration (which is different from usual instrument calibration executed in specialized laboratories using calibrating standards for each measured quantity, e.g. voltage, power, temperature). On-wafer calibrations differ from the standard one because the calibration standards are on the same dimension scale of the devices under test and measured by RF probes. There are several techniques for on-wafer calibration which range from very simple, low frequency (up to tens of GHz) and less precise procedure to more complex calibrations which are more reliable (especially at high frequency) and less sensitive to errors and uncertainty elements (e.g. the uncertainty of the calibration standards) [140].

For NW-FERs, we decided to use a short-open-load-thru (SOLT) calibration, which is a simple techniques based on the measurement of the four standards (short, open, load and trough) that

are usually fabricated on a ceramic substrate called impedance standard substrate (ISS). This technique gives good results up to tens of GHz; however, it is strongly affected by the uncertainty of the four standards, for which the impedance value must be well known.

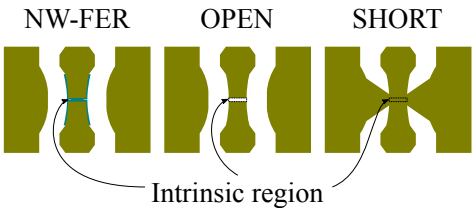
Independently of the calibration procedure, it is important to properly set all the measurement settings (number of frequency points, type of sweep, signal power, power attenuators, etc.) before performing the calibration. For any change of one of these parameters, the calibration loses precision. Other sources of errors which might make the calibration, especially on-wafer, less effective are cables moved, different metal pads and contact forces which influence the contact resistance between the RF probe and pads, different chip temperature, etc.

B.3 Open-short de-embedding

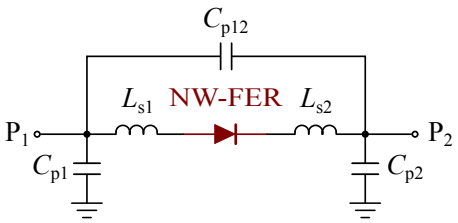
Performing a good calibration allows considering the DUT directly connected to the ports of an "ideal" VNA, that is to say that the source-measure ports are moved to the device input and output on the wafer. At this point, the contribution of the RF pads, which are essential for the on-wafer measurement, needs to be taken into account to extract the behavior of the intrinsic device. Though the RF pads should be properly designed to behave as a 50 Ω transmission line, by using proper software tools that take into account geometrical and material specifications, they might have a different behavior which influences the device measurement. The de-embedding procedure allows removing all the parasitic contributions from the RF pads to obtain measurements describing only the intrinsic device. In this definition, the term parasitic must be carefully interpreted since it refers only to the pads parasitic and not to device parasitic (which should not be removed). Also in this case there are a lot of de-embedding procedures, especially for transistors. Since in our case we measured S-parameters of diode-like devices, an open-short de-embedding is performed, which consists of measuring two dummy structures, one for the open and one for the short (Fig. B.3a to B.3d). Once the S-parameters of the two dummies are known, the de-embedded S-parameters of the DUT can be calculated as:

$$S_{DUT} = \mathbf{z2s}(\mathbf{y2z}(\mathbf{s2y}(S_{meas}) - \mathbf{s2y}(S_{open})) - \mathbf{y2z}(\mathbf{s2y}(S_{short}) - \mathbf{s2y}(S_{open}))) \tag{B.2}$$

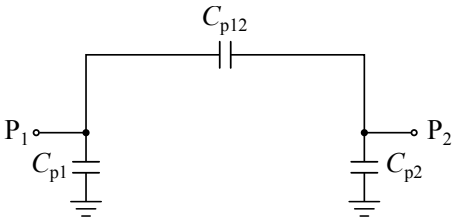
The bold parts in Eq. B.2 refer to the MATLAB functions used to convert a matrix of one type (e.g. S-matrix) into another one (e.g. Y-matrix).



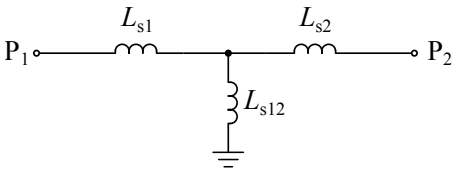
(a) Schematics of a NW-FER with RF pads, an open and a short.



(b) Equivalent circuit of RF pads.



(c) Equivalent circuit of the open dummy structure.



(d) Equivalent circuit of the short dummy structure.

Figure B.3 – (a) Schematic of a NW-FER with RF pads, together with the open and short dummy structures. (b) Equivalent circuit of the RF pads used to connect NW-FERs with RF probes. (c) and (d) Equivalent circuit of the open and short dummy structures, respectively, used for de-embedding NW-FERs.

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Education

03/2015–(12/2019) **Ecole Polytechnique Fédérale de Lausanne, Lausanne**, *PhD*, *Doctoral school of Microsystems and Microelectronics (EDMI)*, POWERLab, prof. Elison Matioli.

10/2012–07/2014 **Politecnico di Torino, Turin**, *Master*, *Electrical engineering*.
Final grade: 110/110 cum laude

10/2009–09/2012 **Politecnico di Bari, Bari**, *Bachelor*, *Electrical engineering*.
Final grade: 110/110 cum laude

09/2004–09/2009 **Istituto Tecnico "Alessandro Volta", Bitonto (BA)**, *High school*, *Electrical specialization*.
Final grade: 100/100 cum laude

PhD project: "*AlGaN/GaN Nanowires: from Electron Transport to RF Applications*"

I use III-Nitride based high electron mobility transistors (HEMTs) to study electron transport and exploit such knowledge to develop new high performance radio frequency (RF) devices. Practically, my work consists of:

- fabricating nanometer-size devices for electron transport studies, such as ballistic transport of electrons at room temperature, to push up the speed/frequency of current devices;
- fabricating RF devices based on nanometer-size geometries to improve RF performance by exploiting different transport regimes and reducing parasitics;
- electrically characterizing RF devices by using different measurement setups based on LabVIEW programming and several instruments, such as: semiconductor analyzers, impedance analyzers, lock-in amplifiers, vector network analyzers and cryogenic-temperature high-magnetic-field setups.

Experience

09/2013 – 04/2014 **Master thesis intern**, AVAGO, Turin, Italy.
We analyzed and designed DFB lasers for short length communication, which consisted of:

- writing a model in MATLAB code to simulate the behavior of lasers below and above threshold;
- analyzing problems related to laser design with a focus on single and multi mode operations;
- proposing new structures with enhanced single mode operation.

Reference: Dr. Giammarco Rossi, e-mail: giammarco.rossi@ieee.org

05/2009 **Electronics technician**, Mel System, S.r.l., Modugno, Italy.
- Standard testing procedures of the electronics systems and repairing damaged units.
- Calibration and operation a CNC machine in the production process.

Summer work (2006-2012) **Salesman**, F.lli Santoruvo, S.n.c., Bitonto, Italy.
- Summer work helping my father in sales, store keeping and wholesale purchases.

Other Student tutoring, volunteer for church summer camps, short experience as kitchen boy.

Skills & Abilities

Programming LabVIEW, MATLAB, C, C++, IGOR

CAD SOLIDWORKS, AUTOCAD, COMSOL

Software ADS, LaTeX, MS Word, MS Excel

Micro/Nano-technology Electron beam lithography, photo-lithography, wet and dry etching, atomic layer deposition, RTA, e-beam evaporator, scanning electron microscope, atomic force microscope, profilometer

Measurement tools Semiconductor analyzers, lock-in amplifiers, impedance analyzers, vector network analyzers, probe stations, cryogenic chambers and superconductive magnets

Soft skills Exceptional time management, team working, creative problem-solving, ability to accept and learn from criticism

Languages Italian: mother tongue. English: C1. French: B1

Get to know me

I like practicing different sports and I love martial art (I am a green belt in judo). I adore cooking traditional Italian dishes and this relaxes me quite a lot. I also like playing video-games in my free time. Despite being shy, I appreciate going out with friends and meeting new people. Movies and TV-series also occupy a portion of my free time and I am keen on reading while commuting to work. I keep myself updated about the situation in my country along with in the rest of the world. I like to keep my house clean without diverging in obsessive cleaning.

Publications

Conferences

IWN 2018, Kanazawa Oral Presentation:"Zero-bias rectifiers based on AlGaN/GaN nanowires for RF detection", G. Santoruvo and E. Matioli

CSW 2018, Boston Oral Presentation:"Multi Nano-Wire In-Plane Gate Field Effect Transistors", G. Santoruvo and E. Matioli

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