Proceedings of the 32th International Symposium on Power Semiconductor Devices & ICs
May 17-21, 2020, Vienna, Austria

Output Capacitance Losses in Wide-Band-Gap Transistors: A Small-Signal Modeling Approach

Mohammad Samizadeh Nikoo*, Armin Jafari, Nirmana Perera, and Elison Matioli*
Power and Wide-band-gap Electronics Research Laboratory (POWERlab)
École Polytechnique Fédérale de Lausanne (EPFL)
Lausanne, Switzerland
*mohammad.samizadeh@epfl.ch, elison.matioli@epfl.ch

***Abstract*—Wide-band-gap (WBG) power semiconductor devices are gaining an increasing interest in power circuits, as they exhibit a low specific ON-resistance (R_{ON}) while providing a high blocking voltage. The energy dissipation corresponding to resonantly charging and discharging their output capacitance (C_{OSS}), however, severely limits their performance at high switching frequencies. In this work, we demonstrate a simple approach based on a small-signal measurement, to model C_{OSS} losses in transistors. The device output capacitance is modeled by an effective C_{OSS} in series with a frequency-dependent resistance R_S. The proposed method is completely based on a small-signal measurement and it directly leads to a general view of frequency-dependent C_{OSS} losses in power transistors. We consider four commercial devices based on GaN and SiC, and using the proposed technique, we evaluate C_{OSS} losses. We verify the model-based prediction with thermal measurements. The precise characterization of C_{OSS}-losses proposed in this paper is essential for designing efficient high-frequency power converters.**

Keywords—Wide-band-gap, GaN, SiC, high frequency, output capacitance, Coss losses.

I. INTRODUCTION

Using wide-band-gap (WBG) semiconductor devices leads to considerable reduction of conduction losses in power converters with respect to Si devices, as they provide a lower specific ON-resistance [1]. WBG semiconductor devices also exhibit a significantly lower gate capacitance with respect to their Si counterparts, which enables WBG devices to operate at much higher switching frequencies. This leads to a considerable size reduction in passive components, therefore, a much higher power density can be achieved [2]. This property together with the ease of integration, also paves the way towards monolithically integrated power circuits, which operate at megahertz switching frequencies [3].

The recently observed energy dissipation caused by resonantly charging and discharging of the output capacitance (C_{OSS}) of WBG semiconductor devices, however, severely limits their performance at high switching frequencies [4]-[8]. This can result in significantly lower-than-expected efficiencies in power converters [9]. Using large-signal measurement methods such as Sawyer-Tower (ST) [4] and nonlinear resonance [7], a frequency-dependent energy dissipation was measured in WBG transistors. This was in contrary to the previously observed frequency-independent C_{OSS} losses in Si superjunction (SJ) transistors [10], [11].

In all of the commonly used large-signal measurement techniques of C_{OSS} losses, separate measurements are needed at different operation points, including voltage-swing, frequency, and dv/dt, which makes it difficult to obtain a full view of C_{OSS} losses in different devices. Furthermore, practical constraints such as power-frequency trade-off in power amplifiers, can substantially limit the loss characterization in transistors especially at high frequencies. A recently proposed method based on a small signal modeling approach, suggested a simple way to fully characterize the frequency-dependent C_{OSS} losses in WBG transistors [8]. The device output capacitance can be modeled by an effective C_{OSS} (C_{OSS}^{eff}) in series with a resistance R_S. These parameters, which can be easily measured by an impedance analyzer, show a complete view of frequency-dependent C_{OSS} losses in power transistors. In this work we demonstrate the selection of devices with lowest C_{OSS} losses based on this modeling approach, just using a simple small-signal measurement, and corroborate them with thermal measurements.

II. SMALL-SIGNAL MODEL

Fig. 1a shows the proposed model for output capacitance, including a nonlinear capacitance in series with resistance R_S and in parallel with resistance R_P. The effect of R_P is dominant at DC, while R_S significantly contributes to high-frequency C_{OSS}-losses (Fig. 1b). Small-signal measurements of the quality factor (Q-factor) of the C_{OSS} show a considerable lossy behavior for C_{OSS} of WBG transistors (Fig. 1c). By applying voltage $v(t)$ to the output capacitance, and considering R_S as a perturbation element, the power loss in R_S can be written as $P_{DISS} = R_S\,(C_{OSS}\,dv/dt)^2$. Considering an operation frequency f, we obtain the charging/discharging C_{OSS} energy dissipation as

$$E_{DISS} = 2R_S(\frac{dv}{dt})\int_0^V C_{OSS}^2\,dv \quad (1)$$

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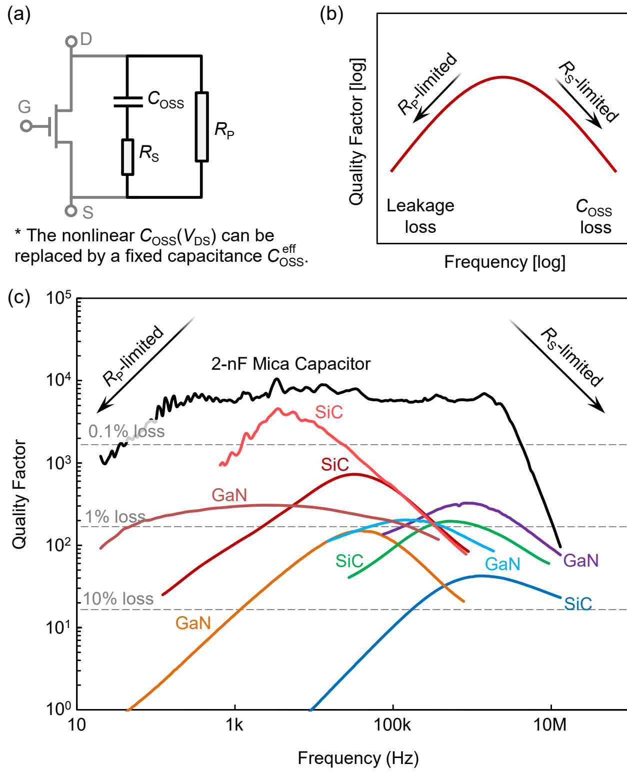

Fig. 1. (a) A model for output capacitance of transistors (OFF state) where C_{OSS} is a nonlinear voltage-dependent capacitance and R_S and R_P represent losses at low and high frequencies, respectively. (b) Schematic of quality-factor (Q-factor) of output capacitance of a transistor representing the amount of C_{OSS} losses. The effect of R_P (mainly corresponding to the leakage current) is dominant at DC, while R_S significantly contributes to the switching dynamics and C_{OSS} losses. (c) Measured Q-factor of output capacitance of several commercial WBG transistors versus frequency at $V_{DS} = 40$ V. The gate and source of transistors where shorted ($C_{OSS} = C_{DS} + C_{GD}$). The amount of losses (2-10%) is in agreement with the previously measured losses using large-signal methods [4]-[7].

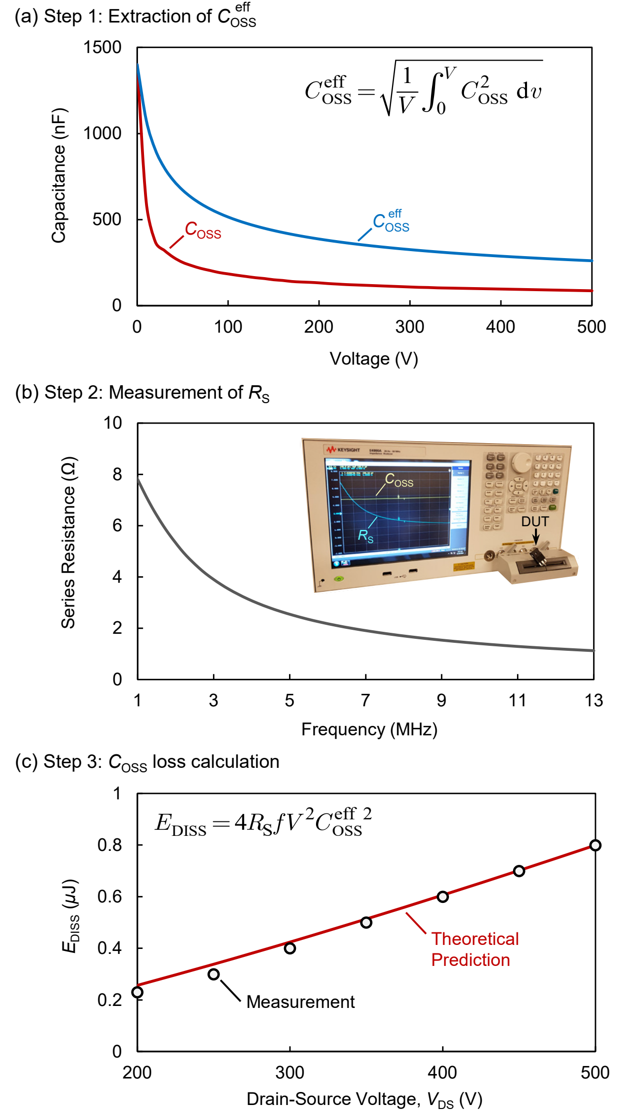

Fig. 2. Procedure of C_{OSS} loss evaluation in wide-band-gap transistors. (a) In the first step, the effective C_{OSS} is extracted using (3) based on data reported in datasheet. (b) The series resistance R_S measured at 40 V versus frequency is measured in the next step. The inset shows the measurement set-up with a E4990A 50-MHz impedance analyzer. (c) Using (1), and based on the effective C_{OSS} and R_S, the C_{OSS} energy dissipation can be calculated. The results corresponding to the frequency of 1-MHz is illustrated (solid line) showing a good agreement with large-signal measurements based on ST method.

which shows a dv/dt-dependence of E_{DISS}. Considering a sinusoidal excitation with frequency f we have

$$E_{DISS} = 4R_S f V^2 C_{OSS}^{eff\,2} \tag{2}$$

where we introduce the following term of effective C_{OSS}, related to the portion of C_{OSS} that contributes to power dissipation:

$$C_{OSS}^{eff} = \sqrt{\frac{1}{V}\int_0^V C_{OSS}^2 \, dv} \tag{3}$$

Equation (2) represents E_{DISS} exclusively as a function of R_S (which can be measured) and C_{OSS}^{eff} (which can be extracted from datasheet).

Fig. 2 shows three steps for E_{DISS} extraction based on the introduced method, for a 1200-V 36-A SiC MOSFET. In the first and second steps, C_{OSS}^{eff} and R_S are obtained. The data presented in datasheet can be used to extract C_{OSS}^{eff} (Fig. 2a), while R_S should be measured with an impedance analyzer (Fig. 2b). In the third step, E_{DISS} is calculated using (1). To verify the predicted results, we compared the results corresponding to the frequency of 1-MHz, with large-signal measurement results, which shows an excellent agreement (Fig. 2c).

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III. Selection of Devices with Lowest C_{OSS} Losses

The small-signal method to evaluate E_{DISS} is a simple technique showing a general view of C_{OSS} losses in WBG transistors and, therefore, can be used to select low-loss devices. Among WBG transistors within the same R_{ON} and voltage rating, the values of C_{OSS} are generally the same; hence, the value of R_S determines the level of C_{OSS} losses. As a result, a single measurement determines the device with lowest amount of C_{OSS} losses, which is preferable for high switching frequency power circuits.

We selected four WBG transistors with similar current capability of ~30-A based on GaN (devices A and B) and SiC (devices C and D). A detailed description of the selected devices is presented in Table I. Figs. 3a-d represent the measured C_{OSS} versus voltage at two different frequencies 1-MHz and 10-MHz, for devices A-D, respectively. These figures show that all of the selected devices have the same range of C_{OSS} values, and the measurement results agree with the values reported in datasheet. Fig. 3e shows the measured R_S at V_{DS} = 40 V versus frequency for devices A-D. Device A (GaN) exhibits the lowest R_S, which corresponds to the lowest E_{DISS}. The method predicts the largest C_{OSS} losses for device D (SiC). To verify the prediction, we submitted devices C and D (with the same package) to a 75-V peak-to-peak sine-wave at three different frequencies (1-MHz, 2-MHz, and 3-MHz) showing significantly higher losses in device D, as predicted by the method (Figs. 3f and 3g).

Table I

Specifications of Evaluated WBG Transistors

Device	Type	Voltage and current rating		R_{ON}**	C_{OSS} (pF)
		Voltage (V)	Current* (A)	(mΩ)	at 400-V
A	GaN FET	600	31	55	72
B	GaN FET	600	26	56	71
C	SiC FET	650	30	80	66
D	SiC FET	650	31	80	64

* Continuous current at 25 ºC.
** Typical ON resistance at 25 ºC.

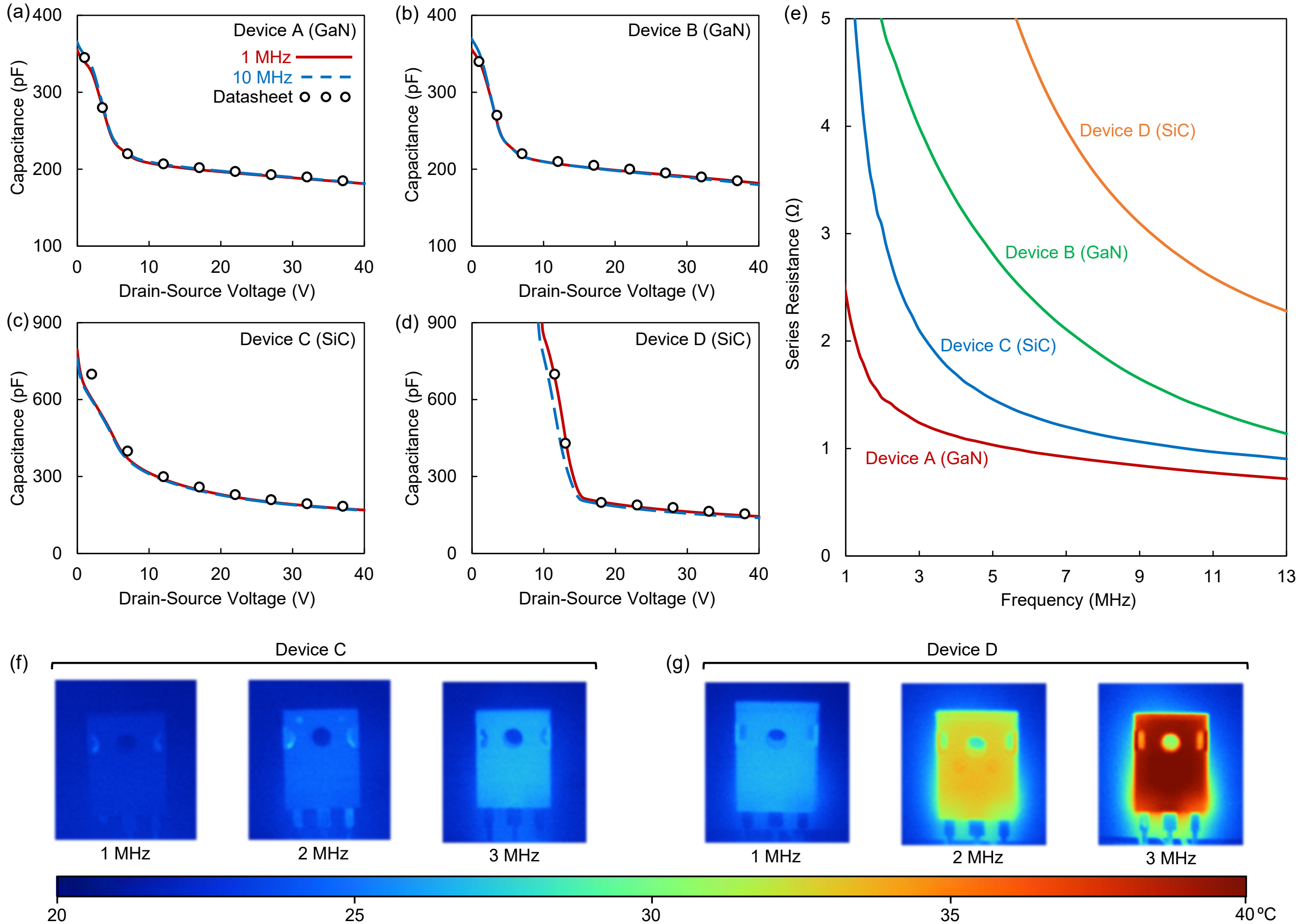

Fig. 3. Measured C_{OSS} versus drain-source voltage at 1 MHz (solid red line) and 10 MHz (dashed blue line) as well as data reported in datasheet (discrete points) for (a) device A (GaN), (b) device B (GaN), (c) device C (SiC), and (d) device D (SiC), all 600/650-V rated with ~30-A current rating (Table I). The figures show consistency of C_{OSS} over frequency as the valid assumption of the proposed method. (e) Series resistance (R_S) of the four devices versus frequency. The method simply predicts lowest and highest losses for devices A and D, respectively. Thermographs of (f) device C and (g) device D (gate and source shorted), both with the same package, submitted to 75-V peak-to-peak sinusoidal waveform (charging and discharging C_{OSS}) at three different frequencies 1 MHz, 2 MHz, and 3 MHz. Device D shows considerably higher losses, as predicted by the proposed method.

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IV. Conclusion

We proposed a new C_{OSS} model and measurement technique that enables selection of devices with lowest C_{OSS}-losses among different WBG transistors, just by performing one small-signal measurement: R_S-versus-frequency. It is also possible to use the measured R_S together with C_{OSS}^{eff} (which can be extracted from datasheet) to estimate the amount of C_{OSS} losses. The generality and robustness of this method enables it to quantify C_{OSS} losses of WBG transistors, which is a crucial source of losses in soft-switched power converters, and to select devices with the best performance.

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