

InAs-on-Insulator Fin Nanostructures for Integrated Computation and Sensing Functions

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“There is no failure except in no longer trying.” — Elbert Hubbard

To my nephew, Vedanth and my late grandmother, Ammomma.

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Manee

Abstract

Field-effect transistors (FETs) have established themselves as a leading platform for electrical detection of chemical and biological species. Their advantages over other optical, mechanical sensing platforms are attributed to being miniaturizable, mechanically durable, label-free, responsive in real-time, compatible with scalable CMOS technology and their cheap manufacturing cost. 3D nanostructures such as nanowires (NWs) show great promise for improving sensitivity and limit of detection due to their high surface-to-volume ratio and non-planar geometry. However, when seen in literature the material of choice has predominantly been silicon because of its mastery over economies of scale in the electronic industry. Few and far in between, alternative materials are being explored and quite noticeable among them is indium arsenide (InAs). InAs is interesting not only for its superior electronic properties but also its integration capabilities. Firstly, with its higher electron mobility, the supply voltage can be scaled down in line with transistor miniaturization trends. Secondly, its small, direct bandgap enables novel heterojunction devices such as tunnel FETs. Finally, InAs integration on silicon has seen major advances over other materials giving it an edge for highly scalable platforms. Indeed, the properties mentioned are interesting from a computation point of view but are also highly favourable for sensing functions.

Rather than the typical InAs NW geometry for sensing explored in literature, in this thesis we focus on 3D fin geometry. From a computation standpoint, a tall fin geometry is interesting for better electrostatic gate control to have a high signal-to-noise ratio as well as enabling higher ON currents in future implementations of tunneling FETs. From a sensing standpoint, the 3D dimensionality favours detection at ultra-low concentrations. We demonstrate n-type, InAs-on-insulator fin nanostructures with a unique vertical aspect ratio as single and multiple-fin arrays. Using nanofabrication and characterization tools, highly crystalline InAs fins of 130 nm fin height and fin width down to 30 nm are built (i.e. an aspect ratio of nearly 4:1). For a tight pitch layout of multiple fin array, where the effective device width exceeds the actual device width and for even tens of millivolts applied voltage, high current levels in microamperes range are read-out. The ion sensitive functioning is validated for hydrogen ions. A sensitivity of 41.2 mV/pH is extracted at 6 microampere drain current. What differentiates this work from other InAs sensor devices in literature is not only the unique 3D fin geometry but also integration method of InAs module on silicon that is catalyst-free, monolithically integrated on silicon, highly scalable and CMOS compatible.

Finally, further study of the devices built for sensing is carried out using metal gating

Abstract

from focussed ion beam (FIB) deposition and ionic liquid (IL) gating. To benchmark the performance of Ionic liquid gating technique, it has been applied to another set of devices SOI Ribbon FETs and compared with its pH response.

Keywords: InAsOI, InAs, Field-Effect Transistor (FET) sensors, FinFET sensor, aspect ratio, Ion-Sensitive FET, nanostructure, pH sensor, ion sensing, SOI, high-k dielectric, III-V integration

Résumé

Les transistors à effet de champ (field-effect transistors, FET) se sont imposés comme une plate-forme de pointe pour la détection électrique d'espèces chimiques et biologiques. Leurs avantages par rapport aux autres plateformes de détection optique et mécanique sont attribués à leur propension à la miniaturisation, leur durabilité mécanique, leur réponse sans marquage (label-free) et en temps réel, leur compatibilité avec la technologie extensible CMOS ainsi que leur coût de fabrication peu élevé. Les nanostructures 3D telles que les nano-fils (Nanowires, NW) sont très prometteuses pour améliorer la sensibilité et la limite de détection en raison de leur facteur d'aspect élevé et de leur géométrie non plane. Cependant, le silicium reste le matériau décrit de manière prépondérante dans la littérature en raison de l'économie d'échelle qu'il permet dans l'industrie électronique, éclipsant de fait l'étude de matériaux alternatifs, tel que notamment l'arséniure d'indium (InAs). L'InAs possède un haut potentiel d'utilisation non seulement grâce à ses propriétés électroniques supérieures, mais aussi pour ses capacités d'intégration. En effet, sa grande mobilité électronique permet une réduction de la tension d'alimentation en parfait accord avec la tendance actuelle de miniaturisation des transistors. De plus, son intervalle de bande interdite faible et direct permet le développement de nouveaux dispositifs à hétérojonction tels que les FETs à effet tunnel. Enfin, l'intégration de l'InAs sur le silicium a connu des avancées majeures par rapport à d'autres matériaux, ce qui lui confère un avantage important pour les plates-formes hautement industrialisables. En effet, les propriétés mentionnées sont intéressantes d'un point de vue performance de calcul mais sont également très favorables pour les fonctions de détection.

Plutôt que de se fonder sur la géométrie de NW d'InAs typique pour la détection qui a été extensivement décrite dans la littérature, nous nous concentrons dans cette thèse sur une géométrie 3D en aileron. D'une part, du point de vue des performances de calcul, une géométrie à aileron haut est intéressante pour un meilleur contrôle de la grille électrostatique afin d'obtenir un rapport signal/bruit élevé, ainsi que pour permettre des courants ON plus élevés dans les futures implémentations de FETs à effet tunnel. D'autre part, du point de vue des performances de détection, la dimensionnalité 3D favorise la détection de molécules d'intérêt à des concentrations ultra-basses. Nous démontrons des nanostructures à aileron de type n, InAs-sur-isolant, avec un rapport d'aspect vertical unique, sous forme de réseaux d'ailerons simples et multiples. En utilisant des outils de nanofabrication et de caractérisation, des ailerons de InAs hautement cristallin de 130 nm de hauteur et de 30 nm de largeur sont produits (i.e. avec un rapport d'aspect proche de 4 :1). Pour une disposition dense de réseaux à ailerons multiples, où la largeur effective du dispositif dépasse la largeur réelle du

Résumé

dispositif, et pour une tension appliquée de seulement quelques dizaines de millivolts, des niveaux de courant élevés dans la gamme des microampères sont lus. La sensibilité ionique des dispositifs a été validée pour les ions hydrogène. Une sensibilité de 41,2 mV/pH est extraite à un courant de drain de 6 microampères. L'innovation de ce projet réside non seulement dans le développement d'une géométrie 3D en aileron unique, mais aussi dans l'utilisation d'une méthode d'intégration du module InAs sur silicium sans catalyseur, d'une façon monolithique, hautement industrialisable, et compatible CMOS.

Enfin, une étude plus approfondie des dispositifs élaborés pour la détection est réalisée avec une grille métallique déposée par faisceau d'ions focalisés (FIB) ainsi que par une grille consistant d'un liquide ionique (IL). Afin d'évaluer les performances du contrôle de la grille par liquide ionique, cette technique a été appliquée à un autre type de dispositifs FET à ruban de Silicium-Sur-Isolant (Silicon-On-Insulator, SOI), et leurs réponses respectives au pH comparées.

Acronyms

ALD	Atomic Layer Deposition
BHF	Buffered Hydrofluoric acid
CMOS	Complementary Metal-Oxide Semiconductor
DC	Direct Current
DHF	Dilute Hydrofluoric acid
EBL	Electron Beam Lithography
FET	Field-Effect Transistor
FIB	Focussed Ion Beam
MOSFET	Metal Oxide Semiconductor Field-Effect Transistor
GND	Ground
IC	Integrated Circuit
LTO	Low Thermal Oxide
MBE	Molecular Beam Epitaxy
MEMS	Micro Electro Mechanical System
MIS	Metal Insulator Semiconductor
RT	Room Temperature
SEM	Scanning Electron Microscopy
SOI	Silicon On Insulator
TEOS	Tetra Ethyl Ortho Silicate Oxide
TCAD	Technology Computer-Aided Design
TFET	Tunneling Field-Effect Transistor
TEM	Transmission Electron Microscopy
VLSI	Very Large Scale Integration

Units of measurements

$^{\circ}\text{C}$	Celsius degree
A	Ampere
C	Coulomb
eV	electron Volt
J	Joule
$^{\circ}\text{K}$	Kelvin degree
kg	Kilogram
m	Meter
s	Second
h	Hour
V	Volt
W	Watt
Ω	Ohm

SI decimal prefixes

Tera	T	10^{12}
Giga	G	10^9
Mega	M	10^6
kilo	k	10^3
hecto	h	10^2
Deca	da	10^1
		1
deci	d	10^{-1}
centi	c	10^{-2}
milli	m	10^{-3}
micro	μ	10^{-6}
nano	n	10^{-9}
pico	p	10^{-12}
femto	f	10^{-15}

Physical constants

Elementary Charge	e (or q)	$= 1.60206 \times 10^{-19} \text{ C}$
Planck Constant	h	$= 6.62606896 \times 10^{-34} \text{ J.s}$
Boltzmann Constant	k_B	$= 8.617343 \times 10^{-5} \text{ eV.K}^{-1}$
Free Space Permittivity	ϵ_0	$= 8.85418782 \times 10^{-12} \text{ F.m}^{-1}$
Air Relative Permittivity	ϵ_r	$= 1$
Speed of Light	c	$= 2.99792458 \times 10^8 \text{ m.s}^{-1}$
Gas Constant	R	$= 8.314 \text{ J/(mol.K)}$

Contents

Acknowledgements	iii
Abstract (English/Français)	vii
Acronyms	xi
Units of measurements	xiii
SI decimal prefixes	xv
Physical constants	xvii
List of figures	xxi
List of tables	xxviii
1 Thesis Overview	1
2 Introduction	3
2.1 Motivation	3
2.2 Computation Unit: MOSFET	4
2.2.1 Conduction Mechanisms	9
2.2.2 Multiple Gate Architecture	11
2.2.3 Novel Gating Architecture: Ionic Liquid Gating	12
2.3 Sensing Platform : Electrochemical transducer	15
2.3.1 Ion selective electrodes	16
2.3.2 FET based sensing	21
2.4 Motivation of InAs architecture for computing and sensing	23
2.5 III-V nanostructures for sensing	23
2.6 Choices in our System	31
2.6.1 Indium Arsenide	31
2.6.2 Geometry: High-Aspect-Ratio (HAR) fin	37
2.6.3 Sensing area	37
2.6.4 Sensing High-k Oxide	38
2.6.5 Junctionless Transistor	38

2.7	Summary	41
3	Technology Development of InAs-On-Insulator (InAsOI) FinFET Nanostructures	43
3.1	Process Overview	43
3.2	Pre-growth steps	44
3.2.1	Alignment Marks	45
3.2.2	Ebeam lithography	47
3.2.3	Silicon reactive ion etching	48
3.2.4	Oxide deposition	50
3.2.5	Template opening ebeam lithography	51
3.2.6	Wafer dicing	52
3.2.7	Silicon anisotropic wet etching	52
3.3	Template Assisted Selective Epitaxy Mechanism	54
3.4	MOVPE Growth characterization	57
3.4.1	Non-idealities in growth	63
3.5	Post growth processing	65
3.5.1	Parasitic removal	65
3.5.2	Source & drain lithography	68
3.5.3	Source & drain metallization	69
3.5.4	ALD isolation & pad opening	70
3.6	Summary	73
4	Measurements & Discussion	75
4.1	InAsOI FinFETs as pH Sensor	76
4.1.1	ISFET Characterization Setup	76
4.1.2	ISFET Measurements	78
4.1.3	Discussion	83
4.2	Ad-hoc Characterization	83
4.3	Ionic liquid gating measurements	85
4.3.1	IL Measurements on SOI Ribbon FETs	85
4.3.2	IL Measurements on InAsOI FinFETs	91
4.4	Metal Gate Patterning	93
4.5	Summary	96
5	Conclusions and Perspectives	97
5.1	Conclusions	97
5.1.1	Scalable III-V Integration platform for sensing: TASE	97
5.1.2	High Aspect Ratio Fin fabrication	98
5.1.3	Experimental characterization - pH sensing, Metal gate and Ionic Liquid gate	98
5.2	Perspectives	99
5.2.1	Design & Fabrication	100

5.2.2	Case for biosensing	102
5.2.3	TFET as a sensitive bio-sensor	102
Bibliography		103
Curriculum Vitae		113

List of Figures

2.1	n-type MOSFET schematic with 4 terminals.	5
2.2	Visualization of Moore's Law	6
2.3	Performance of CPU with time in terms of cost, functionality and high performance.	7
2.4	Dennard scaling law visualized in a MOSFET structure: scaling doping concentration (in orange), physical parameters (in blue), supply voltage (in green)	7
2.5	MOS capacitor behaviour	9
2.6	Drain current (log scale) vs gate voltage - transfer characteristics are shown for three different MOSFET modes a) Inversion b) Accumulation c) Depletion.	10
2.7	Diagram summarizing ionic liquid properties and applications	12
2.8	liquid specifications	14
2.9	Principle of electrochemical sensing.	15
2.10	Main components of a potentiometer cell measurement setup with a reference electrode and ion selective electrode.	16
2.11	Solid state ISE with a oxide layer behaving as ISM for H^+ ions.	18
2.12	EIS models a) Helmholtz, b) Gouy-Chapman, c) Stern.	20
2.13	Interface and potential drop with distance in (left) metal gate electrode and (right) reference electrode in liquid gating.	22
2.14	Motivation for InAs architecture from a computation and sensing perspective.	23
2.15	Left to Right: Change in conductance with different gas molecules, SEM image of NW structure and change in NW conductance as a function of back gate voltage	24
2.16	Left to Right: Concept of air bridge InAs NW sensor, in e) SEM images of the contact over many vertical InAs NWs, f) a zoom of the NW, metal contact and response of NW array to different concentrations of NO_2 down to 9 ppb of NO_2/N_2 in inset.	24
2.17	(a)-(c) Show schematic, SEM image of Ohmic-Ohmic contacted devices and their photo response behaviour at different gate voltages in light and in dark conditions, (d)-(f) show schematic, SEM image of Ohmic-Schottky contacted devices and their photo response behaviour at different gate voltages in light and dark conditions.	25
2.18	a) An SEM image of grown NW array. b) TEM image of the InAs NW. c) schematic of complete structure. d) SEM image of a typical measured device.	26

List of Figures

2.19	(a) Transfer characteristics of InAs NW FET in different vapor environments. b) Transconductance curve obtained from differentiation of data in (a). (c) Schematic of NWFET structure (left) and optical image of a complete device (right). Scale bar 20 μm	27
2.20	Use of vertical InAs NW array to culture mammalian cells and study their cell function.	27
2.21	Flourescence detection of protein immobilized on NW arrays. A) Scheme of functionalization of NW arrays with BSA-biotin and SA-488. B) wide field image showing the spacing of NWs is 2 μm . C) wide field image showing spacing of NWs is 7 μm . D)- F) shows intensity of corresponding yellow lines marked in the figure.	28
2.22	A. A schematic image showing the various NW density areas of vertical InAs NWs. White squares are of 500 \times 500 μm^2 with 2,3,5,7,10 μm spacing between NWs. B. Tilted SEM images of the density of nanowires. C. Morphology differences on the different NW densities where small, rounded forms seen on the high density wires and flat, spread out form on lower densities. D. & E. Living cells signature is seen through maintaining esterase activity (green = calcein-AM) and cell morphology qualitatively similar in red i.e DRAQ5 nuclear label staining.	29
2.23	A. Sensitivity of InAs sensor towards pH 4.7 to 7.8. B) Sensitivity of functionalized InAs NW towards avidin protein.	30
2.24	Energy Band Diagram of intrinsic InAs.	32
2.25	Energy Band Diagram of intrinsic InAs.	32
2.26	Energy Band Diagram of intrinsic InAs	33
2.27	Principle showing energy harvesting from fluidic flow by InAs NW wires	34
2.28	Techniques for III-V Integration on silicon	36
2.29	Simulated InAs-on-insulator FinFET structure.	39
2.30	Transfer characteristics I.	40
2.31	Transfer characteristics II.	40
2.32	Transfer characteristics III.	40
3.1	Classification of process steps for clarity is shown	44
3.2	Alignment marks are visualized on the wafer- prealignment marks, global wafer alignment procedure, die global alignment marks, die local alignment marks	45
3.3	SEM images show evolution of the metal alignment marks with an oxide protection layer. Small square is the metal marks, larger square is the protection oxide.	46
3.4	High resolution SEM image of a used Pt alignment mark - seen is the edge search effect of EBL. Scale bars are 20 μm and 10 μm respectively.	47
3.5	From under exposed to over exposed HSQ structures for different range of Dose, η values depicted in SEM images	49

3.6	Tilted SEM images of different test structures on buried oxide showing vertical sidewall etches	50
3.7	The top and tilted SEM views of an array of 30 nm wide fins where BHF over etch results in a collapse and is resolved with DHF 2% etch. Scale bar left to right - 300 nm, 200 nm, 150 nm	51
3.8	Template oxide enclosing entire Si structure seen in the top view SEM images	52
3.9	SEM images showing openings in PMMA resist of the template oxide in various test structures	53
3.10	a) Schematic of TMAH etch setup with heating and stirring functionality. b) SEM Image of a Si partial etch inside the SiO ₂ template is seen. Scale bar = 200 nm	53
3.11	(a) to (d) Topview SEM images of various structures back etched to different legnth. The bright areas where template oxide is filled with Silicon and dark regions where template oxide is hollow are clearly distinguishable. Scale bar = 1 μ m, 1 μ m, 200 nm, 200 nm.	54
3.12	MOVPE deposition mechanism	55
3.13	MOCVD Reactor Furnace	55
3.14	a) to c) Top view and d) to f) side view schematic of steps of main steps in order to realize templates for epitaxy	56
3.15	Antiphase boundary	56
3.16	Threading dislocations	56
3.17	Plot of growth rate versus fin width for InAs epitaxy run at 550°C for 10 mins	57
3.18	Plot of growth rate versus fin width for InAs epitaxy run at 550°C for 50 mins	57
3.19	Plot of growth rate versus fin width for InAs epitaxy run at 550°C for 50 mins	58
3.20	Top view SEM image of fins with design width of 20 nm and 50 nm with a difference in the back etch length and the grown InAs length for a growth time of 50 mins. Scale bar = 600 nm	58
3.21	The TEM image is taken across the line AA'. High resolution TEM shows a directional etch stop in (111) plane when using TMAH silicon etching. Scale bar = 100 nm, 20 nm.	59
3.22	A zoom of the previous HR TEM image at the hetero interface is shown here. Scale bar = 20 nm.	59
3.23	Diffraction Patterns - a) Single crystalline pattern showing discrete spots. b) when few grains are present the spots begin to form circles. c) large randomly oriented grains show no spots but rings.	60
3.24	a) An energy dispersive x-ray analysis (EDX) gives the elemental map indicating the material composition b) Single crystalline pattern showing discrete spots in the SAED image	60
3.25	The TEM image is taken across the line BB'.b) Focussed ion beam cross section of multiple fin array is shown. c) High Resolution image depicts the unique tall aspect ratio. Scale bar = 500 nm	61

List of Figures

3.26 a) An energy dispersive x-ray analysis gives the elemental analysis map indicating the material composition b) Single crystalline pattern showing discrete spots in the SAED image	62
3.27 SEM images show examples of good clean growths of multi-fin array with growth length larger than 1 μm . Scale bar is 1 μm and 1 μm	63
3.28 SEM images showing a) overgrowth on the device and a parasitic growth on SiO_2 b) overgrown multiple fin structure. c) overgrowth from a clean device growth. Scale bar 10 μm , 1 μm and 1 μm	64
3.29 Shown in SEM image a) is an arrow indicating a gap region then bad seeding of InAs most likely from partially removed silicon in the structure, b) is an outgrowth of InAs due to bad seeding than mere over growth with the arrow indicating the gap and c) another bad seeding that results in a fast over growth. Scale bar 1 μm , 2 μm and 1 μm	64
3.30 Optical microscope image showing unwanted InAs growths all over the chip seen as the black dots	65
3.31 Optical microscope images show before and after cases of using ultrasound and heat to clean unwanted InAs growths. Scale bar 300 μm and 300 μm . .	66
3.32 Optical microscope image shows before and after case of using ultrasound and heat does not result to much variation except minor changes marked in blue circle areas. Scale bar 300 μm and 300 μm	66
3.33 Optical images same section as pictured in previous figure 3.32, before and after case of applying 3 and 4 cycles of UV-sensitive stick and peel tape steps. Differences are marked in blue and green circled areas. Scale bar 300 μm and 300 μm	67
3.34 SEM images showing damages showing same region a) zoomed out where black arrow indicate history of a removed unwanted particle, white arrow indicated unwanted damage b) zoomed in where black arrow indicates history of removed unwanted particle .Scale bar 10 μm and 1 μm	67
3.35 SEM images of two different devices in a) and b) where white arrows indicate damage to grown structures whereas black arrows indicate the partially removed parasitic particles. showing Scale bar 300 nm and 1 μm	68
3.36 Optical microscope image showing a) source and drain contact lithography in PMMA resist and b) zoom in on one device. Scale bar 300 μm and 15 μm . .	69
3.37 Optical microscope image after metallization of source & drain areas. Scale bar is 100 μm	70
3.38 SEM image after metallization of Source & Drain areas. Scale bar is 100 μm	71
3.39 SEM image of a zoom in of source and drain metallization on a single device, in the inset a zoom out of the entire device with pads is seen. Scale bar is 200 nm and 300 nm for inset.	71
3.40 Optical microscope image shows source and drain metallization on many devices leading to the large 150 μm X 150 μm contact pads. Scale bar is 300 μm	72

3.41	Photograph of a chip after complete fabrication	73
4.1	Fluidic measurement setup. Scale bar is 1 cm.	76
4.2	Droplet setup for ISFET measurement	77
4.3	SEM image show s source and drain metallization on complete device and also how the measurement is carried out on the device.	77
4.4	a) pH response of the device and b) voltage sensitivity extraction for the same 40 nm wide fin.	78
4.5	a) At pH 4 repeatability of pH response for different time points in a voltage interval and b) pH response curves repeatability for the entire voltage sweep also showing hysteresis.	79
4.6	a) At pH 4 repeatability of pH response for the entire voltage sweep also showing forward to backward sweeps and b) pH response repeatability at pH 4 for different time points in a select voltage interval.	80
4.7	Cross section illustration of device pointing to likey interface defects resulting in hysteresis in transfer characteristics.	80
4.8	pH response curves for a) device B and b) device C.	81
4.9	Sensitivity extracted at 19 μ A for a) device B and for b) device C.	82
4.10	Hysteresis in device C for pH 5 and pH 7.	82
4.11	Schematic of FIB Deposition Principle	83
4.12	SEM right after EBID Pt deposition process. Scale bar 500 nm and 4 μ m.	84
4.13	I_D - V_G characteristics from a EBID Pt gate modulated device	84
4.14	IL Measurement Setup	85
4.15	Main steps in fabrication process of SOI Ribbon FET.	86
4.16	Main steps in fabrication process of SOI Ribbon FET.	86
4.17	SOI Ribbon FET transfer curve response to IL gating	87
4.18	SOI Ribbon FET1 IL response versus pH Response	87
4.19	Comparison of SOI Ribbon FET1 output characteristics for IL gating and metal gating	88
4.20	Type of voltage signal applied to the gate in order to control sweep rate.	88
4.21	SOI Ribbon FET 1 effect of changing sweep rate on hysteretic loops.	89
4.22	SOI Ribbon FET 2 transfer curve response to IL gating	89
4.23	SOI Ribbon FET 2 IL response versus pH Response	90
4.24	Comparison of SOI Ribbon FET 2 output characteristics for IL gating and metal gating	90
4.25	InAsOI FinFET device response with IL gating drain current to the left axis and gate leakage current to the right of the axis.	91
4.26	Investigation of hysteresis effect in InAsOI FinFET by varying the sweep rate.	92
4.27	InAsOI FinFET IL Reproducibility	92
4.28	InAsOI FinFET vs InAs NW IL gating transfer response	93
4.29	Device schematic for simulation of partial gating electrode (left) 50 % gating and (right) 75 % gating.	93

List of Figures

4.30	Device simulation showing transfer characteristics of partial gating electrode (left) 50 % gating and (right) 75 % gating.	94
4.31	Tilted (30 °) SEM image of a) device before patterning and b) after EBL patterning, tungsten sputtering without any tilt and lift-off of resist. Scale bar is 200 nm and 100 nm.	95
4.32	Tilted (30 °) SEM image of a FIB cross section showing continuous metal film on a multiple fins with tilted sputtering of W but without an EBL step. Scale bar is 100 nm and 100 nm.	95
5.1	TASE device and material activity	97
5.2	InAs fin cross section	100
5.3	InAs fin array design	100
5.4	InAs FinFET with on chip reference electrode and supporting microfluidics .	101
5.5	InAs fin arrays usef for energy harvesting	101

List of Tables

2.1	Table of scaled parameters for dennards law and generalized scaling law . .	8
2.2	Table of ionic liquid specifications	13
2.3	Electrochemical windows calculated for various ILs at a cut-off current density of 0.5 mA/cm ² using GC electrode at 25 °C.	14
2.4	A comparison of silicon & InAs electronic properties.	31
2.5	A comparison of Si & InAs crystal properties.	35
3.1	Summary of the technology development achievements from this chapter. .	73
4.1	Summary of sensor response	96
5.1	III-V Fin geometry comparison	98
5.2	Main conclusions of this work from technology side leading to sensor charac- terization	99

1 Thesis Overview

An overall outline of the thesis structure is given here.

Chapter 2- At the start, a broad context for the work of ion sensing in healthcare and environmental monitoring is provided. Then the reader is refreshed with main concepts to bear in mind while reading the thesis. A). Basics of computing technology are presented: Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) principle, how MOSFET miniaturization benefits the electronic industry, different conduction mechanisms in MOSFET with a focus on junctionless transistor (used in this thesis) and how multiple gate architectures, emphasizing Fin Field-effect transistor (FinFETs) are relevant. Further, a brief discussion for iontronics is given since ionic liquid (IL) gating is also employed to characterize device functioning. B). Field of electrochemical sensing is introduced: principle of conventional ion selective electrodes (ISEs) is given, concepts of Nernst limit, electrical double layer, reference electrode are elucidated. The gradual progression towards solid-state ISEs is explained. Next, we rationalize field-effect transistor (FET) based electrochemical sensing and speak about its figures of merit such as sensitivity, responsivity, detection limit and specificity. The case for importance of a nanoscale FET sensor to improve the various figures of merit is given. C). Through a review of scientific literature for InAs nanoscale sensors the interest of the scientific community in using InAs nanostructures especially NWs for electrochemical and biological sensing is iterated. D). Finally, we systematize the choices in our system in terms of material, integration platform, sensing geometry, sensing area, sensing oxide and summarize these reasons towards an InAsOI FinFET sensor and computing module.

Chapter 3- The entire technology development process steps to realize working devices are detailed here. The fabrication is classified under 3 main divisions- pre-growth steps, epitaxy growth process and post growth processing. Fabrication issues and how they were tackled are extensively presented. All process steps were carried out entirely by the author at the cleanroom of Center for micronanotechnology institute (EPFL) except for the step of metal organic chemical vapor deposition growth that was done by collaborators at IBM Research

Zurich and the transmission electron microscope images taken in collaboration with staff at the Interdisciplinary Center for Electron Microscopy (EPFL). The fabricated devices are referred to as InAs-On-Insulator (InAsOI) FinFETs

Chapter 4- The first measurement results of built devices as ion-sensitive field effect transistor are presented. To further characterize the devices other gating techniques are explored - metal gating and ionic liquid gating are used. Another fabrication batch is necessary in order to carry out more detailed statistical analysis. With changes in design, growth process the limitations of current results can be resolved and steps taken towards this end are also addressed.

Chapter 5- The main contributions of this work are highlighted to conclude the thesis work. For future perspectives a case for sensing based on different electronic principles such as tunneling field effect transistors is made. The chosen technology module of this thesis is highly versatile and suitable for such a future tunneling transistor implementation.

2 Introduction

2.1 Motivation

Internet of Things (IoT) is a concept where a swarm of sensors and devices are deployed ubiquitously, collect data continuously and are connected to the internet to communicate with each other. The concept isn't new as there existed IoT objects such as automatic teller machines (ATMs) and cold drink vending machines as early as 1970s and 1980s that were connected to the internet and monitored remotely. However the context in which IoT is relevant today is all-pervasive from healthcare to environmental monitoring, automotive industry, to agriculture, manufacturing industry and energy management in every day home and office spaces. These IoT devices enable generation and collection of vast amounts of data that can be processed at the edge or the cloud in order to respond in real-time to various scenarios.

IoT is taking the world by storm as the number of smartphones are surging, technology costs are going down, more devices with internet capabilities and sensors are built and the cost of connecting to the internet is decreasing. As of late 2000s, the number of devices connected to the internet were declared to have surpassed the number of people connected to it. And it is further predicted that by 2030 a 100 trillion connected devices will be present in the world [1].

The demand for ion-sensors and biosensors has also risen due to their offering of continuous real-time and parallel detection of multiple species along with being low cost and portable. These features are very attractive for point-of-care applications for healthcare as well as remote environmental monitoring. Rising and aging populations in many parts of the world lead to increased healthcare burden on governments and societies. An increasing concern is reducing these medical costs. Medicine is progressing towards a personalized era thanks to its clinical relevance. In personalized medicine, two key aspects can be differentiated as personalization in the prediction of illness and the treatment of illness are both important. Patient monitoring systems enable early diagnosis of diseases or illness condition. During

illness treatment, tailoring drug therapeutics to individual's unique needs enables maximum drug efficacy. Molecular diagnostics based on patient's DNA allow clinicians to identify the possible outcome of a patient to a particular treatment in advance of administering. Conventional laboratory diagnostic platforms are struggling to cope with these demands of personalized medicine.

On the bright side with developments in semiconductor technology, there has been an emergence of FET based solutions for clinical diagnostics [2, 3, 4, 5, 6, 7]. Advances in electronics, biotechnology, microfluidics and micro-nano technology have paved way for these analytical systems at the micron scale. The FET, a workhorse of the electronics industry is a mature component which can be configured to measure responses to biological or chemical reactions. Ion torrent and DNA electronics are companies which develop next generation sequencing (NGS) techniques where the system directly translates chemical sequences (A, C, G, T) into digital information (0,1) on a semiconductor chip. In other words the system marries chemistry to proven semiconductor technology or is when Watson meets Moore. DNA electronics are examples of companies exploiting diagnostic technology using ion sensitive FETs. The advantages of these technologies are obvious low power consumption, miniaturization, high-throughput, rapid sequencing at an economic scale using semiconductors. NGS is currently driving discovery and enabling the future of personalized medicine.

This FET ion sensing technology has implications not only in the healthcare industry but other industries too. Measurement of ions such as CN^- , F^- , S^- , Cl^- - in the context of water pollution monitoring, Pb^{2+} , Hg^+ , Cd^+ , As^+ - in air pollution monitoring, NO_3^- , NO_2^- - in food processing industry, Ca^{2+} in dairy industry, K^+ in fruit juice industry or H^+ , Na^+ , K^+ , Ca^{2+} in the healthcare industry [8, 9, 10, 11, 12]. It is towards such an FET based ion sensing application that this thesis is also directed.

2.2 Computation Unit: MOSFET

A transistor can be described as the most basic computation component of nearly all modern electronic equipment. In this section, we will see how the evolution of transistor led to great improvements in computing power. And in the next section 2.3.2 how the same technology is also advantageous to a sensing configuration. Any electronic device is made up of millions and possibly billions of transistors working together. This is why efforts in making them smaller, more efficient and cheaper are eternal. The transistor was first patented by Julius E. Lilienfeld in 1925 [13]. However, Walter Brattain, John Bardeen and William Shockley are historically credited with the first successful demonstration of a field-effect transistor in 1948 [14]. A transistor is simply a portmanteau of the words transfer and resistor as it transfers a signal at the input with a particular resistance to the output at a different value. Today, MOSFETs are the most widely used type of transistors in the integrated circuit (IC) industry. They have four terminals: source, drain, gate and bulk. In a lot of times, the source and body terminals are connected to each other making the device three terminal in

2.2. Computation Unit: MOSFET

operation. Essentially the current flow between the drain and source is controlled by the gate terminal through a gate oxide hence the name field-effect as shown in the schematic of figure 2.1(a). The source and bulk terminals are grounded together. In the device, the gate source voltage (or in short, gate voltage) is V_{GS} , the drain source voltage is V_{DS} are applied and the drain current, I_{DS} is read out. The transfer characteristics of a n-type MOSFET is shown in figure 2.1(b). One can distinguish a region where current grows exponentially called the sub-threshold region. After a certain gate voltage called the threshold voltage (V_{Th}) the transistor is considered to be turned ON. Here on, the current grows gradually and eventually enters a linear region of operation.

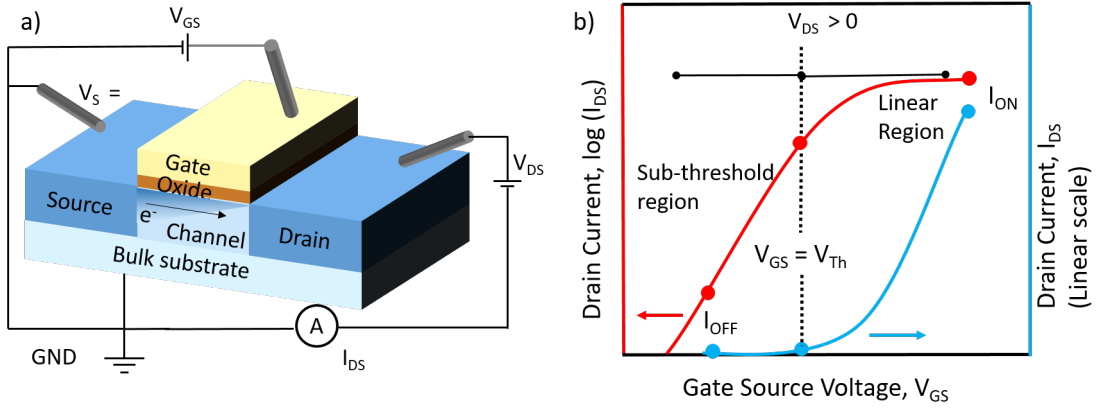


Figure 2.1 – n-type MOSFET schematic with 4 terminals.

When using a MOSFET in digital applications, it is operated as a switch. The transistor switches between two distinct, stable states: OFF and ON, making them binary logic state devices. While the transition from OFF to ON state is relevant in terms of charge needed to change states and for speed of the final operation. Whereas, for MOSFET as an analog block, the transition region between OFF and ON states is very important. In this transition region, the subthreshold region, incremental changes in V_{GS} modulate the output I_D over a wider range. The MOSFET device is at the heart of the electronic industry revolution. Two important figures of merit for MOSFETs are the inverse subthreshold slope, also known as the subthreshold swing (SS) and the transconductance efficiency that are described as follows. Shown in equation 2.1 and equation 2.2 are SS and the units are mV/dec.

$$SS = \frac{dV_{GS}}{d(\log(I_{DS}))} = \left(\frac{dV_{GS}}{d\phi_S} \right) \cdot \left(\frac{d\phi_S}{d(\log(I_{DS}))} \right) = m \cdot n \quad (2.1)$$

where $m = \frac{dV_{GS}}{d\phi_S}$ is known as the body factor and $n = \frac{d\phi_S}{d(\log(I_{DS}))}$ is a factor related to injection mechanism in particular the distribution of electrons according to Fermi-Dirac

statistics and depends only on temperature. Therefore, SS can be re-written as follows:

$$SS = m \cdot n = \left(1 + \frac{C_D + C_{it}}{C_{ox}}\right) \frac{kT}{q} \ln(10) = 59 \left(1 + \frac{C_D + C_{it}}{C_{ox}}\right) mV/dec \quad (2.2)$$

In equation 2.3 is the transconductance efficiency or transconductance-to-current ratio which is an important parameter for analog design.

$$\frac{g_m}{I_{DS}} = \frac{1}{I_{DS}} \frac{\delta I_{DS}}{\delta V_{GS}} = \frac{\delta(\ln I_{DS})}{\delta V_{GS}} = \frac{\ln(10)}{SS} \quad (2.3)$$

MOSFETs implemented in a particular style of circuit design called complementary metal-oxide semiconductor (CMOS) are the norm for the IC industry now. Complementary means logic functions are performed in pairs of devices nMOSFET and pMOSFET. In the pair only one transistor is ON at a time and the combination allows to consume power only momentarily while switching between ON & OFF state. Hence, the main highlights of CMOS technology are good noise immunity and low static power dissipation.

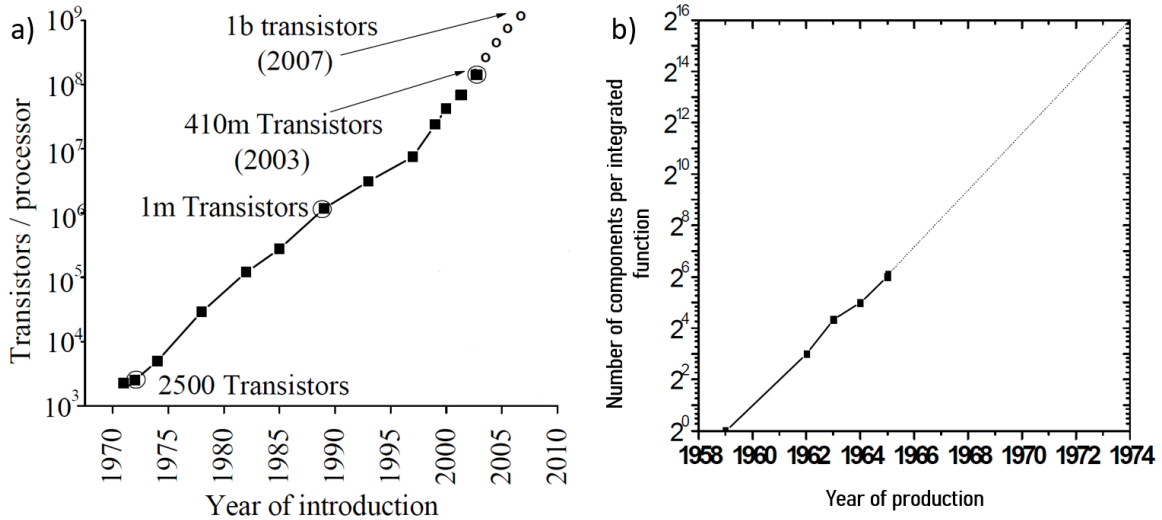


Figure 2.2 – a) Visualization of Moore's Law with the number of transistors in a commercial processor by INTEL with year of introduction, b) Graph prepared by Gordon Moore on the number of components per function growing over the years. Graphs taken from [15, 16].

The microelectronics industry has gained immensely from MOSFET miniaturization. Gordon Moore, co-founder of Fairchild Semiconductor in 1965 published a seminal paper which predicted that the components (transistors, capacitors, resistors and diodes) in an IC doubles roughly every two years [15]. This is visualized in two graphs that alternately

represent the same idea in figure 2.2. In figure 2.2 (a) an increase in number of transistors per processor and in figure 2.2 (b) the increase in number of components both with respect to time in years. Infact this observation he made became so popular that it went on to dictate the economics of the electronic industry for decades and is popularly known as Moore's law.

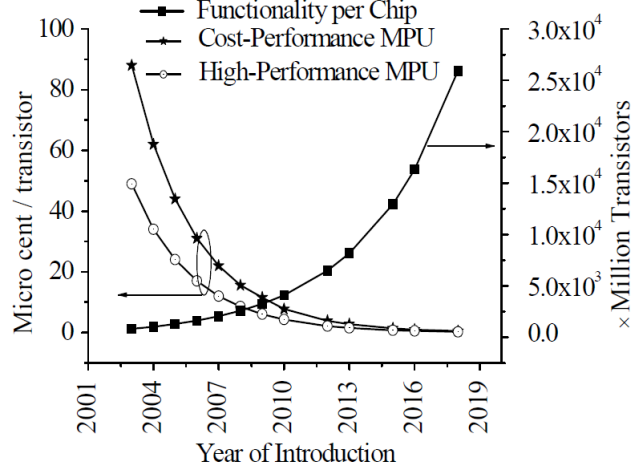


Figure 2.3 – Performance of CPU with time in terms of cost, functionality and high performance.

In the 1960s an IC chip had few transistors, within three orders of magnitude. Whereas today millions and possibly billions of transistors exist on a central processing unit (CPU) chip or a micro-processor unit (MPU) chip as we see in figure 2.3. The advantages of miniaturization and implications of Moore's law can be seen in figure 2.3 which include increasing functionality per chip, reducing manufacturing cost of processor units and building higher preformance systems.

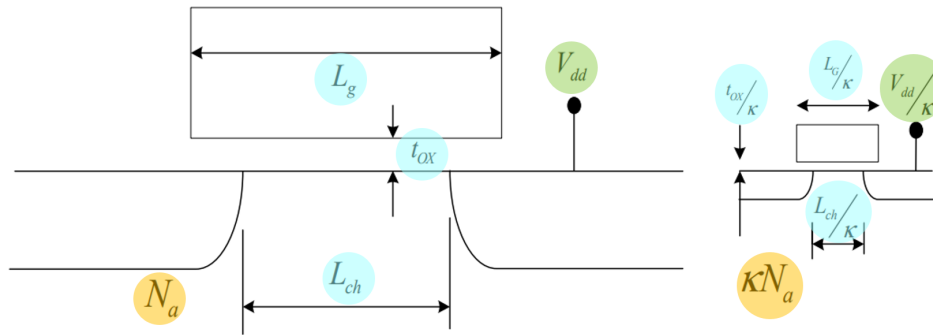


Figure 2.4 – Dennard scaling law visualized in a MOSFET structure: scaling doping concentration (in orange), physical parameters (in blue), supply voltage (in green) Modified from [16].

In 1974, Robert Dennard *et al.* and others published a paper that delved into the how the physics of MOS scaling enables performance enhancement from which constant field scaling theory emerged[17]. A linear transformation by a scaling factor, k is applied to three parameters: supply voltage, V_{dd} , doping concentration, N_a , and to physical dimensions of gate length, L_G , channel length, L_{ch} and gate oxide thickness, t_{OX} in a way that the device electric field scaling remains constant. Pictured in figure 2.4 modified from [16] is a sketch on left (right) is the device before (after) scaling. Despite changes in the above mentioned parameters, the electric field intensity written as Voltage/Length cancels out the scaling factor and remains unchanged.

Scaled Parameters	Constant field Scaling	Generalised scaling
t_{OX}, L, W, X_j, W_d	$1/\kappa$	$1/\kappa$
N_a, N_d (ions/cm ³)	κ	$\alpha\kappa$
Power supply: (V_{dd})	$1/\kappa$	α/κ
Electric field in device: (E)	1	α
Capacitance: (C)	$1/\kappa$	$1/\kappa$
Inversion charge density (Q)	1	α
Circuit delay time: $\tau \sim CV/I$	$1/\kappa$	$1/\kappa$
Power dissipation: (P)	$1/\kappa^2$	α^2/κ^2
Power density ($\sim P/A$)	1	α^2
Circuit density	κ^2	κ^2
Chip Area (A)	$1/\kappa^2$	$1/\kappa^2$
Current, Drift: (I)	$1/\kappa$	$1/\kappa$

Table 2.1 – Scaled parameters for Dennard’s law and generalized scaling law. Taken from [16].

However as the MOSFET scaling continued and the channel length started becoming comparable to the depletion layer width of the source and drain junction negative effects called short channel effects (SCE) started coming into play [18]. The effects of SCEs among others are drain induced barrier lowering (DIBL) and surface scattering of carriers. Therefore when the device dimensions entered sub-micron dimensions, two-dimensional effects in SCE and DIBL became important. Hence, the gradual field approximation became invalid and the field increased and resulted in slower reduction in supply voltage than predicted by constant field scaling [19, 20]. Brews *et al.*, Baccarani *et al.* introduced a more generalized scaling rule taking into account an additional parameter scaling constant ' α ' and generalized scaling

took the form shown in equation 2.4 [19, 20].

$$V'_{dd} = \frac{\alpha}{\kappa} V_{dd} \Rightarrow \alpha = \kappa \frac{V'_{dd}}{V_{dd}} \quad (2.4)$$

where V_{dd} = Supply voltage of previous generation, V'_{dd} = New supply voltage, α = scaling constant, κ = scaling factor. A summary of the Dennard scaling and generalized scaling parameters is shown in the table 2.1.

2.2.1 Conduction Mechanisms

MOSFETs can be classified as normally OFF and normally ON devices when no gate source voltage is applied i.e $V_{GS} = 0$ V. In normally OFF devices, drain current is blocked due to a reverse biased drain-channel junction. On the other hand for normally ON devices, drain current conducts because there is a channel between source and drain and a voltage needs to be applied to turn OFF the device. The work function difference between the gate electrode and the semiconductor helps to tune this normally ON and normally OFF behaviour. An important constituent of a MOSFET is the presence of semiconductor junctions at the source and drain regions and the presence of a MOS capacitor (MOSCAP) block. The MOSCAP under consideration is shown in figure 2.5(a) [21]. Where the body is p-type silicon, the gate oxide is SiO_2 and the gate electrode in this case is N^+ doped polysilicon. The gate voltage is V_G and all potentials are referenced with respect to the body or bulk terminal which is grounded.

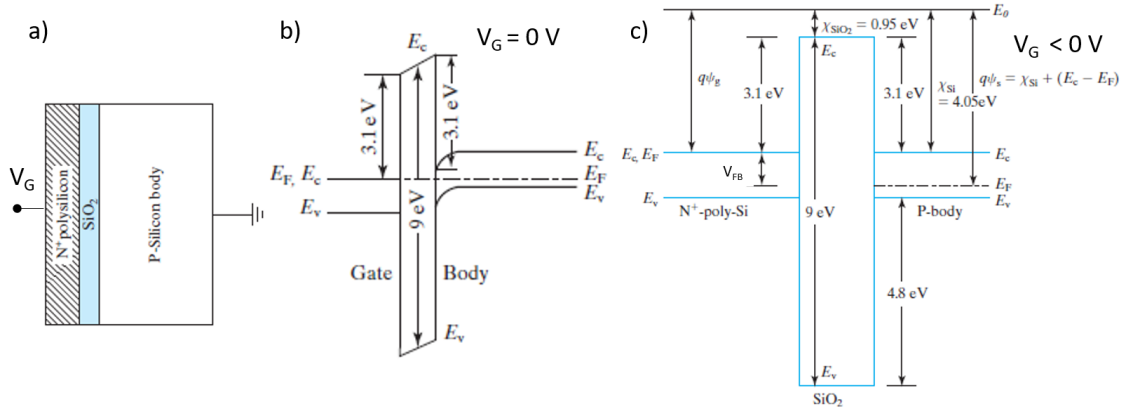


Figure 2.5 – MOS capacitor behaviour. Schematic modified from [21].

In figure 2.5(b) - (c) are energy band diagrams drawn across the three sections of the device when no gate voltage has been applied and when a negative gate voltage is applied respectively. In figure 2.5(c) one can see that the energy bands (E_C and E_V) of the substrate are flat at the gate-oxide-silicon substrate interface and this condition is known as the flat band condition and occurs when a negative voltage is applied at the gate terminal. The

notations of the symbols used in the figure are as follows: E_C = conduction band energy, E_V = valence band energy, E_F = fermi energy level, E_G = band gap, χ_{Si} = electron affinity in silicon, χ_{SiO_2} = electron affinity in silicon dioxide, ψ_g = gate material work function, ψ_S = semiconductor work function and V_{FB} = flat band voltage.

For a n-type MOSFET, the doping configurations and the transfer characteristics for three different operation modes are illustrated in figure 2.6(a)-(c) and are inversion mode, accumulation mode and junctionless mode. Where V_{TH} is the threshold voltage after which the device is considered to be turned ON. The V_{FB} is flatband voltage as described in the earlier paragraph. The transfer characteristics of the three modes resemble each other however it must be kept in mind that the underlying conduction mechanism is still different.

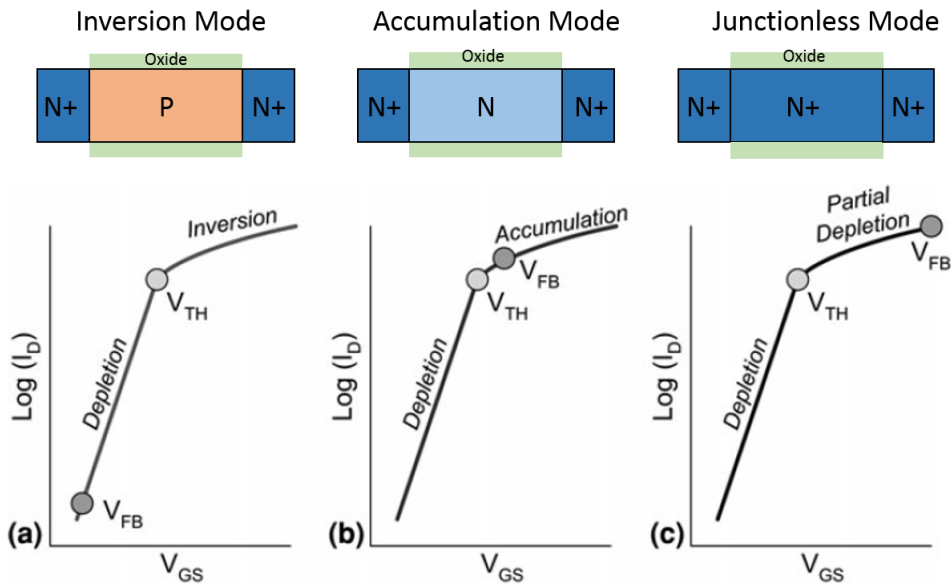


Figure 2.6 – Drain current (log scale) vs gate voltage - transfer characteristics are shown for three different MOSFET modes a) Inversion b) Accumulation c) Depletion. Image taken from [22].

- In inversion mode, below V_{TH} , the device is either partially depleted or fully depleted. And V_{FB} is at a voltage lower than V_{TH} , in the OFF region of the device. Below V_{FB} , the body of the substrate is neutral p-type. Above V_{TH} , when turned ON, the channel region is depleted, forms a weak *inversion* layer and then a stronger inversion layer.
- In accumulation mode, below V_{TH} the channel is fully depleted. When a section of the channel is no longer depleted then one reaches V_{TH} . When V_{GS} is increased further, the channel becomes neutral, with no depletion, reaching V_{FB} . For higher V_{GS} than V_{FB} an *accumulation* layer forms in the ON state of the device.
- In junctionless mode, the entire semiconductor is highly and uniformly doped from source to channel to drain region. Below V_{TH} is partially or fully depleted and turned

OFF. At V_{TH} the peak electron concentration in the channel reaches that of the background doping level, N_D . When V_{GS} is increased further, the entire channel cross section reaches N_D concentration and hence V_{FB} is reached.

Particular junctionless transistors have gained interest as they do not have semiconductor junctions. In inversion mode devices, formation of ultra-shallow junctions with high doping concentrations became a big challenge because of diffusion laws and statistical nature of doping of atoms [22]. A junctionless architecture is a highly doped semiconductor block in the form of a thin layer as used in double gate planar MOSFET (DG MOSFET) or nanowire (NW FET) or a fin (FinFET). The cross section of the device is important as it has to be narrow enough to enable turn OFF.

2.2.2 Multiple Gate Architecture

When MOSFETs were scaled into sub-micron range the performance starts to degrade significantly and this does not favour the miniaturization trend. For a planar MOSFET, the electrostatic control of the channel is essentially one dimensional. This led to problems such as short channel effects - sub-threshold slope degradation and Drain induced barrier lowering (DIBL) when scaled down. Multiple-gate architectures started to emerge in response to enhancing such performance limitations [23]. The electrostatic control over channel can be regained by changing the shape of MOSFET to more two (2D) dimensional or three dimensional (3D) architectures. A multiple-gate is when the gate metal wraps around the channel of nanowire or fin in 3D FET structures. In section 2.6.5 using TCAD simulations the performance of the multi-gate FinFET structure of this thesis work is presented.

2.2.3 Novel Gating Architecture: Ionic Liquid Gating

Iontronics is an emerging field that seeks to control electronic devices with materials such as ionic liquids (IL) in which charge carriers are ions [24]. Iontronics as a technology is overarches the fields of solid-state electronics and biological systems. An IL is a substance, purely ionic, described as a salt and are present in liquid state at unusually low temperatures. They are often compared to the boiling point of water (100 °C) as a reference i.e an IL is a liquid below 100 °C. A diagram in figure 2.7 summarizes the interesting properties of ILs and their applications in a wide range of fields.



Figure 2.7 – Diagram summarizing ionic liquid properties and applications. Taken from [25].

A key aspect of ILs is the formation of an electric double layer (EDL) at the interface of an electronic conductor that is known to induce very high electric fields and results in efficient carrier modulation [26, 27]. The accumulation of charge carriers can be used to demonstrate various phenomena such as phase transition, magnetic ordering and superconductivity [27]. The EDL between ionic conductors (i.e also behaving as electronic insulators) and electronic conductors are exploited to build novel electronic concepts [24, 28]. At the nanoscale with high performance solid-state devices hitting a road block, researchers are pursuing unconventional ways of processing not based on solid-state electronics e.g molecular logic gates [29, 30], chemical logic gates [31], microelectrochemical logic circuits [32] and DNA computing [33]. In the review paper by Chun *et al.*, it is explained how iontronics is close to nature than solid-state electronics in the following ways: 1) since information in biological systems is

2.2. Computation Unit: MOSFET

transmitted by a variety of ions Na^+ , K^+ , Cl^- , Ca^{2+} and 2) biological processors have highly dynamic structures that operate non-linearly. For example, ion transport in cell membranes polarizes and depolarizes neurons in the brain. Charge selectivity towards specific ions or molecules can be tailored indicating the application of iontronics for analytical chemistry. Moreover iontronic devices are made of hydrogels that function in aqueous environments therefore have less restrictions for biocompatible, biodegradable logic circuits for sensing [24].

Ionic liquids specifications.

Ionic liquid	Abbreviation	Melting point ($^{\circ}\text{C}$)	Form	Density at 20°C (g/cm^3)	M. Wt. (g/mol)	Formula
1-(3-methoxypropyl)-1-methylpiperidinium bis (trifluoromethylsulfonyl) imide	[MOPMPip][TFSI]	-72	L	1.41	452.44	$\text{C}_{12}\text{H}_{22}\text{F}_6\text{N}_2\text{O}_5\text{S}_2$
1-(2-Methoxyethyl)-1-methylpiperidinium tris(pentafluoroethyl)trifluorophosphate	[MOEMPip][TPTP]	-	L	-	603.27	$\text{C}_{15}\text{H}_{22}\text{F}_{18}\text{N}\text{OP}$
N-Butyl-3-methyl-pyridinium dicyanamide	[BMPy][DCA]	16	L	1.05	216.29	$\text{C}_{12}\text{H}_{16}\text{N}_4$
N-(3-Hydroxypropyl)pyridinium bis(trifluoromethylsulfonyl)imide	[HPPy][TFSI]	-72	L	1.55	418.34	$\text{C}_{10}\text{H}_{12}\text{F}_6\text{N}_2\text{O}_5\text{S}_2$
N-Hexylpyridinium bis (trifluoromethylsulfonyl) imide	[HPy][TFSI]	4	L	1.39	444.42	$\text{C}_{13}\text{H}_{18}\text{F}_6\text{N}_2\text{O}_4\text{S}_2$
1-Butyl-1-methylpyrrolidinium trifluoroacetate	[BMPyrr][TFA]	31	L/viscous	-	255.28	$\text{C}_{11}\text{H}_{20}\text{F}_3\text{NO}_2$
1-Butyl-1-methylpyrrolidinium bis (trifluoromethylsulfonyl) imide	[BMPyrr][TFSI]	-6	L to viscous	1.40	422.41	$\text{C}_{11}\text{H}_{20}\text{F}_6\text{N}_2\text{O}_4\text{S}_2$
1-Butyl-1-methylpyrrolidinium dicyanamide	[BMPyrr][DCA]	-55	L	1.02	208.30	$\text{C}_{11}\text{H}_{20}\text{N}_4$
1-Butyl-1-methylpyrrolidinium trifluoromethanesulfonate	[BMPyrr][TfO]	3	L to viscous	1.25	291.34	$\text{C}_{10}\text{H}_{20}\text{F}_3\text{NO}_3\text{S}$
1-Hexyl-1-methyl-pyrrolidinium bis (trifluoromethylsulfonyl) imide	[HMPyrr][TFSI]	< -50	L to viscous	1.34	450.47	$\text{C}_{13}\text{H}_{24}\text{F}_6\text{N}_2\text{O}_4\text{S}_2$
Trihexyl(tetradecyl) phosphonium tris(pentafluoroethyl)trifluorophosphate	[P14,666][TPTP]	-50	L to viscous	1.18	928.88	$\text{C}_{38}\text{H}_{68}\text{F}_{18}\text{P}_2$
4-(2-Methoxyethyl)-4-methylmorpholinium tris(pentafluoroethyl)trifluorophosphate	[MOEMMor][TPTP]	-	L	-	605.24	$\text{C}_{14}\text{H}_{18}\text{F}_{18}\text{NO}_2\text{P}$
N-Methoxyethyl-N-methylmorpholinium bis(trifluoromethylsulfonyl)imide	[MOEMMor][TFSI]	-	L	1.51	440.38	$\text{C}_{10}\text{H}_{18}\text{F}_6\text{N}_2\text{O}_5\text{S}_2$
N-Ethyl-N,N-dimethyl-2-methoxyethylammonium bis(trifluoromethylsulfonyl)imide	[N112,102][TFSI]	< -70	L	1.43	412.37	$\text{C}_9\text{H}_{18}\text{F}_6\text{N}_2\text{O}_5\text{S}_2$
Triethylsulfonium bis(trifluoromethylsulfonyl)imide	[S222][TFSI]	-	L	1.46	399.4	$\text{C}_8\text{H}_{15}\text{F}_6\text{NO}_4\text{S}_3$
1-Ethyl-3-methylimidazolium bis(trifluoromethylsulfonyl)imide	[EMIm][TFSI]	-15	L	1.52	391.31	$\text{C}_8\text{H}_{11}\text{F}_6\text{N}_3\text{O}_4\text{S}_2$

Table 2.2 – Table of ionic liquid specifications. Taken from [34].

A number of popular ILs contain cations of piperidinium, pyridinium, pyrrolidinium, phosphonium, morpholinium, ammonium, sulfonium and imidazolium and anions of hexafluorophosphate $[\text{PF}_6]^-$, tetrafluoroborate $[\text{BF}_4]^-$, bis(triflyl)imide $[\text{NTF}_2]^-$, chloride, Cl^- and bis(trifluoromethylsulfonyl)imide (TFSI) [35]. These ILs with their physical properties and chemical formulae are shown in table 2.2. An important property of IL an is the electrochemical window (EW). The EW is the potential range in which the substance is inert; that is neither oxidised nor reduced. This is calculated by subtracting the reduction potential (cathodic limit- E_{CL}) from the oxidation potential (anodic limit- E_{AL}). This is especially important for field effect based devices such as MOSFET as it should coincide with the supply voltages necessary for device operation. Generally, linear sweep voltametry (LSV) or cyclic voltametry techniques are used to measure the EW. Hayyan *et al.* measured and tabulated the EW for various ionic liquids as shown in table 2.3 [34].

IL	E_{CL}	E_{AL}	EW
[P14,666][TPTP]	-3.64	2.17	5.81
[N112,1O2][TFSI]	-3.47	2.52	5.99
[HMPyrr][TFSI]	-3.06	2.61	5.67
[BMPyrr][TfO]	-2.95	1.88	4.83
[BMPyrr][DCA]	-2.95	1.67	4.62
[BMPyrr][TFSI]	-2.92	2.28	5.20
[BMPyrr][TFA] [*]	-2.85	1.35	4.20
[EMIm][TFSI]	-2.07	2.12	4.19
[MOEMMor][TPTP]	-1.95	2.03	3.98
[MOPMPip][TFSI]	-1.94	2.37	4.31
[MOEMMor][TFSI]	-1.93	2.75	4.68
[MOEMPip][TPTP]	-1.75	2.12	3.87
[S222][TFSI]	-1.30	2.21	3.51
[BMPy][DCA]	-1.25	1.71	2.96
[HPy][TFSI]	-1.22	2.74	3.96
[HPPy][TFSI]	-1.12	2.69	3.81

^{*} The EW of [BMPyrr][TFA] was carried out at 35 °C as the melting point is 31 °C.

Table 2.3 – Electrochemical windows calculated for various ILs at a cut-off current density of 0.5 mA/cm² using GC electrode at 25 °C. Taken from [34].

In particular, the ionic liquid 1-ethyl-3-methylimidazolium bis(trifluoromethylsulfonyl)imide (EMIM TFSI) has a good range of EW about 4.19 V and good physico-chemical compatibility with different solids therefore has been the choice of many different materials and devices [36, 34, 37, 38]. Moreover, Liebb *et al.* [36] recently worked with EMIM-TFSI as the choice of ionic liquid gating for InAs NWs hence we chose this IL for our characterization as shall be seen in section 4.3 and compared with their results too. The chemical structure of EMIM TFSI and a picture of a bottle holding it is shown in figure 2.8.

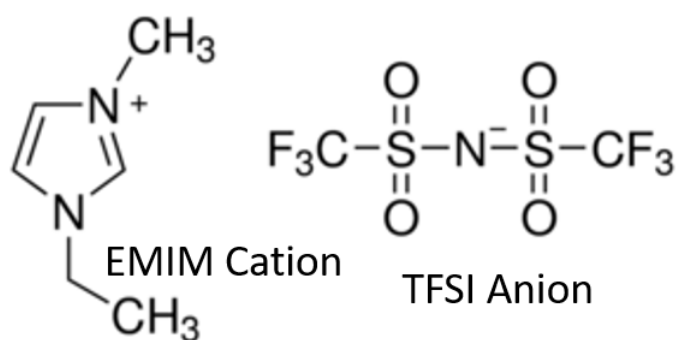


Figure 2.8 – Ionic liquid specifications.

2.3 Sensing Platform : Electrochemical transducer

When an electrochemical sensing system is placed in a solution, a transducer element covered with recognition elements interacts specifically with target analytes primarily through chemical reactions. This chemical event is transformed into an electrical signal via the transducer element as shown in figure 2.9.

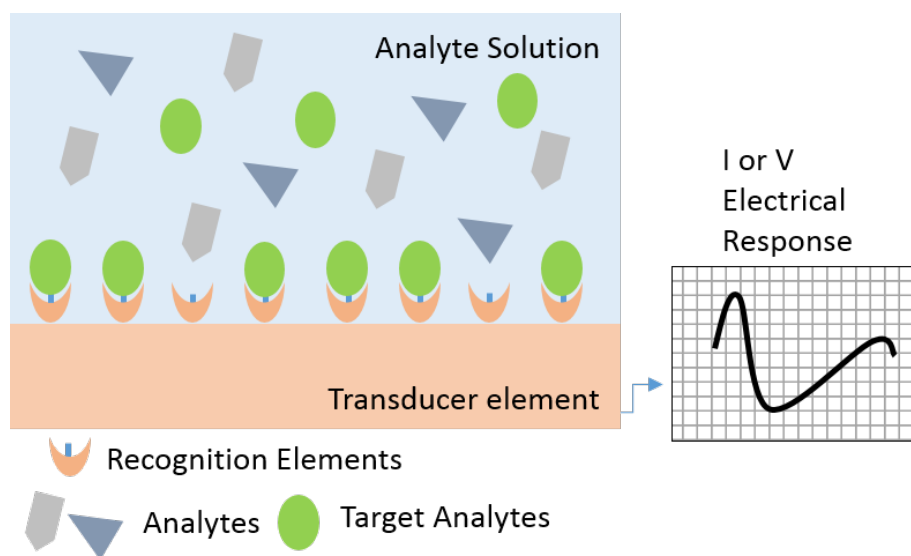


Figure 2.9 – Principle of electrochemical sensing.

The system can be interpreted with ohm's law as given in equation ???. The essence of the measurement lies in either applying a potential and studying the current or vice versa.

$$V = i * Z \quad (2.5)$$

where V = voltage, i = current, Z = impedance

According to the different input controls and readout signals i.e V , i or Z electrochemical sensing is mainly classified into potentiometry, amperometry, conductometry and impedimetry. For a detailed classification be referred to other literature [39]. In potentiometry once an equilibrium is reached at the sensor surface then the potential difference between electrodes is read. In amperometry, a potential is applied through electrodes and the current resulting from redox reactions of species is measured. Conductometric conductivity measurements are taken at multiple frequencies. Whereas in impedimetry there are AC electrical signal changes at the surface mainly due to target conjugation that effect capacitive or resistive changes.

This thesis work focuses on using potentiometric techniques so ion selective electrodes (ISE) are discussed and gradually focus shifts to FET based sensing one of the applications

of this thesis work.

2.3.1 Ion selective electrodes

Among electrochemical sensors, ion selective electrode (ISE) have been an important type due to enabling real time measurement of both positive and negatively charged ions for wide concentrations in a relatively cheap and easy to operate manner. The basic constituents of an ISE sensing system are shown in figure 2.10. It consists of a sample solution, two (or three) electrodes, electronic control and measurement equipment. A reference electrode (RE), a working electrode (WE) and a counter electrode (CE) are the three electrodes. In a two electrode configuration CE is tied to WE. RE enables to have a constant potential in the solution under test. Electrochemical transduction happens at the WE. And the CE along with the WE form the circuit over which the current/voltage is applied or measured. In this system following Ohm's law, V is the potential of WE with respect to RE, whereas i is the current flowing through the WE and the solution and Z is impedance through the same.

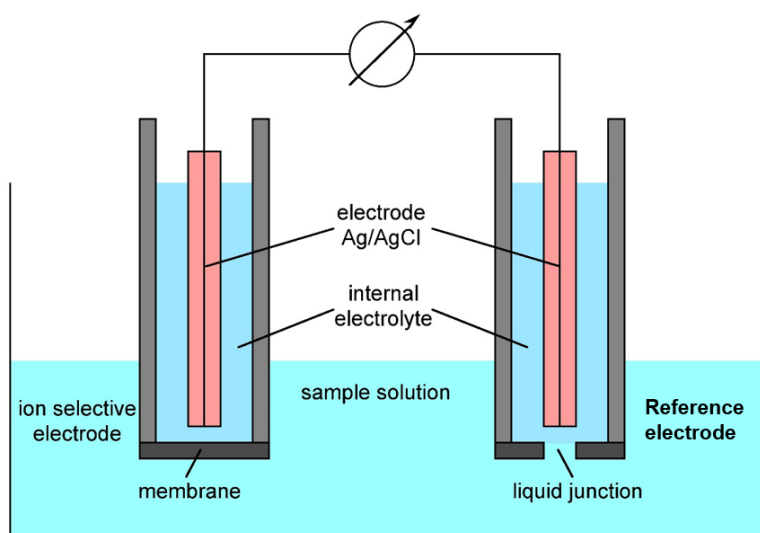


Figure 2.10 – Main components of a potentiometer cell measurement setup with a reference electrode and ion selective electrode.

The ISE is made up of a silver wire, coated with silver salt (AgCl) and immersed in a KCl saturated internal electrolyte and an ion sensitive membrane (ISM). The ISM in contact with the sample solution permits only 'specific' ions to cross and enter the electrode because of a diffusion gradient. On the other hand, the reference electrode consists of a metal wire immersed in an internal solution i.e also KCl saturated and a porous frit instead of the ISM that does not let target ions enter. The RE forms the half cell that provides a stable potential dependent only on chloride ion concentration in the internal solution. The potential drop between the reference electrode and the electrolyte must be defined and stable. Finally, a

2.3. Sensing Platform : Electrochemical transducer

very sensitive voltmeter using low noise cables is connected between ISE and RE that can measure millivolts of potential change. ISE converts the ionic activity of specific ions dissolved in an analyte solution into an electric potential with a logarithmic relation. At equilibrium condition, the potential of the ISM is dependent on the target ion concentration outside the membrane and is dictated by an equation known as the Nernst equation. This is shown in equation 2.6.

$$E = E_0 + \frac{2.030RT}{nF} \log C \quad (2.6)$$

where E is the potential difference across ISM, E_0 is standard-state reduction potential constant to an ISE, R is the universal gas constant (J/mol.K), T is temperature (K), n is ionic charge or valency of ions, F is Faraday constant (C/mol) and C is the concentration of the ionic charge.

While the earlier equation resonates more with chemists, physicists will appreciate the one in equation 2.7.

$$E = E_0 + \frac{2.030kT}{nq} \log C \quad (2.7)$$

where k is the universal boltzmann constant, q is the elementary charge.

One must keep in mind that the measured voltage is not necessarily positive when target ions are present and not necessarily zero when target ions are absent. Since the potential difference measured is a sum of all voltages in the circuit (other junctions) and ISE membrane potential. That is why the sensitivity of ISE is characterized to validate functioning of ISE. The sensitivity of the ISE is defined in the slope of the electrode i.e. a change in potential of electrode (ΔE_{ISE}) per decade change in ion concentration. This theoretical sensitivity limit known as nernstian limit is 59.4/n mV/dec at temperature of 300 K. Where n is the valency of the ions. Therefore for monovalent ions like H^+ , K^+ the nernstian limit is 59.4 mV/dec whereas for divalent ions like Ca^{2+} the limit is 29.7 mV/dec.

However there are several limitations of ISEs that should be addressed in order to increase their applicability.

1. No ISM perfectly allows target ions only, so that unwanted ions can pass.
2. For high concentrations inter-ionic interaction can reduce ionic mobility and there can be a difference between bulk and surface ion concentrations.
3. ISE's given their size cannot handle very low sample volumes.
4. An ISM is supposed to permit only a particular ion to pass through therefore to build a bigger system with multiplex ion detection the setup starts to become really impractical.

5. The presence of liquid contacts internal solutions etc limits the applicability/miniaturization.
6. The internal liquids are susceptible to evaporation with changes in sample temperature and pressure.

There is a rising need for portable analytical instruments utilizing very low sample volumes for analysis on site. And there is a huge requirement to improve reproducibility, stability of measurements for these solid-state ISEs. While points 1,2 above are inherent limitations of ISEs, points 3,4,5,6 can be addressed using solid state ISEs presented in the section 2.3.1. The limitations of SS-ISE can further be enhanced by using FET sensing as will be seen in section 2.3.2.

Solid-state ISEs

The basis of SS-ISE is to replace the liquid contact between ISM and internal electrode with a solid contact, i.e. an electronic substrate to perform ion to electron transduction. This solid contact is known as a solid state conductive material (SSCM). This SSCM can be anything ranging from semiconductors to carbon to metals wires. One side of the ISM is in contact with the SSCM while the other side is in contact with the sample solution. In figure 2.11 is pictured a schematic of such a SS-ISE with a sensing oxide for H^+ ion concentration though the RE is not a solid state one in this case.

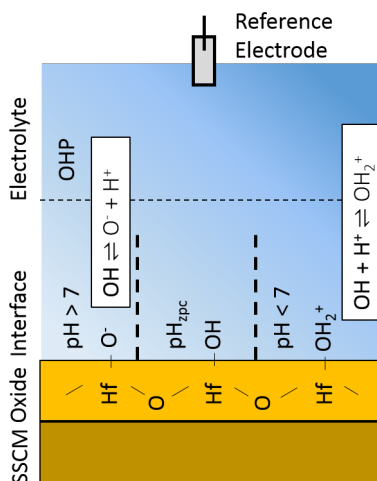


Figure 2.11 – Solid state ISE with a oxide layer behaving as ISM for H^+ ions.

Hirata *et al.* proposed an all SS-ISE made up of a Pt wire coated with a Cu_2S impregnated silicone rubber sensing membrane [40]. After this Cattrall *et al.* proposed the first coated wire electrode with an ionophore as the sensing membrane [41]. Solid contacts based on coated wire electrodes were simple in design but not reliable because of the interruption of

2.3. Sensing Platform : Electrochemical transducer

ion-to-electron transformation at the blocked solid contact/membrane interface [40]. It was found that none of the charged species transferred between membrane and metal contact so it was at best a capacitive interface. And with small interfacial area, the noise level was high and also large signal drifts were noticed. So clearly there was room for more improvement as the stringent conditions for SS-ISEs that had been laid out in 1970s by Nikolskii *et al.* in order to be stable and reliable were not achieved [42]. These stringent conditions are as follows:

1. Should have reversible transitions from ionic to electronic conduction
2. Surfaces should ideally be non-polarizable with high exchange current densities
3. Side reactions should be absent.

The community advanced SS-ISEs with novel solid contact materials, a better understanding of transport and accumulation of water in membranes, control of transmembrane ion fluxes and development of novel sensing platforms. Further, conducting polymers and high-surface area nanostructures as SS-ISEs have gained maximum academic attention towards commercialization of SS-ISE sensors [43, 44].

Electrical Double Layer

In order to describe comprehensively the working of ISEs we need to also discuss electrolyte-insulator-solid (EIS) conductive material interfaces. Whenever there is a fluidic interface an electrical double layer is formed [45]. As written, a double layer consists of two parallel layers of charge. The surface charge layer is the first layer where ions are adsorbed at the surface due to chemical interactions. The diffuse layer is the second layer where counter ions are attracted to the first layer screening other ions from them. This double layer causes a drop in the potential from the oxide surface into the electrolyte. Many models aim to describe how a potential is built at this interface from the early Helmholtz model [46], to Gouy-Chapman model [47, 48] and Stern model [49]. A summary of it is shown in the figure 2.12 (a) to (c).

- The Helmholtz layer treated the EDL as a capacitor and it postulates that only a single layer of counter ions called surface charge layer are adsorbed at the surface. It postulates that this charge itself neutralizes the surface charge in the oxide. Remaining ions of opposite charge are not known to contribute to the potential difference between the surface and the sample solution. Therefore the potential falls linearly from the oxide surface to the bulk of the solution as shown in figure 2.12 (a) and equation 2.8. The Helmholtz layer hypothesizes charges present as rigid layers which is not how nature is.

$$\psi_{surface} - \psi_{solution} = \frac{Q}{C} \quad (2.8)$$

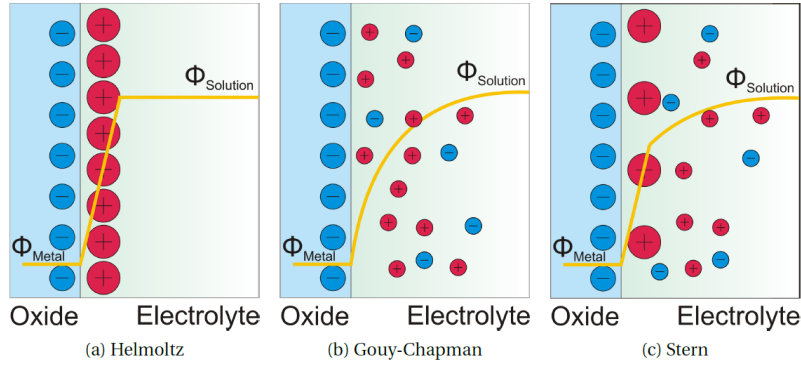


Figure 2.12 – EIS models a) helmholtz, b) Gouy-chapman, c) Stern. Taken from [50].

- In another model, Louis Georges Gouy and David Leonard Chapman independently proposed a diffuse double layer model. The potential at the interface of the charged surface is due to a given number of ions with a specific sign of charge and also an equal number of oppositely charged ions in the solution. In this case the counter ions are not rigidly held. The kinetic energy of the counter ions at the interface is decisive in the resulting thickness of the diffuse layer. Gouy and Chapman proposed that the change in concentration of the counter ions at the surface follows a Boltzmann distribution as shown in figure 2.12 (b) and in equation 2.9.

$$n = n_0 \exp(-ze\psi/kT) \quad (2.9)$$

where n here is the concentration of ions, n_0 is bulk concentration, z is charge on the ion, e is charge on a proton and k = universal Boltzmann constant as already defined. However, double layer thickness values calculated and those found experimentally do not match well with the latter being greater. This may have been related to the assumption that the Boltzmann distribution considers activity as equal to the molar concentration which is not entirely true. Moreover the ions were considered as point charges here so their concentration at the surface was much higher than in reality and led to large capacitance values than those experimentally measured.

- Stern layer model takes into account the location of the ions and hence the fact that these ions cannot approach the surface closer than a few nms. Taking into aspects from both Helmholtz model and Gouy Chapman model the Stern model is shown in figure 2.12 (c). The liquid has two distinct regions with different behaviours the first Stern layer with a linear potential drop and the diffuse layer with an exponential drop. The capacitance of the double layer is written as follows in equation 2.10.

$$C_{DL} = \frac{C_{diff}C_S}{C_{diff} + C_S} \quad (2.10)$$

2.3.2 FET based sensing

ISEs and ion sensitive field effect transistors (ISFET) have similar building blocks since the basis of sensing by conversion of ionic charge into electronic charge is the same. Ion sensitive field effect transistors have been first proposed and developed by Bergveld *et al.* in the 70's. In a simple explanation an ISFET is a MOSFET where the metal gate is replaced by a reference electrode and liquid electrolyte with analyte ions which now contacts the gate oxide. The gate oxide is the sensing oxide with sites that have an affinity for the target ions to bind. Therefore, the concentration of analyte ions through the oxide affect the surface potential of the underlying semiconductor. The ISFET device transduces the surface potential to a current that is read out. Because of a high impedance input in FET, the voltage input(surface potential) is transferred faithfully to a low output impedance. This is a significant advantage of FET sensing over ISEs since background noise is drastically reduced thanks to maximum distance reduction between the ion selective membrane (sensing oxide) and amplifier (semiconductor). Among potentiometric techniques, field effect transistor (FET) based sensing has attracted considerable attention for the following reasons -

- Handling low sample volumes
- Capability for miniaturization to move towards low power systems
- Abilities to build arrays for parallel, multiplex ion detection
- Fast response time
- Seamless integration with computation electronics owing to CMOS compatibility hence low overall cost
- Improvement in signal to noise ratio given that voltage input is transduced thanks to high impedance input and low impedance output

When the metal gate is replaced with an electrolyte and a reference electrode the potential drop from the reference electrode to the semiconductor material must now take into account the additional junctions as shown in figure 2.13. When a fixed voltage is applied to ϕ_G , a certain voltage drops at the first double layer to the electrolyte ($\Delta\phi_{EL}$) and further drops at the next double layer at the surface of sensing oxide ($\Delta\phi_S$). In turn, this affects the threshold voltage of the device. When a potential is applied through the reference electrode, the liquid there is a change in the metal semiconductor workfunction(ψ) and therefore the threshold voltage. A reference electrode is used to maintain a potential in the liquid hence the difference in liquid gate voltage (V_{LG}) is a measure of change in surface potential. Now let's take a look at the electrolyte-insulator-semiconductor interface and draw the potential distribution when a reference voltage is applied as shown in figure 2.13.

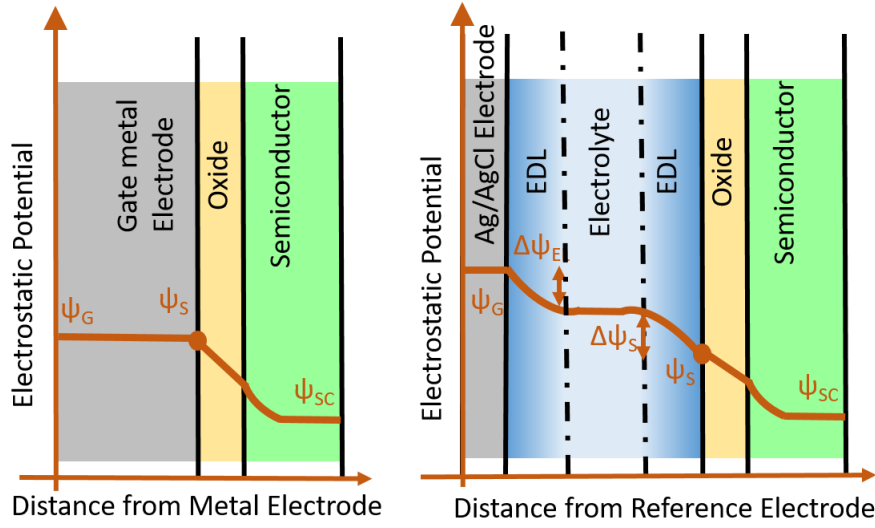


Figure 2.13 – Interface and potential drop with distance in (left) metal gate electrode and (right) reference electrode in liquid gating.

Apart from only silicon the materials used to demonstrate ion sensing, bio sensing, gas sensing have diversified into carbon nanotubes, graphene, 2D materials and III-V semiconductors. Reproducibility, reliability, non-CMOS compatibility are constant issues in such devices. Nevertheless, interesting electronic properties to complement silicon have motivated the choice of these materials for sensing. With the electronics revolution, transistors have mastered economies of scale to be commercially very viable, FETs in particular, are the leading choice in order to implement sensor technology. Advantages of FETs for sensing are their rapid measurement response, easy signal read-out and high sensitivity.

Sensitivity is explained through the site binding model and also through fast dynamic electrochemical exchange occurring at the ISFET surface. Nernst limit places a limit on the achievable voltage sensitivity to be 59 mV/pH for a monovalent ion as described in the paragraph after equation 2.7. Now, let's consider two FET devices with different sub-threshold slopes, 100 mV/dec and 60 mV/dec. Even though the voltage sensitivity in both cases say reaches the Nernst limit of 59 mV/pH, the readout sensitivity differs. Readout sensitivity is defined in equation 2.11. Where I_0 is the initial drain current value before the detection and I_1 is the drain current value changed after interaction with sensor molecule. Readout sensitivity response is defined as the relative change in the drain current due to the sensing event.

$$S_{Readout} = \frac{I_0 - I_1}{I_0} = \frac{\delta I_D}{I_D \delta V_G} \delta V_G = \frac{\delta V_G}{SS} \quad (2.11)$$

2.4 Motivation of InAs architecture for computing and sensing

The figure 2.14 encapsulates the intersection of reasons for why InAs architectures are interesting both towards computation and sensing. Except the first property that is geometry dependent, all the parameters in the middle (in grey) are tied to InAs material. It is for these reasons that there has been exploration of InAs nanostructures for sensing and widely explored are the NW architecture. The case for interests in TFETs for biosensing has not been experimentally demonstrated in InAs devices but will be explained in chapter 5 and in the section 5.2.3 as a future perspective.

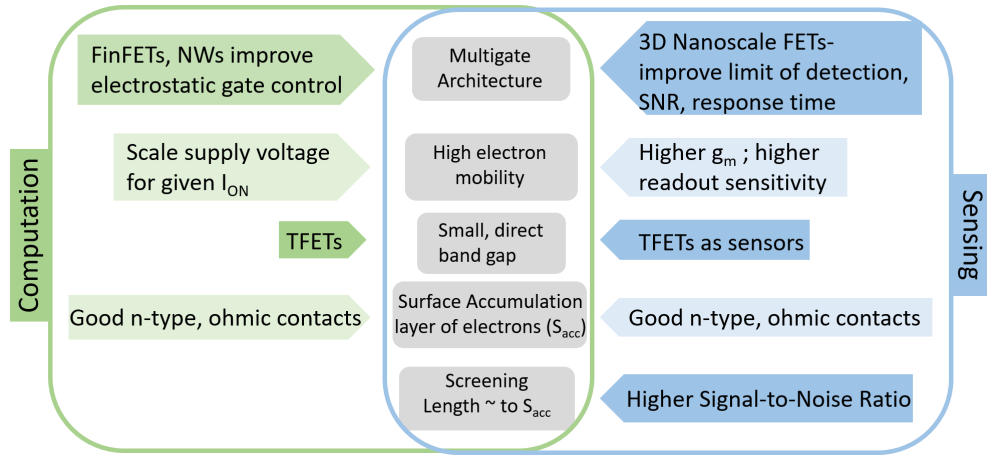


Figure 2.14 – Motivation for InAs architecture from a computation and sensing perspective.

2.5 III-V nanostructures for sensing

We review most works using InAs nanostructures for chemical or biological sensing. Leading from these works, we shall point out in detail the choice of material (InAs) and other design considerations in our system in the section 2.6. Among 3D nanostructures NWs have gained significant attention as high performance nanoelectronic sensing systems [51]. InAs NWs especially have gained significant attention to sense chemical or gas molecules such as NO, NO₂, H₂O, IPA(Iso-propanol), ethanol, acetone and even biological molecule such as proteins, mammalian cells and neuronal cells [52, 53, 54].

Du *et al.* in 2009 were among the first to report gas sensing properties of InAs NWs [52]. They observed change in conductance of the InAs NW-FET for different adsorbed gas molecules such as O₂, NO₂, NH₃, CO as shown in figure 2.15. They also report that adsorbed molecules not only induce charge transfer but also increase carrier mobility. This goes to show that the surface states in InAs NWs play a crucial role in the transport properties. However, no particular sensing oxide other than the native InAs -oxide layer was used and further information on hysteresis is not provided, a back gate was used to bias the channel as

necessary [52].

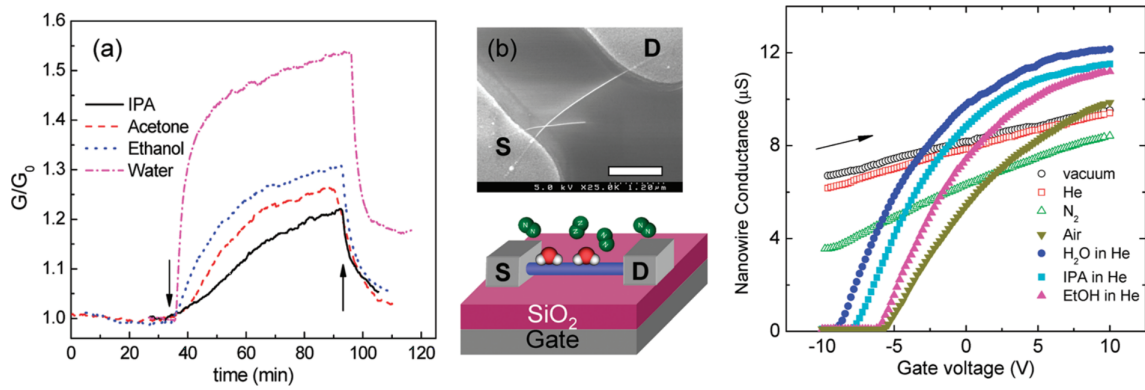


Figure 2.15 – Left to Right: Change in conductance with different gas molecules, scanning electron microscope (SEM) image of NW structure and change in NW conductance as a function of back gate voltage. Rearranged from [52]. Scale bar is 1.2 μm

In 2010, Offermans *et al.* demonstrated an interesting concept of using vertical InAs NW array for gas detection for the first time [55]. In fact, InAs NWs were fabricated gold-free and contacted in their as-grown locations in an air bridge construction leaving a lot of surface ready for gas absorption as shown in figure 2.16. The NWs were grown without Au catalyst but they were grown on non-standard substrates i.e indium phosphide instead of silicon. With NW diameter in the range of 50 nm to 100 nm and lengths of about 3 μm they reported devices with a high yield and are able to make many statistical analyses of the NW properties. The devices are very sensitive with detection of NO_2 down to concentrations below 100 parts per billion (ppb) at room temperature. Though selectivity was not tackled in this work, they addressed this by functionalizing the surface with metalloporphyrin (Hemin) in a subsequent work in 2012 [53].

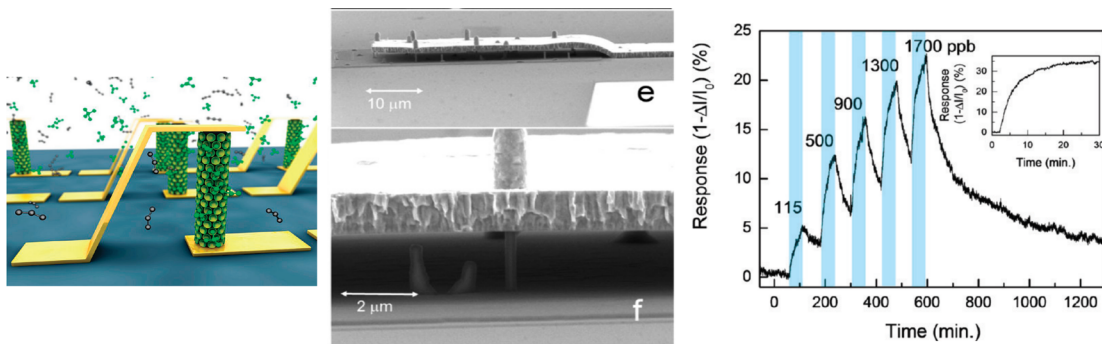


Figure 2.16 – Left to Right: Concept of air bridge InAs NW sensor, in e) SEM images of the contact over many vertical InAs NWs, f) a zoom of the NW, metal contact and response of NW array to different concentrations of NO_2 down to 9 ppb of NO_2/N_2 in inset. Rearranged from [55].

In 2012, Dedigama *et al.* highlighted the performance of the two dimensional electron gas (2DEG) at the surface of InAs [56]. With Hemin functionalization to enable selective interaction with NO molecules they demonstrated InAs in a planar resistor configuration as molecularly controlled resistors (MOCSEs) and also proposed a chemical model for the electron transfer from the 2DEG of InAs to the iron center of the Hemin, which reduces Fe^{3+} to the higher NO molecule affinity state of Fe^{2+} . The 50 nm to 100 nm thin undoped InAs films were grown directly on GaAs substrates by molecular beam epitaxy (MBE) [56].

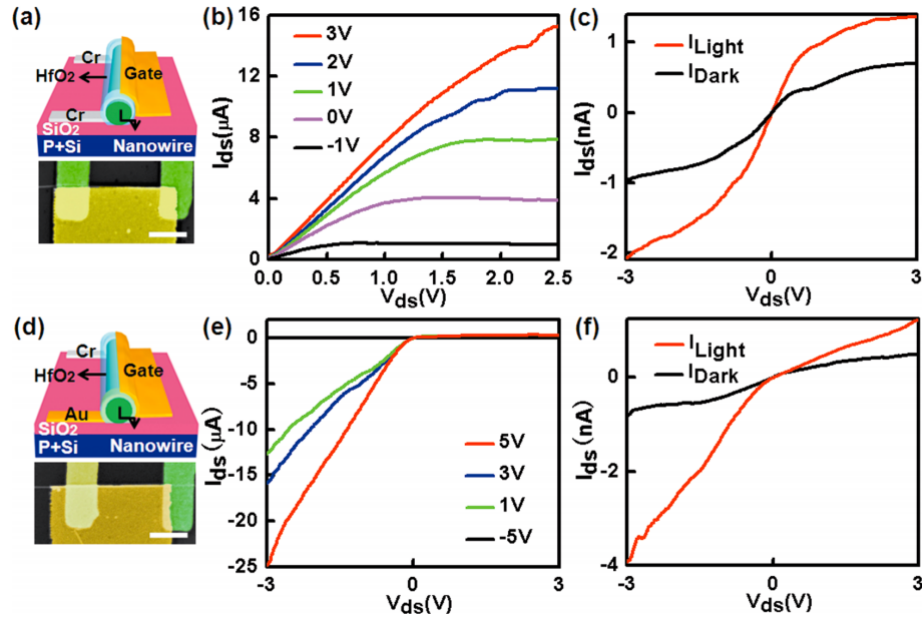


Figure 2.17 – (a)-(c) Show schematic, SEM image of Ohmic-Ohmic contacted devices and their photo response behaviour at different gate voltages in light and in dark conditions, (d)-(f) show schematic, SEM image of Ohmic-Schottky contacted devices and their photo response behaviour at different gate voltages in light and dark conditions. Taken from [57].

Miao *et al.* in 2014 utilized not just the electronic properties of InAs but also the optical properties of InAs i.e. detection of near-infrared wavelengths of up to $\sim 1.5 \mu\text{m}$ [57]. In order to suppress negative effects such as surface defect states and atmospheric molecules, the InAs NW photodetectors were also half-wrapped with a top gate dielectric using 10 nm HfO₂. And it was shown that Schottky-Ohmic contact configuration were about 300% more photoresponsive than Ohmic-Ohmic contacts for source-drain metallization. This is illustrated in figure 2.17. In this case also the InAs NWs were first fabricated on GaAs substrates and then transferred to silicon substrates. The growth lengths were about $7 \mu\text{m}$ and diameters $\sim 40 \text{ nm}$.

Zhang *et al.* also demonstrate sensitivity of InAs NW FETs in H₂O vapor and NO₂, N₂

compared to vacuum in 2015 [58]. Despite hysteretic effects they show a systematic threshold voltage shift in the measured device transfer characteristics. The devices were grown without Au catalyst on a silicon substrate, then transferred to another Si substrate to make horizontal devices as shown in figure 2.18. The native InO_x layer behaves as the sensing oxide.

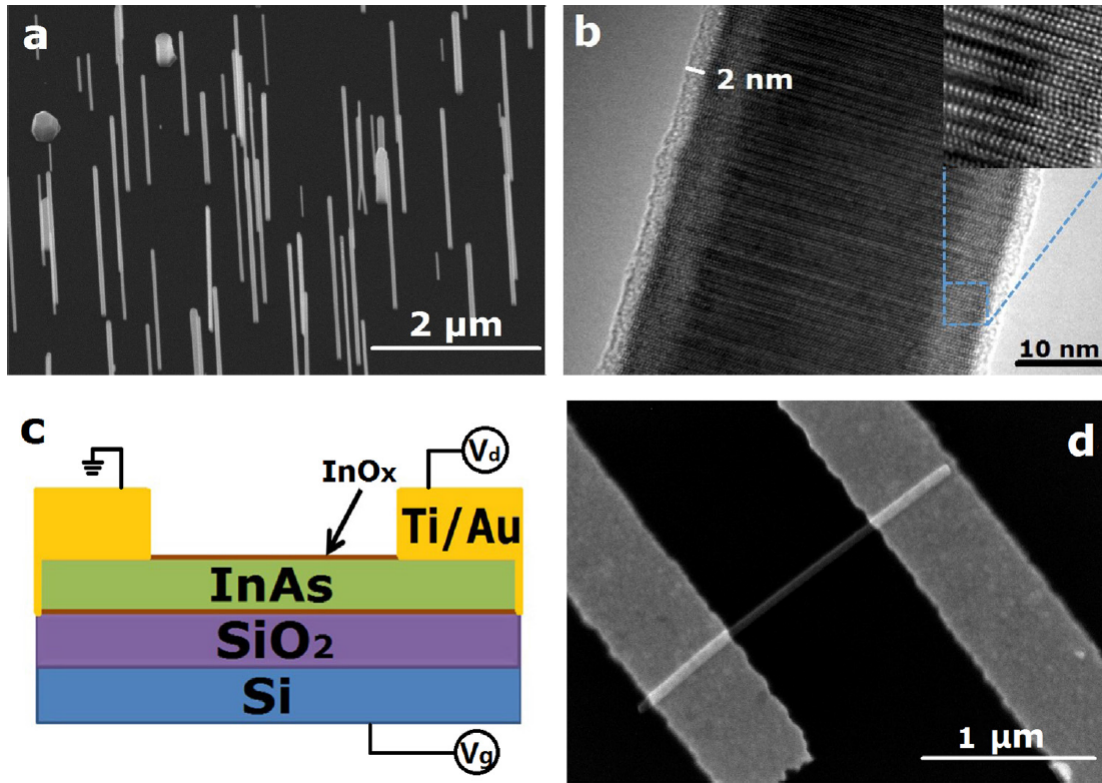


Figure 2.18 – a) An SEM image of grown NW array. b) TEM image of the InAs NW. c) schematic of complete structure. d) SEM image of a typical measured device. Taken from [58].

Tseng *et al.* showed InAs NW sensitivity towards volatile organic compounds i.e vapor containing acetic acid, 2-butanone and methanol [59]. They used gold droplets to catalyze InAs NW growth on GaAs substrates and then transferred the grown NWs to silicon substrate. The method reports that the transfer of NWs based on contact printing [60] is compatible with wafer scale assembly. This is very good since it opens the possibilities for highly ordered, dense regular arrays. However, the placement density and accuracy for contact printing are yet to match that of top-down fabrication. The average diameter of the NWs fabricated was 31 ± 7 nm and the transfer characteristics are shown in 2.19.

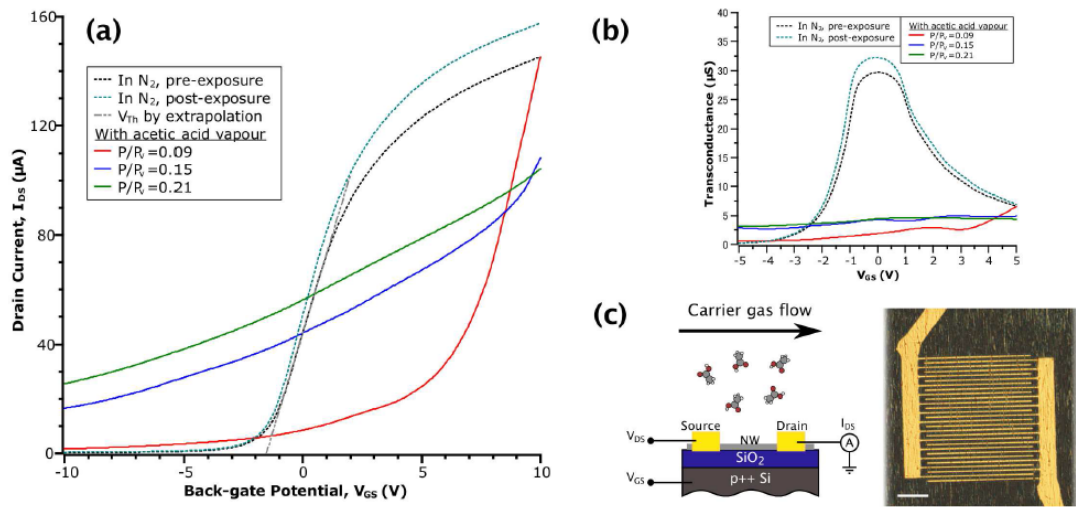


Figure 2.19 – (a) Transfer characteristics of InAs NW FET in different vapor environments. b) Transconductance curve obtained from differentiation of data in (a). (c) Schematic of NWFET structure (left) and optical image of a complete device (right). Scale bar 20 μm . Taken from [59].

So far we looked at work with chemical sensing of various gas molecules and volatile organic compounds. However we shall now see examples of ion sensing and biological molecules studies i.e protein and cell based works.

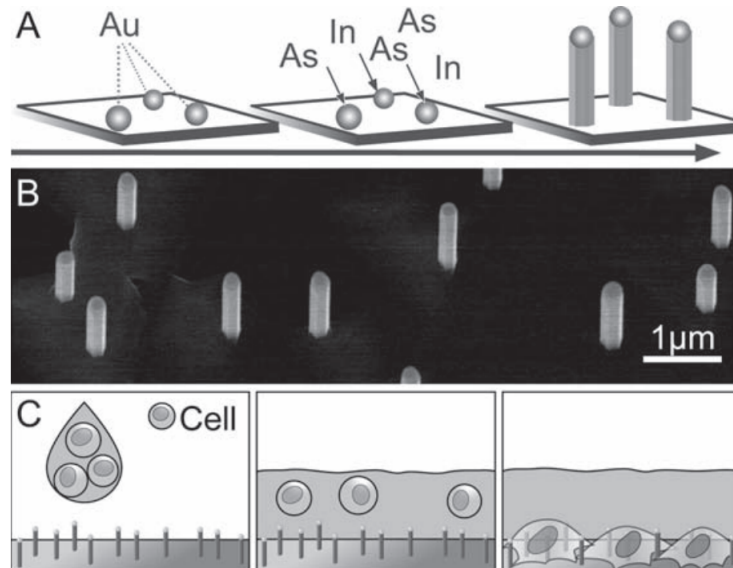


Figure 2.20 – Use of vertical InAs NW array to culture mammalian cells and study their cell function. Taken from [54].

Berthing *et al.* used arrays of InAs NWs using gold atom as catalysts grown on InAs substrates to culture mammalian cells and study their functions as shown in figure 2.20 [54]. The critical cell functions and pathways such as cell adhesion, membrane integrity, intracellular enzyme activity, DNA uptake, cytosolic and membrane expression and neuronal maturation pathway were shown to not be damaged. Essentially the compatibility of InAs material and NW geometry towards human embryonic kidney cells and neuronal cell culture has been re-established through these investigations [54]. Fluorescence imaging was used as the technique to characterize the cell-function properties. Rostgaard *et al.* explain that protein microarrays are important tools for protein assays [61]. However as the transition from micro scale to nanoscale enables miniaturization of the platforms, reduces material consumption, it also increases challenges of reduction in fluorescent signals and compatibility issues with complex solutions. The vertical NW arrays used as a backdrop to immobilize proteins can overcome some of these bottlenecks as they provide large surface area. Fluorescence detection of proteins using NW arrays allows quantitative measurements, spatial resolution tracking individual NWs, on chip extraction and functional analysis and multiplexed detection of different proteins as shown in the figure 2.21. The NWs are fabricated on silicon substrate with gold catalyst reaching lengths of up to $10\text{ }\mu\text{m}$ and diameters down to 40 nm . For a typical NW the aspect ratio is easily 50 ($5\text{ }\mu\text{m}$ length to 100 nm diameter).

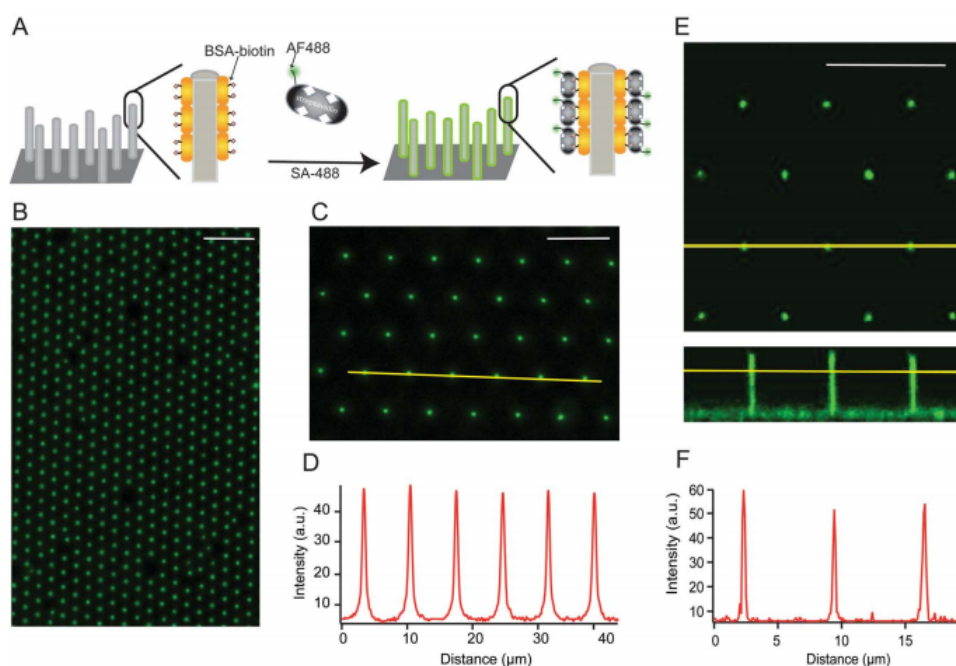
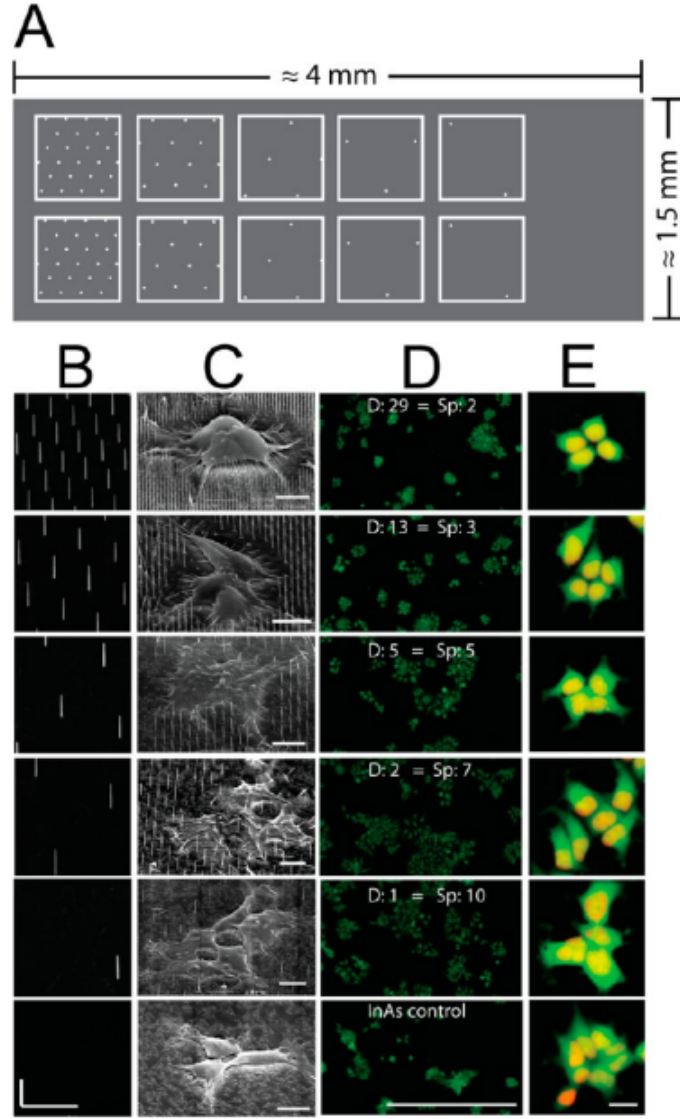


Figure 2.21 – Fluorescence detection of protein immobilized on NW arrays. A) Scheme of functionalization of NW arrays with BSA-biotin and SA-488. B) wide field image showing the spacing of NWs is $2\text{ }\mu\text{m}$. C) wide field image showing spacing of NWs is $7\text{ }\mu\text{m}$. D)- F) shows intensity of corresponding yellow lines marked in the figure. Taken from [61].

In 2013, Bonde *et al.* carried out further studies of cell function of Human embryonic kidney (HEK-293) cells by varying InAs NW density [62].



of

Figure 2.22 – A. A schematic image showing the various NW density areas of vertical InAs NWs. White squares are of $500 \times 500 \mu\text{m}^2$ with 2,3,5,7,10 μm spacing between NWs. B. Tilted SEM images of the density of nanowires. C. Morphology differences on the different NW densities where small, rounded forms seen on the high density wires and flat, spread out form on lower densities. D. & E. Living cells signature is seen through maintaining esterase activity (green = calcein-AM) and cell morphology qualitatively similar in red i.e DRAQ5 nuclear label staining. Taken from [62].

Using NW arrays for a broad range of NW densities that demonstrate its cell-promoting surface that affects cell division and focal adhesion up-regulation. Essential cell functions

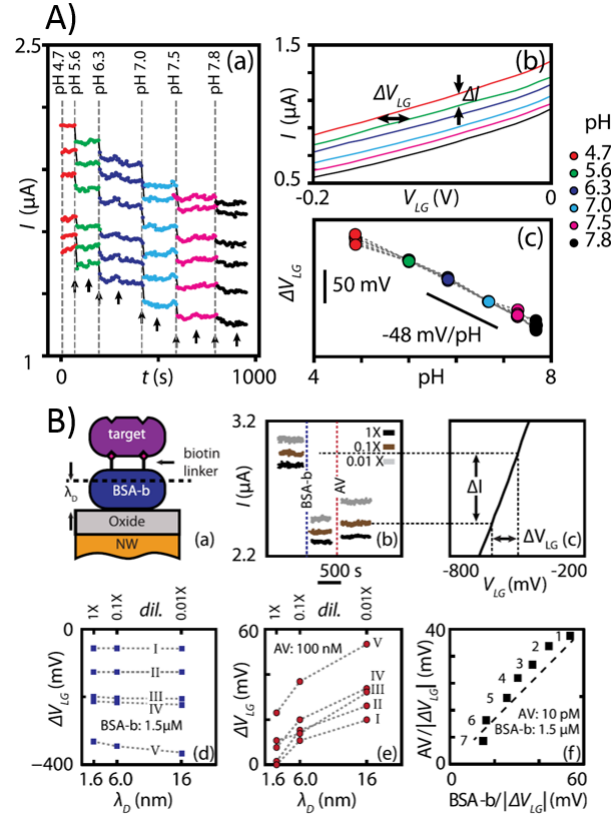


Figure 2.23 – A. Sensitivity of InAs sensor towards pH 4.7 to 7.8. B) Sensitivity of functionalized InAs NW towards avidin protein. Image from [63].

of viability, division, morphology and adhesion are shown to not be impaired by this culture method. This fundamental study provides great insights into how NW density is a very important parameter to take into consideration for developing NW-based platforms for cellular applications as shown in figure 2.22. Upadhyay *et al.* were among the first to demonstrate charge based chemical and biological species FET sensing in InAs NWs [63]. They fabricated InAs NWs on InAs substrate using gold catalyst and MBE then later transferred to Silicon substrate. However Al_2O_3 is used as the sensing oxide which enables to achieve a good sensor sensitivity of 48 mV/pH. Moreover they showed that with further functionalization of the surface with biotinylated Bovine serum albumin (BSA-b) detection of Avidin (AV) down to 10 pM and streptavidin down to 100 nM was demonstrated. It is evident from the multiple works discussed that InAs is an interesting material for chemical and biological sensing applications. Though NWs have been leading chosen geometry due to their facile growth methods other 3D geometries shall be interesting to explore such as ribbon, fin structures especially if there are more motivations such as non-transfer of substrates during processing using mature Silicon conventional processing techniques. It cannot be emphasized enough that the platform to readout these signals and the sensing needs to be the same to ensure a faithful transfer of signals. To the best of our knowledge in these fundamental studies this is yet to be addressed.

2.6 Choices in our System

In this section we shall motivate in detail the choices we made in our system - InAs material properties, geometry structure relevant for sensing, InAs on silicon integration approach to enable scalability. Moreover all these considerations are also advantageous for future novel nanoelectronic device implementations such as tunneling FETs as sensors. This will be discussed in the chapter 5.

2.6.1 Indium Arsenide

Electronic Properties

InAs is a very popular compound semiconductor in the electronics and photonics industry. A comparison of properties for silicon and InAs is shown in table 2.4. Strikingly visible is the high electron mobility of InAs in comparison to silicon. This presents opportunities to greatly scale down supply voltage but still have high drain currents. Moreover the extremely low effective mass of electrons and the small direct band gap for InAs over Si are advantageous for novel device architectures such as tunneling FETs, electron-hole bilayer Tunneling FETs [64, 65, 66] which have unique advantages as sensors and shall be discussed further in chapter 5.

Prop.Mat.	Si	InAs
Electron bulk mobility($\text{cm}^2/\text{V}\cdot\text{sec}$)	1400	40 000
Electron effective longitudinal mass ($/m_0$)	0.98	0.023
Hole bulk mobility($\text{cm}^2/\text{V}\cdot\text{sec}$)	450	500
Light hole effective mass ($/m_0$)	0.16	0.026
BandGap (eV)	1.12	0.36
Effective conduction band density of states (cm^{-3})	$3.2 \cdot 10^{19}$	$8.7 \cdot 10^{16}$
Effective valence band density of states (cm^{-3})	$1.8 \cdot 10^{19}$	$6.6 \cdot 10^{18}$

Table 2.4 – A comparison of silicon & InAs electronic properties.

InAs has a direct band gap of about 0.36 eV and for intrinsic InAs the Fermi level is located very close to the conduction band (E_C) just 0.04 eV below it as visualized in figure 2.24 with data taken from [67]. Hence intrinsic InAs can as well be considered n-type InAs. At room temperature, InAs has an intrinsic carrier concentration of $1 \cdot 10^{15} \text{ cm}^{-3}$. In order to increase the number of charge carriers at room temperature ions should be implanted that either contribute an electron (n-type) or a hole (p-type). Accordingly the Fermi level shifts towards conduction or valence band. The work function of the metal (ϕ_M) and a n-type

semiconductor (ϕ_{nSC}) decide the type of contact at the metal-semiconductor junction.

$$\phi_M > \phi_{nSC} \Rightarrow \text{Schottky} \quad (2.12)$$

$$\phi_M < \phi_{nSC} \Rightarrow \text{Ohmic} \quad (2.13)$$

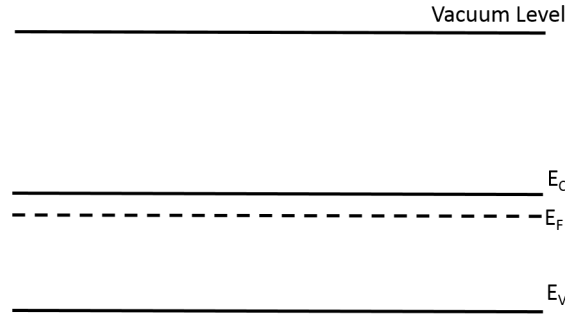


Figure 2.24 – Energy Band Diagram of intrinsic InAs.

Let's delve into the metal-n type InAs contact, at first when the two materials are isolated the bands are as shown in the left portion of figure 2.25. When they are brought into contact because of the difference in Fermi energy (E_F) levels, electrons will flow between the metal and semiconductor until E_F levels are aligned. Electrons flow from the lower work function material (metal) to the material with higher work function (n-InAs) causing E_F on the n-InAs to move up as shown in the right portion of figure 2.25. As there is no barrier for electrons to flow from n-InAs to the metal the type of contact created is Ohmic.

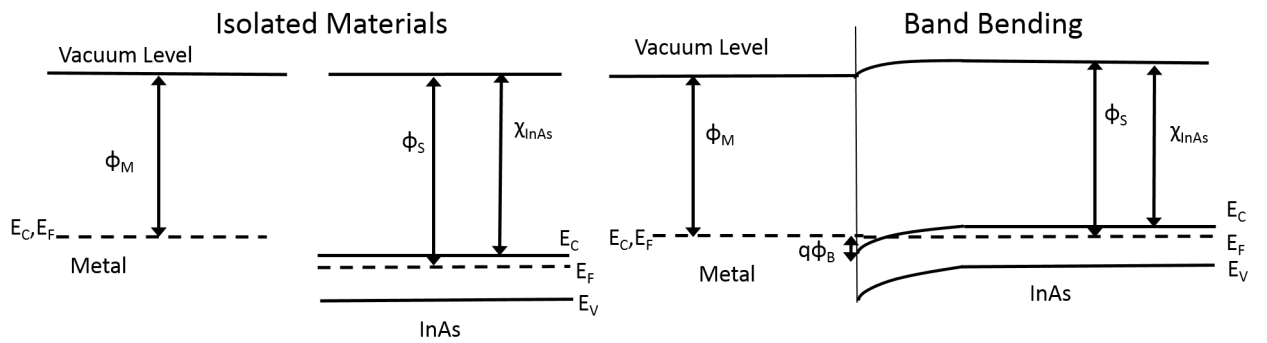


Figure 2.25 – Energy Band Diagram of intrinsic InAs.

Surface Accumulation Layer So far while explaining contacts we took into account the differences between the bulk of the materials. However, the properties at the surface, a few

atomic layers thick can influence greatly the band bending as is the case for InAs. InAs is well known for this surface accumulation layer of electrons which is induced by donor like intrinsic surface states whose energy is determined by surface reconstructions [67]. This layer enables very good, non-alloyed n-type Ohmic contacts with metals but also opens many new technological opportunities. It was studied by Noguchi *et al.* that on a clean surface of InAs(100) grown with MBE that depending on how the surface is cooled the electronic density of this layer changes [67]. At the end of MBE, the surface is cooled and this is carried out under a flow of arsenic flux or indium flux. The chosen gas flow affects band bending as visualized in figure 2.26 [67]. They reported that for As-stabilized surfaces the electron density in the accumulation layer was approximately $1 \times 10^{12} \text{ cm}^{-2}$ and for In-stabilized surfaces was lower at $5 \times 10^{11} \text{ cm}^{-2}$.

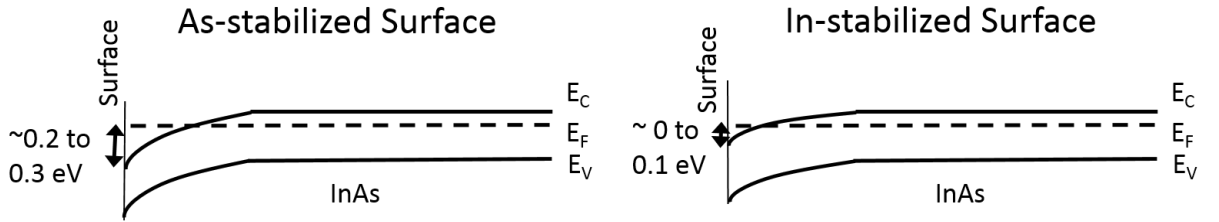


Figure 2.26 – Energy Band Diagram of intrinsic InAs. Drawn with information taken from [67].

Moreover, during studies on metal-semiconductor interfaces it was indeed seen that the barrier height (ϕ_B) was not dependent on the metal work function [68]. In fact, in p-type InAs there was an inversion layer (electron layer) at the surface and the Fermi level was above the conduction band edge at the interface. Due to this Fermi level pinning, ϕ_B is less than or almost equal to zero enabling good ohmic contacts.

Energy Harvesting

A report in 2013 demonstrated an exciting property of energy harvesting through fluidic flow in InAs NWs. However, this property is not exclusive only to InAs [69]. They demonstrated that when an InAs NW FET was placed in a microfluidic channel it could detect the flow rate change and harvest the fluid flow energy for electric power generation. The principle is illustrated in figure 2.27. It was shown that when no drain voltage was applied the ionic flow in the microfluidic channel could generate $\sim \text{mV}$ electrical potential or $\sim \text{nA}$ electric current in the InAs NW with ml/h increase in flow rate due to charge dragging effect. Experimental studies in other nanostructures/substrate have experimentally shown that a net conductance or surface potential difference can be generated in the presence of fluid flow in silicon NW FET [70], carbon nanotube [71, 72].

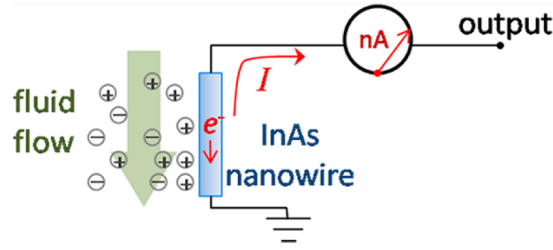


Figure 2.27 – Principle showing energy harvesting from fluidic flow by InAs NW wires. Taken from [69].

III-V on silicon integration

The premise for most sensor technology using silicon or InAs NWs apart from the common geometry arguments for sensing is their attractiveness in enabling low noise signal transduction and integration into miniaturized systems. However this is not achievable unless the same manufacturing technology is used for both computing and sensing platforms[6]. This implies that we should have control over aspects such as device shape definition, device placement and density which are typical strengths of top-down fabrication. Whereas seen in section ?? almost all the InAs NWs devices were not built in such a top-down paradigm but instead grown on non-Si substrates and eventually transferred to Si substrates, involved growth catalysts that could behave as unwanted dopants, used heavy customization techniques and were not CMOS compatible. There is space for a III-V technology to help integrate both the computing and sensing functions and build truly integrated, miniaturized systems. With this context we speak about III-Vs on Silicon in this section. As discussed in section 2.6.1 III-Vs are touted for their superior electron properties over Silicon i.e. n-channel devices but this is only half the story as p-channel counterparts based on semiconductors such as Ge or InGaSb require mention. Silicon as a substrate has been the leader of the electronic industry because of its economic viability therefore combining both these n & p devices on it shall meet successful integration criteria to build next generation devices. However the lattice constants of the n-type and p-type materials vary greatly rendering their combined integration an ongoing issue.

Silicon and InAs have a mismatch in their lattice constants, thermal expansion coefficients and also their crystal structures. A comparison of these crystal properties for Si and InAs is given in table 2.5.

There are global growths and local growth integration approaches as illustrated in figure 2.28 (a)-(d). Figure 2.28(a)-(b) can be classified as global integration techniques and figure 2.28(c)-(d) as local integration techniques. Among the global ones is blanket epitaxy growth where using thick buffer growth layers the differences in the lattice constant mis-matches between silicon and the III-V are relaxed. A major drawback of this technique is using multiple and thick growth layers for the transition to III-V [73, 74]. As a result the transfer of the

2.6. Choices in our System

Property	Si	InAs
Lattice Constant	5.431 Å	6.058 Å
Coefficient of thermal expansion	$2.6 \times 10^{-6} \text{ }^{\circ}\text{C}^{-1}$	$4.52 \times 10^{-6} \text{ }^{\circ}\text{C}^{-1}$
Crystal Structure	Diamond	Zinc Blende

Table 2.5 – A comparison of Si & InAs crystal properties.

thin epitaxial layer to another oxidised silicon substrate is preferred to build devices [75]. One global integration technique that seeks to reduce the thickness of the buffer layers to make process more CMOS compatible is based patterning trenches into the substrate as shown and growing III-V [76]. The aspect ratio trenches behave as dislocation sinks enabling strain relaxation in much thinner layers. The defect density is already well reduced with this technique with threading dislocation densities on the order of 10^9 per centimeter square reported [76]. On the other hand, local integration techniques are also researched based on vapor-liquid-solid phase epitaxy using a catalyst such as gold to directionalize growth and selective area epitaxy. While this catalyst rests on the top of the NW, the NW grows in the upward direction [77, 78, 79]. High yields of NWs free from structural defects were indeed obtained with selective-area growth (SAG) and this using bottom-up technique. Though strain relaxation is efficient in these techniques, III-V nanowire growth directions are highly restricted to only certain planes such as (111) and there are constraints on attainable NW geometry. Template assisted selective epitaxy (TASE) efforts were focused on realizing lateral oxide templates in Silicon in order to address some of these constraints. Shown in figure 2.28 (d) is template-assisted selective epitaxy technique where in vertical nanotubes of oxide are fabricated down to a diameter of 25nm and filled by III-V material [80, 81]. We focus on TASE that is a scalable technique, growing III-Vs on virtually any substrate orientation is one of the big advantages hence it is compliant with industry-standard Silicon (100) substrates. Also III-V growths from polysilicon to build layered structures have also been shown using TASE. We build our devices in the horizontal TASE process for a local III-V integration.

For this work, the integration scheme chosen is based on lateral TASE. It combines aspects of bottom up and top down nanofabrication without placing constraints on the geometry achievable. Not only is the process CMOS compatible but scalable down to devices with small critical widths and scalable in manufacturing of large wafer sizes, entirely on silicon substrate [81]. This provides a lot of flexibility for achievable new geometries from NWs, to ribbon like, cross bars [83] and even high aspect ratio fins through this thesis work. The uniqueness of this process is that a mono-crystalline Si is not obligatory for a crystalline material growth but also poly-crystalline nucleation surfaces can be used. As long as the starting silicon seed is sufficiently small to subdue growth from many nucleation sites first at the interface a region rich in defects is formed but far away from the Si/III-V interface we achieve a single crystalline material due to orientation filtering [83, 84]. Moreover a primary advantage compared to metal-catalysed growth is that the nano template based approach

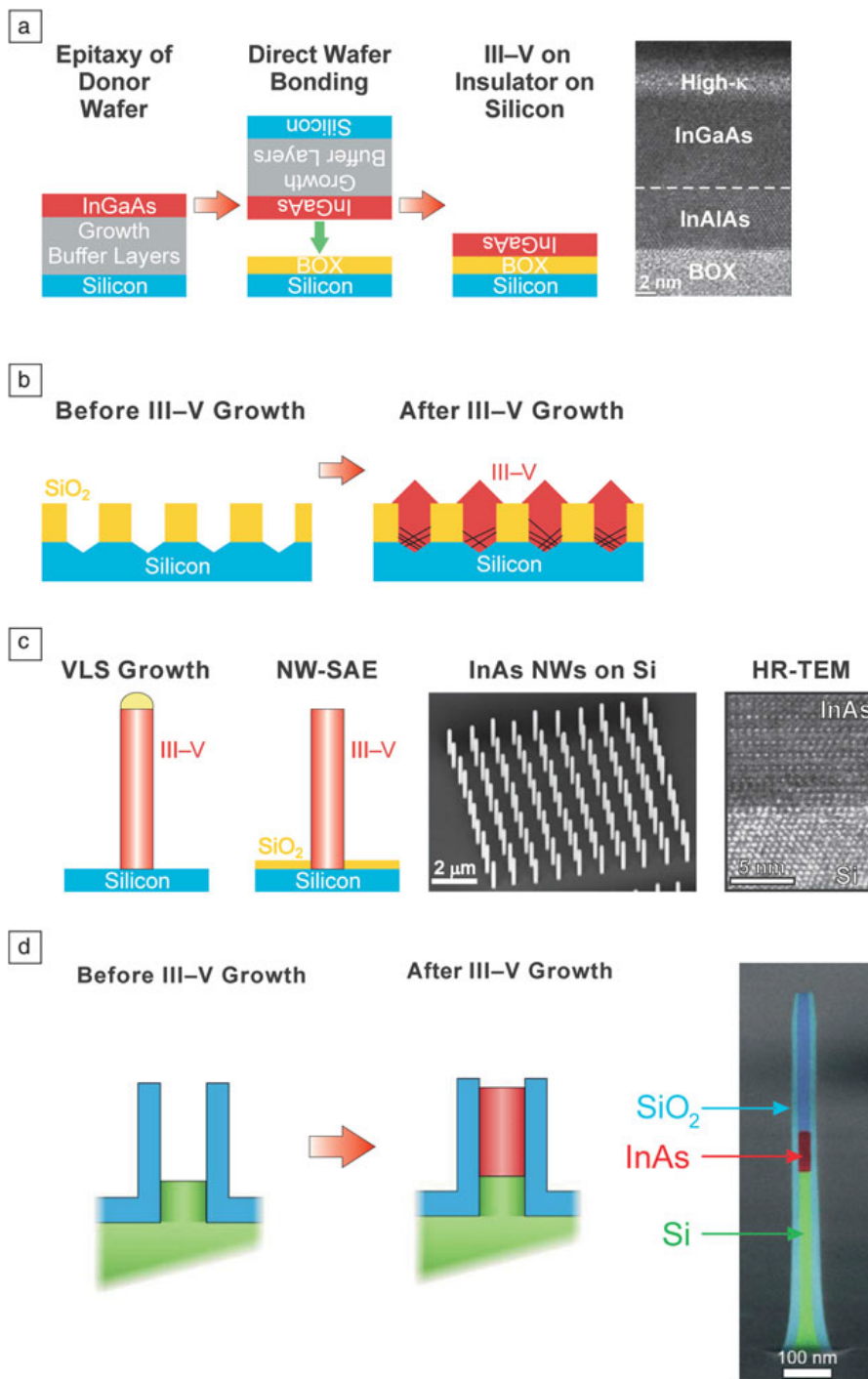


Figure 2.28 – Global approaches - a) Direct wafer bonding of thin epitaxial layers of III-V e.g InGaAs or InAs on insulator on silicon substrate. b) schematic of Aspect ratio trapping before and after growth of III-V. Local integration approaches - c) schematic of InAs NW grown using vapor-liquid-solid (VLS) technique. d) template assisted growth where nanotube templates of oxide are fabricated on silicon and filled using III-V selective epitaxy. Taken from [82].

does not suffer from hetero-interface mixing and a non-intentional core-shell formation [80]. The principles and mechanisms for heterogenous integration explained in this section broadly hold for other III-Vs but is out of the scope of this thesis. For this work the focus is on n-type InAs. Therefore incorporating III-V in silicon in a CMOS compatible process can really increase the commercial viability of InAs based sensors.

2.6.2 Geometry: High-Aspect-Ratio (HAR) fin

Silicon complementary metal oxide semiconductor (CMOS) technology has fueled the electronics industry for many decades thus far. However, with growing performance requirements demanded by today's and tomorrow's age, silicon on its own cannot entirely deliver. Other channel materials need to be incorporated along with it. The international technology roadmap for semiconductors (ITRS) touts III-Vs as leading contenders to replace silicon as channel materials in future device technology nodes for their high carrier mobilities and saturation velocities. Moreover, with limits on scaling of transistors and their pitch dimensions, a vertical geometry is highly favoured for computation. This way the lateral gate length is not limited by the area density. However a tight pitch design comes with its own set of challenges and patterning it as we shall see. It is in this context that a vertical geometry is explored along with its unique advantages for sensing is explained in this section.

Now for sensing, the argument that higher dimensional structures are great for sensing due to their high surface-to-volume (S/V) ratios should be well understood. When it is said that high S/V volume ratios are favourable for sensing in 2D structures (NW, fin) over the planar (1D) counterparts this argument makes sense immediately for electrostatic considerations. However, it is not the full picture since the kinetic processes involved in the capture of target molecules by the sensor are not yet included in the discussion. The settling time (t_s) is time taken by the sensor to capture a particular number of target molecules when inserted into the target solution. The advantages of a nanobiosensor have been well characterized by Nair *et al.* [85], where they specify a trade-off between t_s and minimum detectable concentration (N_0). So the advantage of 2D over 1D will be tangible after referring to the following condition in equation 2.14.

$$t_{s,2D} \leq t_{s,1D} \quad (2.14)$$

Therefore, when considering reasonable response times in few minutes then 2D geometries like fin can allow detection well into the femtomolar regime [85].

2.6.3 Sensing area

For sensing response, a larger area for the flux of target molecules to bind to target receptors is logical. However for computation, densely packing devices is the norm. To reconcile these two differences for a unified platform, a 3D geometry especially, tall fin with a multiple finger

design can satisfy the demands from these two fields. That is, have a larger sensing surface area while restricting the actual device footprint. For this reason, a tight pitch of 250 nm for the multiple finger sensor design is chosen. This way the effective fin width exceeds the actual device width. Also the possibility to build accurate reliable arrays is a requirement for sensors to scale up detection of different ionic species on the same chip [86].

2.6.4 Sensing High-k Oxide

While silicon dioxide serves as a pH sensitive layer it still is not the best among other available oxides because it allows the hydrogen ions to penetrate the oxide and can potentially result in unwanted leakage currents [7]]. The reactions at the gate oxide of the FET determine the intrinsic sensitivity of the device to pH. Therefore, a thin high-k oxide layer serves as the main sensing layer. High-k oxides gained popularity in the electronic industry for sustaining high electric fields without breakdown for very thin layers. HfO_2 is chosen as the high-k sensing oxide for being proton sensitive due to a high density of surface groups, non permeable to H^+ ions allowing a stable response in an aqueous environment [50]. Atomic layer deposition tool is used to wrap completely the device with a thin layer, 20 nm of oxide in this case HfO_2 . HfO_2 also doubles as the layer for isolation of the source and drain contacts from the channel. When a separate isolation oxide and sensing oxide are used the high-k oxide for sensing can be scaled much further.

2.6.5 Junctionless Transistor

The absence of junctions simplifies the fabrication process, reduces device to device variability and relaxes thermal processing steps involved for nanoscale FETs [87]. With an integration process like TASE, identifying the junctions post epitaxial growth can be extremely challenging. And alignment of device contacts to these junctions can place tight restrictions of channel length from the growth step. Therefore a junctionless architecture is chosen for the transistor operation.

Performance Evaluation

In a junctionless FinFET it is well understood that the depleted the highly doped channel body is necessary. And this is essentially dependent on the fin width (W_{fin}) and the doping level (N_D) [22]. The structure of the simulated InAs-on-insulator FinFET is shown in figure 2.29. The important parameters are as follows:

- Software: Sentaurus SYNOPSIS
- Material: InAs
- Junctionless FinFET

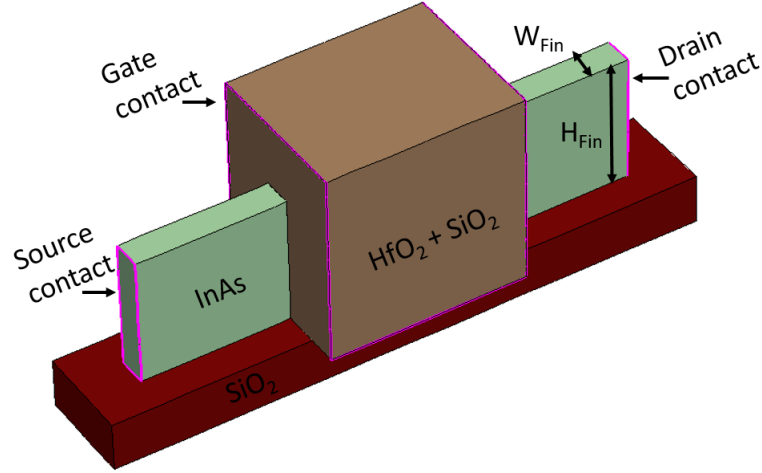


Figure 2.29 – Simulated InAs-on-insulator FinFET structure.

- $H_{fin} = 130 \text{ nm}$
- $W_{fin} = 30 \text{ nm to } 80 \text{ nm}$
- Oxide = $10 \text{ nm SiO}_2 + 20 \text{ nm HfO}_2$
- SRH recombination model applied
- Doping level = $4 \times 10^{17} \text{ to } 8 \times 10^{17} \text{ cm}^{-3}$
- Gate work function = 5 eV

Therefore for a given substrate thickness i.e fin height (H_{fin}) using Sentaurus TCAD simulations the fin width (W_{fin}) and doping level (N_D) are varied to gauge depletion of the junctionless FinFET. From previous TASE integration works we learn that there is a lower limit to the n-type doping level in grown InAs structures this is to be $4 \times 10^{17} \text{ cm}^{-3}$ [83]. Hence the doping is varied limit and for design space of $30 \text{ nm to } 80 \text{ nm}$ of W_{fin} . From figure 2.30 to figure 2.32 the transfer characteristics are shown for three different doping conditions. The aim of the fabrication process is to achieve the narrowest fin width so that it can be depleted at higher doping levels also. Hence, fabrication should be aimed towards narrowest fin widths of the order of 30 nm . However we shall see in our results that the devices which withstand processing till the last steps are the wider fins and we are usually on the black and red curves shown in figure 2.30, figure 2.31 and figure 2.32.

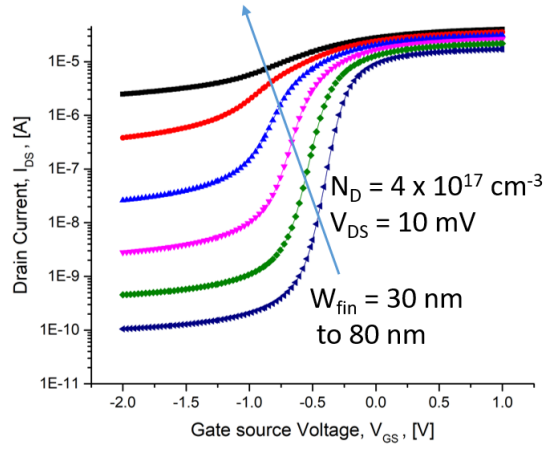


Figure 2.30 – Transfer characteristics I.

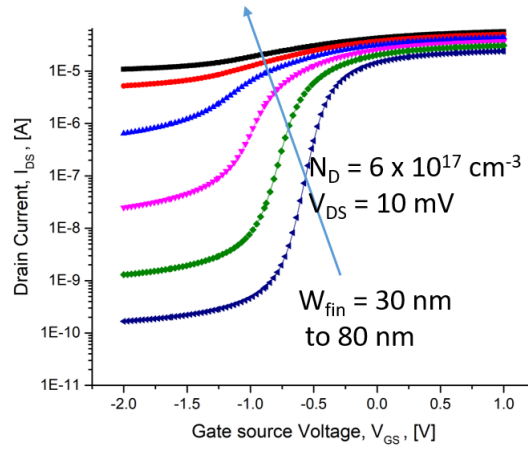


Figure 2.31 – Transfer characteristics II.

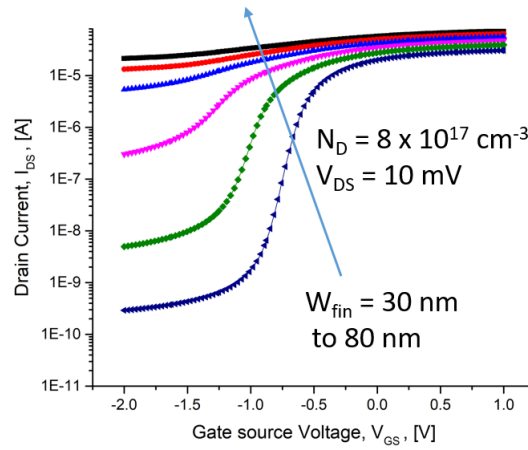


Figure 2.32 – Transfer characteristics III.

2.7 Summary

In this chapter a context for the thesis work is provided. A detailed review of literature works enables us to establish an interest in the material of InAs. Finally a systematic review of the choices of material, geometry, high-k oxide, junctionless transistor design are explained through references to literature and with simulations. The next chapter describes in detail the fabrication process of InAs-On-Insulator (InAsOI) FinFETs for demonstrating ion sensing.

3 Technology Development of InAs-On-Insulator (InAsOI) FinFET Nanostructures

Template assisted selective epitaxy (TASE) process was co-developed and co-patented by personnel from IBM Research-Zurich (Switzerland) & IBM Research-Watson (USA). In this section we developed and explored one novel geometrical facet of its many. This part of the work was carried out with ideation and constant discussions with collaborators Heinz Schmid, Clarissa Convertino and Kirsten Moselund from IBM Research (Switzerland). Almost all processing was carried out entirely by the author at CMI cleanroom in EPFL. However, InAs MOCVD growth step was always exclusively carried out by Clarissa Convertino and/or Heinz Schmid at IBM Research (Switzerland). The Transmission electron images were taken with staff at the Interdisciplinary Center for Electron Microscopy (EPFL).

3.1 Process Overview

The entire fabrication process can be categorized as pre-growth processing (all steps leading to TASE), TASE and post growth processing. The post growth steps vary only at the end for metal gate and liquid gate characterization of the devices. This is outlined in Figure 3.1. In theory, all steps of the entire process are wafer level-compatible including epitaxial growth. However in order to introduce variations in the processing when and where necessary the chips are diced right before the template openings step.

- Technology: SOI
- Number of ebeam masks until epitaxy step: 3
- Number of photo lithography masks until epitaxy step: 1
- Total number of steps until epitaxy step: 25
- Total number of ebeam masks for liquid gating: 5
- Total number of steps for liquid gating: 40

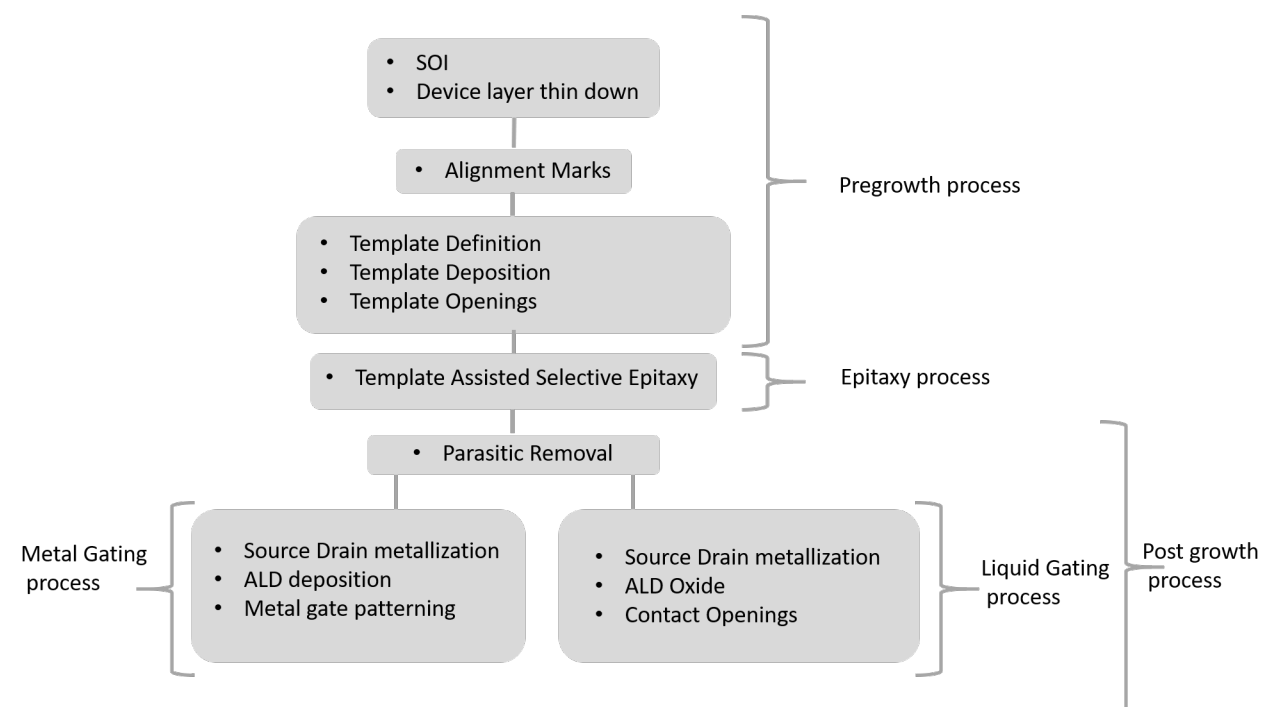


Figure 3.1 – Classification of process steps for clarity is shown

- Total number of ebeam masks for metal gating: 5 or 6
- Total number of steps for metal gating: 40
- Main cleanroom techniques:
 1. E-beam and UV lithography
 2. LPCVD, PECVD, wet oxidation, ALD, evaporation, sputtering
 3. MOCVD
 4. Etching : RIE, ion beam etching, wet etching
 5. SEM, FIB, TEM, optical microscope, mechanical profilometer, ellipsometer and reflectometer
- Software used:
 1. Sentaurus work bench by Synopsis
 2. Layout BEAMER by GenlSys
 3. L-Edit IC Layout by Tanner

3.2 Pre-growth steps

We start with a 100 mm diameter, SOI substrate with a device layer thickness of 220 nm, a buried oxide layer of 2 μm and handle wafer thickness of 725 μm . The SOI device layer has

<100> orientation, is of p-type with a resistivity of 8.5-11.5 $\Omega\cdot\text{cm}$. Using a combination of wet oxidation and blanket buffered oxide etching (BHF) we thin down the silicon device layer to 110 nm.

3.2.1 Alignment Marks

In order to perform a process with 5 ebeam masks, alignment marks are crucial. Moreover alignments down to 100 nm or better are needed in this process. As can be seen in Figure 3.2 all the marks used are shown: wafer pre-alignment marks (red), die global alignment marks (green) and die local alignment marks (purple).

At the wafer scale the e-beam tool first looks for the center of a 29×29 array of $10\ \mu\text{m}$ squares in the pre-alignment marks. The automatic search algorithm finds the center square of this array and is identified as the zero point of the coordinate system at wafer level. Next, the x and y-axis are located using a global alignment procedure of 5 markers from 5 different sets of 3×3 die global alignment marks as highlighted in blue.

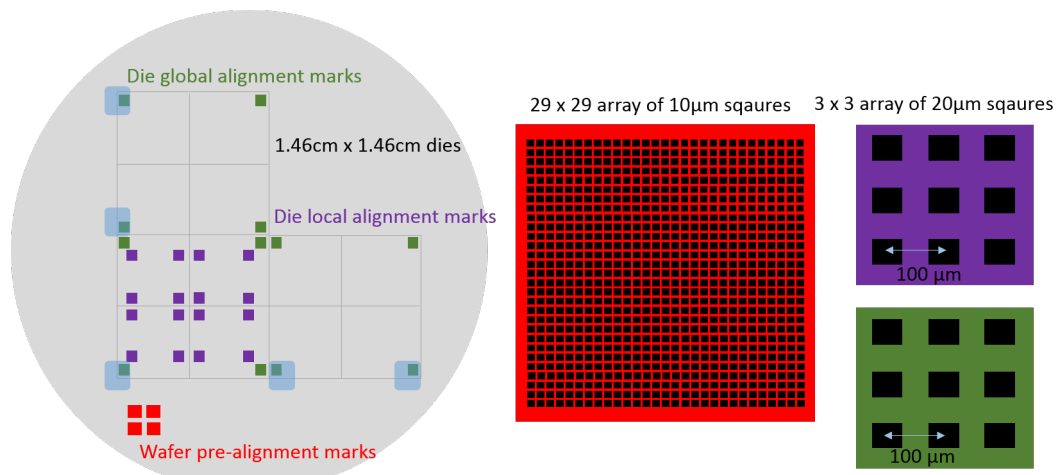


Figure 3.2 – Alignment marks are visualized on the wafer- prealignment marks, global wafer alignment procedure, die global alignment marks, die local alignment marks

The alignment marks squares can be either positive or negative. Positive marks are deposited using a metal with a high atomic number such as gold, platinum or tungsten. Negative marks are etched into the substrate to an etch depth of at least $2\text{--}3\ \mu\text{m}$. In both cases it is sharp edges and a good contrast between the wafer and marker surface that results in high fidelity markers. The markers can be fabricated using optical lithography or e-beam lithography (EBL) alike. We use EBL in marker fabrication since in subsequent steps the masks are also for e-beam steps: this preserves marker identification accuracy by using the same tool. We have experimentally seen that positive markers with a thick oxide protection layer survive well the various etch steps resulting in alignment accuracy down to 100 nm.

The EBL tool specifications and proximity effect parameters are explained in the ebeam lithography section 3.2.2. The EBL exposes a PMMA/MMA bilayer resist. The following parameters were used:

- **Resist thickness PMMA/MMA:** 150 nm/450 nm
- **Dose:** 1000 $\mu\text{C}/\text{cm}^2$
- **Proximity effect correction parameters:** $\beta = 33 \mu\text{m}$ and $\eta = 0.5$

After exposure, the samples are developed in PMMA developer for 1 min. A short descum in oxygen plasma is performed just before metal deposition. In this case we sputter 130 nm of platinum for the markers and lift off the remaining resist. Finally we deposit 500 nm of TEOS oxide as a protection layer for the metal marks. Using optical lithography and a negative tone resist, AZ n-LOF the protection oxide is patterned to remain only on the areas where metal markers are present. The TEOS oxide is etched away in other parts of the wafer using buffered HF(BHF) wet etch. An evolution of the final marks is shown in the scanning electron micrograph (SEM) of figure 3.3.

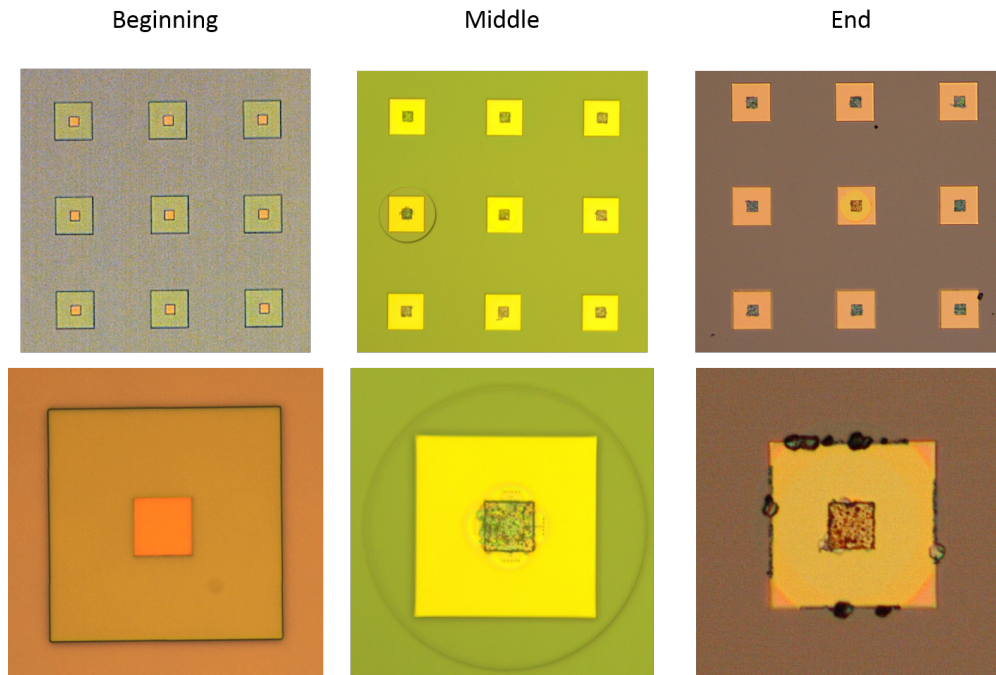


Figure 3.3 – SEM images show evolution of the metal alignment marks with an oxide protection layer. Small square is the metal marks, larger square is the protection oxide.

As seen the metal granulates when subject to high temperature steps as a result of differences in thermal expansion of the protection oxide above and the metal layer below. However we see from the higher resolution SEM image on a used alignment mark that the

edges are found well by the automatic search algorithm of the EBL system despite metal granularity as in figure 3.4.

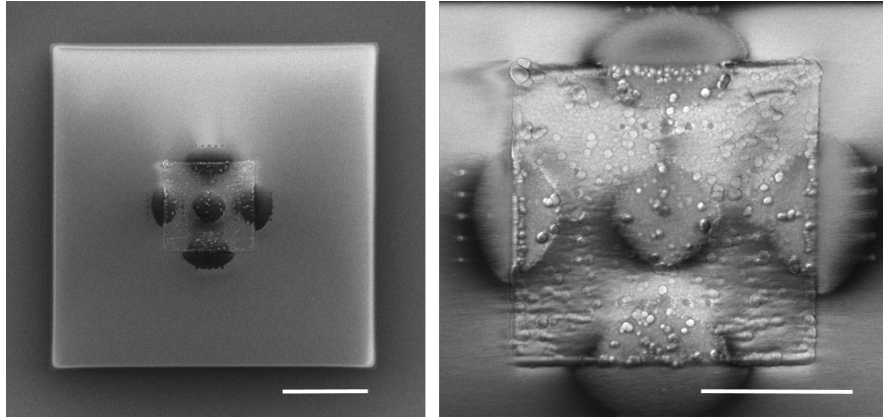


Figure 3.4 – High resolution SEM image of a used Pt alignment mark - seen is the edge search effect of EBL. Scale bars are 20 μm and 10 μm respectively.

In order to ensure that the wafer surface is ultra clean for the EBL step a piranha clean for 10 minutes is performed. Piranha consists of two parts H_2SO_4 with one part H_2O_2 and is an exothermic reaction. This oxidises part of the device layer and silicon device layer is measured to be 108 nm right before EBL using ellipsometry.

3.2.2 Ebeam lithography

The EBL system used is from VISTEC EBPG5000+ (Raith) and consists of a 100 keV thermal field emission gun. It is expected to have an overlay accuracy of down to 20 nm and a minimum pattern resolution of 1 nm. However these stringent performances can be influenced by many factors such as resist type, resist thickness, substrate and parameters for proximity effect corrections. In the entire process, except 2 non-crucial steps of protection oxide patterning at the beginning and contact pads opening at the end, all remaining lithography steps are performed using EBL and require alignment accuracy in the order of 100 nm. It is a very significant part of the fabrication. In every EBL step the layout maybe composed of a high resolution layer and a low resolution layer to optimize the writing procedure.

When a uniform dose is applied on a pattern it is possible that the final result appears under or over exposed. This is due to the pattern density. Therefore a dose application strategy is necessary to correct the effects of proximity of patterns. Proximity effect correction software such as BEAMER GeniSys can enable this. The important parameters are α , β and η that are related to resist, substrate materials and beam energy (in our case - 100 keV). α is related to the distribution of forward scattering electrons in the resist and is negligible for our very thin resist. β depends on the backscattered electrons deposited energy in the resist and is dependent on the substrate composition; for silicon this value is 33 μm . η characterizes the ratio of back scattered and forward scattered electrons, this value is variable for different

resists.

The first ebeam mask is a negative tone resist, HSQ XR1541 002 spun on the SOI wafer using a spin coater. A thin HSQ layer needs to be used to accommodate fin width (Critical Dimension-CD) down to 20 nm. Moreover the HSQ thickness should also serve as a good etching mask to etch the SOI device layer thickness (fin height) of 108 nm. First a series of dose tests are carried out by varying dose and η from values in literature and previous users for a given resist. The subsequent patterns are extensively characterized by SEM in order to finalize the suitable dose and η combination. Eventually after a couple of iterations of the EBL step and the reactive ion etching step in section 3.2.3 we arrive at the final EBL parameters for HSQ XR1541 002 in this step.

- **Spin speed:** 4000 rpm
- **Resist thickness:** 30 nm
- **Resolution:** 2 nm and 50 nm
- **Current:** 5 nA, 200 nA or 150 nA
- **Dose:** 3500 $\mu\text{C}/\text{cm}^2$
- **Proximity effect correction parameters:** $\beta = 33 \mu\text{m}$, $\eta = 1.5$

A short baking step right after the HSQ coating allows to remove more solvents and further reduce the thickness of the resist to arrive at 30 nm. After exposure the unexposed HSQ is washed away in a high contrast developer TMAH25% for one minute. One can see in the SEM images shown in figure 3.5(a)-(d) the pattern evolution from underexposed to overexposed scenario. For the design in figure 3.5(a)-(b) line edge roughness is high, W_{fin} dimension fabricated does not match the designed value of 40 nm and the pixelated ebeam shots are visible in the pad supporting the fin- all signs of underexposure. Whereas in figure 3.5(c) has the right dimension agreement with designed value of 40 nm. Finally, clear overexposure is seen at the junction of pad and fin in figure 3.5(d).

3.2.3 Silicon reactive ion etching

Silicon reactive ion etching (RIE) process is carried out on the STS multiplex using an inductively coupled plasma etching tool that uses HBr chemistry and oxygen. This etch process is very sensitive as process reproducibility depends on previous chamber processes and conditioning. Addition of O_2 is known to increase the etch rate of Si and gradually decrease the etch rate of SiO_2 . The conditioning of the chamber ensures that the chamber walls have a coating of SiOBr that inhibits Br radical recombination. As in the SEM images of figure 3.6 with the right RF power, Br radicals enable silicon anisotropic etching and clean vertical sidewalls.

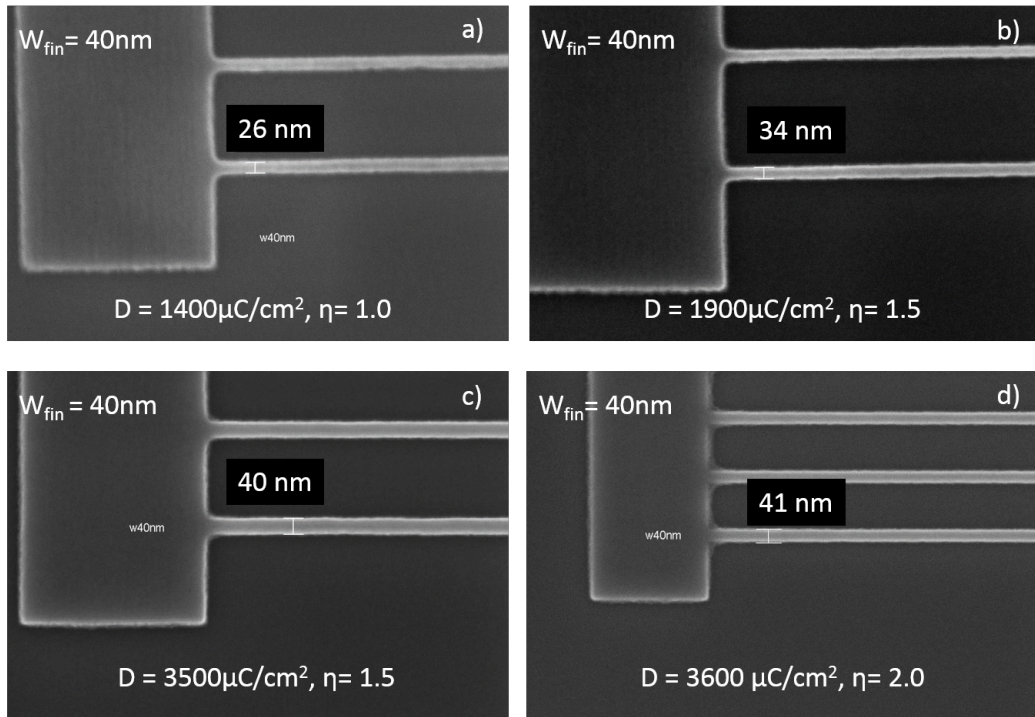


Figure 3.5 – From under exposed to over exposed HSQ structures for different range of Dose, η values depicted in SEM images

The etch rates obtained are:

- **Si:** 185 nm/min
- **HSQ:** 20 nm/min

HBr process has a good etch selectivity towards Si over SiO_2 and the etch selectivity is calculated to be $\text{Si}:\text{SiO}_2 = \sim 9:1$. The etch time in our case was 35 seconds. There is a breakthrough step at the beginning of the etch recipe that is very important, it lasts 10 seconds and is to ensure that the native oxide has been etched to expose the underlying Si.

HSQ stripping

After the HBr etch is complete, using a reflectometer we verify that the landing is indeed on the buried oxide and no residual silicon is left. The remaining HSQ resist needs to be stripped in order to have a clean Si surface for template deposition. The HSQ was initially removed in standard buffered HF ($\text{HF}:\text{NH}_4\text{F}$ is 12.5%:87.5%) but the results were not desirable.

The issue is illustrated in figure 3.7 where the structures collapse given a large L_{fin}/W_{fin} ($1.5 \mu\text{m}/30 \text{ nm}$) ratio. A shorter etch time can result in high variability across the wafer

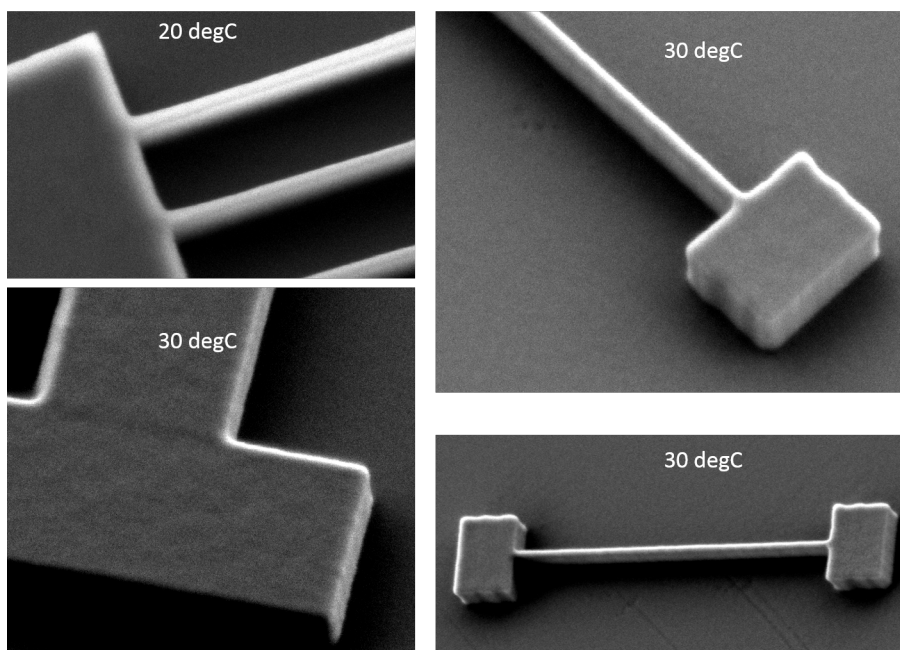


Figure 3.6 – Tilted SEM images of different test structures on buried oxide showing vertical sidewall etches

hence a more dilute etchant with a longer etch time was preferred to resolve this issue. HF 2% was prepared and used for the subsequent HSQ stripping steps. The etch rates of the buried oxide in BHF, DHF are as follows:

- **Etch rate in BHF:** 86 nm/min
- **Etch rate in DHF2%:** 20 nm/min

The etch rate has been reduced by 4 times enabling larger control over the etch process.

3.2.4 Oxide deposition

The silicon islands on buried oxide are now to be covered conformally using SiO_2 referred here on as template oxide. The template oxide consists of 30 nm SiO_2 deposited using atomic layer deposition (ALD) and 50 nm SiO_2 deposited using CVD technique such as low pressure chemical vapor deposition (LPCVD) tetraethyl orthosilicate (TEOS). This is shown in figure 3.8. An annealing step of 850°C for 30 seconds in a nitrogen ambient is performed in order to densify the oxide. It is after this annealing step that granulation of Pt in the alignment markers is seen as shown in the SEM images in figure 3.4.

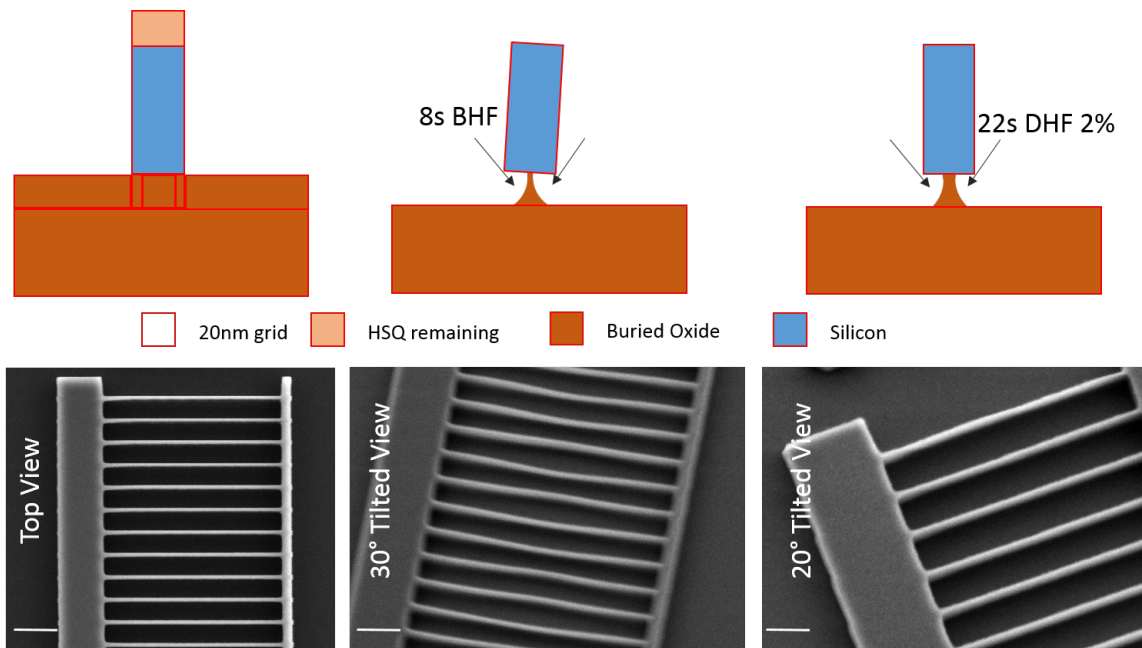


Figure 3.7 – The top and tilted SEM views of an array of 30 nm wide fins where BHF over etch results in a collapse and is resolved with DHF 2% etch. Scale bar left to right - 300 nm, 200 nm, 150 nm

3.2.5 Template opening ebeam lithography

For this step first a single layer of PMMA 950K A4 was spin coated on the entire wafer and exposed using EBL. The EBL parameters are as follows:

- **Spin speed:** 2000 rpm
- **Resist thickness:** 320 nm
- **Resolution:** 10 nm
- **Current:** 20 nA
- **Dose:** 1200 $\mu\text{C}/\text{cm}^2$
- **Proximity effect correction parameters:** $\beta = 33 \mu\text{m}$, $\eta = 0.5$

Development is carried out in a developer made of MIBK & IPA and then in IPA for one minute each. The resulting openings on various test structures is shown in figure 3.9. Alignments with a placement accuracy down to 50 nm are seen in these structures.

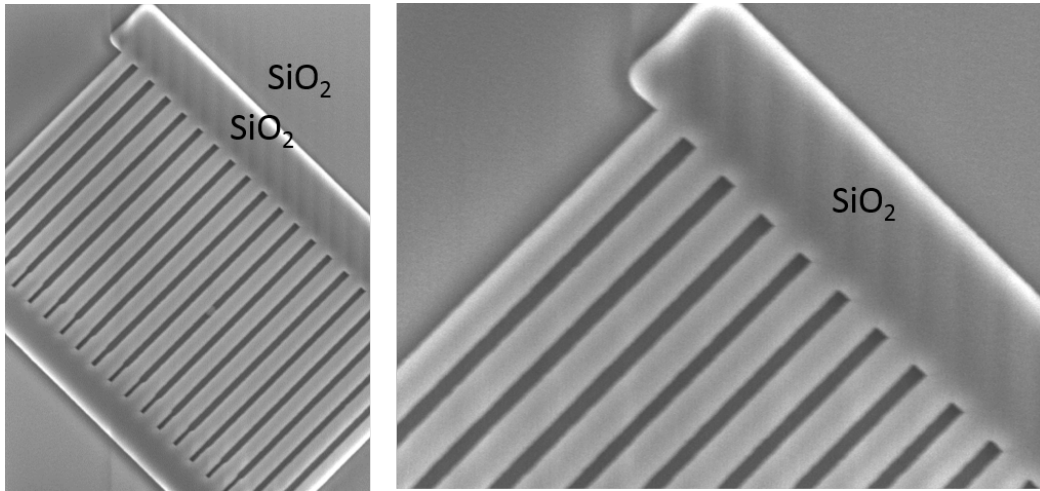


Figure 3.8 – Template oxide enclosing entire Si structure seen in the top view SEM images

Oxide etch

This is done using the PMMA mask. First a short dry etch is carried out, followed by a longer wet etch in DHF in order to expose the underlying silicon.

3.2.6 Wafer dicing

At this stage the wafer is coated with a protective photoresist layer about $2\text{ }\mu\text{m}$ thick and then diced into chips of $1.46\text{ mm} \times 1.46\text{ mm}$. Finally the protective resist and the PMMA resist used for previous lithography steps are removed using solvents. A piranha cleaning is done to clear away any organic residues before the silicon etch in section 3.2.7. Normally, the next steps are all compatible with wafer level processing including the epitaxial growth. However, in order to test different growth conditions, processing conditions the wafer was diced at this stage.

3.2.7 Silicon anisotropic wet etching

Anisotropic wet etching of Silicon is carried out with tetramethylammonium hydroxide (TMAH). As different crystal planes have different activation energies, TMAH takes advantage of this difference, while it etches (100) and (110) planes easily and stops etching at the more dense and stable (111) planes. Though TMAH is available in 25% by weight concentration commercially, TMAH 2% dilution at 70°C has been optimized in previous work [88] and is used for the current etch recipe as well. In our case silicon is known to be etched from inside of long, narrow oxide channels in a slow, controllable fashion with etch rate of about tens of nm/min. Note that this etch rate is specific to our layout and etch rate of blanket silicon

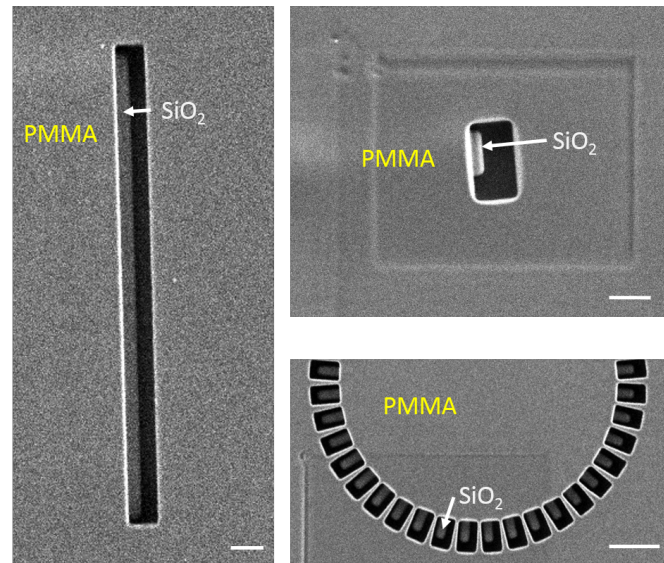


Figure 3.9 – SEM images showing openings in PMMA resist of the template oxide in various test structures

layer without a mask can be quite different.

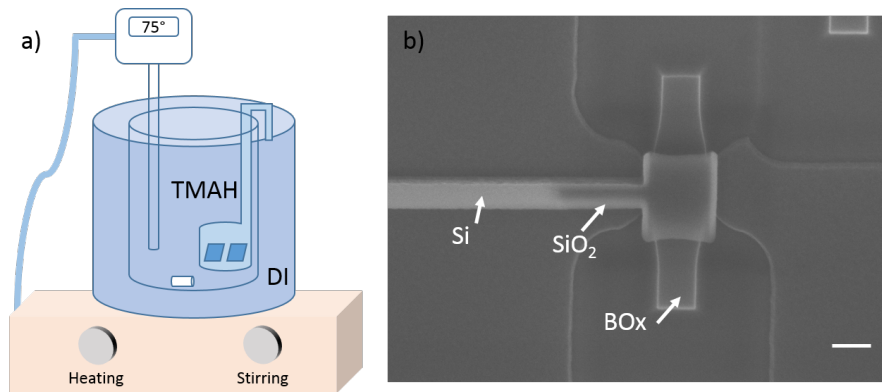


Figure 3.10 – a) Schematic of TMAH etch setup with heating and stirring functionality. b) SEM Image of a Si partial etch inside the SiO_2 template is seen. Scale bar = 200 nm

The etching setup consists of double beakers placed on a hot plate as shown in figure 3.10(a). The outer beaker consists of deionised (DI) water and the inner beaker of TMAH solution. This is to ensure a uniform heating of the TMAH through DI water instead of air. A thermometer is placed inside the TMAH beaker and contains a feedback to maintain a stable temperature of 75°C . The samples are placed in a teflon chip holder and at a time no more than 2 samples were etched in order to avoid shadowing effect. Since the regions to be etched are long, narrow and only accessible from a small opening, magnetic stirring continuously aids uniform etching. The gradual etching of silicon inside the template can be distinguished from the contrast of the SEM image in figure 3.10(b)

We see in figure 3.11(a)-(d) a series of SEM images, structures of various shapes etched back to different lengths. The bright portions of the image represent the oxide template with silicon and the darker regions show only the hollow oxide template. All the structures were oriented along $\langle 110 \rangle$ on the wafer except test structures for study of orientation effects on growth.

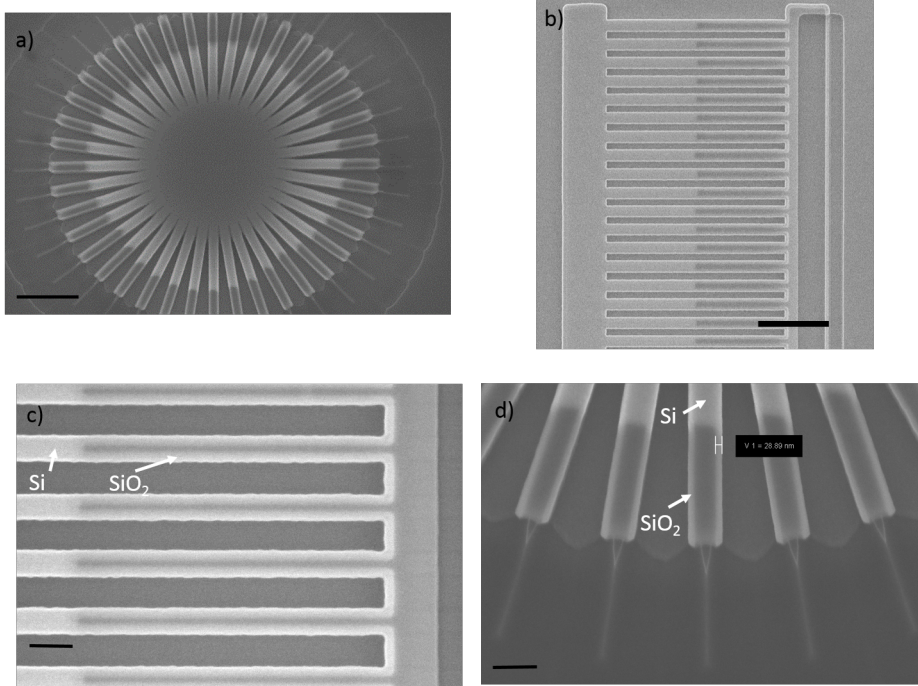


Figure 3.11 – (a) to (d) Topview SEM images of various structures back etched to different lengths. The bright areas where template oxide is filled with Silicon and dark regions where template oxide is hollow are clearly distinguishable. Scale bar = 1 μm , 1 μm , 200 nm, 200 nm.

3.3 Template Assisted Selective Epitaxy Mechanism

TASE is a metal-organic vapour phase epitaxy (MOVPE) or alternatively referred to as metal-organic chemical vapor deposition (MOCVD) based technique to locally grow various types of III-Vs on a semiconductor substrate. The MOVPE process is illustrated in figure 3.12 where a combination of a non-reactive carrier gas + pure group III precursor and another non-reactive carrier gas + pure group V precursor are introduced simultaneously into the chamber, they travel by diffusion and are adsorbed at the surface of the target substrate and heterogeneously grow from the underlying crystalline wafer surface.

This process is carried out in a MOCVD reactor and the constituent parts are pictured in figure 3.13 which consist of inlets from the precursor gases and carrier gas in this case H_2 leading to the growth chamber. The substrate is thermally activated to provide energy for

3.3. Template Assisted Selective Epitaxy Mechanism

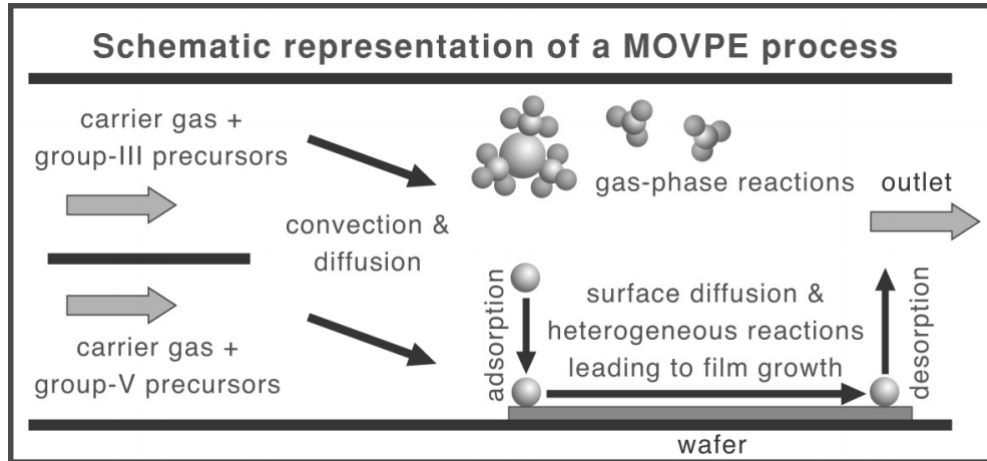


Figure 3.12 – MOVPE deposition mechanism taken from reference [89]

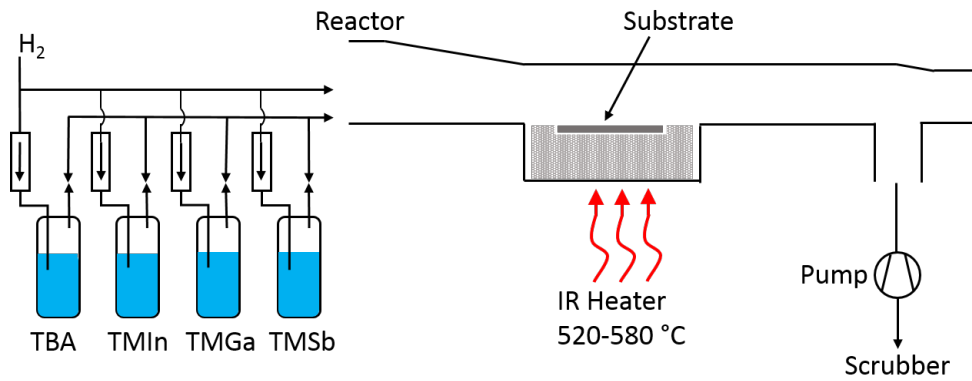


Figure 3.13 – MOCVD Reactor Furnace

the incoming atoms to re-arrange on it's surface. And finally a pump is used to extract out of the chamber the unused gases and products.

In TASE process a dielectric template is built around a small Si seed from which the III-V grows. The Si seed cross section is intended to be as small as possible in order to prevent growth from multiple nucleation sites that can lead to more defects and boundaries. In any case, the growth from the mutiple sites evolves into a single crystalline material away from the Si/III-V interface due to defect filtering. The main steps of TASE process are depicted in figure 3.14. In figure 3.14(a)-(c) represent the top schematic views and in figure 3.14(d)-(f) show the side schematic views of steps: template definition, Si back etching and InAs selective epitaxy.

Otherwise, with a blanket heteroepitaxy growth technique the common defects are shown in figure 3.15 and figure 3.16 when growth buffer layers are not used to relax the strain differences. Antiphase boundaries are formed when two domains of the same phase order

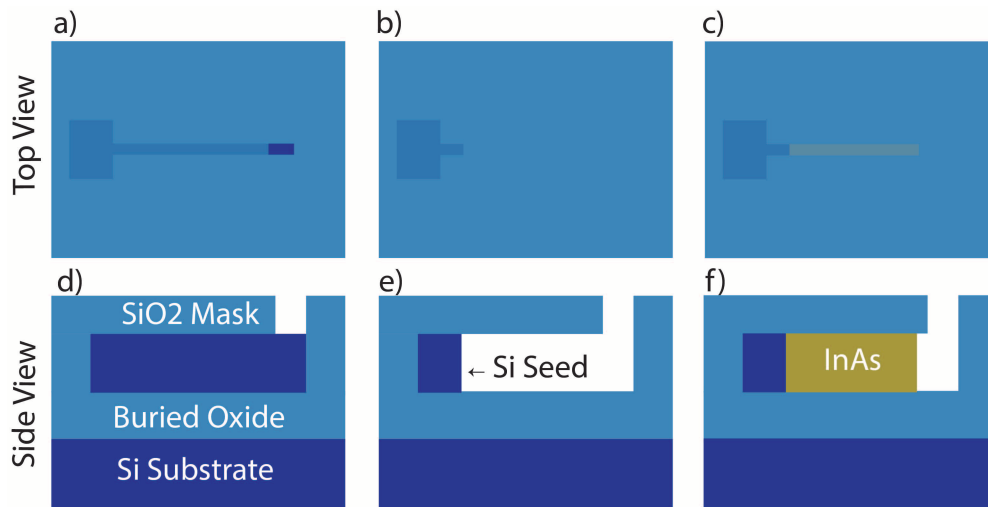


Figure 3.14 – a) to c) Top view and d) to f) side view schematic of steps of main steps in order to realize templates for epitaxy

are separated at the boundary. Misfit dislocation is a linear defect at the interface which propagates through layers of III-V as threading dislocations.

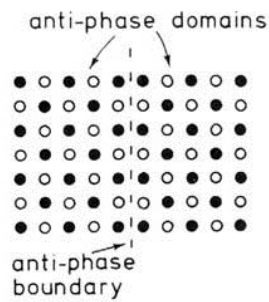


Figure 3.15 – Antiphase boundary. Image source: Google

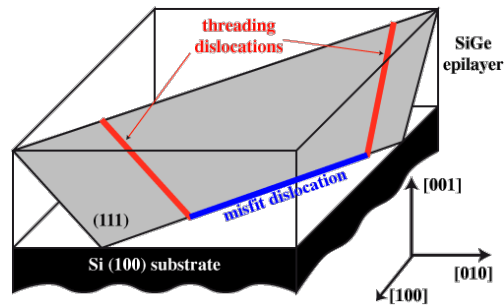


Figure 3.16 – Threading dislocations illustrated taken from [90]

Process Parameters

The important and relevant parameters used for template assisted selective epitaxy of InAs are listed here.

- Trimethylindium (TMIn) and Tertiarybutylarsine (TBAs) precursors and carrier gas H_2
- Flow rate of $2 \mu\text{mol}/\text{min}$ for TMIn
- V/III ratio of 40 or 80
- Temperature of substrate between 520°C to 550°C

3.4 MOVPE Growth characterization

First we look at growth patterns for single fin epitaxy runs with the same process parameters. The samples were observed under optical microscope, scanning electron microscope and where relevant, high resolution transmission electron microscopy was also used. From SEM figures, growth rate versus diameter is extracted and plotted for different epitaxy runs as shown from figure 3.17 to figure 3.19.

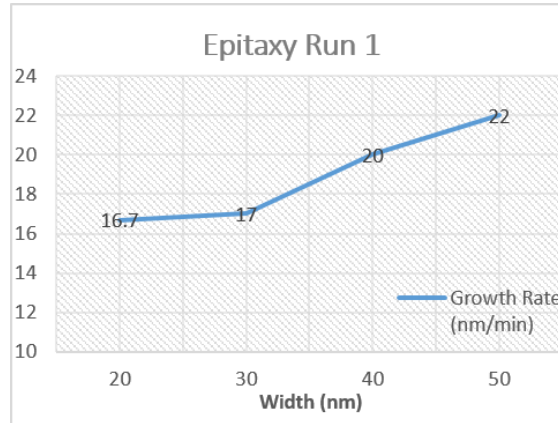


Figure 3.17 – Plot of growth rate versus fin width for InAs epitaxy run at 550°C for 10 mins

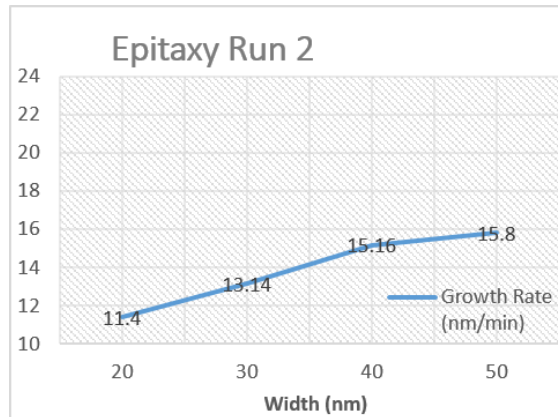


Figure 3.18 – Plot of growth rate versus fin width for InAs epitaxy run at 550°C for 50 mins

A general trend that can be noticed is for example the increase in growth rate with increase in fin width of the template. There is a deviation in the epitaxy run shown in figure 3.19 and this most likely could be due to differences in alignment of PMMA mask openings in the step of section 3.2.5. Since the transport of growth species is diffusion based the diffusion rate is slower inside longer and narrower fin templates. However, a definitive growth rate cannot be determined as it is seen to vary from run to run. But the growth rate is in the

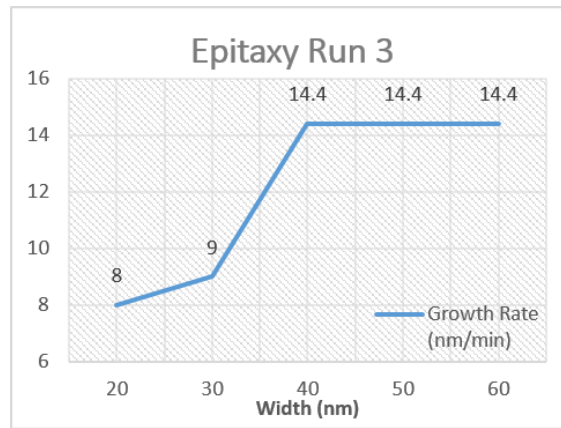


Figure 3.19 – Plot of growth rate versus fin width for InAs epitaxy run at 550°C for 50 mins

range of 8 nm/min to 22 nm/min for design fin widths of 20 nm to about 50 nm. Shown in the SEM of figure 3.20 are two different fin widths from the second epitaxy run at a similar magnification. The yield of InAs growth inside the template is close to 100%. However not all InAs growths are as expected and seen in section 3.4.1.

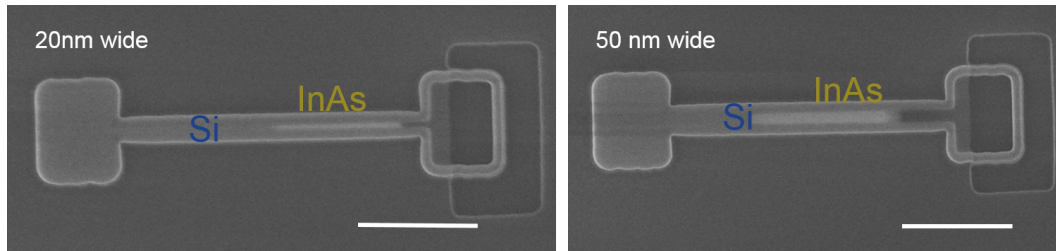


Figure 3.20 – Top view SEM image of fins with design width of 20 nm and 50 nm with a difference in the back etch length and the grown InAs length for a growth time of 50 mins. Scale bar = 600 nm

The width, height and interface roughness of the nanotube template is defined by the quality of fabrication steps thus far and is influenced by surface cleanliness, defects and chamber conditions. Detailed Transmission Electron Microscopy (TEM) analysis is performed on selected devices to characterize the structures further. Seen in figure 3.21 the angle between (100) plane and (111) plane sidewalls is 54.7°. The denser (111) plane acts as an etch stop to the TMAH plane dependent etching as discussed in section 3.2.7. It is important to note that the nanotube template expands in all directions just before MOVPE growth because of a DHF dip. This is clearly seen in the lateral TEM cross section of figure 3.21 where the fin height expands. What is not seen in this particular picture is that the InAs fin width is larger than that for Si fin by a couple of nanometers since the DHF dip etches isotropically. The increase in fin width and fin height is measured to be about 10 nm by observing SEMs.

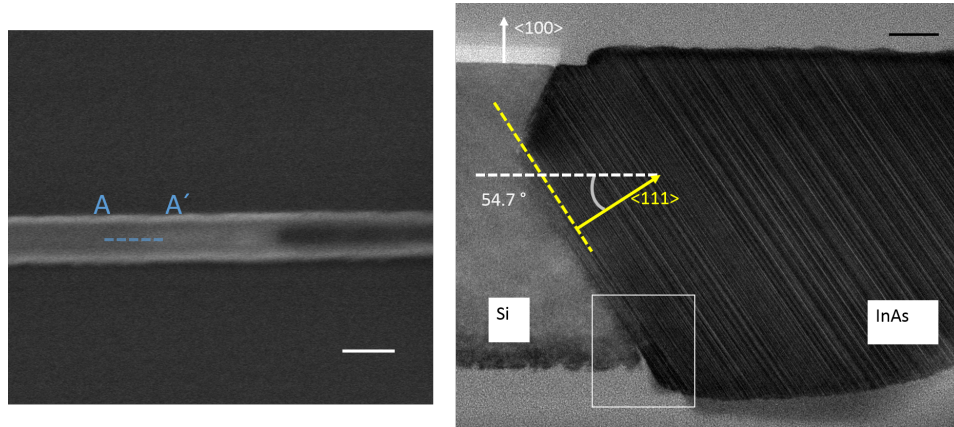


Figure 3.21 – The TEM image is taken across the line AA'. High resolution TEM shows a directional etch stop in (111) plane when using TMAH silicon etching. Scale bar = 100 nm, 20 nm.

Also, one can distinguish very clearly that the transition from silicon to InAs taking place over very few atomic layers (i.e. less than couple of nanometers) as seen in the closeup of figure 3.22. III-V compound semiconductors e.g InAs nanostructures are known to exhibit polytypism where the crystal structure is composed of two crystal orders with very little energy difference - wurtzite (WZ) and zinc-blende (ZB) regions.

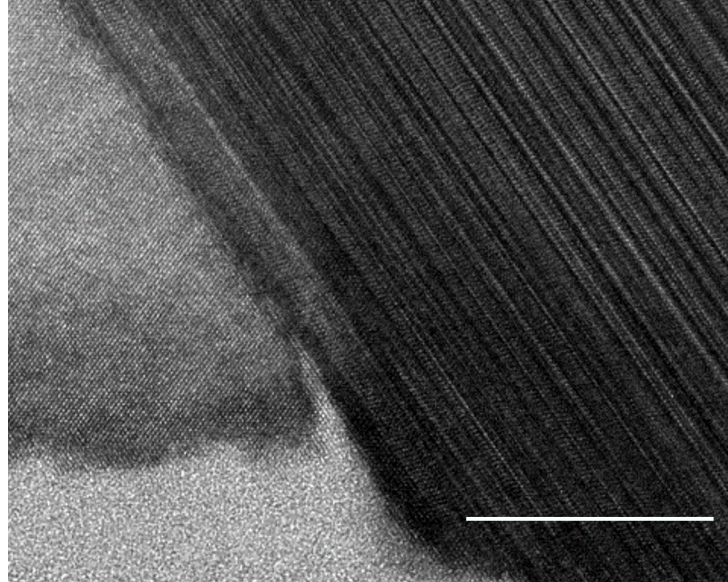


Figure 3.22 – A zoom of the previous HR TEM image at the hetero interface is shown here. Scale bar = 20 nm.

Consider that InAs structure is composed of a pair of In and As atom, defining a single bilayer. A normal ZB sequence consists ABCABC and one for WZ is ABABAB (where each

letter represents a bilayer)[91]. Stacking faults often result when a ZB segment appears in a WZ order or vice versa. A high density of stacking faults can be seen in figure 3.22 whereas antiphase boundaries and dislocations should not be visible. In order to discern whether the crystal is single crystalline, polycrystalline or amorphous the diffractions pattern can help as shown in the figure 3.23(a) to (c) [92].

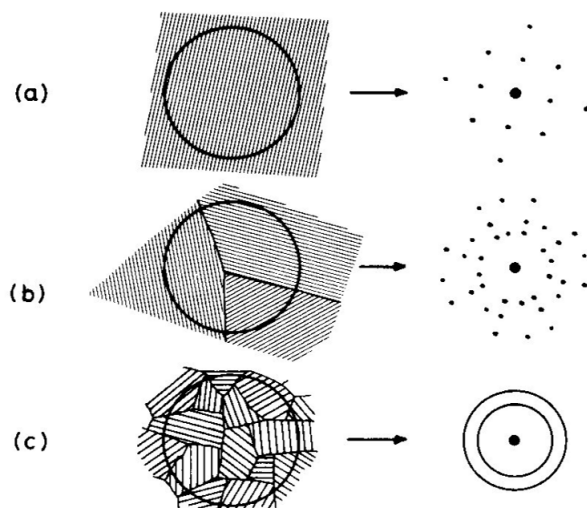


Figure 3.23 – Diffraction Patterns - a) Single crystalline pattern showing discrete spots. b) when few grains are present the spots begin to form circles. c) large randomly oriented grains show no spots but rings. Taken from [92]

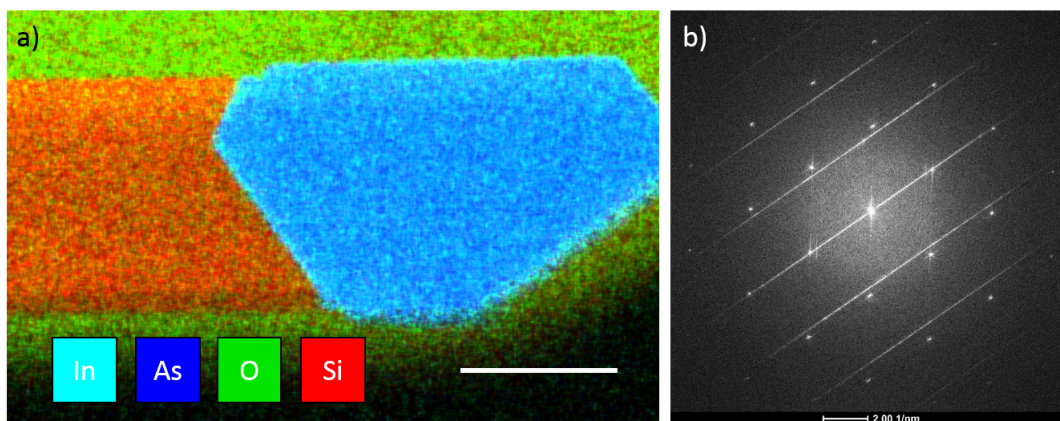


Figure 3.24 – a) An energy dispersive x-ray analysis (EDX) gives the elemental map indicating the material composition b) Single crystalline pattern showing discrete spots in the SAED image

From the figure 3.24(a) an elemental analysis map confirms growth of InAs selectively inside the template from the silicon seed. Also in figure 3.24(b) the selected area electron diffraction (SAED) pattern of a region in grown InAs confirms that the structure is single

3.4. MOVPE Growth characterization

crystalline with the absence of rings or spotty rings. So far we focussed only on the lateral cross section of a single fin whereas let us look at characterization of the multiple fin array as depicted in figure 3.25(a) to (c). An array of 20 fins tightly packed is shown in figure 3.25(a) and the FIB cross section taken across the line BB' is shown in figure 3.25(b). Explored using TASE is the unique geometry of high aspect ratio and a vertical cross section using High Resolution TEM Imaging is shown in figure 3.25(c). The fin height to fin width ratio (130 nm/ 30 nm) is in excess of 4.

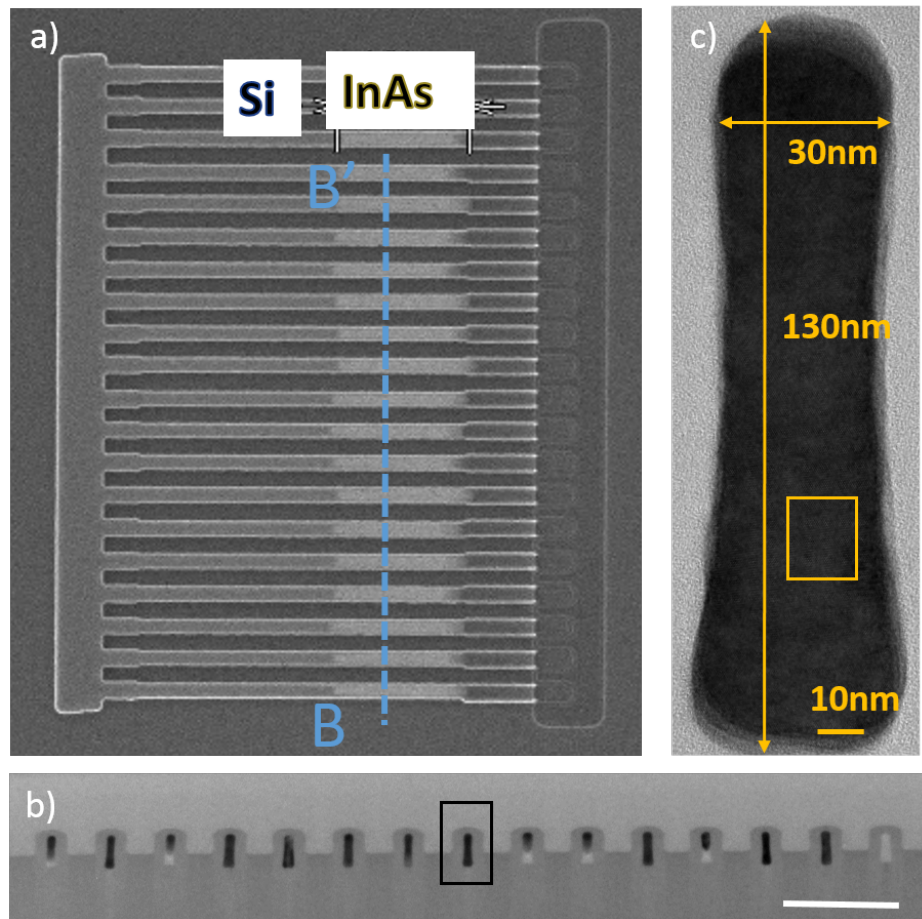


Figure 3.25 – The TEM image is taken across the line BB'. b) Focussed ion beam cross section of multiple fin array is shown. c) High Resolution image depicts the unique tall aspect ratio. Scale bar = 500 nm

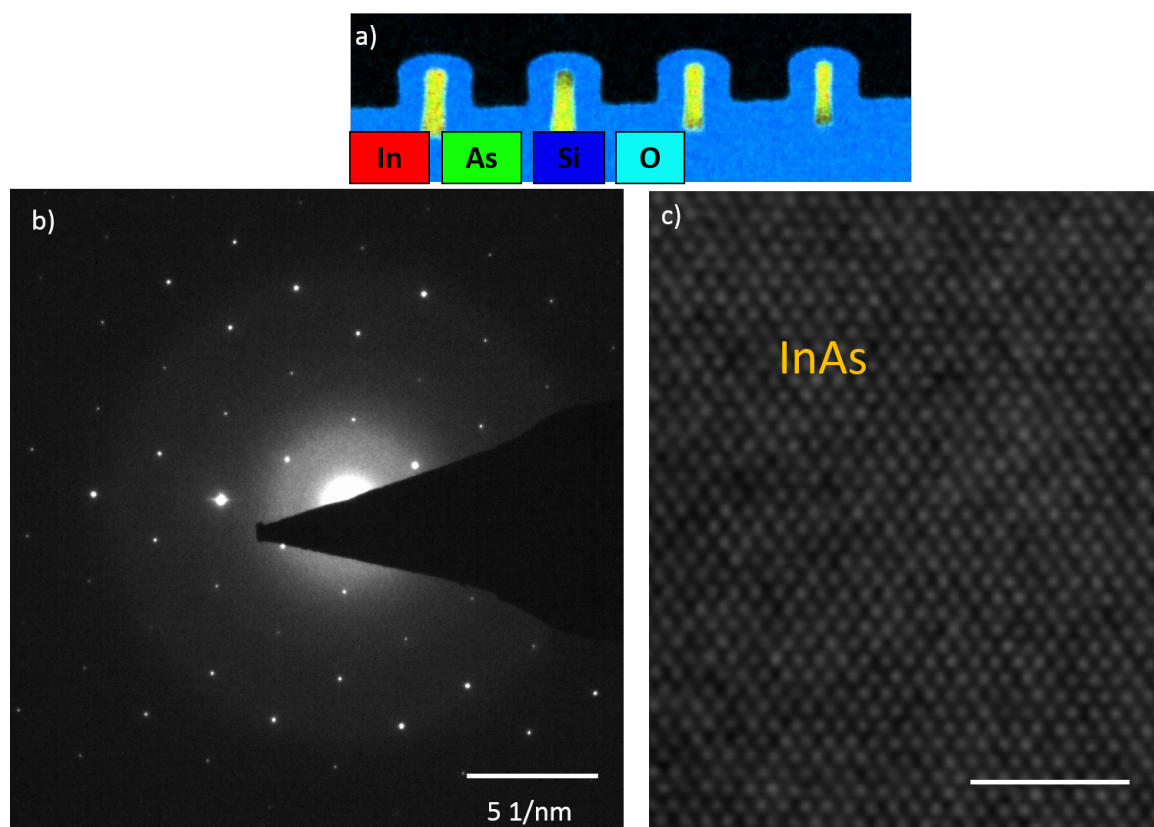


Figure 3.26 – a) An energy dispersive x-ray analysis gives the elemental analysis map indicating the material composition b) Single crystalline pattern showing discrete spots in the SAED image

An elemental analysis map of the multiple fin array also confirms the growth of InAs exclusively inside the SiO_2 template from a Silicon seed as in figure 3.26(a). In figure 3.26(b) the SAED pattern confirms highly single crystalline region of the section marked in orange colour in figure 3.25(c). The doping was indirectly referenced from previous work where unintentionally doped InAs was epitaxially grown with the same conditions [83]. Hence the doping level is approximated to be $4 \times 10^{17} \text{cm}^{-3}$ where most likely dopant sources are the carbon from precursor molecules and silicon dopants on in the tool. For further confirmation of a precise value secondary ion mass spectroscopy (SIMS) measurements can be used. However it must be noted that this technique is destructive and hence was not carried out on the initial limited number of test structures.

3.4.1 Non-idealities in growth

In this section we shall take a look at some of the deviations from ideal expected growths. These reduce the overall usable device yield and hence must be addressed before continuing to next steps. The techniques used to resolve some of these issues are detailed in section 3.5.1.

If we consider that figure 3.27 is an example of good growth, we see that all the multiple fingers of the array are grown sufficiently long ($> 1 \mu\text{m}$) and to larger contact regions on the right of the device. Moreover none of the fins seed from other than the silicon seed.

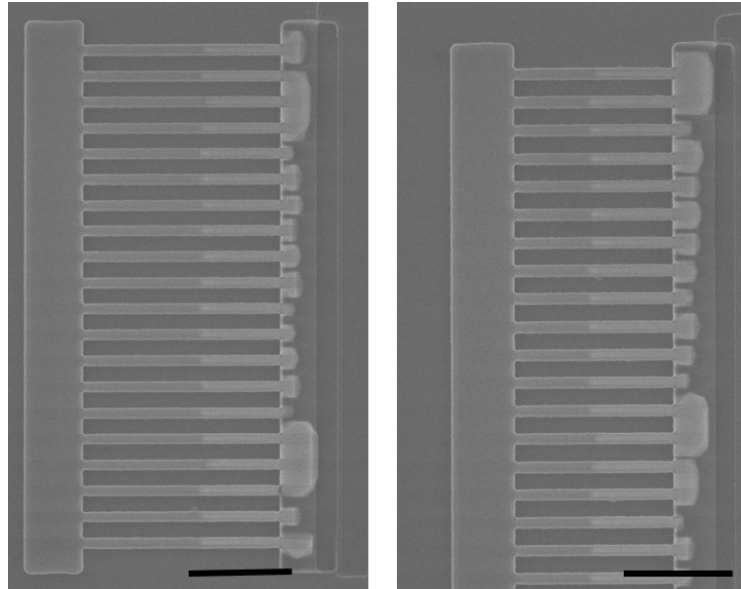


Figure 3.27 – SEM images show examples of good clean growths of multi-fin array with growth length larger than $1 \mu\text{m}$. Scale bar is $1 \mu\text{m}$ and $1 \mu\text{m}$.

However due to run-to-run variations there can be overgrowth as shown in figure 3.28(a) to (c). In figure 3.28(a) one can see that the device is covered entirely by InAs overgrowth and can be distinguished from a bad seeding shown by the arrow. In figure 3.28(b) the huge particle is clearly growing beyond the contact region while this occurs in a less aggressive fashion in figure 3.28(c). A highly undesirable scenario is also when InAs grows from other than Si seed but for example from the SiO_2 templated as indicated by the white arrows in figure 3.29(a) to (c).

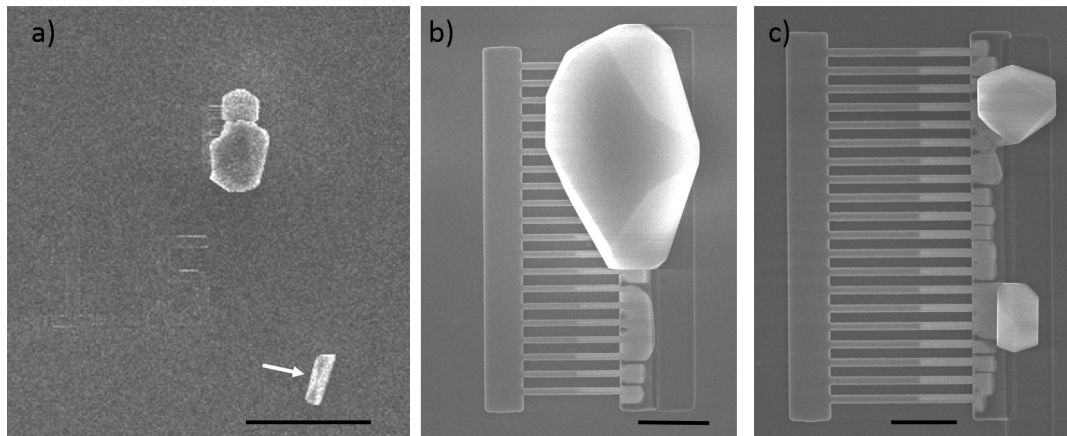


Figure 3.28 – SEM images showing a) overgrowth on the device and a parasitic growth on SiO₂ b) overgrown multiple fin structure. c) overgrowth from a clean device growth. Scale bar 10 μm , 1 μm and 1 μm .

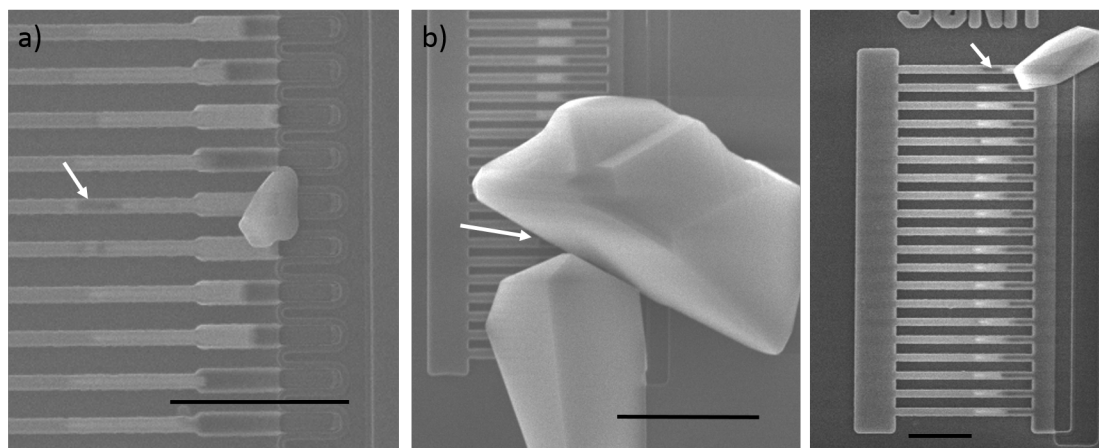


Figure 3.29 – Shown in SEM image a) is an arrow indicating a gap region then bad seeding of InAs most likely from partially removed silicon in the structure, b) is an outgrowth of InAs due to bad seeding than mere over growth with the arrow indicating the gap and c) another bad seeding that results in a fast over growth. Scale bar 1 μm , 2 μm and 1 μm .

3.5 Post growth processing

This section includes fabrication steps common to both electronic and sensing devices. When the processing for these two devices diverges, it shall be indicated.

3.5.1 Parasitic removal

Parasitic InAs particles that appear on the chip need to be addressed else the final device yield can be fairly low since they will interfere with the metallization. Seen in figure 3.30 is how the chip typically looks under an optical microscope right after MOCVD where the black dots represent unwanted large parasitic InAs growths. The various areas where they grow range from on the device region, on SiO₂, buried oxide between devices, over alignment marks possibly also interfering with alignment accuracy. It has been observed that adhesion of the growths on SiO₂ is fairly weak. In this case mild ultra-sonic bath in a heated beaker can remove a majority of these particles.



Figure 3.30 – Optical microscope image showing unwanted InAs growths all over the chip seen as the black dots

In figure 3.31 we see that cleaning the chip in a heated solution of 1165 remover and vigorously stirring it rids the chip of many unwanted growths.

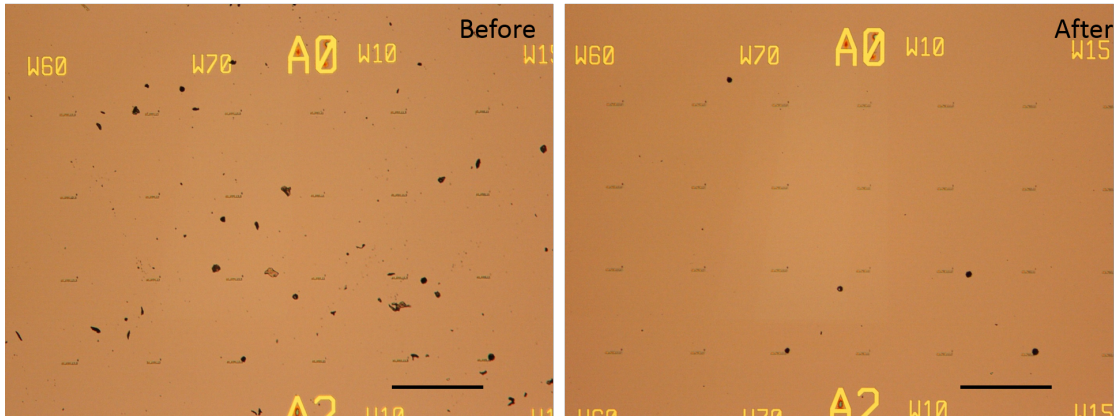


Figure 3.31 – Optical microscope images show before and after cases of using ultrasound and heat to clean unwanted InAs growths. Scale bar 300 μm and 300 μm .

While in some other cases ultra sound is not enough where the growth of unwanted particles is much widespread. On another chip shown in figure 3.32, ultra-sound treatment only minorly removes the unwanted growth as marked in encircled blue region.

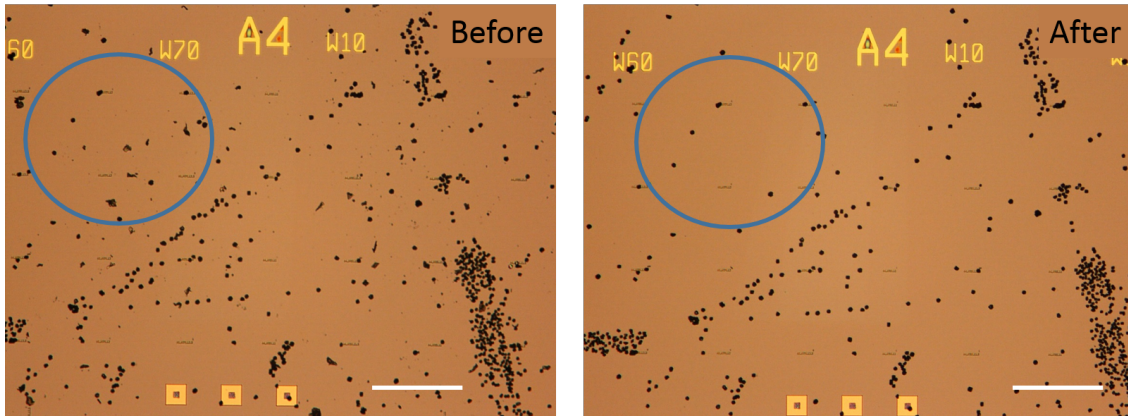


Figure 3.32 – Optical microscope image shows before and after case of using ultrasound and heat does not result to much variation except minor changes marked in blue circle areas. Scale bar 300 μm and 300 μm .

Therefore, a more mechanically aggressive approach has been conceived and used. A stick and peel UV-sensitive film is used. The time of exposure to UV light makes the glue of the UV-sensitive film less sticky can decide how less aggressive the peel becomes. The top face of the chip is placed to the sticky side of the tape. The whole assembly is cured under UV light for couple of seconds and then the tape is manually peeled off. Some results are seen in figure 3.33 where the final result is comparatively so much better than in figure 3.32.

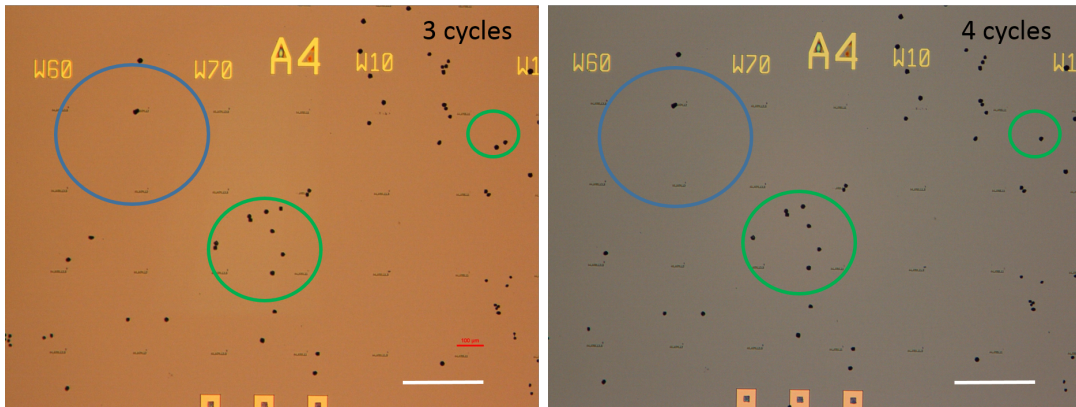


Figure 3.33 – Optical images same section as pictured in previous figure 3.32, before and after case of applying 3 and 4 cycles of UV-sensitive stick and peel tape steps. Differences are marked in blue and green circled areas. Scale bar 300 μm and 300 μm .

Pictured in figure 3.34 (a) and figure 3.34(b) is the same device zoomed out and in respectively after few cycles of stick and peel step. The black arrows indicate remnants of a previous parasitic particle. The white arrow indicates minor unwanted damage caused to an area. In this case, no damage is incurred to the grown device area. But this is not always the situation, with the stick and peel technique some good structures are also damaged as shown in figure 3.35(a) - (b). And it is always a question of trade-off between number of overgrowths to remove and number of good growths already on the chip that could be damaged in order to further improve the yield.

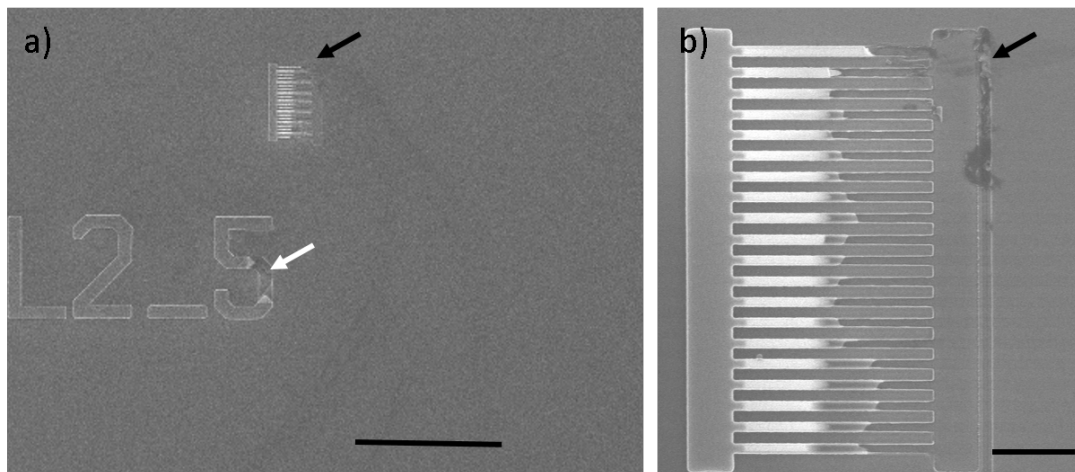


Figure 3.34 – SEM images showing damages showing same region a) zoomed out where black arrow indicate history of a removed unwanted particle, white arrow indicated unwanted damage b) zoomed in where black arrow indicates history of removed unwanted particle .Scale bar 10 μm and 1 μm .

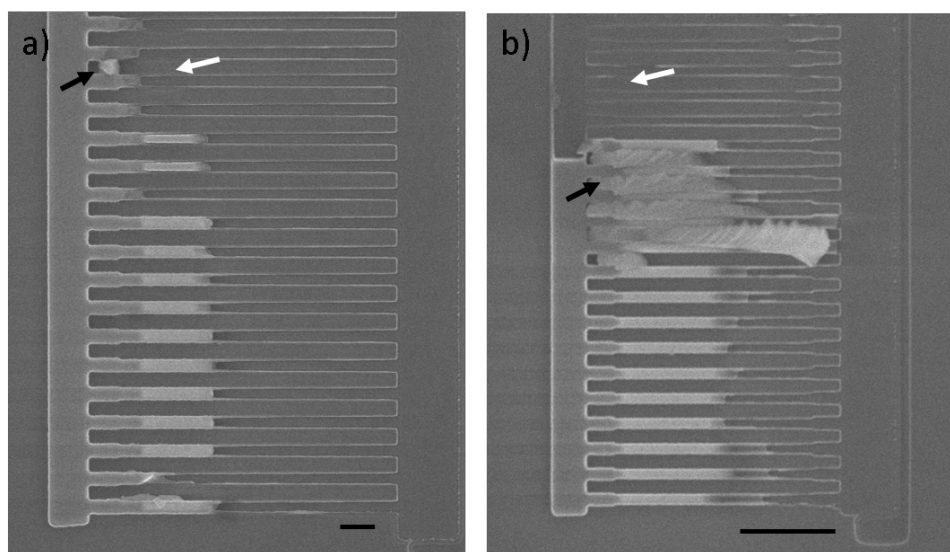


Figure 3.35 – SEM images of two different devices in a) and b) where white arrows indicate damage to grown structures whereas black arrows indicate the partially removed parasitic particles. showing Scale bar 300 nm and 1 μm .

Optical inspection & layout

In order to make up for variations in different process steps such as back etch length, growth rates, alignment inaccuracies due to drifts on e-beam tool we inspect and pick out the promising devices for metallization. However these variations can be reduced in a more commercial cleanroom setup. Then the processing will not have these manual customization steps. Before the contacts lithography, the chips undergo a DHF etch in order to thin down the template to the maximum. But still few nanometers of oxide remain to keep the structure intact during subsequent processing. We trim down to leave 10 nm oxide on all sides.

3.5.2 Source & drain lithography

This e-beam lithography step is carried out in order to align source and drain metallization and leave the channel region for gating. In this EBL step alignment is very critical. It decides the channel region length and also if there is sufficient growth length for source and drain regions. Otherwise, device yield can be drastically reduced at this stage. The parameters for PMMA used are as follows. An optical microscope image the PMMA contacts mask and the zoom of a well aligned mask is shown in figure 3.36(a) to (b).

- **Spin speed:** 4000 rpm
- **Resist thickness:** 450 nm

- **Resolution:** 5 nm, 50 nm
- **Current:** 20 nA, 150 nA or 200 nA
- **Dose:** 1200 $\mu\text{C}/\text{cm}^2$
- **Proximity effect correction parameters:** $\beta = 33 \mu\text{m}$, $\eta = 0.5$

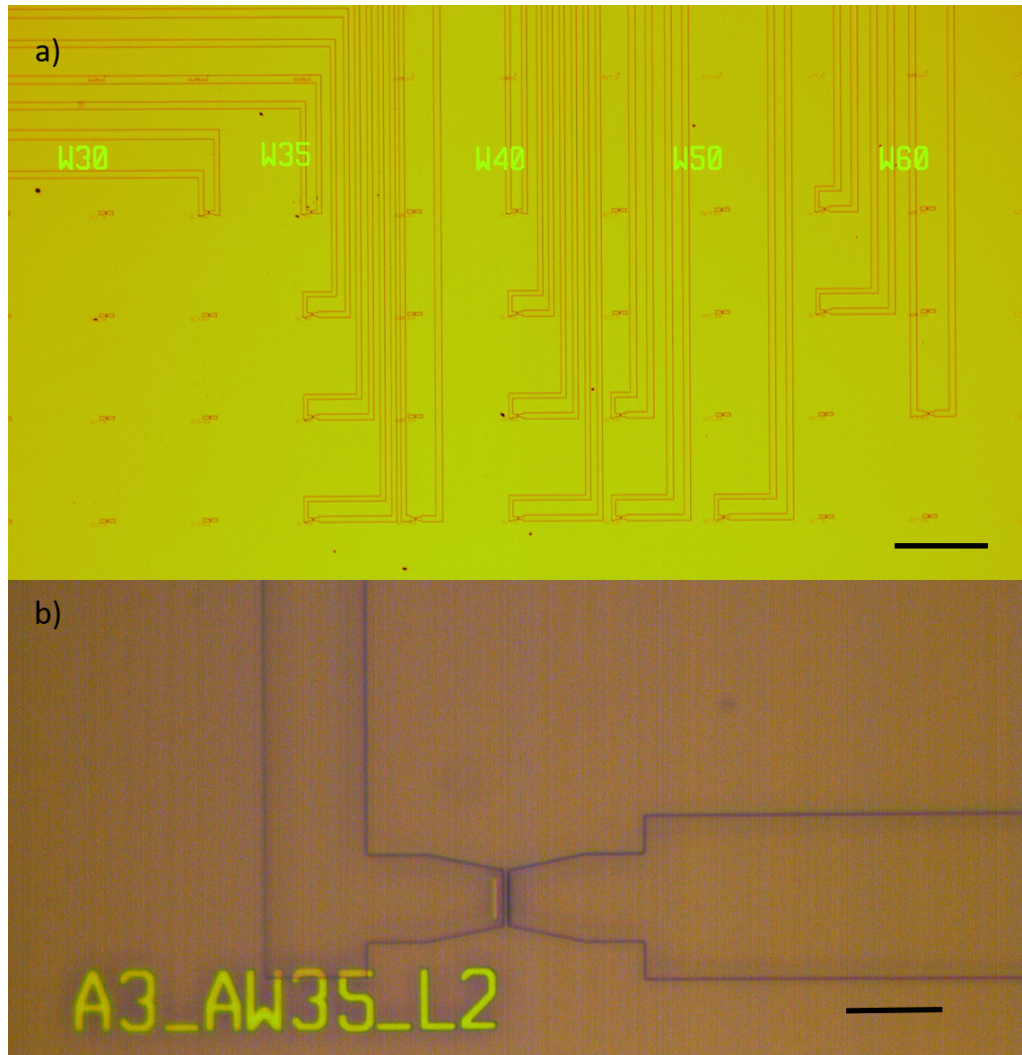


Figure 3.36 – Optical microscope image showing a) source and drain contact lithography in PMMA resist and b) zoom in on one device. Scale bar 300 μm and 15 μm .

3.5.3 Source & drain metallization

A DHF etch step is carried out before the sample is taken to the evaporation chamber. This is to ensure that there is no oxide on the source and drain contact region. Sulfur passivation to control native oxide growth was carried out on some initial chips. But it was noticed

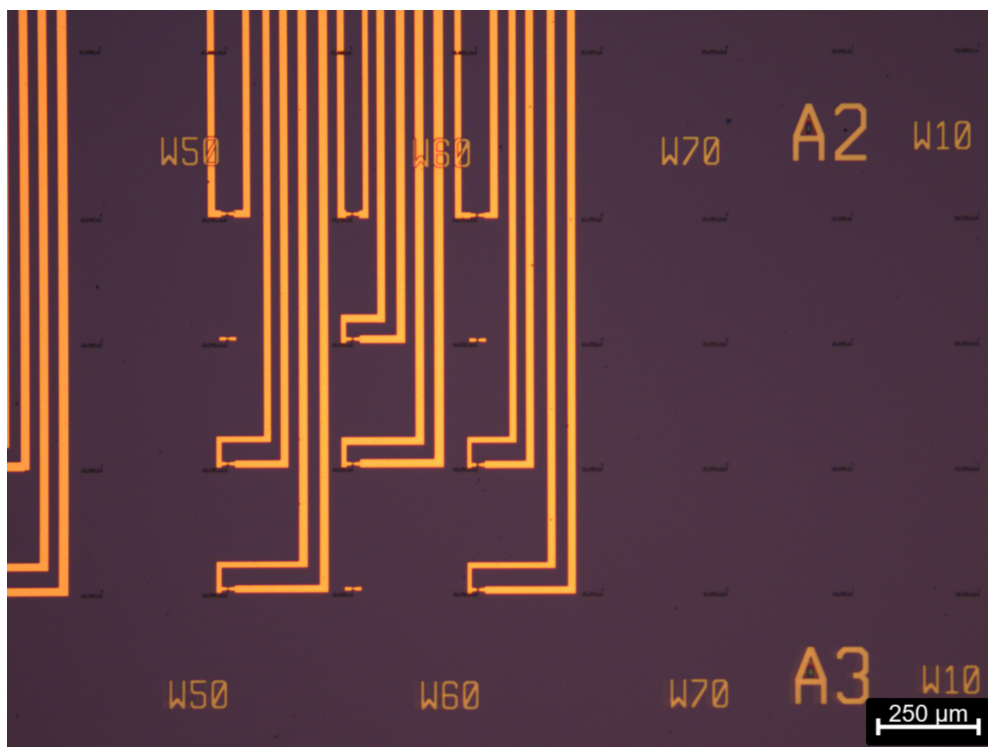


Figure 3.37 – Optical microscope image after metallization of source & drain areas. Scale bar is 100 μm

that the PMMA resist delaminates quite often not resulting in a good reproducibility of the lift-off. Instead, the samples were transported in a vacuum transfer box to the evaporation chamber to limit the native oxide formation. As will be seen in measurements, currents in the microampere range were obtained for even millivolts of drain voltage. Therefore, 20 nm of nickel adhesion layer and 130 nm of gold was evaporated to contact the devices. Then the chip was left for lift-off in 1165 solvent with cycles of heat treatment but without ultra-sonication. The results are seen in a clean lift-off in figure 3.37, figure 3.38 and figure 3.39.

3.5.4 ALD isolation & pad opening

Final step is deposition of the high-k oxide using atomic layer deposition (ALD). 20 nm of HfO_2 was deposited at 200 °C in a ultra-high vacuum thermal ALD chamber. The thick ALD layer is chosen since the oxide also serves as an isolation of source and drain metal from the channel region. The last step is accessing the contact regions for the measurement probes. Hence, the high-k oxide over the 150 μm X 150 μm source and drain contact pads is selectively removed using a photolithography mask and DHF etchant.

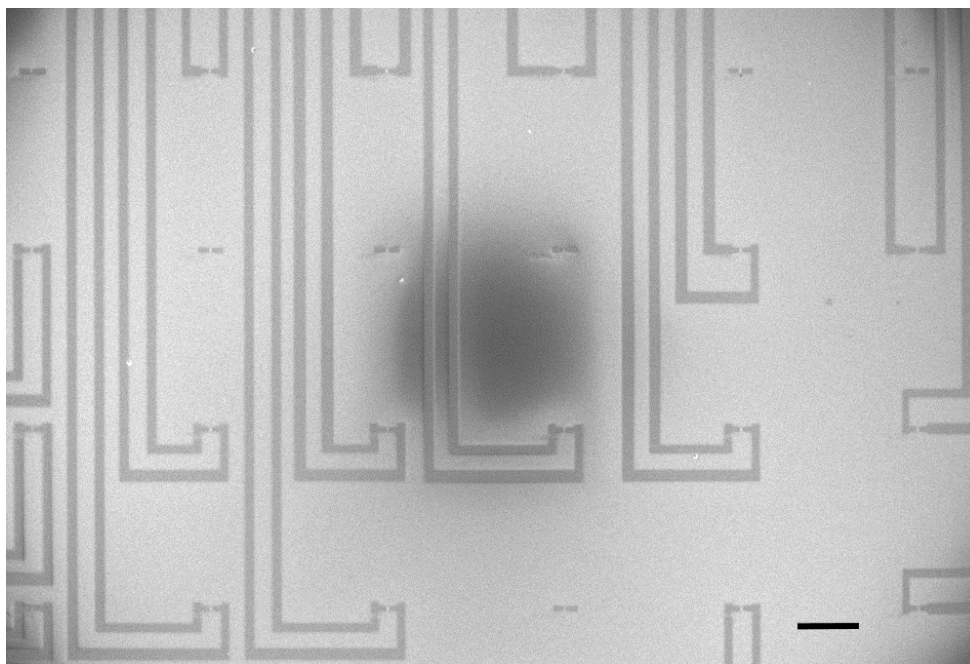


Figure 3.38 – SEM image after metallization of Source & Drain areas. Scale bar is 100 μm

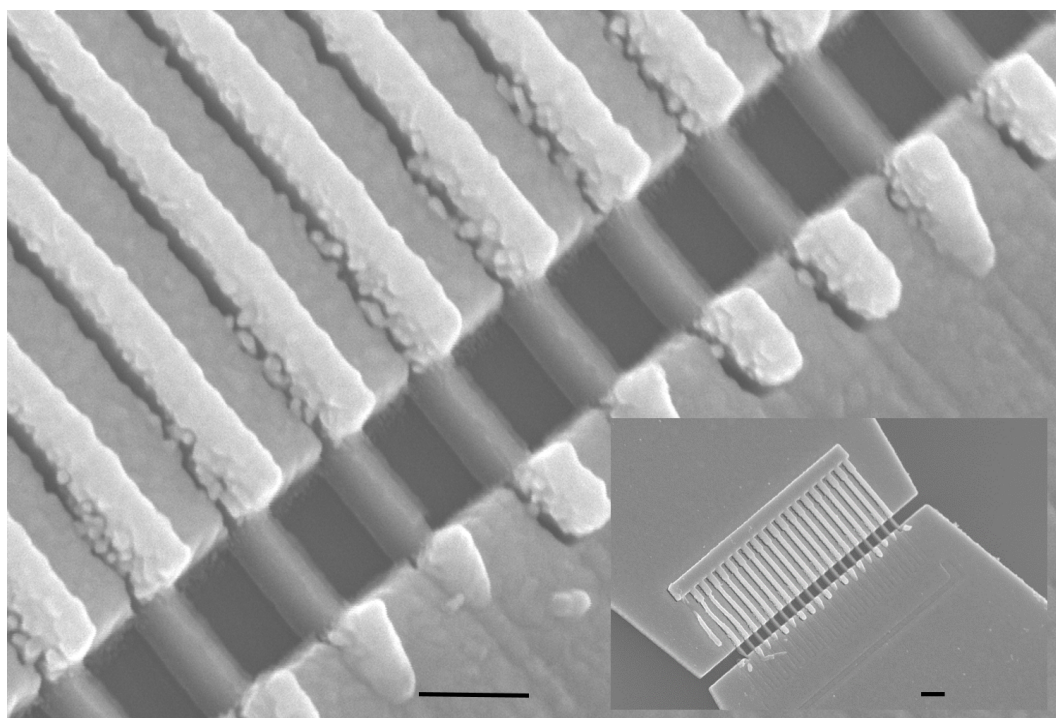


Figure 3.39 – SEM image of a zoom in of source and drain metallization on a single device, in the inset a zoom out of the entire device with pads is seen. Scale bar is 200 nm and 300 nm for inset.

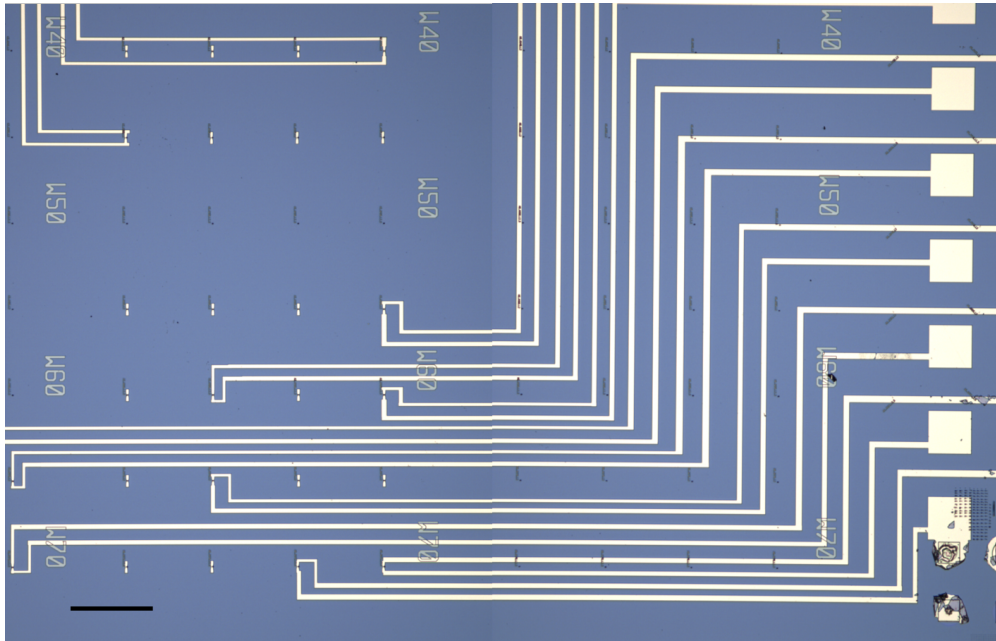


Figure 3.40 – Optical microscope image shows source and drain metallization on many devices leading to the large $150\text{ }\mu\text{m} \times 150\text{ }\mu\text{m}$ contact pads. Scale bar is $300\text{ }\mu\text{m}$.

3.6 Summary

This concludes the technological development steps for the ISFET design devices. A chip after complete fabrication is photographed in figure 3.41. After successful epitaxial growth using horizontal TASE of the unique high-aspect ratio fin geometry for the first time the results were reported at the Silicon Nanoelectronics workshop (2018) as a poster presentation [93]. The completely fabricated devices will here-on be referred to as InAs-on-insulator (InAsOI) FinFETs. In the next chapter we see measurements on some of these devices. Summarizing the findings in this chapter, the template-assisted epitaxy technique (1) enables horizontal templates for fin growth independent of in-plane growth direction and (2) is scalable at least down to 20 nm silicon fin width (30 nm InAs fin width). The main technological achievements are summarized in table 3.1.

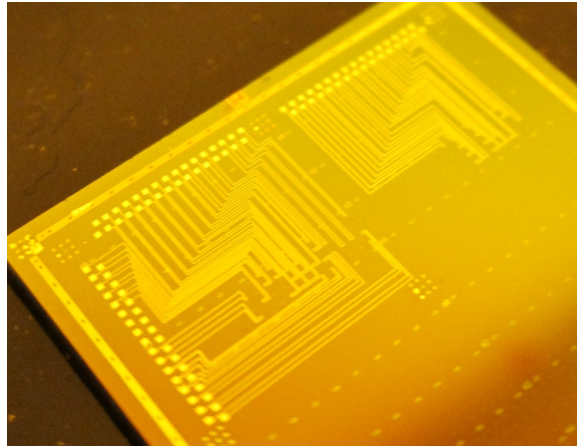


Figure 3.41 – Photograph of a chip after complete fabrication

		Parameter	Value
Technology Development [Rupakula et al., SINW2018]	1	Fin Aspect ratio ($H_{Fin}: W_{Fin}$)	4:1
	2	Fin width (W_{Fin}) scaling	80 nm to 30 nm ; Demonstrated a scalable process
	3	Dense Integration	20 fins; where effective area > planar area
	4	Device placement	Up to 30 nm accuracy
	5	III-V Integration Scheme	Local integration, Catalyst-free, on Insulator process
	6	Substrate	Silicon Monolithic Integration
	7	CMOS Compatibility	Temperature, Materials, Process

Table 3.1 – Summary of the technology development achievements from this chapter.

4 Measurements & Discussion

All the measurement results presented in this chapter are from the same batch of chips used to test all the process steps detailed in the previous chapter 3. However, the measurements are also from the last set of chips exhausting the fabricated wafer. A first characterization of the InAsOI FinFETs as pH sensors is demonstrated in section 4.1. The limitations in device performance are discussed in section 4.1.3. In order to probe differently the devices, an ad-hoc characterization with a metal gate deposited using the focussed ion beam (FIB) tool is carried out in section 4.2. However, this method consumes time, resources and requires a precision level that becomes tedious to repeat another time for metal gates. On the other hand, ionic liquid (IL) gating was proposed and tested as means of studying device behaviour as detailed in section 4.3. Since IL gating, a non-standard technique is relatively less explored, the behaviour of IL is first extensively confirmed on silicon devices in particular SOI ribbon FETs and then applied to our InAsOI FinFETs. The SOI ribbon FETs used in IL measurements were fabricated and kindly provided by Nanoelectronic devices laboratory colleague, Francesco Bellando. Also the pH response and metal gate response measurements on the SOI ribbon FETs were carried out by Francesco. The author carried out all the IL measurements.

4.1 InAsOI FinFETs as pH Sensor

4.1.1 ISFET Characterization Setup

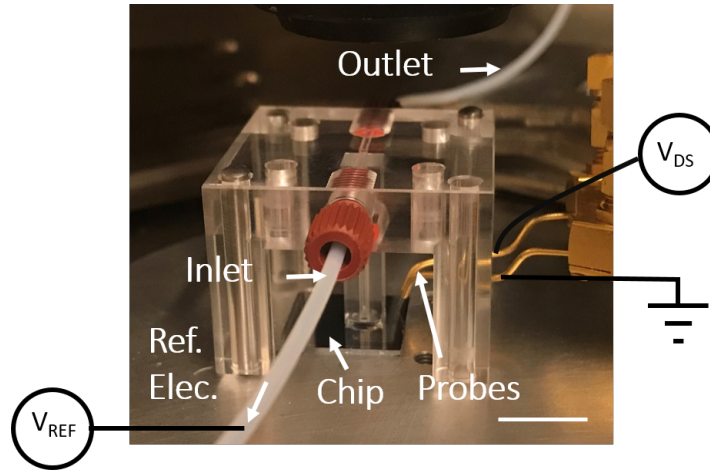


Figure 4.1 – Fluidic measurement setup. Scale bar is 1 cm.

Two types of setups were used interchangeably for pH measurements. The first setup is shown in figure 4.1. It consists of a fluidic holder made in acrylic plastic with the inlets and outlets aligned to the chip placed beneath it. The inlets and outlets allow for the liquid under test to enter and leave the region of interest on the chip. The inlet also houses the reference electrode. The probes seen in gold colour contact the metal source and drain pads located at the extremities of the chip. Liquid pH solutions are exchanged manually via the inlet. The pH solutions were flushed by going from higher pH (lower concentration) to lower pH (higher concentration). The source and drain probes were connected to a precision semiconductor parameter analyzer (Agilent, 4156A) and the entire unit is housed on an electrically shielded cascade probe station (Cascade microtech Inc., Summit 12000). The measurement controls i.e the electrical parameters applied to the probes are mediated by software interface IC CAP (Keysight Technologies).

This pre-fabricated fluidic unit was specifically fabricated for other chips designed for ISFET measurements in our lab. In fact the wiring layout of our InAsOI FinFETs was adapted in order to make measurements using this fluidic unit. But the measurements posed a couple of persistent problems: 1) It was not straightforward to align devices of interest under the O-ring which had to be done under an optical microscope. Further, to switch between devices in different regions of interest, it required dismantling the setup, re-aligning under a optical microscope to re-clamping the O-ring of the fluidic setup to our chip. 2) Moving the probe tips between contact pads of different devices turned to be non-trivial as they were frequently constrained by the tall pillars. Hence, switching between measurements to identify working devices became a hassle.

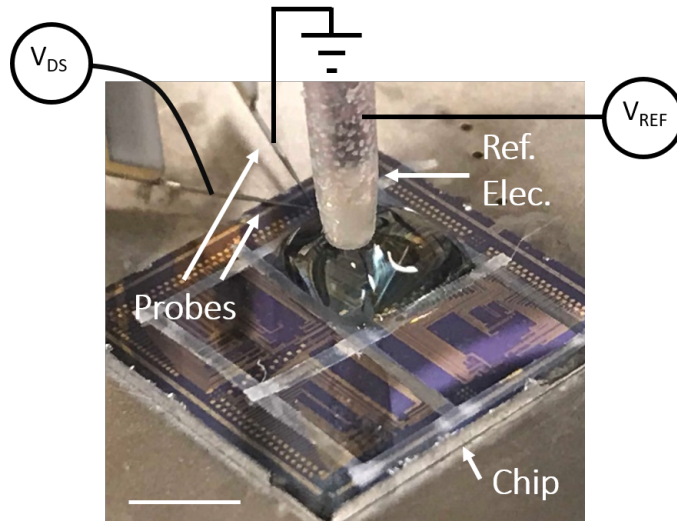


Figure 4.2 – Droplet setup for ISFET measurement

To characterize the prototyped devices in a fast and efficient manner a second setup was preferred for most experiments and it is shown in figure 4.2. As seen in the image, in this open system the type of experiments performed were more restrictive. Short term experiments were still feasible ensuring reliable, repeatable and multiple read-outs. However long term measurements such as stability could not be setup in this configuration. Though the setup appears makeshift it contains all the elements to carry out the measurements reliably and in a reasonable time. The liquid drop is contained by plastic tape around the devices in the region of interest. In order to exchange different pH solution blotting paper is used to absorb old pH solution and new pH solution is manually pipetted to form the large droplet.

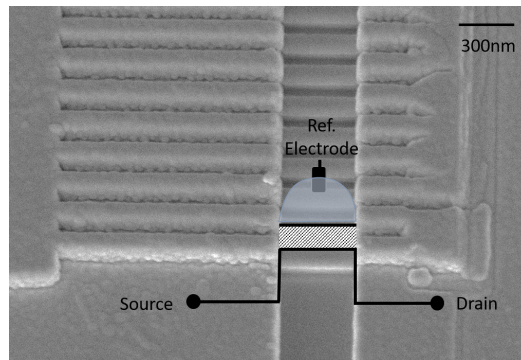


Figure 4.3 – SEM image show s source and drain metallization on complete device and also how the measurement is carried out on the device.

As seen in the figure, the droplet holds very well with the reference electrode, without discernible change in volume even after an hour of letting it be at room temperature in an uncontrolled room environment. In figure 4.3 we can see the ISFET measurement electrodes

super-imposed on a SEM image of an individual device.

4.1.2 ISFET Measurements

InAs FinFET sensor response to pH is presented and analyzed in this section. Couple of devices were characterized and trends were studied are reported in order to proof the concept. No chemical modification of the surface has been performed. The pH buffered solutions were prepared in house. The values of pH solutions were verified using a commercial pH meter. The common device parameters for the following measurements are stated here. Only the differing parameters will be stated subsequently.

- FinFET height = ~ 130 nm
- Device length = ~ 1 μm
- Channel length = ~ 0.5 μm
- Number of fingers = 20
- Pitch = 250 nm
- Device isolation = 20 nm of ALD HfO_2
- pH Buffer = 100 mM phosphate buffer solution (PBS)
- Buried oxide thickness = 2 μm , not used

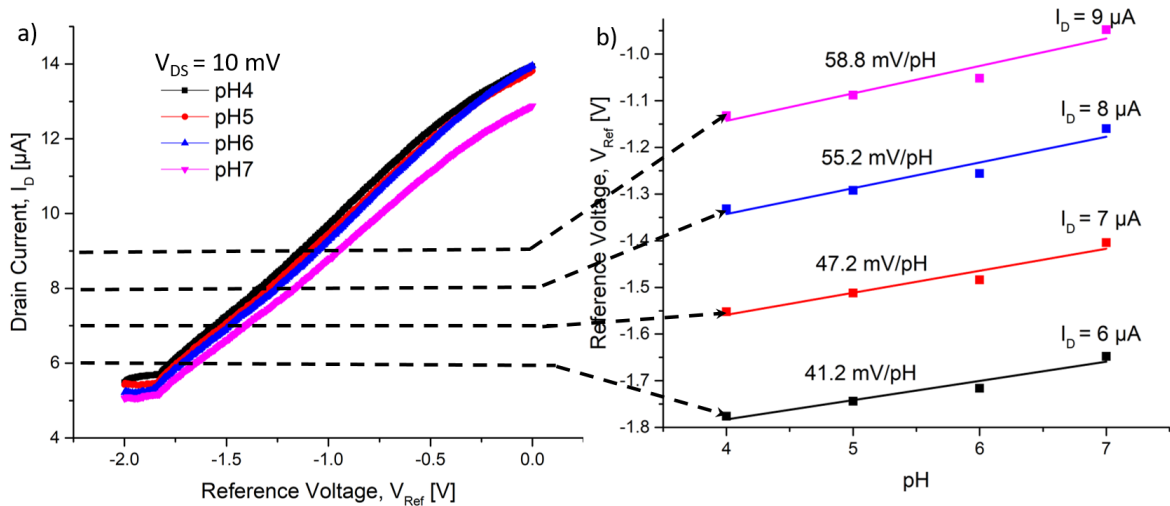


Figure 4.4 – a) pH response of the device and b) voltage sensitivity extraction for the same 40 nm wide fin.

For a device with FinFET width = ~ 40 nm (Device A), shown in figure 4.4(a) is the pH response and drawn to the right in figure 4.4(b) is the sensitivity response extracted at different current levels. Each pH curve is reported after several measurement iterations to pass, allowing the curve to stabilize. The pH values decreasing from pH 7 to pH 4 (increasing H^+ concentration) changes the surface potential distribution ($\Delta\phi_s$) and in turn changes the threshold voltage of the device as seen in a systematic left shift of the transfer curves. The voltage sensitivities also confirm the device nernstian response. Though there is deviation for pH 7 response, a linear fitting of the points shows a high linearity in the range of pH 4 to pH 6. At lower drain current values the response of pH 7 becomes more linear as well and hence we extract voltage sensitivity of 41.2 mV/pH at 6 μA where the entire pH range is more linear to an accurate value.

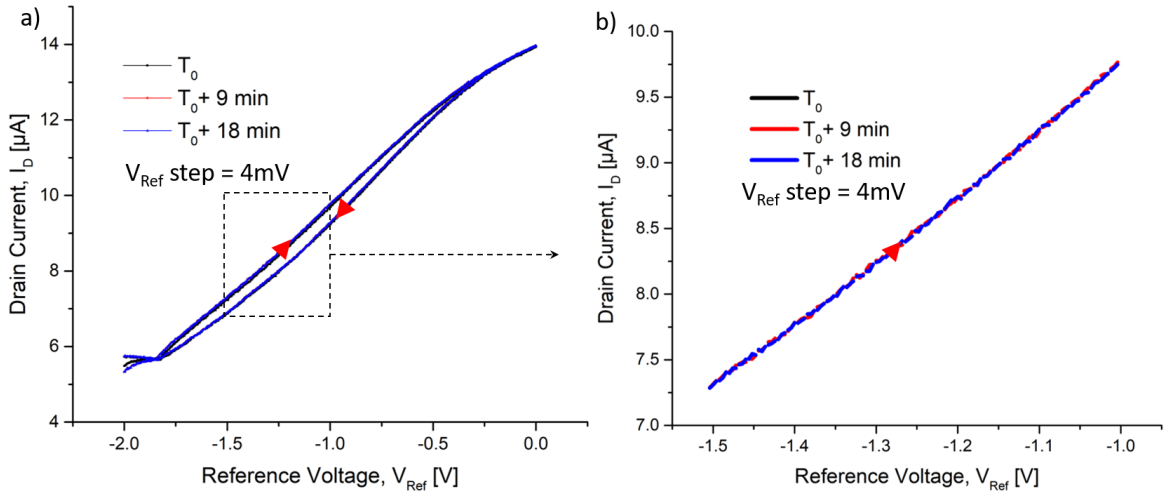


Figure 4.5 – a) At pH 4 repeatability of pH response for different time points in a voltage interval and b) pH response curves repeatability for the entire voltage sweep also showing hysteresis.

In figure 4.5(a)-(b) measurement repeatability is verified for device A, whose pH response is reported previously. The arrows represent the forward and backward sweeps. In figure 4.5(a), for pH 4, the response curve for the entire voltage interval ($-2 \text{ V} < V_{Ref} < 0 \text{ V}$) with hysteresis is shown. The analysis of hysteresis is given shortly after. First, even in the open system setup shown in figure 4.2 the volume of the drop does not change in any noticeable fashion in this 20 minute interval enabling reliable measurements. Secondly, the pH 4 response curves shown in black, red and blue at the three different times 9 minutes apart are practically indistinguishable. For the same pH 4 response, we can zoom in on a select voltage interval ($-1.5 \text{ V} < V_{Ref} < -1 \text{ V}$) as in figure 4.5(b) again and confirm that there is no noticeable shift in the responses at three different timestamps.

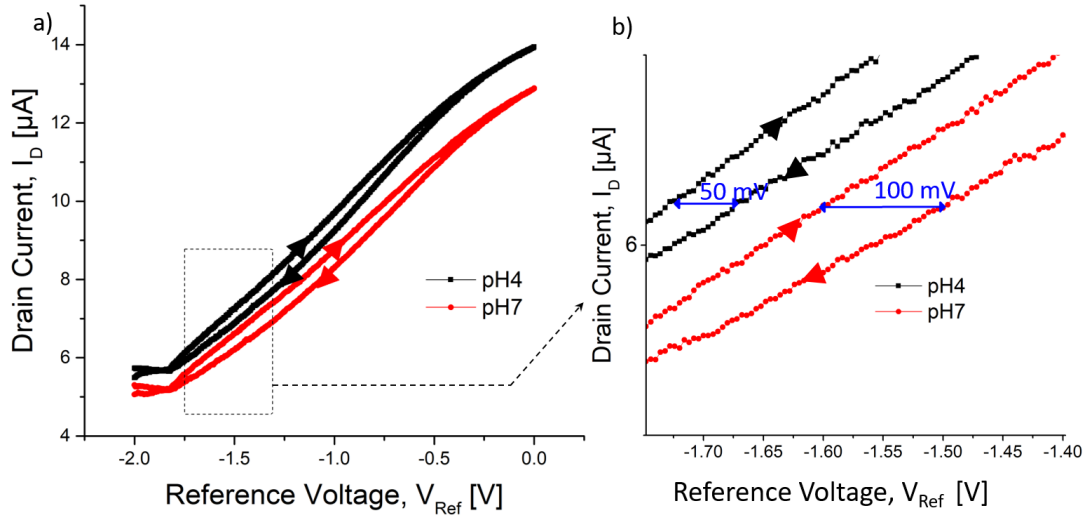


Figure 4.6 – a) At pH 4 repeatability of pH response for the entire voltage sweep also showing forward to backward sweeps and b) pH response repeatability at pH 4 for different time points in a select voltage interval.

In figure 4.6(a)-(b) we focus on the hysteresis response of device A. In the figure 4.6 the loop of voltage sweep for 2 pH values i.e pH 4 and pH 7 are demarcated in the black and red curves. In the zoom of figure 4.6(b) the hysteresis is calculated to be 50 mV for pH 4 curve and for pH 7 whose response shows more deviation than other values it is calculated to be about 100 mV. The origin of hysteresis is drawn in figure 4.7. There most likely are interface defects between the deposited SiO_2 and grown InAs layer but also between the remnant SiO_2 and deposited HfO_2 . A first solution to counter the hysteresis is to engineer the interface of oxide and semiconductor. The template SiO_2 can be created by oxidation of the silicon fin rather than by just an oxide deposition. In our case, for a high aspect ratio structure to endure the oxidation-etch cycles one would need some time to optimize the right parameters hence deposited oxide was chosen. On the other hand, deposited oxide is relevant when moving to stack up devices in 3D and growing III-Vs from polysilicon and not only from monocrystalline silicon. A more detailed study of the hysteresis with the sweeping speed is carried out in section 4.3.

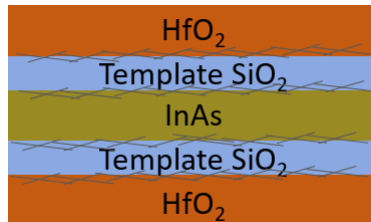


Figure 4.7 – Cross section illustration of device pointing to likely interface defects resulting in hysteresis in transfer characteristics.

In literature of InAs NW sensor devices, there are few instances of reports on double sweeps or hysteresis values let alone quantification. Among these we can make a rudimentary comparison. Upadhyay *et al.* mention of a large hysteresis but quantification is not provided. On the other hand, Zhang *et al.* report values of hysteresis as large as 17.8 V, in their case a back gate has been used [58]. Also, in Offermans *et al.* a value for hysteresis in the order of 20 V is also reported [53] again with a back gate operation and the hysteresis is attributed to the top sensing interface of InAs/In_xO_y. It is mentioned that this value is similar to that reported by Du *et al.* [52].

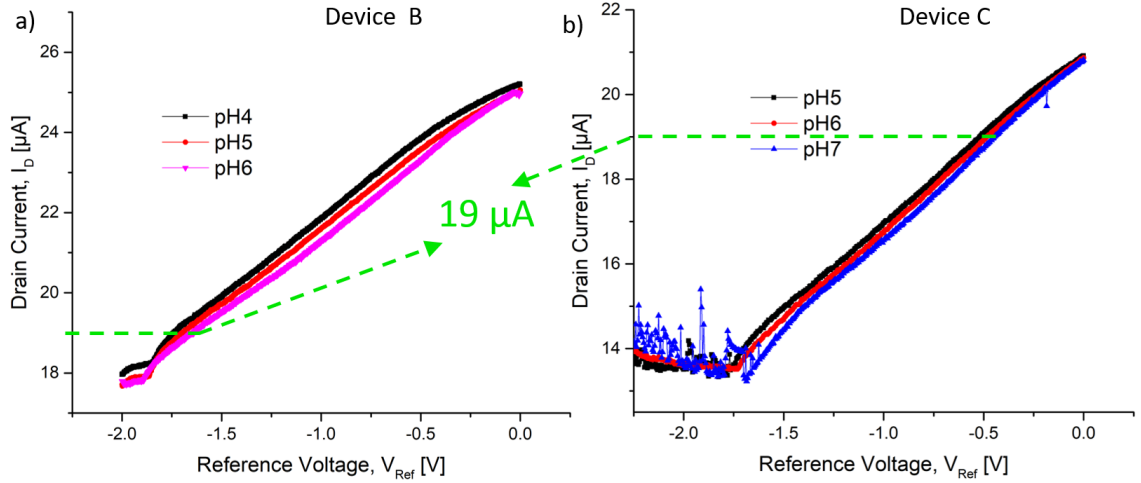


Figure 4.8 – pH response curves for a) device B and b) device C.

In figure 4.8(a)-(b) we compare two other devices (B and C) with similar geometry i.e. fin width = 70 nm. It is visible that the device ON and OFF current levels are similar with only minor differences arising perhaps due to variations in contact resistance. Also, the modulation region is about 30 % in both of them. For the device B three pH values pH 4, pH 5 and pH 6 were measured and for device C pH 5, pH 6 and pH 7 were measured.

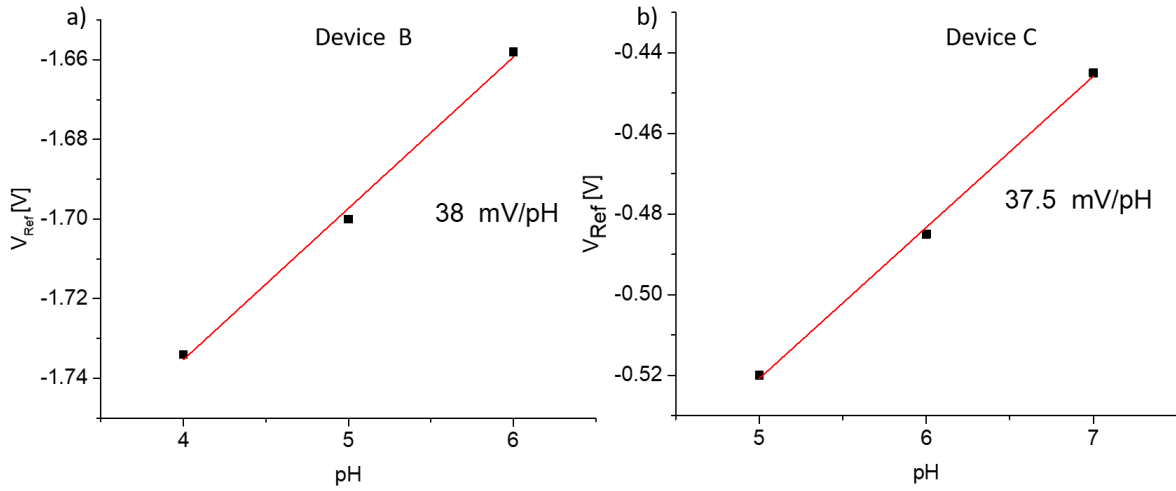


Figure 4.9 – Sensitivity extracted at $19 \mu\text{A}$ for a) device B and for b) device C.

In figure 4.9(a)-(b) the sensitivity is extracted at a current level for example $19 \mu\text{A}$ which is present in both the devices in order to make a fair comparison. It is evident that the sensitivity in both the devices is extracted to be almost equal at 38 mV/pH . The fitting of the points indicates a good linearity in the measured pH range. Moreover, these values for sensitivity agree quite well with that extracted for device A of 41.2 mV/pH . A marginally better sensitivity of 41.2 mV/pH is extracted for device A which is the narrower fin. Again, a confirmation of the hysteresis is shown in figure 4.10. The value is again less than 100 mV similar to that calculated for device A.

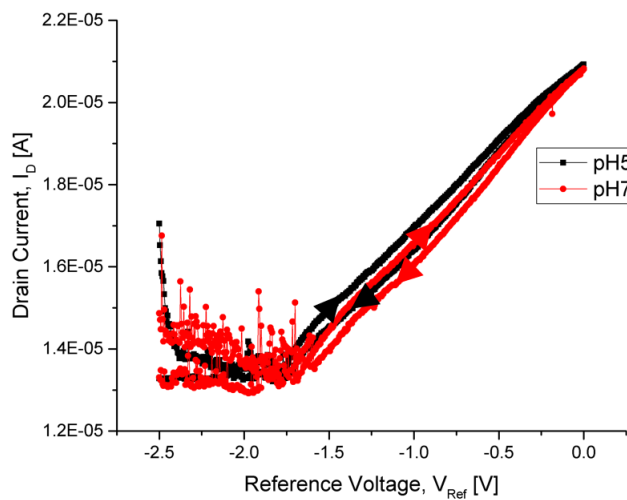


Figure 4.10 – Hysteresis in device C for pH 5 and pH 7.

4.1.3 Discussion

In this prototyping phase, a response to pH well in the Nernst limit is seen in the handful of InAsOI FinFETs characterized as sensors. The measurements were repeated many times at different time intervals to confirm the response. However, more number of devices need to be measured in a subsequent fabrication batch to speak of device to device variability in detail and carry out a more in-depth statistical analysis. It is clear from the curves in figure 4.4(a) and figure 4.8 that the devices are only partially depleted. For the 70 nm wide fins (device B and C) the ON current modulation is only about 30% whereas for the narrower 40 nm fin (device A) the modulation improves to about 50% of ON current. In order to probe this partial modulation additional characterization needs to be performed on remaining devices. We used first tried an ad-hoc characterization using a metal deposited from focussed ion beam (FIB) tool and then more characterization with ionic liquid gating.

4.2 Ad-hoc Characterization

A simplified overview of the principle of electron beam induced deposition (EBID) of metal is shown in figure 4.11. The metal+organic compound molecule is introduced using a gas injector into the chamber and the electron gun is focused on the target site of deposition. At the target site the electron gun burns the volatile organic pre-cursor molecule while the non-volatile metal grows on the substrate.

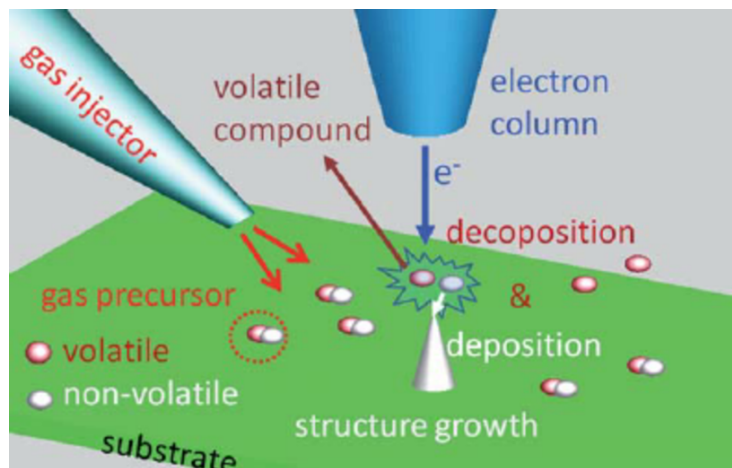


Figure 4.11 – Schematic of FIB Deposition Principle

EBID of platinum (Pt) metal on our structures is shown in figure 4.12. The placement accuracy of the Pt gate is appreciable in the SEM image on a 70 nm wide fin. This was only possible after several trial and miss alignment attempts. In figure 4.13 the transfer curve on one such device is shown. Only 15% modulation of the ON current is seen not very different from previous pH measurements. This could likely be due to large cross section that

is not depleted but also is highly likely that the Pt gate covers only partially the fin sidewalls and cannot control the entire height of the fin. Moreover, one cannot rule out the possibility that remnant hydrocarbon molecules in the Pt do not lead to a continuous gating over the channel. This patterning turns out to be tedious requiring time and skill for the alignment and imaging procedure. A simpler technique is necessary to characterize the devices in a more straightforward fashion and IL gating was explored for this reason.

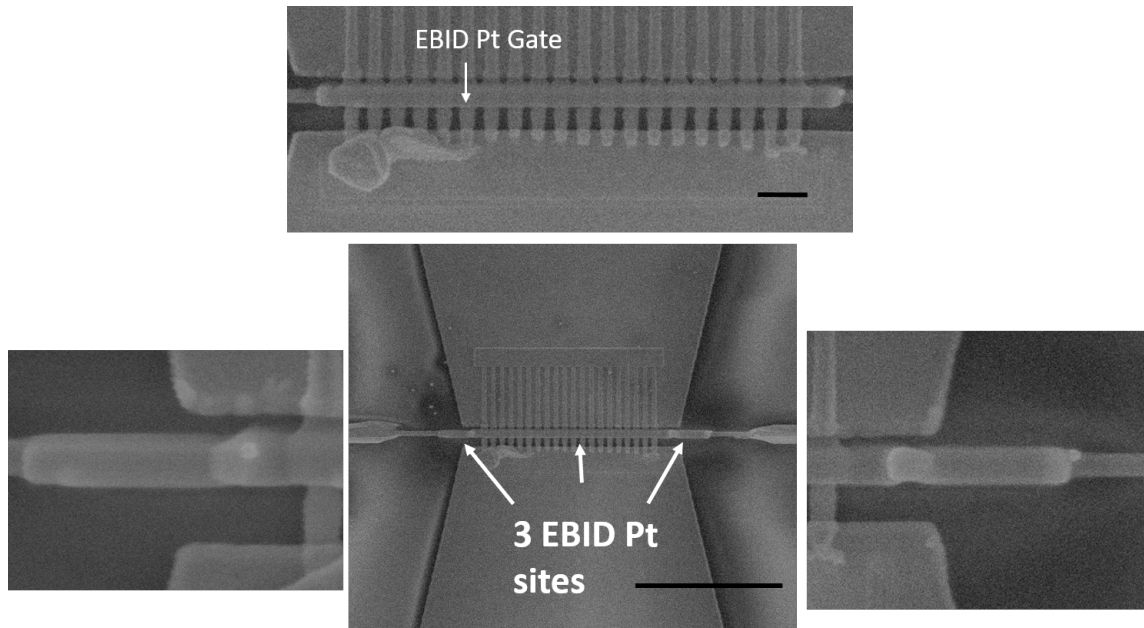


Figure 4.12 – SEM right after EBID Pt deposition process. Scale bar 500 nm and 4 μm .

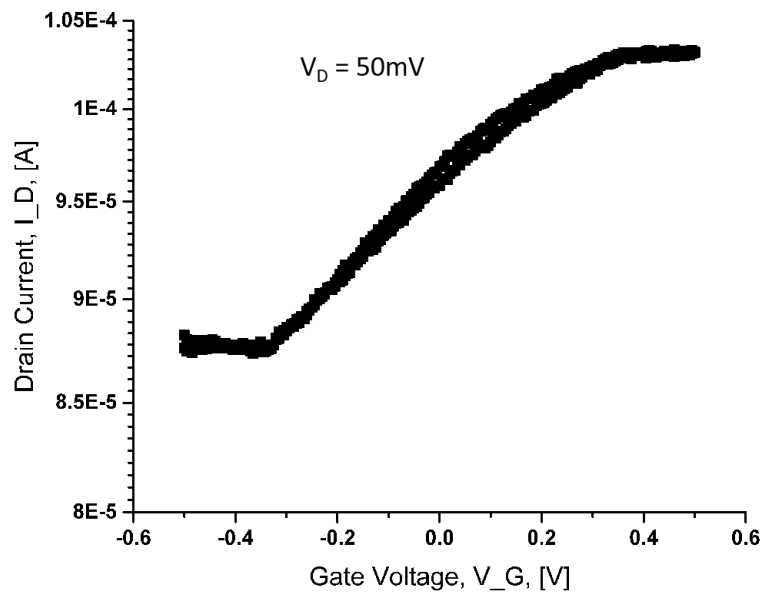


Figure 4.13 – I_D - V_G characteristics from a EBID Pt gate modulated device

4.3 Ionic liquid gating measurements

The setup for ionic liquid (IL) gating measurement is shown in figure 4.14. High precision tips are used to contact the source and drain regions and a tungsten probe is used to apply a potential to the IL. The IL used is EMIM TFSI (1-ethyl-3-methylimidazolium bis(trifluoromethylsulfonyl)imide) commercially purchased from Sigma-Aldrich. The two sets of devices as will be seen in section 4.3.1 and section 4.3.2 are characterized using this IL:

- SOI ribbon FETs
- InAsOI FinFETs

Characterization of the IL functioning on conventional silicon and better performing devices will pave the way to explore this relatively unconventional gating substance of IL. The comparison of pH response and IL response on these silicon devices enables a another level of confirmation of IL gating behaviour. After these checks, the IL was applied to our InAsOI FinFETs.

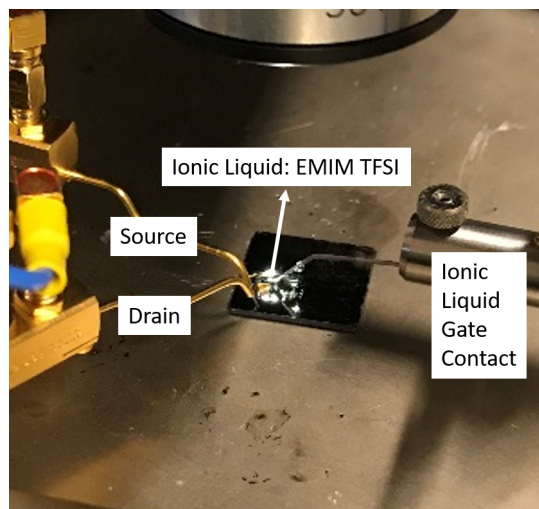


Figure 4.14 – IL Measurement Setup

4.3.1 IL Measurements on SOI Ribbon FETs

The measurements reported in this section were carried out on the SOI Ribbon ISFETs. They are n-type fully depleted SOI ribbon FETs. The structure, fabrication process and device characteristics are published in detail by Garcia *et al.* [12]. However, a summary of the process flow is shown again here in figure 4.15(a)-(f). Finally, the optical microscope image of a complete device is shown in figure 4.16.

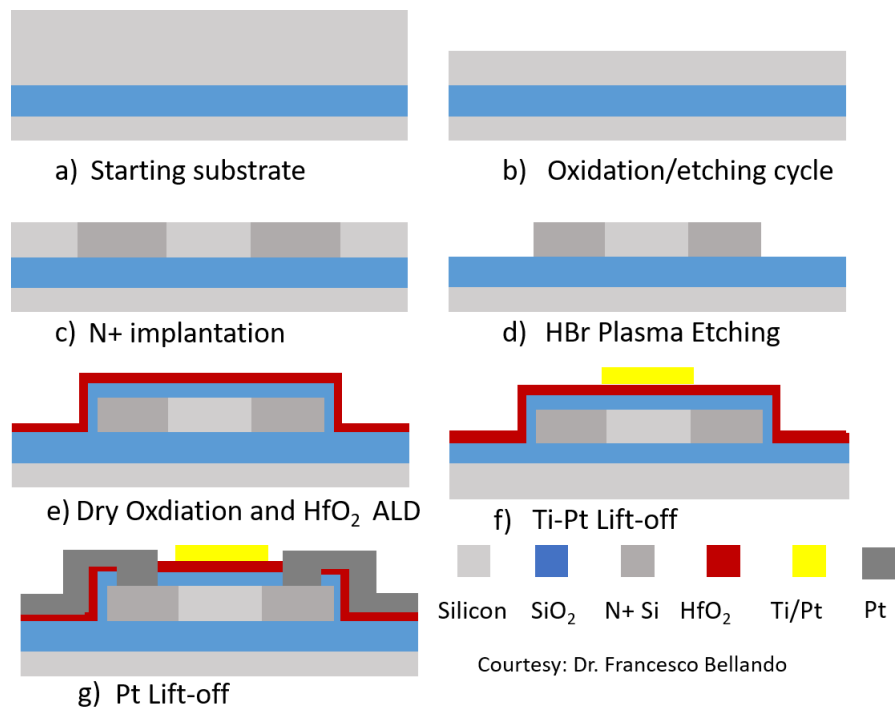
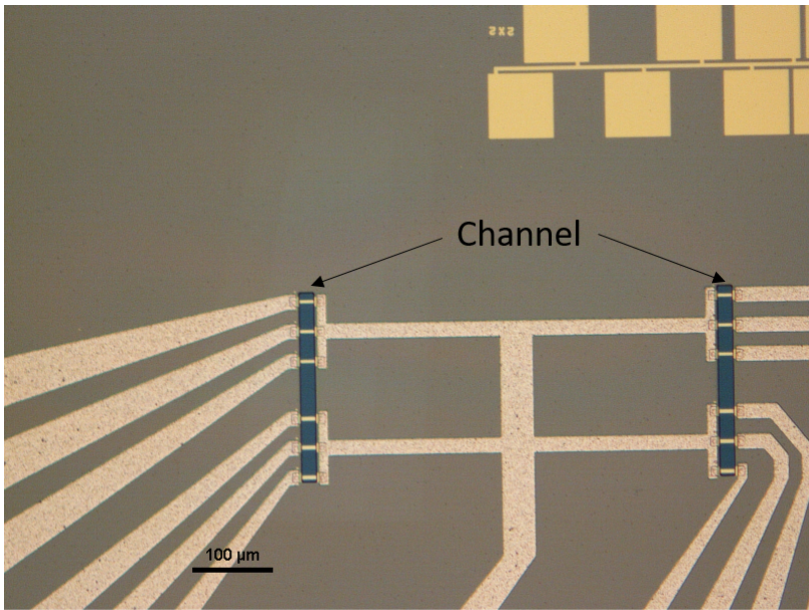


Figure 4.15 – Main steps in fabrication process of SOI Ribbon FET.



Courtesy: Dr. Francesco Bellando

Figure 4.16 – Main steps in fabrication process of SOI Ribbon FET.

In figure 4.17 and figure 4.22 the transfer characteristics in linear scale is shown for two

4.3. Ionic liquid gating measurements

different devices. These sets of results help us confirm the working of IL before applying it to the InAsOI FinFETs fabricated in this thesis work.

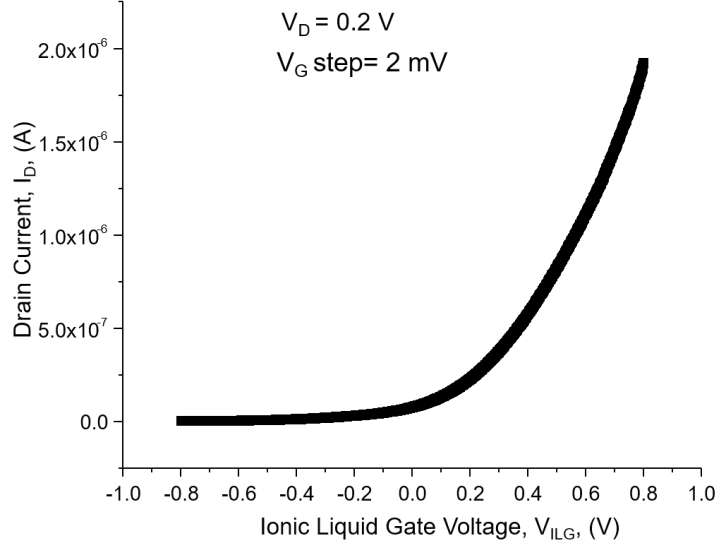


Figure 4.17 – SOI Ribbon FET transfer curve response to IL gating

In figure 4.18(a)-(b) in semi-log scale, the transfer characteristics of SOI Ribbon FET 1 using IL gating and the liquid pH is seen. In both cases the ON and OFF current values are very similar in the range of few microamperes and few nanoamperes, respectively. The current ON/OFF ratio is similar in both the cases and nearly three orders of magnitude. The SS for IL gating is about 533 mV/pH and for pH response is about 266 mV/pH. This difference in sub-threshold slopes arises due to the different capacitances in play between the liquid gating and sensing oxide interface of both the systems.

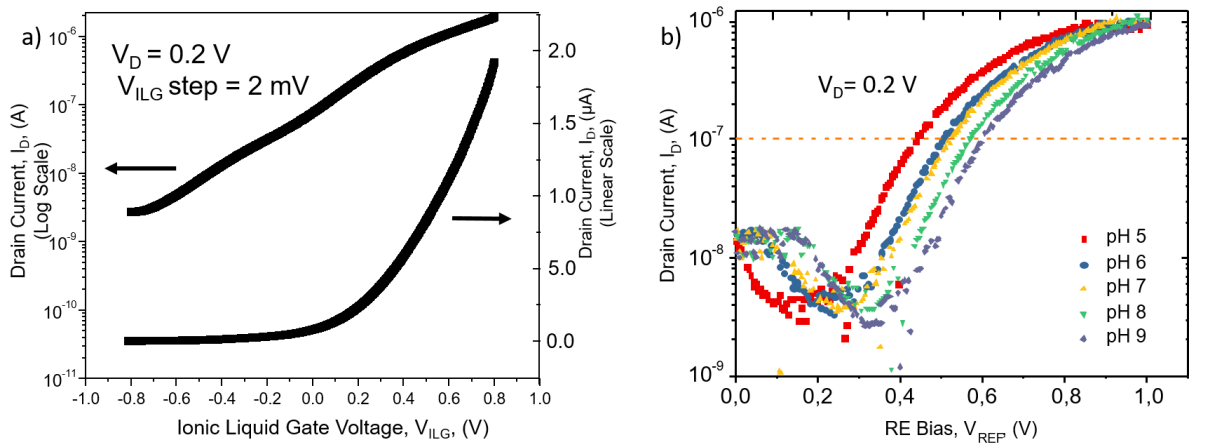


Figure 4.18 – SOI Ribbon FET1 IL response versus pH Response

The output characteristics of the same SOI ribbon FET with IL gating and metal gating are shown in figure 4.19(a)-(b). The device is turned on in both cases but since there most likely is a different work function of the gating substance they turn OFF at different gate voltages.

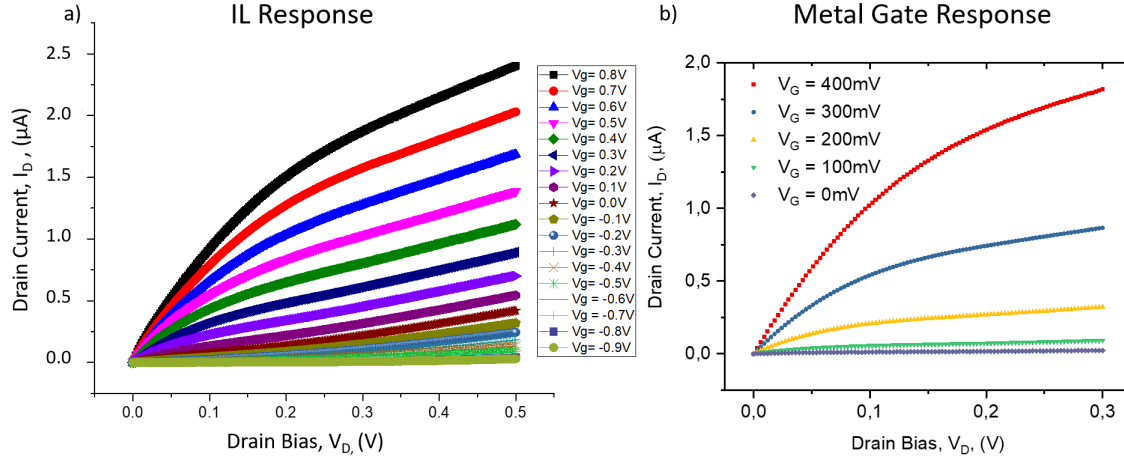


Figure 4.19 – Comparison of SOI Ribbon FET1 output characteristics for IL gating and metal gating

Next, we perform an analysis of the hysteresis in the SOI ribbon FET device. We also see the effect of varying gate voltage at different sweep rate. The exact sweep rate was not monitored in the experiment. The rate was changed by varying the gate voltage step for each measurement while keeping the duration of the pulse constant throughout and is illustrated in the graphic in figure 4.20.

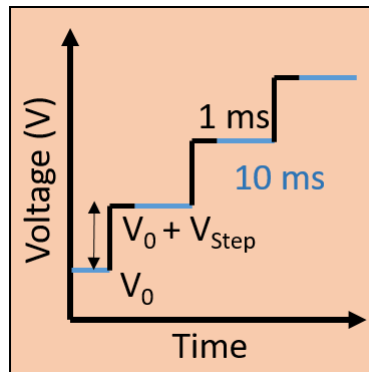


Figure 4.20 – Type of voltage signal applied to the gate in order to control sweep rate.

Changing the sweep rate enables us to find the optimum where hysteresis is at a minimum. In figure 4.21(a)-(d), the transfer characteristics response measured during a gate voltage cycle of $V_{ILG} = +1$ V to -1 V (forward sweep) and $V_{ILG} = -1$ V to $+1$ V (reverse sweep) at

4.3. Ionic liquid gating measurements

room temperature (300 K) for different sweep rates is shown. It is seen that for a slow sweep the hysteresis is low and about 200 mV and as the sweep speed is increased the hysteresis goes to reach 350 mV. As the sweep rate is increasingly difficult for the IL to follow the change in gate voltage and hysteretic loops become larger. A similar trend is published by Liebb *et al.* [36].

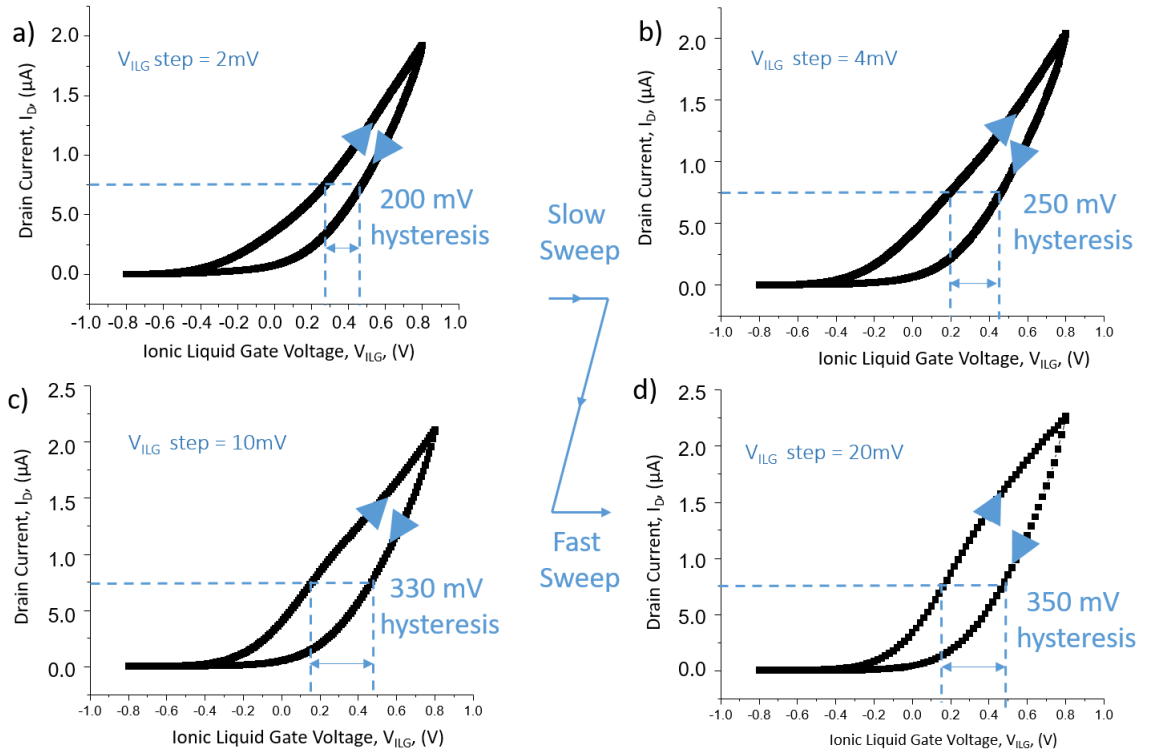


Figure 4.21 – SOI Ribbon FET 1 effect of changing sweep rate on hysteretic loops.

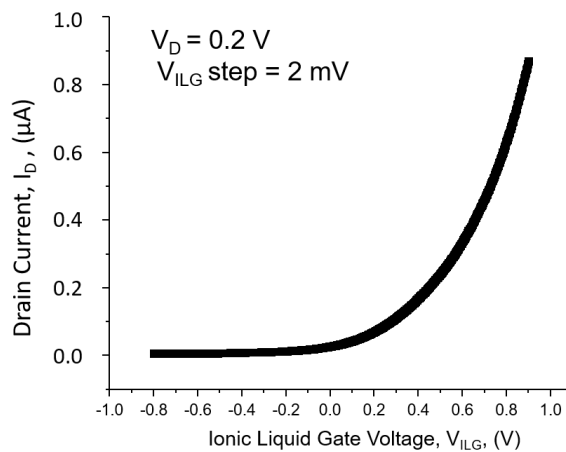


Figure 4.22 – SOI Ribbon FET 2 transfer curve response to IL gating

In figure 4.22 is another SOI ribbon FET whose transfer characteristics are shown to demonstrate that only a single measurement was not carried out. Again, in figure 4.23(a)-(b), a comparison of the IL gating to the pH response is shown. The ON and OFF ratios are similar but not exactly as in the previous comparison because this pH response curve is not for the same exact device but rather shown for a qualitative comparison. Also in figure 4.24 the output characteristics of a IL gated and metal gated device shown that the device operation goes from ON to complete turn OFF.

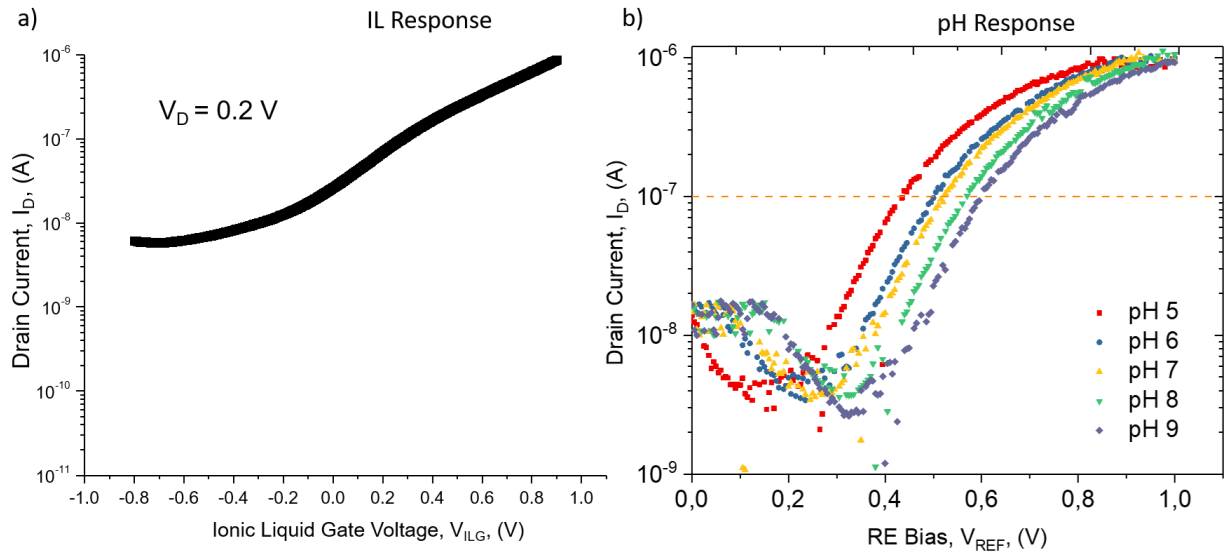


Figure 4.23 – SOI Ribbon FET 2 IL response versus pH Response

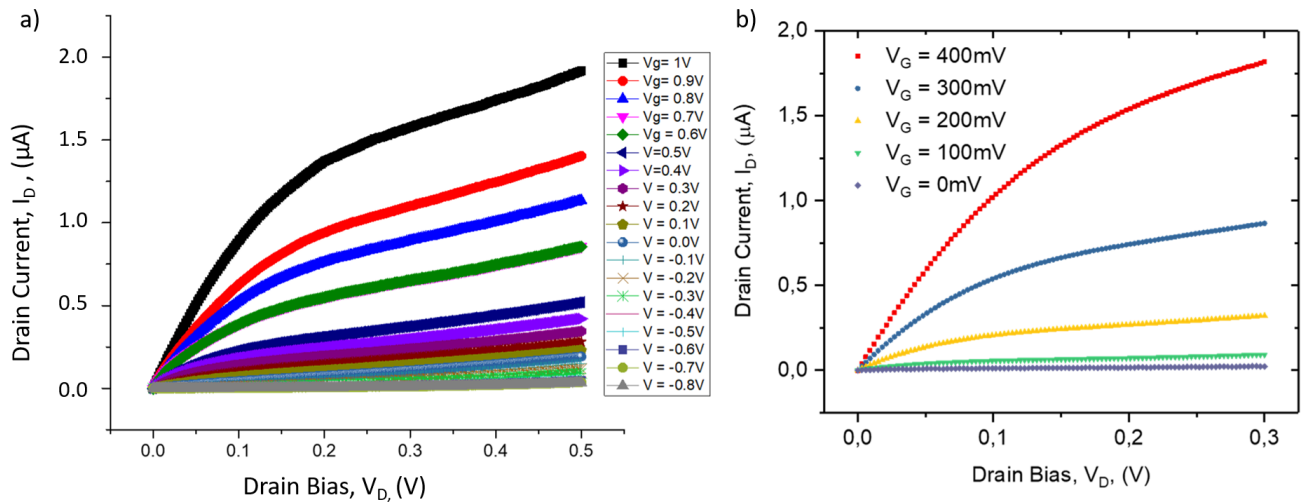


Figure 4.24 – Comparison of SOI Ribbon FET 2 output characteristics for IL gating and metal gating

4.3.2 IL Measurements on InAsOI FinFETs

The ionic liquid (IL) gating measurements were performed on different devices from the same chip used in section 4.1.2. The samples were cleaned with solvent and the high-k oxide surface was reactivated with an oxygen plasma step. The measurement was performed a couple of weeks after validation of pH sensing. This goes to show that the device performance was quite stable with time. In figure 4.25 (a) is the $I_D - V_{ILG}$ characteristic of an InAsOI FinFET device with a 70 nm wide fin at a drain voltage of 10 mV. The modulation of the ON current is only 30 % but a response to the potential of the liquid gating is indeed seen. Moreover, one can distinguish from the axis to the right on figure 4.25 in grey color the gate leakage current which is in the range of tens of nanoamperes.

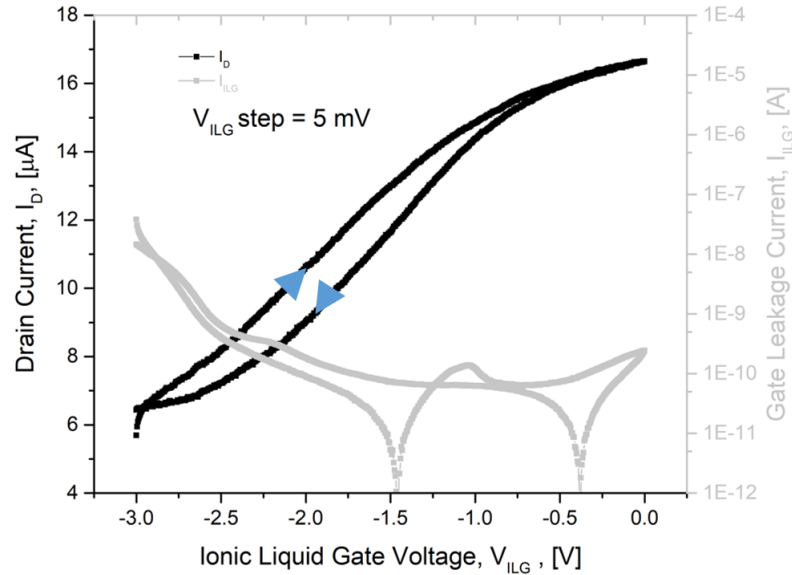


Figure 4.25 – InAsOI FinFET device response with IL gating drain current to the left axis and gate leakage current to the right of the axis.

In figure 4.26 the effect of hysteresis on sweep rate was investigated. The rate is varied as discussed before by changing the voltage step while keeping the duration of the pulse constant. First, a hysteresis of about 200 mV is seen. With the change in the sweep rate there is no noticeable change in the hysteresis window. A likely explanation is that device is narrowly depleted and sits in the saturation region of the transfer characteristic curve where the sweep rate does have no significant impact on hysteresis.

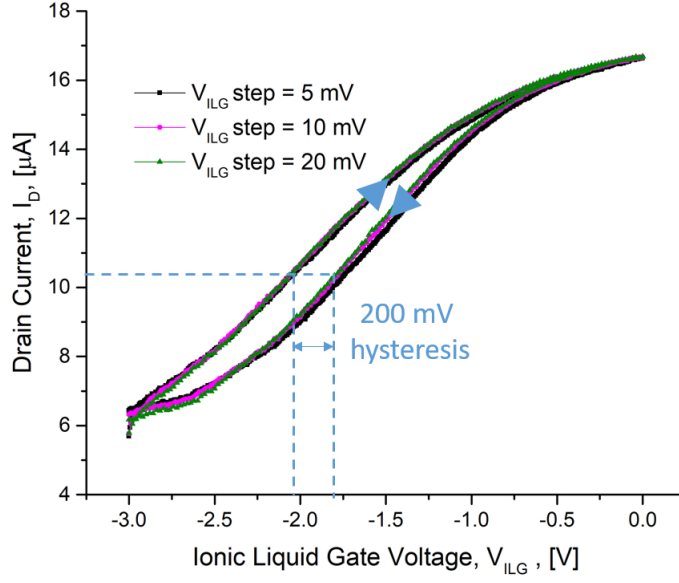


Figure 4.26 – Investigation of hysteresis effect in InAsOI FinFET by varying the sweep rate.

In all the figures the voltage step refers to the amplitude of value, V_{step} shown in figure 4.20. In figure 4.27(a)-(b) two devices D and E with the same geometry are compared at the same drain bias applied of 10 mV. In both the graphs to the left axis we have the drain current (in black) and to the right axis we have the gate leakage current (in blue). The gate leakage current is few nanoamperes in both devices and atleast three orders of magnitude lower than the device current. The modulation of ON current is extremely similar, in each case it is 50% and 53%, respectively. The hysteresis in devices D and E is also in the similar range for the device shown in figure 4.26.

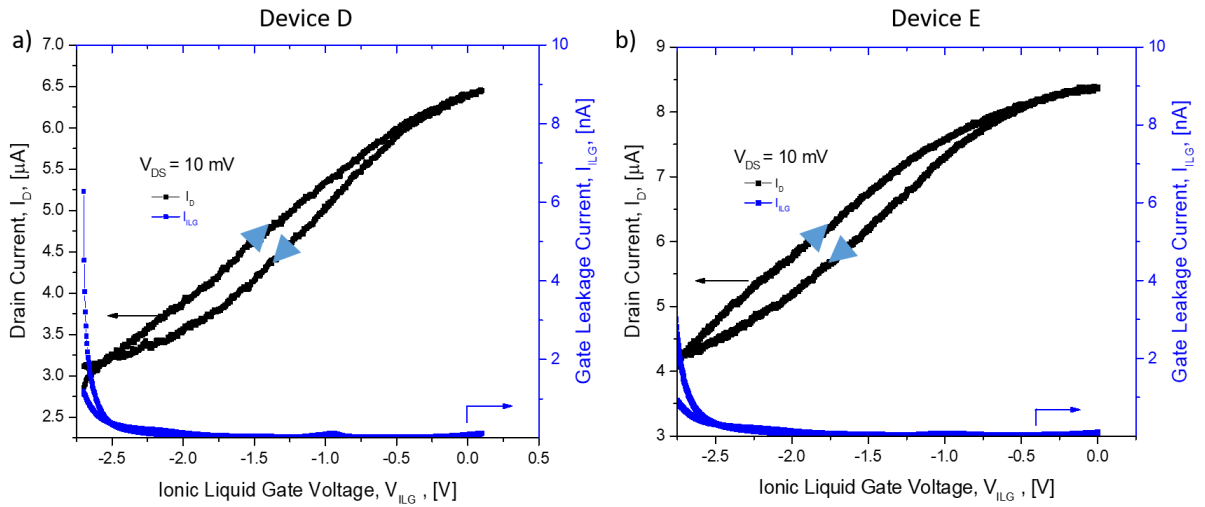


Figure 4.27 – InAsOI FinFET IL Reproducibility

Now, we put our device into perspective with others reported in literature. We compared our InAsOI FinFET to an InAs NW by Liebb *et al.* in figure 4.28(a)-(b). The InAs NW has a diameter of 70 nm and our device is a 70 nm wide InAsOI FinFET. The measurement of InAs NW is taken from the supplementary information of [36]. The curves are comparable in their qualitative behaviour. The modulation of the ON current level is about 30 %. Liebb *et al.* also attribute the partial modulation to a higher doping level per cross section that does not allow full depletion [36]. However, one can see that not only is our measurement less noisy but also the hysteresis measured is 100 mV and lower than their 250 mV.

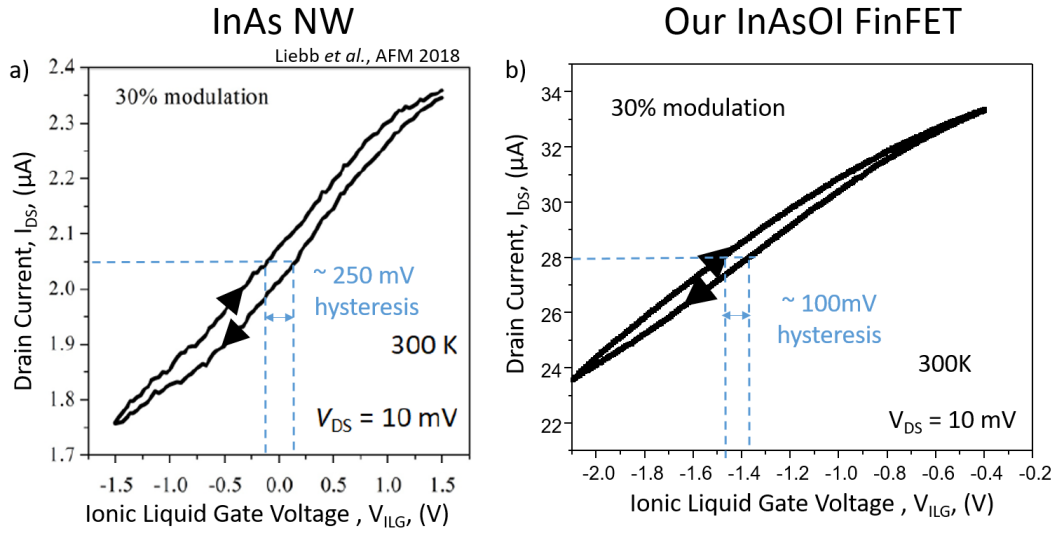


Figure 4.28 – InAsOI FinFET vs InAs NW IL gating transfer response

4.4 Metal Gate Patterning

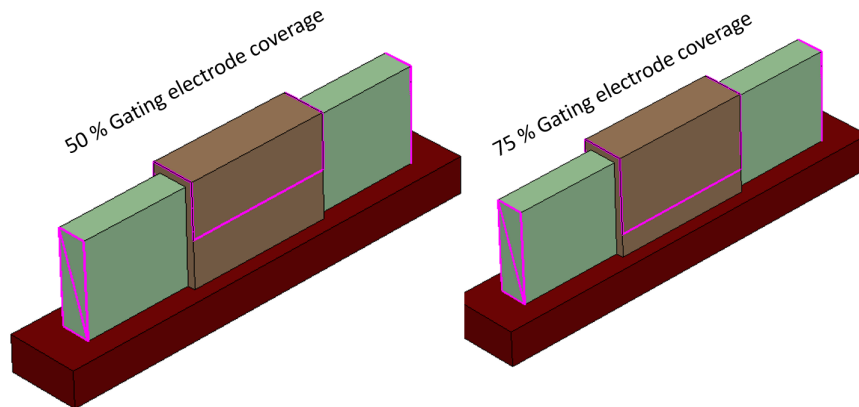


Figure 4.29 – Device schematic for simulation of partial gating electrode (left) 50 % gating and (right) 75 % gating.

Ways to improve the transfer characteristics of the device, deplete it and move towards turn OFF have been investigated. A reliable control of the channel cross section can be achieved if the gating is guaranteed on the entire height of the fin i.e continuous sidewall coverage. We performed some simulations with partial gating conditions to verify that this could be one of the reasons of incomplete modulation. All the parameters for the simulations here are the same as those given in section 2.6.5. Even for a fin width of 40 nm, one can see in the simulation of partial gating in figure 4.30 that OFF performance can degrade easily by 3 to 4 orders of magnitude going from the nanoamperes range to the microamperes range. Especially with multiple fins in parallel, masking the OFF currents of each other is not easy and even one leakage path can result in huge OFF current levels as could likely be in our case.

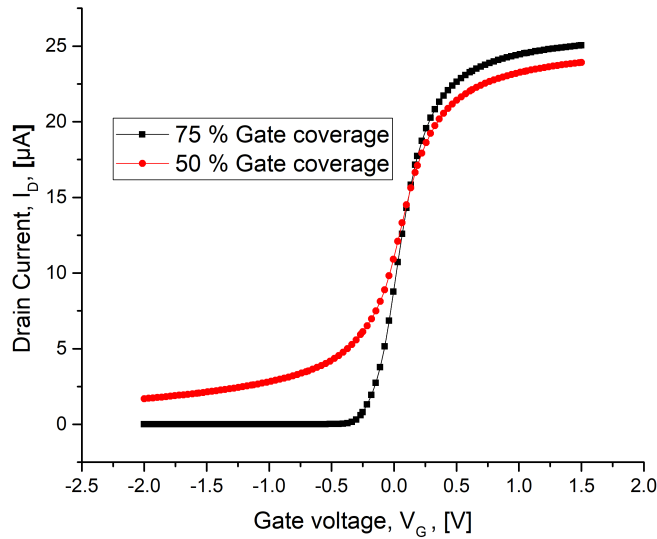


Figure 4.30 – Device simulation showing transfer characteristics of partial gating electrode (left) 50 % gating and (right) 75 % gating.

A process to build a metal gate on our devices InAsOI FinFETs in the current batch i.e without any new design modifications to the chips is described.

1. A first, simple direct EBL patterning with resist, then metal sputtering and lift-off step for metal gate patterning was attempted. Ebeam resist used is PMMA and sputtered metal was tungsten (W). The result was not very successful since the channel is extremely narrow of 100 nm. Shown in the 30 ° tilted SEM image of figure 4.31(a)-(b), a before and after gate patterning on the device. In figure 4.31(b) the metal film only present on the edges and is not continuous on the fin sidewall. This can also have to do with the very tight pitch of the fins in this design.

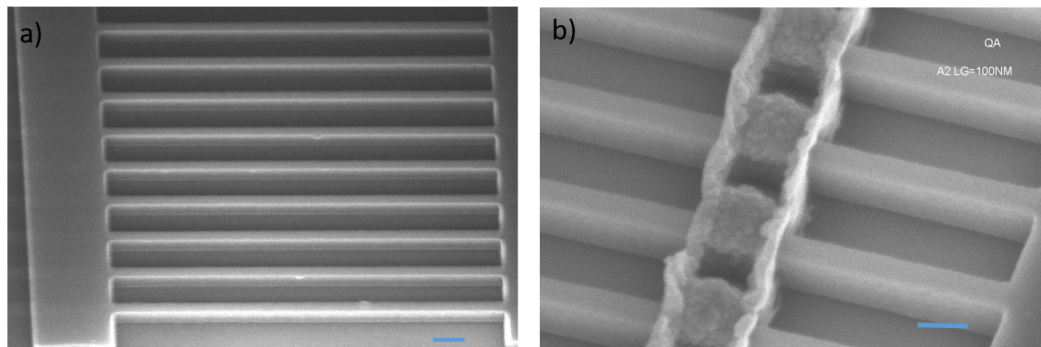


Figure 4.31 – Tilted (30 °) SEM image of a) device before patterning and b) after EBL patterning, tungsten sputtering without any tilt and lift-off of resist. Scale bar is 200 nm and 100 nm.

2. To solve the issue with fin coverage first we wished to use another approach of first sputtering and then etching the metal gate away in regions not wanted. For this we did a first test with manual tilted sputtering of the samples. Seen in figure 4.32 are the FIB cross section after one angle of tilted sputtering. One can distinguish perfectly that the metal film is continuous between the fin spacings and covers well the entire height of fin sidewalls. Next is to pattern these samples using an EBL mask and dry etch technique.

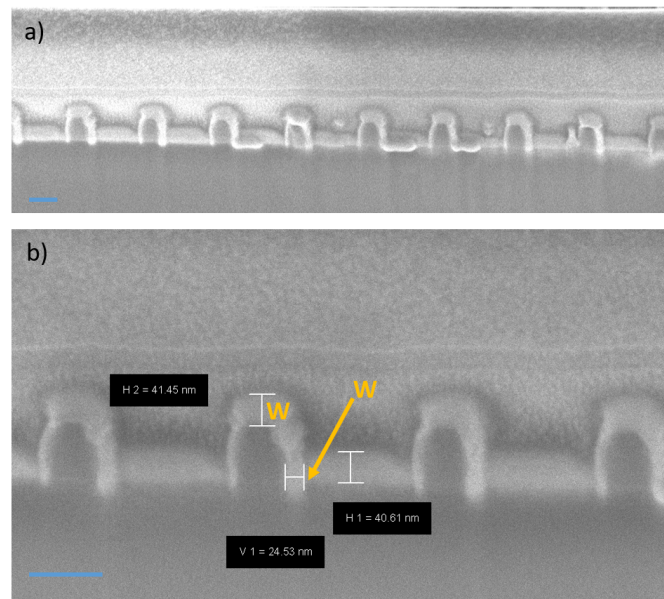


Figure 4.32 – Tilted (30 °) SEM image of a FIB cross section showing continuous metal film on a multiple fins with tilted sputtering of W but without an EBL step. Scale bar is 100 nm and 100 nm.

4.5 Summary

InAsOI FinFETs have been demonstrated as pH sensors [94]. The performance metrics for the first proof-of-concept devices are shown in the table 4.1. Moreover additional gating using ionic liquid has been proposed and tested on the devices and a comparison with better hysteresis than other InAs NW is measured. There is scope for further investigation- such as device-to-device variability before extracting more ISFET response curves. This is only possible in a next fabrication batch where small fin widths are targetted and the design pitch is relaxed for sensing.

		Parameter	Value
A first sensor characterization [Rupakula et al., ESSDERC 2019, Rupakula et al., IEEE J- EDS, 2020 (submitted)]	1	pH Sensitivity	41.2 mV/pH
	2	Linearity	Highly linear for 3 values of pH
	3	Hysteresis	~ 150 mV
	4	Ohmic Contacts	~ 700 Ω ; At $V_{DS} = 10$ mV, tens of μA of I_{DS}
	5	Current Modulation	up to 50% change in drain current

Table 4.1 – Summary of sensor response

5 Conclusions and Perspectives

5.1 Conclusions

The main technological achievements are first summarized in this section perspectives for the future are presented.

5.1.1 Scalable III-V Integration platform for sensing: TASE

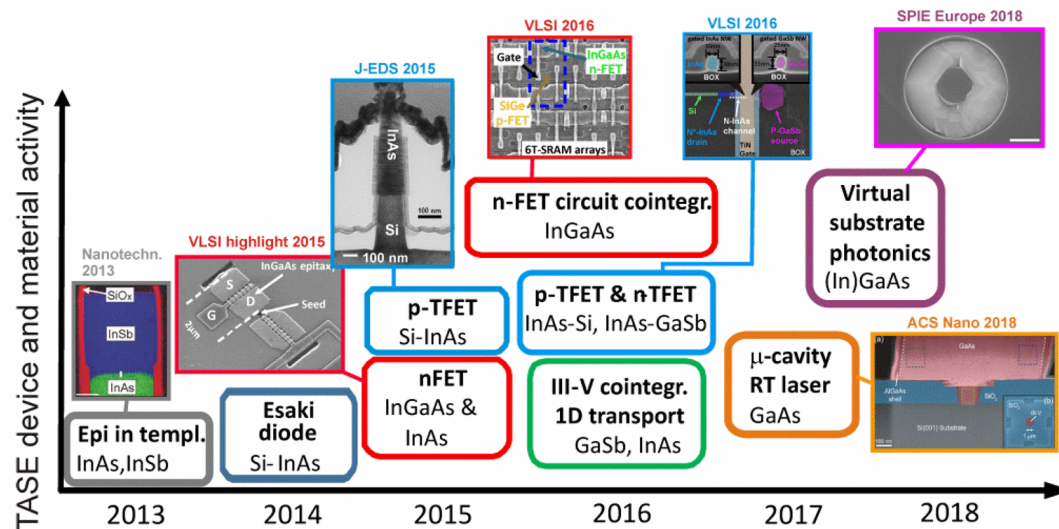


Figure 5.1 – TASE device and material activity over time taken from [95]

The prime advantage of the demonstrated InAsOI FinFETs can be attributed to III-V growth directly on silicon platform without a catalyst. This makes devices built on this InAsOI platform highly scalable. An essential feature of furthering the field of FET based sensing is the ability to carry out multiplex ion detection. TASE enables the definition of multiple fin arrays at precise locations down to few nanometers. The extremely high placement accuracy

provided by a top-down fabrication approach such as TASE is no match for the bottom-up assembly typical for NWs fabrication. Plenty of diverse device concepts and materials have been demonstrated with TASE as summarized in figure 5.1. Adding to this TASE activity is our demonstration of sensing [94]. Noticeably new electronic architecture such as tunneling FETs are demonstrated and also co-integration of p-type and n-type devices conforms to CMOS compatibility.

5.1.2 High Aspect Ratio Fin fabrication

A tall fin (fin height:fin width = $\sim 4:1$) of InAsOI(InAs on insulator) on a silicon substrate has been demonstrated. In comparison to other works in literature this geometry stands out especially for being on a silicon substrate as is compared in table 5.1 with data extracted by looking at references [93, 96, 97, 98, 99, 100, 101, 102, 103] respectively. Moreover, other TASE works devices with horizontal [83] and vertical [81] NW geometry have been shown. Establishing TASE as a very versatile technological platform. To the best of our knowledge it is the first time FinFET structures in InAsOI have been investigated for ion sensing.

Ref.	Sub.	III-V Type	Indium Mole Fraction	Fab. Technique: Etching or Growth	H _{fin} (nm)	W _{fin} (nm)	Aspect Ratio, H _{fin} : W _{fin}
Oxland et al.	InAs	InAs	1	Etching	20	25	4:5
Radosavljevic et al.	InAlAs	InGaAs	0.53	Etching	50	30	5:3
Kim et al.	InP	InGaAs	0.53	Etching	20	30	2:3
Thathachary et al.	InP	InGaAs	0.7	Etching	120	38	$\sim 3:1$
Zota et al.	InP	InGaAs	0.53	MOVPE	16	40	2:5
Vardi et al.	InP	InGaAs	0.53	Etching Digital Etch	170 170	25 8	$\sim 7:1$ $\sim 20:1$
Czornomaz et al.	Si	InGaAs	0.7	Epitaxy	25	50	1:2
Kim et al.	Si	InAs	1	Etching	9	40	$\sim 1:4$
This work Rupakula et al.	Si	InAs	1	MOCVD	130	30	$\sim 4:1$

Table 5.1 – III-V Fin geometry comparison.

5.1.3 Experimental characterization - pH sensing, Metal gate and Ionic Liquid gate

With its unique sensing geometry, ion sensing principle has been demonstrated for InAsOI devices with the sensitivity extracted at different current levels in the microampere range [94]. Despite full depletion of the fins not being achieved linear response to pH in the modulated range is observed. Moreover further methods to validate the partial depletion

using non-conventional gating such as FIB deposited Pt gate and Ionic liquid have been tested. Hysteresis curves are also reported for these measurements.

		Parameter	Value
Technology Development [Rupakula et al., SiNW2018]	1	Fin Aspect ratio (H_{Fin} : W_{Fin})	4:1
	2	Fin width (W_{Fin}) scaling	80 nm to 30 nm ; Demonstrated a scalable process
	3	Dense Integration	20 fins; where effective area > planar area
	4	Device placement	Up to 30 nm accuracy
	5	III-V Integration Scheme	Local integration, Catalyst-free, on Insulator process
	6	Substrate	Silicon Monolithic Integration
	7	CMOS Compatibility	Temperature, Materials, Process
A first sensor characterization [Rupakula et al., ESSDERC 2019, Rupakula et al., IEEE J-EDS, 2020 (submitted)]	8	pH Sensitivity	41.2 mV/pH
	9	Linearity	Highly linear for 3 values of pH
	10	Hysteresis	~ 150 mV
	11	Ohmic Contacts	~ 700 Ω ; At $V_{DS} = 10$ mV, tens of μA of I_{DS}
	12	Current Modulation	up to 50% change in drain current

Table 5.2 – Main conclusions of this work from technology side leading to sensor characterization.

5.2 Perspectives

The work can be improved on different fronts - design, fabrication, extension to especially biomolecule sensing to exploit nanoscale design and application to TFET sensors to push detection limits.

5.2.1 Design & Fabrication

Growth lengths

So far most works reported with TASE have shown devices to maximum growth lengths of 1.2 to 1.5 μm . While for computation this may not be an issue but for sensing larger sensing areas are desired. With multiple fins in parallel as arrays this could be addressed.

Fin width

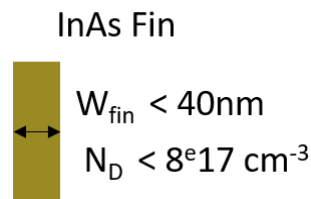


Figure 5.2 – InAs fin cross section

The presence of buried oxide below the Si device layer in the SOI substrate could place a limit on the minimum achievable fin width with our current HSQ resist processing. Perhaps in industry this issue does not arise as EBL is not a standard lithography technique but it is UV lithography. UV lithography employs organic resists and for removal of this organic resist HF based solution are not necessary and hence can keep intact the fin integrity. In the current state of the tool, with TASE process for non-intentionally doped InAs structures the doping could not be controlled below $4 \times 10^{17} \text{ cm}^{-3}$. With this limitation only the fin width has to be aggressively scaled to enable full depletion of films.

Multiple-fin array

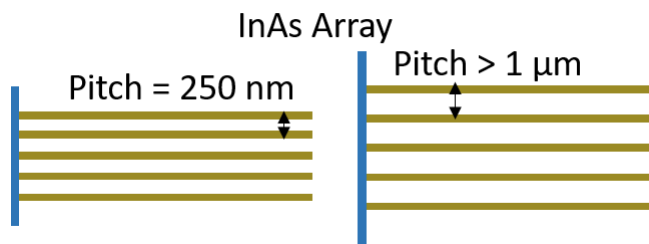


Figure 5.3 – InAs fin array design

The tight pitch of the multiple fin array needs to be relaxed in order to accomodate functionalization layer and the arrival of bigger bio-molecules. Ions are in the size range of angstroms and hence nanometer spacing is not a hindrance for their arrival and detection.

SU8 microfluidics and on-chip reference electrode

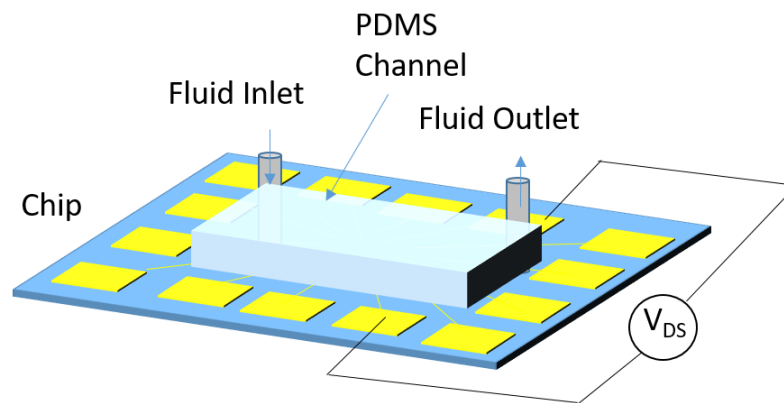


Figure 5.4 – InAs FinFET with on chip reference electrode and supporting microfluidics

To claim a truly miniaturized system, the reference electrode should be fabricated on-chip and its reliability, stability tested in line with works [12, 104, 105]. Studies for longer time frames in days are necessary to validate its proper functioning and this is why building a robust microfluidic system around the device is necessary for further measurements such as reponse times.

Fluidic flow

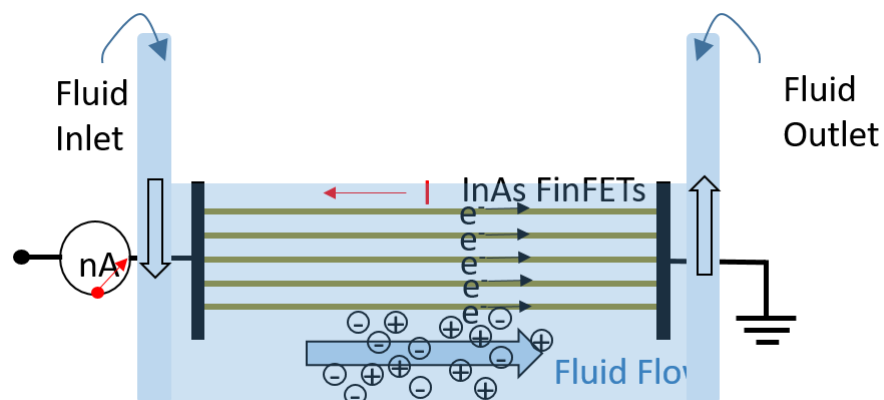


Figure 5.5 – InAs fin arrays usef for energy harvesting

Interesting experiments of exploring and harvesting fluidic flow energy can be carried out once a more robust microfluidic system is put in place.

Wafer Scale

In order to test different process conditions the wafer was cleaved into dies early in the process. However, end-to-end wafer scale process can and should be implemented to claim a scalable manufacturing process.

5.2.2 Case for biosensing

Theoretically, the technology module, InAsOI fin structure is compatible with biosensing. However, without design modification it is not feasible. The importance of nanostructures to improve limit of detection can be perceived for targets with ultra-low concentrations e.g protein molecules, DNA, viruses, cortisol, PSA, interleukin and streptavidin. The current tight pitch design needs to be relaxed. The device to device spacing is 250 nm but taking oxide into consideration the actual gap between two fins is less than 120 nm. This is not a hindrance to ions, but restricts large molecules from entering between fins. For ions of hydrogen, calcium, sodium, potassium and molecules of glucose, lactate, urea for most healthcare applications lower than μM is not relevant.

5.2.3 TFET as a sensitive bio-sensor

As discussed in section 5.2.2 that nanoscale phenomena of FET will be appreciable for target receptors when ultra-low concentrations of detection are under question. The current sensitivity of a sensor is best for the steepest region of transistor operation i.e. the sub-threshold region. FETs are limited in current sensitivity because their SS is restricted to 60 mV/dec because of Boltzmann statistics. However, tunneling FETs are not limited to $SS = 60 \text{ mV/dec}$ because of their non-thermal charge injection mechanism (quantum mechanical band-to-band tunneling). Though the voltage sensitivity of both TFET and FET can be similar, it is the current sensitivity that will be affected by the SS. It is known that TFETs are plagued by low ON currents due to their physical mechanism. The tall geometry in a direct bandgap material such as InAs becomes appreciable in this scenario.

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MANEESHA RUPAKULA



Microtechnical Engineer

- 5 plus years of hands-on experience in an ISO 5 cleanroom laboratory with expertise in nano fabrication
- Ability to work well on a team in fast-paced projects to meet demanding time-lines
- Displays good analytical, organizational, troubleshooting & presentation skills
- Can communicate in 6+ languages owing to multi-national study, work and living experiences

Nano
Healthcare
Sensors
Regulatory
Device
Process
Medical
IoT
Micro
Engineering
Development
Management
Assurance
Analysis
Business
Market
Quality

Education

- PhD** **École Polytechnique Fédérale de Lausanne (EPFL), Switzerland** 2015-Present
Doctor of philosophy (PhD) in Microengineering
• Relevant Coursework: Wearable sensing and computing, Highlights in microtechnology, Management of innovation and technology transfer, Creative problem solving
- MSc** **Politecnico di Torino, Italy** Sep 2011 - Mar 2015
Master of Science (MSc) in Electronic Engineering
Major in Micro nano integrated Systems | Mark: 92/110
• Relevant Coursework: Physics and technological processes of micro systems, Micro nano systems for biological and chemical applications, Physics modelling of micro nano systems, Electronic design automation tools, Basics quantum mechanics, Solid state physics
- BTech** **Jawaharlal Nehru Technological University, India** Sep 2007 - Jul 2011
Bachelor of technology (BTech) in Electronics and communication Engineering | Mark : 78/100
• Relevant Coursework: Applied physics, Mathematical methods, Electronic devices and circuits, VLSI design, Signal processing

Research & Development Experience

PhD Student & Research Development Engineer

NANOLAB, EPFL

- Lead end-to-end project development: conception, design, simulation, fabrication and characterization of III-V nanostructures for chemical, bio-sensing and electronic applications. Collaborated with IBM(Switzerland) under European project E2Switch.

Highlight: Results presented in two conferences; one for a talk and one for poster presentation.

- Co-process development of foundry fabricated Integrated circuit chips to incorporate into a wearable health care monitoring system. Potential Class II novel diagnostic medical device. Collaborated with a multidisciplinary team in a startup Xsensio SA. (Switzerland).

Highlight: Work as co-author resulted in three conference presentations and a journal publication.

- Co-assisted in lithography development for a first of its kind microprocessor based on Nanoelectromechanical (NEMS) systems. Worked closely with KTH(Sweden) and IBM(Switzerland) under European project NEMIAC.

Highlight: Processing and transfer of samples to collaborators within time frame to complete fabrication. Role acknowledged in collaborator's PhD Thesis Dissertation.

- Fabrication towards realization of Tunnel FET for dynamic memory applications

Highlight: Poster presentation at micro and nano engineering, 2014 conference

Master Thesis & Research Assistant

The Molecular Foundry, LBNL

- Design of experiments for etch process optimization towards nanofabrication of Silicon and Gallium Arsenide Photonic crystals to study interesting optical phenomena.
- Imprint nanolithography and characterization of opto-nano biosensors for a start-up funded by Department of Energy (USA).

113

Highlight: Hired as paid part-time employee for last 3 months of the internship period

Languages

English ●●●●●

French ●●●●●

German ●●●●●

Italian ●●●●●

Personal Interests

- **Biking** to work as a means to improve fitness & adopt an eco-friendly lifestyle
- Volunteer as a **compère** and organizer at familial, collegiate and regional events
- **Writing** about travel, language, culinary and cultural experiences in various social media channels and a blog.
- **Teaching** Indian Film (Bollywood) dance at different social gatherings
- **Learning** new languages to expand intellectually and integrate culturally
- **Hiking** in summer with groups of people to spend time closer to nature

Personal Info



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20 June 1991



Swiss B Permit;
Indian Nationality



Scan for LinkedIn profile

Awards & Recognition

- **Third position** for best poster award in microengineering doctoral school research day 2019 at EPFL.
- Italian **Government Scholarship** for Master in Science & Technology for academic year 2011 to 2012. Granted a monthly stipend to cover living expenses for one study year.
- **First runner-up** at Techstars Startupweekend, Lausanne in February 2019 for presenting a platform-scale startup pitch. Offered 3 months coaching from GENILEM Vaud.
- **First position** at local school in Hyderabad, India in All India Senior School Certificate Examination, 2007.

Technical Skills

Fabrication Techniques | Photo & e-beam lithography | Physical & chemical vapour deposition | Wet & dry etching | Inkjet printing | Microfluidics |

Characterization Tools | Scanning electron microscopy | Atomic force microscopy | Profilometry | Focussed ion beam patterning | Electrical probe station | White light interferometry |

Data Skills

Software | Origin | Matlab | Microsoft office |

Programming | Latex | MATLAB | C |

Design Skills

Software | Sentaurus synopsys | COMSOL | Beamer | Adobe illustrator | Layout-editor |

Trainings and Workshops

- Medical technology and evaluation by University of Minnesota, Coursera Online course (ongoing)
- Internet of Things: How did we get here? by University of California, San Diego, Coursera Online course (ongoing)
- Lean Techniques in a fabless workflow workshop by Prof. Wim Bogaerts from Ghent University
- Workshop on social styles by Accenture at EPFL
- Sustainability conference by One World and Buhler

Publications

- M. Rupakula et al., "Monolithically integrated catalyst-free High Aspect Ratio InAs-On-Insulator (InAsOI) FinFETs for pH sensing," European Solid-State Device Research Conference (ESSDERC 2019), pp. 106-109.
- M. Rupakula et al., "High Aspect Ratio InAs-on-Insulator fins in Silicon Substrate Towards Logic Applications", SiNW 2018 - Silicon Nanoelectronics Workshop.
- J. Zhang, M. Rupakula et al., "Sweat Biomarker Sensor Incorporating Picowatt, Three-Dimensional Extended Metal Gate Ion Sensitive Field Effect Transistors", ACS Sensors 2019 4 (8), 2039-2047.
- J. Zhang, M. Rupakula et al., "All CMOS Integrated 3D-Extended Metal Gate ISFETs for pH and Multi-Ion (Na^+ , K^+ , Ca^{2+}) sensing." 2018 IEEE International Electron Devices Meeting (IEDM).

Complete list available on Google Scholar here.