PCIM Europe Digital Days 2020

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Abstract

DC power distribution systems in marine applications are in the process of being established as the preferred solution for shipboard power distribution systems. This paper presents a bus-tie switch topology for the protection of such systems. The device is based on a four quadrant switch with single active semiconductor and is designed to be modular and scalable, so it can be adapted to different interruption current and bus voltage levels. The developed prototype has been experimentally validated for its thermal behaviour in continuous conduction and switching performances, as well as in standalone operation with digital controller added to the power stage. The simplicity of the device topology offers interesting prospects for DC power distribution systems.

1 Introduction

Shipboard LVDC PDNs have been shown to provide increased efficiency and flexibility of operation when compared to their AC counterparts [1]–[5]. This is mainly due to the decoupling of the mechanical rotational speed of the generators through rectification of their electrical outputs, but also due to the absence of reactive power and elimination of large and heavy components such as line frequency transformers and integration of energy storage. Nevertheless, the protection of such systems remains challenging, and approaches based on a combination of fuses, solid state switches and generator de-excitation have been proposed as a means to protect the system in the event of a short circuit fault. As a part of the PDN protection, solid state bus tie switches (SSBTSs) are expected to provide the first line of defence by separating interconnected sectors of the PDN in the event of a fault, and do so as fast as possible [6], [7]. Due to the high capacitance and low inductance present in LVDC PDNs, the evolution of the fault current is significantly faster than in AC systems of equivalent working voltage. Interruption of the fault current needs to be performed in the range of tens to hundreds of µs, forcing bus-tie switches to be semiconductor based devices. SSBTSs do not have the same role as main circuit breakers and therefore are not intended to interrupt very high current levels that can occur in the system. Their operation must be prompt enough to prevent the fault current from reaching values outside the safe operating area (SOA) of the employed devices. To this date, several topologies of SSBTSs have been proposed, based on different operating principles [8], [9]. These can be

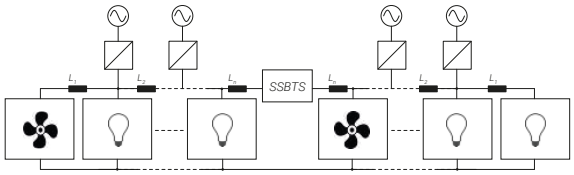

Fig. 1: Presented topology as part of a shipboard power distribution network (PDN), connected between the positive terminals of the DC bus.

ISBN 978-3-8007-5245-4

broadly categorized into four main groups:

- Interrupting topologies are such that the fault current is interrupted at the moment of the device opening [10]–[13].
- Limiting topologies have the ability for the fault current to freewheel upon interruption, reducing the switching stress on the device [14], [15].
- Resistive topologies store the energy stored in the system inductance in a capacitor that is then discharged into a specially allocated resistor [16].
- Resonant topologies artificially create a current zero by means of a capacitive discharge to allow the interruption of a fault current even by means of devices such as thyristors [17]–[19].

In these groups are also found commercially available systems from ABB [20] and SIEMENS developed up to the 1 kV voltage level with a power rating reaching several MW. This paper presents a novel SSBTS topology based on a well known 4Q switch, further extended to meet the challenges of limitation of current rise rate and interruption of a fault current in its early phase. The presented topology only requires a single active semiconductor switch and operates while only being connected to one terminal of the DC bus. It also achieves freewheeling of the current in L_{didt} internally to the SSBTS itself, as seen in Fig. 2d. Furthermore, thanks to its self contained current freewheeling and clamped terminal voltage, the topology can achieve increased power rating through series and parallel connection of several units. Finally, the determination of the presence of a fault condition is simple in this topology, and can be performed by observing the current in L_{didt} or the voltage at its terminals. This also allows for standalone operation of the device, which is presented and experimentally demonstrated in this paper.

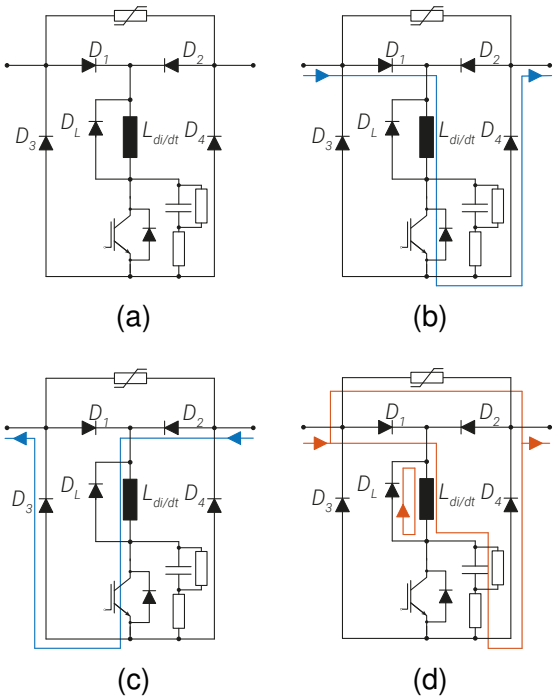

Fig. 2: (a) 4Q switch based SSBTS topology; (b) Current forward path in the SSBTS; (c) Current reverse path in the SSBTS; (d) Current path during breaking through snubber and MOV.

2 SSBTS Topology

Fig. 2a shows the proposed SSBTS topology with all the relevant elements needed for correct operation. To convert the 4Q switch into an SSBTS able to safely and repeatedly interrupt its rated current, the following components are added: (i) A current rate limiting inductor L_{didt} together with its antiparallel diode D_L, to prevent an uncontrolled rise of the current in the DC bus in the event of a fault; (ii) An metal oxide varistor (MOV) at the terminals of the device to limit the voltage on the SSBTS to a specified upper limit; (iii) An RC snubber in parallel with the IGBT switching device to accommodate for the presence of stray inductance internal to the SSBTS' mechanical design.
Forward, reverse and interruption current paths are shown in Figs. 2b, 2c and 2d respectively. Compared to existing SSBTS topologies, the topology in Fig. 2a adds one semiconductor in the current path (2 diodes, 1

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IGBT), therefore slightly increasing conduction losses of the device. Nevertheless, the self-contained nature of the topology provides significant advantages with respect to other solutions. First, to operate, the topology only needs to be connected between the positive terminals of the bus connecting the sectors of the PDN it interfaces, as shown in Fig. 1. This decreases complexity and cost of the device installation.
Additionally, together with the clamping of the terminal voltage provided by the MOV, this allows for simple series connection of the device while still allowing for L_{didt} current freewheeling. This is not the case for topologies that perform this frewheeling through access to the negative bus bar [14]. Also, the unidirectionality in the current in L_{didt} allows for quick transitions of the current direction from one DC side to another, and *vice versa*, as the current rate limiting inductor will not oppose a change in current direction, thanks to its ability to freewheel through D_L. Finally, the use of a single active device reduces the number of gate driver units and control interfaces required in the system, increasing its reliability.

3 Small Scale Prototype

To evaluate the ability of the presented topology to effectively perform all the tasks of the SSBTS as presented in the previous section, a prototype is designed and built.

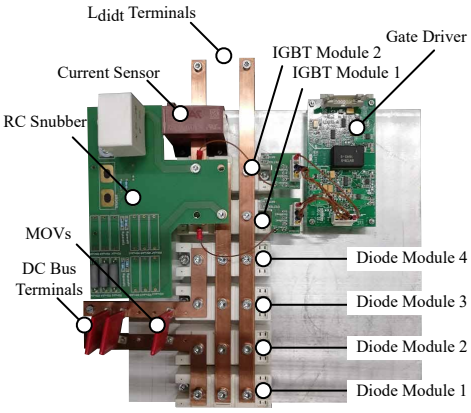


Fig. 3: SSBTS prototype without connected L_{didt} inductor and voltage sensor.

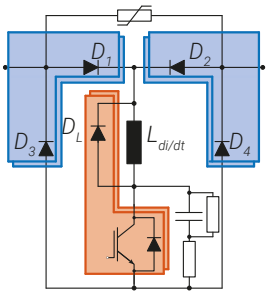


Fig. 4: Paralleling of semiconductor modules. D_1 and D_3 are physically in the same diode module, of which there are two connected in parallel. The same is true for D_2 and D_4, and for D_L and the IGBT switch.

This prototype, shown in Fig. 3, is designed based on scaled down ratings compared to those of an actual shipboard PDN. The prototype is defined by three levels of current: (i) I_{nom}, the steady state thermal current for which the device is sized, meant to be conducted indefinitely; (ii) I_{trip}, the tripping current of the device. Once this value is exceeded, it is assumed that a fault condition is present and the device is switched *OFF*; (iii) I_{max}, the maximum interruption current of the device while having the active semiconductors operate inside their SOA. The chosen values for these currents are displayed in Tab. 1.

Tab. 1: Prototype current and voltage ratings.

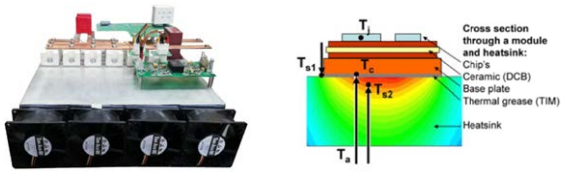
I_{nom}	$\leq$ 100 A	I_{trip}	100 A
I_{max}	200 A	V_{DC}	500 V

As current ratings in the range of several kA of shipboard PDNs often exceed the capabilities of the largest commercially available semiconductor modules, multiple modules have to be paralleled to achieve the required current capacity. In this prototype, modules have also been paralleled in each position. This is unnecessary considering the current rating of the prototype, but judged to be interesting by the authors as it allows some insight into the current sharing behaviour that is expected to be necessary at the MW level at which shipboard PDNs operate. The paralleling is performed so that no two devices contained in the same modules conduct at the

ISBN 978-3-8007-5245-4

Tab. 2: Ratings of semiconductor modules used in the prototype. *SKKD150F12* diode modules, and *SKM150GAL12T4* IGBT modules.

IGBTs	V_{CES}, 1200 V	I_C @ T_C = 80 °C, 179 A
Diodes	V_{RRM}, 1200 V	I_{FAV} @ T_C = 85 °C, 119 A



(a) (b)

Fig. 5: (a) SSBTS with fans providing forced air cooling; (b): Location of thermocouple for case temperature (T_c) measurement [21].

same time. This is shown in Fig. 4. The selected semiconductors ratings are shown in Tab. 2. The selected MOVs at the DC bus terminals of the device are *Littelfuse V421HG34*, chosen based on their clamping voltage, energy rating and an estimation of the stray inductance of the DC bus to be up to 1 $\frac{\mu H}{m}$, and a length of 10 m. The RC snubber in parallel with the IGBT position uses a 1 µF capacitor and 2.2 Ω resistor and is intended to absorb the energy in the stray inductance internal to the SSBTS (the actual design is omitted from the paper, due to limited space). The discharge resistor in parallel with the capacitor is of high value and does not influence the performance of the snubber during breaking. The current rate limiting inductor is not inherently a part of the prototype and is discussed in Section 4 together with switching tests.

The prototype also includes on board current and voltage (not in the figure) sensors to measure the current in L_{didt} and the voltage at its terminals.

4 Conduction and Breaking Tests

Before any form of control is integrated into the device, it was necessary to evaluate the

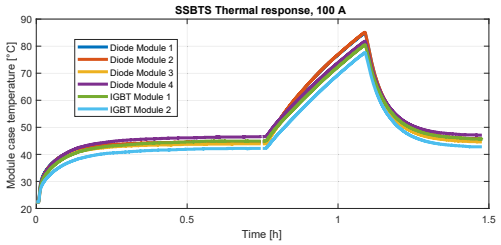


Fig. 6: Module case temperature with 100 A current in the SSBTS and varying forced air cooling.

hardware performance in terms of the device's ability to conduct its nominal current and interrupt fault currents. To do this, two tests are devised. The first test is a conduction test, in which the thermal performance of the SSBTS is evaluated. The device is connected to a low voltage high current DC source and a constant current of $I_{nom} = 100\,\mathrm{A}$ is circulated through the device. During this test, no current rate limiting inductor is connected to the SSBTS, as the main purpose of this test is to evaluate the temperature sharing between parallel connected semiconductor devices. Thermocouples are inserted in channels in the heatsink reaching under each of the modules of the SSBTS and sensing the case temperature of each module. Cooling fans are added to the heatsink as shown in Fig. 5a to allow a degree of freedom in controlling the heatsink to ambient thermal resistance. Fig. 6 displays the results of this test. Initially, the cooling fans are operated until a thermal steady state is reached around the 45 minute mark. At this point, the temperature

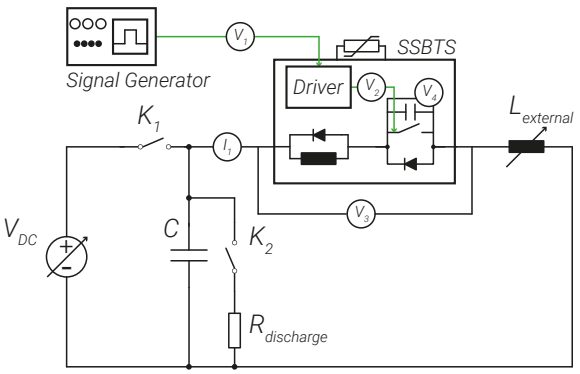


Fig. 7: Setup for externally controlled switching test.

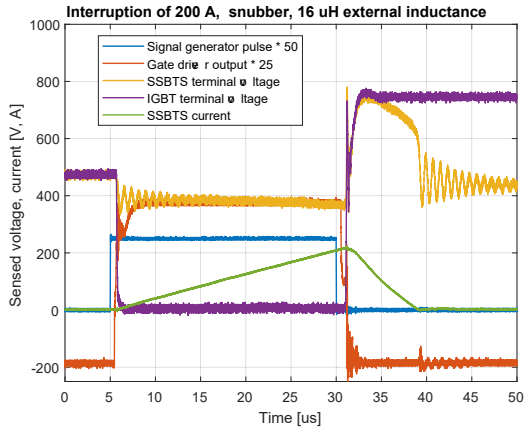


Fig. 8: SSBTS switching 200 A. Starting at $t_{fault} = 5\,\mu s$ the current rises at a rate of $\approx 8\,\frac{A}{\mu s}$ until it is interrupted at $t = 30\,\mu s$. The current is then shunted into the MOV and driven to zero in less than $10\,\mu s$.

of the modules is well shared and kept within the range of 5 °C, with modules located near the center of the heatsink displaying higher temperatures. After the steady state is reached, cooling fans are turned off, and the case temperature is allowed to increase up to 85 °C, at which time the fans are once again turned on. The test shows that the forced air cooling is able to bring the case temperature of the modules back to the initial steady state of approximately 45 °C.

The second test is the interruption of a fault current. To perform this test, a di/dt limiting inductor is connected to the SSBTS. The test setup is shown in Fig. 7 and operates as follows: (i) a DC voltage source is used to charge a 230 µF capacitor up to 500 V; (ii) the SSBTS is connected between the capacitor and an external inductor $L_{external}$ that simulates DC bus bar stray inductance; (iii) a signal generator is connected to the SSBTS gate driver to turn the device *ON* and *OFF*. Once the SSBTS is turned *ON*, the capacitor and the sum of the di/dt limiting inductor and $L_{external}$ resonate and result in an almost linear current increase in the device. The L_{didt} in the SSBTS is chosen so as to limit the rate of increase of the current to 10 $\frac{A}{\mu s}$. As the voltage on the capacitor is of 500 V, an available inductor of the value of 48 µH provides a close enough rate of current increase. For

Fig. 9: *PLEXIM RT Box* with SSBTS interface board. The board provides the *RT Box* with fibre optical interface to the SSBTS gate driver, and electrical interface to the sensors. Additionally, analogue and digital I/Os are available for the controller to be externally accessed.

the purpose of this computation, the external inductor $L_{external} = 16\,\mu H$ is neglected. As the inductance present in the test setup and the DC voltage are constant, different *ON* times provided by the signal generator will result in different final values of current in the device according to 1):

$$I_{OFF} = \frac{V_{DC}}{L_{didt} + L_{external}} t_{on} \qquad (1)$$

Fig. 8 provides results for the switching of 200 A. An *ON* pulse of 25 µs, that with a 500 V DC capacitor and a total of 64 µH of inductance is expected to result in a current rise of almost 200 A. In the figure, the 200 A threshold is ultimately exceeded. This is due to the charging of the snubber capacitor that results in the current not being immediately shunted into the MOV as soon as the device is opened.

5 Autonomous Operation

In Section 4 it has been determined that the SSBTS can conduct up to 100 A in steady state, and interrupt 200 A. For the device to have the functionality required of an SSBTS, it should be able to recognise the presence of a fault and turn off autonomously. For this purpose, a controller is added to the device in the form of a *PLEXIM RT Box*. Even though it is normally used for Hardware-in-the-Loop simulation, it is used for Rapid Control

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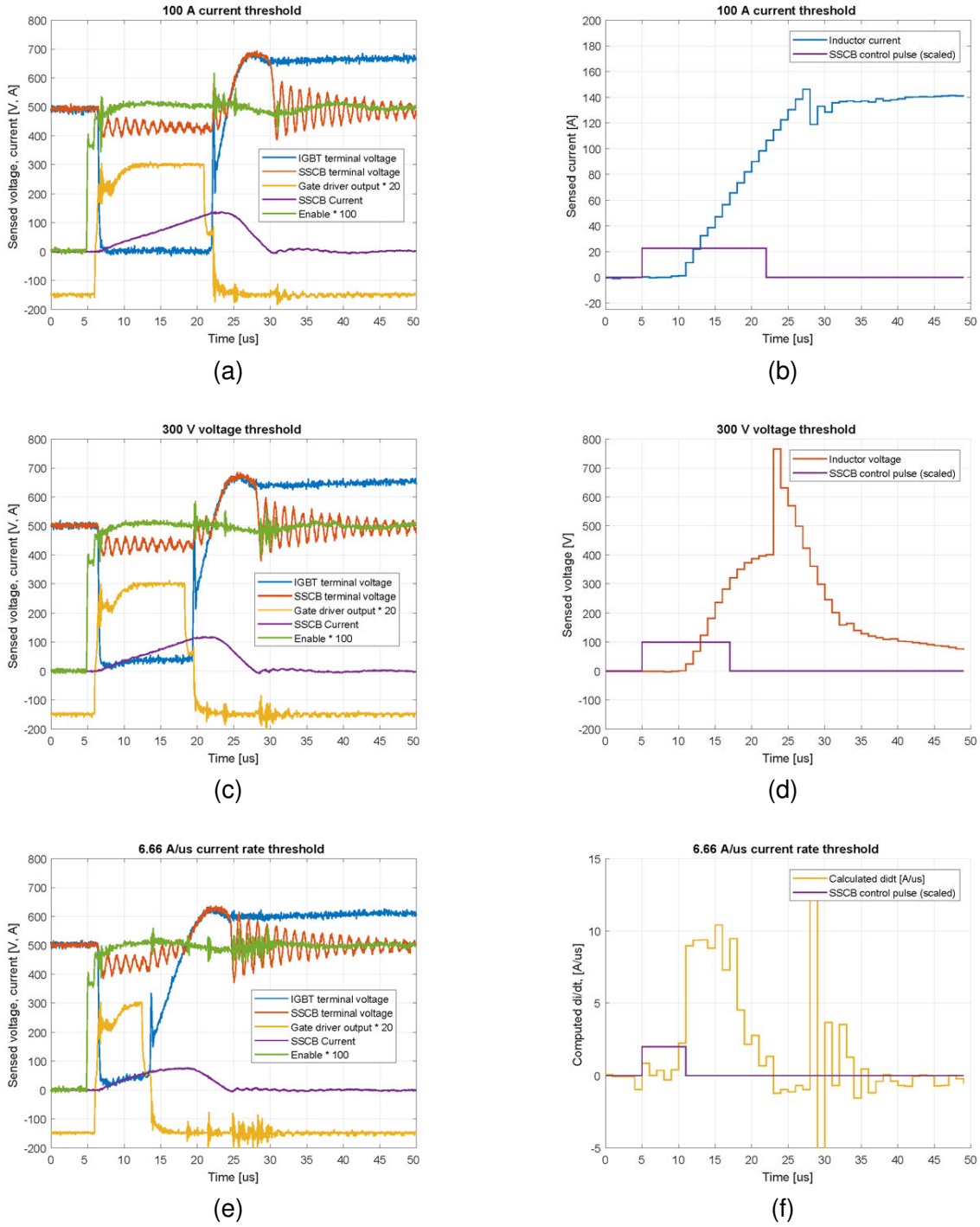

Fig. 10: The autonomous operation of the SSBTS allows the observation of the switching as measured by the external oscilloscope, and the internal reading of the controller according to the different tripping criteria. (a),(c),(e) show the interruption based on L_{didt} current threshold, L_{didt} voltage threshold and L_{didt} current increase rate threshold, respectively; (b),(d),(f) show the corresponding sensed and computed quantities in the RT Box operating at 1 MHz. Due to the current having to reach I_{trip} before interruption is initiated, (a) results in the longest reaction time and highest final current in the SSBTS. (b) provides faster interruption as the voltage on L_{didt} terminal is free to instantly increase to its final value at the time of the fault, while (c) provides fastest interruption through a combination of the fast reaction and rise time of the current sensor, and $\frac{di}{dt}$ computation that results in the threshold being reached almost immediately after the fault takes place.

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Prototyping in this case. The controller is provided access to the current and voltage measurement by the sensors, through a purpose built interface board. The board also provides fiber optical emitters and receivers to interface the SSBTS gate driver, and analogue outputs to read values from the controller. The controller and interface board are displayed in Fig. 9.
The controller samples the L_{didt} current and voltage sensor outputs at a time interval of 1 µs (1 MHz). A fault condition can be identified in three possible ways:

- By measuring the current magnitude and comparing it with the predefined trip level I_{trip}.
- By calculating the current rate of increase $\frac{dI}{dt} = \frac{I(k)-I(k-1)}{T_{sempling}}$, and comparing it against the predefined threshold.
- By measuring the voltage at the terminals of L_{didt}. This provides similar information to the current rate of increase, as $\frac{dI}{dt} = \frac{V_{DC}}{L_{didt}+L_{external}}$.

Of course, sampling and comparison of the measured value against a threshold result in additional delay in the response of the controller. The total delay is the sum of multiple delays: $d_{total} = d_{sensor} + d_{controller} + d_{actuator}$. Depending on the switching criterion used, the sensor and controller delay will vary. Tests are performed with all three switching criteria and their results are presented in Fig. 10a to 10f. Here, the SSBTS is turned on at $t = 5\,\mu s$ and turns off autonomously once the controller detects a fault condition. It can be clearly seen that different fault identification criteria result in different *ON* times of the device.

Current magnitude threshold
The current magnitude threshold based fault detection results in the longest fault interruption time. This is due to the current in L_{didt} having to reach the value of 100 A before the turn-*OFF* process is initiated. Therefore, there are approximately 10 µs in which the fault condition is present, but the controller is not yet reacting;

Voltage threshold
The voltage threshold results in faster interruption than the current magnitude threshold. This is because as soon as the SSBTS is closed, a large portion of the DC bus voltage appears on the L_{didt} terminals. Nevertheless, as the response and rise time of the voltage sensor employed are larger than those of the current sensor, the current still increases up to the value of $\approx 115\,\mathrm{A}$ before it is interrupted;

Current rate threshold
The current rate threshold results in the fastest interruption, with the device current only reaching a value of $\approx 75\,\mathrm{A}$, in the experiments. This is due to a combination of the fast response and rise time of the employed current sensor, and the fact that the current rise happens with relatively constant rate over the duration of the fault.
Based on the results displayed in Fig. 10, one can also observe that all values measured by the sensors connected to the *RT Box* suffer a significant spike and subsequent transient at the time of the SSBTS turning *OFF*. During the assembly of the prototype, no effort was made to minimise the effect of EMI on the sensing devices.

6 SSBTS Scalability

As discussed in Section 2, the self contained freewheeling and the clamped terminal voltage of the device are well suited for parallel and series connected operation of the proposed SSBTS topology. Both options are shown in Figs. 11a and 11b. For a given system voltage and increased power ratings, larger currents would have to be conducted and interrupted, and this is easily achieved through device paralleling. The same is true for a given system current and increased voltage rating, through series connection of the devices. In either of these configurations, the voltage and current stress on the individual devices is not increased, and each SSBTS operates in the same way as a single device in a DC bus of appropriate ratings. A combination of parallel and series connection is also possible,

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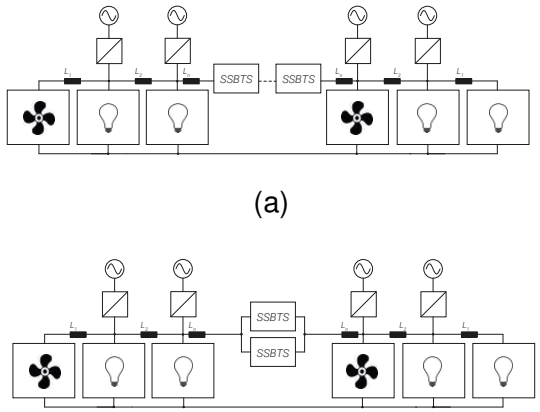

(a)

(b)

Fig. 11: (a) Series connected SSBTS units for increased voltage capability; (b) Parallel connection for increased current capability.

if required.
From the point of view of control, the threshold based nature of the fault identification, whether current magnitude, rise rate, voltage or a combination of the three is used, lends itself to simple scaling with the use of several SSBTS units. In this case, it is recommended that the tripping of a single unit, whatever the tripping criterion, correspond to the tripping of the whole SSBTS array, in order to avoid different units being stressed in a non-uniform way. Results pertaining the operation of multiple units are not presented in this paper and are the subject of future work.
Ultimately, the autonomous switching of the device has proved to be effective in limiting the SSBTS current below $I_{max} = 200\,\mathrm{A}$, no matter the criterion used to identify the presence of the fault. The voltage stress on the devices is also maintained well below the semiconductors' ratings showing that the proposed topology is a suitable alternative to existing solutions with the advantages listed in Section 2.

7 Conclusion

This paper has proposed and demonstrated the operating principles of an SSBTS topology for shipboard DC PDNs. A prototype has been developed and tested during conduction and current interruption, including standalone operation with an integrated controller. The controller can employ different fault identification methods, based on current magnitude, rate of increase, or terminal voltage. The reliability of the topology is increased thanks to its connection simplicity and single active semiconductor device, making it a valid option for DC applications.

8 Acknowledgements

The work presented in the paper is sponsored in part by Hyundai Electric & Energy Systems and in part by the European Research Council (ERC) under the European Union's Horizon 2020 research and innovation programme (Grant agreement No. 818706).

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