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Thermal Study of a Modular Multilevel Converter Submodule

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Abstract

Modular multilevel converters are gaining attention since medium voltage direct current grids have been proposed as the new key technology for the future transmission and distribution systems. The design of such systems need to address several challenges and this paper presents a thermal study of a modular multilevel converter full-bridge IGBT based submodule. Thorough tests have been performed under severe ambient thermal conditions and electrical stresses, typical to regular modular multilevel converter operation. Presented results demonstrate an excellent match between theoretically predicted numbers and those obtained in a custom-designed experimental test setup.

1 Introduction

Since modular multilevel converter (MMC) concept was first introduced in 2001 [1] a wide range of applications, topologies, and control schemes have been proposed and studied like MV-motor drives, STATCOM & UPQC and power transmission systems (HVDC systems, multi-terminal HVDC systems, and offshore wind farm systems) [2], [3]. In particular, the MMC used as a rectifier or inverter is interesting solution since medium voltage direct current (MVDC) grids have been reconsidered for future transmission and distribution systems. The MMC presents modular design, voltage and current scalability, high efficiency, high waveform quality, high availability, dc short-circuit fault ride-through capability among other advantages [4]. The submodule (SM) is the fundamental building block component in any MMC and must be designed carefully to achieve high reliability. Special attention must be paid during the sizing process of power devices and its cooling system design since over-temperature and thermal cycling are the major stressors that induce failure [5], [6]. Nevertheless, it is only possible through experimental tests to assess whether the power devices operate within its thermal limits. Along with the reviewed literature, the thermal problem is tackled mostly employing different mathematical modeling and simulations and less attention has been paid to experimental assessment. One of the reasons for this is the fact that the majority of reported MMC prototypes are academic scaled-down versions, that are oversized and not optimized, while industrial designs are normally not reported and detailed. For instance, the authors in [7] and [8] utilise a classical approach to calculate the SM's semiconductor power losses. However, in [7], the thermal model is based on the Cauer representation while in [8] the thermal analysis is carried out using finite element method (FEM). Researchers in [9] present a simulation-based method for the losses calculation that combines the MMC average and the SM's instantaneous model in a modular way, bringing the possibility to compare different high-

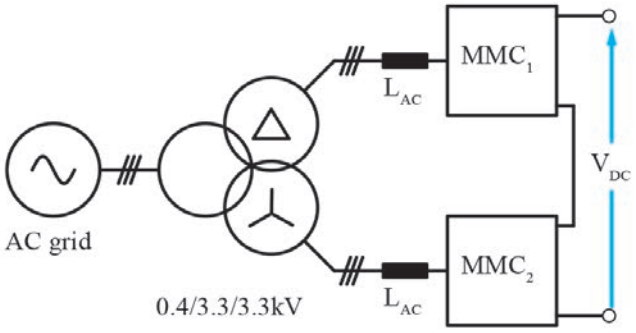

Fig. 1: Structure of the MMC based rectifier composed of two MMCs fed from a 12-pulse transformer.

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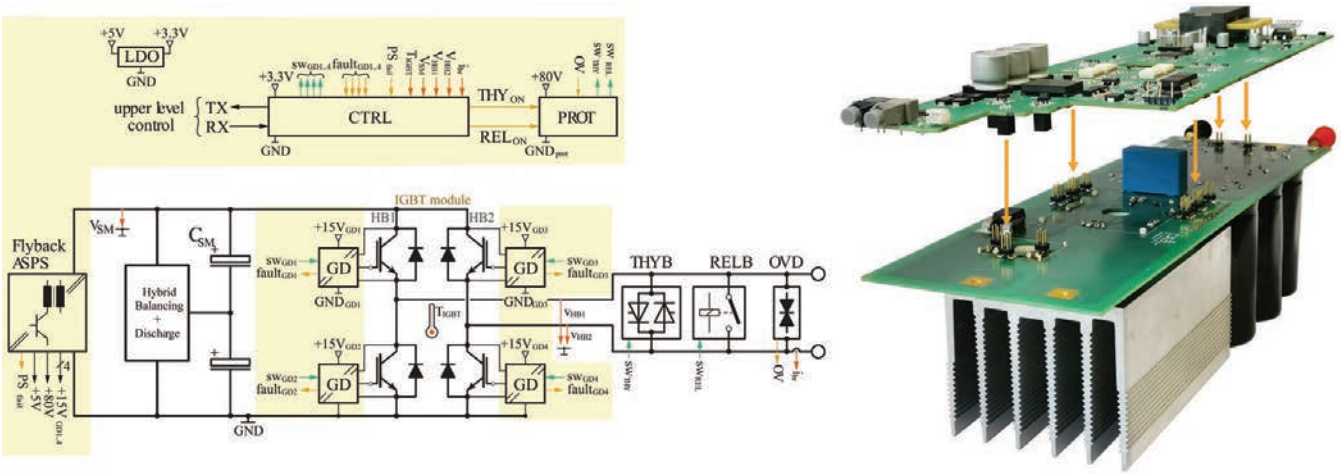

Fig. 2: Left side: SM's conceptual scheme. Yellow label corresponds to the low-voltage components. Remaining elements are the power components. Right side: SM prototype. Top PCB: low-voltage components. Bot. PCB: power components.

level and low-level control strategies as well as different SM configurations. Work in [10] presents the power loss and thermal characterization of both the half-bridge and full-bridge SM at the IGBT chip level by means of simulations and FEM, respectively. None of the works mentioned above have presented experimental verification of the estimated losses and thermal analysis. On the other hand, [11] proposes a SM's thermal balancing method. It was proposed to use a third-order polynomial to calculate conduction and switching losses from datasheet's operating curves and a second-order Foster model to estimate the thermal behaviour. Also, experimental tests have carried out to validate the power loss, thermal estimations, and the balancing method proposed.

This paper presents an experimental-based thermal study of the MMC SM's semiconductors in order to make sure they operate within its thermal limits. Presented results demonstrate the SM's power devices operate properly under nominal power and the worst thermal condition. Moreover, the SM is pushed beyond its designing parameters in order to determine the overload capacity and minimal required cooling effort for safe operation.

2 Sub-module characteristics

The SM of the MMC system shown in Fig. 1, composed of two MMCs, is presented in this work. The ac side of each converter is rated at 3.3 kV and are connected to the grid trough a conventional 12-pulse transformer. The dc side of each converter is able to generate voltage in the range of $\pm$ 5 kV and are connected in series in order to generate arbitrary voltage in the range of $\pm$ 10 kV. Each MMC is made out of 48 full-bridge SMs (8 per branch), operated with rated dc link voltage around 650 V.

The SM under test (cf. Figure 2) is built with the $SEMIKRON$ - $SK50GH12T4T$ 1.2 kV/50 A IGBT full-bridge module. A parallel connection of three capacitor branches, each of them consisting of a series connection of two 1.5 mF/400 V electrolytic capacitors, form a total SM capacitance of 2.25 mF. For protection, a fast and non-permanent bypass is realized with a 1.2 kV/72 A anti-parallel thyristor module (THYB), while a permanent bypass is provided by a relay (RELB). Losses of these components are not relevant during normal operation. An auxiliary submodule power supply (ASPS) supplies with low voltage the local controller (CTRL), the communication components (TX/RX), the IGBT's gate-drivers and the protection circuitry. Nominal heatsink's thermal resistance is 0.65 K W^{-1} under natural convection. More SM's operation details have been presented in [12] and [13]. A summary with SM's operating values is presented in Table 1.

3 Semiconductor losses

Semiconductor power losses are calculated using Eq. 1 for conduction power loss (P_c) and Eq. 2 for

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switching power loss (P_{sw}).

$$P_c = \frac{1}{T}\int_0^T V_c(I_{Load})I_{Load}(t)dt \quad (1)$$

$$P_{sw} = I_{Load}(E_{on} + E_{off} + E_{rr})f_{sw}\frac{V_{SM}}{V_{CE_{ref}}} \quad (2)$$

where T is the calculation period, V_c is the voltage during conduction, I_{Load} is the circulating current, E_{on} is the energy loss during the IGBT turn-on, E_{off} is the energy loss during the IGBT turn-off, E_{rr} is energy loss during diode turn-off, f_{sw} is the switching frequency, V_{SM} is the dc bus voltage of the SM and $V_{CE_{ref}}$ is the voltage at which the switching energy losses are defined. Finally, the total SM's loss is given by Eq. 3.

$$\begin{aligned} P_{total} = {} & P_c^{I-HB1_T} + P_c^{D-HB1_T} + P_c^{I-HB1_B} \\ & + P_c^{D-HB1_B} + P_c^{I-HB2_T} + P_c^{D-HB2_T} \\ & + P_c^{I-HB2_B} + P_c^{D-HB2_B} + P_{sw}^{HB1_T} \\ & + P_{sw}^{HB1_B} + P_{sw}^{HB2_T} + P_{sw}^{HB2_B} \end{aligned} \quad (3)$$

where $HB1$ and $HB2$ indicate half-bridge 1 and half-bridge 2 respectively (cf. Fig. 2).
Figure 3 shows the SM's thermal network used to calculate the maximum chip-level junction temperature T_j. T_s is the temperature measured inside of the IGBT module by means of an internal thermal-resistor. $R_{th_{j-s_{IGBT}}}$ is the junction to T_s thermal resistance for the IGBT, $R_{th_{j-s_{diode}}}$ is the junction to T_s thermal resistance for the diode and $R_{th_{s-a}}$ is the T_s to ambient thermal resistance. In this value the thermal resistance of the heatsink is also included. A reasonable expression to estimate T_j is given in Eq. 4 and Eq. 5.

$$\begin{aligned} T_j = T_s + max(& P_{c+sw}^{I-HB1,2_{T,B}} R_{th_{j-s_I}} \\ & + P_{c+sw}^{D-HB1,2_{T,B}} R_{th_{j-s_D}}) \end{aligned} \quad (4)$$

$$T_s = T_a + P_{total}R_{th_{s-a}} \quad (5)$$

By means of PLECS simulations, which already consider the previous expressions, the simulated

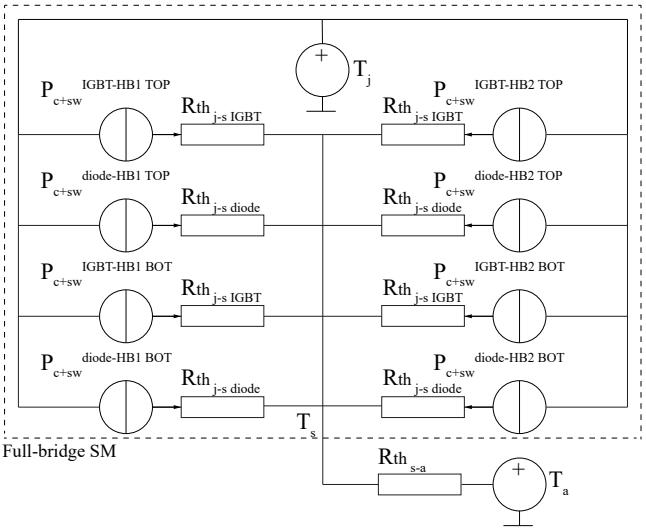

Fig. 3: Full-bridge SM's IGBT module thermal network.

semiconductor power losses and its thermal behaviour are presented in Fig. 4, where $R_{th_{j-sIGBT}}$ and $R_{th_{j-sdiode}}$ are 0.65 K W and 1.05 K W respectively. $R_{th_{s-a}}$ is 0.3 K W.

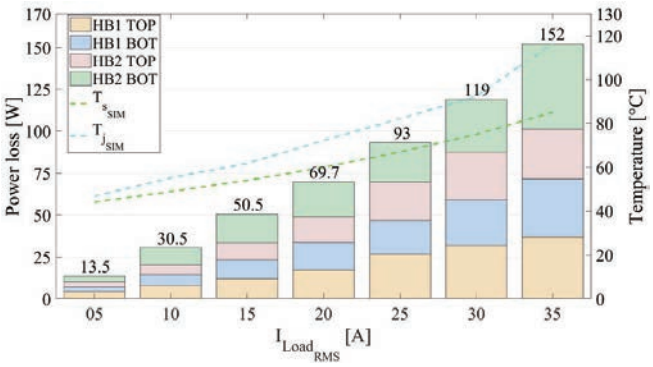

Fig. 4: SM's simulated semiconductor power loss and its thermal behaviour. HBx˙TOP represents the top IGBT-Diode set in the half-bridge 1 or 2. HBx˙BOT represents the bottom IGBT-Diode set in the half-bridge 1 or 2.

4 Experimental test setup

The experimental test setup is composed of two main parts. The electrical test setup, which aim is to emulate specific condition of voltage and current in the SM's terminals and, the thermal test setup, with the goal to produce a specific ambient condition (air temperature) and vary the air flow that circulates through the SM.

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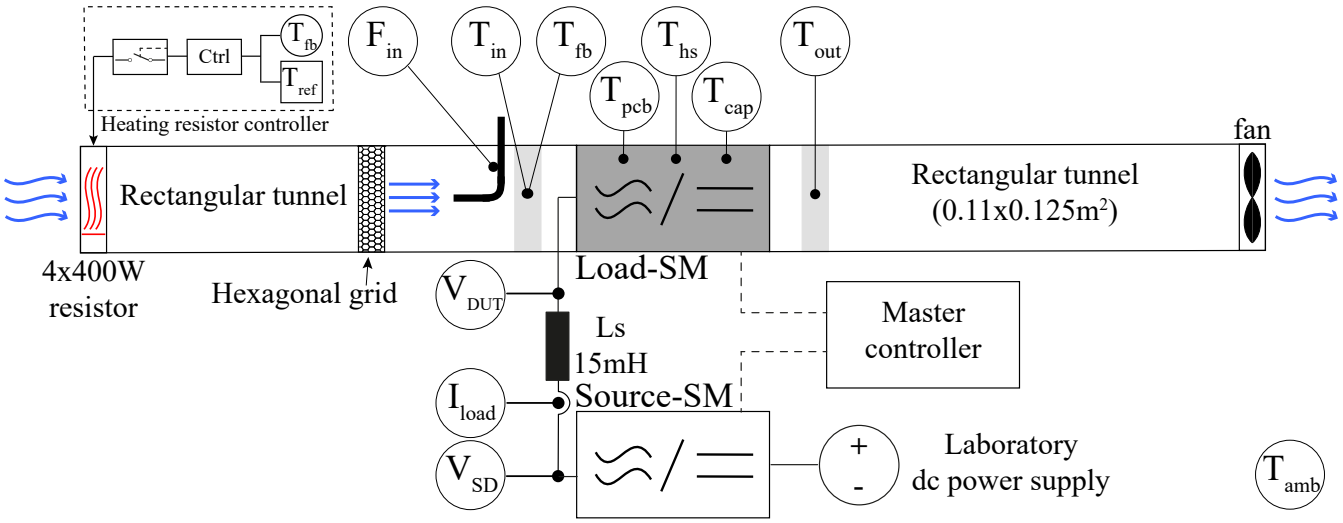

Fig. 5: Experimental test setup scheme using B2B configuration with two SMs.

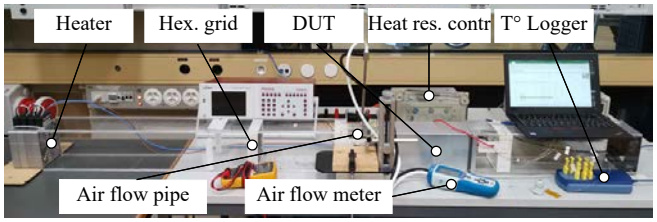

Fig. 6: Laboratory thermal test setup. It is shown only thermal components.

4.1 Electrical test setup

The electrical test setup part consists in two identical SMs connected in back-to-back (B2B) configuration in order to circulate power between them (cf. Fig. 5). The source SM is used for the purpose of stimulating the load SM by means of imposing a specific current (emulated branch current) that circulates through the coupling inductance L_s. The master controller calculates the corresponding modulation indexes for each device and it sends them through the optical-fiber link (TX-RX in Fig. 2) as well as a digital command to synchronize both PWM carriers every 125 µs. Also, master controller receives T_s temperature measured by each device (T_{IGBT} - CTRL in Fig. 2) and executes protection actions (to stop the test) in case of dc overvoltage, overcurrent and T_s overtemperature. Considered emulated branch current reference (or I_{Load}) contains three components [12]:

– a dc component, which corresponds to the active power exchange between the dc and ac side of the converter;

– a fundamental frequency ac component, which corresponds to half the ac grid current i_g;

– an optional second harmonic circulating current component, with amplitude $i_{circ,2}$ and phase ϕ.

thus, voltage and current waveform references generated by source SM in the setup are:

$$V_{SM_{ac}} = mV_{SM}sin(\omega t) \tag{6}$$

$$I_{Load} = \frac{3}{4}mI_g cos\phi + \frac{1}{2}I_g sin(\omega t + \phi) - \frac{m}{4}I_g cos(2\omega t + \phi) \tag{7}$$

where $V_{SM_{ac}}$ is the peak output voltage synthesized by the SM, V_{SM} is the SM's dc voltage, I_{Load} is the peak current that circulated through the SMs of the same branch, I_g is the peak SM's line current, m is the modulation index, ω is the grid frequency and ϕ is the voltage and current phase angle. The desired operating point of the MMC defines the parameters m, I_g and ϕ, producing different stresses of the SM. For the particular case of this work, the branch current emulation considers only the fundamental component.

During commissioning, the source SM is first tested

operating as an inverter. An ac-dc rectifier is connected in its dc terminals as a dc supply and a passive R-L load in its ac terminals. Figure 8 presents input and output active power during a total 15 kV A test showing the SM's operation at full power. Figures 7, Fig. 9 and Fig. 10 present the voltage and current waveforms of both the source and load SM. In Fig. 7 current is set at 20 A rms, in Fig. 9 current is set at 35 A rms, and in Fig. 10 current is set at 40 A rms (overload condition), showing the proper operation of the B2B configuration.

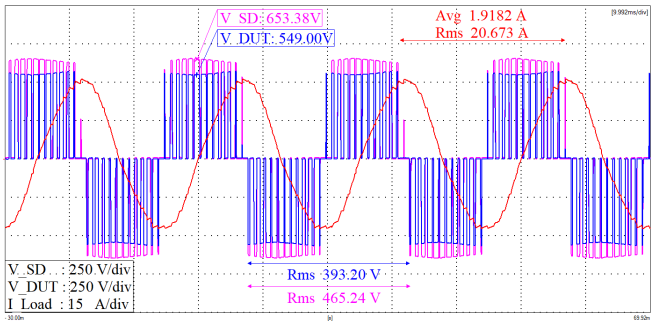

Fig. 7: Voltage and current waveforms of the source and load SM. Reference settings are $m = 0.8$, $\phi = 80°$ and $I_{max} = 28$ A. Source SM's output current is positive.

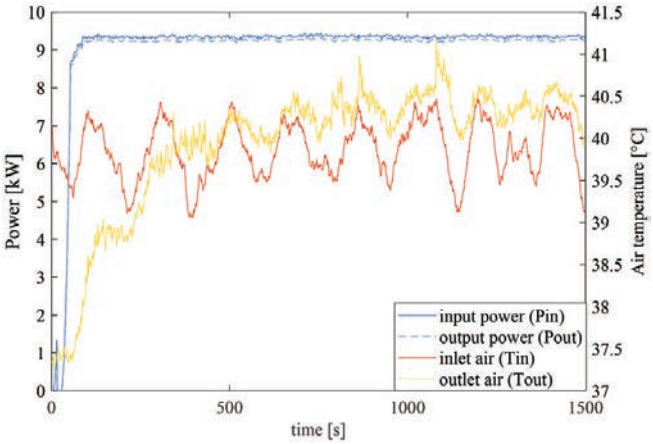

Fig. 8: Input output active power measurements and inlet outlet air temperature in the source SM. Test conditions: $T_{ref} = 40$ °C, $F_{in} = 2\,\mathrm{m\,s^{-1}}$, $V_{in} = 650$ V, $V_{out} = 460$ V, $S_{out} = 15$ kV A, $freq = 50$ Hz and $freq_{sw} = 1$ kHz.

4.2 Thermal test setup

The thermal part of the scheme shown in Fig. 5 is composed of two rectangular-profile tunnels with same the same SM's cross-section (0.110 x $0.125m^2$). The left side of the tunnel has a 4x400 W resistor which operation is controlled in order to preheat the inlet air to the desired temperature, above the room temperature. An hexagonal-shape metal grid is used to reduce the air's turbulences before the air-flow measurement (F_{in}), but it is not essential for test setup principles. Thermocouples T_{fb} and T_{in} measure the inlet air temperature used as the feedback for the hysteresis heating resistor controller and recorded by the temperature data logger respectively. T_{out} measures the outlet air temperature. In the last part of the tunnel a fan is placed for the extraction of the air with a maximum air speed of $5\,\mathrm{m\,s^{-1}}$. Thermocouples, T_{pcb} placed in the power PCB over one ac terminal, T_{hs} placed in the heatsink, close to the IGBT full-bridge case, and T_{cap} placed in a dc bus capacitor, are connected to the temperature data logger.

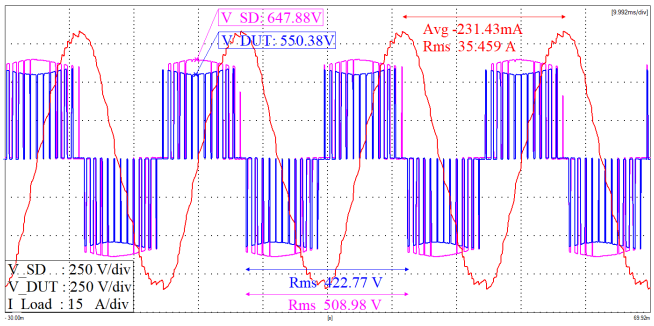

Fig. 9: Voltage and current waveforms of the source and load SM. Reference settings are $m = 0.9$, $\phi = 90°$ and $I_{max} = 50$ A. Source SM's output current is positive.

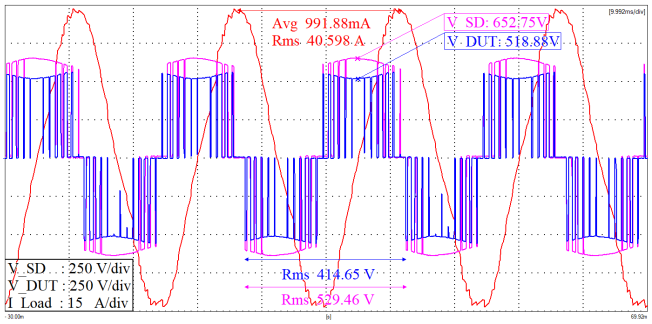

Fig. 10: Voltage and current waveforms of the source and load SM. Reference settings are $m = 0.98$, $\phi = 90°$ and $I_{max} = 56$ A.

During commissioning, thermal data was taken in order to estimate the accuracy of temperature controller (max. error of 2.5 %) and, to observe the quality of the measurements and general

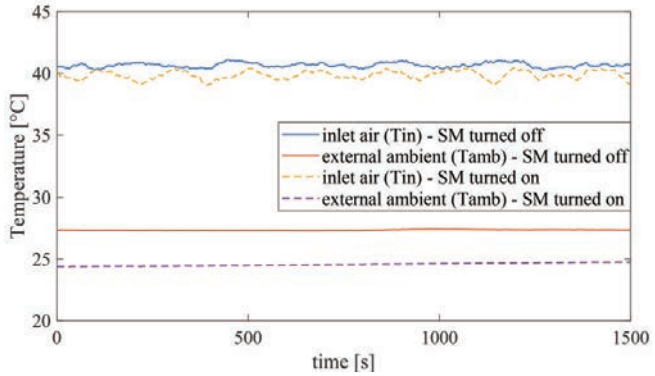

Fig. 11: Inlet air temperature when the SM is operating at full power and when is turned off. Inlet air temperature reference is 40 °C

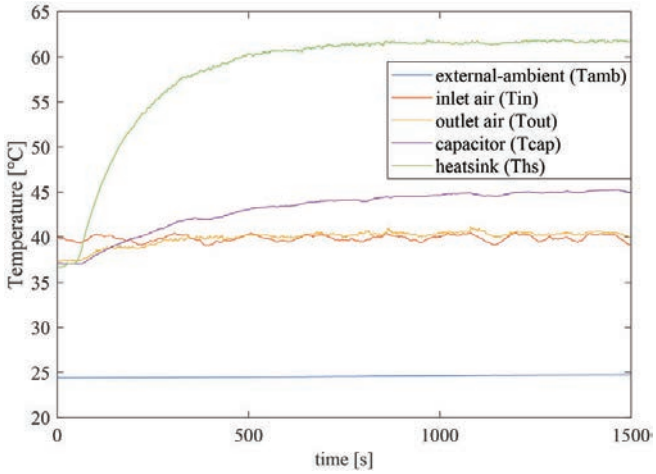

Fig. 12: Highest temperature of 63.8 °C appears at the heatsink while second higher of 43.5 °C appears in capacitor. Test conditions: T_{ref} = 40 °C, F_{in} = 2 m s^{-1}, V_{in} = 650 V, V_{out} = 460 V, S_{out} = 15 kV A, $freq$ = 50 Hz and $freq_{sw}$ = 1 kHz.

performance. Figure 11 shows T_{in} while the source SM was operating at full power and turned off. Figure 12 shows thermocouple measurements while the source SM operates at full power.

It is important to mention that the manufacturer recommends operating IGBT module while thermal resistor T_s measurement is below 100 °C. A safety margin of 10 °C is taken into account.

A summary of the B2B test conditions are presented in Table 2.

Tab. 1: SM's operating values

	Min.	Nominal	Max.	Units
Power	-	16	20	kV A
AC rms voltage	-	460	500	V
AC rms current	-	35	40	A
Switching freq.	-	500	1000	Hz
Power factor	-1	-	1	-
DC bus voltage	300	650	700	V
T_s	0	-	100	°C

Tab. 2: Experimental test conditions

	Value	Unit
Max. power	20	kV A
DC bus voltage	650	V
Coupling inductance	15	mH
Switching freq.	1000	Hz
Fundamental frequency	40-50	Hz
Max. T_s.	90	°C
Inlet air temp. Ref.	40	°C

5 Experimental results

The main goals of this work are to characterize the SM's thermal behaviour at different current levels, and to determine a minimal cooling effort (air speed passing through the SM) ensuring semiconductors' junction temperature less than 125 °C at worst case operating conditions.

The load SM's current and voltage waveforms at the terminals and temperatures were measured and recorded while circulating rms current was increased in steps of 5 A every 5 min aprox. Figure 13 shows measured temperatures with respect to the time. In $t = 30$ min output current is nominal, T_{hs} reaches 61 °C and $T_{cap} = 43.7$ °C. With the aim to determine the minimum cooling effort, at the same time, the air speed is reduced to 1 m s^{-1}. Under this condition, T_{hs} reaches 63.8 °C while T_s is at 83.4 °C. Lower air speed might causes exceeding the maximum temperature T_s. In $t = 40$ min air speed is increased to 2 m s^{-1} and circulating current is pushed to 40 A rms. In this condition (cf. Fig. 10) T_{hs} reaches 65.5 °C while T_s is at 87.8 °C. A larger current might causes exceeding the maximum temperature T_s. Figure 14 shows T_{hs} and T_s with

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respect to the SM's rms load current. Also, it shows $T_{s_{SIM}}$ and $T_{j_{SIM}}$ which were presented in the Fig. 4. T_a is set as 40 °C. $T_{s_{sim}}$ and T_s are close, showing similar tendency. $T_{s_{sim}}$ underestimation below $I_{Load} = 30$ A could be explained due losses (cf. Table 3) from the dc bus capacitor, ASPS and balancing circuit that extra heat-up the air inside of the SM's case. In fact, for simple inspection of Eq. 3, an extra 1 °C in T_a increases 1 °C T_s.

Tab. 3: Estimated SM's permanent losses.

	DC bus capacitors	Hybrid balancing circuit	ASPS	Total
Losses [W]	5.6	4.7	1.2	11.5

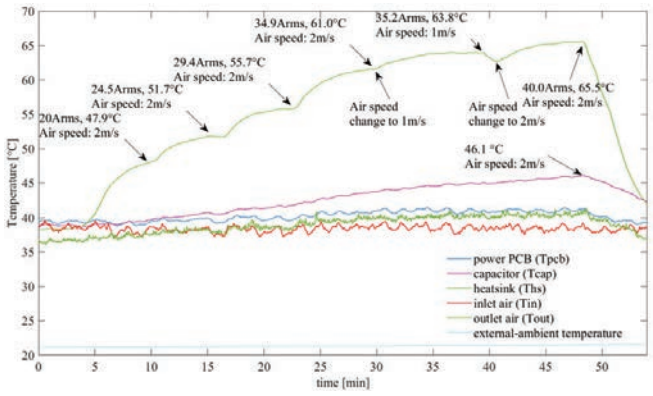

Fig. 13: The load SM's temperatures measured during different load and air speed conditions.

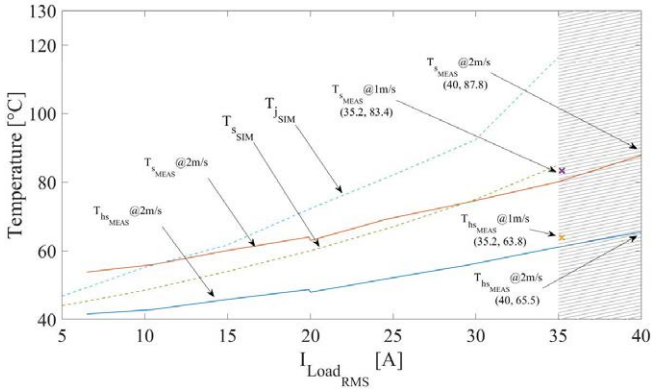

Fig. 14: Experimental and simulated load SM's temperature characterization with respect to the load current (I_{Load}).

6 Conclusions

This work presented a complete experimental setup in order to characterize a MMC SM from the thermal point of view. Ambient temperature and branch current can be emulated in order to operate the SM close to those conditions found in the real MMC application. As a baseline test, only fundamental branch current reference is used. It was found that the load SM's T_s temperature reaches 80 °C at nominal current and 87.8 °C at overload condition while air speed is set at 2 m s^{-1}. On the other hand, when reference current is set at nominal value but the air speed is reduced to 1 m s^{-1} the T_s temperature reaches 83.4 °C. In consequence, under the worst thermal condition (40 °C as inlet air temperature) it has been shown that the SM's power devices operate in a safe way since T_s is kept below 100 °C as is recommended by the manufacturer. Even more, it has been found that the minimal cooling effort needed at nominal power is 1 m s^{-1}. Simulated results using PLECS's thermal tool showed similar results.

References

[1] R Marquardt, "Stromrichterschaltungen mit verteilten energiespeichern", *German Patent DE10103031A1*, vol. 24, 2001.

[2] M. N. Raju, J. Sreedevi, R. P Mandi, and K. S. Meera, "Modular multilevel converters technology: a comprehensive study on its topologies, modelling, control and applications", *IET Power Electronics*, vol. 12, no. 2, pp. 149–169, 2019.

[3] H. Akagi, "Classification, Terminology, and Application of the Modular Multilevel Cascade Converter (MMCC)", *IEEE Transactions on Power Electronics*, vol. 26, no. 11, pp. 3119–3130, 2011.

[4] A Lesnicar and R Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range", in *2003 IEEE Bologna Power Tech Conference Proceedings,*, vol. 3, 2003, 6 pp. Vol.3–.

ISBN 978-3-8007-5245-4

[5] H. Wang, M. Liserre, and F. Blaabjerg, “Toward reliable power electronics: Challenges, design tools, and opportunities”, *IEEE Industrial Electronics Magazine*, vol. 7, no. 2, pp. 17–26, 2013.

[6] H. Wang, M. Liserre, F. Blaabjerg, P. de Place Rimmen, J. B. Jacobsen, *et al.*, “Transitioning to Physics-of-Failure as a Reliability Driver in Power Electronics”, *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 2, no. 1, pp. 97–114, 2014.

[7] W. Ali and A. Bissal, “Loss and Thermal Analyses for Modular Multilevel Converters”, in *2019 21st European Conference on Power Electronics and Applications (EPE ’19 ECCE Europe)*, 2019, P.1–P.7.

[8] M. Wu Cong, Y. Avenas, M. Miscevic, M. Wang, R. Mitova, *et al.*, “Thermal analysis of a submodule for modular multilevel converters”, in *2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014*, 2014, pp. 2675–2681.

[9] J. Freytes, F. Gruson, P. Delarue, F. Colas, and X. Guillaud, “Losses estimation method by simulation for the modular multilevel converter”, in *2015 IEEE Electrical Power and Energy Conference (EPEC)*, 2015, pp. 332–338.

[10] P. D. Judge, M. M. C. Merlin, P. D. Mitcheson, and T. C. Green, “Power loss and thermal characterization of IGBT modules in the Alternate Arm converter”, in *2013 IEEE Energy Conversion Congress and Exposition*, 2013, pp. 1725–1731.

[11] F. Hahn, M. Andresen, G. Buticchi, and M. Liserre, “Thermal Analysis and Balancing for Modular Multilevel Converters in HVDC Applications”, *IEEE Transactions on Power Electronics*, vol. 33, no. 3, pp. 1985–1996, 2018.

[12] A. Christe and D. Dujic, “Virtual Submodule Concept for Fast Semi-Numerical Modular Multilevel Converter Loss Estimation”, *IEEE Transactions on Industrial Electronics*, vol. 64, no. 7, pp. 5286–5294, 2017.

[13] M Utvic, I. P. Lobos, and D Dujic, “Low Voltage Modular Multilevel Converter Submodule for Medium Voltage Applications”, in *PCIM Europe 2019; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2019, pp. 1–8.

ISBN 978-3-8007-5245-4