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Abstract

This paper analyzes the effectiveness of the integration of the series inductor into the medium frequency transformer used for series resonant or dual active bridge converters - galvanically isolated DC-DC converters for high-power medium-voltage (solid state transformer) applications. The design of the two different DC-DC converter topologies is provided, considering high power ratings, with the emphasis on the required reference electrical parameters of the medium frequency transformer, especially the leakage inductance. An internally developed design optimization tool is used to analyze the influence of these reference parameters on the medium frequency transformer efficiency and power density, thus providing valuable insights and design guidelines.

1. Introduction

With the worldwide increase of the installed power of modern high-power electric applications, e.g. renewable energy generation, energy storage, e-mobility, railway etc., the solid state transformer (SST) [1] or power electronic transformer (PET) [2] concept is seen as the enabling technology of the future. With the still limited blocking voltages of the power semiconductor modules, the majority of solutions encountered in the literature resort to some kind of input-series output-parallel (ISOP) connection of the identical converter cells, as shown in Fig. 1, allowing for the direct connection on the medium-voltage MV side and high-current capabilities on the low-voltage (LV) side.

To enable the floating potential of the MV side of the cells, the galvanic insulation between primary and secondary side of each cell needs to be ensured. The two most common DC-DC converter topologies used as a building block of the SST cells are the series resonant converter (SRC) and dual active bridge (DAB), as given in Figs. 1b and 1c, respectively. These both use a medium-frequency transformer to achieve the galvanic insulation and input-output voltage matching. The MFT is therefore a key component of any SST, having a significant influence on its efficiency and power density.

Unlike in the case of LV switched mode power supplies, where various complex MFT structures can be used to efficiently match the reference electric parameters [3], in case of MV MFTs, simple constructions are preferred in order to facilitate the MV insulation [4]. While there are several references discussing the optimal modularity (number of cells connected in series/parallel) of the SSTs from the front-end [5] and the cell level [6] point of view, the design range of the SST is still not fully explored from the side of the DC-DC converter topology and its influence on the MFT parameters. This paper provides a comparative analysis of the MFTs, designed for the two SSTs with equivalent ratings, one based on the SRC and the other on DAB DC-DC converter topology, thus exploring the effectiveness of integration of the series inductor into the MFT.

Design of the SST and SRC and DAB DC-DC converter cells is presented in Sec. 2, providing the reference electrical parameters for the MFTs. A comparative analysis of influence of these reference parameters on the medium frequency transformer efficiency and power density is performed in Sec. 3. Main findings are summarized in Sec. 4.

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Tab. 1: SST and MFT electrical specifications

SST Specifications			
SST power	P_{SST}	1	MW
SST MV input	V_{MVDC}	10	kV
SST LV output	V_{LVDC}	750	V
Number of DC-DC cells	N	10	/
Semicond. blocking voltage	$V_{b.Si}$	1.7	kV
DC-DC Cell Specifications			
SST power	P_{Cell}	100	kW
Cell input voltage	V_{in}	1	kV
Cell output voltage	V_{out}	750	V
Switching frequency	f_{sw}	10	kHz
SRC MFT Specifications			
MFT power	P_m	100	kW
MFT primary voltage	V_{m1}	1	kV
MFT secondary voltage	V_{m2}	750	V
MFT primary current max.	I_{m1}	175	A
MFT primary current RMS	I_{rms1}	117	A
MFT leakage inductance	L_s	7.6	µH
Operating frequency	f_{sw}	10	kHz
DAB MFT Specifications			
MFT power	P_m	100	kW
MFT primary voltage	V_{m1}	1	kV
MFT secondary voltage	V_{m2}	750	V
MFT primary current max.	I_{m1}	127	A
MFT primary current RMS	I_{rms1}	117	A
MFT leakage inductance	L_s	83.3	µH
Operating frequency	f_{sw}	10	kHz

L_s is the total MFT leakage inductance ($L_{\sigma 1} + L'_{\sigma 2}$) referred to the primary side

2. SST Design

The considered SST structure and specifications are provided in Fig. 1 and Tab. 1, respectively. It consists of an ISOP connection of the identical isolated DC-DC converter cells. The selection of $1.7\mathrm{kV}$ Si semiconductors, considering a reasonable semiconductor blocking voltage utilization factor, leads to a design with 10 identical cells with $1\mathrm{kV}$ primary DC bus voltage and rated $100\mathrm{kW}$ - 10% of the total power. The switching frequency is set to $10\mathrm{kHz}$. While a detailed study of the influence of the SST modularity, choice of the semiconductor modules and switching frequency can be found in [6], in this study, these have been fixed to the aforementioned representative values.

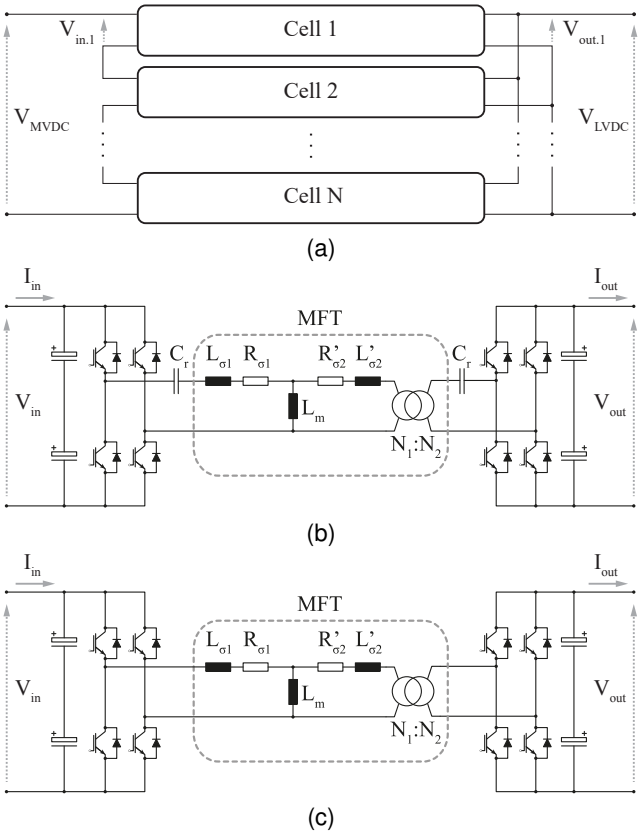

Fig. 1: SST ISOP configuration (a) and DC-DC converter topologies offering galvanic insulation, commonly used within SSTs: (a) SRC converter (b) DAB converter.

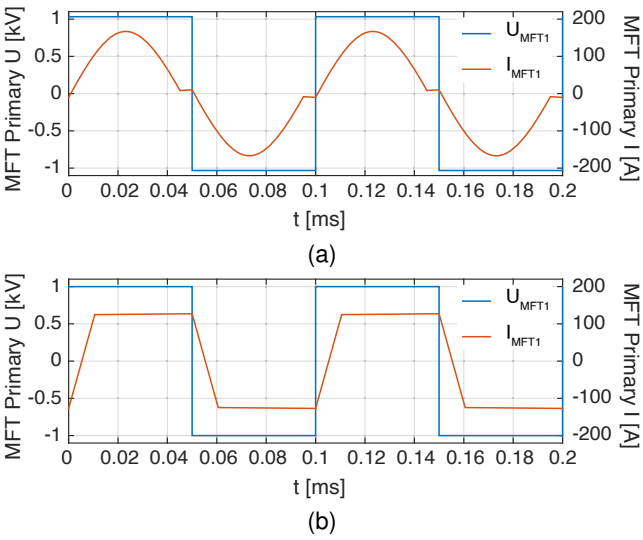

Fig. 2: Primary side MFT voltage and current waveforms in nominal operation, according to Tab. 1: (a) SRC and (b) DAB converter.

For the sake of simplicity and a more straightforward comparison, both in the case of a SRC and

DAB DC-DC converter cell, it is assumed that the converter stage is realized as a full-bridge. This results in the same input and output voltage specification of the MFT in both cases, as provided in Tab. 1.

2.1. SRC DC-DC Cell Design

The design of the resonant tank of the SRC, as shown in Fig. 1b, can be performed based on the desired operating mode and selected quality factor (Q). Using the first harmonic approximation, the equivalent nominal-load resistance referred to the primary side of the transformer can be calculated according to (1).

$$R_{ac1} = \frac{8n^2V_{out}^2}{\pi^2 P_n} \tag{1}$$

The reference values for the total series resonant capacitance and inductance can be calculated as

$$C_r = \frac{1}{2\pi f_0}\frac{1}{QR_{ac1}} \tag{2}$$

$$L_r = \frac{1}{2\pi f_0} QR_{ac1} \tag{3}$$

respectively, where

$$f_0 = 1.1 f_{sw} \tag{4}$$

is the desired resonant frequency. It is set 10% above the switching frequency to achieve subresonant operation, where the turn-off current of the primary side switches is limited to relatively small MFT magnetizing current, as shown in Fig. 2, whereas the secondary side diode current is reduced to zero, thus eliminating reverse recovery losses. Quality factor is set to 0.1 to ensure a resonant tank characteristic that will result in a large zero voltage switching (ZVS) region within the subresonant frequency range, hence ensuring the soft turn-on of the active switches at the intended operating point.

The reference magnetizing inductance of the resonant tank is designed to limit the maximum magnetizing current to the desired active switch turn-off current (I_{off}) according to equation (5).

$$L_m = \frac{V_{out}n}{8f_{sw}I_{off}} \tag{5}$$

2.2. DAB DC-DC Cell Design

For the design of the DAB DC-DC cell, it is assumed that the DAB is operating with 50% duty cycle pulses, as given in Fig. 2. In case of the given operation, the power flow is dictated by the phase shift of the given pulses between the primary and the secondary side as

$$P_{DAB} = \frac{nV_{m1}V_{m2}\varphi(\pi-\varphi)}{2\pi^2 f_{sw}L_s} \tag{6}$$

where n is the MFT transformation ratio, V_{m1} and V_{m2} are the primary and secondary side voltage pulse amplitudes, respectively, φ is the phase shift of the secondary side pulses relative to the primary side, f_{sw} is the switching frequency and L_s is the total series inductance.

The next reasoning is used to define the appropriate L_s. The theoretical maximum power is transferred at $|\varphi| = \pi/2$, and this point also represents the limit of stability which must not be reached. In that respect, the substitution of $|\varphi| = \pi/2$ into (6) leads to the expression for the maximum power operating range

$$P_{DAB.max} = \frac{nV_{m1}V_{m2}}{8f_{sw}L_s}. \tag{7}$$

The series inductance L_s should therefore be designed to ensure that this maximum power is higher than the rated DAB converter power level considering a reasonable margin

$$P_{DAB.max} = K_P P_m \tag{8}$$

where $P_{DAB.max}$ is the designed maximum theoretical power of the DAB at the limit of stability, P_m is the rated power of the converter, and $K_P > 1$ is the overpower margin. Substitution of (7) into (8) and some rearranging leads to the constraint for the maximal value of the series leakage inductance

$$L_s = \frac{nU_1U_2}{8f_{sw}K_P P_m}. \tag{9}$$

High K_P provides a large overpower margin, but in also narrows down the φ range of the converter in normal operation. This causes the power control to becomes increasingly sensitive to noise and signal latency. The appropriate selection of K_P and the

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Tab. 2: Considered MFT design choices

Transformer type	Shell
Winding type	Helical concentric
Conductor type	Litz Wire (AWG 32) (150°C)
Core type	Rectangular cut cores (UU)
Core material 1	Nanocrystalline (140°C)
Core material 2	Si-Ferrite N87 (100°C)
Cooling conditions	Natural air convection at 25°C

Temperatures in brackets denote the maximum allowed material temperatures

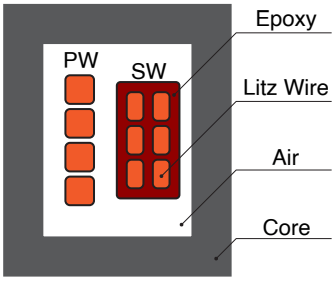

Fig. 4: Illustration of the MFT cross-section, describing the insulation concept. The inner, LV winding, is freely suspended in the air, held by a coil former. The MV insulation of the secondary winding is assumed to be realized with solid epoxy coating of appropriate thickness.

resulting L_s is therefore a trade-off between ensuring the appropriate power margin (ensuring stable operation) and robustness of the whole system to various imperfections, present in any practical control hardware implementation. In this study, L_s is designed for $K_P = 1.5$, as a reasonable overpower margin that still results in a relatively wide φ range of the converter in normal operation (between -0.7 and 0.7 rad).

3. Comparative MFT Analysis

The aforementioned reference series inductance ($L_{s.ref}$) can be integrated within the MFT by appropriate design of its leakage inductance

$$L_{s.ref} = L_{\sigma 1} + L'_{\sigma 2} \tag{10}$$

where $L_{\sigma 1}$ and $L'_{\sigma 2}$ are the primary and secondary MFT leakage inductance referred to the primary side, as displayed in Figs. 1b and 1c. Another option is to add a series inductor (L_{ind}), specially designed to complement the total MFT leakage inductance in order to match the required reference

$$L_{s.ref} = L_{\sigma 1} + L'_{\sigma 2} + L_{ind}. \tag{11}$$

The derived reference specifications of the MFTs with integrated series inductor, are summarized in Tab. 1, and the nominal primary side current and voltage vaweforms are displayed in Fig. 2. While the two MFTs have the same power ratings and experience the same voltage excitation, the current waveforms and the total leakage inductance refer-

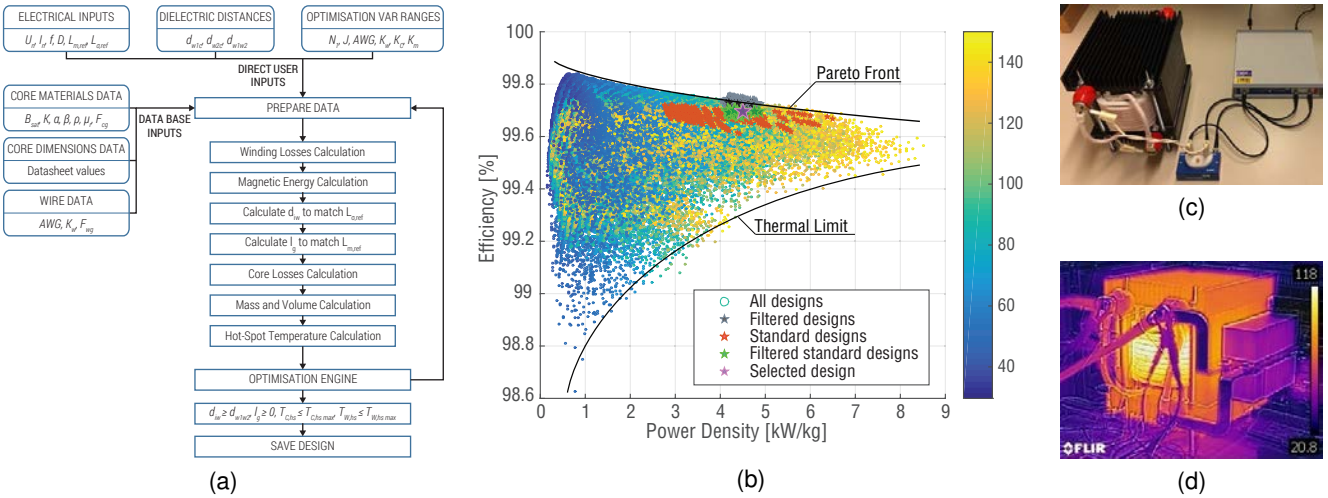

Fig. 3: Methodology [7]: (a) A brute-force model-based MFT design optimization algorithm; (b) Set of all feasible designs and filtered optimal design; (c) Measurement of the optimal MFT prototype electric parameters using Bode 100 vector network analyzer; (d) Thermal camera image of the MFT prototype at full load steady state operation.

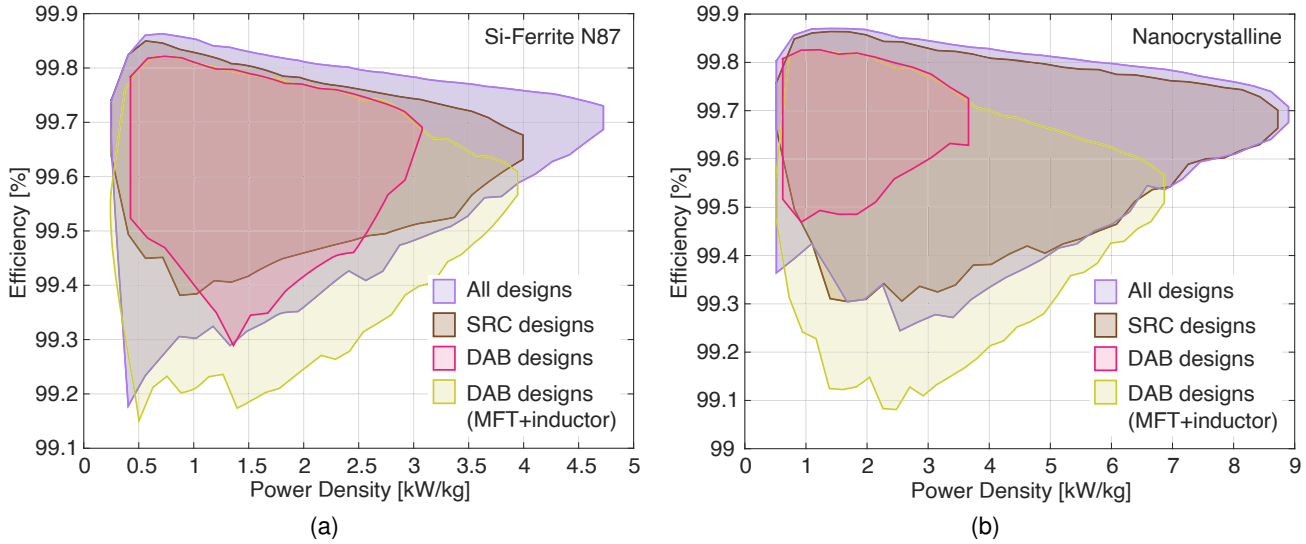

Fig. 5: Plots of all feasible MFT design sets for the two different core materials: (a) Si-ferrite and (b) Nanocrystalline. Plots show all feasible MFT designs for the given specifications: regardless of the leakage inductance (all designs), with the leakage inductance according to the SRC series inductor reference (SRC designs) and with the leakage inductance according to the DAB series inductor reference (DAB designs), as given in Tab. 1. Plot of all feasible designs of the MFT-inductor pairs, according to DAB series inductor reference, are presented in yellow. All of the designs assume design choices and solid epoxy cast $10\mathrm{kV}$ insulation level for the secondary (MV) winding as provided in Tab. 2 and Fig. 4.

ences are different for the two converters. It can be seen that the DAB converter requires a one order of magnitude higher series equivalent inductance. In case of compact design, where the series inductor is integrated within the MFT leakage inductance, this represents a significantly different design reference. On the other hand, while the current amplitude is higher in case of the SRC, the RMS values are identical in both cases, and therefore the expected ohmic winding losses. Note that this is a first order harmonic approximation of the winding losses where higher frequency harmonics are not taken into account separately, accurate enough for design comparison purposes - winding loss estimation errors below 10%.

In order to analyze the design implications tied to this different reference point, an internally developed and experimentally verified (on a $100\mathrm{kW}$, $10\mathrm{kHz}$ MFT prototype) MFT design optimization algorithm, as presented in [7], [8] and illustrated in Fig. 3, is used to produce and analyze the sets of all feasible MFT designs, as provided in Fig. 5. Considered MFT geometry, materials and design choices are summarized in Tab. 2 and Fig. 4. Two different core materials, characteristic for the given operating frequency, are investigated, namely: Si-ferrite and nanocrystalline. Solid cast epoxy is considered for the necessary $10\mathrm{kV}$ insulation of the MV (secondary) winding, as illustrated in Fig. 4.

Analyzing the feasible MFT design sets, it can be seen that the leakage inductance reference has a strong influence on the expected MFT maximum performance in terms of efficiency and power density. In case of a low leakage inductance requirement, such as the case of the SRC MFT, it can be seen that the "SRC designs" sets feature a slightly lower efficiency and power density compared to the sets of all feasible MFT designs "All designs".

On the other hand, the integration of high leakage inductance significantly compromises both the efficiency and power density of the MFT. This is due to the fact that the increase of the leakage flux field, responsible for leakage inductance, also affects the winding losses thus decreasing the efficiency and increasing the thermal constraint of this design set. This result suggests that in case of inductor integration, a much better performing MFT can be made in case of SRC converter compared to DAB, as shown in Fig. 5. Consequently, the design with external inductor represents an interesting option in case of a DAB converter based SST.

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Tab. 3: Highest power density designs without leakage inductance constraint (All designs)

Si-Ferrite N87		Nanocrystalline	
Pow. Dens.	Tot. Leakage	Pow. Dens.	Tot. Leakage
$4.7\mathrm{kW/kg}$	$22.3\mu\mathrm{H}$	$9.1\mathrm{kW/kg}$	$8.7\mu\mathrm{H}$

It is interesting to notice that the relative positions of these sets are different for the two materials. This can be explained by analyzing the MFT designs with highest power density from the unconstrained set ("All designs" from Fig. 5 without leakage inductance constraint) for both core materials. The power density and leakage inductance of these designs are given in Tab. 3. In case of nanocrystalline, the leakage inductance of this design is only slightly higher compared to the reference SRC leakage inductance from Tab. 1. This explains the very good matching of the these two sets, "SRC designs" and "All designs" and bad matching with "DAB designs" which require much higher leakage inductance. On the other hand, the ferrite design with highest power density features a higher leakage inductance, thus resulting in slightly worse matching between "SRC designs" and "All designs" and better matching between "DAB designs" and "All designs" compared to the nanocrystalline case. In this context, good matching with "All designs" means less sub-optimal, since any constrained design set is a subset of the unconstrained set.

While it is not possible to relax the maximum allowed leakage inductance constraint in case of the SRC design, in case of DAB, any MFT design that has a lower total leakage inductance than the required reference can be complemented with an external inductor, according to (11). Plot of all feasible designs of the MFT-inductor pairs, according to DAB series inductor reference, are presented in Fig. 5 in yellow. A similar design optimization algorithm, as shown in Fig. 3 has been developed for AC inductors. AC inductor designs have been optimized for minimum possible mass considering the same design choices, as given in Tab. 2, and for the range of specifications that complement the maximum feasible MFT design set ("All designs") to match the required DAB series inductance reference, as provided in Tab. 4 and Fig. 6. Similar to the case of MFT, only the active components of the

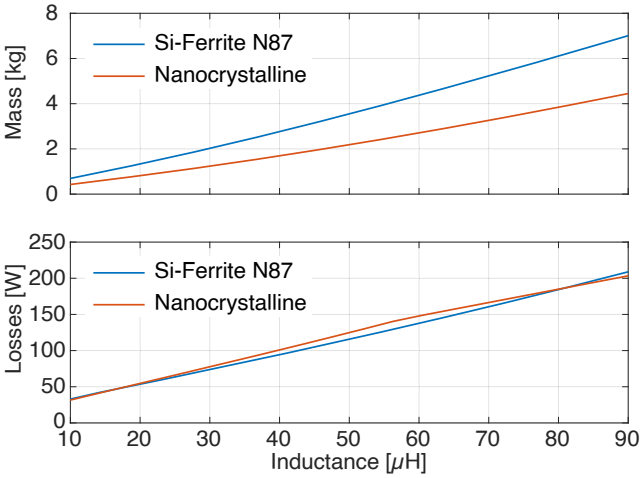

Fig. 6: Plots of optimized inductor characteristics, (top) mass and (bottom) losses, within the reference parameter range of interest (Tab. 4) for the two considered materials - nanocrystalline and Si-Ferrite N87. Note that the inductors have been purely optimized for the minimum possible weight, with respect to the maximum allowed temperatures of the core and windings, as provided in Tab. 2.

Tab. 4: Inductor Electric Specifications

I_m	I_{rms}	L_{ind}	f_{sw}
$127\mathrm{A}$	$117\mathrm{A}$	$[10-90]\mu\mathrm{H}$	$10\mathrm{kHz}$

Note that L_{ind} range is set to complement any of the feasible MFT designs (Fig. 5) with not enough leakage inductance for DAB converter application

inductor, core and the windings, are considered in mass and loss calculation. The design set of MFT-inductor pairs is generated by pairing each of the MFT designs form "All designs" with a matching inductor, such that (11) is satisfied. Note that only the same core material combinations are considered - e.g. ferrite MFT with ferrite inductor.

As can be seen in Fig. 5, the design set of MFT-inductor pairs exhibits significantly higher combined maximum power density compared to the integrated series inductor alternative - roughly 30% and 100% in case of ferrite and nanocrystalline designs, respectively. Note that that the inductor losses and mass have been added to those of the corresponding MFT in the MFT-inductor pair plots in Fig. 5.

Based on these results, it can be seen that the correct design and coordination of magnetic components can significantly improve the performance of the system.

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4. Conclusion

The choice of DC-DC converter topology of the SST cell results in significantly different reference electric parameters of the MFT. Designing the MFT with such specifications can significantly affects the MFT maximum performance in terms of efficiency and power density. This paper provides a comparative analysis of different solutions - MFTs designed for the two SSTs with equivalent ratings, one based on the SRC and the other on DAB DC-DC converter topology thus exposing the effectiveness of integration of the series inductor into the MFT.

It has been found that, for the given scenario, the MFT designs for the SRC specifications exhibit significantly higher maximum power density compared to the DAB alternative with integrated series inductor, especially in case of the designs with nanocrystalline core (roughly 2.3 times higher). It was also shown that the MFT-inductor pair can achieve a significantly better performance in comparison to the MFT with integrated series inductor alternative in case of DAB. While in case of ferrite core design, the MFT-inductor pair for DAB has a similar maximum performance as an MFT for SRC, in case of nanocrystalline design, the SRC MFT can still achieve a higher maximum power density (roughly 25% higher compared to DAB MFT-inductor).

Based on this study, it can be concluded that, depending on the specific scenario, a significant improvement of power density can be achieved by careful consideration of system requirements and appropriate design and coordination of magnetic components.

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