

**At the end of scaling:
2D materials for computing and sensing applications**

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Some humans would do anything to see if it was possible to do it. If you put a large switch in some cave somewhere, with a sign on it saying 'End-of-the-World Switch. PLEASE DO NOT TOUCH', the paint wouldn't even have time to dry.

Terry Pratchett (1948-2015)
Thief of Time

Alla mia famiglia, agli amici e a Ladina

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Nicolò Oliva

Abstract

In the past half-century, the digital revolution completely changed the world we live in and the ways we experience it. Over this period, the underlying force supporting the continuous technological development has been the geometrical scaling of transistor dimensions, resulting in an exponential increase of the computation power density as well as a drastic decrease of chip cost. Approaching the end of the CMOS scaling era, the semiconducting industry faces enormous challenges to redefine its research priorities. Moreover, novel strict requirements on energy efficiency, system autonomy and remote sensing are posed by the development of the Internet of Things (IoT) networks. The quest for novel materials and device working principle is therefore more critical than ever. "More than Moore" devices aim to overcome the fundamental physical limitations of the MOSFET structure so to either replace or complement CMOS technology in a broad range of applications. Among this variegated research field, tunnel FETs have attracted a consistent interest in the last decades because of their steep turn on characteristic enabling the power supply scaling while maintaining a low standby power consumption. Several materials and TFET architectures have been demonstrated, with both promising results and great challenges in the quest for reducing the persisting performance gap with the established CMOS technology.

The aim of this thesis is to demonstrate the potential of two dimensional (2D) materials and heterojunctions for the realization of "More than Moore" devices as well as for high sensitivity sensors. The continuously expanding family of 2D materials offers a huge catalog of electronic, mechanical and optical properties. The transition metal dichalcogenide (TMDC) group in particular includes a set of promising semiconductors with relatively large, number of layer dependent, band gap. MoS₂ FET with excellent performance have been reported, while WSe₂ has the potential of becoming the base for a true 2D CMOS platform.

MOSFET devices were fabricated starting from black phosphorous and WSe₂ in order to investigate respectively fabrication strategies characterized by a reduced air exposure and the deposition of high k dielectric on 2D flakes. We then investigated the opportunities offered by the deterministic transfer of 2D flakes realizing both 3D/2D and 2D/2D heterojunction devices. The first reported VO₂/MoS₂ devices have been demonstrated obtaining a good rectifying characteristic and excellent, temperature tunable photosensitivity. Prototypes of three terminal devices based on this junction open the possibility for true VO₂ based field effect devices. Finally, a heterojunction TFET based on WSe₂/SnSe₂ is presented. Our devices exhibit an excellent turn on characteristic and a direct comparison with the built-in, same flake WSe₂ FET show how they outperform the MOSFET realized in the same material system. Moreover, we propose a new device combining the advantages of both MOSFET and TFET in a unique structure.

Key words: two dimensional (2D) materials), heterojunctions, tunnel FET, band to band tun-

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neling (BTBT), insulator-metal transition (IMT), functional oxides, vanadium dioxide (VO_2), Complementary metal oxide semiconductor (CMOS), electrical characterization, atomic force microscopy (AFM), scanning electron microscopy (SEM), X-ray diffraction (XRD), steep-slope devices, field effect transistor (FET), reconfigurable electronics.

Riassunto

Nell'ultimo mezzo secolo, la rivoluzione digitale ha cambiato completamente il mondo in cui viviamo e interagiamo con quello che ci circonda. Durante tutto questo periodo, il continuo sviluppo tecnologico è stato reso possibile dalla riduzione delle dimensioni fisiche dei transistor, che ha determinato un aumento esponenziale della capacità di calcolo e una drastica diminuzione del costo dei chip. Avvicinandosi alla fine dell'era di riduzione delle dimensioni dei CMOS, l'industria dei semiconduttori affronta enormi sfide nel ridefinire le sue priorità di ricerca e sviluppo. Inoltre, lo sviluppo del cosiddetto Internet of Things (IoT) pone nuove stringenti necessità in termini di efficienza energetica, autonomia e sensoristica remota. La ricerca di nuovi materiali e dispositivi elettronici è pertanto più importante che mai. I dispositivi classificabili come "Moore than Moore" hanno come obiettivo il superamento delle limitazioni fisiche fondamentali dei MOSFET, in modo da rimpiazzare o integrare la tecnologia CMOS in un ampio spettro di applicazioni. In questo variegato campo di ricerca, i tunnel FETs hanno attirato un notevole interesse nelle ultime decadi grazie alla ripida curva di accensione/spegnimento che permette la riduzione della tensione di alimentazione mantenendo un basso consumo nello stato di standby. Numerosi materiali e architetture per TFET sono stati considerati, ottenendo risultati incoraggianti ma sottolineando allo stesso tempo le grandi sfide da affrontare per colmare la differenza di performance con la consolidata tecnologia CMOS.

L'obiettivo di questa tesi è dimostrare il potenziale dei materiali due dimensionali (2D) e delle eterogiunzioni per realizzare dispositivi "More than Moore" e sensori ad alta sensibilità. La famiglia dei materiali 2D è in continua espansione e offre un'ampia scelta di interessanti proprietà elettroniche, meccaniche e ottiche. Il gruppo dei materiali transition metal dichalcogenide (TMDC) comprende una serie di semiconduttori promettenti, caratterizzati da un band gap relativamente grande e dipendente dal numero di strati di materiale. FET realizzati a partire da MoS_2 e con ottime caratteristiche elettriche sono stati più volte dimostrati in letteratura, mentre WSe_2 ha il potenziale per diventare la base di una vera e propria piattaforma CMOS due dimensionale. Dispositivi MOSFET sono stati fabbricati a partire da fosforo nero e WSe_2 per sperimentare rispettivamente tecniche di fabbricazione con ridotta esposizione all'aria e la deposizione di dielettrici ad alta costante dielettrica su materiali 2D. Quindi, abbiamo valutato le opportunità offerte dal trasferimento deterministico di strati 2D per la realizzazione di eterogiunzioni 3D/2D e 2D/2D. I primi dispositivi basati su giunzioni VO_2/MoS_2 sono stati dimostrati, ottenendo un'ottima caratteristica rettificante e un'eccellente fotoresponsività termosensibile. Prototipi di dispositivi a tre terminali basati su questa eterogiunzione aprono alla possibilità di realizzare veri e propri dispositivi ad effetto di campo basati su VO_2 . Al termine della tesi, presentiamo un TFET basato sull'eterogiunzione $\text{WSe}_2/\text{SnSe}_2$. Il nostro dispositivo esibisce una eccellente curva di accensione/spegnimento e un raffronto diretto con WSe_2 FET costruiti sugli stessi strati di materiale delle eterogiunzioni dimostra che il TFET ha migliori performance nel regime sot-

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to soglia. Inoltre, proponiamo un nuovo dispositivo con l'obiettivo di combinare i vantaggi di MOSFET e TFET in un'unica struttura.

Parole chiave: Materiali 2 dimensionali, eterogiunzioni, tunnel FET, tunneling da banda a banda (BTBT), transizione isolante-metallo, ossidi funzionali, diossido di vanadio (VO_2), CMOS, caratterizzazione elettrica, AFM, SEM, XRD. dispositivi a steep-slope, transistor a effetto di campo (FET), elettronica riconfigurabile.

Zusammenfassung

Im vergangenen halben Jahrhundert hat die digitale Revolution die Welt, in der wir leben, und die Art und Weise, wie wir sie erleben, völlig verändert. In diesem Zeitraum war die zugrunde liegende Kraft, die die kontinuierliche technologische Entwicklung vorantrieb, die geometrische Skalierung der Transistordimensionen. Dies führte zu einer exponentiellen Erhöhung der Rechenleistungsdichte sowie zu einer drastischen Senkung der Chip-Kosten. Mit dem Ende der CMOS-Skalierungsära steht die Halbleiterindustrie vor enormen Herausforderungen, um ihre Forschungsprioritäten neu zu definieren. Darüber hinaus werden durch die Entwicklung des Internet der Dinge (IoT) neue strenge Anforderungen an Energieeffizienz, Systemautonomie und Fernerkundung gestellt. Die Suche nach neuartigen Materialien und Funktionsprinzipien von Geräten ist daher kritischer denn je. Die "More than Moore"-Bauelemente zielen darauf ab, die grundlegenden physikalischen Grenzen der MOSFET-Struktur zu überwinden, um die CMOS-Technologie in einem breiten Spektrum von Anwendungen entweder zu ersetzen oder zu ergänzen. In diesem vielseitigen Forschungsbereich haben Tunnel-FETs in den letzten Jahrzehnten aufgrund ihrer steilen Einschaltcharakteristik, die eine Skalierung der Stromversorgung bei gleichzeitig niedrigem Standby-Stromverbrauch ermöglicht, ein beständiges Interesse geweckt. Es wurden mehrere Materialien und TFET-Architekturen vorgestellt, wobei sowohl vielversprechende Ergebnisse als auch grosse Herausforderungen bei der Suche nach der Verringerung des fortbestehenden Leistungsabstands zur etablierten CMOS-Technologie zu verzeichnen waren.

Das Ziel dieser Arbeit ist es, das Potential von zweidimensionalen (2D) Materialien und Heteroübergängen für die Realisierung von "More than Moore"-Geräten sowie für hochempfindliche Sensoren zu zeigen. Die sich ständig erweiternde Familie der 2D-Materialien bietet einen riesigen Katalog von elektronischen, mechanischen und optischen Eigenschaften. Insbesondere die Gruppe der Übergangsmetall-Dichalkogeniden (TMDC) umfasst eine Reihe von vielversprechenden Halbleitern mit relativ grosser, schichtabhängiger Bandlücke. Es wurde über MoS_2 FET mit ausgezeichneter Leistung berichtet, während WSe_2 das Potenzial hat, die Basis für eine echte 2D-CMOS-Plattform zu werden.

MOSFET-Bausteine wurden ausgehend von schwarzem Phosphor und WSe_2 hergestellt, um entsprechende Herstellungsstrategien zu untersuchen, die sich durch eine reduzierte Aussetzung in der Luft und die Abscheidung von hohem k -Dielektrikum auf 2D-Flakes auszeichnen. Anschliessend untersuchten wir die Möglichkeiten, die der deterministische Transfer von 2D-Flakes bietet, um sowohl 3D/2D- als auch 2D/2D-Heteroübergangsbaulemente zu realisieren. Die ersten berichteten VO_2/MoS_2 -Bauelemente haben nachweislich eine gute Gleichrichtungscharakteristik und eine ausgezeichnete, temperaturabstimbare Lichtempfindlichkeit erhalten. Prototypen von drei Endgeräten, die auf dieser Verbindung basieren, eröffnen die Möglichkeit für echte VO_2 -basierte Feldeffektgeräte. Schliesslich wird ein Heteroübergang TFET auf der Basis von $\text{WSe}_2/\text{SnSe}_2$ vorgestellt. Unsere Geräte weisen eine hervorragende Einschalt-Eigenschaft und ei-

nen direkten Vergleich mit dem eingebauten, gleichfarbigen WSe₂ auf. Die FETs zeigen, wie sie die im gleichen Materialsystem realisierten MOSFETs übertreffen. Ausserdem schlagen wir ein neues Bauelement vor, das die Vorteile von MOSFET und TFET in einer einzigartigen Struktur kombiniert.

Schlüsselwörter: Zweidimensionale (2D) Materialien), Heteroübergänge, Tunnel-FET, Band-zu-Band-Tunnelung (BTBT), Isolator-Metall-Übergang (IMT), funktionelle Oxide, Vanadiumdioxid (VO₂), Komplementärer Metalloxid-Halbleiter (CMOS), elektrische Charakterisierung, Rasterkraftmikroskopie (AFM), Rasterelektronenmikroskopie (REM), Röntgenbeugung (XRD), Bauelemente mit steiler Neigung, Feldeffekttransistor (FET), rekonfigurierbare Elektronik.

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Acronyms

2D Two dimensional.

3D Three dimensional.

AFM Atomic force microscopy.

ALD Atomic layer deposition.

BTBT Band to band tunneling.

CMi Center of MicroNanoTechnology.

CMOS Complementary metal-oxide-semiconductor.

CVD Chemical vapor deposition.

DC Direct current.

DUT Device under test.

e-beam Electron beam.

e.g. *exempli gratia*.

EPFL École polytechnique fédérale de Lausanne.

et al. *et alii* (and others).

FEM Finite element method.

FET Field-effect transistor.

FinFET Fin field-effect transistor.

GAA Gate all around.

IC Integrated circuit.

ICDD The International Centre for Diffraction Data.

Acronyms

IMT Insulator-metal transition.

LESO-PB Laboratoire d’Energie Solaire et de Physique du Bâtiment.

LPCVD Low pressure chemical vapor deposition.

MEMS Micro electromechanical systems.

MIM Metal-insulator-metal.

MIT Metal-insulator transition.

MOSFET Metal-oxide-semiconductor field-effect transistor.

NDR NEgative differential resistance.

NW Nanowire.

PC-TFET Phase change tunnel field-effect transistor.

PIN p-doped intrinsic n-doped.

PLD Pulsed laser deposition.

PVD Physical vapor deposition.

R&D Research and development.

ReRAM Resistive random access memory.

RF Radio frequency.

SEM Scanning electron microscopy.

SMU Source monitor unit.

SOI Silicon on insulator.

SPM Scanning probe microscopy.

SPTS SPP Process Technology Systems.

SSOI Strained silicon on insulator.

SWCNT Single-walled carbon nanotube.

TCAD Technology Computer-Aided Design.

TEM Transmission electron microscopy.

TFET Tunnel field-effect transistor.

TMDC Transition metal dichalcogenides.

TMO Transistion metal oxide.

UHV Ultra-high vacuum.

VMU Voltage monitor unit.

XRD X-ray diffraction.

List of symbols

Symbol	Unit	Description
	-	Electron affinity
B_{3dB}	Hz	Bandwidth -3 dB (FWHM)
C_G	F	Discrete capacitance under ground plane
C_S	F	Discrete capacitance under signal line
C_{OFF}	F	Equivalent capacitance in OFF-state
C_{ON}	F	Equivalent capacitance in ON-state
C_{TOT}	F	Equivalent series capacitance of C_S and C_G
C_d	F	Depletion capacitance in a MOS structure.
C_{ox}	F	Oxide capacitance in a MOS structure.
C	F	Capacitance
E_C	-	Conduction band
E_{Fi}	-	Intrinsic Fermi level
E_F	-	Fermi level
E_V	-	Valence band
G_D	-	Internal drain voltage amplification in a PC-TFET
G_G	-	Internal gate voltage amplification in a PC-TFET
H	V	Hysteresis window in VO_2 switch IV characteristic
IL	dB	Insertion loss
I_{ACT}	A	Current value before IMT in 2-terminal switch
I_{DS}	A	Current flowing between drain and source terminals in a FET.
I_{OFF}	A	I_{DS} current value at $V_{GS} = 0V$ in a FET
I_{ON}	A	Current value after IMT in 2-terminal switch
I_P	A	Probing current in resistivity measurement.
I_d	A	Current flowing in the drain terminal in a FET.
I_g	A	Current flowing in the gate terminal in a FET.
I	A	Current
$L0$	mm	Length of LRL reference line
L_n	mm	Length of LRL line n
L_{VO_2}	m	Length of the VO_2 switch
L	H	Inductance
M_E	-	Electrical strength of the switch
N_D	cm ⁻³	Drain doping in TFET
N_S	cm ⁻³	Source doping in TFET

List of symbols

Symbol	Unit	Description
P_{ACT}	W	Switching power to trigger IMT in 2-terminal switch
Q	J	Heat
RL	dB	Reflection loss
R_C	Ω	Resistance of the crystal film
R_L	Ω	Gate load resistor in gate PC-TFET
R_L	Ω	Loss resistance
$R_{C_{IMT}}$	Ω	Resistance of the VO ₂ crystal before the IMT
R_S	Ω	Resistance in series of the VO ₂ switch
$R_{VO_2 OFF}$	Ω	Resistance of the VO ₂ switch in insulating state
$R_{VO_2 ON}$	Ω	Resistance of the VO ₂ switch in conductive state
R_{VO_2}	Ω	Resistance of the VO ₂ switch
$SS_{PC-TFET}$	mV · dec ⁻¹	Subthreshold slope of a PC-TFET
SS_{TFET}	mV · dec ⁻¹	Subthreshold slope of a TFET
SS_{VO_2}	mV · dec ⁻¹	IMT current jump divided by voltage step in a VO ₂ switch IV characteristic
SS	mV · dec ⁻¹	Subthreshold slope
S_{11}	dB	S-parameter 11
S_{21}	dB	S-parameter 21
TR	-	Tuning range
T_C	K	VO ₂ crystal temperature
T_{IMT}	°C	Insulator to metal transition temperature
T_{MIT}	°C	Metal to insulator transition temperature
T_{ox}	F	Oxide thickness in TFET
T	°C	Temperature
V_C	V	Voltage drop across crystal film
V_{23}	V	Voltage drop between terminals 2 and 3 in 4-point in resistivity measurement.
V_{ACT}	V	Voltage needed to trigger IMT in 2-terminal switch
V_{DSINT}	V	Voltage drop between drain and source internal terminals in a PC-FET.
V_{DS}	V	Voltage drop between drain and source terminals in a FET.
V_{GSACT}	V	Voltage drop between gate and source terminals that triggers the IMT in a PC-FET.
V_{GSINT}	V	Voltage drop between gate and source internal terminals in a PC-FET.
V_{GS}	V	Voltage drop between gate and source terminals in a FET.
V_{IMT}	V	Voltage needed to trigger IMT
V_{INT}	V	Voltage drop on the VO ₂ 2-terminal switch
V_{th}	V	Threshold voltage in a FET.
V	V	Voltage
W_{VO_2}	m	Width of the VO ₂ switch
Y_{11}		Admittance parameter 11
Y_{21}		Admittance parameter 21

Symbol	Unit	Description
ΔL	mm	Line length difference with respect to reference in LRL
ΔT	K	Hysteresis window width in VO ₂ resistivity versus temperature curve
Δ_G	meV	Band-gap reduction
Δf	Hz	Bandwidth at -3 dB (FWHM)
Φ_m	eV	Gate metal workfunction
λ_0	m	Free space wavelength at the central frequency in a tunable filter
λ	m	Wavelength of X-ray source
θ	°	Incident angle of the X-ray
ε_r	-	Relative dielectric permittivity
ε	F · m ⁻¹	Material dielectric constant
a_H	m	Bohr radius
a	m	Filter length
b	m	Filter width
c	-	Coefficient relating M_E and M_T
d	m	Position of the VO ₂ switch along the spiral in CPW DGS filter
d	m	Distance between atomic planes in a crystal
e	C	Electron charge
f_r	Hz	Resonant frequency
f_0	Hz	Resonant frequency in a tunable filter
f_{max}	Hz	Maximum value of the resonant frequency in a tunable filter
f_{min}	Hz	Minimum value of the resonant frequency in a tunable filter
f	Hz	Frequency
g	m	CPW ground spacing
k	W · K ⁻¹	Effective thermal conductance
m^*	Kg	Carrier effective mass
m	-	Body factor
n_C	m ⁻³	Mott transition critical carrier density
n	mV · dec ⁻¹	n-factor
n	-	Integer
s	m	Spiral spacing in CPW DGS filter and inductor.
t	m	Spiral width in CPW DGS filter and inductor
t	m	Thickness of VO ₂ film
v_{ph}	m · s ⁻¹	Phase velocity
w	m	CPW signal width
x_{max}	-	Maximum value of property x
x_{min}	-	Minimum value of property x
x	-	Value of property x
Ψ_S	V	Surface potential in a FET.

List of symbols

Symbol	Unit	Description
D	-	Drain node in FET
G	-	Gate node in FET
G _{INT}	-	Internal gate node in PC-FET
S	-	Source node in FET
S _{INT}	-	Internal source node in PC-FET

List of units

Name	Symbol	SI units	Quantity
Ampere	A	A	Electric current
Bar	bar	10^5 Pa	Pressure
Coulomb	C	$A \cdot s$	Electric charge
Decade	dec	-	Interval $[10^r, 10^{r+1})$, $r \in \mathbb{R}$
Decibel	dB	-	Unit for ratio between two power values in logarithmic scale.
Degree	°	$180^{-1} \pi$ rad	Angle
Degree Celsius	°C	K ($T_{\text{°C}} = T_{\text{K}} - 273.15$)	Temperature
Electronvolt	eV	$1.6022 \cdot 10^{-19}$ J	Energy
Farad	F	$s^4 \cdot A^2 \cdot m^{-2} \cdot kg^{-1}$	Electrical capacitance
Henry	H	$Kg \cdot m^2 \cdot s^{-2} \cdot A^{-2}$	Electrical inductance
Hertz	Hz	s^{-1}	Frequency
Joule	J	$Kg \cdot m^2 \cdot s^{-2}$	Energy
Kelvin	K	K	Temperature
Kilogram	Kg	Kg	Mass
Meter	m	m	Length
Minute	min	60 s	Time
Ohm	Ω	$kg \cdot m^2 \cdot s^{-3} \cdot A^{-2}$	Electrical resistance
Second	s	s	Time

List of units

Name	Symbol	SI units	Quantity
Standard cubic centimeters per minute	sccm	$0.001689 \text{ Pa} \cdot \text{m}^3 \cdot \text{s}^{-1}$	Flow
Volt	V	$\text{kg} \cdot \text{m}^2 \cdot \text{s}^{-3} \cdot \text{A}^{-1}$	Electric potential difference
Watt	W	$\text{Kg} \cdot \text{m}^2 \cdot \text{s}^{-3}$	Power

List of elements and materials

Ag	Silver
Al	Aluminium
Al₂O₃	Aluminium oxide
Ar	Argon
Au	Gold
BP	Black Phosphorous
C₄F₈	Octafluorocyclobutane
Cr	Chromium
Cu_xO	Copper oxide
Ga	Gallium
GaAs	Gallium Arsenide
GaAs	Gallium arsenide
GaSb	Gallium Antimonide
Ge	Germanium
GeSn	Germanium Tin
H₂	Hydrogen
He	Helium
HfO₂	Hafnium oxide
HfSe₂	Hafnium Diselenide
In	Indium
InAs	Indium Arsenide
InP	Indium Phosphide
ITO	Indium tin oxide
MMA	Methyl methacrylate
MoS₂	Molybdenum Disulphide
Ni	Nichel
nLOF	Thermally stable negative resist

List of elements and materials

O₂	Oxygen
Pd	Palladium
PDMS	Polydimethylsiloxane
PMMA	Poly(methyl methacrylate)
Pt	Platinum
Si	Silicon
SiGe	Silicon Germanium
SiO₂	Silicon oxide
SnSe₂	Tin Diselenide
Ti	Titanium
Ti₂O₃	Titanium sesquioxide
TiN	Titanium nitride
TiO₂	Titanium dioxide
V	Vanadium
V₂O₃	Vanadium sesquioxide
V₂O₅	Vanadium pentoxide
VO	Vanadium monoxide
VO(OC₃H₇)₃	Vanadyl tri-isopropoxide
VO₂	Vanadium dioxide
VOCl₃	Vanadium oxytrichloride
W	Tungsten
WSe₂	Tungsten Diselenide
Zn	Zinc
ZnO	Zinc oxide

1 | Introduction

The invention of the transistor in 1947 is a fundamental historic moment, probably unparalleled in terms of its influence on our quality and style of life. In few decades, this electronic device completely changed the everyday habits of most of mankind, launching an unprecedented era of technological progress known as Information Revolution. Figure 1.1 shows the first transistor (1947) back to back with the advanced 10 nm node commercialized by Intel in 2018 [1, 2]. Only 71 years separate these two devices, during which the transistor completely transformed our world.

The semiconductor industry has provided a previously unthinkable computing power, that in turn enabled game-changing discoveries in practically every science field while contributing to create entirely new areas of scientific inquiry. With the widespread diffusion of internet, the planet has dramatically shrunk, making available an enormous amount of information to members of any background and social class. Moreover, the technical skills developed to continuously improve the performance of electronic devices benefited incredibly very different engineering applications.

Alongside facilitating a drastic improvements of human capabilities to understand, control and live our universe, the technological revolution initiated by the transistor introduced new enormous moral, social and technical challenges.

1.1 Brief CMOS history and More-Moore approach

Integrated circuits (ICs), since their invention in the early 50s of 20th century, have determined an unprecedented technological revolution in our society, contributing to completely alter our everyday life [3]. The first transistor invented by Shockley, Bardeen and Brattain was a point contact transistor, replaced shortly after by the bipolar junction transistor (BJT). BJTs are three terminal devices, where the current flowing between the emitter and collector contacts is controlled by the bias and current of the third terminal, the transistor base. A fundamental step in the transistor ongoing evolution was the Complementary Metal-Oxide-Semiconductor (CMOS) technology, that opened the doors to the digital era. By packing together two unipolar, complementary devices, a nMOSFET (Metal-Oxide-Semiconductor Field Effect Transistor) and a pMOSFET, CMOS technology allowed to drastically reduce the cost and dramatically improve the performance of the fundamental digital computing blocks.

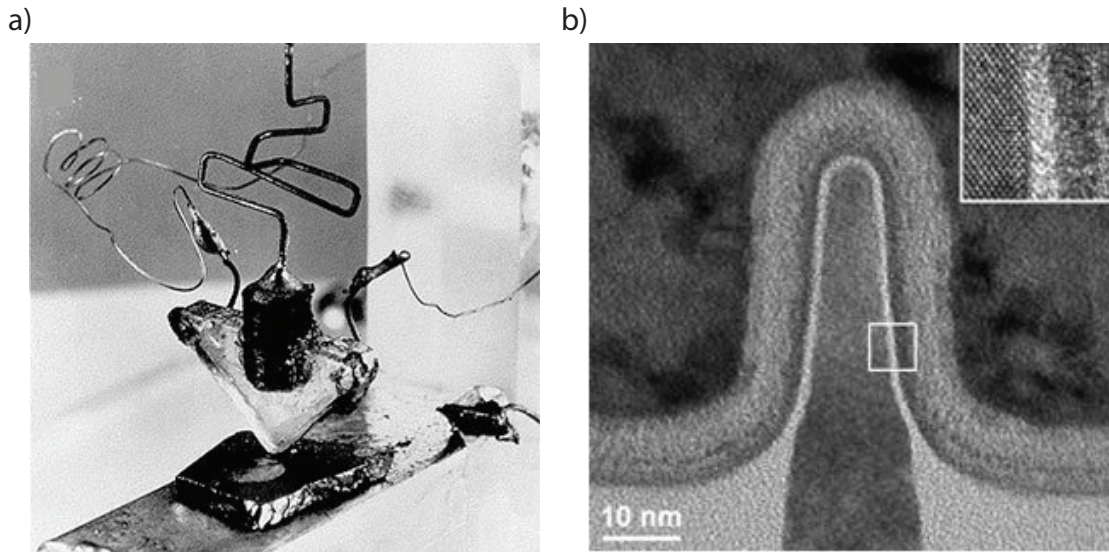


Figure 1.1: a) First transistor realized in 1947 by W. Shockley, J. Bardeen and W. Brattain in 1947. b) Advanced 10 nm FinFET node produced by Intel in 2018. Adapted from [1, 2].

The key advantage of MOSFETs over BJTs is the almost zero static power consumption granted by the introduction of the gate dielectric [4]. The gate contact, contrary to the BJT base, controls the conduction of the semiconductor thanks to only its bias, providing a practically infinite input impedance and an almost zero static gate current. Therefore, the static power consumption of a MOSFET is considerably lower with respect to a bipolar transistor. The introduction of MOSFETs enabled a massive increase of the transistor area density and consequently of the computation capability while maintaining reasonable power requirements.

Since the demonstration of the potential and interest of CMOS, the semiconductor industry focused most of its resources in the race for scaling transistors physical dimensions. Indeed, decreasing the transistor size allows to increase the device density (i.e. decrease the required area for fixed transistor count) and improve the performance, by reducing the capacitances in the device thus enhancing the maximum operating frequency. Gordon Moore, the co-founder of Fairchild Semiconductor and Intel, observed and predicted in 1965 that the number of transistors in a dense integrated circuit doubles approximately every two years, as shown in Figure 1.2 where the exponential growth projection is directly compared to the transistor count of commercial microprocessors. This empirical observation is well known under the name of *Moore's law*, and it has been closely respected for several decades [5].

It is possible to distinguish two main periods in the IC scaling race. Silicon (Si) is not by chance the elective semiconductor for practically all the IC products (important exceptions do subsist). It is a semiconductor incredibly abundant in nature, it can be refined to extremely high levels of purity and it exhibits excellent conduction properties. Moreover, if exposed to air, bulk silicon self-passivates by growing few nanometers of self-limiting silicon dioxide (SiO_2). The possibility of growing easily a stable oxide on Si surface proved to be a fundamental advantage for the CMOS technology, that requires a high quality dielectric to electrostatically control

1.1. Brief CMOS history and More-Moore approach

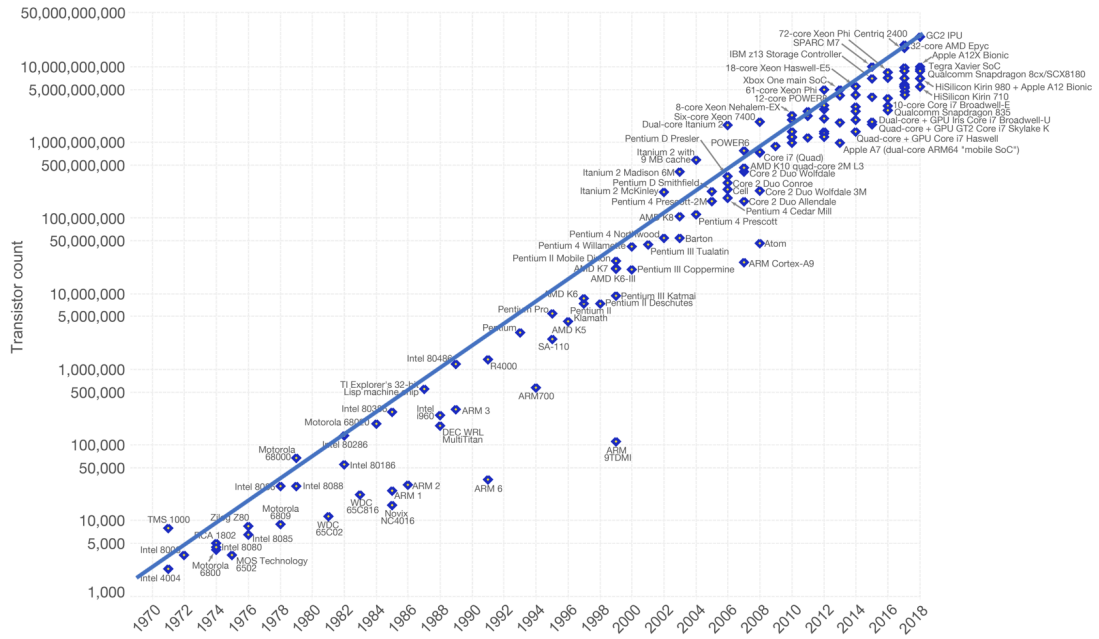


Figure 1.2: Comparison of the Moore's law prediction on the transistor count and data obtained from manufactured microprocessors. Adapted from [6].

the semiconductive channel. The development of precise doping techniques (diffusion and later implantation) represented the last ingredients required to kick off the so called "happy scaling" era. Following a set of design principles known as Dennard's rules [7], the industry was able to drastically decrease transistor dimensions by relying on a purely geometrical scaling of the precedent generation fabrication parameters, perfectly following Moore's prediction. Figure 1.3 shows the evolution of the gate length over the years, compared with the extrapolation derived from Dennard's law [8, 9]. Proceeding along the scaling roadmap, material and technological boosters needed to be introduced so to improve the transistors performance and to overcome limitations not observed before in large devices. Examples of the new materials introduced in advanced CMOS nodes include high-k dielectrics, metallic gate, copper interconnections and SiGe or strain engineered channels. Moreover, in aggressively scaled nodes, parasitic effects related to contacts and interconnections became more and more significant with respect to the shrinking channel contributions [10, 11]. Before 2010, a saturation of the gate length was observed and the continuous decrease of transistor dimensions required drastic architectural changes. In order to mitigate the non-idealities plaguing small transistors (short channel effect, drain induced barrier lowering, etc.), new architectures and geometries have been proposed and implemented, such as Intel FinFET and the SOI technology [9, 12–14]. Currently, the 14 nm node technology is mastered by the major fab companies in the world. Industrial demos and first products have already been presented for 10 and 7 nm nodes, while researchers demonstrated 5 nm FETs [15].

This approach to the future of the semiconductor industry is known as "More-Moore". The technical challenges related to these extremely scaled nodes are enormous, requiring a complete revolution of the lithographic tools. Moreover, even though theoretically feasible, deep sub 10 nm technologies may prove to be not economically viable, both in terms of infrastruc-

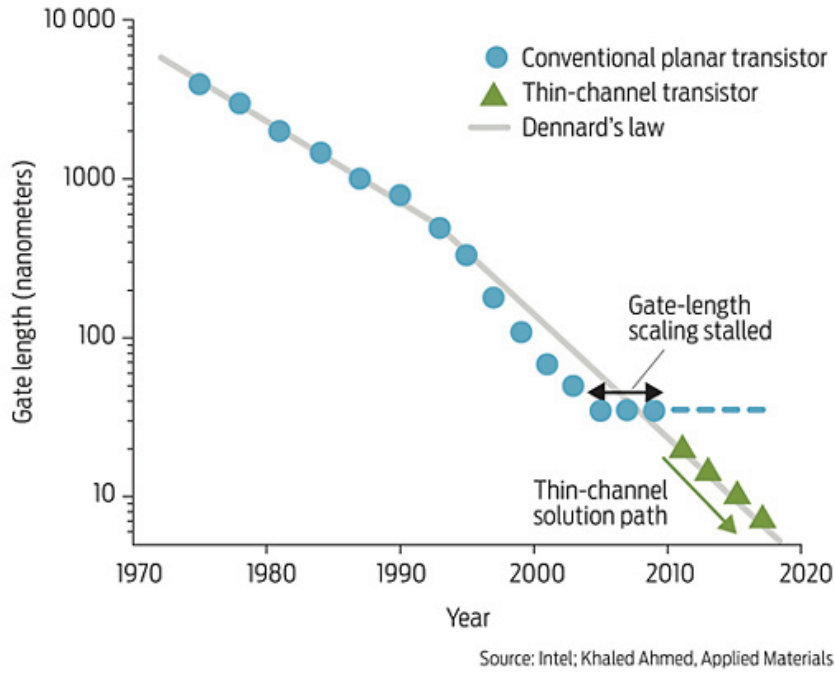


Figure 1.3: Scaling of the gate length following the predictions of Dennard's law. The scaling stalled before 2010. Adapted from [9].

ture investment required for the development and concerns related to the device reliability and reproducibility [16].

A second fundamental challenge for More Moore devices is related to the power density in the fabricated chips. With the scaling of the transistor dimension, the device area scales quadratically. If the power supply cannot be decreased accordingly, the power density in the chip is bound to increase in every new technological node. Figure 1.4 shows the evolution of the power density along the years [17]. After 2000, the values skyrocketed, overcoming the power density achieved in a nuclear reactor! Even revolutionizing the cooling strategies, such a power density surge is incompatible with the strict reliability, aging and safety requirements of most applications. Therefore, we recently entered a sort of "dark silicon" era: it is possible to pack more and more devices in the same chip area, but we cannot afford to turn them on all at the same time. Similarly to human brains, current and future chips will exploit only a percentage of the transistors at a given moment, so to maintain the total power density within acceptable limits. The development of optimized computing algorithms is therefore becoming more and more vital.

At last, CMOS technology is constrained by a fundamental limit, that ultimately contributed to the end of the "happy scaling" era and the stalling of the power supply scaling. MOSFET carrier injection is based on the thermionic effect, i.e. "hot", high energy carriers are jumping over a potential barrier whose height is modulated by the gate of the device. The capability of translating a variation of the gate bias in a variation of the output current is the very essence of field-effect devices working principle. A quantitative parameter used to express the quality of

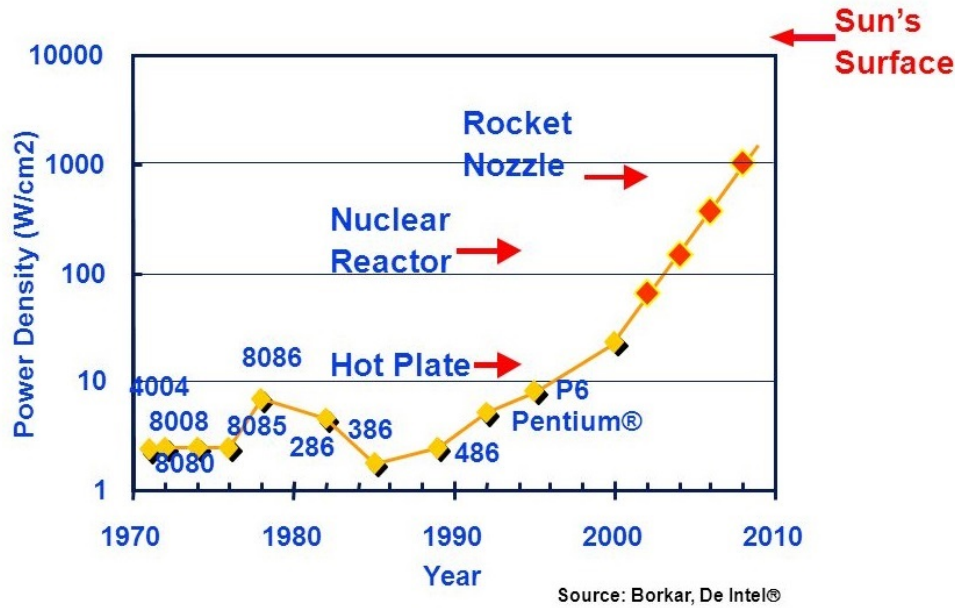


Figure 1.4: Evolution of the power density in microchips from 1970 to 2010. The power density values achieved in other physical environments are reported for comparison. Adapted from [17]

such gate control on the channel conductance is the so called subthreshold slope (SS), defined as the inverse slope of the logarithm of the drain current with respect to the gate bias. In CMOS devices, SS is physically limited to be at best equal to 60 mV/dec at room temperature (translates to: a variation of at least 60 mV on the gate bias is required to see a variation of one order of magnitude of the output current) [18]. Even assuming ideal devices, since the minimum SS is fixed, the scaling down of the transistor size and its power supply will result in an increase of the OFF state power consumption. Recently, the standby power is becoming comparable to the dynamic power consumption, as shown in Figure 1.5a [9]. As a result, the transistor threshold voltage and consequently the power supply cannot be scaled excessively so to limit the unacceptable surge in the leakage power.

Figure 1.5b is a qualitative representation of the current challenges in electronics design related to the power consumption of the fabricated chips. The power wall represents the maximum power per processor core that can be safely handled without damages to the devices. In order to overcome this limitation while continuing to improve the computing performance, designers exploit multiple cores so to split the tasks and decrease the resulting power density per core. Parallel computations have been demonstrated to be an efficient strategy, but the increase of cores number inevitably involves the increase of the system complexity. It is then possible to envision a second wall, a "parallelism" limit to the complexity of the processor architecture above which the addition of other cores is no longer convenient or feasible.

In order to solve or at least mitigate the power crisis in CMOS technology and to pursue the

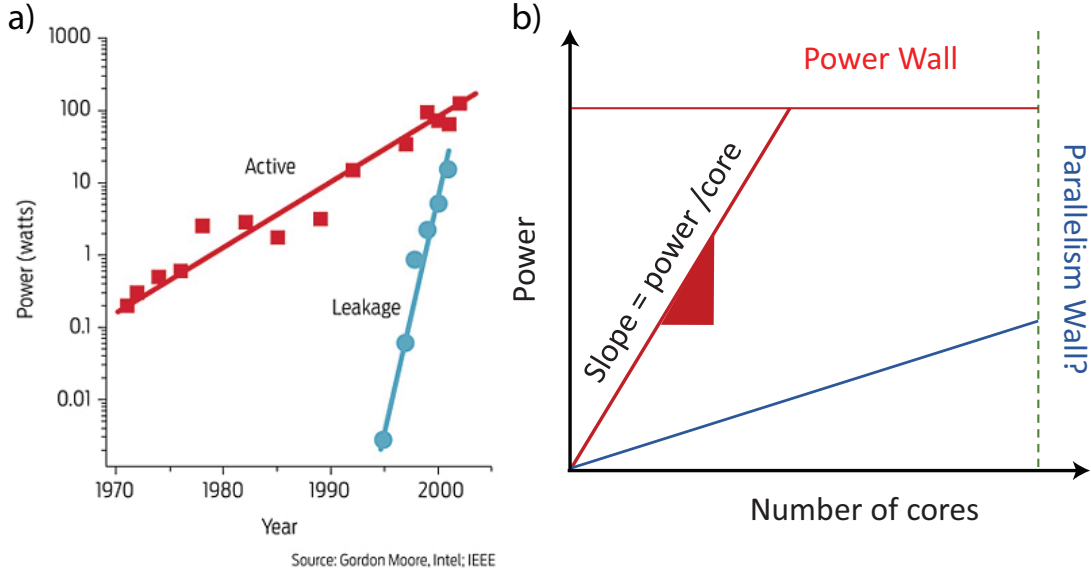


Figure 1.5: a) Evolution of the active and leakage power consumption over the scaling timeline. Adapted from [9] b) Design limiting walls, power density limit and number of cores limit resulting from the excessive system complexity.

power supply scaling, several new devices, collectively labeled under the More-Than-Moore name, have been proposed and investigated

1.2 More-Than-Moore devices

The More-Than-Moore landscape is definitely more complex and variegated than the More-Moore approach, despite being clearly further from commercial applications [19]. The common denominator among the different possibilities that have been explored is the replacement or *enhancement* of the thermionic carrier injection mechanism, so to be able to overcome the 60 mV/dec barrier and enable aggressive supply voltage scaling. In order to group the More-Than-Moore devices in different families, it is useful to start from the mathematical expression of the subthreshold slope in a generic field-effect device:

$$SS = \frac{\partial V_G}{\partial \log I_D} = \frac{\partial V_G}{\partial \log \Psi_S} \frac{\partial \Psi_S}{\partial \log I_D} = m \cdot n \quad (1.1)$$

Here m is referred to as body factor and it is an expression of the capacitive gate coupling efficiency, while n is the device ideality factor and is a direct consequence of the carrier injection mechanism exploited in the transistor [18]. In MOSFET devices, the thermionic injection mechanism at the base of the conduction physically limits the minimum values achievable for these

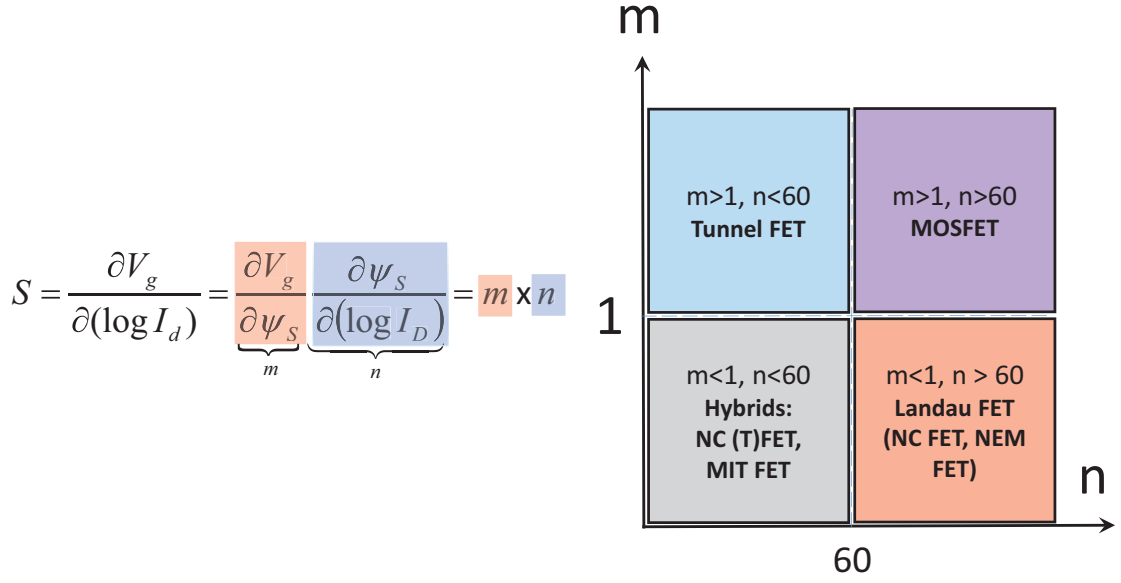


Figure 1.6: Subthreshold slope expression and map of FET design space.

factor to 1 and 60 mV/dec respectively. Therefore, the minimum value of the subthreshold slope of an ideal MOSFET is limited to 60 mV/dec at room temperature. By considering these two parameters as independent variables, we can divide the electronics device design space in four regions, as shown in Figure 1.6.

It is worth to discuss and provide a few examples of characteristic devices for each of the regions that go beyond the MOSFET space.

1.2.1 Landau FET

Devices exhibiting sub unity body factor ($m < 1$) but still exploiting thermionic injection are known as Landau FETs. The key to break the 60 mV/dec barrier in this case relies on the change of the capacitive coupling mechanism between gate and semiconductive channel. Two notable categories of the Landau FET family are the nano electromechanical (NEM) FET and the negative capacitance FET.

In a NEM FET, the gate is physically separated from the dielectric and the channel. By applying a voltage larger than the pull-in voltage of the mechanically suspended gate, the electrode is brought in direct contact with the dielectric deposited on the channel, thus suddenly enhancing the capacitive coupling and therefore the drain current. Figure 1.7a shows an example of suspended gate FET, together with a SEM image of a fabricated device [20]. The structure is quite similar to a conventional MOSFET, with the introduction of an air gap between gate contact and channel dielectric, usually obtained by etching off a sacrificial layer. The single sweep transfer characteristic of this device is shown in Figure 1.7c. When the gate bias overcomes the pull-in threshold, the electrode collapses on the channel resulting in the increase of the output current. It

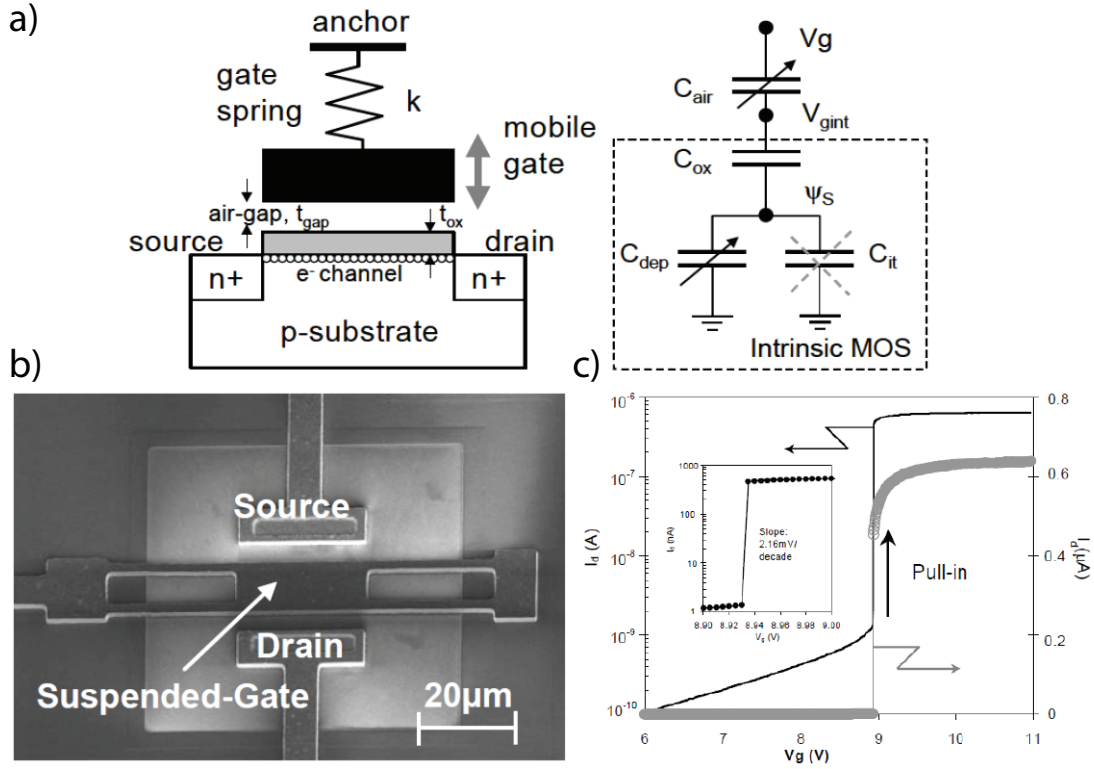


Figure 1.7: a) Schematic and equivalent capacitive circuit of a NEM FET. b) SEM image of a suspended gate FET, with the gate contact physically separated from the semiconducting channel. c) Transfer characteristic showing the sharp ON-OFF transition. Adapted from [20].

is important to notice the high voltage bias required to induce the pull-in of the gate and therefore the OFF-ON transition.

NEM FETs exhibit an almost zero subthreshold slope and a practically null gate leakage current in OFF state, but their use in real applications is strongly limited by the large hysteresis determined by the intrinsic and unavoidable mismatch between pull-in and pull-out voltages, the reduced maximum switching frequency and the relatively large power supply required. Moreover, the reliable scaling of such mechanical structures to dimensions comparable to CMOS circuitry presents noticeable challenges.

Negative capacitance FETs relies instead on a more conventional transistor architecture, to which it is added a ferroelectric dielectric layer. Figure 1.8 offers a brief overview of NC FET working principle, starting from the device schematic and capacitive equivalent circuit. The energy vs polarization curve for a ferroelectric materials is shown in Figure 1.8b. The presence of two minima in the energy landscape determines a bistable behavior, with a transition region where the equivalent capacitance of the ferroelectric layer is negative. By exploiting this region of biasing it is possible to achieve a body factor smaller than one. However, ferroelectrics introduce a considerable unwanted hysteresis in the device transfer characteristic [21] because of the instability of the energy vs polarization curve. In order to stabilize the system, it is possible to

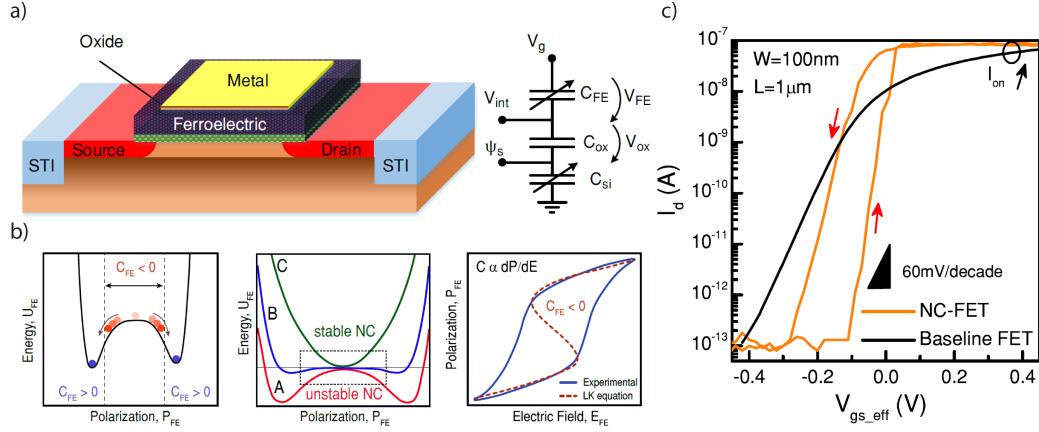


Figure 1.8: a) Schematic and equivalent capacitive circuit of a negative capacitance FET. b) Polarization curves, showing the bistable energy landscape enabling the negative capacitance phenomena in ferroelectrics, the stabilized NC and the polarization vs electric field graph. c) Transfer characteristic of a NC FET directly compared to the internal, baseline FET. Adapted from [23].

add a conventional dielectric layer to the gate stack so to introduce a series capacitance. If properly balanced, this can result in a transfer characteristic maintaining the steep subthreshold slope while mitigating the hysteresis increase, as shown in Figure 1.8c.

NC FETs have very recently attracted a huge research interest because of the small subthreshold slope achievable combined with the possibility of stabilizing the ferroelectric FET with a linear dielectric so to achieve hysteresis free behavior. At the same time, promising reports of ferroelectricity in doped and strained high-k dielectrics, such as silver or gadolinium doped hafnium oxide ($Ag:HfO_2$, $Gd:HfO_2$) make it possible to envision the realization of integrated negative capacitance CMOS devices. More and more, NC is seen as a promising technology booster for both CMOS and other More-than-Moore devices [22].

1.2.2 Tunnel FET

The $m > 1$, $n < 60$ mV/dec region is the undisputed realm of the Tunnel FET (TFET). To achieve subthermal subthreshold slope while maintaining a body factor larger than one, a change of injection mechanism is required. In TFETs, carriers are injected through a energy barrier rather than above it as in conventional MOSFETs based on thermionic injection. The steep subthreshold slope is indeed achieved by exploiting band to band tunneling from the source region of the device to the channel [18]. The typical silicon TFET architecture strongly resembles a MOSFET, but it requires an asymmetric doping so to obtain a p-i-n structure. The similarity with established CMOS devices is a key advantage of the TFET technology, that could be implemented alongside MOSFETs without the need for different fabrication tools or an excessive complexity increase

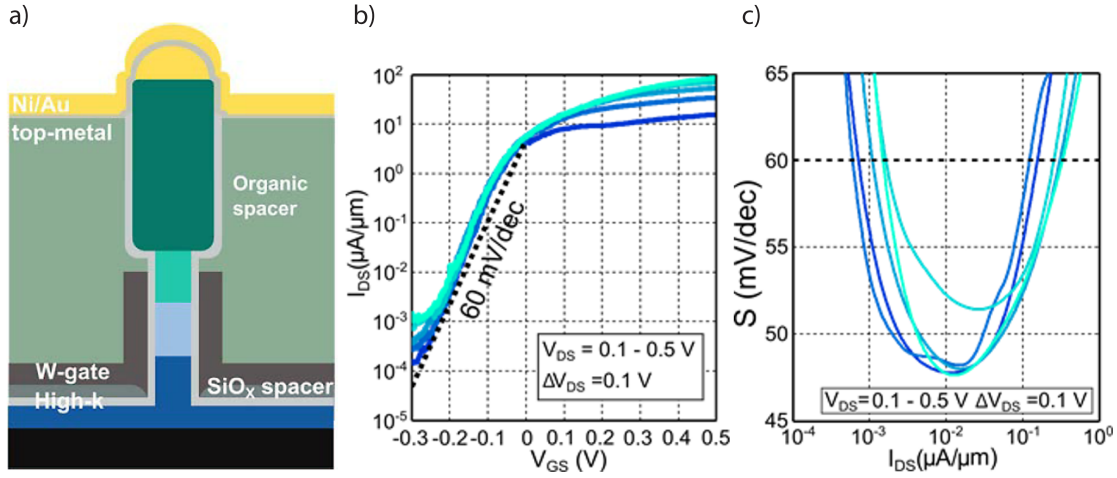


Figure 1.9: a) Schematic of the best experimental TFET, based on a InAs/GaAsSb/-GaSb vertical heterojunction. b) Transfer characteristic of the device for increasing values of the drain to source bias. c) Subthreshold slope as a function of the output current, showing subthermal swing over two orders of magnitude of I_D . Adapted from [24]

of the process flow. The fundamental advantage of TFET is the steep, temperature insensitive subthreshold slope, that allows it to outperform CMOS in the turn-on, low current region [18]. However, the very nature of the BTBT mechanism limits the maximum output current, so that typically TFETs have significantly smaller I_{ON} than MOSFETs with comparable structure.

Figure 1.8 shows the structure and the transfer characteristic of the best reported experimental TFET [24]. This device is based on a vertical InAs/GaAsSb/GaSb heterojunction and reaches subthermal SS over two orders of magnitude of the output current.

A second type of device able to reach the $n < 60$ mV/dec design space is the impact ionization MOSFET. In this case, the output current is obtained from the control of the avalanche breakdown of a gated p-n junction diode [25, 26]. Exploiting this principle, subthreshold slope values as low as 5 mV/dec have been demonstrated [25]. However, the avalanche mechanism determines the presence of a high density of high energy ("hot") carriers, that compromise the reliability of the device by accelerating both the dielectric and the channel aging [27].

1.2.3 Hybrid FET

Finally, the last part of our design space (Figure 1.6) is home to hybrids devices, that combine different strategies so to achieve both $m < 1$ and $n < 60$ mV/dec. Two of the most important families of devices in this area are NC TFETs and metal-insulator transition (MIT) FET.

Negative capacitance TFETs have a quite self-explanatory name: the basic idea is to exploit the negative capacitance as a technology booster for TFET devices, so to obtain an even steeper turn-on thanks to the sub-unity body factor [21].

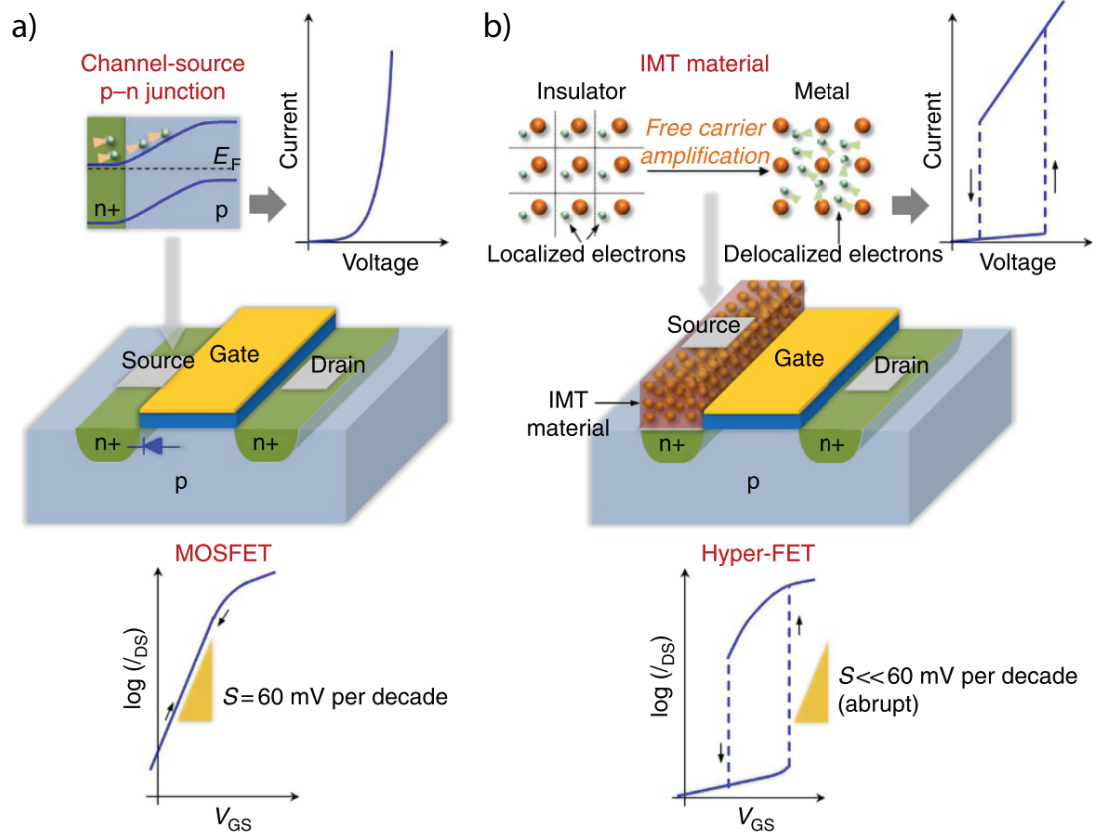


Figure 1.10: a) Schematic and qualitative characteristic of a MOSFET. b) Schematic and qualitative characteristic of a phase change FET realized by depositing a material exhibiting insulator to metal transition in series to the MOSFET source. Adapted from [28]

MIT FETs instead rely on the thermal or electrical induced insulator to metal transition observed in some functional oxides. Such phase transition is connected to the collapse of the electronic band gap of the oxide, and therefore with the sudden increase of the electronic concentration. MIT switches can be used in series to the gate or source of a FET so to achieve extremely steep but hysteretic output characteristic [28–30]. Figure 1.10 shows the structure of the first reported MIT FET, based on the addition of a functional oxides resistor exhibiting MIT in series to the source of a MOSFET device.

1.3 2D Materials to the rescue

Since the discovery and isolation of graphene in 2004, two dimensional materials have attracted an enormous research interest [31]. The expanded 2D material family covers basically all the interesting physical properties for electronics devices [32]. 2D metals, semi-metals, semiconductors and dielectrics have been isolated. Superconductivity and peculiar magnetic properties have as well recently been demonstrated [33, 34]. Moreover, the physical behavior of most of

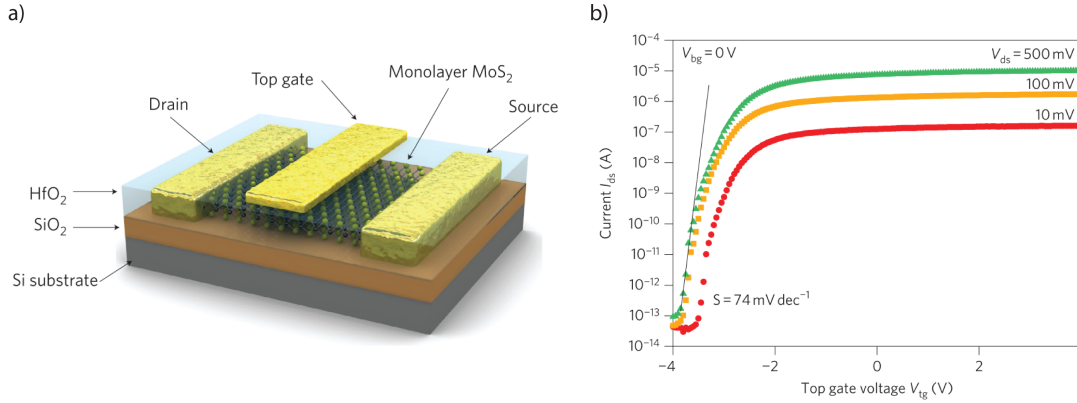


Figure 1.11: a) Schematic of a top gated monolayer MoS₂ FET with high-k dielectric. b) Transfer characteristic, showing a good value of the subthreshold slope. The MoS₂ FET works in depletion mode, i.e. negative bias on the top gate leads to the depletion of carriers in the channel. Adapted from [38]

these materials is strongly dependent on the number of layers present in the flake, so that their properties can be effectively tuned by controlling precisely the exfoliation or deposition procedure.

It is practically impossible to cite all the interesting applications of these materials across an ever growing range of research fields. Here, we are going to focus on 2D materials for FET and sensor devices. The most important features that make 2D materials promising for electronic applications can be summarize as follows:

- atomically thin channel, granting optimal gate control and reduced short-channel effects [35, 36];
- increased surface to volume ratio, enabling sensors with ultra high sensitivity [37];
- unique electronic properties [35, 38, 39];
- possibility of assembling complex, multi material heterojunctions [40];
- excellent mechanical properties, ideal for high strain applications [41];
- transferable at room temperature, compatible with back end of the line CMOS processes [42].

The first ingredient for a successful FET is a semiconducting channel with sufficiently large band gap. Therefore, despite being the first and arguably the most studied 2D material, graphene is not an ideal candidate, since it exhibits a null band gap. Even though a gap of up to few meV can be opened in graphene bands by exploiting ingenious fabrication or biasing strategies, such small values are not adequate to achieve reasonable ON/OFF current ratios in field effect devices meant to be operated at room temperature [35].

The transition metal dichalcogenide (TMDCs) family collects the most interesting candidates for the realization of both MOSFET and 2D based steep-slope FETs. Characterized by the MX₂

structure, where M is a transition metal atom and X a chalcogen atom, several of these materials present in the bulk form a finite indirect band gap. MoS_2 , WS_2 , MoSe_2 , WSe_2 and MoTe_2 for instance have a finite, relatively large band gap that transitions to a direct band gap when exfoliated down to the monolayer. MoS_2 in particular has been thoroughly investigated for the realization of depletion mode nFETs exhibiting excellent $I_{\text{ON}}/I_{\text{OFF}}$ ratio and nearly ideal subthreshold slope [38]. In [39], a ultrashort MoS_2 transistor gated using a SWCNT providing excellent electrostatic control has been recently demonstrated.

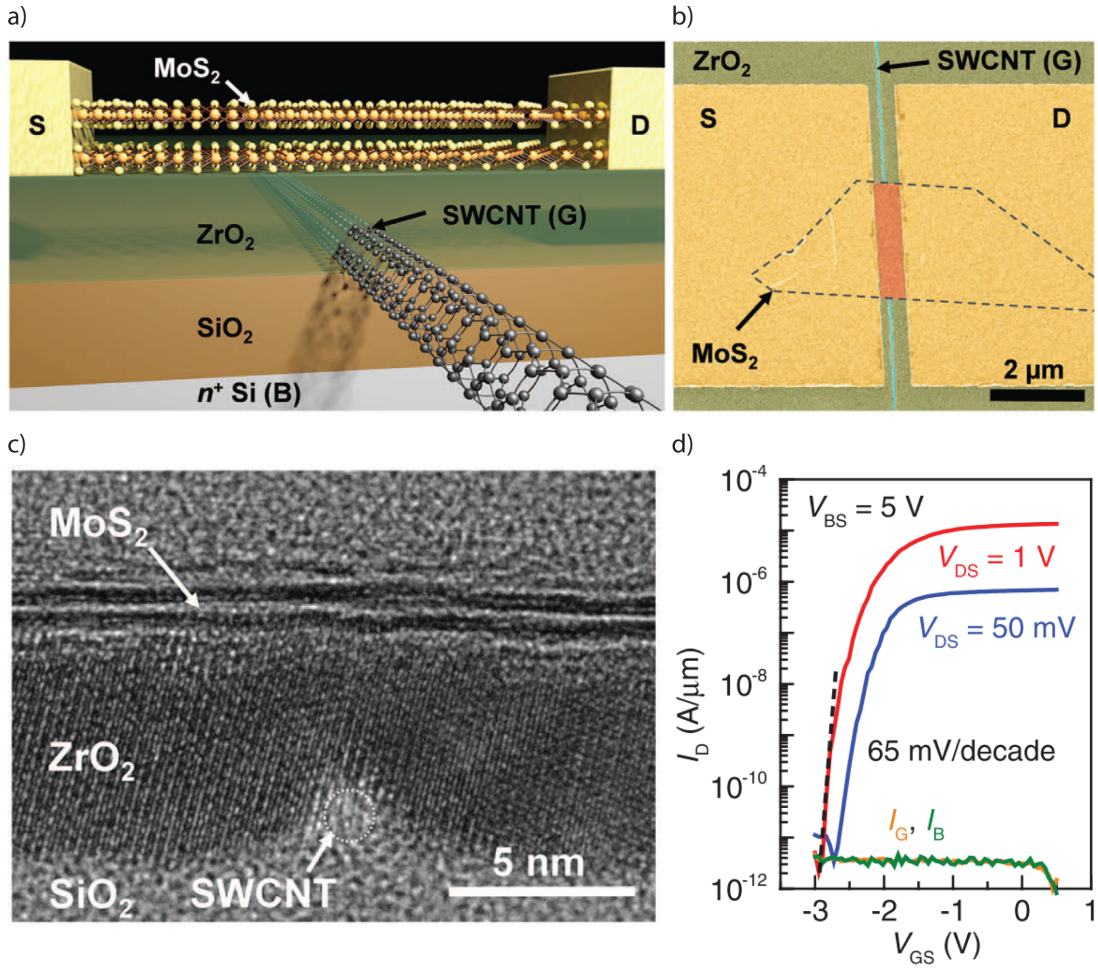


Figure 1.12: a) Schematic of a MoS_2 FET back-gated using a single wall carbon nanotube as gate contact. b) Colorized SEM image of the final device. c) TEM cross section showing the monolayer MoS_2 channel, the ZrO_2 dielectric and the contour of the SWCNT. d) Transfer characteristic of the device. Adapted from [39].

However, MoS_2 exhibits mainly n-type conduction, with only few reports of p type polarity obtained by either chemical doping, selection of peculiar substrates for the exfoliation or exotic metallic contacts [43–45]. WSe_2 on the contrary shows ambipolar conduction, and its polarity can be easily tuned exploiting clean and reversible electrostatic doping strategies [46]. Therefore, this material is the most promising for the realization of a true complementary 2D platform based on a single material system. The main limitation of the TMDC family remains the low carrier

mobility [32, 46, 47].

A more recent addition to the 2D material cosmos is black phosphorous (BP), a stable solid phosphorous elemental compound [48–50]. Similarly to TMDC, it has a finite band gap that however is direct even in its multilayer flakes. Moreover, pristine black phosphorous flakes show extremely high hole mobilities, overcoming one of the main limitations of TMDCs [48]. However, BP is not stable in ambient conditions, and it requires processing under inert atmosphere and a passivation layer is required to realize reliable electronic devices [51].

A fundamental advantage offered by 2D materials over conventional bulk semiconductors is the possibility of assembling mechanically a huge variety of heterostructures with no limitations concerning the lattice matching. Indeed, while conventional heterojunctions can be obtained only using materials with similar lattice constant so to avoid excessive strain or even non crystalline interfaces developed during the growth process, mechanical exfoliation and deterministic transfer open the door to clean, purely crystalline heterojunctions with atomically sharp interfaces [40]. A variety of 2D heterojunction systems with unique optical, electrical and quantum properties have been demonstrated in recent years [52–54].

However, 2D materials come with few important limitations:

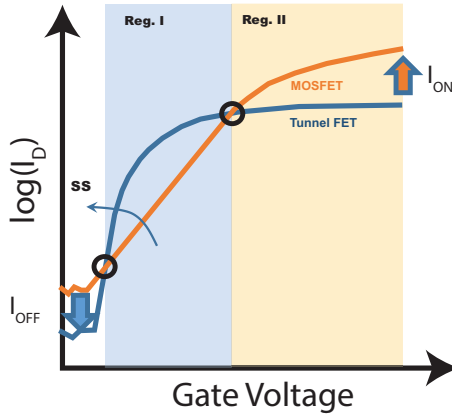
- no possibility for diffusion or implantation doping [55];
- high contact resistance deriving from van der Waals gap between metal and 2D material [56];
- Fermi level pinning at the metal-semiconductor interface, resulting in hard to control barriers for carriers injection in the 2D material [56];
- lower quality of epitaxial with respect to exfoliated flakes [57, 58];
- difficult scalability of the synthesis process.

Several challenges lie ahead on the path towards integration of 2D materials with CMOS for sensing or computing applications. However, the unique opportunities offered by the large 2D family are at the center of an incredible academic and industry research effort. The aim of this thesis is to propose device structures and fabrication approaches demonstrating the potential of this unique class of materials for both computing and sensing applications, in particular in a end-of-the scaling scenario.

1.4 Structure of the thesis

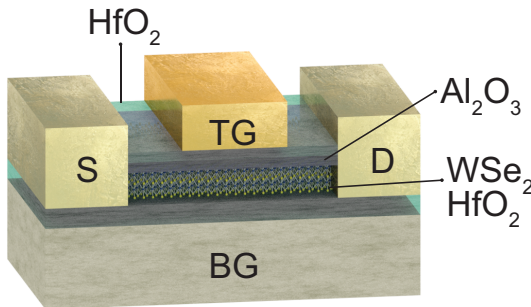
The thesis is structured as follows:

Chapter 2: Field effect devices: Metal-Oxide-Semiconductor FET and Tunnel FET



This chapter briefly discusses the physical principles at the base of both MOSFET and TFET operations. In particular, the impact of the different working principles on the performance of these two classes of devices as electronic switches in relation to the expected characteristic of an ideal switch is discussed. An overview of the current status of research on tunnel FETs is offered, with particular focus on the unique opportunities offered by recent research breakthroughs involving 2D materials and mixed dimensionality heterojunctions.

Chapter 3: 2D Planar Field effect transistors

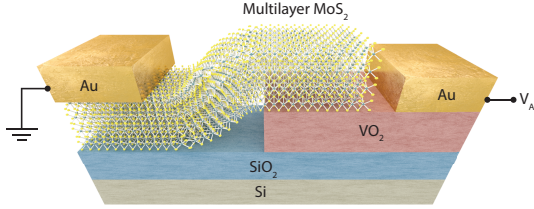


This chapter presents the fabrication and electrical characterization of planar 2D MOSFETs. The first part is dedicated to the process developed for the fabrication of top gated black phosphorous FETs with bottom contacts embedded in the silicon dioxide substrate on which the flakes are exfoliated. A detailed electrical characterization is provided, showing how the work-function engineering of the metallic contacts can be exploited so to achieve either p-type or n-type FETs. Then, a double gated WSe₂ structure for

high performance n-type FETs is presented. A detailed characterization of the impact of the two gates on the channel conduction and transfer characteristic hysteresis is provided. Finally, the frequency dependence of the device hysteresis is studied and discussed in comparison to alternative top gated devices reported in literature.

Chapter 1. Introduction

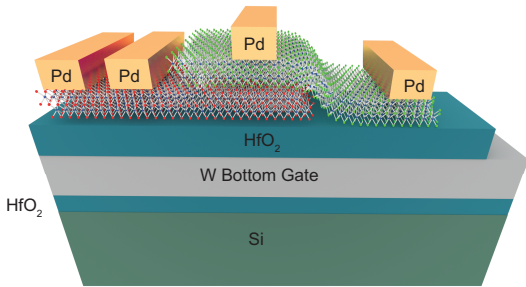
Chapter 4: 2D/3D Heterojunction devices



This chapter introduces the first heterojunction discussed in this thesis, based on a VO_2/MoS_2 structure. The peculiar properties of VO_2 are discussed, together with an overview of the deposition techniques and their impact on the metal to insulator transition characteristic exhibited by this functional oxide. Then, two terminal devices based on the proposed heterojunction are characterized, showing how it is possible to achieve diodes with good rectification

ratio. The characteristic of a photodiode based on the VO_2/MoS_2 heterojunction is presented together with a detailed experimental study of the temperature effect on its performance. Finally, three terminal devices based on the deposition of a high-k dielectric and a top gate contact on the MoS_2 flake are described. The gate bias is able to effectively modulate the diode rectification ratio. Moreover, the transfer characteristic shows excellent subthreshold slope, showing the possibility of obtaining high quality gated VO_2/MoS_2 heterojunctions that can lead to true VO_2 based field-effect devices.

Chapter 5: 2D/2D Heterojunction devices



This chapter presents the fabrication and characterization of a 2D/2D Tunnel FET based on a $\text{WSe}_2/\text{SnSe}_2$ heterojunction. A rationale about the choice of a suitable couple of 2D materials is provided and corroborated by DFT simulations of the expected band alignment. A detailed description of the developed fabrication process is presented, followed by an in depth electrical characterization. In particular, a one to one comparison between MOSFET and TFET devices

built on the very same flakes is carried on so to better benchmark the heterojunction device and provide the relevant figures of merit. Finally, a new device combining MOSFET and TFET strong assets, named Dual Transport Steep Slope FET, is proposed and demonstrated.

Chapter 6: Conclusions and perspectives

The last chapter summarizes the main contributions of the thesis and both the natural development of the research activity here described and the longer term perspectives of 2D materials for electronic devices.

2 | Field effect devices: Metal-Oxide-Semiconductor FET and Tunnel FET

This chapter focuses on the qualitative discussion of the working principle of both MOSFET and TFET. The importance of the subthreshold slope as fundamental parameter to compare electronic switches for digital applications is presented in detail. An overview of the current state of the art in both 3D and 2D TFETs is presented. Finally, the challenges and opportunities offered by 2D heterojunction devices are introduced.

2.1 Metal-Oxide-Semiconductor FET

The Metal-Oxide-Semiconductor (MOS) field effect transistor is the fundamental device behind the Information era technological revolution. The transistor effect is obtained in its structure by modulating the conductivity of a semiconducting channel comprised within the source and drain contacts exploiting a third terminal labeled as gate. The gate electrode and the MOSFET channel are physically separated by a dielectric layer, responsible for the introduction of a capacitive coupling for the transfer of the gate bias to the channel electric field. The gate dielectric provides a high input impedance, that enables both a near zero gate static power consumption and an easy cascading of logic gates.

Figure 2.1a shows the schematic structure of an enhancement mode bulk planar nMOSFET. Source and drain contacts are defined by n^+ doped pockets in the p-doped silicon substrate. The channel, i.e. the silicon region separating source and drain, is electrostatically controlled by the gate contact deposited on a thin dielectric layer. In the OFF state, with V_{DS} different from zero and null gate bias, the only contributions to the drain current come from the gate and source/drain junctions leakage currents. By increasing the gate bias, the density of electrons in the channel is gradually enhanced until the inversion point is reached, corresponding to an electron density larger than the hole one. The channel resistance is in this case much smaller, resulting in a high drain current. The MOSFET can be seen as a gate modulated non linear resistor.

Chapter 2. Field effect devices: Metal-Oxide-Semiconductor FET and Tunnel FET

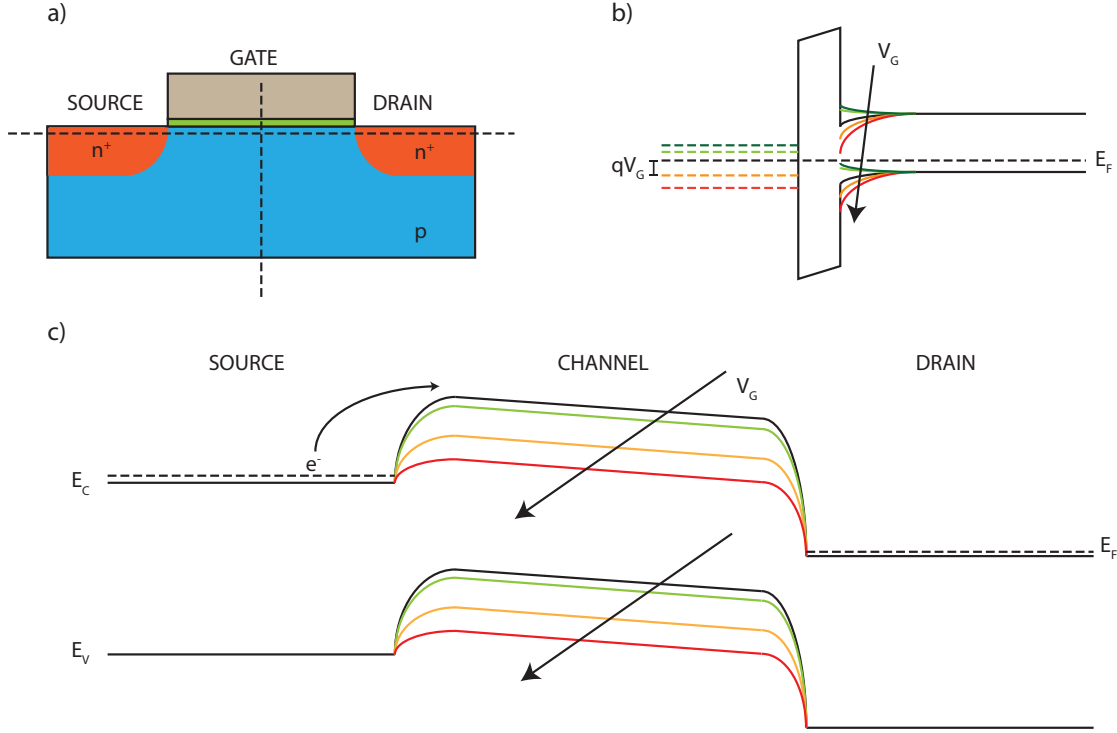


Figure 2.1: a) Schematic of a planar bulk nMOSFET, with the highlighted three contacts. b) Qualitative band diagram along the vertical cutline with the emphasized impact of gate bias on the channel bands. c) Qualitative band diagram along the channel plane of the MOSFET, showing how the gate bias can modulate the barrier for thermionic injection of electrons from source to channel conduction band.

In order to acquire a deeper understanding of the physical mechanisms at the base of the MOSFET working principle, it is important to consider the qualitative band diagrams along the two fundamental axis of the device, drawn in Figure 2.1a. Figure 2.1b shows the band diagram moving from the gate metal to the silicon channel along a first cutline perpendicular to the substrate. For zero bias applied to the gate, the Fermi level in the gate and the silicon channel is aligned. A positive V_G results in a downward shift of the silicon bands at the channel-dielectric interface. Therefore, the conduction band approaches the Fermi level, i.e. the electron density in the channel increases. The inversion point is reached when the minority and majority carriers concentration is equal, and the gate voltage required to reach this condition is known as threshold voltage ($V_{th,inv}$). Finally, for $V_G > V_{th}$, the electron density is larger than the hole one, determining the onset of the *strong inversion* regime and a low resistance between source and drain. Conversely, for negative gate biases, the silicon bands are bent upward, resulting in hole *accumulation* in the channel valence band and high channel resistance.

It is important to take into account the effect of both gate and drain to source biases. The qualitative band diagram along the device channel for $V_{DS} > 0$ V is drawn in Figure 2.1c. The positive drain voltage determines a misalignment of the Fermi levels in the source and drain of the MOSFET. Therefore, electrons tend to migrate from the source conduction band to the drain one. However, with zero or negative bias applied to the gate, electrons meet a large energy barrier

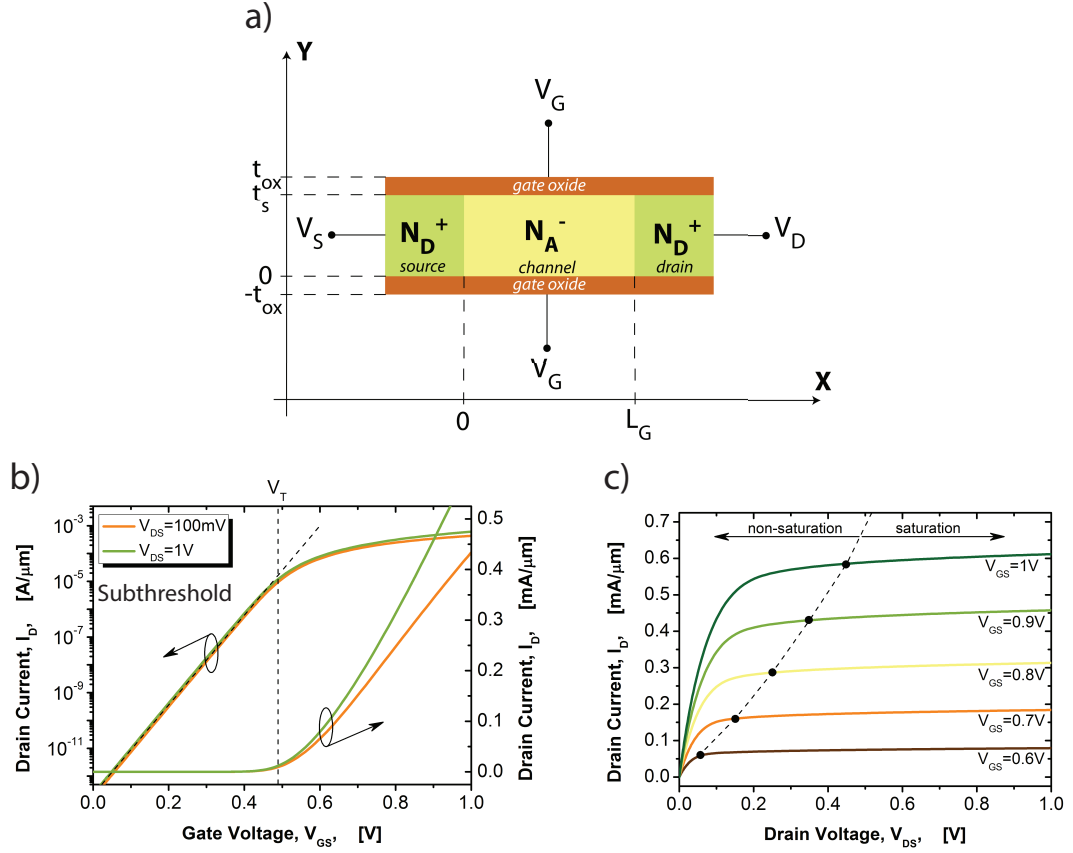


Figure 2.2: a) Sketch of a DG MOSFET structure. Simulation of the transfer a) and output b) characteristic. The simulations have been performed assuming a silicon thickness $t_{si} = 20$ nm, a gate length $L_G = 100$ nm, a channel Boron doping $N_A = 10^{16} \text{ cm}^{-3}$, a SiO_2 gate oxide 2.5 nm thick and a metal gate workfunction $q\Phi_m = 4.7$ eV. Adapted from [59]

that prevents the formation of a sizeable current flow. Only electrons sufficiently energetic, or sufficiently "hot", can be injected above the barrier (thermionic injection). A positive gate bias determines the decrease of the channel energy barrier, facilitating the thermionic injection from source to channel, resulting in an increase of the output current.

Depending on the terminal voltages, the device characteristic can be divided in different regions, as shown in Figure 2.2 [59]. For V_{GS} smaller than the threshold voltage, the MOSFET is in the so called subthreshold regime. In this region, the drain current depends on the diffusion of high energy electrons from the source. Therefore, the current depends exponentially on the gate modulation of the source to channel energy barrier as shown in Figure 2.2b. In the subthreshold region, the drain voltage doesn't impact significantly the output current. For $V_{GS} > V_{th}$ and small V_{DS} (non saturation regime), the device behaves as a gate modulated linear resistor, as represented in the first half of Figure 2.2c. Finally, for $V_{GS} > V_{th}$ and $V_{DS} > V_{DS,sat} = V_{GS} - V_{th}$ the transistor enters the saturation regime, where the current is almost independent from the drain to source bias (Figure 2.2c).

2.1.1 Subthreshold regime

In the subthreshold regime of operation, the semiconductor channel is in weak inversion and the drain current is dominated by the diffusion of electrons. The behavior of the MOSFET in this regime is fundamental for low power applications, since it determines how the device switches on and off and therefore the static power consumption. Moreover, the subthreshold region is often exploited in analog applications, since it allows to maximize the transconductance efficiency of the MOSFET [60]. The fundamental parameter to describe the current dependence on the gate voltage in weak inversion is the subthreshold slope. Its minimum value can be expressed as:

$$SS_{\min} = \frac{\partial V_G}{\partial \log I_D} \min = \frac{\partial V_G}{\partial \log \Psi_S} \frac{\partial \Psi_S}{\partial \log I_D} = \left(1 + \frac{C_S}{C_{\text{ins}}}\right) \frac{k_B T}{q} \ln 10 \quad (2.1)$$

where C_S and C_{ins} are respectively the semiconductor and insulator capacitances. If an ideal m factor of 1 is achieved, the minimum subthreshold slope reduces to $(k_B T/q) \ln 10$, i.e. to 60 mV/dec assuming a 300 K temperature. Therefore, in the best case scenario, in order to increase or decrease the output current of a MOSFET by one order of magnitude, the gate voltage must be varied of at least 60 mV.

The fixed lower limit to the subthreshold slope has dramatic consequences when the threshold voltage is reduced so to be able to correspondingly decrease the power supply. The transfer characteristic of a reference nMOSFET with fixed slope S is shown in Figure 2.3. In order to maintain the same I_{ON} current level while decreasing the power supply voltage, the gate overdrive voltage, i.e. the difference between the supply itself and the device threshold voltage, must be kept constant. Therefore, a decrease of V_{DD} requires a correspondent reduction of V_{th} . However, because of the fixed subthreshold slope, a decrease of V_{th} entails a rigid left-shift of the IV characteristic in Figure 2.3. Consequently, the I_{OFF} current will increase dramatically as well as the standby power consumption. The situation is also aggravated by the observed V_{th} roll-off for short channel transistors, which can lead to a further increase of the power consumption [61].

Electronic switches with steeper turn-on characteristic could enable the voltage scaling at constant gate overdrive maintaining a much smaller I_{OFF} value, or provide larger drive currents with the same power supply. In our quest for a good electronic field effect device, it is useful to briefly discuss what we expect from the "perfect" switch.

2.2 The ideal switch

In order to compare the performance of different electronic devices as digital switch, it is important to define the characteristics of an ideal switch. The perfect switch exhibits [62–64]:

- ON current as high as possible;
- zero OFF current (resulting in maximum $I_{\text{ON}}/I_{\text{OFF}}$ ratio);

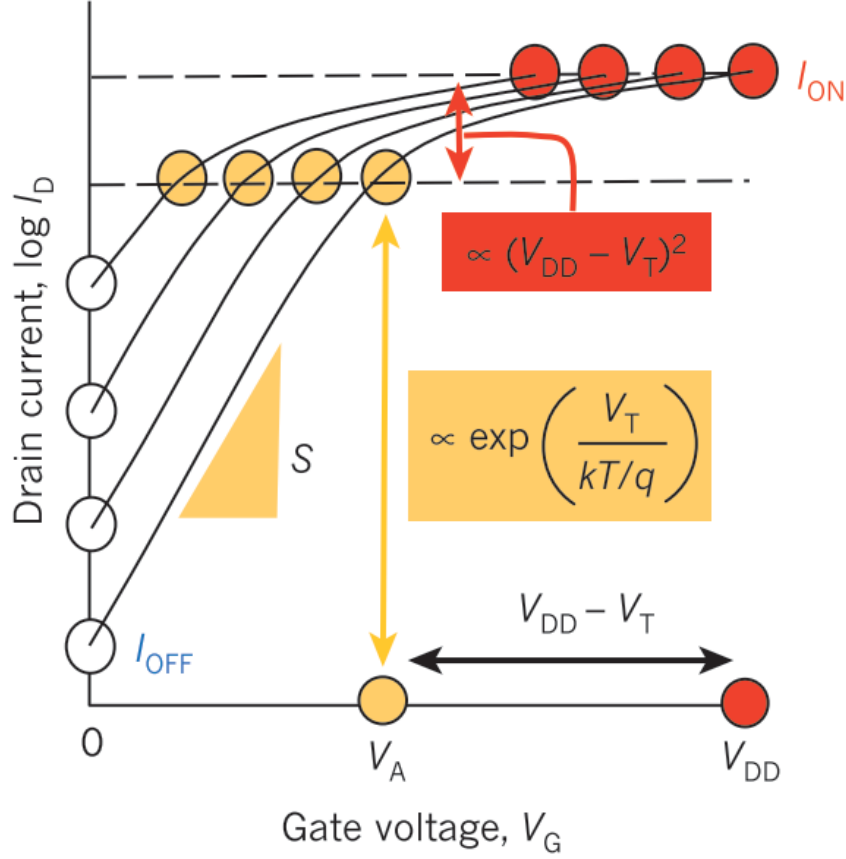


Figure 2.3: Consequences of the gate overdrive ($V_{DD}-V_G$) scaling for a MOSFET with fixed subthreshold slope. Adapted from [18].

- infinitely steep transition between the ON and OFF state ($SS = 0$ mV/dec);
- zero hysteresis in double sweep measurements;
- infinite switching speed (i.e. negligible capacitance and therefore small switching time);
- negligible footprint.

While the dynamic performance is of fundamental importance for the determination of the clock frequency and computation capability of a technology, here we are going to focus on the steady state characteristics of the ideal electronic switch. The low OFF state current and the steep turn on transition are fundamental to pursue an aggressive scaling of the power supply voltage without incurring in an excessive increase of the static power consumption of the device. An acceptably large ON current grants a good drive capability and a high operation frequency.

In Figure 2.4, the transfer characteristics of the ideal switch, a reference MOSFET with minimum SS equal to the room temperature Boltzmann limit and the envisioned steep slope FET are directly compared. Ideally, in order to replace CMOS a steep slope FET should not only present

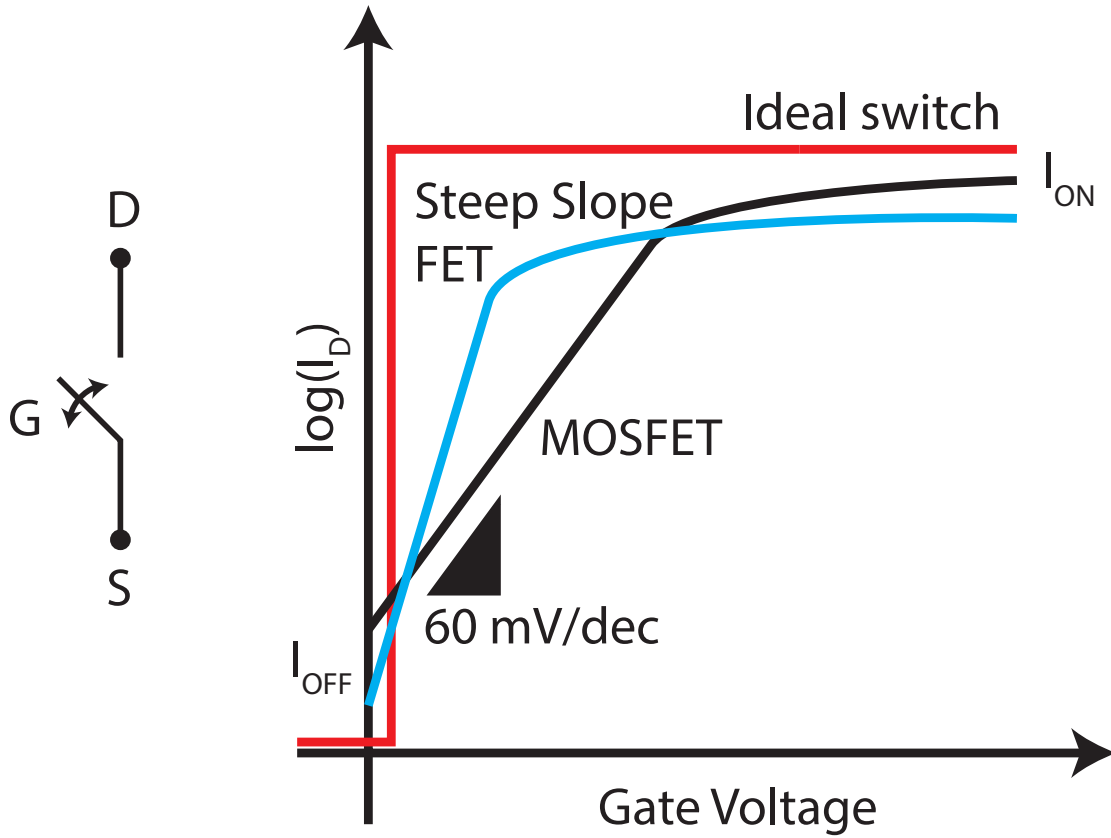


Figure 2.4: Comparison of transfer characteristics of an ideal switch, a nMOSFET and the envisioned steep slope FET. Ideally, a steep slope alternative for MOSFET should maintain a similar I_{ON} while drastically decreasing the I_{OFF} .

a sharper turn-on characteristic, so to outperform MOSFETs in the subthreshold region, but it should provide similar ON current level for the same power supply.

2.3 Tunnel FET

The transistor effect in a tunnel FET is obtained by exploiting the gate contact to inhibit or enable the onset of a band to band tunneling current between the source and the channel. Contrary to the MOSFET, here the gate doesn't modulate the height of an energy barrier but it rather introduces a energy overlap region between the source conduction (valence) and channel valence (conduction) bands so to obtain a pTFET (nTFET). Moreover, the gate voltage affects the thickness of the tunneling energy barrier seen by the carriers. Figure 5.11a reports the schematic structure of a planar pTFET. The device is quite similar to the MOSFET presented in Figure 2.1, with a fundamental difference in the doping along the channel. In order to properly operate, such a planar TFET requires a n-i-p doping profile: the source is heavily n (p) doped, the channel is intrinsic while the drain must be p (n) doped [59, 65]. This dopants distribution results in a "ladder" like band diagram when moving along the channel from source to drain, as shown in

Figure 5.11b.

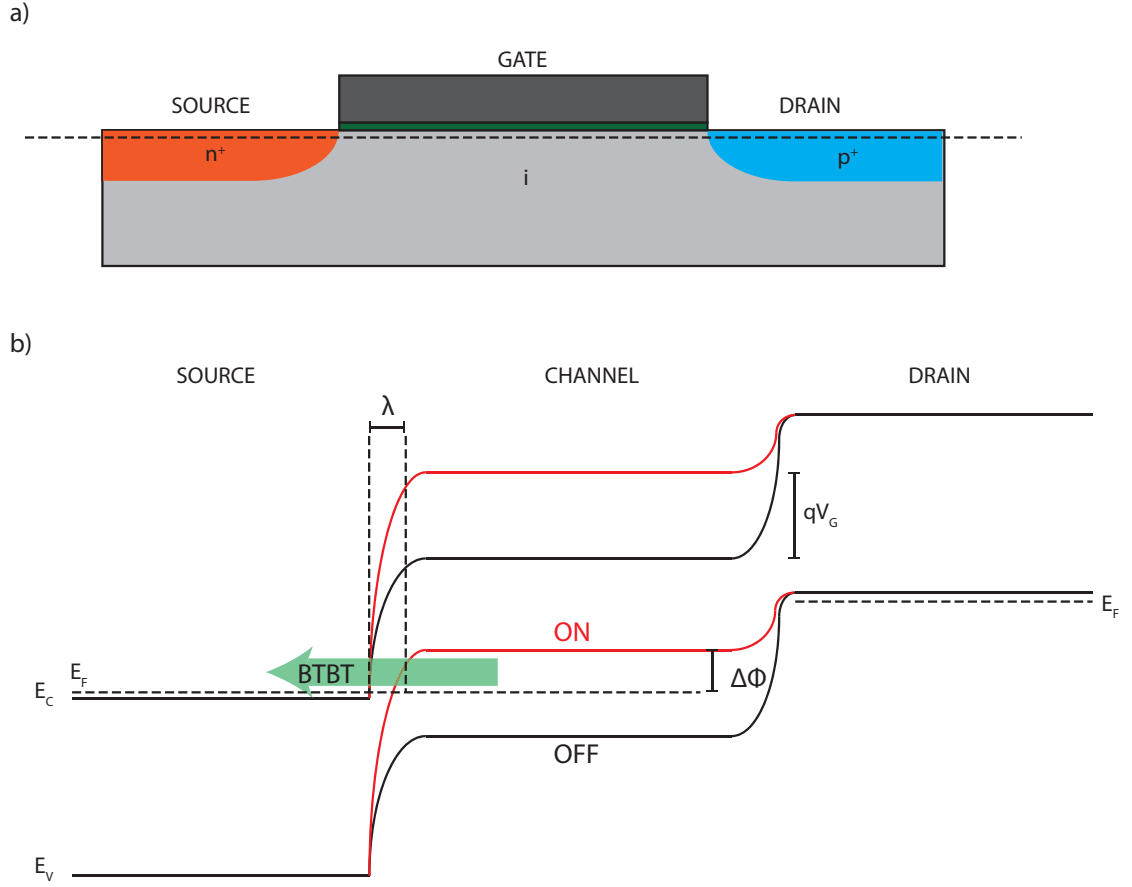


Figure 2.5: a) Schematic of a planar bulk pTFET, with the highlighted three terminals. b) Qualitative band diagram along the channel plane of the TFET, showing how the gate bias can inhibit or enable the onset of a band to band tunneling current by controlling the energy overlap region between source conduction band and channel valence band.

For null gate bias and negative (positive) drain to source voltage the pTFET (nTFET) is in its OFF state: no energy overlap between source conduction band and channel valence band is present, so the carriers in the channel don't see available states toward which tunnel to. Applying a negative gate voltage, the channel bands are pulled upward. Suddenly, the electrons in the channel valence band see available states in the source conduction band and a band to band tunneling current can flow in the device [18, 59]. The current of a TFET is proportional to the integral of the source-channel interband tunneling probability, that can be approximated to:

$$T_{\text{WKB}} = \exp\left(-\frac{4\lambda\sqrt{2m^*}\sqrt{E_g^3}}{3q(E_g\Delta\Phi)}\right) \quad (2.2)$$

where m^* is the tunneling effective mass, E_g is the bandgap, λ is the tunneling length, describing

the extent of the source-channel tunneling region, and $\Delta\Phi$ is the energetic difference between the source conduction band and the channel valence band (see Figure 5.11b) [18]. The gate voltage modulates the surface potential at the tunneling interface. Negative gate bias in particular reduces λ and increases $\Delta\Phi$, enabling the onset of the BTBT current. For a given semiconductor, the ON current achieved exploiting BTBT is intrinsically smaller than the current level obtained by thermionic injection, because of the higher probability of the latter with respect to the tunneling mechanism. Therefore, when comparing TFET and MOSFET performance on a particular material and technology platform, the best case scenario is the one shown in Figure 2.6. Ideally, the TFET offers a smaller I_{OFF} than the MOSFET but lower I_{ON} . It is possible to divide the graph in two regions, which are delimited by the crossing points of the characteristics of the two devices. In region one, taking advantage of the steeper turn-on, the TFET can outperform the MOSFET, offering higher current for the same gate voltage (or same current with lower gate voltage, i.e. lower power supply). Exiting the subthreshold region, the MOSFET curve crosses the tunnel FET transfer characteristic defining a second region. Indeed, for larger gate voltages, the MOSFET offers higher ON current levels.

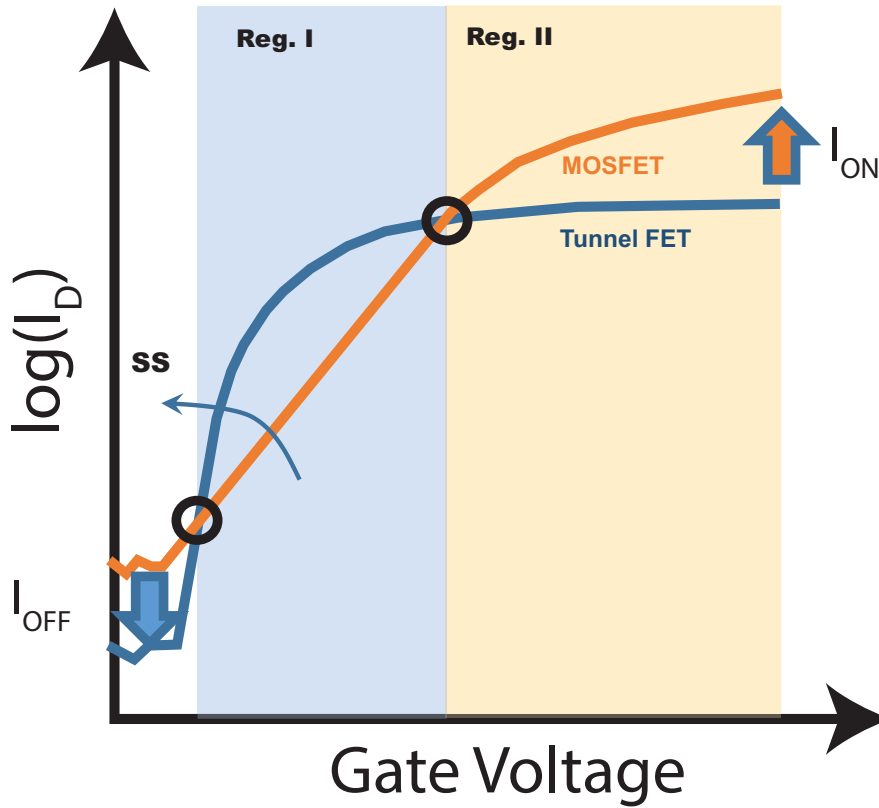


Figure 2.6: Qualitative comparison of transfer characteristics of TFET and MOSFET realized in the same material system.

Therefore, TFET could outperform CMOS technology for low power, low current devices, but it is difficult for this technology to compete in the high performance, high current applications. Rather than replacing CMOS, TFETs can therefore become a complementary technology, taking advantage of the lower power consumption to target the emerging market of remote sensing and simple, low power computing tasks. Starting from Figure 2.6 it is possible to identify three

fundamental features of a "good" TFET:

- ON current not excessively smaller if compared to the corresponding MOSFET;
- low OFF current to minimize the standby power consumption;
- subthermal subthreshold slope ($SS < 60$ mV/dec) over several decades of the output current.

2.3.1 TFET performance overview

While able to reach subthermal subthreshold slopes, silicon TFETs typically exhibit much smaller ON current levels if compared to equivalent FETs and consequently quite limited drive capability. Therefore, a considerable research effort has been dedicated to the investigation of alternative material systems that could provide not only a steep turn-on but also acceptable current levels. Figure 2.7 is a collection of the results obtained from several research groups, directly compared with the transfer characteristic of commercial MOSFETs [66]. It is worth to focus on some common trends, in particular considering the different architectures and materials investigated. For instance, independently from the considered TFET, basically all the results published exhibit smaller I_{ON} than the reference FinFETs. Moreover, all silicon homojunction devices are grouped quite at the bottom of Figure 2.7: despite exhibiting much smaller I_{OFF} than the FinFET and in some cases steeper turn-on, all these devices show unacceptably low current levels. Therefore, the silicon platform is not suited for the development of a complementary TFET technology. An interesting alternative is offered by III-V materials, that exhibits high carrier mobilities and small band gaps that contribute to boost the ON current level. However, the OFF current is strongly degraded in most of these devices. Several research groups have focused on III-V heterojunction devices so to maintain low standby power consumption and high current levels. Indeed, by properly selecting the materials to be employed in the heterojunction it is in theory possible to obtain sharp junctions with maximized energy overlap, and so enhanced tunneling probability. In 2011 Intel demonstrated the potential of this class of materials realizing both nMOSFET and nTFET based on the same InGaAs platform [67, 68]. The structure of this TFET is shown in Figure 2.8 together with a direct comparison of the transfer characteristic of the two types of devices. As expected from the best case scenario outlined in Figure 2.6, in this case the III-V TFET outperforms the MOSFET in the subthreshold region providing a steeper turn on, but it provides considerably reduced ON current levels.

A low density of interface traps is fundamental to achieve subthermionic SS in heterojunction TFET. Indeed, the presence of traps at either the oxide/semiconductor or semiconductor/semiconductor interface enables the so called trap assisted tunneling (TAT) mechanism that strongly degrades the turn-on characteristic of the device. This phenomenon and its effect on the TFET performance is shown in Figure 2.9, where the impact of an increasing density of interface traps in a InAs/Si heterojunction TFET is compared to the experimental transfer characteristic of the device [91]. Even a low density of traps is sufficient to lose the steep turn-on, reaching slopes value even larger than the ones achieved in scaled MOSFET nodes.

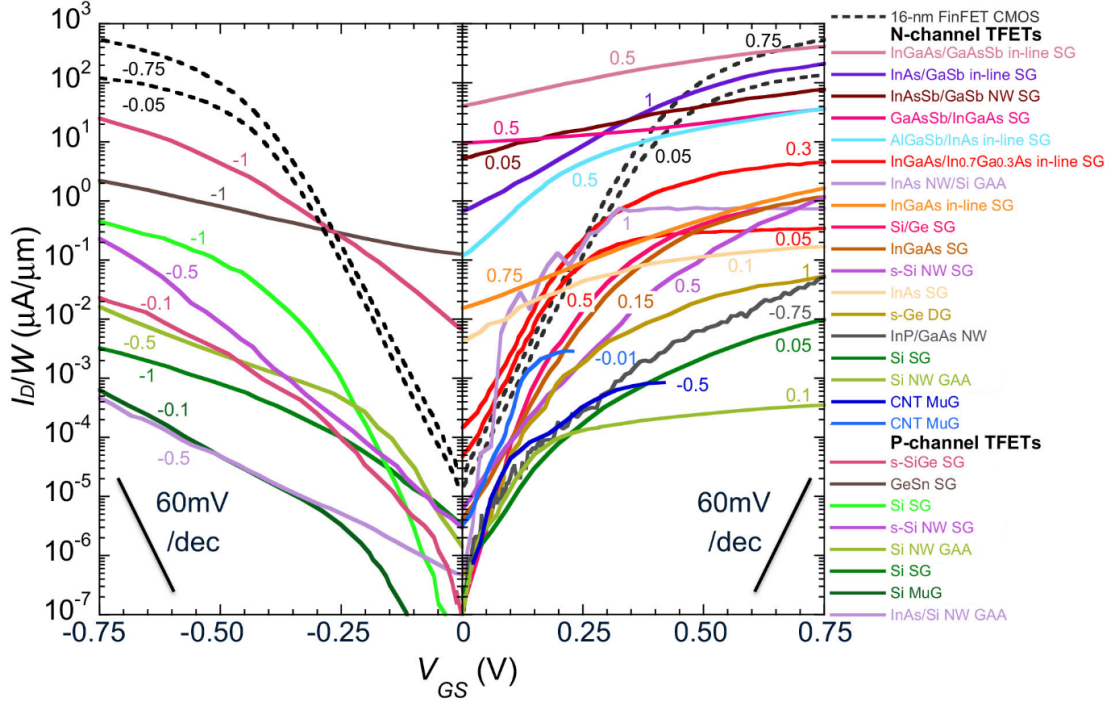


Figure 2.7: Direct comparison of the transfer characteristics of commercial MOSFET (16 nm low-power FinFET) and published results on several TFETs based on a variety of structures and materials. Adapted from [66], with data from [69–90].

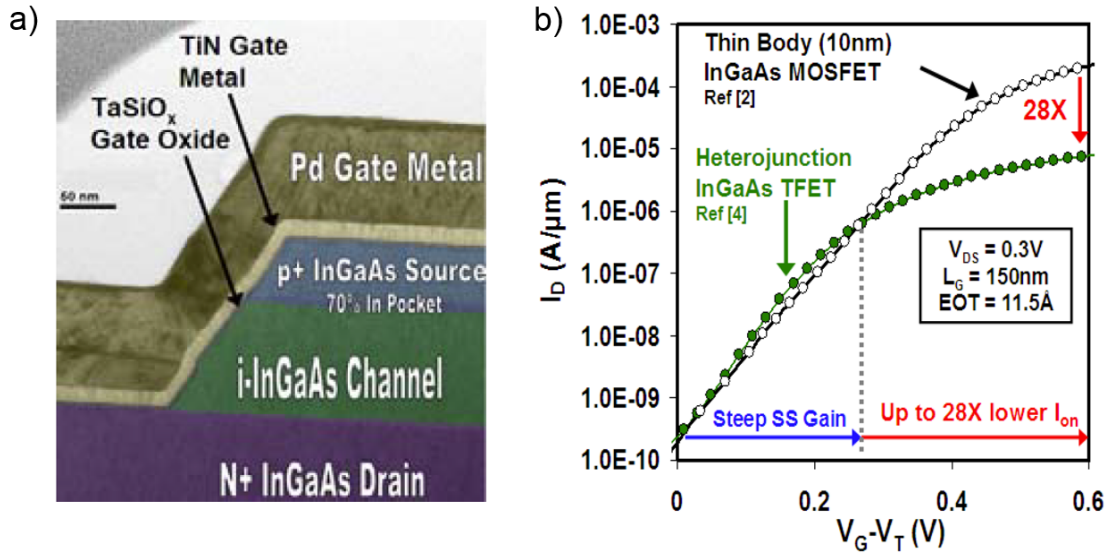


Figure 2.8: a) Structure of the InGaAs TFET demonstrated by Intel. b) Direct comparison of TFET and MOSFET transfer characteristics obtained from devices realized in the same material system. Adapted from [67, 68].

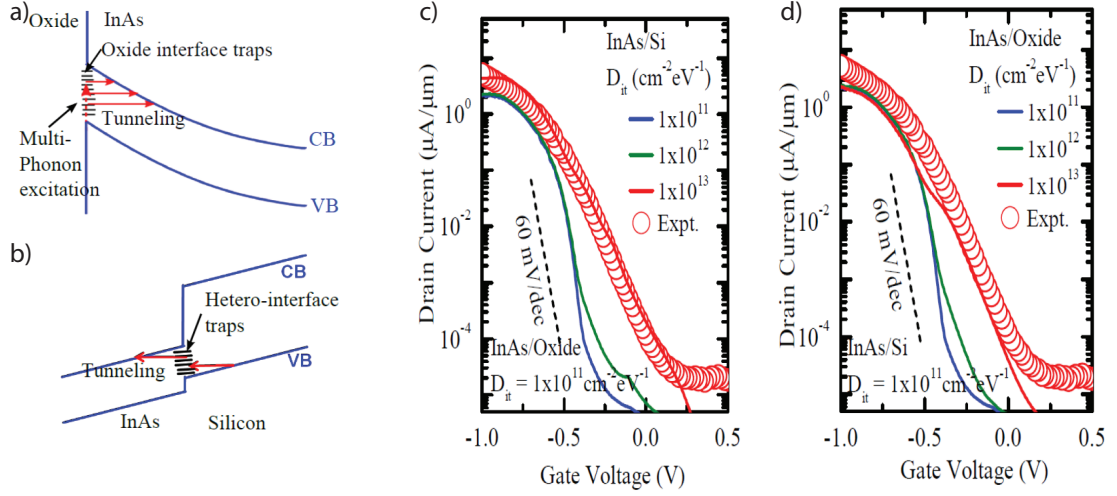


Figure 2.9: Trap assisted tunneling paths at the a) oxide-semiconductor interface and b) at the heterojunction interface in a InAs/Si TFET. c) Simulated transfer characteristic for different values of the density of traps at the heterojunction interface compared with the experimental characteristic. d) Simulated transfer characteristic for different values of the density of traps at the oxide-semiconductor interface compared with the experimental characteristic. Adapted from [91].

2.3.2 Signatures of BTBT and TFET operation

Depending on the FET architecture and the selected semiconducting materials it is not always evident whether the current measured is due to band to band tunneling rather than thermionic injection or trap assisted tunneling. Therefore, it is useful to briefly introduce three typical signatures visible in the electrical characteristics of a FET that are clear sign of the onset of BTBT and so of the potential use as TFET:

- negative differential resistance (NDR) in the output characteristics;
- subthermal subthreshold slope in the transfer characteristic;
- temperature independent subthreshold slope.

Each of these features is usually sufficient to correctly identify a band to band tunneling mechanism. However, they are not necessarily observed in real devices because of non idealities and parasitic effects.

The negative differential resistance can be observed in forwardly polarized tunneling junctions in case the band alignment at equilibrium provides a tunneling path even at $V_{DS} > 0$ V. Such a phenomenon is commonly observed in Esaki diodes [59, 65], as described in Figure 2.10. In an Esaki diode under equilibrium, there is a non zero energy overlap between the n-doped conduction band and the p-doped valence band. Under negative bias (Figure 2.10c), electrons tunnel from the p-doped semiconductor to the n-doped area, determining an exponential increase of

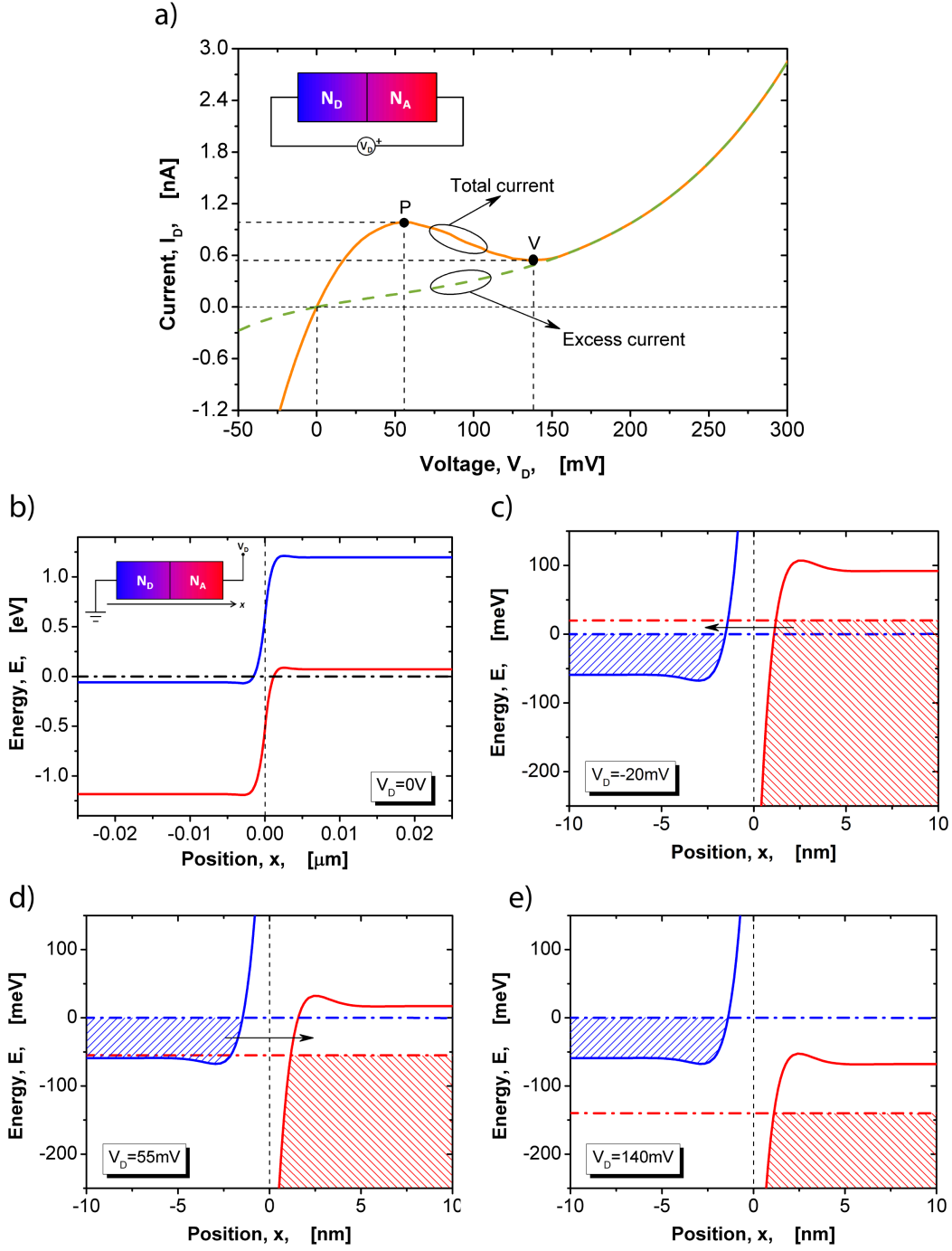


Figure 2.10: a) Simulated IV curve for an Esaki diode ($N_A = 5 \cdot 10^{20} \text{ cm}^{-3}$, $N_D = 3 \cdot 10^{20} \text{ cm}^{-3}$) showing the negative differential resistance effect. Bands alignment at the tunneling junction at b) equilibrium, c) negative drain bias, d) small positive bias and e) large positive bias. Adapted from [59].

the current. Figure 2.10d shows the band alignment under positive, small applied bias: because of the non zero energy overlap a tunneling path is open from the n side conduction band to the p side valence band, determining the increase of the junction current. For larger positive bias (Figure 2.10e), the bands overlap decreases, determining the decrease of the output current. Finally, under large bias thermionic injection typical of pn diodes kicks in and overcomes the BTBT effect, determining the current increase shown in Figure 2.10a.

The sub 60 mV/dec room temperature subthreshold slope is surely the most characteristic feature of TFET, and it represents the main advantage of this class of devices over MOSFET. However, even in FETs actually exhibiting a BTBT current, reaching a subthermal slope is not a given. Indeed, if the tunneling junction is not sufficiently sharp and exhibits a large density of defects, the SS value drastically increases as shown in Figure 2.9d.

Finally, a fundamental signature of BTBT conduction is the temperature insensitive SS. Ideally, a TFET should maintain the same subthreshold slope both at room and cryogenic temperatures, while MOSFETs slope decreases with the decrease of temperature because of the thermionic injection temperature dependence. However, in case a trap assisted tunneling mechanism is actually participating in the definition of the TFET current, the subthreshold slope value does depend on the device temperature. By decreasing the temperature, more and more trap states are frozen, resulting in a steepening of the turn-on characteristic of the TFET. Once all the traps states are made unable to participate to the conduction, the subthreshold slope stabilizes and becomes temperature insensitive [92]. The constant subthreshold slope of TFETs could be interesting for the realization of interface circuits between room temperature systems and quantum computing processors, who typically work at fractions of Kelvin. Logic blocks with temperature insensitive characteristic would be extremely interesting in order to cover the huge temperature gradient in such a system.

2.4 2D FET and TFET

As discussed in the introduction, the large variety of 2D materials successfully synthesized and the huge research interest attracted recently by this subject led to development of such a variety of electrical devices that it would be difficult to provide here a comprehensive summary. Therefore, the focus of this discussion is the typical structure exploited to realize 2D FETs, and a brief overview of the attempts done to realize and demonstrate 2D based tunnel FETs.

Depositing good quality dielectrics on the surface of 2D materials is often challenging due to the low reactivity of their surface [93]. Moreover, the dielectric deposition can significantly impact the properties of the 2D flakes in terms of carriers mobility and even polarity. As a result, the great majority of works published on 2D FETs rely on back gated architectures. Typically, the substrate is based on a highly doped silicon wafer capped by a dielectric layer, often SiO_2 . The thickness of the bottom dielectric layer is critical to provide a good optical contrast for the thin flakes, that can be then easily identified by optical microscopy [94]. Of course, the thicker the dielectric, the larger the gate voltage required to effectively modulate the channel conduction. 2D flakes can then be exfoliated or transferred on the substrate, where they are identified relying on optical microscopy. The device is completed by depositing metallic contacts. A common strategy relies

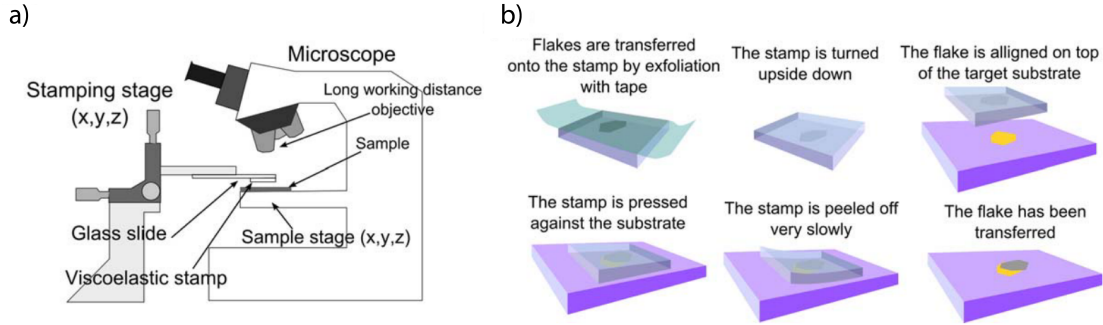


Figure 2.11: a) Setup used for the deterministic transfer of 2D flakes exploiting a viscoelastic stamp. b) Summary of the different phases of the transfer process. Adapted from [42].

on electron beam lithography (EBL) on a bilayer polymer (MMA/PMMA) followed by metal evaporation and lift-off. Evaporation is usually preferred to sputtering for both the easier lift-off process and the lower potential damage to the 2D material [93]. The MMA/PMMA bilayer grants both a good resolution of the EBL step and a relatively easy, non-aggressive lift-off process in commercial acetone.

In order to fabricate 2D/2D heterojunction devices, the typical process and structure is quite similar, with the important addition of a deterministic transfer step. Indeed, while the first layer can be exfoliated in a random position on the substrate, that is then inspected to find good flakes, the second 2D material must be carefully positioned so to obtain a non zero overlap area. Several strategies, each with its own advantages and drawbacks, have been proposed and demonstrated. Here, we focus on the transfer technique we exploited for the fabrication of the heterojunction devices presented in this work. In order to transfer 2D flakes with a completely dry procedure it is sufficient to use a polydimethylsiloxane (PDMS) stamp [42]. A sketch of the setup and the summary of the different phases of this process are reported in Figure 2.11. PDMS is a transparent, silicon based organic polymer of widespread use in microtechnology in particular for microfluidics applications. The flakes to be transferred can be exfoliated by scotch-taping directly on a PDMS stamp, that it is then positioned on a glass slide. Taking advantage of the transparency of both the glass and the polymer in the visible range, it is possible to align the flakes to be transferred with respect to the 2D material already present on the fabrication substrate. Indeed, the glass slide can be mounted, with the PDMS stamp upside down, on a manipulator and placed under a microscope lens. Then, by simply changing the focus of the optical system it is possible to control and correct the relative position of the flakes on the substrate and on the stamp. Finally, PDMS is brought in contact with the substrate and slowly peeled off, so that the flake to be transferred adheres preferentially to the receiving surface.

The deterministic transfer techniques enable the realization of 2D heterostructures, by realizing junctions with either other 2D flakes or more conventional 3D semiconductors. Heterojunctions based on 2D materials are particularly promising for the realization of tunnel FETs, since they provide access to an incredibly variegated range of band alignments and to clean, atomically sharp tunneling interfaces [96]. Several simulation results have been published predicting optimal TFET performance for 2D/2D heterojunctions based on either in-line or vertical tunnel-

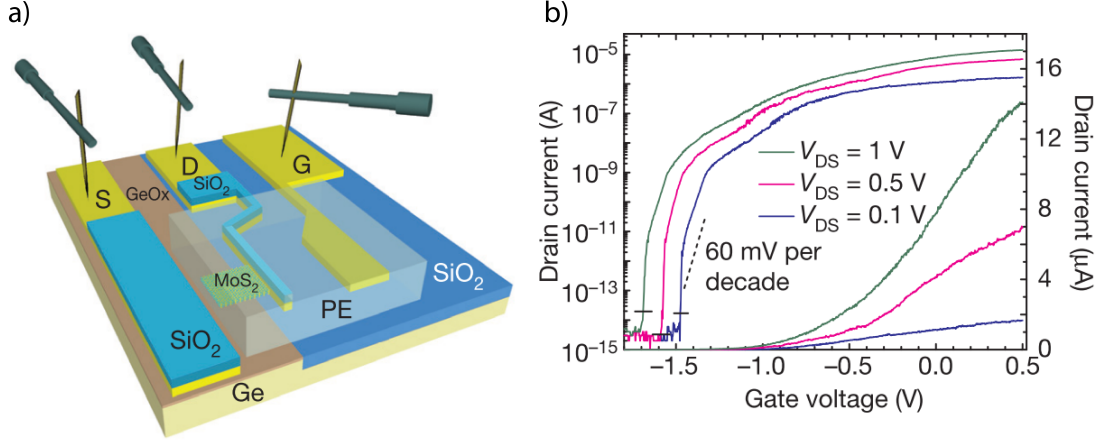


Figure 2.12: a) Structure of a Ge/MoS₂ TFET measured using an ionic liquid gate. b) Transfer characteristic, showing subthermal subthreshold slope. Adapted from [95].

ing [97, 98]. Moreover, numerous reports of room temperature or cryogenic NDR in the output characteristic of 2D heterojunctions are present in literature. However, only few devices reaching subthermal subthreshold slopes at room temperature have effectively been experimentally demonstrated. Among these studies it is worth to mention a mixed dimensionality heterojunction, based on a Ge/MoS₂ system. The schematic of this device is shown in Figure 2.12a, and it relies on an ionic liquid gate to provide the gate bias with a high equivalent gate capacitance [95]. Figure 2.12b reports the measured transfer characteristic, showing a steep turn-on of the device current over several orders of magnitude of the output current.

Several challenges contribute to sub optimal performance of 2D based TFETs:

- fabrication residues at the tunneling interface;
- low quality of the dielectric layer, resulting in insufficient gate coupling;
- band alignment different from theoretical predictions;
- difficulty in controlling the doping of 2D materials.

In the following chapter of these thesis we shall see the contributions provided throughout this project for the realization of 2D, 2D/3D and 2D/2D MOSFET and TFETs and towards the solution of part of the mentioned 2D materials limitations.

3 | 2D planar field effect transistors

This chapter presents an overview of the research dedicated to the fabrication and characterization of 2D planar FETs, with particular attention to the fundamental role played by dielectric layers on the final device performance, stability and electrical polarity. The interest of black phosphorous as high hole mobility complement to the TMDC family of 2D materials is introduced. In order to reduce the exposure of this material to oxidant and contaminating agents during the fabrication process, we discuss the possibility of using predeposited metallic contacts. A structure based on embedded, pre-deposited electrodes is designed and validated by the electrical characterization of top gated BP FETs. The possibility of tuning the device polarity by properly selecting the workfunction of the embedded contacts is demonstrated. In the second part of the chapter, we briefly discuss the potential of WSe₂ to realize a true complementary 2D MOSFET technology by exploiting electrostatic doping to tune the flake polarity. The challenges related to the deposition of high-k dielectric with good properties on 2D materials are highlighted, followed by the description of the process flow developed to obtain high quality HfO₂ on WSe₂ FET. The fabricated double gated WSe₂ FETs are electrically characterized, and a detailed discussion of the impact of both top and back gate on either the back or top gated transfer characteristic is provided. Finally, we discuss the frequency dependence of the devices hysteresis. The content of this chapter is based on the work presented in [99–102].

3.1 Top gated Black Phosphorous FETs with pre-patterned embedded electrodes

Black phosphorous (BP) is a layered van der Waals material of the elemental phosphorous allotropes family. It is synthesized by heating white phosphorous powder at high pressure [51]. Its crystalline structure is orthorhombic and it is based on phosphorous atoms covalently bonded with three neighbors so to create a single-layer honeycomb lattice. Black phosphorous exhibits direct band gap (0.3 eV in bulk up to 1.5 eV in the monolayer) and high hole mobility [48]. These characteristics contribute to make BP a promising alternative or complement to transition metal dichalcogenides (TMDCs), a class of 2D materials typically exhibiting indirect band gap, prevalent electronic conduction and limited carrier mobilities [103–105]. Moreover, the presence of a finite band gap allows to obtain reasonable I_{ON}/I_{OFF} ratios, overcoming the fundamental limitation of graphene FETs [35]. The small, direct band gap opens promising opportunities for the implementation of BP based infra-red and visible photodetectors.

However, a fundamental challenge for black phosphorous based devices is the instability of this material in ambient conditions. The electrical and mechanical properties of non-passivated samples exposed to air and moisture are rapidly degraded to such an extent that the functionality of the fabricated devices is irreversibly compromised [51]. Effective passivation of exfoliated BP flakes has been demonstrated via deposition of Al_2O_3 or HfO_2 capping layers [106, 107]. The resulting field effect devices exhibited stable and encouraging performance.

The most commonly reported fabrication procedure for BP FETs relies on the exfoliation of black phosphorous flakes on a SiO_2 layer followed by the deposition by lift-off of the electrical contacts, similarly to the majority of 2D material based FETs [48, 50, 108, 109]. The flakes are then passivated by the deposition of a dielectric capping layer or measured under high vacuum conditions. However, both the mechanical exfoliation and the fabrication of the electrode contacts are likely to determine a prolonged exposure of the fragile and oxygen sensitive BP flakes to air. The exfoliation in inert glove boxes can contribute to drastically reduce the deterioration of the samples, but it requires bulky dedicated equipment and it doesn't solve completely issues deriving from process induced degradation. The introduction of pre-patterned source and drain contacts has been proposed so to complete as many processing steps as possible prior to BP exfoliation, thus greatly reducing the exposure time to contamination sources [51]. Moreover, this strategy for the electrode deposition allows maximizing the accessible area of black phosphorous for sensing applications while granting a potential excellent top gate electrostatic control on the contact area [110]. However, the reported devices showed an $I_{\text{ON}}/I_{\text{OFF}}$ ratio lower than 10 and reduced carrier mobility [51].

The purpose of this project was to investigate the potential benefits of pre-patterned *embedded* source and drain contacts. With respect to simply pre-patterned electrodes, embedding electrodes in a SiO_2 layer allows reducing the amount of mechanical stress on black phosphorous flakes due to topography steps with height comparable or larger than the flakes thickness. The reduced topography of the receiving substrate can contribute as well to greatly increase the exfoliation yield. By opportunely selecting the workfunction of the metallic contacts we were able to selectively suppress one of the conduction branches, obtaining both n and p-type devices on the same substrate [101, 111].

3.1.1 Black Phosphorous FET fabrication

The developed process flow is summarized in Figure 3.1. The starting substrates is constituted by a silicon wafer oxidized so to obtain a top SiO_2 layer 280 nm thick. The areas designed to host the embedded source and drain contacts were lithographically defined using a direct writing laser tool, VPG200, and a direct resist, ECI 3027. We then etched 45 nm deep boxes in the SiO_2 layer exploiting a combination of dry and wet etching. The electrodes were then formed by evaporation and lift-off of either Ti (5 nm) and Au (40 nm), or Ti (5 nm) and Ag (40 nm), depending on the targeted electrical polarity of the final device. By carefully controlling both the dielectric etching and the metal deposition (the deposited metal thickness was directly monitored with a quartz crystal in the deposition chamber) it was possible to reduce the step between the electrodes top surface and the SiO_2 layer to few nanometers. This fabrication approach enables the realization of back contacts exhibiting much smaller surface roughness with respect to pre-

3.1. Top gated Black Phosphorous FETs with pre-patterned embedded electrodes

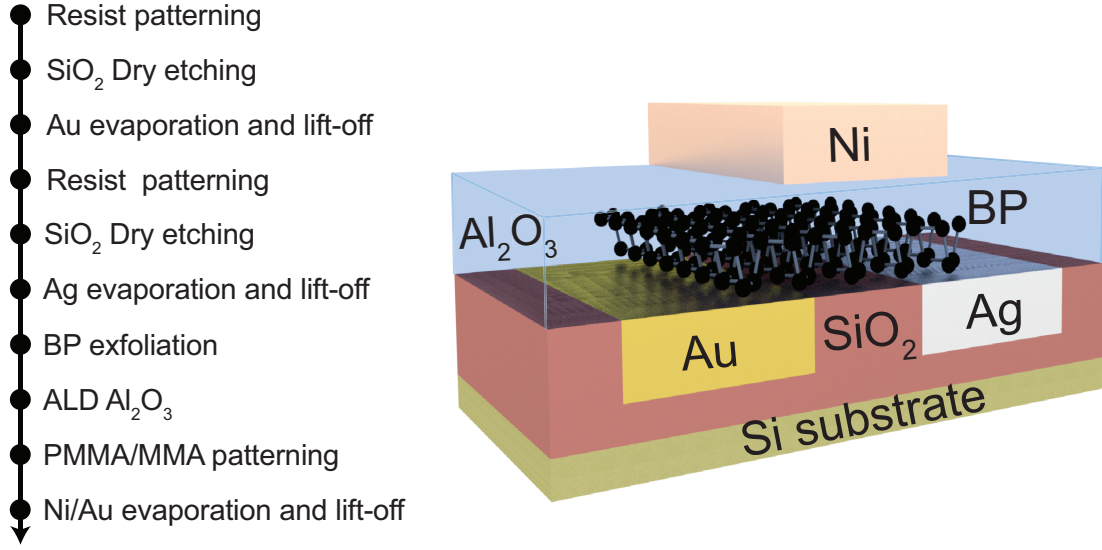


Figure 3.1: Schematic view of the complete device and summary of the fabrication process flow.

patterned non-embedded electrodes [51], providing an exfoliation substrate with considerably reduced topography so to facilitate the transfer of BP flakes.

Next, black phosphorous flakes were mechanically exfoliated from a bulk crystal sample (synthesized by *Smart Elements*) following the scotch taping technique. In order to reduce to the minimum the exposure to ambient oxidizing agents as oxygen and water vapor, the samples were passivated shortly after exfoliation by depositing 15 nm of alumina (Al₂O₃) via atomic layer deposition (ALD). The alumina capping layer serves also as top gate dielectric in our final device. The ALD deposition was performed in a BENEQ TFS 200 reactor heated at 200 °C, using TMA and H₂O as precursors. Just before the ALD step the silicon substrate was rinsed in acetone and IPA in order to remove most of the glue residues left during the exfoliation. We then identified flakes favorably connected to the embedded electrodes using optical microscopy. Finally, the top gate electrode was fabricated by patterning a MMA/PMMA bilayer using electron beam lithography (EBL) and evaporating and lifting off a Ni (50 nm) and Au (10 nm) stack. In order to limit the gate leakage current, the top gate mask has been designed so to avoid any overlap of the gate electrode and the embedded back contacts. The thickness of the black phosphorous flakes was determined using atomic force microscopy (AFM), as shown in Figure 3.1. The results reported in the following have been obtained from BP FETs realized with flakes with thickness in the 30/40 nm range. A detailed explanation of each step of the process flow is provided in appendix Figure A.1.

3.1.2 Results

All the electrical measurements presented in the following have been performed at ambient conditions and room temperature on a Cascade prober using an HP 4156C semiconductor parameter analyzer. The Al₂O₃ passivation layer grants a long lifetime of the devices, with no observed

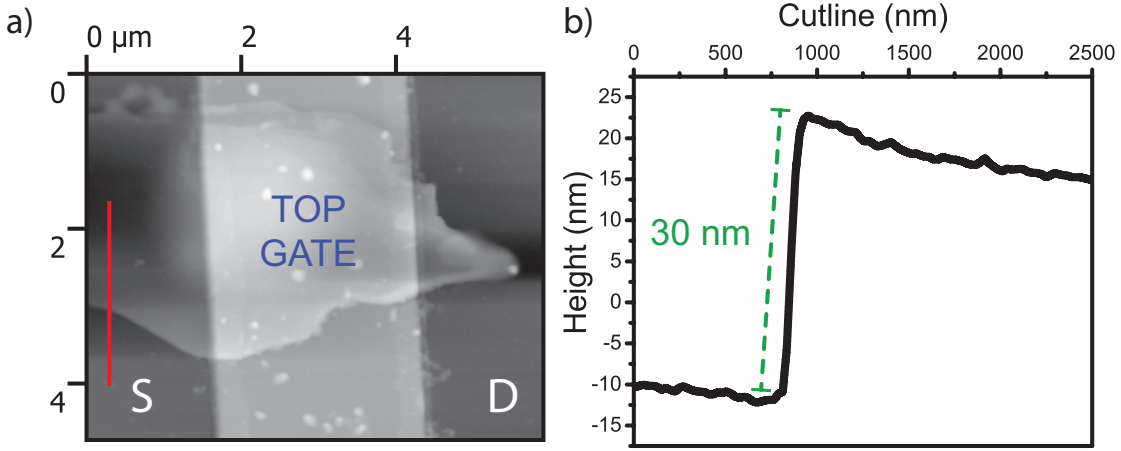


Figure 3.2: a) AFM topography image of a fabricated device, obtained in contact mode after the deposition of the capping layer and top gate electrode. The red line shows the cutline used to estimate the flake thickness. b) Height profile along the cutline, providing an estimated thickness of 30 nm.

ageing-related failures over several months.

Impact of electrodes workfunction on BP FETs polarity

With the objective of studying the impact of the workfunction of the metals used for the pre-patterned electrodes, we fabricated and characterized Au, Au-Ag and Ag-Ag contacted devices. The transfer characteristics in linear scale for three representative devices with these metal electrodes combinations are shown in Figures 3.3a,b and c. The reported $I_D(V_G)$ curves have been obtained applying a drain to source bias of absolute value equal to either 750 or 500 mV.

Au contacted devices exhibit a clear p-type conduction with a strong suppression of the electron transport, while both Ag and Au-Ag devices, where the Ag contact is used as FET source, show prevalent n-type conduction. The role played by contacts workfunction in the determination of BP FETs polarity can be understood referring to the qualitative vacuum band diagram reported in Figure 3.4. Multilayer BP flakes have a band structure similar to the bulk one, characterized by a 0.3 eV direct band gap and a 4.15 eV workfunction [48, 50]. Polycrystalline Au and Ag exhibit respectively a 5.1 eV and a 4.26 eV workfunction. As shown in Figure 3.4, Ag is expected to offer a small barrier for electron injection to BP conduction band, enabling the n-type conduction observed in silver contacted BP FETs. Vice versa, Au contacts favor holes injection while providing a high barrier for thermionic injection of electrons in BP conduction band. An analogous BP FETs polarity-control mechanism based on low workfunction metals (Al and Ti) has been reported for top contacted devices [109, 112].

3.1. Top gated Black Phosphorous FETs with pre-patterned embedded electrodes

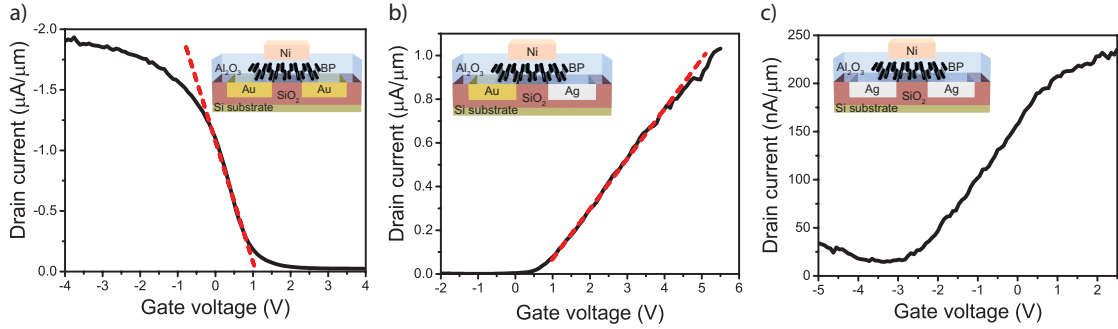


Figure 3.3: Comparison of the transfer characteristics of BP FETs realized with different combinations of embedded back contacts. The Au-Au contacted device has been measured applying a drain to source bias equal to -750 mV, while the Ag contacted devices were measured under 500 mV. a) Au contacted devices exhibit a clear p-type dominant conduction. b) and c) Devices with Ag contacts or Au-Ag electrodes with Ag used as transistor source shows n-type polarity. The red dotted lines in a) and b) represents the linear fit performed to estimate the carrier mobility. Insets: schematic representations of BP FETs with the different sets of embedded electrodes.

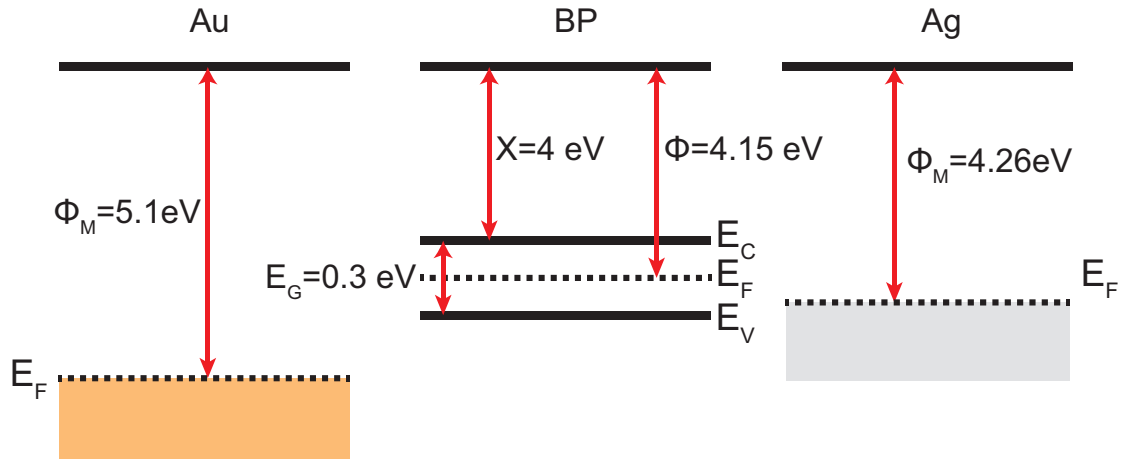


Figure 3.4: Qualitative band diagram in vacuum of Au, multilayer BP flakes and Ag. Multilayer BP flakes show a band diagram similar to bulk samples. Polycrystalline Ag exhibits a workfunction close to BP, so it is a promising candidate for electron injection in black phosphorous conduction band. Au on the contrary has a much larger workfunction, favoring hole conduction in the BP channel.

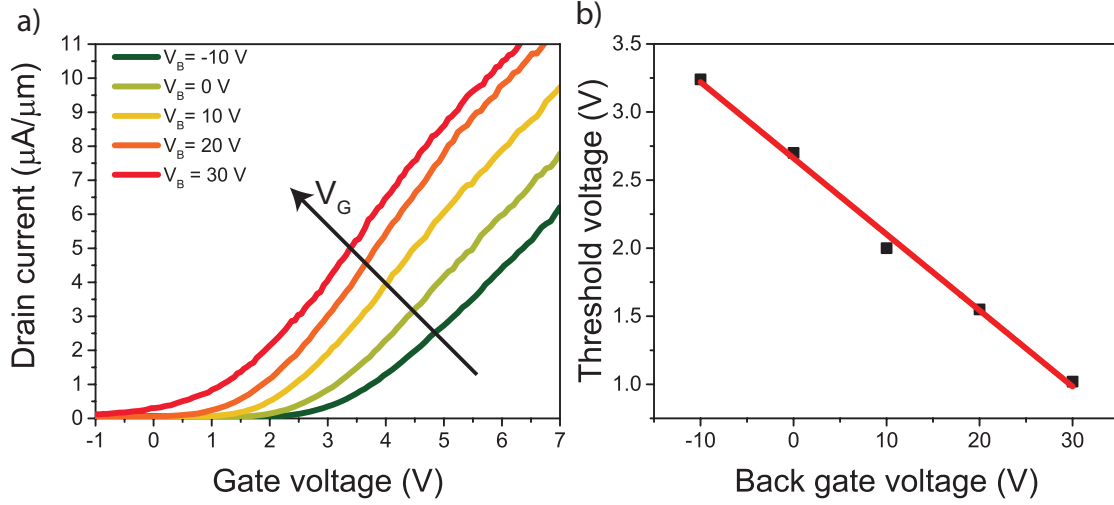


Figure 3.5: a) Top gate transfer characteristic of a n-type device measured at different back gate bias values. A clear negative shift of the $I_D(V_G)$ curve is observed under positive substrate bias. b) Extracted threshold voltage as a function of the back gate bias. The linear fit provides an estimated top gate threshold voltage sensitivity to the substrate bias of -56 mV/V. The drain to source bias for this measurements is set at 3 V.

Impact of back gate bias on transfer characteristic

As shown in the schematic structure in Figure 3.1, the BP channel can be electrostatically controlled by both the metallic top gate and the silicon substrate. However, because of the 280 nm thick SiO_2 layer present in between the flake and the back gate, the resulting back gate capacitive coupling is inevitably weak. Therefore, a relatively large back gate bias is required to significantly impact the FET conduction. Moreover, the introduction of large embedded metal contacts placed closer to the back gate with respect to the FET channel provides a preferential leakage path from the electrodes that would mask the gate leakage from the BP flakes. Therefore, rather than sweeping the back gate bias in order to use it as main driving gate, we studied the impact of a fixed bias applied to it on the top gate transfer characteristic.

Figure 3.5 reports the transfer characteristics of a n-type device measured at different values of substrate bias. The increase of the back gate voltage from negative to positive values determines a clear negative shift of the transfer characteristic. Indeed, the top gate threshold voltage extracted from the intercept of the linear part of the $I_D(V_G)$ curve decreases linearly with the increase of the substrate bias as shown in Figure 3.5b. The extracted slope gives a negative shift in the top gate threshold voltage of 56 mV per applied volt at the back gate.

The back gate can be efficiently exploited to program the threshold voltage of the device by tuning the bands in the channel, providing a further degree of freedom for the fine tuning of the top gated BP FET conduction.

3.1. Top gated Black Phosphorous FETs with pre-patterned embedded electrodes

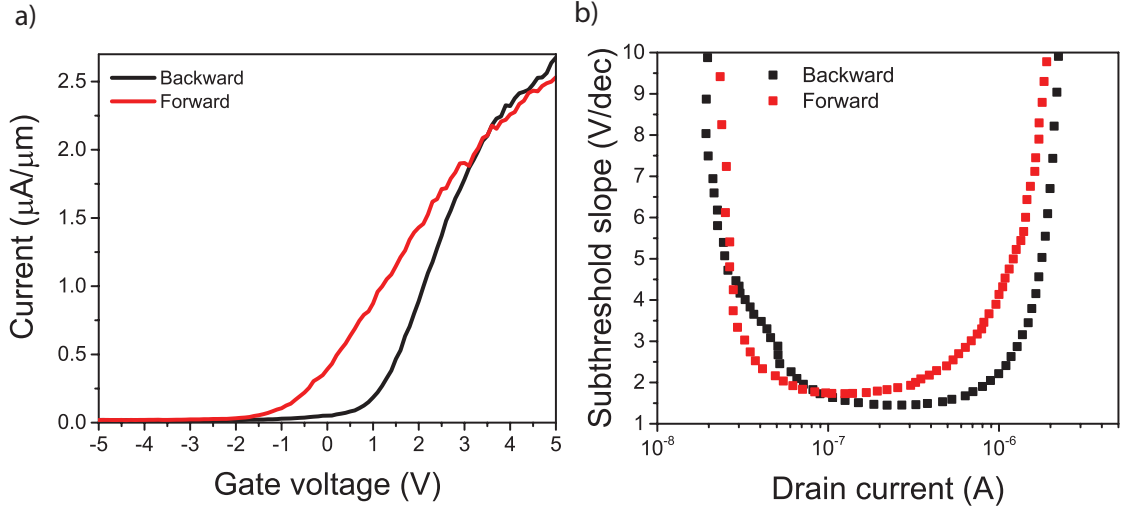


Figure 3.6: a) Double sweep transfer characteristic of a n-type device. The measured hysteresis is 1.7 V. The minimum subthreshold slope b) is 1.5 V/dec, maintained over one order of magnitude of the output current. The drain to source voltage is 5 V.

Top gate hysteresis and subthreshold slope

Al_2O_3 has been proven to provide a good passivation against oxidizing agents for black phosphorous flakes [106] and a high breakdown field. However, it is known to be characterized by a high density of interfacial charge traps, in particular when deposited on 2D materials. In order to characterize the impact of such traps on the FET conduction, we performed a double sweep measurement on a n-type device with the back gate grounded. The result is shown in Figure 3.6. The measured hysteresis between forward and backward sweeps is 1.7 V, suggesting that the $\text{Al}_2\text{O}_3/\text{BP}$ interface indeed hosts several trap states.

Figure 3.6b shows the subthreshold slope plotted vs the output current for the two sweep directions of the top gate voltage. A minimum value of 1.5 V/dec over one order of magnitude of the output current has been extracted. Such results suggest that the quality of the deposited dielectric alumina layer is not excellent, as commonly observed for ALD depositions on 2D materials. Consequently, both the hysteresis and the gate coupling efficiency are far from optimal. However, the measured top gate leakage current is extremely low, remaining below 5 pA/ μm in all the measurements reported in this work.

A substantial reduction of the hysteresis could be obtained with the deposition of other high-k dielectrics like HfO_2 , that however presents nucleation and film continuity issues on 2D flakes [113]. A significant improvement of the subthreshold slope is expected in devices realized with thinner BP flakes and thinner Al_2O_3 layer, so to increase both the channel band gap and the capacitive coupling between channel and top gate.

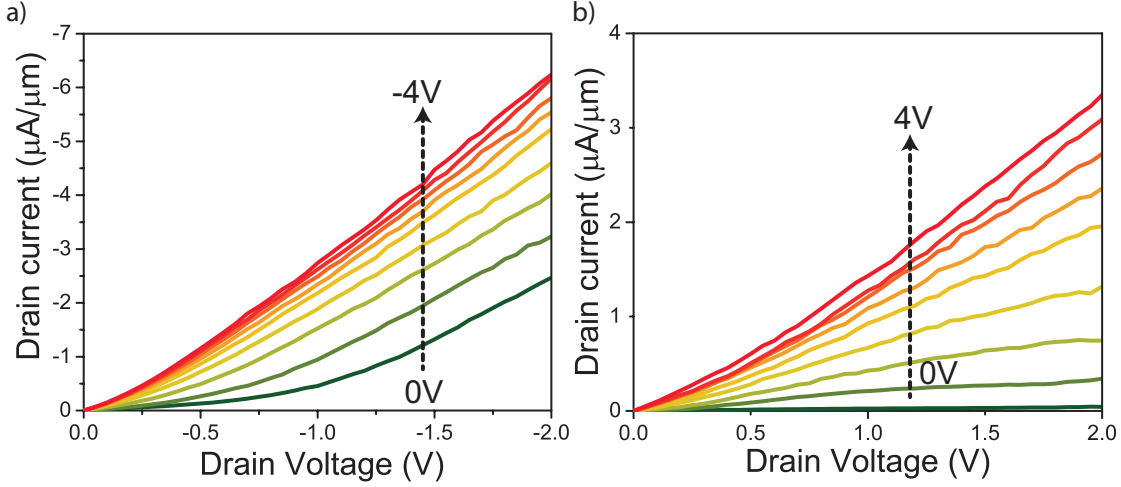


Figure 3.7: Output characteristic $I_D(V_D)$ in linear scale of the Au a) and Au-Ag b) contacted BP FETs measured at different values of the gate biases. For both the devices and set of contacts there is no saturation of the output characteristic. The gate bias is swept from 0 V to ± 4 V.

Transfer and output characteristic of n and p type BP FET

In this section we present a detailed characterization of the realized FETs, focused on representative p and n-type devices. All the measurements reported have been obtained with the back gate grounded. We fabricated both the devices on the same wafer and with the same processing conditions. The dielectric deposition was performed simultaneously on the two FETs. The p-type device is contacted with Au electrodes and has gate length $L = 2.6 \mu\text{m}$ and width $W = 1.5 \mu\text{m}$. The n-type FET has Au drain and Ag source, with $L = W = 1.6 \mu\text{m}$. The output characteristics of these two devices, measured under different values of the top gate bias, are reported in Figure 3.7. The $I_D(V_D)$ curves of both the Au contacted device (Figure 3.7a) and the Ag-Au one (Figure 3.7b) show no saturation for the considered gate bias range.

We report in Figure 3.8 the transfer characteristics of the same devices in semi-logarithmic scale, obtained measuring the $I_D(V_G)$ curves at different drain-to-source biases. The p-type FET (Figure 3.8a) shows a $I_{\text{ON}}/I_{\text{OFF}}$ current ratio larger than two orders of magnitude. The n-type device instead (Figure 3.8b) reaches a $I_{\text{ON}}/I_{\text{OFF}}$ of 1700. These results greatly outperform the ON/OFF current ratios reported for pre-patterned non-embedded contacts, and could be further improved in BP FETs realized with thinner flakes and back gate dielectric, taking advantage of the larger black phosphorous band gap and the higher quality of the substrate dielectric layer [51].

Figure 3.9 shows the extracted gate transconductance (g_m) curves as a function of the gate bias for the two devices, measured under several values of the drain to source bias. The Au contacted device transconductance (Figure 3.9a) exhibits a relatively narrow peak in the gate bias range from -1 V to 1 V. This suggests that the contact resistance is playing a major role in limiting the transconductance, preventing the saturation of the curve at the peak value. Indeed, at large negative gate biases, the series resistance provided by the contacts becomes larger than the BP channel resistance determining a decrease of the transfer characteristic slope and the consequent

3.1. Top gated Black Phosphorous FETs with pre-patterned embedded electrodes

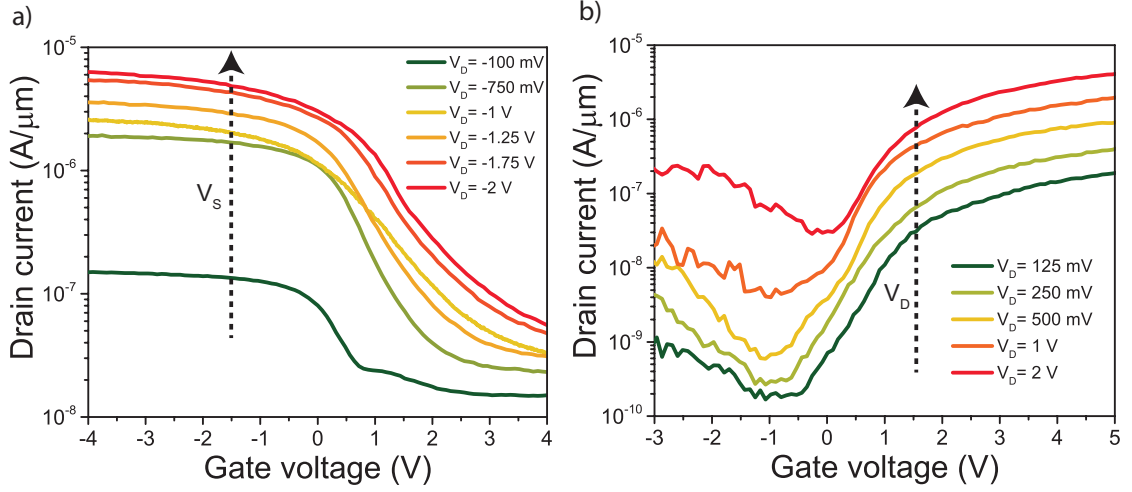


Figure 3.8: Transfer characteristics $I_D(V_G)$ at different drain-to-source biases in semilog scale of the characterized p-type a) and n-type b) BP FETs. The p-type device reaches a I_{ON}/I_{OFF} ratio larger than 10^2 , while the n-type FET provides a ON/OFF current ratio larger than 10^3 .

degradation of the transconductance. Conversely, the n-type device transconductance, reported in Figure 3.9b, saturates to its peak value over a large window of gate voltages suggesting a lower impact of the contact resistance on the n-type FET conduction.

Field effect mobility extraction

We then extracted the two-terminal effective field effect mobility, μ_{FE} , using the following equation:

$$\mu_{FE} = \frac{g_m L}{W C_{ox} V_{DS}} \quad (3.1)$$

where g_m is the transconductance extracted from the linear part of the $I_D(V_G)$ curve (see Figures 3.3a and b), W is the channel width and C_{ox} is the gate capacitance per unit area for the deposited 15 nm of Al_2O_3 . The relative permittivity of the dielectric layer has been estimated to be equal to 6.9 by characterizing MIM structures included on the same wafer of the devices. The obtained hole mobility for the Au contacted transistor is $10 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$ at $V_{DS} = -750 \text{ mV}$, while the Au-Ag FET exhibits an electron mobility of $1.8 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$ at $V_{DS} = 500 \text{ mV}$.

In order to obtain a more accurate estimation of the carriers' mobility by at least partially decoupling the impact of the contact resistances, we applied the so-called Ghibaudou Y function method, which provides a robust evaluation of the low-field carrier mobility in 2D channel field effect devices [103]. Assuming that the contact resistance is not dependent on the gate bias, the

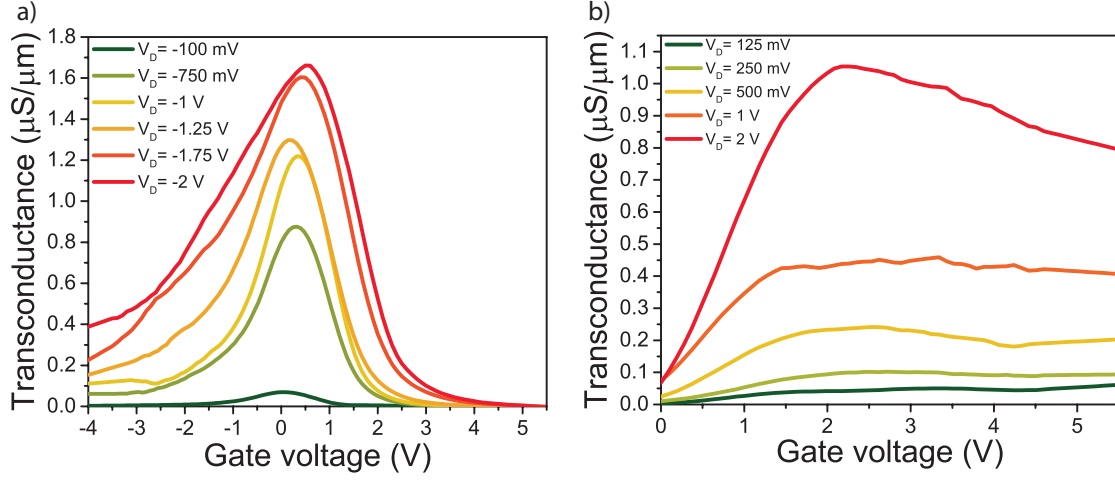


Figure 3.9: Gate transconductance $g_m(V_G)$ at different drain to source biases of the characterized p-type a) and n-type b) BP FETs. The Au contacted device shows a peak in the transconductance curve while the n-type g_m saturates to its maximum value over a wide range of the applied gate bias.

Y function expression reduces to:

$$Y = \frac{I_D}{\sqrt{g_m}} = \sqrt{\frac{\mu C_{ox} |V_{DS}| W}{L}} (V_G - V_T) \quad (3.2)$$

where V_T is the threshold voltage. The carrier mobility is then given by:

$$\mu_{FE} = \frac{L}{C_{ox} |V_{DS}| W} \left(\frac{\partial Y}{\partial V_G} \right)^2 \quad (3.3)$$

Figure 3.10b shows the Y functions extracted for the two reported devices, and the corresponding fit of the linear region from which it is possible to estimate the low field mobility applying equation 3.3. The obtained mobilities are $40 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ for holes in the Au contacted FET (Figure 3.10a) at $V_{SD} = 750 \text{ mV}$ and $2 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ for electrons in the Au-Ag device (Figure 3.10b) at $V_{DS} = 500 \text{ mV}$. The large enhancement of the hole mobility for the p-type device estimated with the Y function method together with the gate dependence of the transconductance shown in Figure 3.9, suggests that the contact resistance is playing a relevant role in limiting the Au contacted device performance. Vice versa, the n-type device shows a limited increase of the extracted mobility obtained applying the Y function method, suggesting that Ag constitutes indeed a good contact for electron injection in BP.

The extracted mobility values and I_{ON}/I_{OFF} ratios are larger than the ones reported for pre-patterned non-embedded contacts, but are still lower than other results published for top contacted BP

3.1. Top gated Black Phosphorous FETs with pre-patterned embedded electrodes

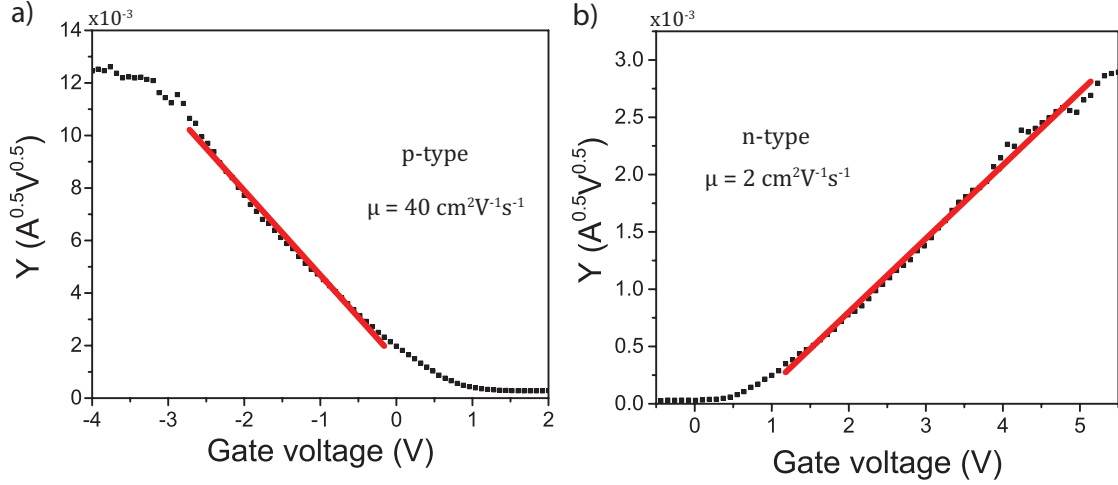


Figure 3.10: Extracted Y function vs gate voltage of a) the p-type BP FET at $V_{SD} = 750 \text{ mV}$ and b) n-type device at $V_{DS} = 500 \text{ mV}$. The mobility can be extracted from the slope of the linear part of the curve, shown in red in the figure.

FETs [48, 109]. Other sources of mobility reduction not considered here could be the interface roughness scattering, the high density of oxide traps in the SiO_2 and Al_2O_3 dielectric layers and the anisotropic mobility distribution in the 2D plane of black phosphorous [107, 114]. The performance of p-type devices could also be negatively affected by the choice of the top gate dielectric, since Al_2O_3 has been reported to impact considerably the p-type dominant conduction mechanism in black phosphorous FETs by providing a n doping effect [107]. It is also important to obtain a direct estimation of the Schottky barrier height at the bottom contact channel interface and a measurement of contact resistance as a function of the gate bias.

3.1.3 Summary

In summary, we have demonstrated for the first time complementary top gated black phosphorous FETs obtained by workfunction engineering of embedded pre-patterned contacts, exhibiting enhanced performance with respect to alternative implementations of BP FETs with pre-patterned electrodes. Both n and p-type devices have been characterized, exhibiting electron and hole mobilities respectively $2 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ and $40 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ extracted applying the Y function method. Moreover, we proved that Ag is a promising choice for electron injection in black phosphorous FETs, whose polarity can be controlled by properly selecting the contacts workfunction. The silicon substrate can be used as back gate to program the threshold voltage of the top gate transfer characteristic, providing a further degree of freedom for the biasing of the devices. Typical devices show a hysteresis of 1.7 V , minimum subthreshold slope of 1.5 V/dec and a top gate leakage current below $5 \text{ pA}/\mu\text{m}$.

The proposed fabrication approach minimizes the exposure of unprotected flakes to ambient oxidants and contaminants. The use of embedded back contacts allows a significant reduction of the substrate topography, granting a good transfer and a reduced stress on the BP flakes. The

proposed BP FETs structure is particular interesting for sensing application since it maximizes the sensing area and enables the possibility of programming the device threshold voltage using the silicon substrate as back gate. Enhancements of the performance would require the reduction of the contact resistance and the improvement of the capacitive coupling between the top gate and the black phosphorous channel. The design of the gate mask can be modified to include an overlap of the top gate and the contacts, so to make possible an effective electrostatic doping of the flake areas in direct contact with the back electrodes. The deposition of high-k dielectrics with lower interface trap density with respect to Al_2O_3 and the transfer of thinner BP flakes are fundamental to improve the overall performance of the device.

3.2 Double-gated n-type tungsten diselenide FETs with high-k top gate dielectric.

Most of the currently available semiconducting TMDCs exhibits prevalent electronic conduction, resulting typically in n-type depletion mode FETs as it is the case for MoS_2 . Undoped WSe_2 interestingly shows ambipolar conduction, with demonstrated high hole and electron mobilities and the possibility of fabricating enhancement mode FETs [47, 115, 116]. This feature combined with the capability of controlling the device polarity by either the choice of the metal contacts work function or electrostatic doping makes this material promising for the realization of a complementary 2D technology [46, 47].

Usually, 2D FETs are realized by relying on a back gate architecture [46, 47, 115–117]. The implementation of high performance top gated devices has been generally prevented by several challenges related to dielectric deposition on 2D materials. Excellent results in terms of degradation prevention and field-effect mobility preservation have been obtained by capping WSe_2 with hBN flakes [117, 118], but because of this material low-k and the complexity introduced by the deterministic assembly of 2D/2D heterojunctions this solution is unpractical for the production of high performance, standardized and scaled devices. The direct deposition of high-k dielectrics on 2D materials, following a parallel development with respect to advanced Si nodes, would be therefore the preferred approach, but it results in either discontinuous, leaky films or a large density of border traps determining huge hysteresis windows [113].

We report here high performance double gated n-type WSe_2 FETs with excellent top gate sub-threshold slope (SS) and reduced hysteresis. The gate dielectric in our devices consists of a stack of a thin Al_2O_3 seed layer and a HfO_2 dielectric layer. The alumina seed layer is obtained from the oxidation of 1.5 nm of evaporated Al, and a 5 nm thick HfO_2 film is deposited by atomic layer deposition [101, 111]. The fabricated devices were electrically characterized with particular focus on the different impact of top and back gates on the channel conduction. We propose also a detailed discussion of both the back gate and top gate hysteresis, characterized as a function of the measurement frequency and the width of the biasing window. We also compare the hysteresis results with those measured for top gated MoS_2 FETs with Al_2O_3 insulator and observe a considerable improvement [119].

3.2. Double-gated n-type tungsten diselenide FETs with high-k top gate dielectric.

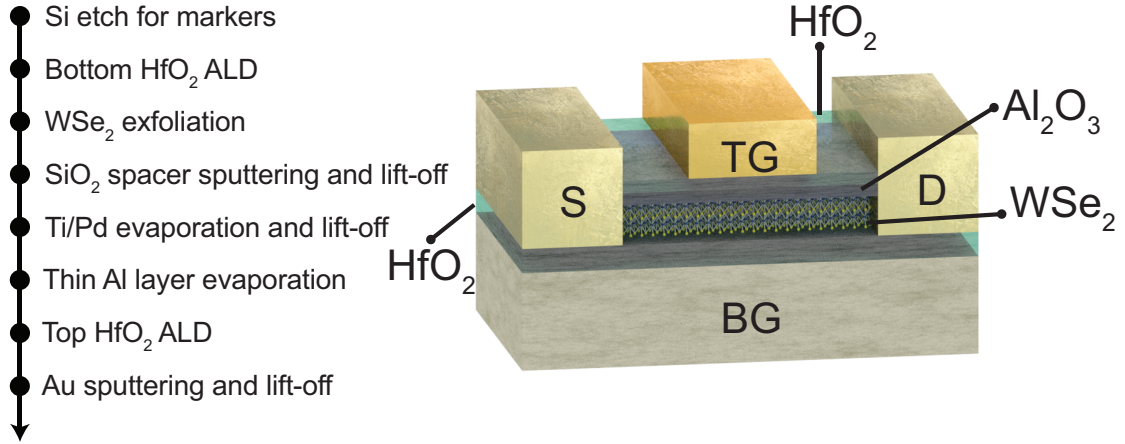


Figure 3.11: Schematic view of the realized double gate devices and summary of the fabrication process flow.

3.2.1 Device Fabrication

The proposed device consists of an asymmetrical double-gated WSe_2 FET, with a common back gate and a top gate overlapping the central part of the semiconducting channel. A schematic of the complete device is shown in Figure 3.11 together with the summary of the proposed process flow. The starting substrate consists of a low resistivity p-doped Silicon wafer. ALD in a BENEQ TFS 200 reactor at 200 °C, using TEMAH and H_2O as precursors was performed to deposit the 10 nm thick HfO_2 layer that serves as back gate dielectric. Next, WSe_2 flakes were mechanically exfoliated starting from a bulk crystal sample (synthesized by *hq graphene*) using the scotch taping technique. Thin flakes of appropriate size were then identified by inspecting the sample with an optical microscope.

Since the back gate is extended over the entire back side of the wafer, if the source and drain contacts were to be deposited directly on the HfO_2 layer the resulting leakage would be considerably larger than the leakage coming from the channel. Consequently, a 50 nm thick SiO_2 film was deposited by sputtering and lift-off on the areas around the flakes so to greatly increase the dielectric thickness between the contact pads and the Si substrate. The source and drain contacts were deposited on the flakes using electron-beam lithography on a PMMA/MMA bilayer resist followed by evaporation and lift-off of a Ti (1.5 nm)/Pd (100 nm) stack. Devices were then completed with the top gate dielectric and metal contact. In order to improve the quality of the dielectric grown on the WSe_2 flake, we deposited a seed layer consisting of 1.5 nm of evaporated Al prior to the ALD step. The Al layer was then oxidized in air to obtain a thin Al_2O_3 film on which 5 nm of HfO_2 were deposited using the same reactor and recipe exploited for the back gate. Finally, the top gate metal was deposited by sputtering and lift-off of a Ni (80 nm)/Au (40 nm) stack after a last EBL step. A colorized SEM image of the complete device is shown in Figure 3.12a. The WSe_2 flakes thickness was measured using AFM in contact mode, as shown in Figure 3.12b. The results reported in the following have been obtained from devices realized with few layers flakes. A detailed representation of each step in the process flow is reported in

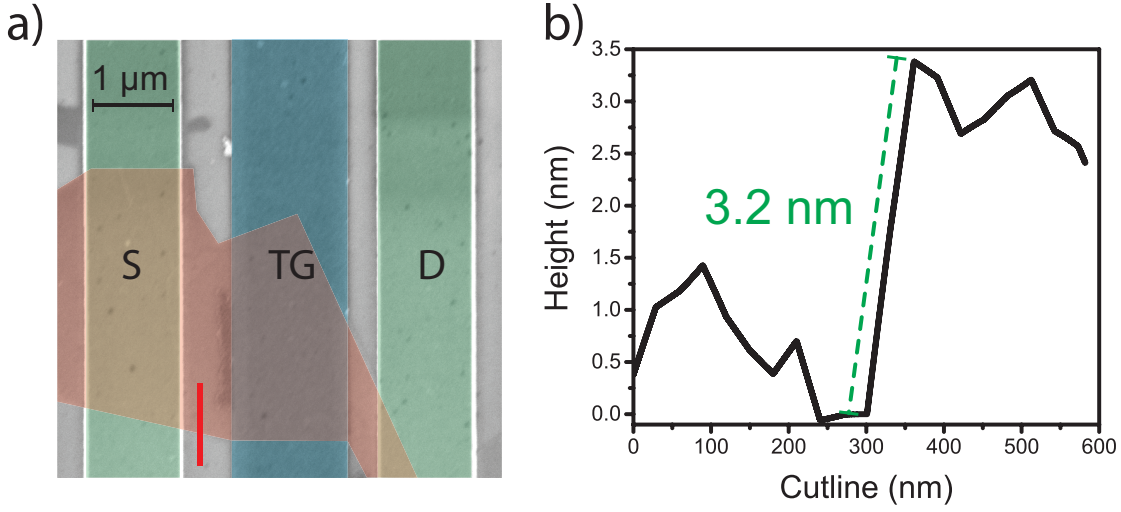


Figure 3.12: a) False colored SEM image of a device after the deposition of the top gate contact. The top gate is extended only over the center of the channel, resulting in a limited control of the ungated regions between the gate and the source/drain contacts. The red line shows the cutline along which the AFM profile in b) was measured. The estimated thickness of the flake is 3.2 nm.

appendix Figure A.2.

3.2.2 Results

All the electrical measurements reported in this section have been performed in EPFL at ambient conditions and room temperature using an HP 4156C semiconductor parameter analyzer on a representative device. We focused our analysis on the electron conduction in the channel to reduce the measurements stress on the device. Therefore, in most measurements the gate bias window is asymmetrical with respect to 0 V. The reported transistor is $2.6 \mu\text{m}$ long and $2 \mu\text{m}$ wide, with a channel thickness of 3.2 nm.

Back gated and top gated transfer characteristic

In order to study the impact of the back and top gates on the WSe_2 channel conductance we measured the double-sweep transfer characteristics and output characteristics sweeping one of the gates potential while maintaining the second at a fixed bias. The results are reported in Figure 3.13. Looking at the two $I_D(V_G)$ curves on a linear scale (back gate in Figure 3.13a, top gate in Figure 3.13c) it is clear that the back gated device behaves as an enhancement mode FETs, while when operated under the top gate control the device operates in depletion mode. The drain current of the top gated FET tends to saturate under positive gate bias because of the reduced control of the top gate on the ungated WSe_2 flake areas close to the source and drain contacts (see Figure 3.12a). The series resistance offered by these regions is set by the fixed bias applied

3.2. Double-gated n-type tungsten diselenide FETs with high-k top gate dielectric.

to the back gate. The hysteresis can be evaluated by comparing the threshold voltage (V_{th}) of the up and down sweeps. The V_{th} value was estimated by the intercept of the linear part of the transfer characteristic curve. As explained in the following, the actual value of the threshold voltage shift between forward and backward sweep is strongly dependent on the gate bias sweep rate (S). The back gated FET exhibits a 272 mV hysteresis when measured with a 5.2 V/s sweep rate. When controlled by the top gate sweep, the device hysteresis is reduced to 70 mV tested sweeping the gate bias at 1 V/s.

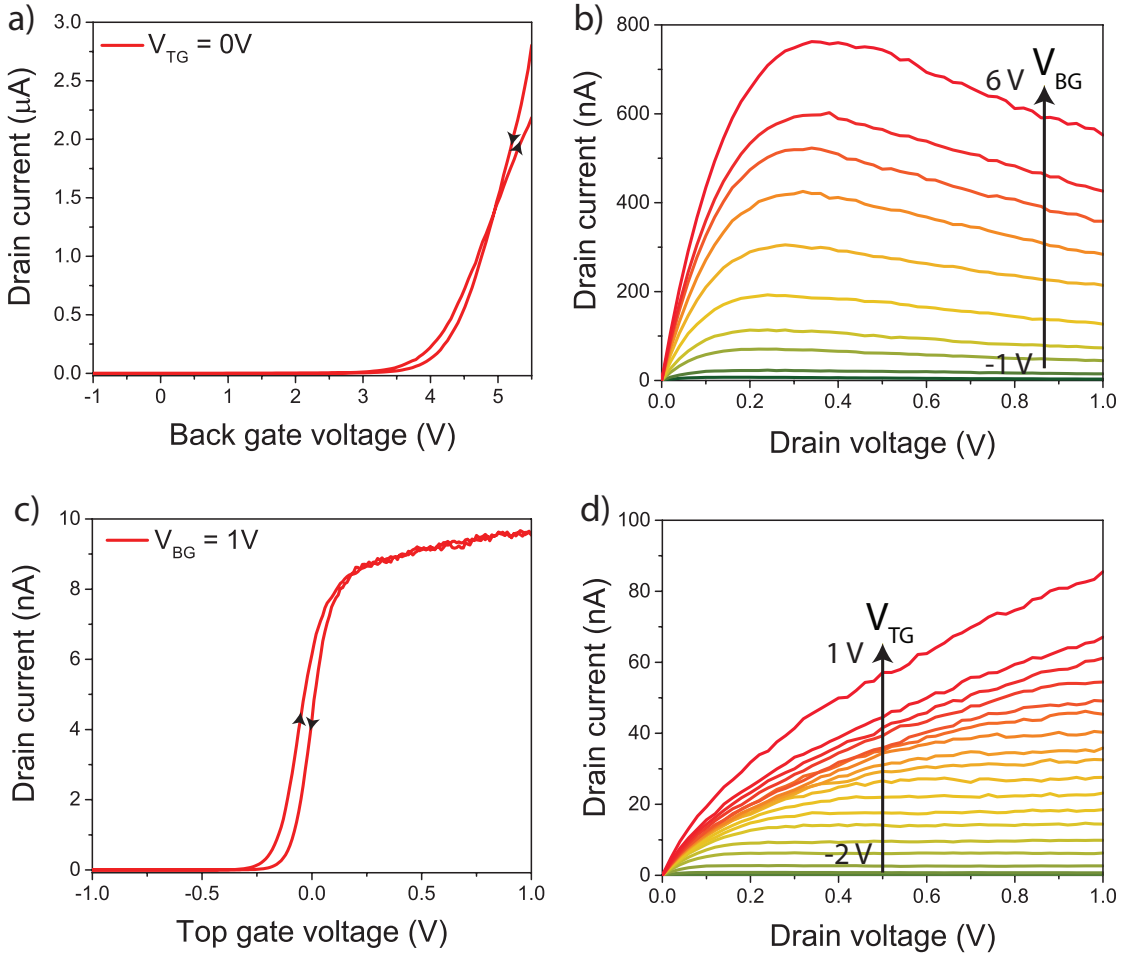


Figure 3.13: Double sweep transfer characteristic and output characteristic of the fabricated WSe₂ FET. a) Double sweep back gate $I_D(V_G)$ curve measured at $V_{DS} = 100$ mV applying 0 V to the top gate. The sweep rate is 5.2 V/s. b) Back gate $I_D(V_D)$ characteristic measured under a top gate bias of -2 V and for back gate bias in the -1/+6 V range. c) Double sweep top gate $I_D(V_G)$ curve measured at $V_{DS} = 100$ mV applying 1 V to the back gate. The top gate sweep rate is 1 V/s. d) Top gate $I_D(V_D)$ characteristic measured under a back gate bias of +3 V and for a top gate bias in the -2/+1 V range.

The back gate output characteristic in Figure 3.13b exhibits current saturation and negative differential resistance is observed at large V_{BG} values, likely because of self-heating effects in the

WSe₂ flake [118]. The $I_D(V_D)$ curve for the top gate FET is reported in Figure 3.13d, and shows how current saturation is achieved for drain biases below 1 V with no evidence of negative differential resistance.

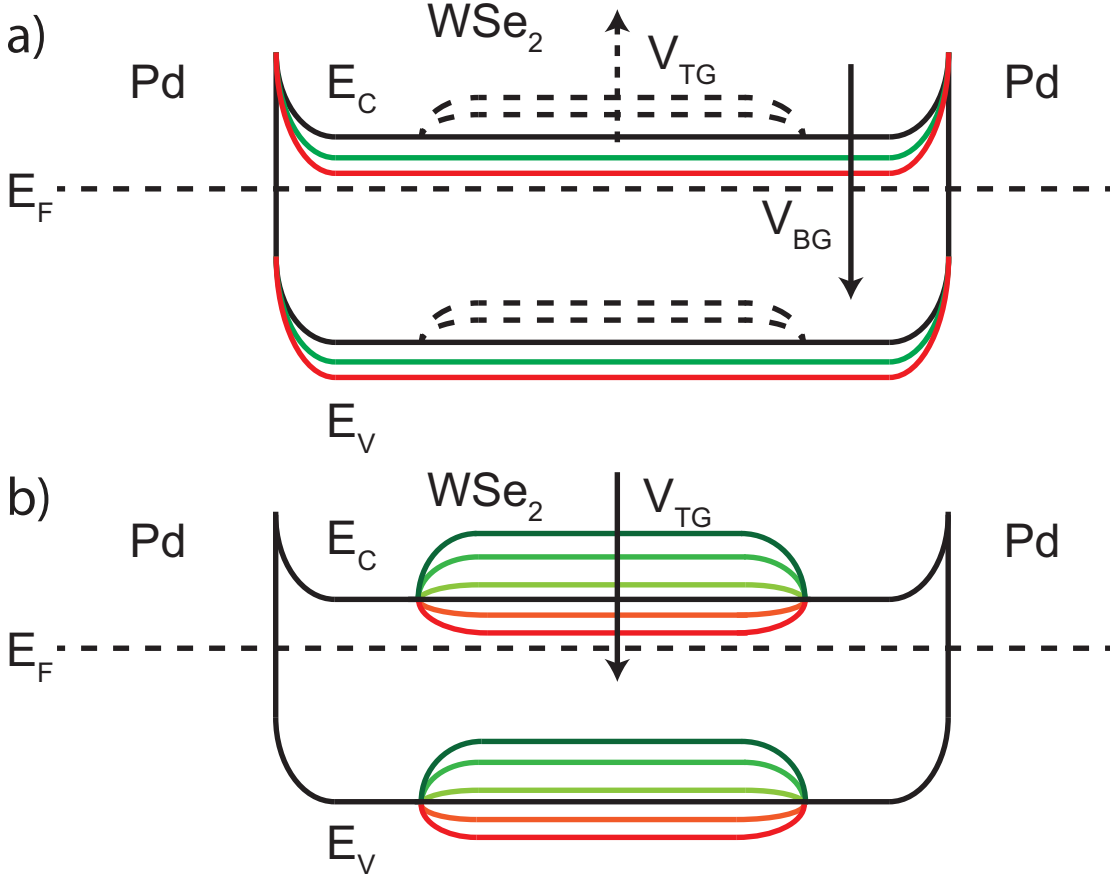


Figure 3.14: Double gated WSe₂ band diagram under a) back gate and b) top gate electrostatic control. The drain to source voltage is assumed to be 0 V.

Figure 3.14 shows the qualitative band diagram of both the back and top gated WSe₂ FET, including the Pd metallic contacts. Under back gate control, a positive bias determines a lowering of the bands in the channel, resulting in a n-type electrostatic doping and an increase of the current. In this configuration, a fixed bias applied to the top gate affects the center of the channel, contributing to its depletion or accumulation (dotted curves in Figure 3.14a). When operated using the top gate, the WSe₂ FET can be set to be normally ON by applying a fixed positive bias to the back gate. By sweeping the top gate voltage towards negative values, the central part of the channel is gradually depleted of electrons and the transistor can be turned OFF. Conversely, setting the top gate bias at positive values, the electron density in the gated section of the channel increases. However, the limited electrostatic control on the ungated sections of the channel determines the already discussed drain current saturation for large top gate voltages (see Figure 3.13c).

3.2. Double-gated n-type tungsten diselenide FETs with high-k top gate dielectric.

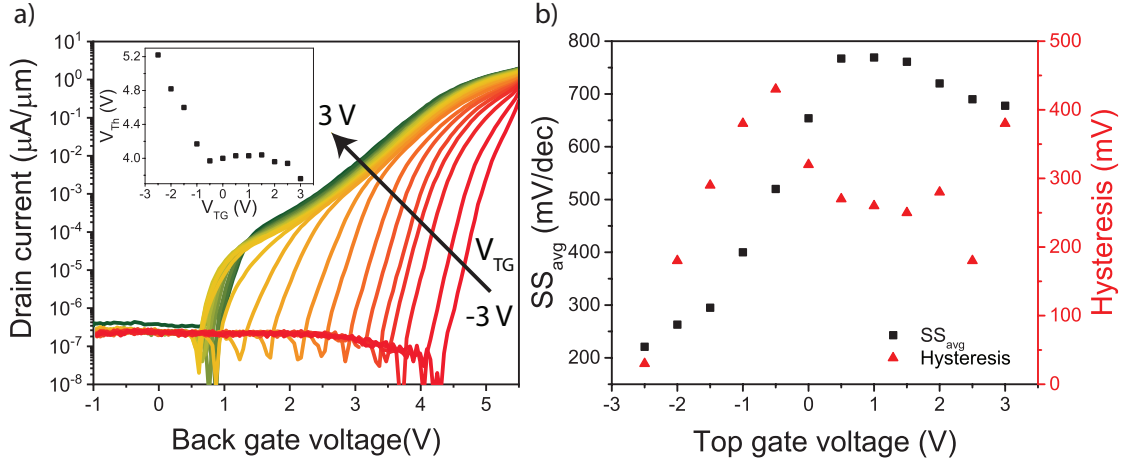


Figure 3.15: a) Normalized transfer characteristic of the back gated FET under different top gate biases, in the ± 3 V range. Inset: evolution of the threshold voltage as a function of V_{TG} . b) Negative top gate biases result in a decrease of both the average subthreshold slope and the hysteresis. All the measurements were performed at $V_{DS} = 100$ mV and sweeping the back gate bias at 5.2 V/s.

Impact of top gate bias on back gated FET characteristic

In order to study the impact of the top gate bias on the back gated device conduction, we measured the back gate transfer characteristic under different fixed top gate voltages V_{TG} in the ± 3 V/ ± 3 V bias window, applying a drain bias of 100 mV. The results are shown in Figure 3.15, while Figure 3.16 shows a qualitative depiction of the impact of V_{TG} values on the channel conduction. Sweeping the top gate bias from positive to negative values determines a positive shift of the threshold voltage (inset of Figure 3.15a). A positive V_{TG} favors the accumulation of electrons under the top gate. As shown in Figure 3.16a, two channels can contribute to the conduction in the flake: the top one constituted by accumulated electrons while the back one is an inversion channel controlled mainly by the back gate. The resulting subthreshold current shows two different slopes, corresponding to the onset of these two conduction paths. The back gate threshold voltage saturates under positive bias being limited by the potential required to electrostatically dope the flake area not covered by the top gate. Under negative top gate bias, corresponding to the situation presented in Figure 3.16b, the WSe_2 area below the top gate is fully depleted of electrons and only the inversion channel formed by the back gate dictates the conduction in the flake. This mechanism translates in a unique and steeper subthreshold slope as well as the expected positive shift of the threshold voltage.

The I_{ON}/I_{OFF} current ratio remains larger than 6 orders of magnitude for all the top gate bias values investigated, despite a small decrease in I_{ON} observed for negative V_{TG} biases. The OFF state current is limited by the back gate leakage, which remains below $0.5 \text{ pA}/\mu\text{m}$ for all the measurements reported thanks to the mentioned SiO_2 layer deposited below the source and drain contact pads. Moreover, a clear increase of the steepness of the subthreshold current is observed, as reported in other implementations of double-gated WSe_2 FETs. Figure 3.15b summarizes the evolution of both the average subthreshold slope over 5 orders of magnitude of the output current

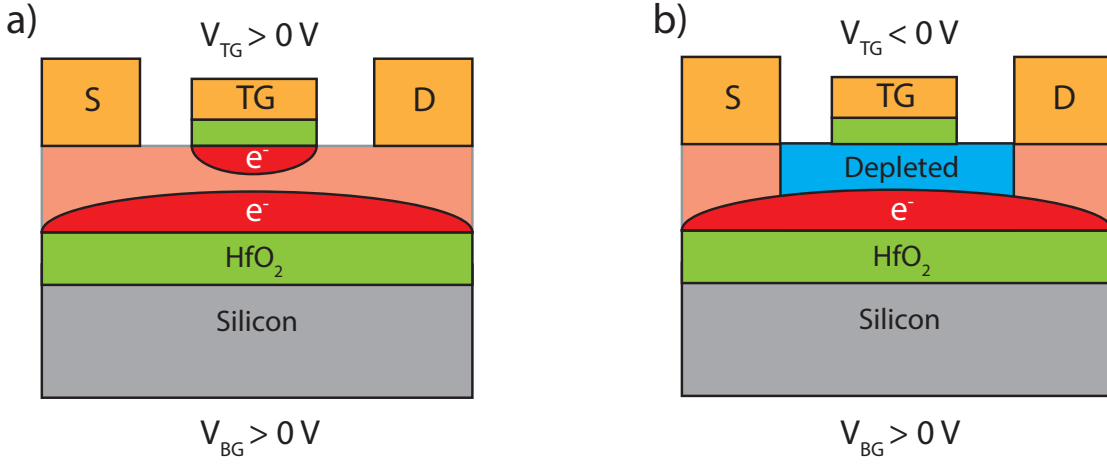


Figure 3.16: a) Impact of positive fixed top gate bias on the back gated WSe₂ FET transfer characteristic. Two channels can be formed resulting in two different slopes observed in the $I_D(V_G)$ curve. b) Impact of negative fixed top gate bias on the back gated WSe₂ FET transfer characteristic.

and the back gate hysteresis with the applied bias to the top gate.

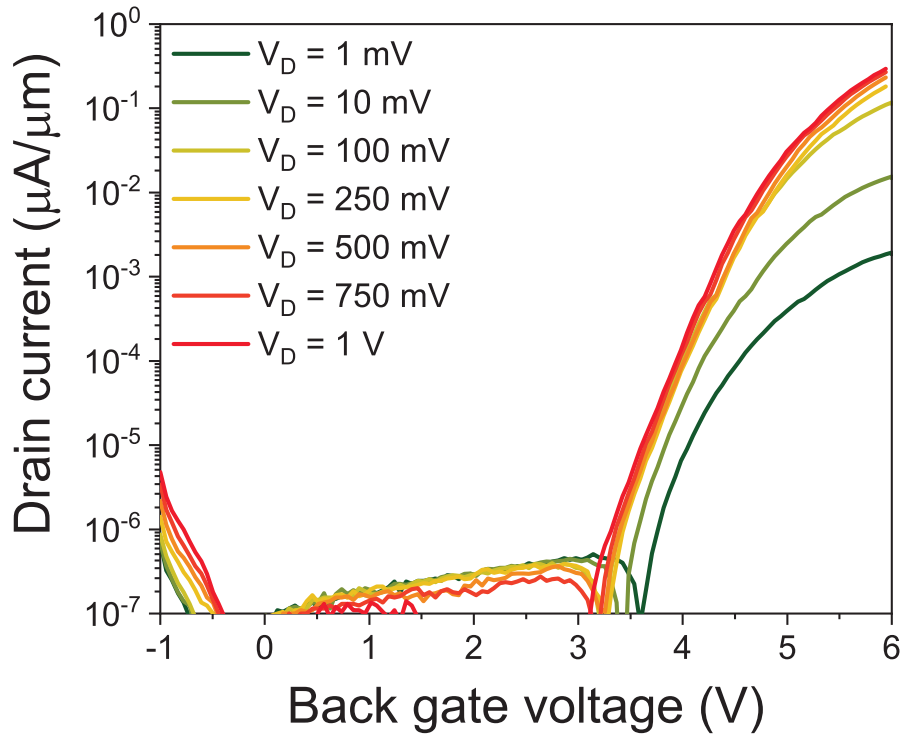


Figure 3.17: Normalized transfer characteristic $I_D(V_G)$ of the back gated FET at different V_{DS} biases in semilog scale, measured with $V_{TG} = -2$ V. For drain voltages larger than 100 mV, the device exhibits a I_{ON}/I_{OFF} ratio larger than 6 orders of magnitude. The average subthreshold slope does not vary significantly with respect to the drain bias.

3.2. Double-gated n-type tungsten diselenide FETs with high-k top gate dielectric.

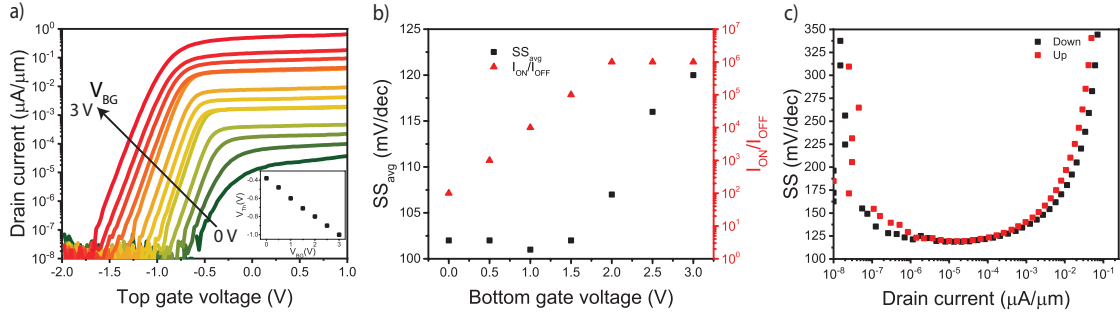


Figure 3.18: a) Normalized transfer characteristic of the top gated device under different back gate voltages in the 0/+3 V bias range measured at $V_{DS} = 100$ mV. Inset: threshold voltage as a function of the applied V_{BG} . b) I_{ON}/I_{OFF} ratio and average subthreshold slope over four orders of magnitude of the output current as a function of V_{BG} . c) Subthreshold slope as a function of the drain current for both the upward and downward cycles, measured applying $V_{BG} = 3$ V and $V_{DS} = 100$ mV. A good match is observed between the two sweeps, with a minimum SS below 125 mV/dec. All these results have been obtained sweeping the top gate bias at 2.4 V/s.

We report in Figure 3.17 the normalized back gated transfer characteristic measured at different values of the drain-to-source bias and with $V_{TG} = -2$ V. For drain voltages larger than 100 mV, the I_{ON}/I_{OFF} ratio exceeds six orders of magnitude, while the average subthreshold slope does not vary significantly with the drain bias.

Impact of back gate bias on the top gated FET

In order to study the impact of the back gate bias on the top gated device, we measured the top gate transfer characteristic under different back gate voltages V_{BG} in the 0 V/+3 V bias window, applying a drain bias of 100 mV. The results are shown in Figure 3.18, while Figure 3.19 shows a qualitative depiction of the impact of V_{TG} values on the channel conduction. The increase of the back gate bias determines a negative shift of the top gated FET threshold and a clear increase of the I_{ON}/I_{OFF} ratio. The top gate leakage current remains below 50 fA/ μm for all the reported measurements. Positive V_{BG} values determine an n-type electrostatic doping of the entire WSe_2 channel that can be then depleted of electrons in the central section by applying a negative bias to the top gate. The inset of Figure 3.18a shows how the threshold voltage decreases linearly with the increase of the back gate bias, with an extracted -0.2 V shift for applied volt to the back gate. The evolution of both the average subthreshold slope and the I_{ON}/I_{OFF} ratio is reported in Figure 3.18b. For back gate biases larger than 2 V, the ON/OFF current ratio exceeds 6 orders of magnitude, and the top gated FET reaches performance equivalent to the back gated device while maintaining a steeper turn-on characteristic. The average subthreshold slope over 4 orders of magnitude of the output current reaches values close to 100 mV/dec, and degrades only slightly with the increase of the back gate bias. Figure 3.18c shows the subthreshold slope as a function of the drain current for both the upward and the downward voltage sweeps, measured under $V_{BG}=3$ V and $V_{DS}=100$ mV. The extracted top gate SS is quite independent from the direction of the top gate bias sweep.

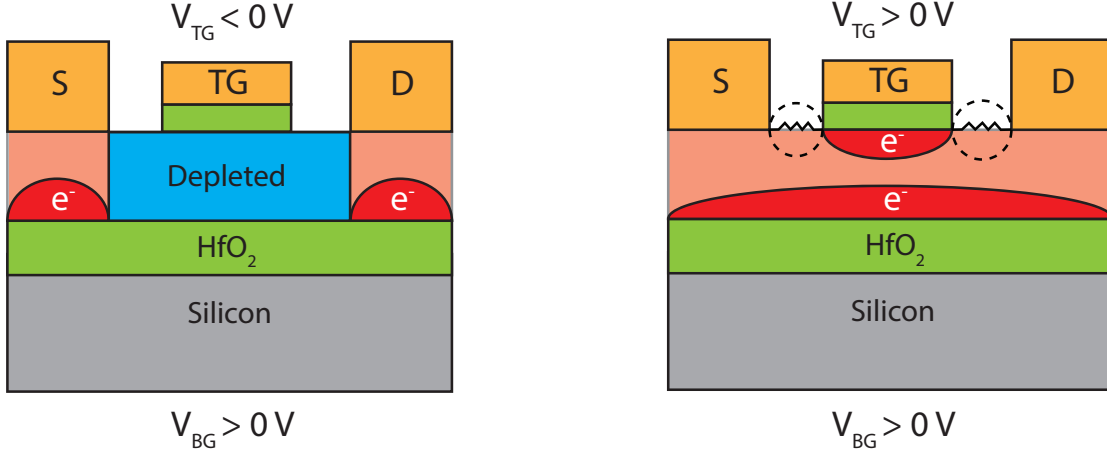


Figure 3.19: Under positive bottom gated bias, the channel is normally n-doped. a) Negative top gate voltages allow to switch off the WSe₂ FET by depleting the central section of the channel. b) Conversely, under positive top gate bias the electrons are free to flow between source and drain. The observed saturation of the output current is due to the resistance offered by the ungated sections of the channel.

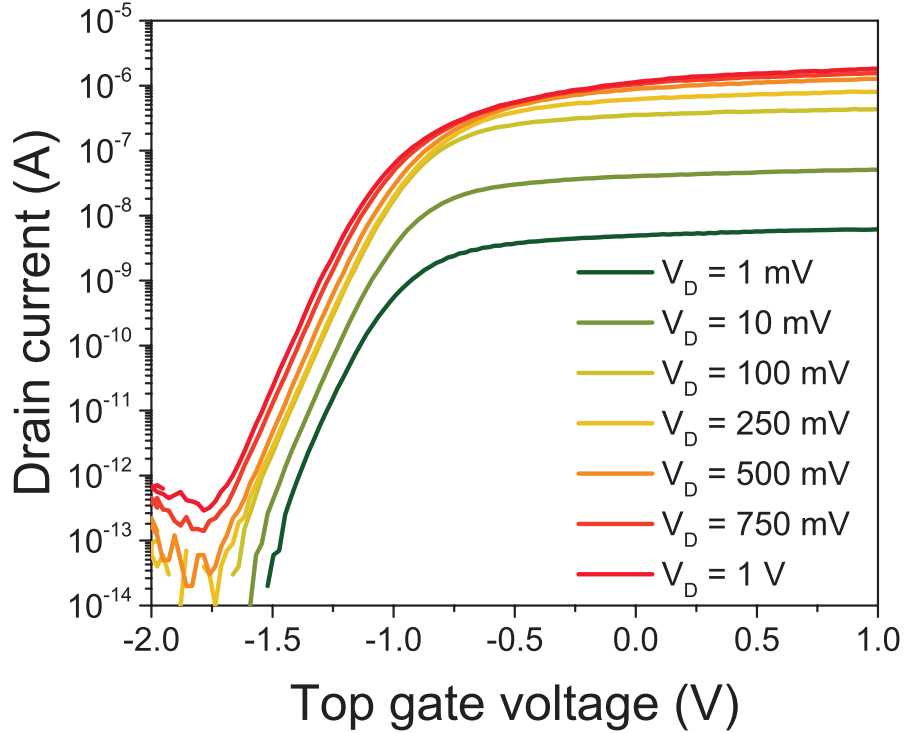


Figure 3.20: Normalized transfer characteristic $I_D(V_G)$ of the top gated FET at different drain-to-source biases on the semi-log scale, measured at $V_{BG} = 3$ V. For drain voltages larger than 100 mV, the device exhibits a I_{ON}/I_{OFF} ratio larger than 6 orders of magnitude.

3.2. Double-gated n-type tungsten diselenide FETs with high-k top gate dielectric.

In Figure 3.20 we show the top gated normalized transfer characteristic measured under increasing values of the drain-to-source bias and applying a 3 V back gate voltage. Similarly to what was observed for the back gated characteristic, a drain voltage of 100 mV is sufficient to obtain an ON/OFF current ratio larger than 10_6 . Remarkably, the average subthreshold slope is not affected by the increase of V_{DS} .

Field effect mobility extraction

We extracted the two-terminal top gate effective field effect mobility μ_{FE} using equation 3.1. Also for these devices, the dielectric capacitance per unit area C_{ox} has been directly measured by characterizing MIM structures included on the same wafer of the devices. The obtained electron mobility at $V_{DS} = 1$ mV and $V_{BG} = 3$ V is $10.74 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$.

In order to obtain a more accurate estimation of the carriers' mobility by decoupling part of the impact of the contact resistance, we applied the Y function method as discussed previously. Figure 3.21 shows the extracted Y function for the reported top-gated FET, obtained with $V_{DS} = 1$ mV and $V_{BG} = 3$ V. From the fitting of the linear region, in red in the figure, it is possible to extract the low field electron mobility (see equation 3.3), estimated to be $22.15 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$, in line with the two-terminals mobility reported in other works on WSe_2 FETs [46, 47, 116, 117].

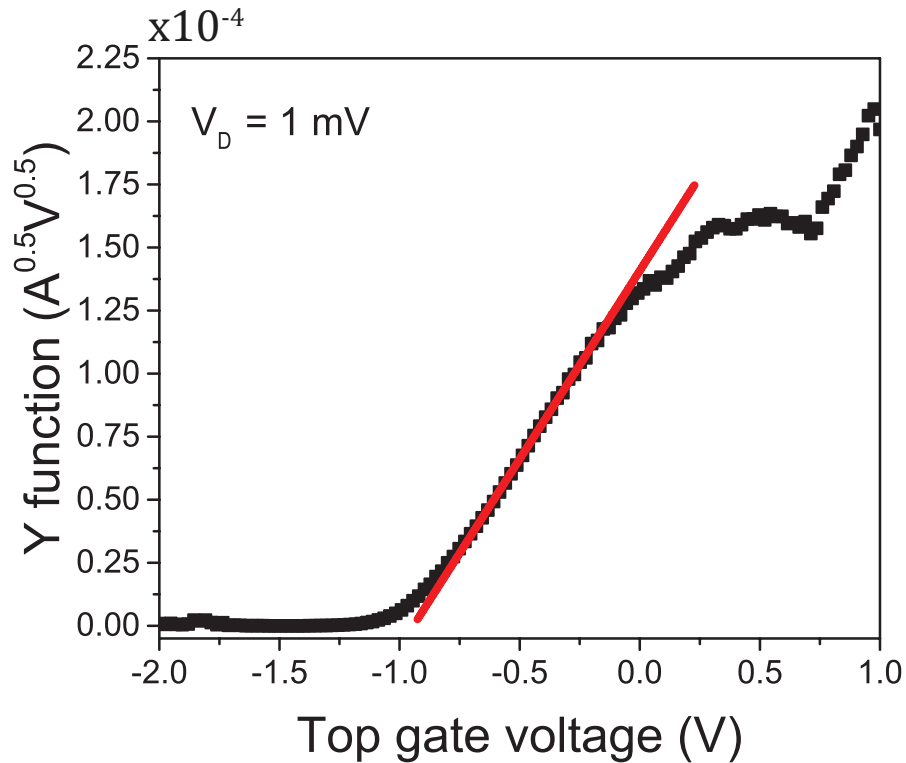


Figure 3.21: Extracted Y function vs top gate voltage for the top gated FET at $V_{DS} = 1$ mV and $V_{BG} = 3$ V. The mobility can be extracted from the fitting of the linear part of the curve, shown in red in the figure.

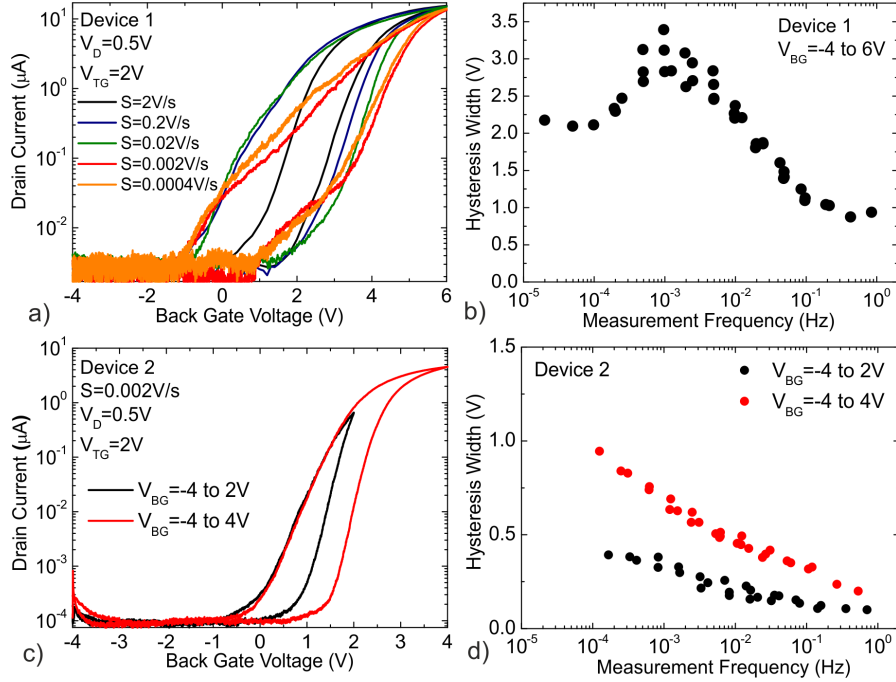


Figure 3.22: a) The back gate transfer characteristics of the Device 1 measured using different sweep rates. b) The corresponding $\Delta V_{\text{H}}(f)$ dependence exhibits a maximum. c) The back gate transfer characteristics of the Device 2 measured using very slow sweep rates and different sweep ranges. d) The corresponding $\Delta V_{\text{H}}(f)$ dependences exhibit an increase of the hysteresis for slower sweeps.

Hysteresis Dynamics

Finally, we performed a detailed study of the hysteresis dynamics in our devices by measuring the gate transfer characteristics using different sweep rates and, consequently, sweep times t_{sw} . The results presented in this section have been obtained at TU Wien measuring under vacuum conditions. Two few-layers representative devices were tested, indicated in the following as Device 1 and Device 2. In order to correctly represent our results, we extract the hysteresis width ΔV_{H} near the threshold voltage and plot it versus the measurement frequency $f = 1/t_{\text{sw}}$.

In Figure 3.22 we show that the dynamics of hysteresis observed on the back gate transfer characteristics can be different for different devices. For instance, Device 1 exhibits some saturation in the hysteresis for very slow sweeps (Figure 3.22a), which leads to a clear maximum of the $\Delta V_{\text{H}}(f)$ dependence (Figure 3.22b). This behavior is very similar to our predictions and means that a considerable number of oxide defects contributing to the hysteresis have enough time to become charged during the slow sweeps [120]. The latter also affects the shape of the gate transfer characteristics, as we see in Figure 3.22a. In contrast, for the Device 2 (Figure 3.22 c,d) we observe an increase of the hysteresis width for slow sweeps, while the maximum is not reached. At the same time, the hysteresis becomes larger for wider sweep ranges, which indicates that a larger amount of oxide defects comes into play [121].

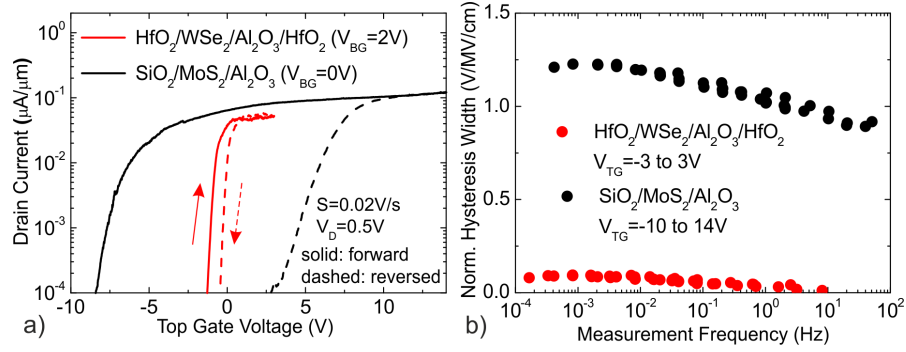


Figure 3.23: a) Comparison of the top gate transfer characteristics for our devices and their counterparts with MoS₂ channel and Al₂O₃ (23.5 nm) top gate insulator. The current is normalized by the channel width. b) When normalizing ΔV_H to the oxide field factor, the hysteresis in our devices appears considerably smaller.

In Figure 3.22a we show the hysteresis on the top gate transfer characteristics of our devices and CVD-grown MoS₂ FETs with 23.5 nm thick Al₂O₃ as a top gate insulator reported in our previous work [121]. For a proper comparison of the hysteresis in different technologies, we normalize ΔV_H by the oxide field factor $K=\Delta V/d_{ox}$, where ΔV is the sweep range width and d_{ox} is the oxide thickness. Thus, in Figure 3.22b we show that in our devices with scaled top gate insulator the hysteresis is over an order of magnitude smaller. At the same time, the dependence versus the measurement frequency is similar in both cases, which suggests that the hysteresis is caused by similar oxide defects in Al₂O₃ which present a fundamental property of this material.

3.3 Summary

In summary, we have demonstrated double gated n-type WSe₂ FETs with excellent high-k top gate dielectric obtained combining an evaporated and oxidized thin Al₂O₃ seed layer and the ALD of a 5 nm thick HfO₂ film. The resulting device can be controlled by either the top or the back gate, using the opposite gate to finely tune the FET performance. When back gated, the device behaves as an enhancement FET, whose hysteresis and subthreshold slope can be greatly improved by applying a negative voltage to the top gate. An average subthreshold slope close to 200 mV/dec has been achieved. Conversely, the top gated transistor works in depletion, and the back gate bias can be exploited to enhance the ON/OFF current ratio and shift the threshold voltage. As a result, the device exhibits an I_{ON}/I_{OFF} ratio larger than 10⁶ and an average subthreshold slope approaching 100 mV/dec, which is independent from the drain bias. Both the top and the back gate are characterized by a leakage current below 0.5 pA/μm in all the reported electrical measurements. Finally, the hysteresis of the top gate transfer characteristics is considerably improved compared to previously reported top-gated MoS₂ FETs with thicker Al₂O₃ insulator [120].

We believe that the proposed approach for the deposition of high-k dielectrics on WSe₂ provides a promising path for the development of high performance top-gated FETs. Given the small leakage current measured, the dielectric stack could be subject to a further scaling of the HfO₂ layer

thickness while seed layers with better dielectric performance than Al_2O_3 could contribute to an enhanced top gate control and reduced double sweep hysteresis. An improvement of the drive current and ON/OFF current ratio requires the reduction of the contact resistance, achievable by an annealing of the contacts prior to the deposition of the top gate dielectric.

4 | 2D/3D Heterojunction devices

This chapter presents the properties and potential applications of mixed dimensionality VO_2/MoS_2 heterojunctions. A brief overview of the peculiar properties of VO_2 is offered together with the electrical characteristic of two terminal devices realized with this functional oxide. Moreover, the circuit configurations proposed to realize steep slope FETs including a vanadium dioxide resistor [28, 29] are discussed. The fabrication and electrical characterization of VO_2/MoS_2 is presented in detail, focusing on the excellent rectification characteristic of two terminal devices and the impact of the temperature on the IV curve. A tunable photoresponsivity photodiode is characterized, providing insight about the light absorption at the interface between MoS_2 and VO_2 in both its insulating and metallic phase. Finally, the electrical characteristic of gated heterojunctions is discussed, highlighting how such a system represents a stepping stone towards truly effective, field modulated VO_2 devices. The content of this chapter is based on the work presented in [29, 122, 123].

4.1 Vanadium dioxide

Metal-insulator transition (MIT or IMT for the reverse transition) in functional oxides has been a topic of interest in solid state physics and electronics since the 1950s, when F.J. Morin reported that in some vanadium and titanium oxides, such as vanadium monoxide (VO), dioxide (VO_2), sesquioxide (V_2O_3) and titanium sesquioxide (Ti_2O_3), the resistivity sharply increases of several order of magnitude when the temperature is decreased below a certain transition temperature (T_{MIT}) [124].

Several other oxides exhibiting a metal to insulator transition have been since discovered and reported in literature. Figure 4.1 shows a collection of such functional oxides and the relative phase transition temperature [125].

The vanadium-oxide system is of particular interest in the transition metal oxides (TMO) family. There are several stable vanadium oxide phases in addition to VO_2 , as shown in the phase diagram for the vanadium oxygen system in Figure 4.2. Many of these exhibit a MIT such as V_2O_3 or V_3O_5 , while others such as VO or V_2O_5 [127] do not. Table 4.1 reports the most common vanadium oxides phases with the relative transition temperatures. The resistivity reconfiguration in function of temperature, i.e. the resistivity jump observed in correspondence of the phase transition, for the vanadium oxides exhibiting MIT is shown in Figure 4.3. The best reconfigurability

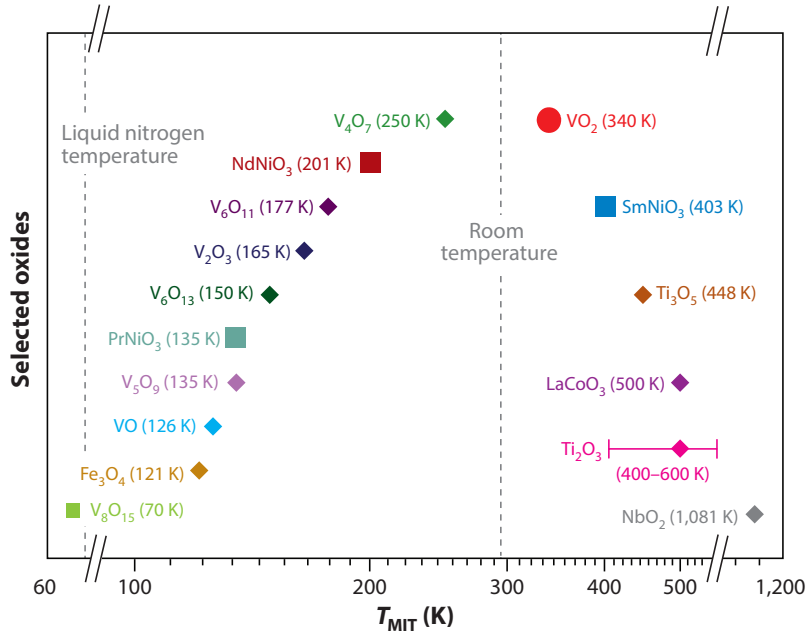


Figure 4.1: Metal insulator transition temperatures in bulk crystals of some selected oxides. Adapted from [125].

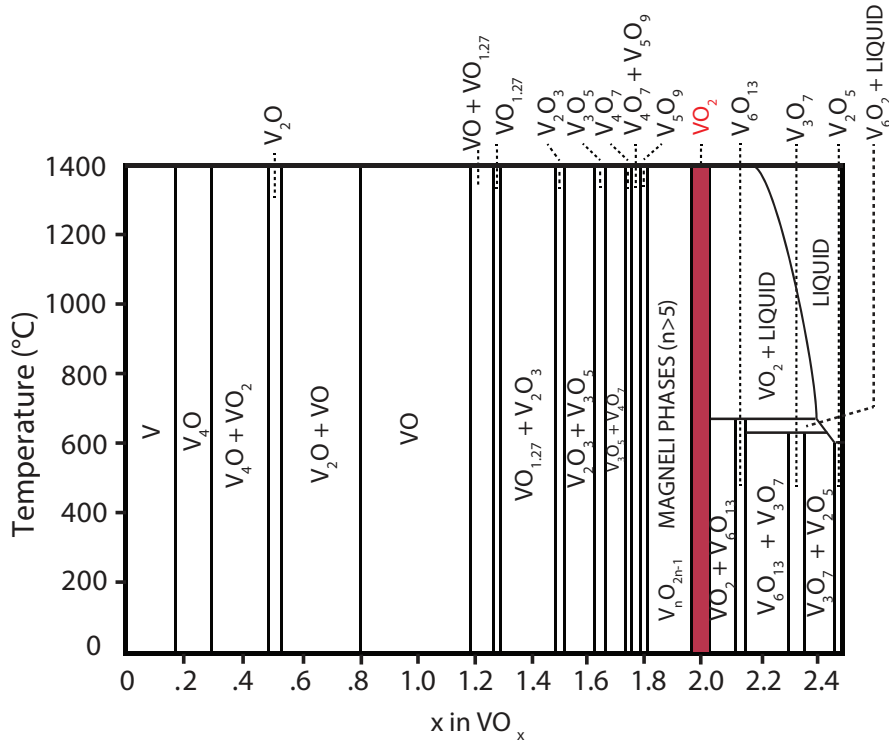


Figure 4.2: Phase diagram of the vanadium-oxygen system. Adapted from [126].

Oxide	T_{MIT} (K)	Conductivity jump at T_{MIT}
VO	-	Metal
V ₂ O ₃	150	10^7 - 10^{10}
V ₃ O ₅	450	10^2
V ₄ O ₇	240	10^3
V ₅ O ₉	130	10^6
V ₆ O ₁₁	170	10^4
V ₇ O ₁₃	-	Metal
V ₈ O ₁₅	70	10^1
VO ₂	340	10^5
V ₆ O ₁₃	150	10^6
V ₂ O ₅	-	Insulator, E_g 2.5 eV

Table 4.1: Vanadium Oxides with respective transition temperature [124, 127–129].

is offered by V₂O₃, that can reach a contrast of up to 10^{10} . However, the MIT temperature of this oxide is fixed at 150 K, well below ambient condition. Its applications for electronic devices are therefore quite limited.

In the vanadium oxides family, VO₂ is of particular interest because of its transition temperature conveniently placed just above ambient temperature (340 K). Below T_{MIT} , VO₂ presents a monoclinic insulating phase with a energy gap $E_g \sim 0.6$ - 0.7 eV in the 3d orbital bands (Figure 4.4). Increasing temperature above T_{MIT} the crystal structure changes to tetragonal rutile. This transition is associated to the collapse of the energy gap and a resulting increase of the electron density in VO₂ conduction band. As a result, the conductivity vs temperature curve present jumps of up to five orders of magnitude separated by an hysteresis window of about 2 K in crystal bulk samples [125, 127]. The magnitude of the resistivity reconfiguration, the transition temperature and the amplitude of the temperature hysteresis window are good indicators to evaluate the quality of the material in terms of stoichiometry and crystallinity.

The physical mechanism responsible for the triggering of the insulator to metal transition in VO₂ has been a subject of intense discussion in the scientific community. The changes in the crystal structure at the critical temperature, that cause a doubling of the unit cell period, could be treated in terms of Peierls transition. Several direct experiments which point out, for instance, the pressure dependency of T_{MIT} [130], suggest an important role played by phonons in the MIT mechanism. On the other hand, effects associated with electronic correlation typical of Mott type transitions are observed in both semiconducting and metallic phases of VO₂ [131]. While this debate might seem an academic problem for condensed matter physicists, it is nevertheless an issue of fundamental importance to assert the feasibility of a VO₂-based Mott-FET. A pure Peierls behaviour would prevent any type of direct electrostatic control on the onset of the MIT mechanism, and therefore exclude the possibility of realizing effective VO₂ field effect devices.

VO₂ insulator to metal transition (IMT) can be induced by thermal, electrical, magnetic or optical excitations and is typically hysteretic [29, 30, 132]. Noticeably, the electrically induced phase transition results in an extremely steep drop of the resistivity.

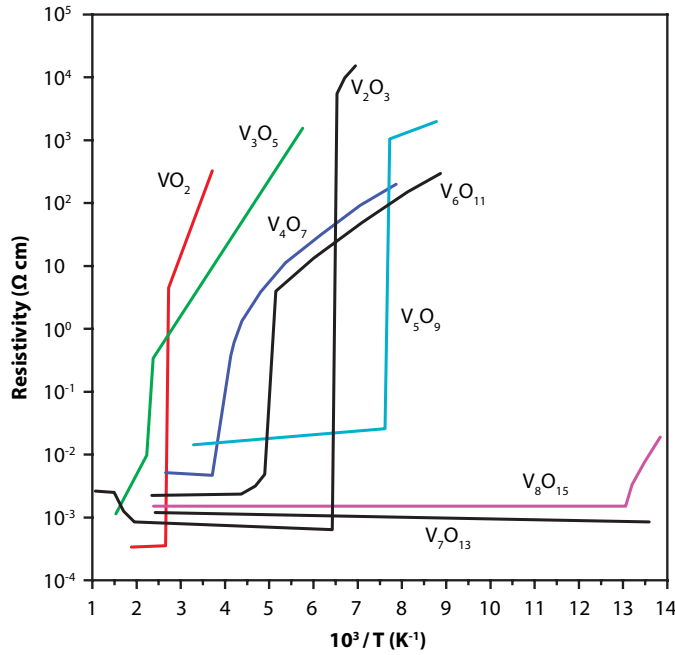


Figure 4.3: Metal insulator transitions in different vanadium oxides phases. Adapted from [127].

4.1.1 VO₂ deposition techniques.

The performance and reliability of VO₂ based devices strongly depends on the deposition strategy and the selected substrate. The main deposition techniques reported in literature are:

- **Magnetron sputtering:** VO₂ films are deposited using either DC or RF sputtering of pure Vanadium target, or RF sputtering of VO₂ or other Vanadium oxides [122, 133, 134]. In order to obtain the right stoichiometry, temperature and oxygen pressure are fundamental parameters. Thanks to the possibility of cosputtering different targets at the same time, it is possible to obtain doped VO₂ films [135].
- **Pulsed Laser Deposition (PLD):** A physical vapor deposition (PVD) technique based on a high-power pulsed laser beam ablating the target to be deposited on the substrate. The high power reached by the beam allows to locally vaporize the target. By controlling the vacuum level, the partial reactive gas pressures and the substrate temperature it is possible to control the stoichiometry of the obtained films. Despite being a relatively new technology, still not established in the microelectronics industry, it has gained lot of interest in particular for the deposition of oxides. VO₂ deposition can be obtained starting either from a V, V₂O₃, V₂O₅ or VO₂ target. The low temperature deposition of VO₂ with this technique has been recently reported, paving the way for the fabrication of CMOS compatible VO₂ devices [126, 133, 136].

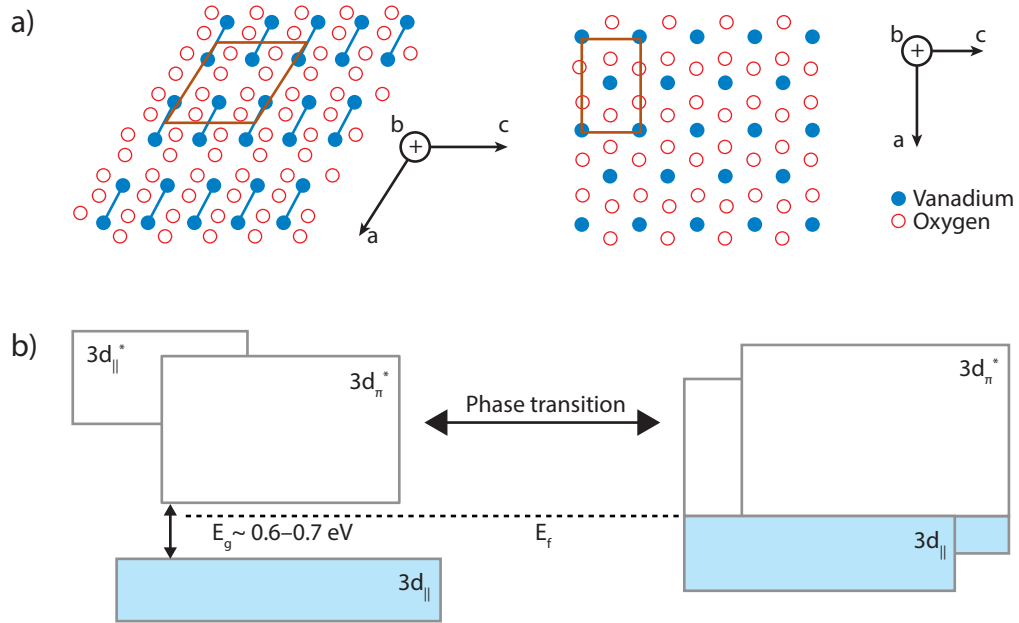


Figure 4.4: a) Cross-sectional view of the IMT structural change of VO_2 from monoclinic insulating phase to tetragonal rutile metallic phase and b) associated band structure change and band gap collapsing. Adapted from [125].

- **Chemical Vaport Deposition (CVD):** Based on the reaction and deposition of gaseous reactants on the substrate. This is the first technique explored for bulk VO_2 synthesis and for thin film deposition. CVD allows as well the doping of VO_2 , and large area deposition for coating of large surfaces has been demonstrated [137–139].
- **Evaporation:** A PVD technique based on the evaporation of a target obtained by either Joule heating of the holding crucible or by focusing a high current electron beam on the material. Introducing reactive species in the vacuum chamber it is possible to control the final film stoichiometry [140–142].
- **Atomic Layer Deposition (ALD):** a particular CVD technique based on sequential pulses of two gaseous volatile precursors which react with the surface of the substrate in a self-limiting process. ALD provides a complete conformality and an extremely precise control of the film thickness, since the deposition is realized practically atomic layer by atomic layer [143, 144].
- **Sol-Gel process:** based on spin coating of a colloidal solution on the substrate, which is then converted thermally into a solid material [145–147].

The phase transition properties of VO_2 strongly depends on the quality of the deposited films, in particular on the final crystallinity and strain. In order to approach bulk VO_2 characteristics, epitaxial depositions are fundamental. Hetero epitaxy of vanadium dioxide requires substrates with good lattice constant match and similar thermal expansion coefficients. Epitaxial

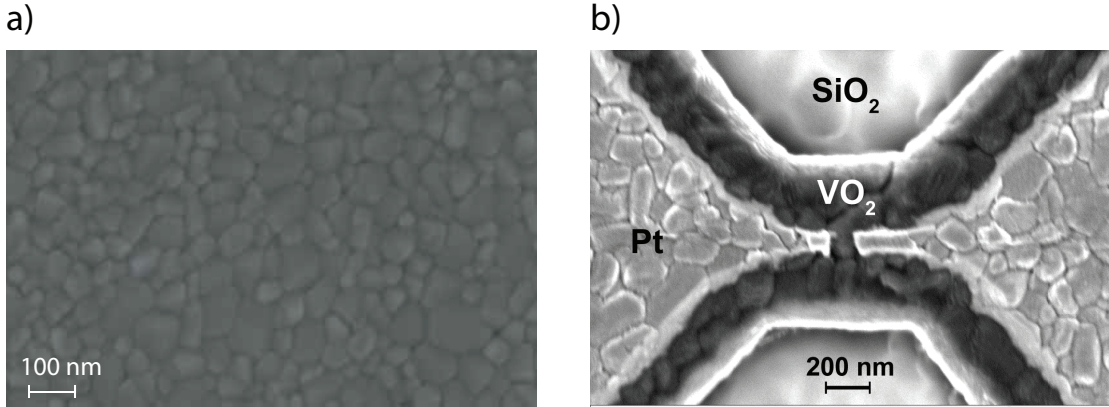


Figure 4.5: a) SEM image of a sputtered 75 nm thick VO_2 film. b) SEM image of a VO_2 two terminals switch fabricated etching by IBE the VO_2 film and depositing by evaporation and lift-off Pt contacts. Adapted from [126].

VO_2 has been demonstrated on titanium dioxide (TiO_2), sapphire (Al_2O_3) and magnesium fluoride (MgF_2) [148–153]. The best performance for thin film VO_2 samples have been obtained by epitaxy on sapphire, with resistivity ratio close to the five orders of magnitude exhibited in the bulk crystal and hysteresis windows as narrow as 2 K [133].

However, in order to demonstrate CMOS compatible devices, VO_2 layers must be grown on either Si or SiO_2 films, whose lattice mismatches with respect to crystalline vanadium dioxide prevent an epitaxial growth. Polycrystalline VO_2 films with reproducible electrical and thermal IMT and up to three orders of magnitude of resistivity reconfigurability can be deposited with various techniques on Si and SiO_2 [126]. An example of a 75 nm thick VO_2 film deposited on SiO_2 in EPFL is reported in Figure 4.5, that collects both an SEM image of the pristine functional oxide and a second image of a complete two terminal device, obtained by patterning VO_2 by IBE and evaporating and lifting-off Pt contacts.

4.1.2 VO_2 two terminal devices.

The thermal and electrical switching of VO_2 planar structures has been investigated since the discovery of the IMT in this material. A typical VO_2 switch structure fabricated at EPFL micro-fabrication facility (CMi) is reported in Figure 4.6. VO_2 layers are deposited by either magnetron sputtering or PLD on SiO_2 capped silicon wafers. Electron beam lithography is performed on MMA/PMMA resist bilayer to deposit by lift-off in acetone Pt metal contacts. A second ebeam lithography step on nLOF negative resist provides a soft mask for the subsequent etching step. VO_2 can be etched with either dry, wet or physical approach [140, 154, 155]. The device shown in Figure 4.6a was obtained by removing the oxide portion not protected by the resist exploiting ion beam etching (IBE). The IV characteristic measured at room temperature is shown in Figure 4.6b: a steep, hysteretic electrically induced phase transition corresponding to a sudden variation of the resistivity is clearly observed.

The actual electrical power required to induce the electrical IMT in a switch depends on both

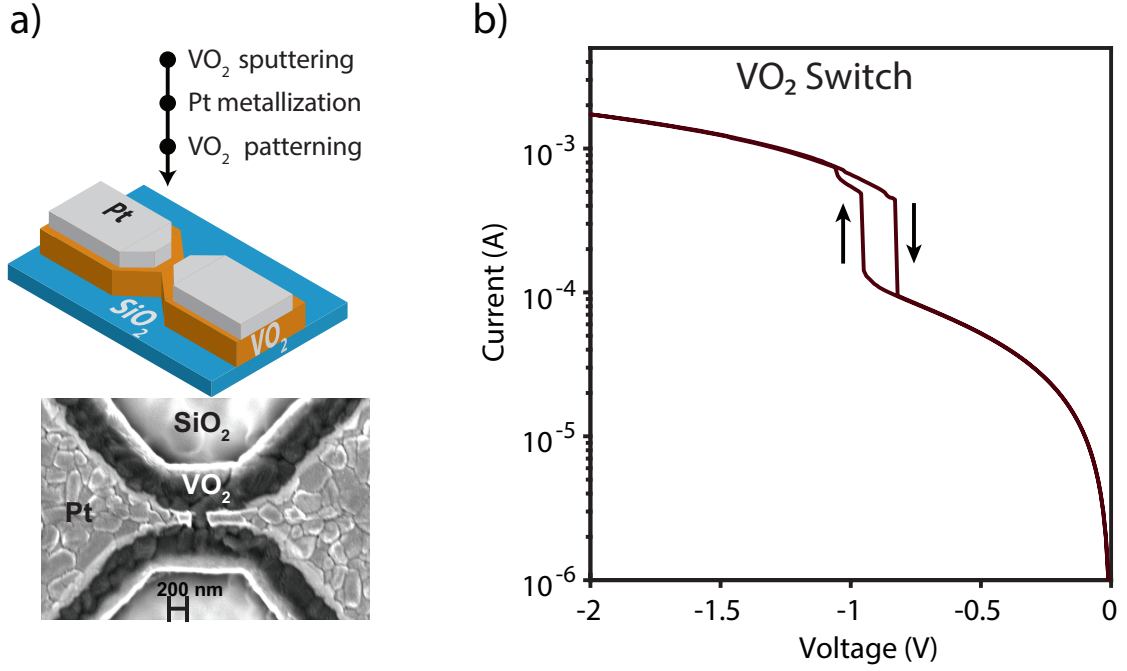


Figure 4.6: a) Summary of the process flow, structure schematic and SEM image of a VO₂ switch fabricated at EPFL CMi. b) IV characteristic of a representative two terminal VO₂ device exhibiting sharp and hysteretic electrically induced IMT.

material and design parameters. In particular, for a given VO₂ film thickness, the switching power increases with the increase of the VO₂ switch length. Conversely, the switching power per μm tends to decrease with the increase of the switch width [126]. Two terminal VO₂ switches can be included in the design of RF phase shifters and filters in order to introduce a temperature and electrical tunability of the overall RF functionalities [136, 156].

4.1.3 VO₂ for steep-slope FETs.

Given the persisting uncertainty concerning the fundamental mechanism at the base of VO₂ IMT and the possibility of electrically inducing such phase transition, several attempts of realizing a true three terminal switch based on a VO₂ semiconducting channel have been carried on in recent years. Unfortunately, conventional FET structures based on the deposition of low or high k dielectrics on the functional oxide failed to prove the possibility of controlling electrostatically the IMT temperature or voltage threshold [125, 157, 158]. Partial success has been obtained by employing ionic liquid gating [159, 160]. However, the impact of the gate bias on VO₂ electrical properties was at best limited, and often the oxide was irreversibly chemically modified, resulting in altered characteristics. Moreover, the obtained conductance variations required long electrostatic actuation times and they were finally related to a variation of the oxygen vacancies concentration rather than to a conventional electrostatic doping effect [161–163].

Nevertheless, the IMT of VO₂ resistors connected in series to the source or gate of field-effect

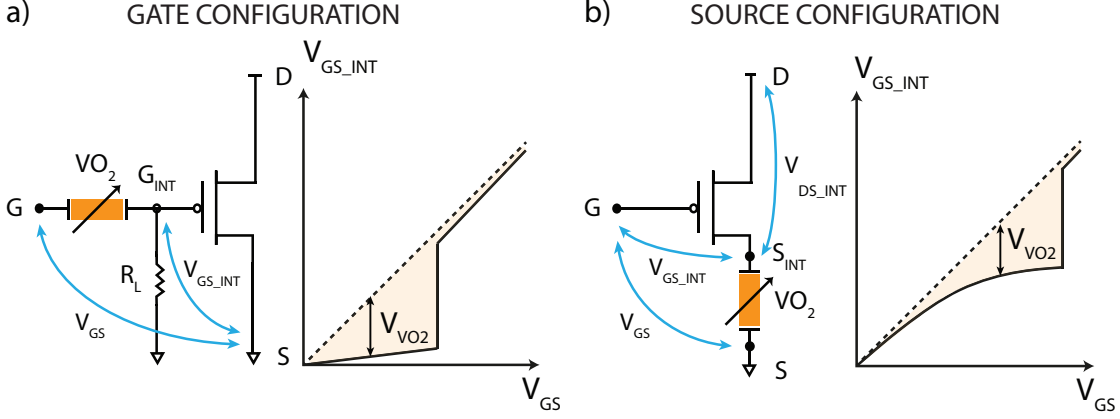


Figure 4.7: Circuit schematic and evolution of the internal gate to source bias in a PC FET realized connecting a VO_2 resistor in series to either the gate a) or the source b) of a field effect transistor. Adapted from [29].

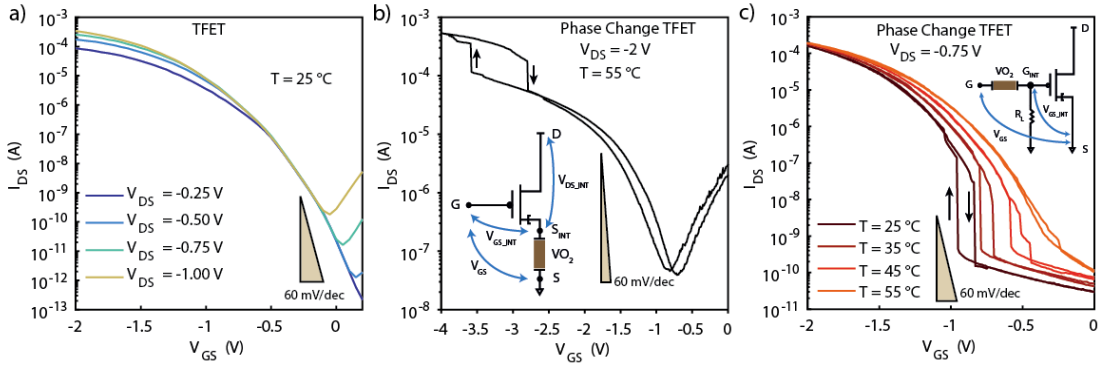


Figure 4.8: a) Silicon nanowire TFET baseline transfer characteristic. b) Transfer characteristic of the PC TFET in source configuration. c) Transfer characteristic of the PC TFET in gate configuration. Adapted from [29].

devices has been exploited to demonstrate switching slopes well below the 60 mV/dec Boltzmann limit constraining the MOSFET subthreshold slope. Figure 4.7 shows the circuits of the so called phase change FET (PC FET) in either gate (Figure 4.7a) or source (Figure 4.7b) configurations. The working principle of such a device is quite straightforward: triggering the IMT of a VO_2 resistor connected in series to the gate or source of a transistor, the internal gate to source bias increases suddenly, determining an increase of the output current with a sub 60 mV/dec slope deriving from the steep phase transition [29, 30].

As mentioned in chapter 2, the first demonstration of such a FET was performed in source configuration [164]. In [29, 30], both the gate and source configurations were demonstrated starting from a silicon nanowire pTFET, whose baseline characteristic is shown in Figure 4.8a.

Connecting a VO_2 resistor in series to the TFET source, the internal V_{GSint} seen by the FET is reduced because of the voltage drop on the insulating VO_2 . For sufficiently high gate bias, the

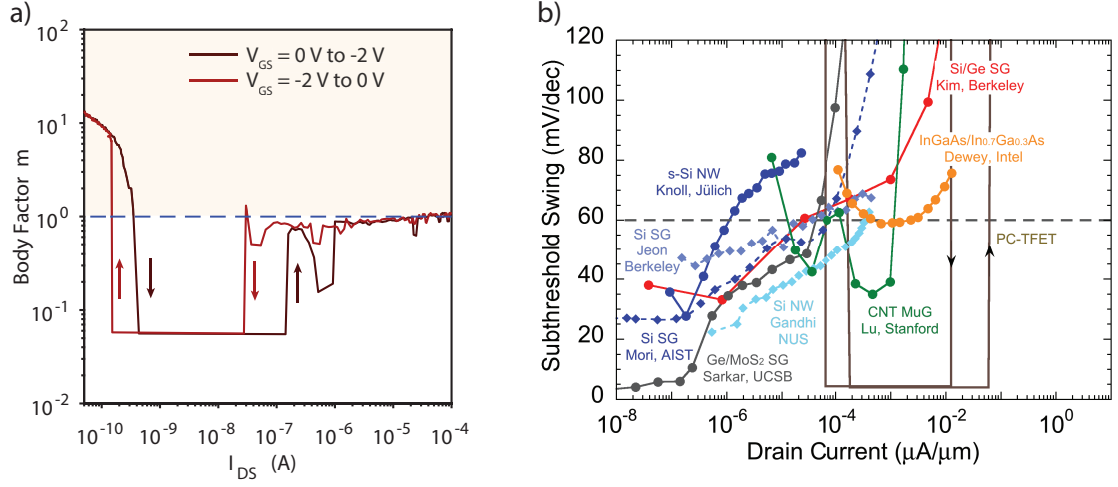


Figure 4.9: a) Body factor of the PC TFET in gate configuration as a function of the output current. b) SS vs current of the PC TFET compared to other steep slope devices. Adapted from [29].

current of the TFET is able to trigger the functional oxide IMT. VO_2 resistance drops drastically, determining a large increase of the internal gate to source bias, corresponding to a jump of the output current with the same sub 60 mV/dec slope characterizing VO_2 insulator to metal transition as shown in Figure 4.8b. In this case, in order to decrease the electrical power required to trigger the IMT, the temperature of the device was increased to 55 °C.

The circuit of the PC TFET in gate configuration is slightly more complex, requiring the addition of a load resistor, R_L , between the internal gate node and ground. This element is required so to provide a gate current sufficient to trigger the IMT of a VO_2 resistor placed between the external and the internal gate nodes (see inset of Figure 4.8c). By increasing the gate to source bias applied to the PC FET, the current flowing in the two gate resistors will increase. When a sufficient electrical power is achieved, the functional oxide becomes metallic determining a sudden increase of V_{GSint} and a consequent steep jump of the output current, as shown in Figure 4.8c.

The IMT transition of the VO_2 resistor determines the increase of the internal gate voltage and therefore a sudden variation of the surface potential in the semiconductive channel. This enables to break the barrier limiting the value of the body factor in conventional MOSFET. As shown in Figure 4.9a, the body factor of the PC TFET in gate configuration is below one over more than two orders of magnitude of the output current. Consequently, the subthreshold of the device reaches deep subthermal values on a similar range of the drain current. Figure 4.9a directly compares the SS vs output current for several different steep slope FETs. The PC TFET in gate configuration is the only one reaching extremely sharp transition for large current values. However, the addition of a resistive voltage divider on the gate of a FET determines a low gate impedance and therefore a large gate current, required in any case to trigger VO_2 IMT. Therefore, while in theory allowing to reduce the power supply by exploiting the steep slope, the gate PC TFET introduces a relevant static gate power consumption. Moreover, because of the intrinsic hysteretic nature of the IMT in the VO_2 , independently from the considered configuration the PC TFET exhibits a relatively large hysteresis in the transfer characteristic.

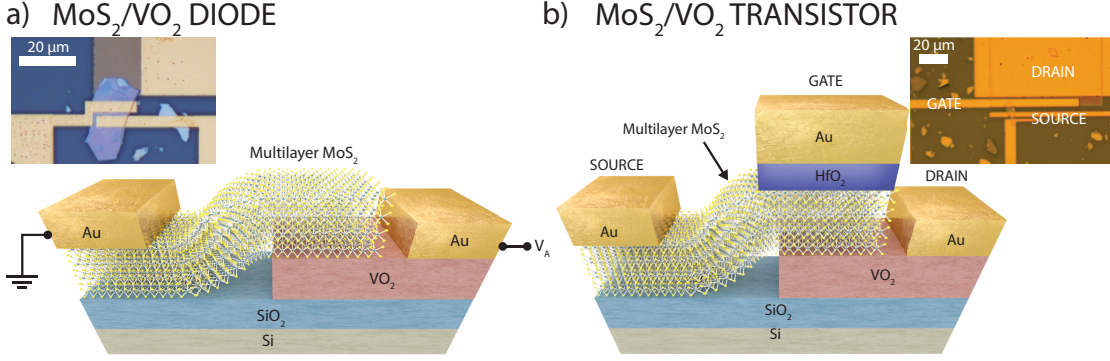


Figure 4.10: Schematic of MoS_2/VO_2 heterojunction devices: a) two terminal device and b) field-effect device. Inset: optical images of the fabricated devices.

Unfortunately, the narrow band gap of VO_2 in its insulating state determines a rather small resistivity and therefore a high leakage currents in the "OFF" state of a VO_2 based two or three terminals switch. Moreover, the electrical induced phase transition requires typically several hundreds of μW to few mW of power, therefore contributing greatly to the device power consumption. Large insulating state leakage and reduced gate control on the carrier density are currently two fundamental challenges on the road for VO_2 based devices and circuits. The structure proposed in the following targets these issues by shifting the electrostatic control from the functional oxide to a wide band gap 2D semiconductor, that can substantially limit the OFF current while enabling field effect control over the device conduction.

4.2 VO_2/MoS_2 heterojunction devices

We demonstrate in this section a new device based on a vdW heterostructure junction formed by VO_2 and multilayer molybdenum disulphide (MoS_2) flakes. MoS_2 is a 2D material of the TMDC family, characterized by dominant electronic conduction. Multilayer flakes exhibit a 1.3 eV indirect band gap, that widens with the decrease of the layer number [38, 165]. Our two-terminal VO_2/MoS_2 heterojunction devices exhibit good current rectification performance and excellent optical responsivity, both tunable in temperature thanks to the strongly temperature dependent properties of VO_2 . Moreover, we demonstrate the possibility of inducing the vanadium dioxide IMT by electrical excitation at room temperature, obtaining a stable and reversible switching of the VO_2 side of the junction. Finally, we demonstrate the first field-effect devices based on MoS_2/VO_2 heterojunctions, obtaining a good electrostatic control on the junction conduction and a substantial reduction of the I_{OFF} current with respect to three terminal devices with VO_2 channels [122, 166].

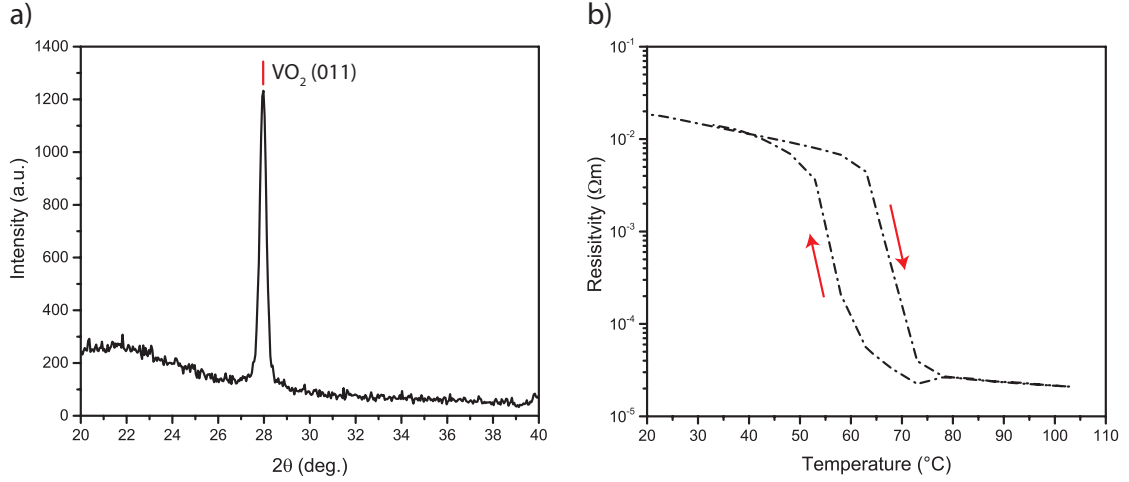


Figure 4.11: a) XRD spectrum of the sputtered 75 nm thick VO₂ film showing a clean peak at 28° corresponding to VO₂ (011) crystal plane. b) Resistivity curve of the same film, exhibiting IMT around 68 °C and a resistivity reconfigurability of three orders of magnitude.

4.2.1 Heterojunction fabrication

Figure 4.10 shows a schematic representation of the fabricated MoS₂/VO₂ heterojunction devices, together with optical images of the final result. The first step in the process consists in the deposition of the VO₂ layer on top of a silicon wafer previously thermally oxidized in order to obtain a 2 μm thick SiO₂ layer. A 75 nm thick polycrystalline vanadium dioxide film was deposited by reactive DC magnetron sputtering of a vanadium target in high-vacuum conditions at Laboratoire d’Energie Solaire et de Physique du Bâtiment (LESO-PB) in EPFL. The power on the vanadium (V) metal target (two inches of diameter, 99.95 % purity) was set to 150 W. Ar process gas (purity 99.999 %) was introduced in the chamber and the flow was regulated by a mass flow controller. During the deposition, the oxygen pressure was kept constant by a Proportional Integral Derivative (PID) feedback control. This regulated the oxygen flow based on the pressure readings of a Zirox XS22 lambda-probe oxygen sensor. The temperature was measured by a stationary thermocouple above the rotating substrate holder and was kept constant at 600 °C. During deposition the substrate was rotating at 15 rpm. An in situ annealing was performed during the slow cooling of the sample (30 °C/min). The XRD spectrum obtained from the as deposited VO₂ film is reported in Figure 4.11a. A clear peak at 28° corresponding to VO₂ (011) crystalline plane was observed [153]. Figure 4.11b shows the resistivity curve measured vs temperature, demonstrating a hysteretic IMT around 68 °C. The resistivity ratio between the conductive and insulating phase in our sample reaches almost three orders of magnitude. Reference VO₂ switches were fabricated on this film by etching VO₂ squares and depositing Au contacts by sputtering and lift-off. EBL on a negative ebeam resist, nLOF, was performed to obtain a soft mask on the functional oxide. The VO₂ film was then patterned by wet etching in a commercial Cr etch solution diluted in deionized water to a 1:4 ratio. The resulting resistors exhibit a reversible and stable electrically induced IMT, as shown in Figure 4.12.

MoS₂ powder was synthesized by heating a mixture containing stoichiometric amounts of molyb-

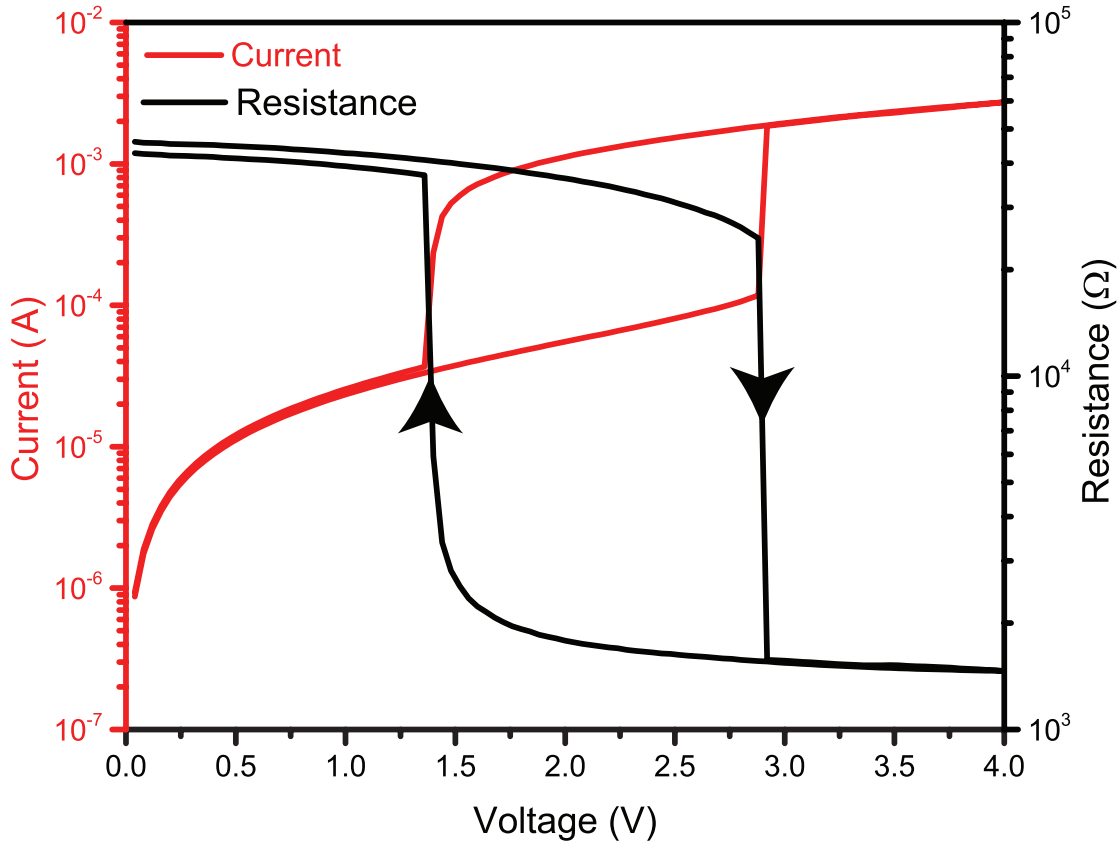


Figure 4.12: Current (red) and resistance (black) characteristic of a VO_2 reference switch fabricated using the same film at the base of the heterojunction devices.

denum (99.9 % pure, Alfa Aesar) and sulfur (99.999 % pure, Alfa Aesar) at 1000 °C for 7 days in an evacuated and sealed quartz ampule. The mixture was slowly heated from room temperature to 1000 °C for 12 h in order to avoid any explosion due to the strong exothermic reaction and the high volatility of sulfur. From this powder, MoS_2 crystals were grown using chemical vapor transport (CVT) with iodine as transport agent at ca. 5 mg/cm³. The total powder charge is 5 g. A very slight excess of sulfur is always included (typically 0.5 wt% of the charge) to ensure the stoichiometry in the resulting crystals. The excess of sulfur is not incorporated into the dichalcogenide crystals but condenses as elemental sulfur onto the wall of the quartz tube at the end of the CVT process. The source and growth zones were kept at 1060 and 1010 °C, respectively, for 7 days in evacuated and sealed quartz ampules. After this time the furnace is turned off, a small fraction of the charge is transported toward the colder end of the tube, forming crystals with diameters of about 2-8 mm and thick tens of microns. The resulting crystals were washed with acetone and dried in vacuum. X-ray diffraction study has shown that MoS_2 obtained in this way belongs to the 2H polymorphism [167].

MoS_2 multilayer flakes were mechanically exfoliated on a PDMS stamp using the scotch taping technique. An adapted manipulator and a glass slide holding the PDMS stamp were used to transfer the obtained flakes on the edge between the pre-patterned VO_2 structures and the exposed SiO_2 layer [42]. The results reported in the following have been obtained transferring MoS_2

flakes of thickness ranging between 40 and 100 nm. Two-terminal devices were then completed with a further EBL step followed by lift-off of 100 nm thick gold contacts on the two sides of the junctions, as shown in Figure 4.10a. Top-gated devices required the deposition of a dielectric layer on the junction area. Following the same technique developed for WSe₂ double-gated FETs and presented in chapter 3, an Al₂O₃ seed layer was deposited by sputtering and oxidation in air of a 2 nm thick Al layer. Then, 5 nm of HfO₂ were deposited by ALD. The gate contact was fabricated by sputtering and lift-off of 1 nm Ta and 140 nm Au after a last EBL step performed on a MMA/PMMA bilayer. Figure 4.10b shows a schematic view and a optical image (inset) of the complete device. A detailed process flow is illustrated in the appendix Figure A.3b.

4.2.2 Results

Two-terminal devices

The qualitative band diagram for the heterojunction of multilayer MoS₂ and VO₂ is drawn in Figure 4.13 based on the data reported in literature [168–174]. When VO₂ is in the insulating state (Figure 4.13a, b), both the materials are intrinsically n-type semiconductors [38, 168]. Since MoS₂ workfunction is smaller than VO₂ one, at the formation of the heterostructure electrons are transferred from the first to the second, resulting in the upward bending of MoS₂ bands close to the junction (see Figure 4.13b). Because of VO₂ larger dielectric constant and electronic density, most of the band bending falls on the MoS₂ side of the heterojunction [168]. The discontinuity in the conduction band (ΔE_C) is estimated to be 1 eV according to the affinity rule, while the built-in voltage is in the 0.35/0.75 eV range [168, 175, 176]. Overall, the realized junction is expected to be a n-n heterostructure with type II band alignment. The band diagram of the junction with VO₂ in the metallic phase is shown in Figure 4.13c. The introduced Schottky barrier is estimated to be comparable to ΔE_C [175].

The I-V curve of a representative heterojunction at room temperature, obtained grounding the contact on MoS₂ and sweeping the voltage on the VO₂ side, is shown in Figure 4.14. A clear rectifying behavior is observed, with a rectification ratio larger than 10³ at +/- 2 V. Under positive applied voltage, the current shows an initial exponential increase, as expected for a diode forwardly bias. At larger voltages, the current dependence on the applied voltage becomes linear because of the series resistance, to which contribute both the contact resistance and the MoS₂ area between the metal pad and the junction. The electrical behavior of the junction at room temperature can be understood referring to the qualitative band diagram in Figure 4.13b. By applying a positive bias to VO₂, electrons tend to move from MoS₂ conduction band to VO₂ one. The injection along this path requires to overcome the built-in energy barrier at the junction. By increasing the positive bias, more and more electrons have energies high enough to overcome such barrier. Therefore, the injection from MoS₂ conduction band is favored resulting in the observed exponential increase of the current. Conversely, under reverse bias electrons tend to follow the opposite path, moving from VO₂ conduction band to MoS₂. Carriers in this case must face the large ΔE_C barrier (Figure 4.13a), that strongly limits the reverse current in our device determining the observed good rectifying behavior.

The device characteristic close to 0 V can be described in first approximation using the ideal

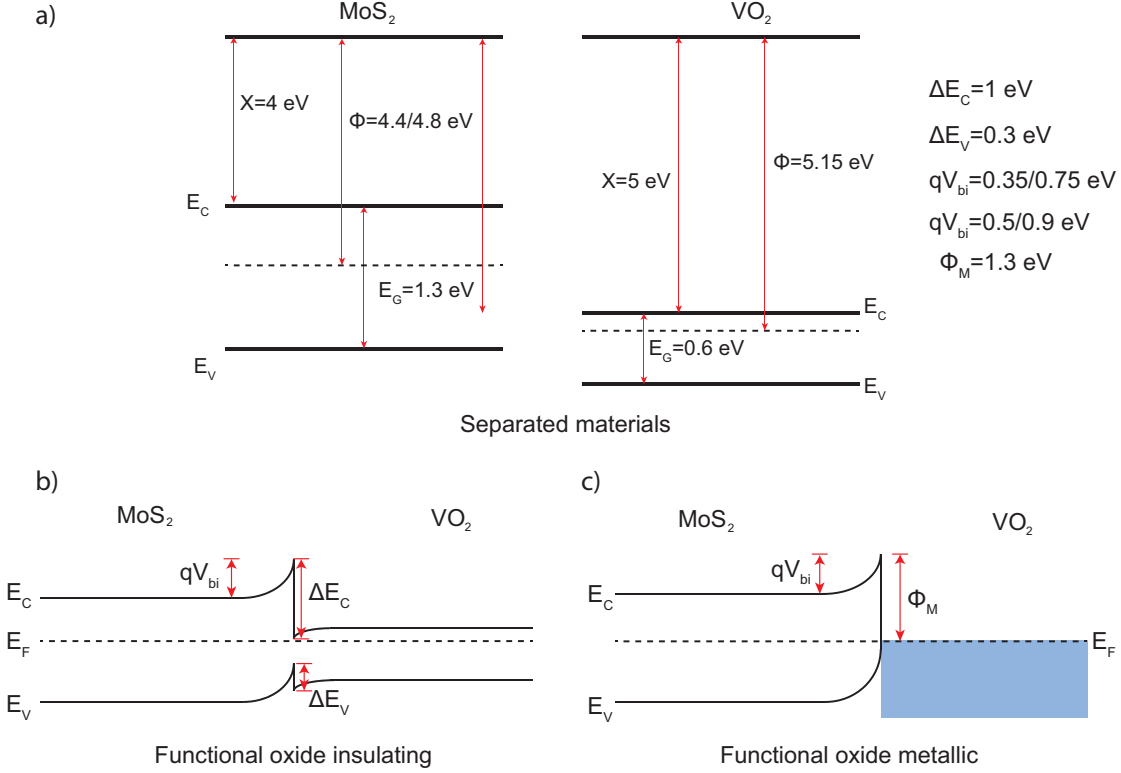


Figure 4.13: Qualitative band diagram of a) the separated materials and of the heterojunction with VO₂ in insulating b) and metallic c) phases.

diode model. The diode current is then given by the Shockley equation:

$$I_D = I_S (\exp(qV_a/nk_B T) - 1) \quad (4.1)$$

where I_S is the saturation current, V_a the applied voltage and n the diode ideality factor. In Shockley model, the saturation current is independent from the applied voltage. This expression provides a good fit of the forward current of the heterojunction, as shown in Figure 4.15: the extracted ideality factor is 1.75. However, it is clear that such model fails to describe the non-saturating reverse current in the junction. A more accurate matching can be obtained using the Fang-Howard model [177], specifically developed for rectifying n-n heterojunctions and based on the introduction of a voltage dependent I_S expression:

$$I_S = \frac{A_0}{T} (V_a + V_{bi})^{3/2} \exp(-qV_{bi}/k_B T) \quad (4.2)$$

where A_0 is a parameter related to the heterostructure material properties and V_{bi} is the built in voltage at the heterojunction.

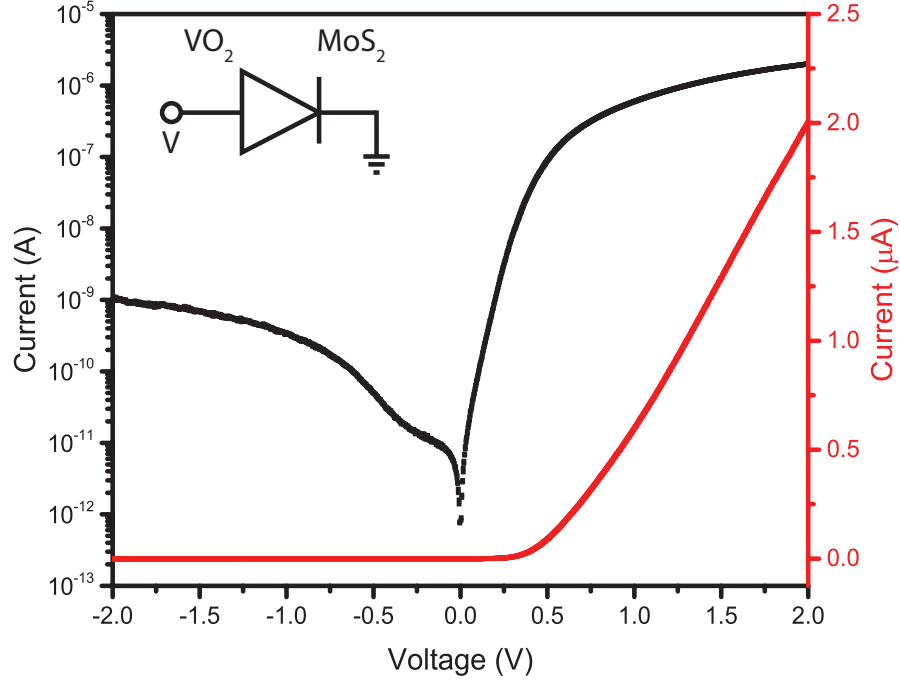


Figure 4.14: Room temperature I-V curve of a representative two-terminal heterojunction device in linear (red) and logarithmic (black) scale.

By taking into account the strong abundance of electrons on both sides of the junction, Fang-Howard model is well adapted to our case, and it provides a 1.85 ideality factor. The obtained values of the quality factor, both smaller than two, suggest that the forward current in the heterojunction is affected by two main recombination mechanisms: minority carriers recombination in the neutral regions and recombination in the space charge region [178].

VO₂ insulator to metal phase transition is expected to increase the device conductance by collapsing the functional oxide band gap and therefore greatly increasing the electronic density in the functional oxide conduction band. The temperature impact on the heterojunction conduction has been investigated measuring the I-V characteristic at increasing temperatures as shown in Figure 4.16a. A gradual increase of both forward and reverse currents is observed approaching the IMT temperature. Above the transition temperature, the increase of the current tends to saturate. In this region, the device behaves as a Schottky rectifier, since VO₂ is in its metallic phase. The band diagram of the junction with metallic VO₂ is drawn in Figure 4.13x. The Schottky barrier (Φ_M) is estimated to be close to ΔE_C , while the built-in voltage should increase slightly since VO₂ work function is reported to increase across the IMT [175]. The observed increase of the reverse current following the temperature can be explained with the boost of electron density in VO₂ conduction band, changing from 10^{18} cm^{-3} in the insulating phase up to 10^{23} cm^{-3} in the metallic one. Therefore, above IMT many more electrons are available for injection over the Schottky barrier into MoS₂ conduction band. The increase of the forward current can be attributed instead to the stronger thermionic injection in VO₂ conduction band from the MoS₂ side. Thermionic injection over a potential barrier is indeed strongly sensitive to the temperature, because of its impact on the electrons energy.

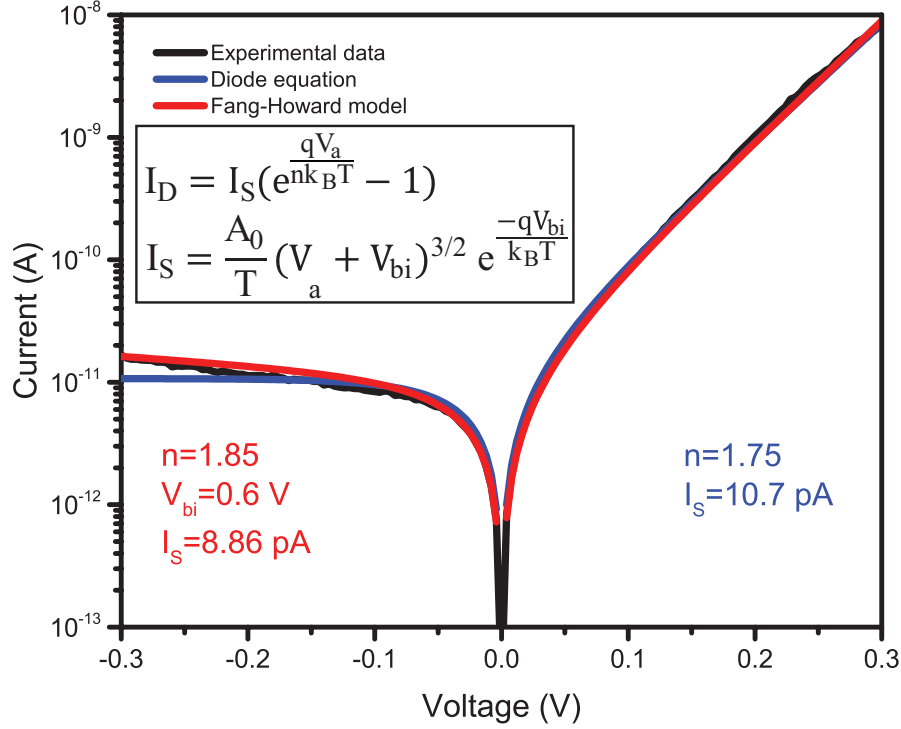


Figure 4.15: Ideal diode (blue) and Fang-Howard model (red) compared to the experimental characteristic (black). The Fang-Howard model is able to describe the non-saturating reverse current by modifying I_S expression, as reported in the inset.

Noticeably, the heterojunction with metallic VO_2 is still rectifying, exhibiting roughly the same rectification ratio and a larger forward current with respect to the junction with semiconducting VO_2 . Therefore, our device can be reconfigured to behave as either a n-n heterojunction or a Schottky junction while maintaining good rectification properties.

In order to gain a more detailed insight in the junction conduction we extracted the conductance slope $S_G = (\partial \log G / \partial dV)^{-1}$ for the forward current measured at different temperatures. The result is drawn in Figure 4.16b. At room temperature, the device exhibits an excellent minimum S_G value of 120 mV/dec, which suggests that the heterojunction is abrupt and characterized by a reduced density of interface defects. This observation is further supported by the absence of any hysteresis in the double sweep I-V characteristics (see Figure 4.16a) and by a relatively low extracted diode ideality factor of 1.75 under forward bias. The conductance slope increases across the IMT and tends to decrease after the phase transition. A similar evolution is observed also for the ideality factor and saturation current, as shown in Figure 4.17. The ideality factor increases approaching the IMT temperature, while it decreases above it, consistently with what has been reported for GaN/VO_2 heterojunctions [168]. The proposed explanation behind this evolution is related to the polycrystalline nature of VO_2 film, whose grains exhibits slightly different transition temperatures. Therefore, while approaching and overcoming the IMT critical temperature, not all the grains change phase at the same time, resulting in an increase in the ideality factor. Well above the IMT point, all the grains are in the metallic phase and the ideality factor drops again.

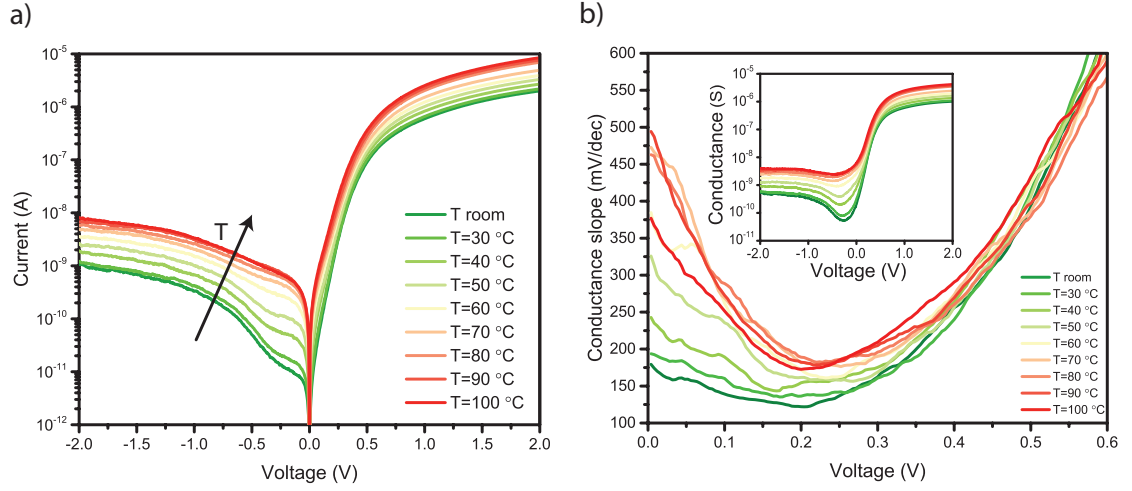


Figure 4.16: a) Measured I-V curve of the heterojunction at increasing values of the substrate temperature. b) Conductance slope under positive bias and increasing temperatures. Inset: conductance vs applied voltage.

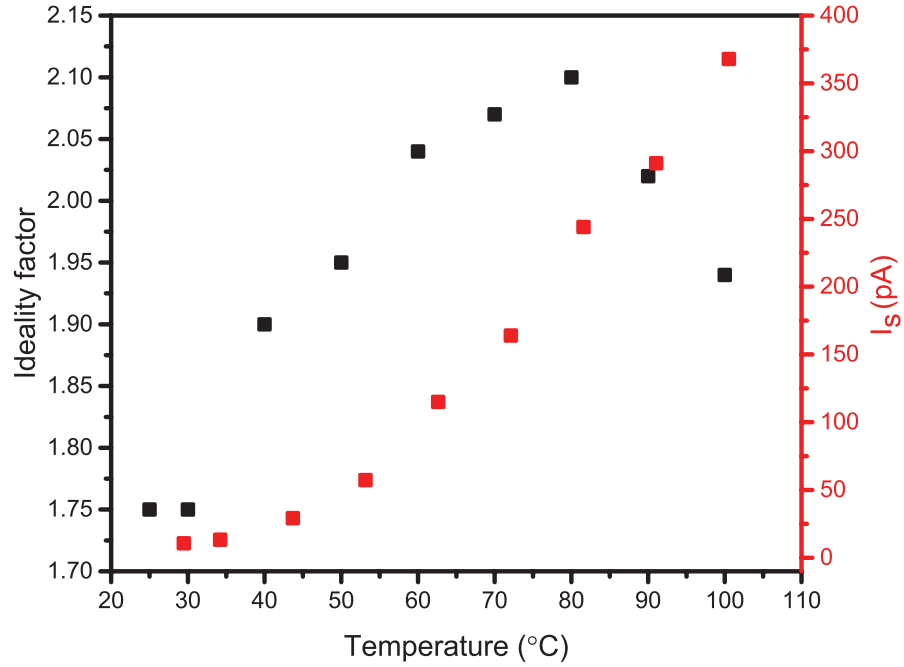


Figure 4.17: Evolution of MoS₂/VO₂ heterojunction ideality factor (in black) and reverse saturation current (in red) as a function of temperature.

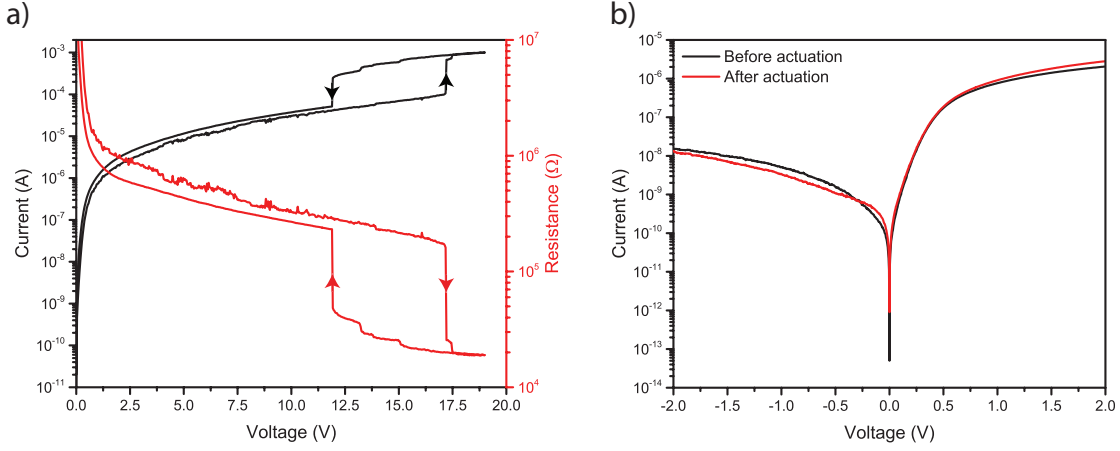


Figure 4.18: a) Electrical characteristic of a two terminal heterojunction device under forward bias large enough to trigger VO_2 IMT. b) I-V curve of the same device before (black) and after (red) the electrically induced IMT.

The capability of electrically inducing the IMT of the VO_2 side in the heterostructure has been proven in a room temperature experiment by increasing the forward bias applied on the junction. The resulting I-V curve is shown in Figure 4.18a. The biasing configuration used for the measurement is the same shown in Figure 4.10a, with the addition of a series resistance R_s of 1 k Ω to limit the maximum current in the device. The characteristic in Figure 4.18a exhibits two steep jumps in correspondence of the electrically induced IMT and MIT of VO_2 , separated by a hysteresis window. The voltage required to trigger the IMT is significantly larger with respect to the values that can be achieved in pure VO_2 switches (see the reference switch in Figure 4.12). The large actuation voltage required is due to both the considerable resistance offered by the heterojunction and the relatively large distance between the MoS_2 edge and VO_2 metallic contact (typically more than 1 μm due to the limitations of the deterministic transfer process). Remarkably, the proposed device delivers a much lower leakage current in the diode subthreshold region with respect to pure VO_2 switches. This feature combined with the envisioned possibility of modulating dynamically the IMT threshold by gating the MoS_2 side of the junction could pave the way to more energy efficient VO_2 switches.

For the device in Figure 4.18a, the power thresholds required to electrically induce the IMT and MIT transitions from an n-n heterojunction to a Schottky diode and vice versa are respectively 1.83 mW and 2.89 mW. We verified that the relatively large actuation power density required to trigger the IMT did not alter the electrical behavior of the heterojunction by measuring the electrical characteristic before and after the electrical induced IMT. Figure 4.18b shows a direct comparison of the two I-V curves: no major variations are observed, demonstrating a full reversibility of the VO_2 phase change and the stability of the heterojunction conduction.

VO_2 properties can be effectively used to fine tune the conduction in the heterojunction. It is interesting to evaluate the impact of its phase transition on the sensing capability of the proposed device. A variety of MoS_2 based photodetectors has been proposed and demonstrated in recent years. Such devices usually exhibit incredibly high photoresponsivity, but slow response [179–181]. Upon exposure to light, the VO_2/MoS_2 characteristic shifts resulting in a non zero open

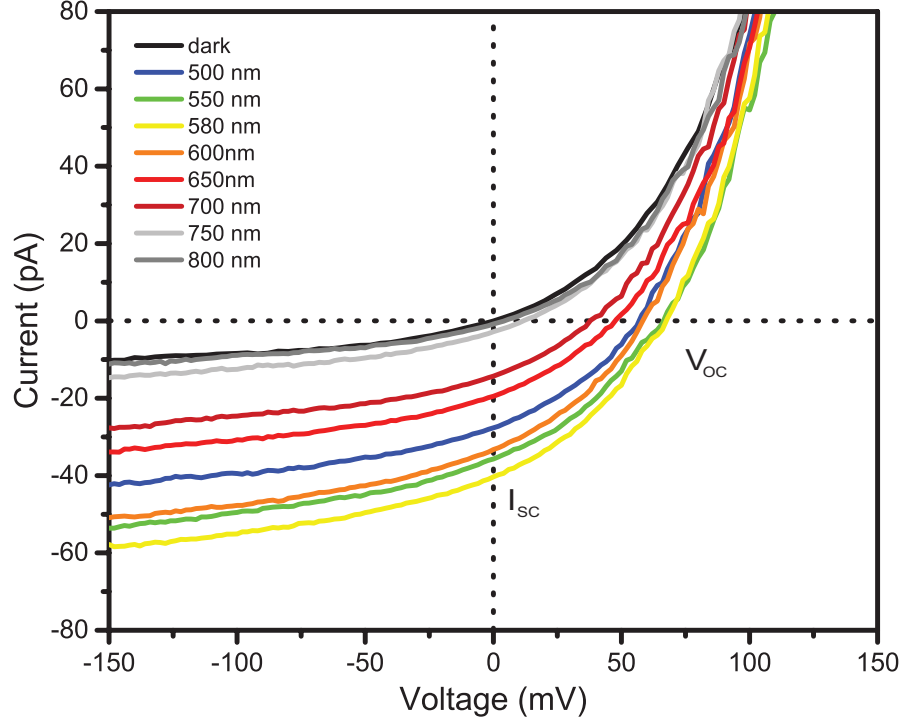


Figure 4.19: I-V characteristic of the heterojunction in dark conditions and under illumination at different wavelengths. The illumination power density is 330 nW/mm².

circuit voltage (V_{OC}) and short circuit current (I_{SC}) as shown in Figure 4.19 for different wavelength values of the incoming light. Contributions to the photoresponse from both the MoS₂ and the VO₂ regions far from the heterojunction have been found to be negligible by measuring separately the characteristics of the two materials contacted with the same electrode stack used in the heterojunction. Therefore, we conclude that the overlap area defining the junction provides the dominant contribution to the observed light response.

The measured I_{SC} shows a linear dependency with respect to the incident power density, as shown in Figure 4.20a for illumination at a wavelength of 600 nm. We also characterized the time domain photoresponse of the device by measuring the evolution of I_{SC} in response to ON/OFF transitions of the light source (see Figure 4.20b). The extracted response time at room temperature is 3.5 ms, considerably smaller than the ones reported in literature for several other implementations of MoS₂ based photodetectors [182–184].

The origins of the observed photovoltaic effect can be traced back to the splitting of photogenerated carriers made possible by the built-in voltage at the heterojunction. Electrons are then collected at the contact on the MoS₂ side of the device while holes are injected in VO₂. The band diagram in Figure 4.21a provides a graphical representation of the mechanism at the base of the measured photocurrent. A similar working principle has been reported for p-n homojunctions based on doped multilayer MoS₂ flakes, leading to high photoresponsivity values and relatively small response times [45, 182]. The built-in voltage in our devices is estimated to be in the 0.35/0.75 eV range. Most of the band banding is distributed on the MoS₂ side because of the

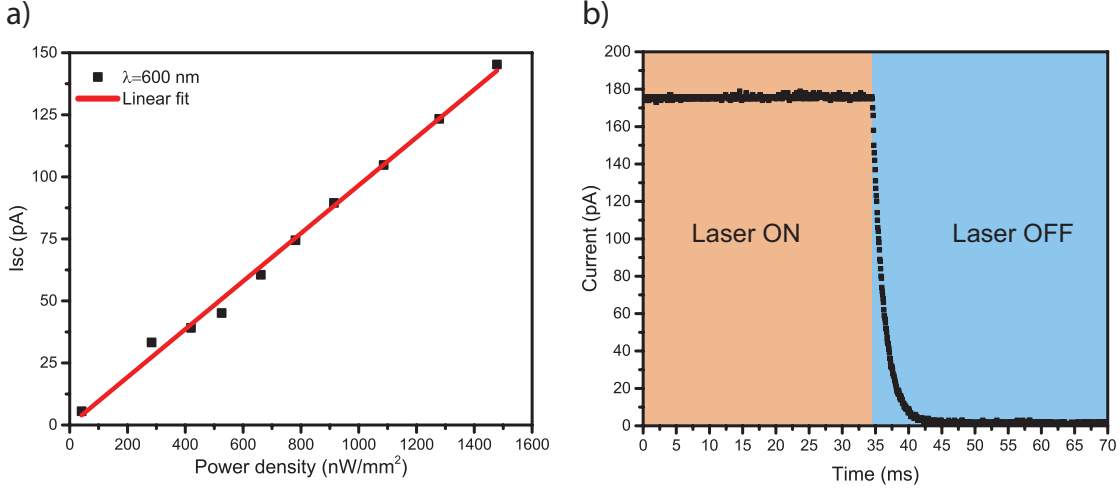


Figure 4.20: a) Measured short circuit current under illumination at $\lambda = 600$ nm with increasing power density. b) Transient response of the heterojunction short circuit current. The extracted response time is 3.5 ms.

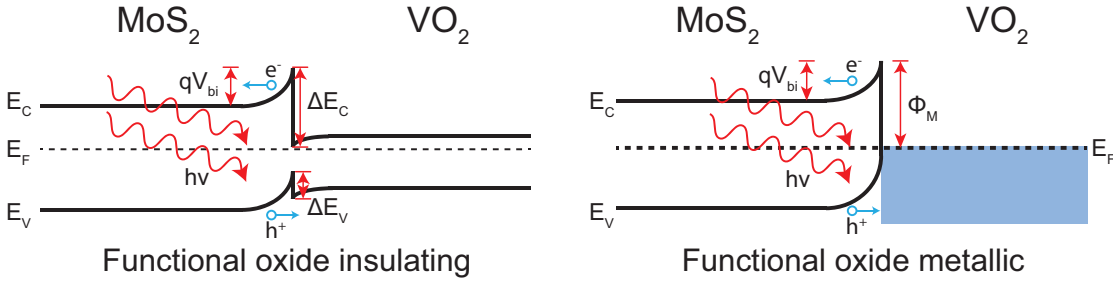


Figure 4.21: Origin of the photogenerated current in a) MoS₂/VO₂ insulating and b) MoS₂/VO₂ metallic junctions.

considerable larger dielectric constant and electron concentration in VO₂ [185]. The lower limit for the electric field at the junction, responsible for the photogenerated carrier separation, can be then estimated assuming that the MoS₂ flake is depleted through its entire thickness (maximum 100 nm). The resulting electric field is therefore between 35 and 75 kV/cm, and it is sufficient to efficiently separate and accelerate the photogenerated carriers.

We characterized the impact of temperature on the wavelength resolved photoresponsivity $R(\lambda)$ at zero applied bias, defined as the ratio between the photogenerated current and the incident power on the device. The results are reported in Figure 4.22. It is possible to locate the cut-off wavelength between 750 and 800 nm across all the investigated temperature range. This suggests that light absorption happens mostly in the MoS₂ side of the heterojunction, with this material band gap limiting the minimum light frequency absorbed [181]. At room temperature, a maximum photoresponsivity of 1.25 A/W was measured at 550 nm, and values exceeding silicon photodiode performance have been obtained in the 500/650 nm range [186]. Responsivity values larger than one have already been reported in p-n junctions based on multilayer MoS₂ flakes, and can be attributed to the efficient photocarrier separation operated by the built in voltage

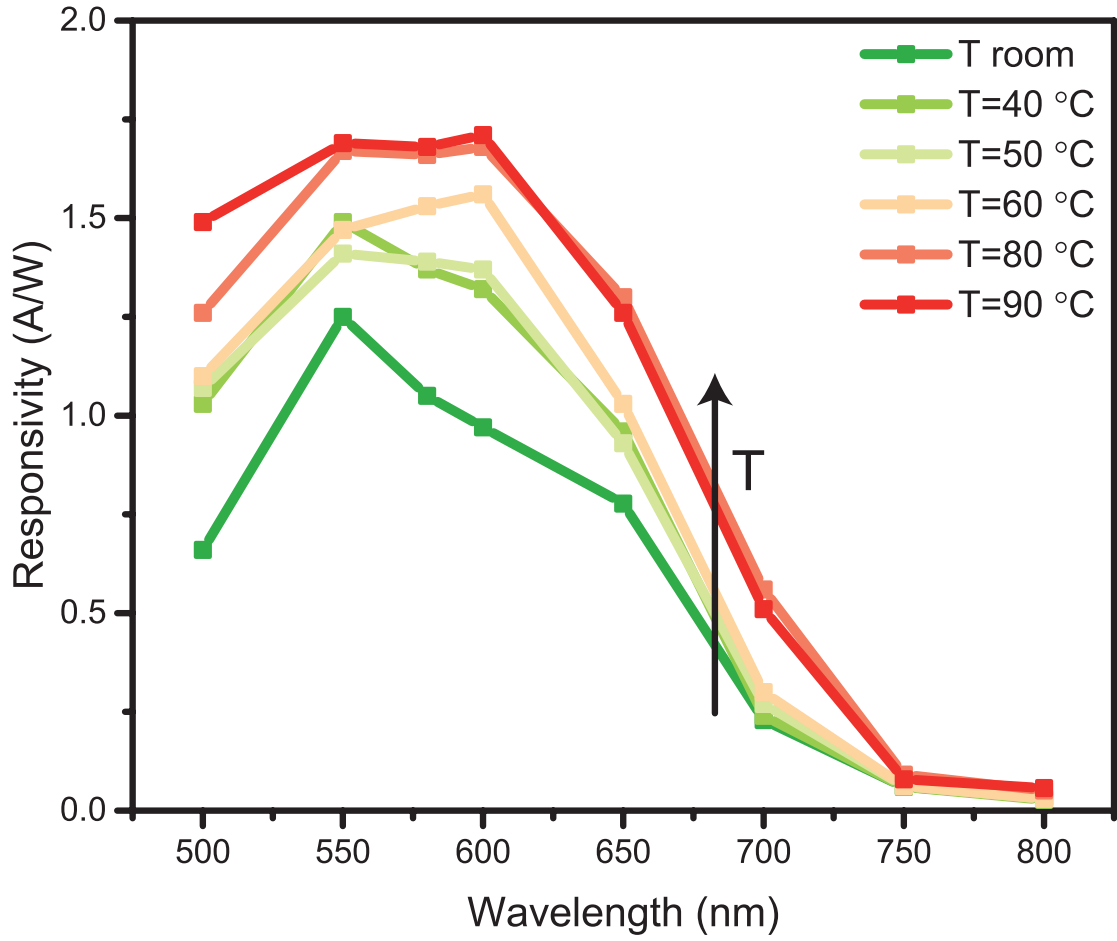


Figure 4.22: Spectral evolution of the heterojunction photoresponsivity measured at increasing temperatures.

at the junction [45, 182]. The photoresponsivity in the visible range is clearly boosted by the temperature rise and it tends to saturate above the VO₂ IMT temperature.

This enhancement can be explained by different mechanisms. First, the reported increase of VO₂ work function with temperature determines a larger built-in voltage and therefore a stronger electric field at the junction that provides a more efficient separation of photogenerated carriers [175, 185]. Secondly, the MoS₂ depleted thickness could increase because of VO₂ work function and carrier density boost, resulting in an increase of the photosensitive volume [131]. Moreover, another potential contribution could derive from the change of VO₂ optical properties producing potentially beneficial optical interference effects responsible for an enhanced light absorption. Indeed, recent studies reported that the photoluminescence of monolayer MoS₂ flakes on VO₂ substrates increases upon heating VO₂ above the IMT temperature, most likely because of constructive optical interference effects [187, 188].

The generated electrical power P_{el} as a function of the applied voltage at different temperatures under 600 nm light illumination with an incident power density of $1.48 \mu\text{W}/\text{mm}^2$ is shown in Figure 4.23a. The temperature increase results in a boost of I_{SC} and a larger reverse current,

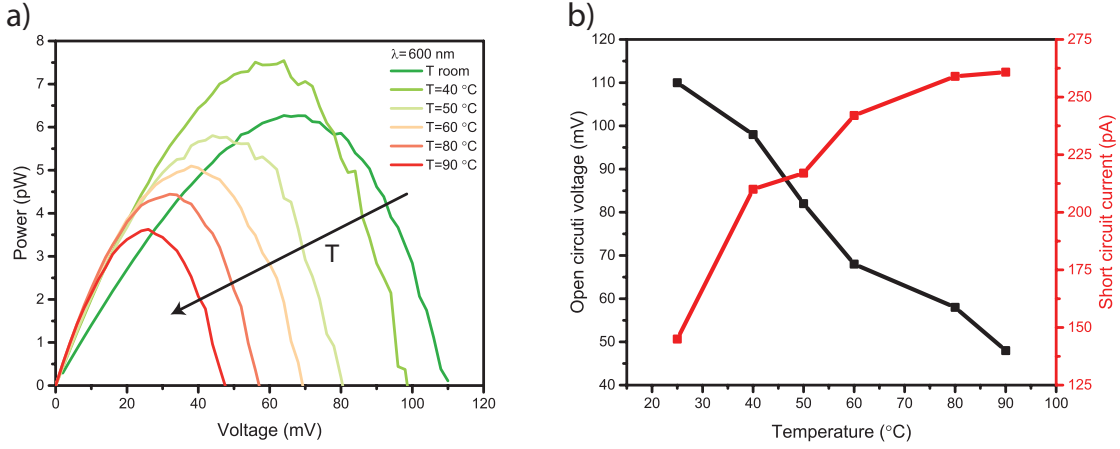


Figure 4.23: a) Electrical power generated by the heterojunction under 600 nm light with an incident power density of $1.48 \mu\text{W}/\text{mm}^2$. b) Temperature evolution of both open circuit voltage and short circuit current under the same illumination conditions.

as reported in Figure 4.16. This is related to a more favorable leakage path for photogenerated carriers, which causes a drop of V_{OC} . Since V_{OC} decreases at a faster rate than I_{SC} grows (see Figure 4.23b), the harvesting of the optical power becomes less efficient at high temperatures [181]. Therefore, VO_2 IMT is beneficial for the heterostructure photosensitivity but appears detrimental for its energy harvesting capability.

Field-effect devices

Finally, we realized and characterized three terminal devices based on these heterojunctions. Figure 4.24 shows the I-V characteristic of a junction measured at room temperature before and after the deposition of the $\text{Al}_2\text{O}_3/\text{HfO}_2$ gate stack. Both the forward and reverse current are boosted, likely because of the 200 °C annealing of the contacts performed during the ALD step required to deposit the gate dielectric.

An applied negative bias to the top gate determines a significant reduction of the forward current and consequently of the rectification ratio as reported in Figure 4.25a. Figure 4.25b shows drain current and output conductance measured at different gate bias values. The output characteristic shows no saturation in the considered range of drain voltages. The impact of gate bias on the junction conduction can be explained in terms of the qualitative band diagram depicted in Figure 4.26. For $V_G < 0$ V, MoS_2 bands are shifted upward in the gated region, resulting in a depletion of electrons in its conduction band and therefore in the reduction of the diode forward current and output conductance.

The transfer characteristic of a second device measured at a drain bias of 1.5 V and at room temperature is reported in Figure 4.27 together with the gate leakage current and the transconductance curve. The heterojunction transistor shows a n-type depletion mode conduction with a I_{ON}/I_{OFF} ratio of three orders of magnitude, limited by the series and junction resistance, and an I_{OFF} as low as $4.7 \text{ pA}/\mu\text{m}$. The extracted transconductance shows a narrow peak due to the

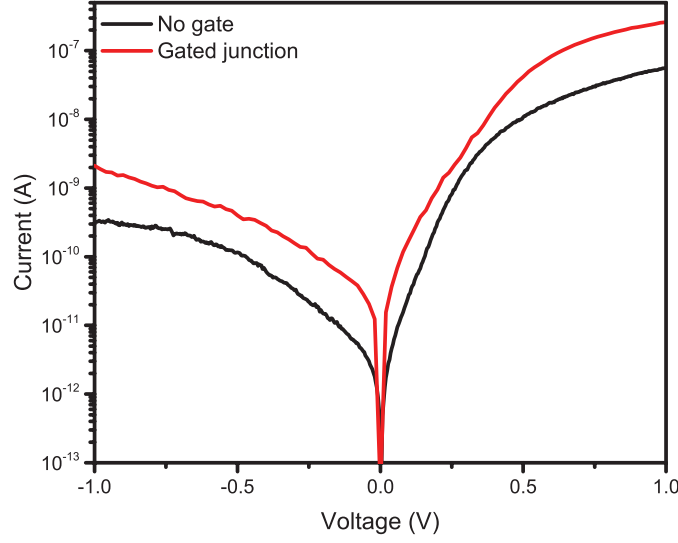


Figure 4.24: Comparison between the junction I-V characteristic measured before and after the gate dielectric deposition.

observed drain current saturation. Noticeably, the gate leakage current remains relatively low in the investigated bias window, suggesting a good quality of the high k dielectric deposited on the heterojunction. The introduction of a large band gap 2D semiconductor is therefore proved to enable a consistent decrease of the leakage current in VO₂ based devices. Unfortunately however, in our structure we couldn't reliably obtain a current density high enough to trigger the functional oxide IMT. Indeed, as shown in Figure 4.18, the voltage to be applied at the heterojunction to induce the phase transition is too large to be sustained by the gate dielectric. Optimized devices realized with thinner VO₂ and MoS₂ flakes and a considerably lower parasitic series resistance are required to demonstrate an electrostatically tunable IMT.

Figure 4.28 reports the device subthreshold slope as a function of the drain current: a minimum value of 130 mV/dec is achieved and maintained over almost two decades of the output current. The double sweep transfer characteristic in the inset shows a 300 mV hysteresis. Both these values suggest a high quality of the deposited top gate dielectric.

4.2.3 Optimized heterojunction structure

Figure 4.29a shows the qualitative structure of the fabricated and characterized VO₂/MoS₂ three terminal heterojunction devices. In such a heterostructure, the critical parameters to determine the threshold voltage (and power) required to trigger VO₂ IMT are the distance between the MoS₂ flake and the metallic contact deposited on VO₂ (L_{VO_2}) in the figure) and the parasitic resistances in series to the junction. The L_{VO_2} design parameter depends on the deterministic transfer procedure, since the position of the MoS₂ flake is fundamental to determine the length of the vanadium dioxide section to be switched when triggering the phase transition. The challenges related to the precise control of the transfer procedure do not allow to reliably reduce the distance between the 2D flake and VO₂ contact to less than few μm . The proposed optimized structure

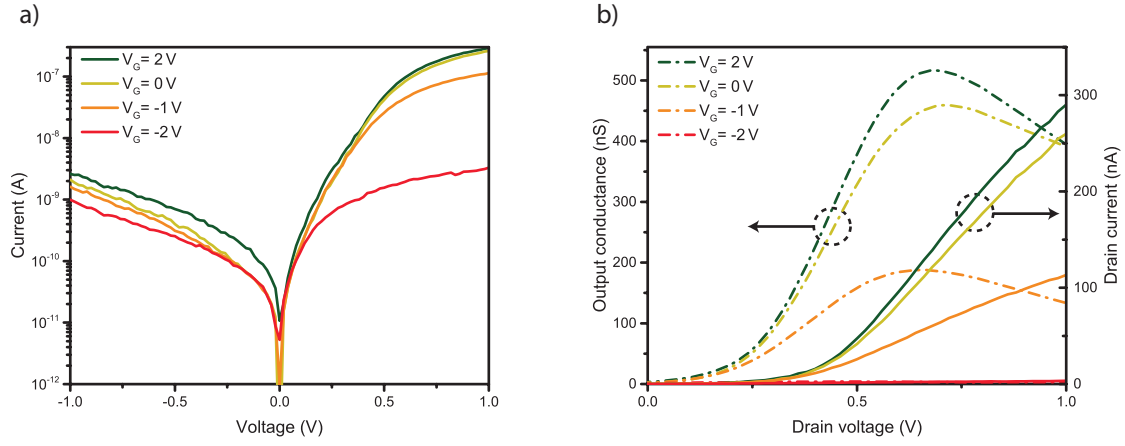


Figure 4.25: a) Impact of gate bias on the heterojunction I-V characteristic in logarithmic scale. b) Output characteristic of the heterojunction FET in linear scale and impact of gate bias on output conductance.

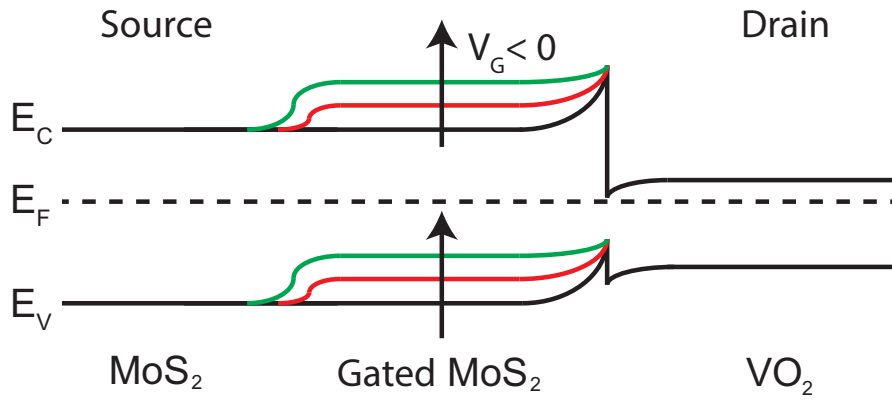


Figure 4.26: Impact of the gate bias on the heterojunction band diagram.

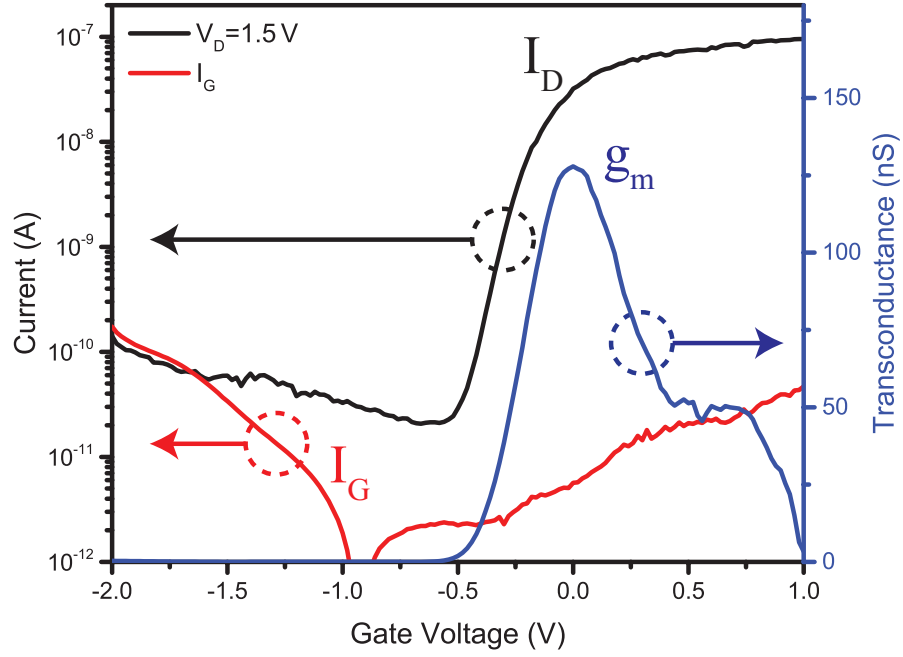


Figure 4.27: Transfer characteristic, leakage current and transconductance of the gated MoS₂/VO₂ heterojunction.

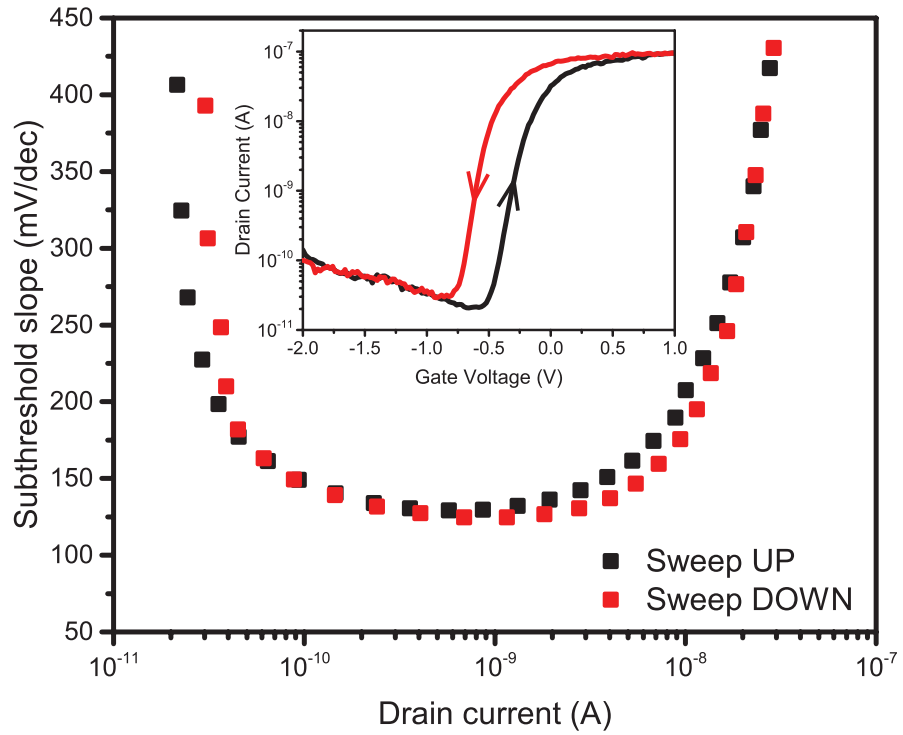


Figure 4.28: Double sweep subthreshold slope as a function of the output current. Inset: double sweep transfer characteristic showing a 300 mV hysteresis.

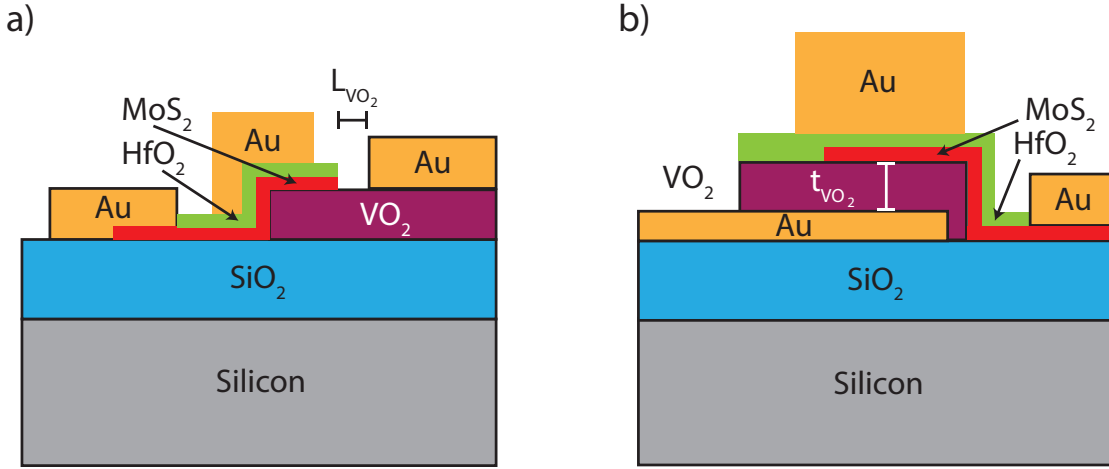


Figure 4.29: a) Structure of the fabricated VO₂/MoS₂ FET. b) Optimized structure for reduced actuation power and enhanced electrostatic control of VO₂ transition.

has the objective to eliminate this difficult to control parameter by transitioning from an in-plane actuation of vanadium dioxide to the control of only the VO₂ thickness. The schematic of the new architecture is presented in Figure 4.29b. The VO₂ film in this case has to be deposited on a metallic bottom contact, that will be exploited as the drain of the VO₂/MoS₂ FET. The following steps for the heterojunction fabrication are the same discussed for the devices presented. This structure has the fundamental advantage of decoupling the MoS₂ flake position and the extent of the VO₂ length to be switched, that can be easily reduced to less than 100 nm by carefully controlling the deposited thickness. We expect the resulting threshold voltage for the IMT to be drastically reduced and hopefully to be brought in the range accessible for the gate bias of the heterojunction FET.

4.2.4 Summary

In this chapter, the phase transition and deposition techniques of vanadium dioxide are discussed and investigated in detail. VO₂ two terminal devices are presented with particular attention to the temperature and electrical induced reconfigurability of their resistance. Then, we described the possibility of connecting VO₂ resistors in series to either the gate or source of a FET so to transfer the steep IMT resistivity transition to the field-effect device transfer characteristic obtaining subthermal subthreshold slopes. We presented our VO₂/MoS₂ heterojunctions as interesting for the mitigation of the large leakage current observed in pure vanadium dioxide devices and for the realization of temperature tunable photosensors. The fabrication of both two and three terminal devices based on this heterostructure is discussed. The origin of the good rectifying characteristic of the junction are investigated referring to the band alignment considering the two possible VO₂ phases. The possibility of realizing VO₂/MoS₂ photodiodes with high sensitivity and fast photoresponse is considered, and the performance of such a device is discussed in detail. Finally, the characteristic of three terminal devices is presented, highlighting the excellent electrostatic control on the heterojunction conduction. An optimized architecture for low power electrostatic actuation of VO₂ side of the junction, based on the collected experimental results, is proposed.

5 | 2D/2D Heterojunction devices

The final step in our project was the assembly of 2D/2D heterojunction devices, exploiting the same deterministic transfer setup exploited for the fabrication of VO_2/MoS_2 junctions. The aim is to demonstrate vertical band-to-band tunneling, so to enable the realization of 2D steep slope FETs. The first section is dedicated to the criteria underlying the choice of materials for the design of a 2D heterojunction TFET. Then the fabrication and detailed electrical characterization of $\text{WSe}_2/\text{SnSe}_2$ heterojunction devices are presented. Both room temperature NDR in the output characteristic and subthermal subthreshold slope in the $I_D(V_G)$ curve testify to the onset of a BTBT mechanism responsible for the conduction in the heterojunction. The obtained TFET are benchmarked against the performance of the WSe_2 FET built on the very same flake used in the heterojunction. Finally, a new device, combining the advantages of MOSFET and TFET topologies, is presented and demonstrated. This chapter is based on the work presented at IEDM 2019 and published in the conference proceedings [189].

5.1 Materials choice

In order to demonstrate the potential of 2D/2D systems for tunneling FET devices it is critical to properly select the pair of material candidates forming the heterojunction. In literature several materials have been identified as promising by relying on atomistic simulations of the band alignment and the resulting electronic transport [190, 191]. Moreover, several reports of trends toward negative differential resistance, or even actual measurements of room temperature NDR, have recently been presented in a variety of 2D systems [54, 97, 98, 192, 193]. The onset of BTBT conduction has been consistently reported in $\text{WSe}_2/\text{MoS}_2$, BP/SnSe_2 , BP/MoS_2 and $\text{WSe}_2/\text{SnSe}_2$ heterojunctions [54, 95, 192–196]. However, only few heterojunction devices actually achieved subthermal subthreshold slope [196, 197].

Some of the most important criteria for the selection of the best candidates for an heterojunction TFET are:

- proper band alignment at the junction, ideally broken band gap or at least staggered;
- good electrostatic control over the semiconductor doping of at least one of the sides of the junction;

- possibility of achieving simultaneously high hole and electron concentrations in the two sides of the heterojunction;
- air stable, easy to transfer 2D materials.

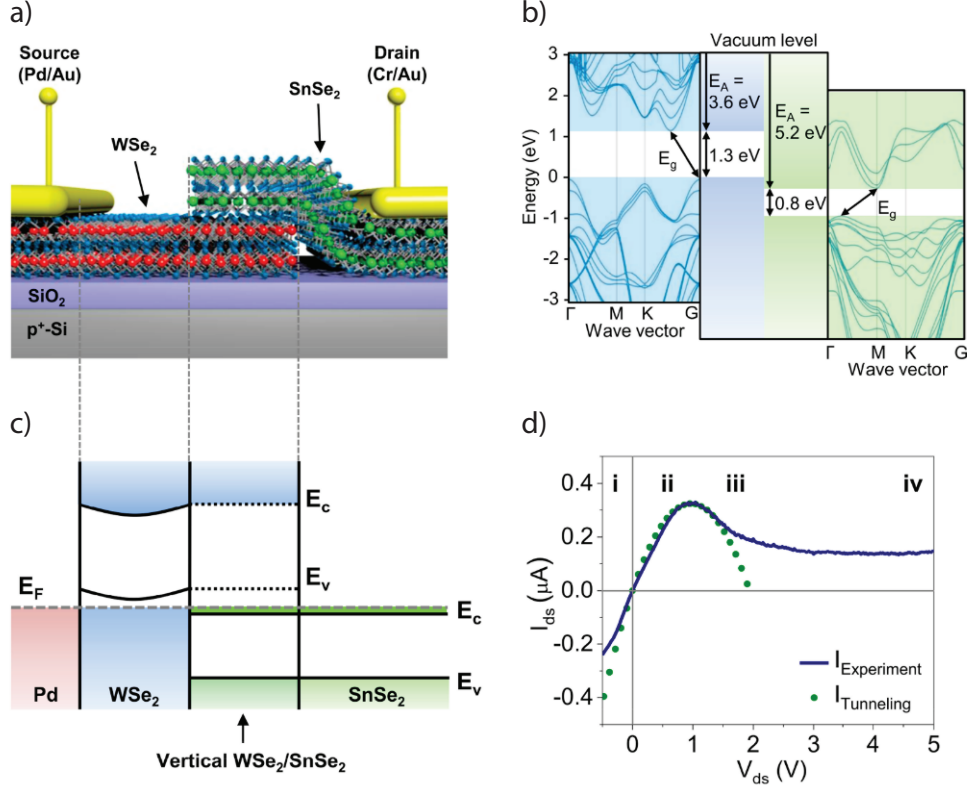


Figure 5.1: a) Schematic of a bottom gated $\text{WSe}_2/\text{SnSe}_2$ heterojunction device. b) Band structures of WSe_2 and SnSe_2 obtained from DFT calculations. The heterojunction is of type III, with broken band gap. c) Expected band alignment of the heterojunction and of the Pd contact. d) Experimental and theoretical fitting of the output characteristic of a representative $\text{WSe}_2/\text{SnSe}_2$ device exhibiting room temperature NDR. Results adapted from [54].

Based on this short wishlist we identified our optimal pair of materials in WSe_2 and SnSe_2 . As discussed in chapter 3, pristine WSe_2 is ambipolar. Its conduction can be easily tuned exploiting electrostatic control, so to obtain unipolar p or n type devices [46], and good values of hole and electron mobility have been demonstrated. Conversely, SnSe_2 is degenerately n doped, with an electron density quite independent from the gate bias applied [198, 199]. The expected band alignment for a $\text{WSe}_2/\text{SnSe}_2$ heterojunction is of the third type, providing a broken or nearly broken band gap potentially ideal for the onset of band to band tunneling, as shown in Figure 5.1c [54, 193, 198, 200]. Room temperature NDR has been demonstrated in devices based on this heterojunction (see Figure 5.1d), but to the best of our knowledge no pTFET with subthermal subthreshold slope at room temperature has been built using these materials.

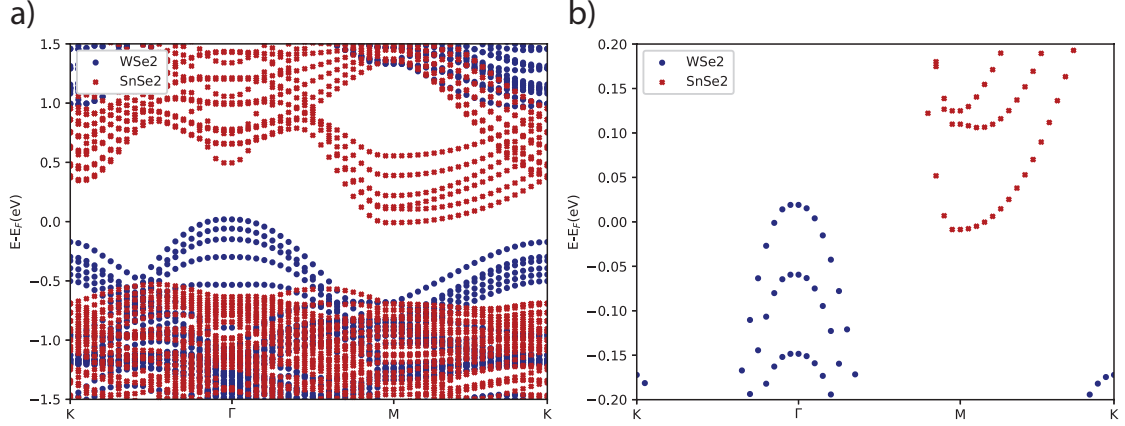


Figure 5.2: a) Band diagram of WSe₂ (blue) and SnSe₂ (red) derived from DFT calculations using meta-GGA functionals. b) Zoom in of the edges of WSe₂ valence band and SnSe₂ conduction band. The expected band alignment is of broken-band gap type, with an estimated energy overlap of 27 meV.

We confirmed the optimal band alignment of the WSe₂/SnSe₂ system by DFT calculations of the two materials bands using GGA functionals. In order to accurately model the band alignment of the heterostructure, VASP, a density functional theory (DFT) tool, is employed [201]. A supercell containing six layers of each material is constructed by applying a relative rotation of 30° and a small strain of 0.22 % to both layers, resulting in a hexagonal cell containing four units of WSe₂ and three units of SnSe₂ in their respective layers. Electronic structure calculations are performed using the generalized gradient approximation (GGA) of Perdew, Burke and Ernzerhof (PBE), with a 11x11x1 Monkhorst-Pack k-point grid and a 500 eV plane-wave cutoff energy [202]. The convergence criteria is set to less than 10⁻² eV/Å forces acting on each ion and a total energy difference smaller than 10⁻³ eV between two subsequent iterations. Van der Waals interactions are included through the DFT-D3 method of Grimme [203]. The resulting computed band structures of WSe₂ and SnSe₂ are shown in Figure 5.2a, where the bands have been colored to indicate the material from which they originate. A closer look at the derived band alignment is provided in Figure 5.2b, that shows a type III, broken gap with an estimated energy overlap of 27 meV.

5.2 WSe₂/SnSe₂ heterojunctions

5.2.1 Fabrication

The process flow designed for the fabrication of our WSe₂/SnSe₂ heterojunction devices is summarized in Figure 5.3a. A 50 nm thick HfO₂ film was deposited by atomic layer deposition on a silicon wafer. In order to define the bottom gate contact, we patterned a MMA/PMMA bilayer by electron beam lithography. We then evaporated and lifted-off 50 nm of tungsten (W). The bottom gate structure was completed by depositing 10 nm of HfO₂ in the same ALD reactor used for the first step.

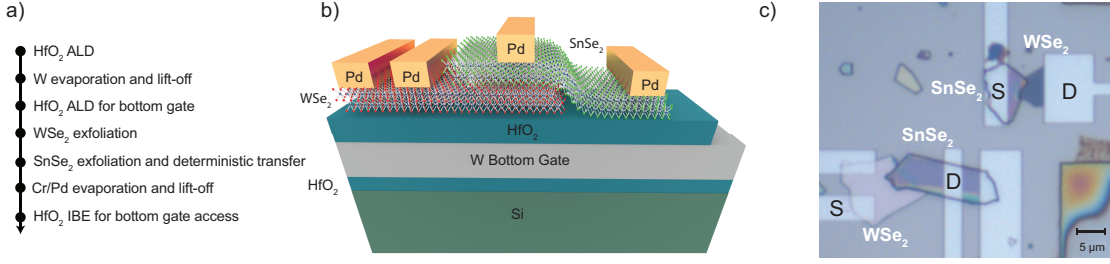


Figure 5.3: a) Summary of the main steps of the process flow followed for the fabrication of our 2D/2D heterojunction devices. b) Three dimensional representation of the final structure of the device. c) Optical image of two representative devices.

The WSe₂ and SnSe₂ bulk crystals were purchased by commercial providers, respectively *hq-graphene* and *2D Semiconductors*. WSe₂ flakes were mechanically exfoliated directly on the processed substrate. Ideal flakes with proper thickness, dimensions and placement were identified by optical microscopy. SnSe₂ flakes were exfoliated first on a PDMS stamp and then deterministically transferred on the selected WSe₂ flakes [42]. Source and drain contacts were then obtained by lift-off of a Cr/Pd stack (5 nm/50 nm) after a second EBL step on MMA/PMMA resist. Finally, in order to secure access to the W bottom gate we etched locally the dielectric by ion beam etching (IBE), using a PMMA layer as mask. A three dimensional schematic of the final structure is represented in Figure 5.3b. Figure 5.3c shows an optical image of two fabricated devices: it is possible to clearly distinguish the two flakes constituting the heterojunction, the overlap region and the Pd metallic contacts. Depending on the dimensions of the flakes, either two or four electrodes were deposited on the heterojunction, so to be able to characterize separately the single flakes and the heterostructure conduction mechanisms. Our devices are fabricated with 10 nm thick WSe₂ flakes and relatively thick, multilayer SnSe₂ flakes (thickness larger than 50 nm). Figure 5.4 shows an SEM image of a complete heterojunction device together with an AFM profile of a typical WSe₂ flake. A detailed process flow illustrating each step is presented in the appendix Figure A.4.

5.2.2 Electrical characterization

All the electrical measurements have been performed at room temperature and ambient conditions. Throughout the electrical measurements here presented, WSe₂ is used as the drain of the heterojunction device.

As a first step, we characterized the electrical properties of individual SnSe₂ and WSe₂ flakes taking advantage of the four Pd contacts deposited per device (see Figure 5.3b). Figure 5.5a shows the double-sweep transfer characteristic of a SnSe₂ FET measured at a drain to source bias of 10 mV. As expected, given the degenerate n doping typical of this 2D material, the gate bias has a very limited capability of modulating the conduction in the channel [198, 199], that cannot be depleted of electrons for the investigated range of voltages resulting in an extremely limited ON/OFF current ratio. The output characteristic in Figure 5.5b shows that a good ohmic contact is achieved between the Pd contacts and multilayer SnSe₂ flakes. For this measurement,

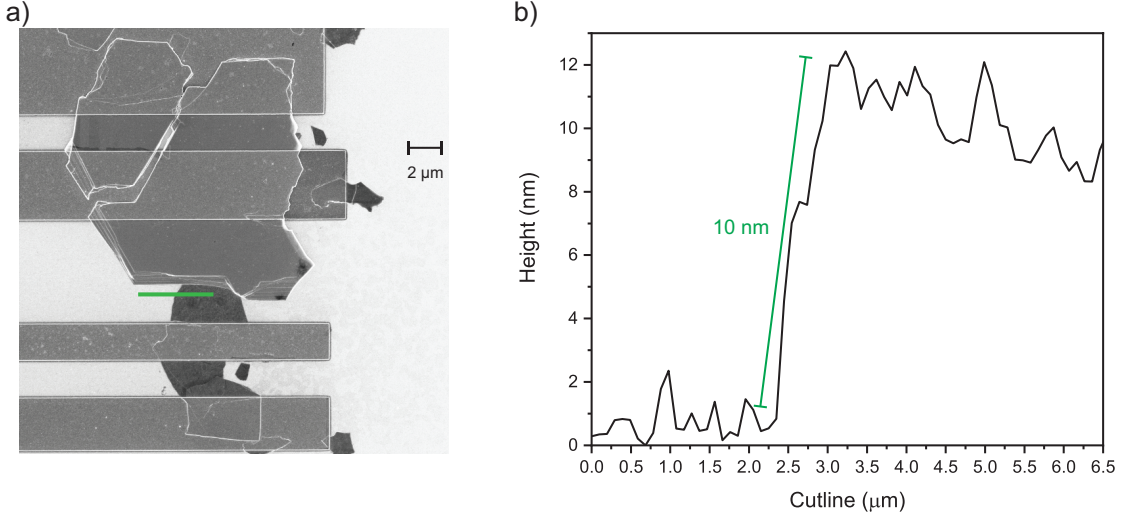


Figure 5.4: a) SEM image of a representative heterojunction device. The red line represents the cutline along which the profile in figure b) was measured by AFM. The extracted WSe₂ flake thickness is around 10 nm.

the gate bias was kept to 0 V.

The double sweep transfer characteristic of a representative WSe₂ FET (MOSFET 1) is reported in Figure 5.6a, where we group the results obtained for different values of the drain bias. The device exhibits a p-type polarity, with ON/OFF current ratio larger than 10⁶ and hysteresis below 250 mV. The n branch conduction is quite suppressed, and the device characteristic can be regarded as unipolar. The average subthreshold slope ranges from 90 to 110 mV/dec. Interestingly, these devices outperform both in terms of hysteresis and turn-on slope the bottom gated WSe₂ devices reported in chapter 3. The enhanced performance is likely due to the improved electrostatic coupling, deriving from the use of a metallic bottom gate contact rather than the silicon bulk.

The FET gate transconductance (g_m) is reported in Figure 5.6b and it shows a peak and saturation over the -0.5/-1 V window of gate bias, depending on the V_{DS} value. The hole mobility can be estimated applying the Y function method. The extracted Y function at $V_D = 100$ mV is shown in Figure 5.7, and from the fitting of the linear part of the curve a hole mobility of 1.6 cm²V⁻¹s₁ is obtained, comparable to state of the art results for alternative WSe₂ FETs. [46, 47, 204]. The output characteristic in Figure 5.8 shows that the contact between the Pd electrodes and WSe₂ is Schottky and no saturation of the output current is observed for the considered gate biases.

We then characterized the heterojunction devices, starting from a device (TFET 1) realized with the same WSe₂ flake used for MOSFET 1. The double sweep transfer characteristics for increasing values of the drain voltage is reported in Figure 5.9. With respect to the built-in WSe₂ FET, the heterojunction device exhibits a threshold voltage shifted by 250 mV to more negative values, with comparable hysteresis. The I_{ON} at $V_{DS} = 500$ mV reaches 10 nA/μm², slightly lower than MOSFET 1 current. Its subthreshold slope (SS) appears to be significantly improved. The transconductance dependence on the gate bias is shown in Figure 5.10. Again, a shift towards

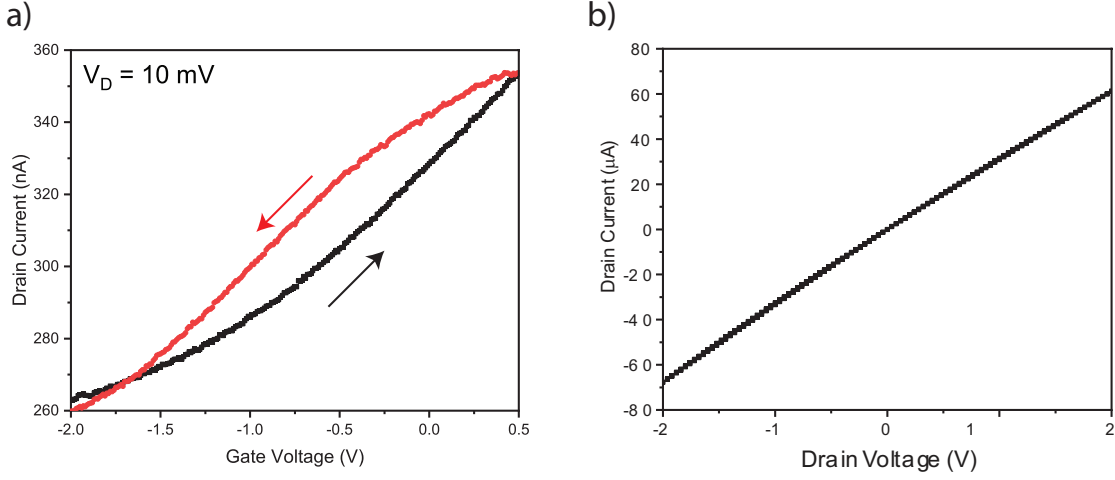


Figure 5.5: a) Double sweep transfer characteristic of a representative SnSe₂ FET measured applying $V_{DS} = 10 \text{ mV}$. The gate has a limited control on the conduction in the flake. b) Double sweep output characteristic showing a good ohmic contact between Pd electrodes and multilayer SnSe₂ FET. The gate voltage in this measurement is kept at 0 V.

more negative bias of the peaks and a decrease of the maximum value is observed with respect to MOSFET 1.

The heterojunction band diagram in Figure 5.11, drawn based on material properties documented in literature [54, 193, 200, 205, 206], shows a possible BTBT path between SnSe₂ conduction band (CB) and WSe₂ valence band (VB). Applying a small positive drain bias to WSe₂, electrons can tunnel from SnSe₂ to WSe₂ valence band to be then collected at the Pd drain contact. A negative bias applied to the bottom gate determines an upward shift of WSe₂ bands, corresponding to an increase of the allowed energies state overlap between SnSe₂ CB and WSe₂ VB and consequently of the heterojunction current. Conversely, a positive gate bias gradually reduces and then completely removes the overlap by shifting WSe₂ bands downward, switching off the tunneling current.

Figure 5.12 shows TFET 1 room temperature output characteristic in semilog and linear scales, measured at different values of the bottom gate voltage. A clear NDR region is present in the characteristics, and both its position and amplitude are efficiently modulated by the gate bias. The evolution of the peak and valley currents together with the associated voltages is shown in Figure 5.13. As clearly visible in Figure 5.12b, positive gate voltages determine a right shift of the NDR region and a decrease of the peak to current ratio, whose maximum value exceeds 10 for $V_G = -1 \text{ V}$. This suggests the onset of a robust BTBT mechanism, that can be efficiently modulated electrostatically by the bottom gate.

As mentioned, the structure of our device offers the unique opportunity of benchmarking the heterojunction TFET against the WSe₂ MOSFET built on exactly the same flake. Figure 5.14a shows a direct comparison of the transfer characteristics of TFET 1 and the corresponding MOSFET, both measured at $V_{DS} = 500 \text{ mV}$. The TFET threshold voltage has been shifted so to match

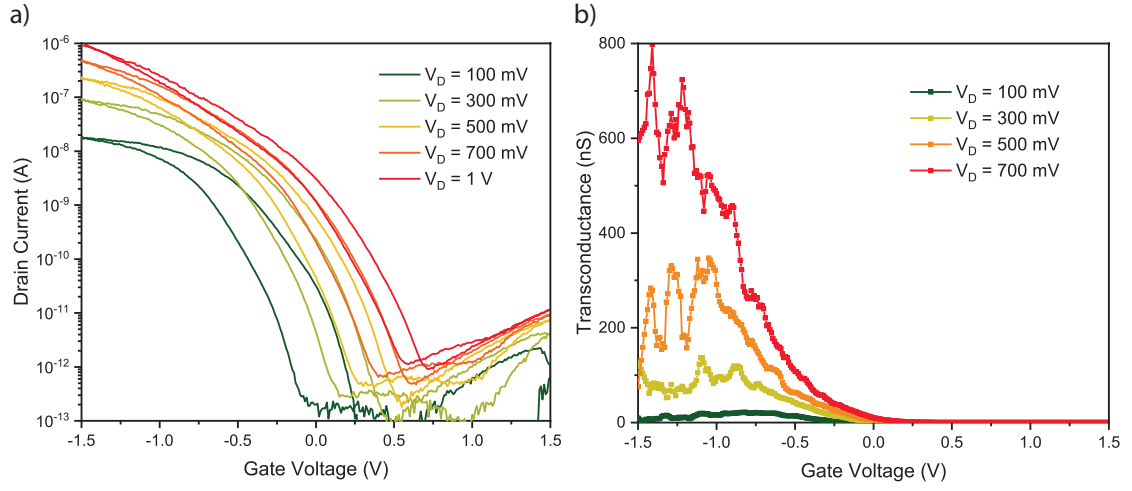


Figure 5.6: a) Double sweep transfer characteristic of a representative WSe₂ FET (MOSFET 1) at increasing drain biases. b) Corresponding gate transconductance.

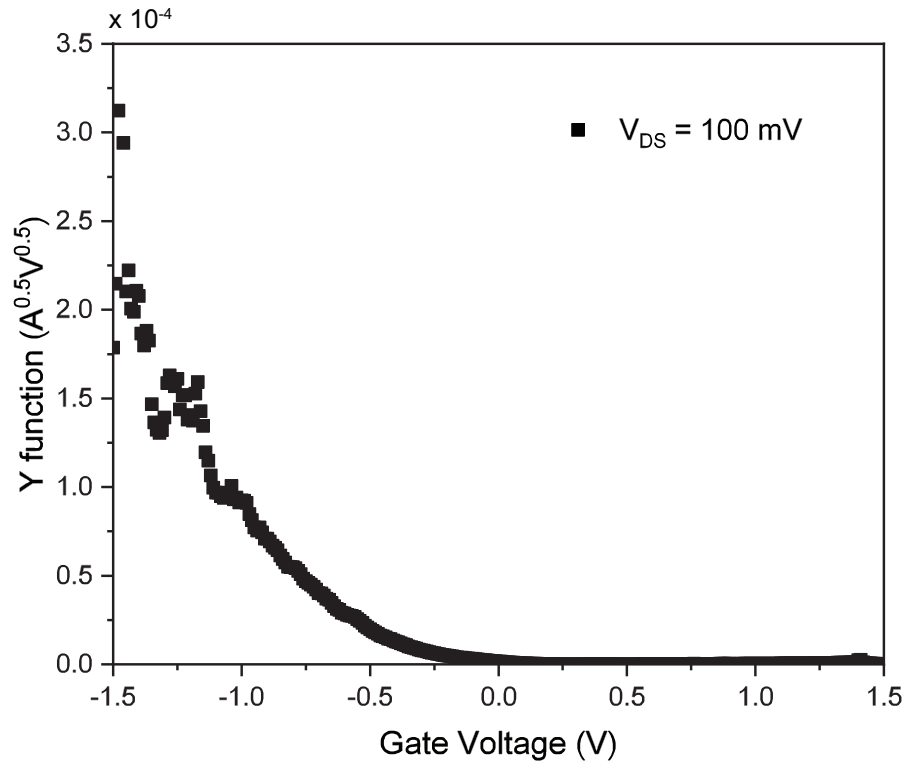


Figure 5.7: Y function obtained from a representative WSe₂ FET (MOSFET 1) at $V_{DS} = 100$ mV.

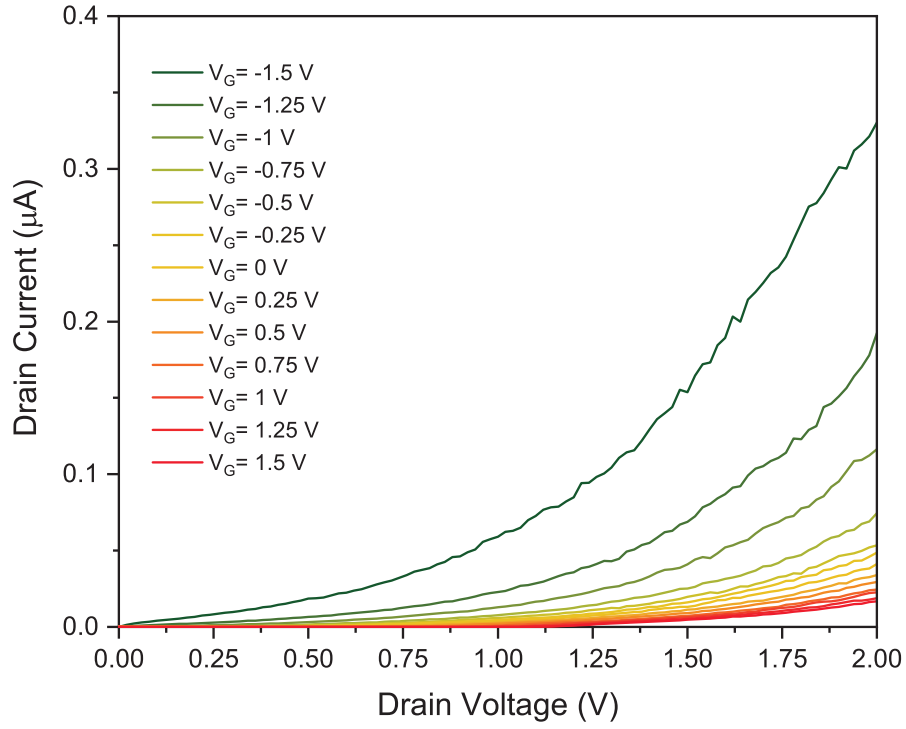


Figure 5.8: Output characteristic of a WSe₂ FET (MOSFET 1) at increasing gate biases.

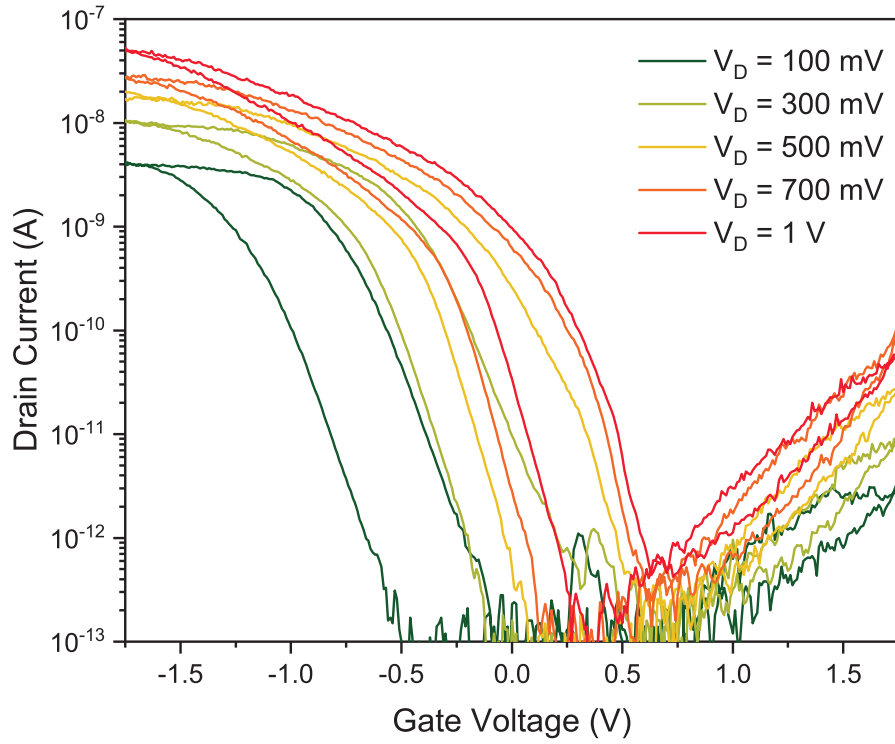


Figure 5.9: Double sweep transfer characteristic of a representative WSe₂/SnSe₂ device (TFET 1) at increasing drain biases.

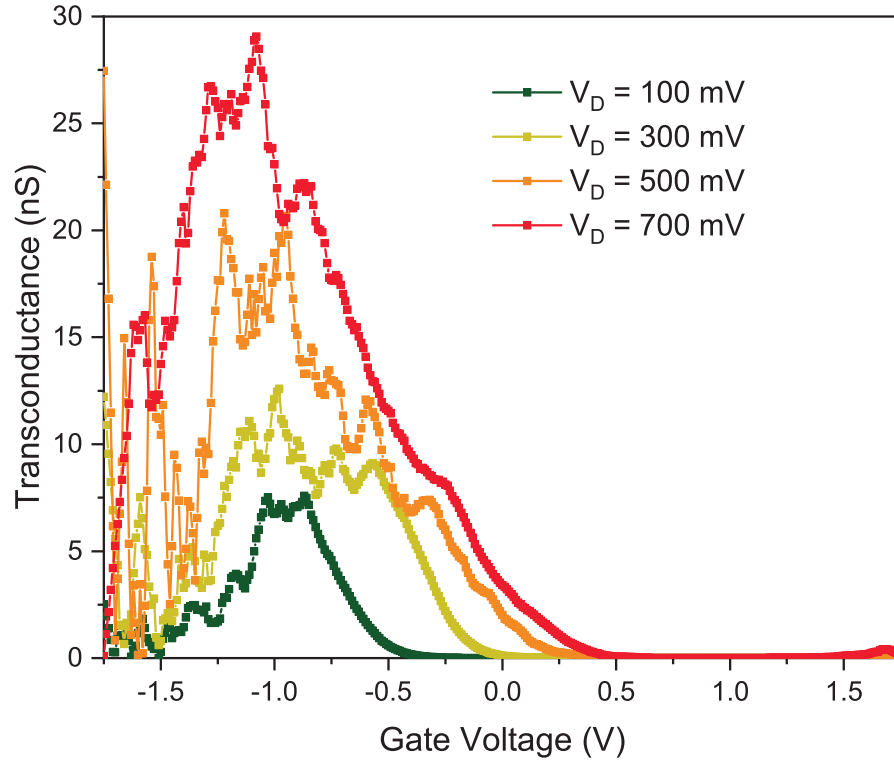


Figure 5.10: Transconductance of WSe₂/Sn₂ TFET 1 at increasing values of the drain bias.

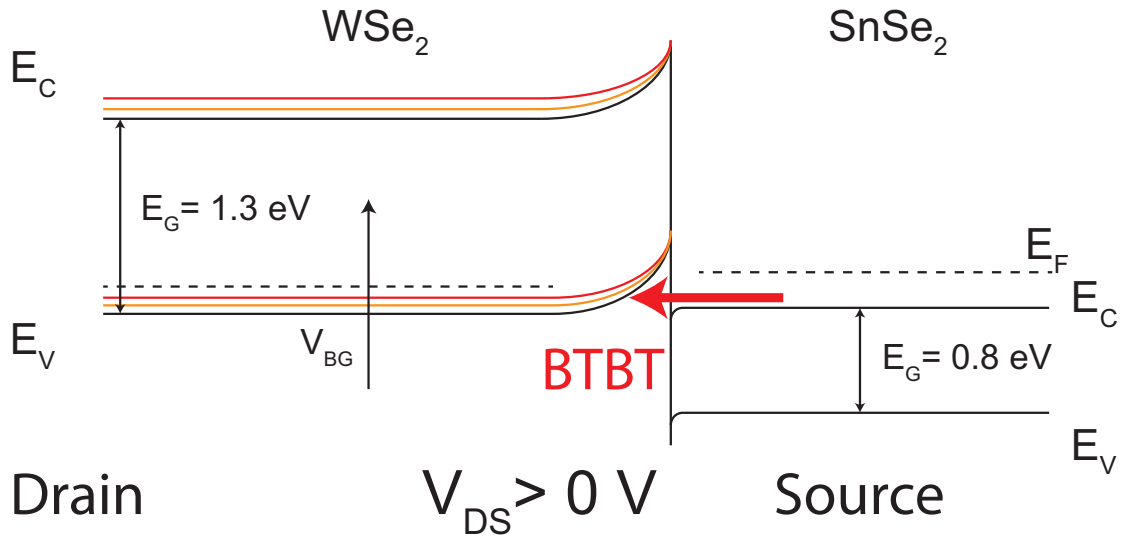


Figure 5.11: Qualitative band diagram of the WSe₂/SnSe₂ heterojunction, highlighting the proposed BTBT path and the impact of the bottom gate bias on WSe₂ bands and energy overlap between the two materials of the junction.

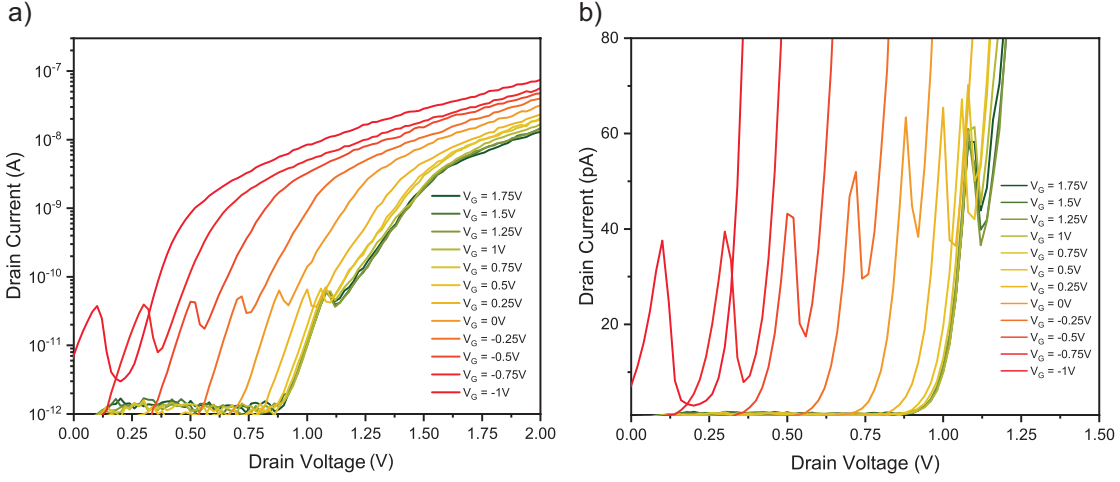


Figure 5.12: a) TFET 1 output characteristic in semilog scale for different values of the gate bias. b) Same characteristic in linear scale, so to better appreciate the NDR region.

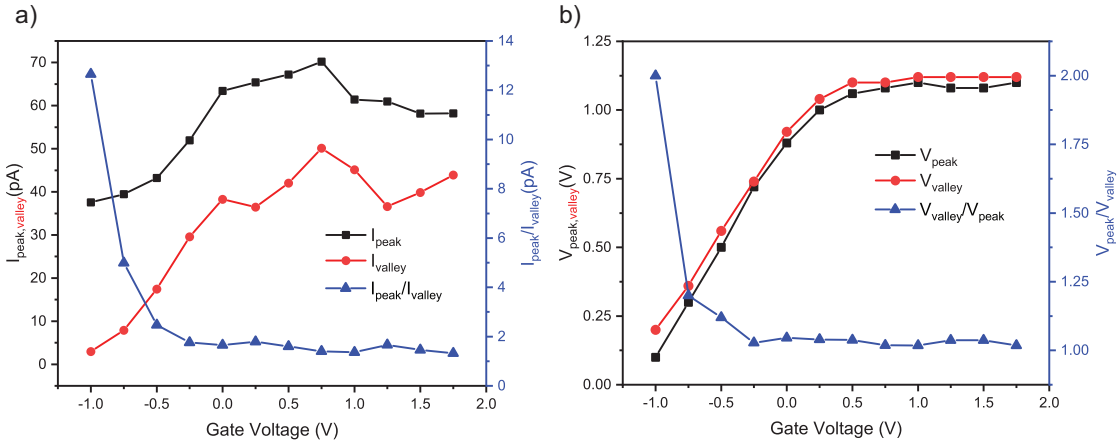


Figure 5.13: a) Evolution of TFET 1 NDR peak and valley current, together with their ratio, as a function of the applied gate bias. b) Corresponding variation of the peak and valley voltages and of their ratio.

the WSe₂ FET one to favor a more immediate comparison. TFET 1 shows both a lower I_{OFF} current and better subthreshold slope compared to the MOSFET, crossing its characteristic at low current level and indeed outperforming the WSe₂ FET over almost two orders of magnitude of the output current. It is important to notice that the gate leakage current for both the devices is below 10 pA over the entire bias window investigated. The point SS vs the drain current is plotted in Figure 5.14b for both devices. TFET 1 not only reaches subthermal minimum SS, but it maintains a sharper output characteristic of MOSFET 1 over more than two orders of magnitude of the output current.

A second comparison between another TFET (TFET 2) and its built-in WSe₂ FET is carried on in Figure 5.14c. The TFET threshold has been shifted to match the MOSFET one. In this case it is even clearer that the TFET outperforms the MOSFET over the entire subthreshold region, clearly crossing the WSe₂ transfer characteristic. The gate leakage current for both the devices is consistently low. Figure 5.14d shows the SS as a function of the output current, and it confirms that TFET 2 reaches subthermal swing and sustain lower SS of its corresponding WSe₂ FET for more than three orders of magnitude of the output current. To the best of our knowledge, these devices are the first to outperform MOSFETs built in the same material system and architecture since the results reported in 2011 by Intel (see Figure 2.8) [67, 68].

Table 5.1 summarizes the performance of our devices compared to the state of the art 2D/2D TFET reported in literature. We achieve the lowest point SS, while maintaining excellent $I_{\text{ON}}/I_{\text{OFF}}$ ratio and demonstrating the possibility of co-integrating the heterojunction TFET and the 2D MOSFET [54, 193, 196, 207]. The demonstrated device provides further insight into the potential of 2D/2D heterojunctions for tunneling devices.

Finally, Figure 5.14e collects the transfer characteristic of three heterojunction TFETs built on two chips processed in parallel. All the curves have been measured at a drain bias of 500 mV. Gate leakage current, subthreshold slopes and ON/OFF current ratios for the three devices are comparable, showing the robustness and relatively low variability of our fabrication process. Figure 5.14f shows the subthreshold slope of the three devices as a function of the output current. TFET 3 reaches our best point swing, $SS = 35$ mV/dec at room temperature. Remarkably, all the fabricated TFET devices achieve subthermionic turn-on slopes.

The subthreshold slope is a fundamental parameter to qualify the performance of our heterojunction devices for digital applications. In order to assess the potential for analog electronics as well, it is useful to compare the transconductance efficiency of the TFET against its built-in WSe₂ FET. The transconductance efficiency is defined as the ratio between the gate transconductance and the drain current (g_m/I_D) [208]. The resulting curve for TFET 2 is shown in Figure 5.15. The heterojunction device outperforms its built-in MOSFET for more than three orders of magnitude of the output current and it reaches more than twice the peak transconductance efficiency.

5.2.3 Dual Transport Steep Slope FET (DT-FET)

Figure 5.16 presents a qualitative best case scenario when comparing MOSFET and TFET transfer characteristics. Because of the steeper turn-on deriving from the BTBT current, a TFET can outperform the MOSFET in the low current/low power region. Conversely, the MOSFET

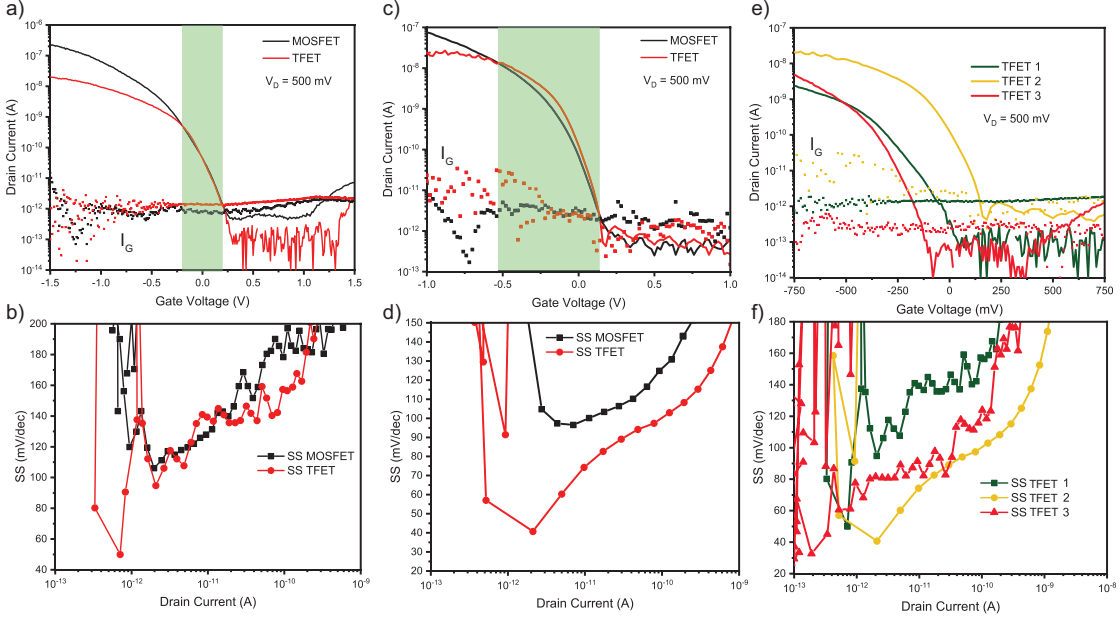


Figure 5.14: a) Transfer characteristics of TFET and MOSFET 1, built on the same WSe₂ flake. The threshold voltage of the TFET has been shifted so to match the MOSFET one and favor the performance comparison. b) Point subthreshold slope as a function of the output current for MOSFET and TFET 1. c) Transfer characteristic of a second TFET (TFET 2) compared directly to its built-in MOSFET characteristic. Also in this case the TFET threshold has been shifted so to match the MOSFET one. d) Point SS as a function of the drain current for MOSFET and TFET 2. e) Comparison of the transfer characteristics of three TFET devices fabricated in parallel. f) Point SS as a function of the drain current for the three TFET. All achieve subthermionic subthreshold slope. For all the reported measurements, the drain to source bias was fixed to 500 mV. The reported transfer characteristics include also the gate leakage for both TFETs and MOSFETs.

thermionic I_{ON} current in a given material system and technology is intrinsically larger than TFET one, so that it is the most indicated device for high current/high frequency applications. The inset in Figure 5.16 shows the equivalent circuit and the output characteristic of the device proposed and demonstrated in this work: the Dual Transport Steep-Slope FET (DT FET). By connecting in parallel a TFET and MOSFET built on the same flake with properly engineered threshold voltages, it is possible to harvest the benefits of both the steep BTBT current and high thermionic ON current. The DT FET turns on following the TFET characteristic, and then reaches the high current values provided by the MOSFET thermionic injection.

Figure 5.17 shows a colored SEM image of one of our fabricated heterojunction devices together with the schematic of the proposed DT FET. By using the middle WSe₂ contact as common drain and grounding both the sources of the heterojunction TFET and the WSe₂ FET, we can realize a new device, that we term 'Dual Transport Steep Slope FET' (DT FET). The resulting output current of the DT FET is the sum of the TFET and MOSFET currents. If their threshold voltages are properly engineered so to have $V_{Th,TFET} > V_{Th,MOSFET}$, the DT FET inherits the characteristic ad-

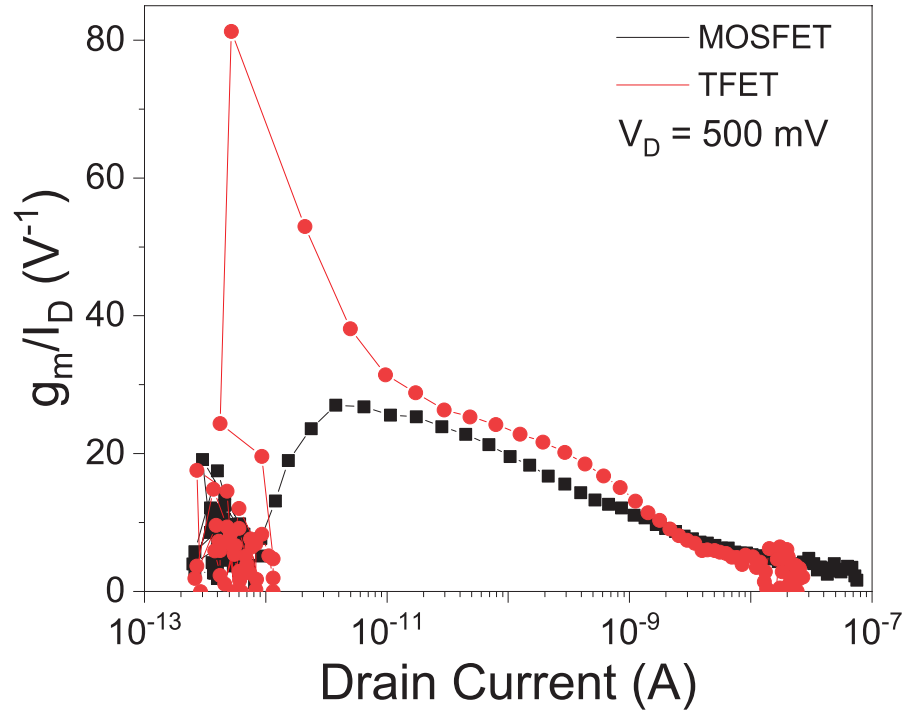


Figure 5.15: Comparison between TFET 2 and its built-in WSe₂ FET transconductance efficiencies.

2D TFETs	Material System	MOS-FET cointg.	SS min (mV/dec) @ RT	I _{ON} /I _{OFF}
This work	WSe₂/SnSe₂	Yes	35 mV/dec @ V_{DS} = 500 mV	>10⁵ @ V_D = 500 mV
Roy et al., APL, 2016 [187]	WSe ₂ /SnSe ₂	No	100 mV/dec @ V _{DS} = -1 V	~10 ³ @ V _D = -1 V
Fan et al., ACS Nano, 2019 [51]	WSe ₂ /SnSe ₂	No	90 mV/dec @ V _{DS} = 500 mV	~10 ⁶ @ V _D = 500 mV
Yan et al., Small, 2017 [190]	WSe ₂ /SnSe ₂	No	50 mV/dec @ V _{DS} = 500 mV	10 ⁵ @ V _D = 500 mV
He et al, ADM, 2018 [203]	MoS ₂ /WSe ₂	No	200 mV/dec @ V _{DS} = 1V	10 ⁵ @ V _D = 1 V
DT FET (This work)	WSe₂/SnSe₂ + WSe₂ FET	Yes	Measured: 100mV/dec @ V_{DS}=600mV Optim.: 55 mV/dec @ V_{DS}=500mV	Meas.: 10⁵ @ V_D = 600mV Optim.: 10⁵ @ V_D = 500mV

Table 5.1: Performance comparison between our WSe₂/SnSe₂ TFET and DT FET with respect to alternative 2D/2D tunneling devices reported in literature. Data obtained from [54, 193, 196, 207]

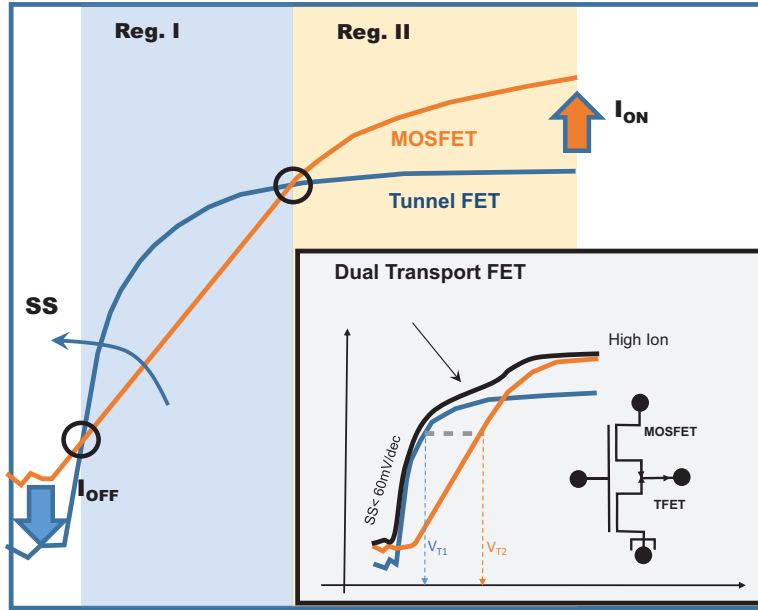


Figure 5.16: Qualitative comparison of MOSFET and TFET transfer characteristic. Inset: expected characteristic of the DT FET, harvesting the respective advantages of MOSFET and TFET.

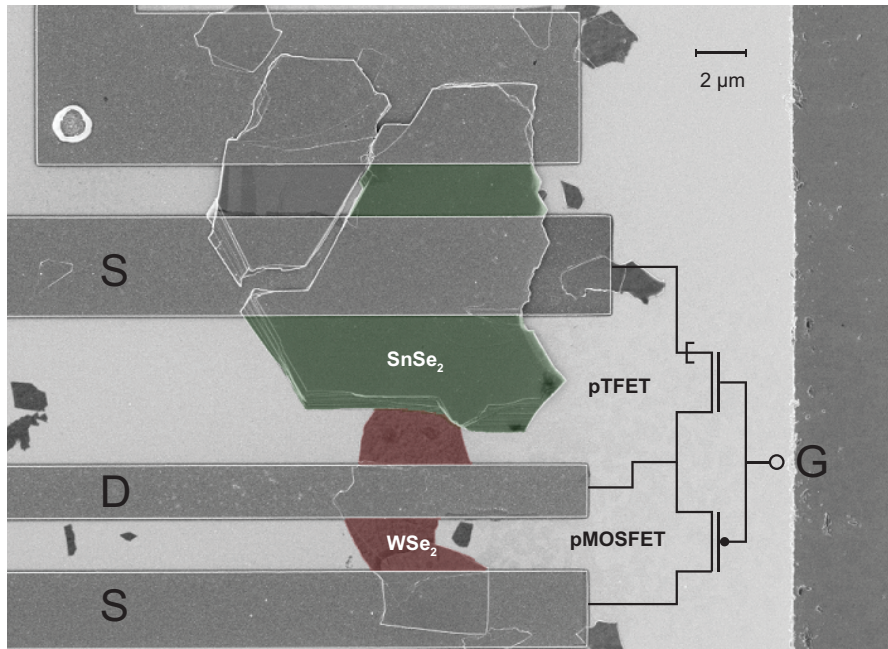


Figure 5.17: SEM image of a representative WSe₂/SnSe₂ heterojunction device and circuit schematic of the proposed Dual Transport Steep Slope FET. The p-type heterojunction TFET is connected in parallel to the p-type WSe₂ MOSFET.

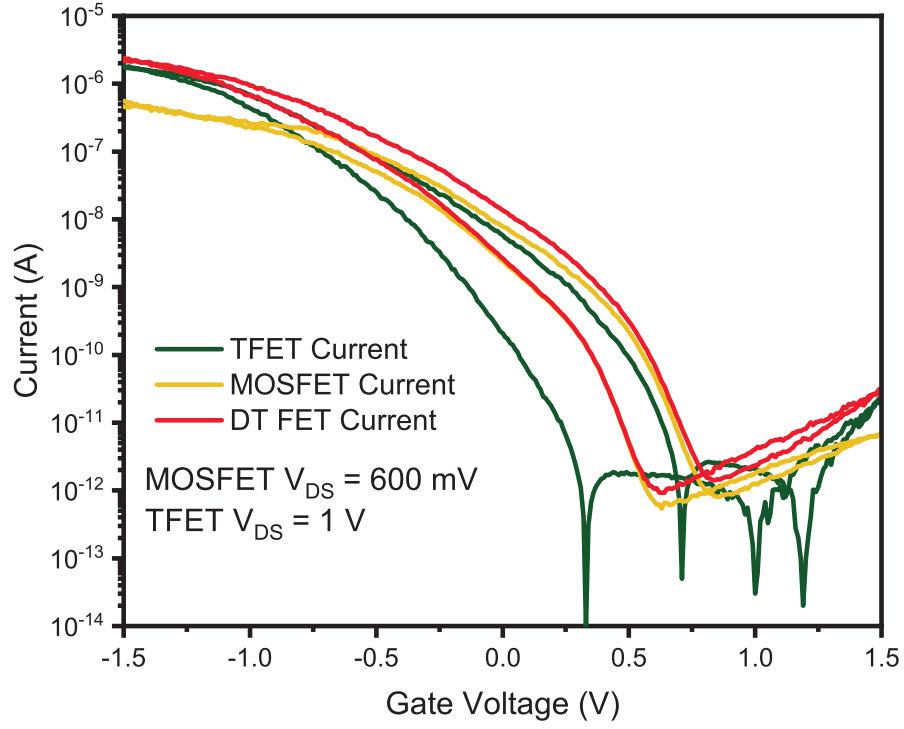


Figure 5.18: Transfer characteristic of the measured DT FET together with the characteristics of TFET 1 and its built-in MOSFET.

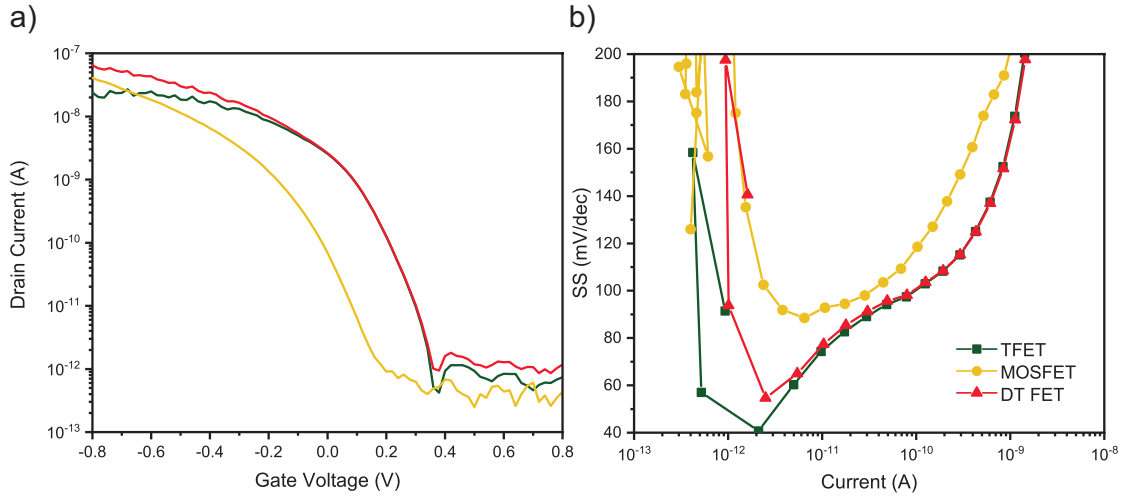


Figure 5.19: a) transfer characteristic and b) subthreshold slope of an optimized DT FET obtained from the shifted transfer characteristic of TFET and MOSFET 2.

vantages of both the devices: steep subthreshold slope due to BTBT current and high thermionic I_{ON} current (see inset of Figure 5.16).

In order to validate the working principle of the device, we measured TFET 1 and its MOSFET in the discussed DT FET configuration, using the middle contact as drain and the two lateral Pd electrodes as source. Unfortunately, our fabricated TFETs have a threshold voltage more negative than the associated FETs (as shown in Figure 5.9). Therefore, the optimal condition for DT FET operation is not satisfied. We decreased the differences in the two thresholds by applying different V_{DS} voltages at the two devices. The DT FET transfer characteristic is shown in Figure 5.18, together with the characteristics of the constituent TFET and MOSFET. The relative V_{DS} are 1 V for the TFET and 600 mV for the MOSFET. The DT FET current turns on following the MOSFET because of its smaller threshold voltage and it follows the TFET characteristic only at large negative gate bias. By engineering the V_{Th} mismatch, for example by means of a top gate for the WSe_2 MOSFET, it is possible to achieve a DT FET with steep turn-on and high I_{ON} . Figure 5.19 shows an optimized DT FET transfer characteristic and subthreshold slope obtained starting from TFET 2 characteristic and shifting it so to have a threshold voltage slightly higher than its MOSFET. The resulting device exhibits the advantages of both its components: a subthermionic SS (Figure 5.19b) and a high I_{ON} .

5.2.4 Summary

We have demonstrated the first ever co-integrated subthermionic 2D/2D $WSe_2/SnSe_2$ vertical ptype tunnel FET and WSe_2 MOSFET realized on the very same flake. The device is fabricated by deterministic assembly of the van der Waals heterojunction on top of a tungsten/ HfO_2 bottom gate stack. DFT calculations confirm that this heterojunction presents an optimal broken gap band alignment, resulting in room temperature subthermal subthreshold slope and sizeable, gate tunable negative differential resistance observable in the output characteristic. A record low point subthreshold slope of 35 mV/dec at $V_{DS} = 500$ mV has been demonstrated, while maintaining $I_{OFF} < 0.1$ pA/ μm^2 and a ON/OFF current ratio exceeding 10^5 . The fabricated pTFET clearly outperforms the built-in WSe_2 MOSFET, crossing its characteristic over several orders of magnitude of the output current and providing better digital and analog performance in the subthreshold region. The demonstrated heterojunction device provides a new insight in the potential of 2D/2D systems for the realization of high performance steep-slope devices. Moreover, the possibility of cointegrating on the same flake both MOSFET and TFET with no increase in the process flow complexity paves the way to new circuit topologies able to harvest the steep TFET turn-on characteristic granted by the band to band tunneling conduction mechanism and the high MOSFET thermionic ON current.

6 | Conclusions and Perspectives

The objective of the project summarized in this thesis was the study and demonstration of the potential of 2D materials for the realization of electronic devices for sensing and computing applications. A technology platform has been created so to efficiently transfer 2D flakes and fabricate sharp, low defect heterojunction devices in EPFL fabrication facility and NanoLab laboratory. The impact of both the contacts workfunction and the gate dielectric deposition strategy on the properties of a variety of 2D materials has been studied by investigating double gated MOS-FETs. Mixed dimensionality VO_2/MoS_2 heterojunctions have been fabricated and characterized in order to assess both electrical conduction and photovoltaic properties. In particular, the VO_2 unique temperature dependent characteristics have been successfully exploited to fine tune the photoresponsivity of a VO_2/MoS_2 photodiode. Moreover, top gated VO_2/MoS_2 devices pave the way for the achievement of a true electrostatic control of the IMT transition in functional oxide three terminal devices. Finally, the potential of 2D/2D heterojunctions was demonstrated realizing a vertical tunneling $\text{WSe}_2/\text{SnSe}_2$ pTFET with subthermal subthreshold slope at room temperature and able to outperform WSe_2 MOSFETs built in on the same WSe_2 FET. A detailed comparison of the two co-integrated devices is carried on and a new device configuration combining the advantages of both 2D MOSFET and TFET, labeled dual transport steep slope FET, is proposed and preliminary demonstrated.

6.1 Summary of contributions to the research field

The main contributions of this work are the following:

1. **BP FETs with pre-patterned embedded contacts.**

We demonstrated the possibility of embedding metallic electrodes in the oxide layer used as receiving substrate for the mechanical exfoliation of black phosphorous flakes. The use of pre-patterned contacts allows to greatly reduce the exposure of this sensitive, fragile material to ambient atmosphere during the fabrication process. Moreover, by embedding the electrodes a smooth substrate with reduced topography is achieved, granting a good exfoliation yield and low mechanical stress on the transferred flakes. By selecting the workfunction of the contacts, both n and p type BP FETs were demonstrated on the same chip. The same structure can be conveniently adapted to any unstable or oxidizing 2D material for the minimization of the contamination during the processing.

2. High-k dielectric deposition on WSe₂ flakes.

The deposition of high quality, low leakage and low hysteresis hafnium oxides on WSe₂ was demonstrated by fabricating double gated devices. A frequency analysis of the hysteresis dynamics was presented to validate the good performance exhibited by our top gate WSe₂ FETs. An average subthreshold slope approaching 100 mV/dec and a gate leakage current below 1 pA/ μ m have been consistently demonstrated for top gated devices.

3. Multi gate electrostatic control on the conduction in double gated WSe₂ FET.

We studied the impact of top and back gate on the conduction of WSe₂ channels controlled by sweeping the opposite gate bias. Back gated devices behave as enhancement mode FETs, with ON/OFF current ratio exceeding 10^6 and a average subthreshold slope of 200 mV/dec. By applying a negative bias to the top gate, both the hysteresis and the SS can be improved at the cost of a small decrease of the ON current level. Conversely, top gated devices measured with positive back gate bias behave as depletion FETs. The average subthreshold slope approaches 100 mV/dec, while the ON/OFF ratio can be boosted to 10^6 by increasing the positive back gate bias.

4. First demonstration of devices based on VO₂/MoS₂ heterojunctions.

We fabricated the first ever two-terminal devices based on VO₂/MoS₂ heterojunctions. The electrical properties and the impact of the temperature dependent band diagram of vanadium dioxide have been carefully characterized and explained in relation to the variation of the band alignment at the junction. The heterojunction has a rectifying characteristic both at room temperature and above VO₂ IMT. Moreover, we demonstrated the possibility of electrically triggering the IMT of the VO₂ side of the junction.

5. Characterization of VO₂/MoS₂ photodiodes with tunable photoresponsivity.

We demonstrated the possibility of realizing VO₂/MoS₂ based photodetectors with high sensitivity and fast response. Moreover, the heterojunction photoresponsivity can be efficiently tuned by controlling the device temperature, thanks to the strongly temperature dependent VO₂ properties.

6. Prototyping of gated VO₂/MoS₂ heterojunctions.

Gated VO₂/MoS₂ heterojunction devices were fabricated and electrically characterized. The obtained FET exhibits a ON/OFF current ratio larger than 10^3 and a subthreshold slope as small as 130 mV/dec. The demonstrated good electrostatic control over the heterojunction conduction opens the door to a new class of three terminal devices based on VO₂ where the electron density in the functional oxide is modulated by tuning the properties of a second semiconductor.

7. WSe₂/SnSe₂ tunnel FET with room temperature subthermal subthreshold slope.

We demonstrated WSe₂/SnSe₂ bottom gated heterojunction devices with the aim of achieving a reliable BTBT conduction mechanism. The realized devices can be operated as pTFET with record minimum point SS of 35 mV/dec for this type of heterojunctions and room temperature NDR observed in the output characteristic. Moreover, the proposed structure enables the direct performance comparison between pTFET and WSe₂ MOSFET fabricated on the very same flake. The tunnel FET outperforms the WSe₂ FET in the subthreshold region, maintaining better characteristic over more than three orders of magnitude of the output current.

8. Dual transport steep slope FET: harvesting the advantages of both MOSFET and TFET devices.

A new type of device, named dual transport steep slope FET is proposed and demonstrated. The DT FET aims to combine the steep turn-on of a TFET with the high thermionic ON current of a MOSFET starting from our $\text{WSe}_2/\text{SnSe}_2$ heterojunctions. By connecting in parallel the heterojunction pTFET and the WSe_2 pMOSFET, the output current measured is the sum of the two devices contributions. By engineering the relative threshold voltages it is indeed possible to follow the TFET characteristic at turn on, while reaching the MOSFET current at larger gate biases. The resulting DT FET inherits the subthermal subthreshold slope while maintaining the large thermionic ON current.

6.2 Perspectives

The presented work represents a first exploration of the potential of 2D materials and heterojunctions for both sensing and computing applications. Several further steps are required to assess the actual potential and to improve the encouraging features observed. Among the topics to be investigated directly connected to the discussed projects we can individuate a short representative list:

- **Optimization of dielectric deposition on WSe_2 and other 2D materials.**

We demonstrated the possibility of growing good quality HfO_2 on WSe_2 following the deposition of an Al seed layer that is then oxidized in air to obtain a thin Al_2O_3 layer. It is important to evaluate the impact of different seed layers on WSe_2 FETs, in particular in the effort of demonstrating complementary high performance transistors. A variety of readily oxidized metals can be investigated for the fabrication of top gated 2D devices: the ideal candidate should have a corresponding oxide with a high dielectric constant so not to degrade the capacitive coupling and a sufficiently low leakage.

- **Gated photodiodes based on VO_2/MoS_2 heterojunctions.**

The fabricated VO_2/MoS_2 photodiodes show good, temperature tunable photoresponsivity. We also demonstrated how it is possible to gate such heterojunctions achieving a good electrostatic control. The next step would therefore be the realization of photodiodes gated using a transparent top contact, like indium tin oxide (ITO). The gate electrode would provide a further degree of freedom for the programming of the device photoresponse.

- **Optimized VO_2/MoS_2 three terminal devices.**

As discussed in Chapter 4, the fabricated VO_2/MoS_2 three terminal devices can be efficiently electrostatically controlled. However, the resulting current density is not sufficient to trigger the VO_2 IMT. The proposed optimized structure (see Figure 4.29b) would allow a considerable reduction of the electrical power required for the phase transition. For sufficiently thin VO_2 films, we expect to be able to electrostatically trigger the IMT, thus demonstrating a true steep-slope FET based on vanadium dioxide.

- **Threshold engineering in $\text{WSe}_2/\text{SnSe}_2$ TFET and DT FET optimization**

The results obtained from the $\text{WSe}_2/\text{SnSe}_2$ heterojunctions are encouraging. A further im-

provement of the TFET performance could be easily achieved by scaling the thickness of the bottom gate dielectric, currently constituted by 10 nm of HfO_2 . Moreover, the annealing of the devices following the contacts deposition could help to consistently boost the ON current level. In order to demonstrate the optimal operation of the DT FET, the WSe_2 MOSFET threshold voltage should be smaller with respect to the 2D/2D TFET turn-on bias. We envision two alternatives to achieve this condition: the deposition of two different metals as contacts to the WSe_2 flake or the deposition of a top dielectric and electrode on the semiconducting flake. The first solution is easier from a fabrication standpoint since it requires only a further mask and lift-off. However, estimating the impact of metals workfunction on the actual value of a 2D FET threshold voltage is not straightforward. The fabrication of a top gate on the WSe_2 FET would surely be more challenging, but it would offer the fundamental possibility of adjusting dynamically the MOSFET threshold so to provide on the fly tunability.

- **$\text{WSe}_2/\text{SnSe}_2$ flexible TFET**

The device structure presented in Chapter 5 could be quite easily replicated on a flexible substrates. Indeed, we started experimenting the fabrication of WSe_2 FETs on a polyimide substrate, that would enable interesting applications for both sensing and the study of strain impact on the device performance. The process flow developed for flexible $\text{WSe}_2/\text{SnSe}_2$ TFETs is quite similar to the one presented in this work, since the deposition of the bottom gate stack can be performed directly on a silicon wafer coated by polyimide. The polyimide can be then removed by dissolving an underlying metallic adhesion layer.

More in general, the research on 2D materials for electronics applications is ever expanding. New two dimensional materials are discovered each year, and even more are theoretically expected to be isolated down to their monolayer. It is not easy to outline the most interesting topics to investigate in such a wide landscape. Nevertheless, we believe that the following arguments are of particular fundamental and industry interest:

- **Integration of heterojunction devices at CMOS back end of the line.**
- **Flexible sensors based on 2D devices.**
- **Contact resistance reduction.**

A | Appendix: Detailed process flows

A.1 Black phosphorous FETs

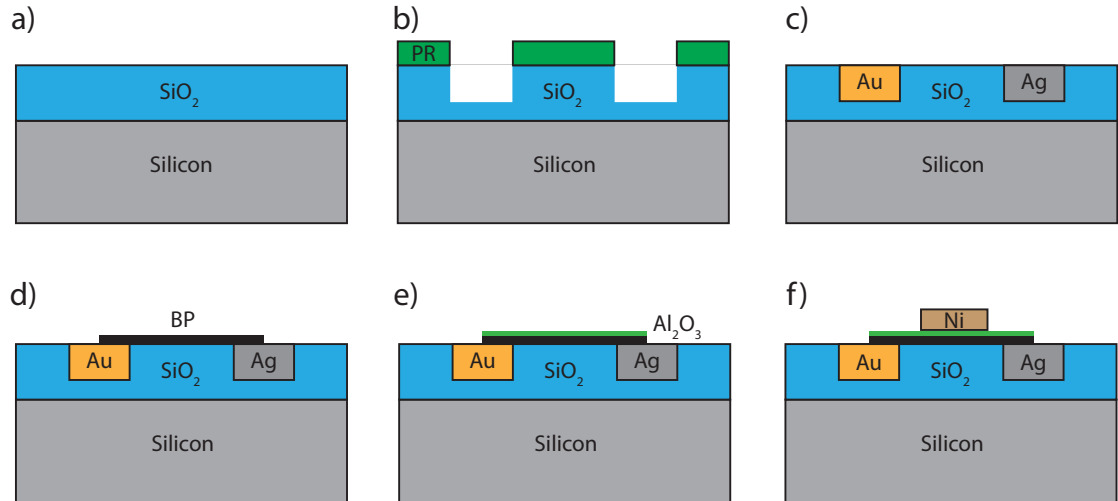


Figure A.1: a) Starting substrate: silicon wafer oxidized so to obtain 280 nm SiO₂. b) Laser maskless photolithography and dry etching of 50 nm boxes in SiO₂ in CHF₃ and SF₆ plasma. c) Evaporation of 50 nm Au or Ag and lift-off. d) Black phosphorous flake exfoliation. e) 15 nm Al₂O₃ ALD. f) EBL on MMA/PMMA bilayer resist, evaporation and lift-off of 50 nm of Nickel.

A.2 Double gate WSe₂ FETs

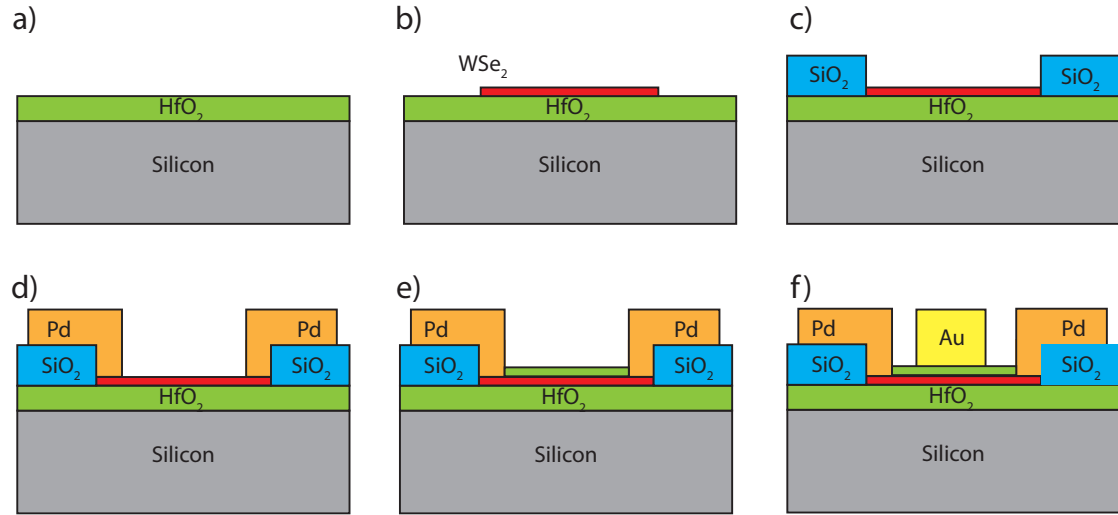


Figure A.2: a) ALD of 20 nm of HfO₂ on a silicon wafer. b) Exfoliation of WSe₂ flakes. c) EBL on MMA/PMMA resist, sputtering of 50 nm SiO₂ and lift-off. d) EBL on MMA/PMMA resist, evaporation of 50 nm of Pd and lift-off. e) Evaporation of a 1.5 nm thick Al seed layer and ALD of 5 nm of HfO₂. f) Final EBL step on MMA/PMMA, evaporation and lift-off of Au.

A.3 VO_2/MoS_2 heterojunction devices

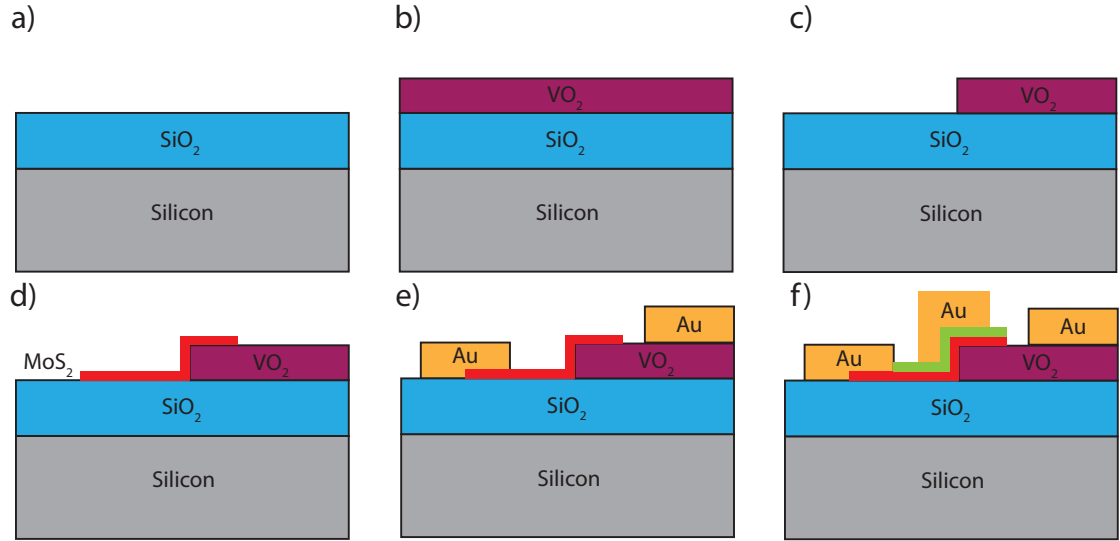


Figure A.3: a) Starting substrate: silicon wafer oxidized so to obtain $2\ \mu\text{m}$ of SiO_2 . b) DC magnetron sputtering of $75\ \text{nm}$ of VO_2 . c) Laser maskless photolithography and VO_2 wet etching in diluted commercial Cr etch solution. d) MoS_2 flakes deterministic transfer. e) EBL on MMA/PMMA bilayer, evaporation of $50\ \text{nm}$ of Au and lift-off. f) Al seed layer evaporation, $5\ \text{nm}$ HfO_2 ALD, EBL, Au evaporation and lift-off to complete the gate stack of three terminal heterojunction devices.

A.4 WSe₂/SnSe₂ heterojunction TFET

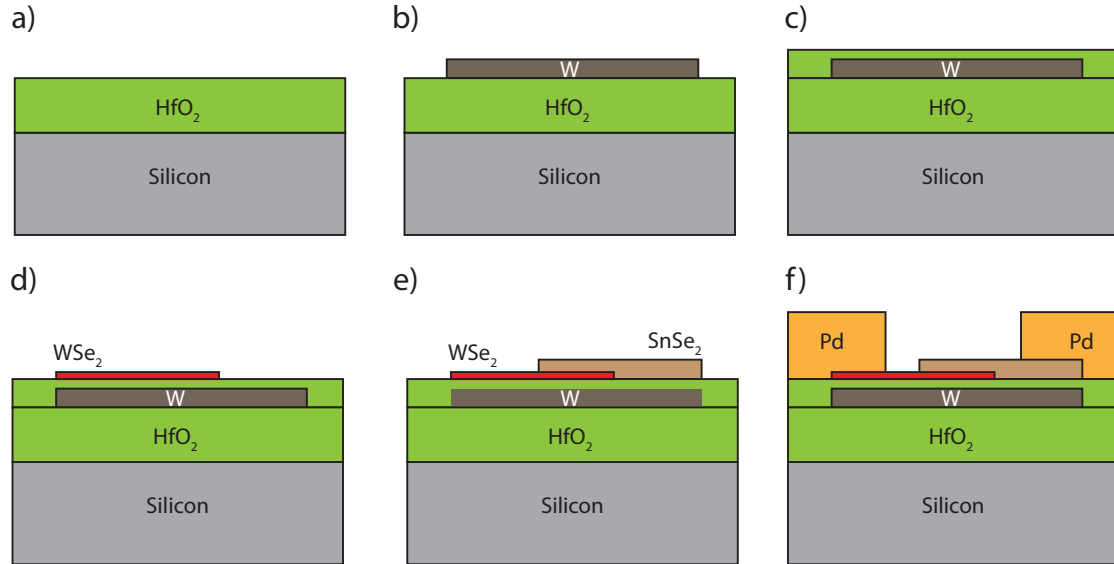


Figure A.4: a) ALD of 50 nm of HfO₂ on a silicon wafer. b) Laser maskless photolithography on nLOF negative resist, 50 nm W sputtering and lift-off. c) Second ALD step for the deposition of 10 nm thick HfO₂ as bottom gate dielectric. d) Exfoliation of WSe₂ flakes. e) Deterministic transfer of SnSe₂ flakes. f) EBL on MMA/PMMA bilayer, 5 nm/50 nm evaporation and lift-off of Cr/Pd contacts.

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- [2] N. Oliva, E. Casu, W. Vitale, I. Stolichnov, and A. Ionescu, “Polarity Control of Top Gated Black Phosphorous FETs by Workfunction Engineering of Pre-Patterned Au and Ag Embedded Electrodes,” *IEEE J. Electron Devices Soc.*, vol. 6, 2018, ISSN: 21686734. DOI: 10.1109/JEDS.2018.2817289.
- [3] N. Oliva, E. A. Casu, M. Cavalieri, and A. M. Ionescu, “Double gate n-type WSe₂ FETs with high-k top gate dielectric and enhanced electrostatic control .,” *Eur. Solid-State Device Res. Conf.*, pp. 114–117, 2018. DOI: 10.1109/ESSDERC.2018.8486867.
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- [5] N. Oliva, Y. Y. Illarionov, E. A. Casu, M. Cavalieri, T. Knobloch, T. Grasser, and A. M. Ionescu, “Hysteresis dynamics in double-gated n-type WSe₂ FETs with high-k top gate dielectric,” *IEEE J. Electron Devices Soc.*, pp. 1–1, 2019, ISSN: 2168-6734. DOI: 10.1109/JEDS.2019.2933745.
- [6] N. Oliva, E. A. Casu, C. Yan, A. Krammer, T. Rosca, A. Magrez, I. Stolichnov, A. Schueler, O. J. Martin, and A. M. Ionescu, “Van der Waals MoS₂/VO₂ heterostructure junction with tunable rectifier behavior and efficient photoresponse,” *Sci. Rep.*, vol. 7, no. 1, pp. 1–8, 2017, ISSN: 20452322. DOI: 10.1038/s41598-017-12950-y.
- [7] N. Oliva, E. A. Casu, W. A. Vitale, I. Stolichnov, and A. M. Ionescu, “Complementary black phosphorous FETs by workfunction engineering of pre-patterned Au and Ag embedded electrodes,” *Eur. Solid-State Device Res. Conf.*, pp. 102–105, 2017, ISSN: 19308876. DOI: 10.1109/ESSDERC.2017.8066602.

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- [9] E. Casu, W. Vitale, N. Oliva, T. Rosca, A. Biswas, C. Alper, A. Krammer, G. Luong, Q. Zhao, S. Mantl, A. Schuler, A. Seabaugh, and A. Ionescu, “Hybrid phase-change — Tunnel FET (PC-TFET) switch with subthreshold swing < 10mV/decade and sub-0.1 body factor: Digital and analog benchmarking,” in *2016 IEEE Int. Electron Devices Meet.*, IEEE, Dec. 2016, pp. 19.3.1–19.3.4, ISBN: 978-1-5090-3902-9. DOI: 10.1109/IEDM.2016.7838452.
- [10] E. A. Casu, W. A. Vitale, M. Tamagnone, M. M. Lopez, N. Oliva, A. Krammer, A. Schuler, M. Fernandez-Bolanos, and A. Ionescu, “Shunt capacitive switches based on VO₂ metal insulator transition for RF phase shifter applications,” in *2017 47th Eur. Solid-State Device Res. Conf.*, IEEE, Sep. 2017, pp. 232–235, ISBN: 978-1-5090-5978-2. DOI: 10.1109/ESSDERC.2017.8066634.
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STRENGTHS

- Semiconductor devices design and simulation.
- Cleanroom microfabrication expertise.
- Multidisciplinary, international cooperation.
- Electrical measurements and testing.
- Statistical data analysis for devices performance assessment.
- Project management.

EDUCATION

2016-2020

PHD MICROSYSTEMS AND MICROELECTRONICS, EPFL

2013-2015

MSC MICRO AND NANOTECHNOLOGIES, EPFL/GRENOBLE INP/POLITO

PROFESSIONAL EXPERIENCE

2016-2020

NANOELECTRONIC DEVICES LABORATORY (NANOLAB), EPFL

LAUSANNE, SWITZERLAND

“AT THE END OF THE SCALING: 2D MATERIALS TO THE RESCUE”, DOCTORAL THESIS

I managed the development of 2D/3D and 2D heterojunction devices for sensing and computing applications. Core tasks included the design, simulation, microfabrication and electrical characterization of TFETs as energy efficient switches. Such devices can deeply affect the market of low-power, distributed nodes that are key for the Internet of Things revolution. In addition, I worked on the development and fabrication of functional oxides based devices. I trained and aided collaborators from EPFL start-ups for advanced electrical measurements using automated setups.

2015

PIAZZA MICRO AND NANOSYSTEMS LABORATORY (PMANS), CMU

PITTSBURGH, PENNSYLVANIA, USA

I developed, simulated and fabricated Aluminum Nitride (AlN) piezoelectric MEMS transformers that have been included in my design of an inductorless, IC compatible DC-DC converter. The circuit topology was implemented in a PCB demonstrator.

2015

HYBRID LABORATORY, INSTITUT NÉEL

GRENOBLE, FRANCE

Focus on material analysis by AFM and Raman spectroscopy on superconducting 2D materials.

TECHNICAL SKILLS

ELECTRICAL CHARACTERIZATION

Steady state DC, RF, cryogenic and automatic wafer scale measurements, Cascade and Karl Suss probers, training and collaboration with EPFL start-ups for electrical measurements, statistical analysis of results.

SEMICONDUCTOR DEVICES SIMULATION

Sentaurus TCAD, Advanced Design System (ADS), Cadence, COMSOL, Analytical modelling.

MICROFABRICATION

Cleanroom proficiency, maskless lithography, Ebeam lithography, dry and wet etching, Atomic Layer Deposition (ALD), thin film deposition, PDMS.

MATERIAL ANALYSIS

Atomic Force Microscopy (AFM), Raman spectroscopy, Scanning Electron Microscopy (SEM), X-Ray Diffraction (XRD).

PROJECT MANAGEMENT

Technical reporting, budget management, problem solving, scientific setup design and purchase, lab organization, team building, wide international experience, coordination of inter-laboratory projects.

IT

Matlab, OriginLab, COMSOL, C++, Latex, Illustrator, Office Suite (ECDL certificate).

LANGUAGES

- Italian, native language.
- English, fluent written and spoken. FCE certificate level C1.
- French, B1 level in written and oral.
- German, beginner.

PUBLICATIONS AND AWARDS

- One article in the top 100 Material Science chart for 2017 Scientific Reports.
- Six first author articles: five IEEE, one Nature Publishing Group.
- Two presentations at IEEE International Electron Devices Meeting (IEDM 2017 and 2019)

EXTRA ACTIVITIES

- Member of Italian mountain club, shelter manager during summer over several years.
- Hiking, trekking, bouldering.
- Voracious reader.

PERSONAL DETAILS

Italian citizenship, 28 years old, Swiss residence permit B, Swiss driving license (Type B)