A CMOS Image Sensor Pixel Combining Deep Sub-Electron Noise With Wide Dynamic Range

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Abstract—This letter introduces a 5-transistors (5T) implementation of CMOS Image Sensors (CIS) pixels enabling the combination of deep sub-electron noise performance with wide dynamic range (DR). The 5T pixel presents a new technique to reduce the sense node capacitance without any process refinements or voltage level increase and features adjustable conversion gain (CG) to enable wide dynamic imaging. The implementation of the proposed 5T pixel in a standard 180nm CIS process demonstrates the combination of a measured high CG of $250 \mu\text{V}/e^-$ and low CG of $115 \mu\text{V}/e^-$ with a saturation level of about $6500 e^-$ offering photo-electron counting capability without compromising the DR and readout speed.

Index Terms—CMOS, 4T, 5T, CIS, conversion gain, sub-electron noise, wide dynamic.

I. INTRODUCTION

PHOTOELECTRON counting capability emerges as the ultimate limit to reach for CMOS image sensors (CIS). Indeed, CIS performance has been dramatically increased since their first development [1] on several aspects including speed, resolution or power consumption. The sensitivity of CIS has been, also, significantly improved in terms of quantum efficiency, dark current and fill-factor [1]. Recently, remarkably low noise pixels have been presented [2]–[5]. Photon counting capability has been reached in [3], [4] using process refinements resulting in lower sense node (SN) capacitance increasing the pixel conversion gain. This has been achieved by shaping the potential profile along the signal path in a way that isolates the SN from the transfer gate (TG) overlap capacitance and reducing the overlap with the reset transistor by shrinking its channel width from the SN side. These process modifications resulted in high conversion gains exceeding $300 \mu\text{V}/e^-$ which is at the origin of the low read noise performance. But this improvement comes at the cost of additional process refinements and a low full-well capacity of only $200 e^-$. The same idea of isolating the SN capacitance from the transfer and reset gates overlaps has been exploited in [5]. But in this case, the reset transistor has been completely removed and replaced by an implant generating

Fig. 1. The proposed PPD based 5T pixel architecture with the control timing diagram showing the difference between the high CG and low CG modes.

the reset with a punch-through effect. This technique resulted in a read noise of $0.27 e^-_{\text{RMS}}$ after cooling the sensor to -10°C with a conversion gain of $220 \mu\text{V}/e^-$. The downside of this technique is the fairly high required reset voltage of 25 V incompatible with standard CMOS and therefore generated off-chip. In addition, this technique involves some process modifications since additional implants are used and also leads to a relatively low full-well capacity of $1500 e^-$.

In this letter, we present a novel 5T pixel, integrated in a standard 180nm CIS process, without any process refinements and offering photo-electron counting capability without dynamic range (DR) penalty thanks to a dual conversion gain feature. The proposed pixel demonstrates a conversion gain (CG) adjustable between $250 \mu\text{V}/e^-$ and $115 \mu\text{V}/e^-$ with a saturation level of $6500 e^-$. The low SN capacitance is achieved by isolating the SN from the reset and TG overlap capacitances thanks to an additional gate. That same gate is also used to tune the CG. The low SN capacitance

Manuscript received April 3, 2020; accepted April 13, 2020. Date of publication April 16, 2020; date of current version May 21, 2020. The review of this letter was arranged by Editor O. Manasreh. (Corresponding author: Assim Boukhayma.)

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Color versions of one or more of the figures in this letter are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/LED.2020.2988378

Fig. 2. Idealistic potential profile across the photoelectrons path starting from the PPD, going to the IN through the TX1 TG and then to the SN through the second gate TX2. (a) corresponds to the SN charge dump. (b) depicts the IN node setting to an intermediate voltage between the pin voltage and the SN one. (c) represents the SN reset and (d) the charge transfer.

is then complemented with a low readout noise achieved by implementing an in-pixel thin oxide PMOS source follower (SF) with an optimal sizing as suggested in [6], [7].

II. THE PROPOSED 5T PIXEL ARCHITECTURE AND WORKING PRINCIPLE

Fig. 1 shows a schematic view of the proposed 5T pixel and its corresponding timing diagram. Compared to a conventional 4T scheme, this pixel features an intermediate node (IN) that can be isolated from the SN by means of an additional gate allowing an important reduction of the SN capacitance. The reset phase consists in three steps. First, the RST switch is closed connecting IN to V_{RST} . While V_{RST} is set to VDD, the potential barrier between IN and SN is lowered by setting TX2 to a voltage V_{TX2H1} in order to dump the charge from the SN as depicted in **Fig. 2**. TX2 is set back to 0 in order to split the IN and SN and freeze the SN voltage at its maximum level. V_{RST} is then switched to a lower voltage V_{RSTL} between the pin voltage of the PPD V_{pin} and $V_{SN,max}$. After this step, the reset switch is opened again to freeze the IN voltage at a value V_{IN} as depicted in **Fig. 2**. The last step of the reset phase consists in setting TX2 to a voltage V_{TX2H2} making the barrier between the IN and SN equal or slightly higher than V_{IN} as shown in **Fig. 2**. In this way, any excess charge transferred to IN would diffuse towards the SN. After lowering back TX2, the SN reset voltage $V_{SN,rst}$ is sensed. Transferring the charge integrated in the PPD to the SN takes place by pulsing both TX1 and TX2 as depicted in **Fig. 2**. TX1 is pulsed to a value V_{TX1H} in order to set the voltage under the TG between the PPD pin voltage V_{pin} and the intermediate node voltage V_{IN} while TX2 is pulsed again to transfer this charge to the SN. The signal corresponds to the difference between the SN voltage after reset $V_{SN,rst}$ and the one sensed after the transfer $V_{SN,transfer}$.

III. TEST AND CHARACTERIZATION

The proposed pixel is implemented in a 240 by 80 array fabricated in a 180 nm CIS process. The pixel layout features a pitch of 10 μm with a fill factor of 60% mainly limited by the minimum distance between the PPD and the PMOS SF wells imposed by the layout rules. Note that multiple gated PPDs can share the same IN, TX2 gate and SF stage in order to reduce the pixel pitch. The chip embeds analog buffers to drive the output voltage of the pixel to an external ADC. In order to assess the impact of the proposed technique on the conversion gain, the pixels are characterized using the photon transfer curve (PTC) by plotting the signal variance as a function of the mean value for different light exposures [8]. The PTC is

Fig. 3. Measured PTC in both low CG mode obtained by sharing the SN with the IN, and high CG mode, obtained by splitting the IN and the SN.

linear when the shot noise dominates and the slope of this linear part corresponds to the conversion gain. **Fig. 3** shows the measured PTC of the 5T pixel for both high and low CG configurations. The high CG configuration is performed by controlling the pixel following the timing diagram of **Fig. 1** and setting V_{RSTL} to 1.76 V, V_{TX1H} to 1.2 V, V_{TX2H1} to 2.2 V and V_{TX2H2} to 1.5 V. The low CG configuration is performed by connecting the IN with SN. **Fig. 3** shows that the PTC curve follows a linear trend demonstrating a shot noise dominance in both modes. The high CG curve deviates from its linear trend for higher charge transfers suggesting that other noise mechanisms like kTC noise take place when the TX2 transistor goes out of saturation regime. The split of IN from SN allows a successful increase of the CG to about $250 \mu V/e^-$ compared to $115 \mu V/e^-$ in low CG mode. The high CG corresponds to an SN total capacitance of 0.64 fF. The contribution of the thin oxide minimum size PMOS SF is estimated from calculation and simulation to be 0.4 fF accounting for an oxide capacitance density of $9 \text{ fF}/\mu m^2$, a width and length of 0.2 μm . Hence the SN remaining contribution related to the parasitic coupling with the neighboring metal lines, the junction capacitance of the n+ implant and the overlap with the splitting gate is as low as 0.24 fF, making the SF gate contribution to the SN capacitance the dominant component. This gives another reason for implementing a thin oxide SF. Indeed the minimum thick oxide SF width and length allowed by the foundry for the used process are 0.45 μm and 0.6 μm , with a gate oxide capacitance density of $4.5 \text{ fF}/\mu m^2$, resulting in larger minimum SF gate capacitance of about 0.81 fF which is close to the double of the gate capacitance of a minimum size thin oxide transistor. In order to verify the full well capacity of the proposed pixel for this test configuration, **Fig. 3** shows

Fig. 4. Measured response to LED light for low and high CG modes demonstrating linear response to light for both configurations.

Fig. 5. PCH obtained at room temperature without amplification.

the measured PTC of the proposed 5T pixel up to saturation in low CG mode. The PTC collapses around 0.65 V which corresponds to a pixel full well of more than $5600 e^-$. This measurement confirms that the proposed technique allows achieving high CGs without compromising the pixel DR. Note that this DR can be even further improved by increasing the capacitance of the IN. Fig. 4 shows the response to light from a red LED measured from the proposed 5T pixel for both low CG and high CG configurations. The LED illumination is controlled by a current generator in the pseudo-linear region. Fig. 4 demonstrates a linear response to light and confirm the CG measurement conclusion of Fig. 3. Indeed the ratio between the slopes of the two linear responses to LED light corresponds to the ratio between high and low CG. The readout noise is measured at the output of the readout chain composed of a low noise on-chip buffer and an off-chip 19 bits ADC after which a correlated multiple sampling of order 4 is applied in digital domain. Thanks to the high CG of $250 \mu V/e^-$ and optimized PMOS SF, the read noise is as low as $0.32 e^-_{RMS}$. This result is confirmed by Fig. 5 obtained by plotting the histogram of 1500 pixel outputs while the chip is exposed to very low input light. The histogram features peaks and valleys where each peak corresponds to a charge quantum. The presence of a peak at $-1 e^-$ suggests the presence an asymmetry between the rising and falling edges of TX_2 or a leakage at the level of the SN.

Fig. 6. Bright to dark lag measurement showing the outputs of 4 consecutive readouts, normalized to the first readout, in the dark after a bright exposure for both the proposed pixel and a reference 4T pixel.

IV. DISCUSSION

The proposed pixel involves charge diffusion through the IN during the transfer. This may give rise to possible limitations related to excess noise, incomplete charge transfer or pixel-to-pixel non-uniformity especially if the control voltages are not set properly. Regarding the noise during the charge transfer, the TX_2 transistor operates in saturation regime and therefore behaves as a current source pumping the charge from the source node (IN) to the drain node (SN). After the transient charge transfer, an approximately stationary regime is reached in which both kTC noise and shot noise related to TX_2 become negligible. Concerning the incomplete charge transfer, Fig. 6 shows the lag measurements for both the proposed 5T pixel and a reference 4T pixel present on the same chip and implementing the same PPD. The 5T pixel exhibits higher lag due to the lower voltage applied on TX_1 and the additional diffusion path separating the IN from the SN. However this lag increase is not dramatic since the charge transfer in standard CIS 4T pixels is already limited either by internal diffusion or the presence of a potential barrier underneath the TG [9], [10]. Regarding the photo-response non-uniformity (PRNU), a measurement in HCG mode have been performed on a subset of 1500 pixels. The dynamic PRNU corresponds to 0.8% which is similar to the one obtained on standard 4T pixels from the same foundry [7] implementing similar SFs. This suggests that this CG variation is mainly due to the SF gate size spatial variation. Future research should cover the impact on the saturation level and consider larger pixel arrays.

V. CONCLUSION

High CG is key for deep-subelectron noise pixels based on PPD and in-pixel SF. A new PPD based 5T pixel scheme enhancing the conversion gain is presented. It enables reaching CG as high as $250 \mu V/e^-$ in a standard 180 nm CIS process without any process refinements for SN capacitance reduction, fully operating at 3.3 V without the need of any high voltage source and without compromising the DR or readout speed. This pixel has also the advantage of featuring an in-pixel adjustable conversion gain allowing for DR extension without degrading the noise performance.

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