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Scalable Solid State Bus Tie Switch for Flexible Shipboard Power Systems

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***Abstract*—The need to increase efficiency and reduce operating cost of shipboard DC power distribution networks results in a desire to increase the operating voltage of such installations to the medium voltage levels. Devices such as solid state bus-tie switches are an essential component of such systems, as they allow for system reconfigurations and prevent fault propagation across different sections of the system. This paper presents a scalable solid state bus-tie switch topology designed initially for low voltage power distribution networks, but easily scalable in terms of voltage and current. The use of a single active device greatly increases simplicity and reliability of the solution. The ability to extend the current and voltage ratings has been verified on the prototypes through extensive experimental tests in parallel and series connection, respectively. Several methods for fault detection are discussed and further verified experimentally.**

***Index Terms*—Fault protection, Marine equipment, Microgrids, Scalability**

I. Introduction

In existing commercial applications, DC shipboard power distribution networks (PDNs) have proved preferable to their AC conterparts at the low voltage level ($\leq 1\,\mathrm{kV}$) due to increased system flexibility and efficiency. The economic and operational advantages demonstrated by such solutions at the LV level promoted interest in increasing the total installed power of such vessels above the power level of $20\,\mathrm{MW}$ - $30\,\mathrm{MW}$. Above these power levels, LVDC systems become voluminous, heavy and overall impractical, and moving to higher voltage levels is desirable for shipboard PDNs in both commercial and military applications. This would further result in more efficient and cost effective vessel operation and would facilitate an increase in overall system installed power [1]–[4]. Additionally, compared to current MVAC PDNs, also MVDC systems allow for increased flexibility in the design of the entire shipboard electrical power system [5], [6].

Similarly to LVDC shipboard PDNs, MVDC systems are safety critical, and therefore employ redundancy to avoid failure of the whole PDN in the event of a fault [7], [8]. This can be done by clustering power supplies and loads into switchboards forming sectors of the PDN, as seen in Fig. 1. The interconnection between these sectors is performed by solid state bus tie switches (SSBTSs) that allow reconfiguration of the power system according to the vessel's operating mode. Additionally, these prevent a fault in one of the sectors from propagating to adjacent ones by quickly opening and isolating the fault, therefore operating as the first line of defence of the system and providing protection selectivity [8]–[10]. Due to the very fast dynamics of faults in DC distribution systems when compared to their AC counterparts, SSBTSs must be able to:

- Provide ultrafast current interruption in the range of tens of μs, quickly isolating the faulty part of the system from the healthy one.
- Have acceptable conduction losses in operation, as the power generation can be located on either side of the SSBTS.
- Allow for four-quadrant operation.
- Include fault detection logic to autonomously detect and interrupt fault currents, avoiding the need for communication towards the upper control layers, which would inherently introduce delays.

Shipboard PDNs operating at the LV level benefit from a substantial standardisation of technology around the offering of large industrial players like Siemens and ABB. These systems, operating at $1\,\mathrm{kV}$, exploit the availability of equipment such as low voltage generators, rectifiers, breakers, etc. On the other hand, there currently exists no standardised voltage for MVDC systems. The voltage of such systems can range from $3\,\mathrm{kV}$ to $12\,\mathrm{kV}$ [11] or even go as high as 25kV, as suggested in recommendations [12]. This depends on the application and employed equipment, making the development of a standardized SSBTS solution for bus interfacing challenging. For this reason, custom solutions need to be found for each individual system, leading to increased cost and production times. The lack of MVDC standardised voltage levels and suitable equipment is a "*chasing one's tail*" problem, as it is complicated to determine which of the two should be the first step. In this context of lack of standardisation, a scalable SSBTS device able to be adapted to diverse system voltages and power levels can provide an effective solution. This scalability would offer the advantage of using a single device to:

- Accommodate different and increasing voltage levels of

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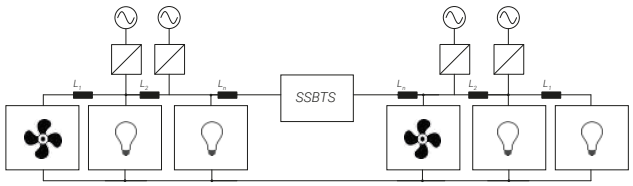

Fig. 1: Shipboard PDNs cluster power sources and loads into clusters interfaces by SSBTSs to prevent faults from one sector of the PDN to propagate into healthy sectors, and to reconfigure the system according to the ship operating mode. Depending on the voltage and current level of the system, the actual SSBTS is realized through series or parallel connection of basic units to achieve the required current and voltage requirements, respectively.

PDNs.

- Accommodate different current levels, associated with different power levels of PDNs.
- Depending on the device failure mode, provide some degree of redundancy.

A device with such series and parallel connection abilities allows for the system voltage and power level to be scaled up without loss of efficiency when compared to the use of a single unit. These properties allow the device to provide an effective and flexible solution to bridge the current technological gap, that can significantly reduce the degree of customisation required in individual installations. In time, optimal solutions can be found as standard operating system voltages are determined. Based on these considerations, this paper presents a scalable SSBTS topology and its operating principle, highlighting the measures taken to achieve scalability, both in terms of voltage and current. Two identical prototypes based on the described topology are assembled and thoroughly tested in different configurations, and a complete set of results is provided for each case.

Section II provides a description of the employed SSBTS topology and principles of its operation, highlighting the characteristics that make the design scalable. Section III describes the assembled prototype of the device and presents an overview of its performance when employed as a single unit with an integrated (external) controller. Section IV provides the result of parallel thermal testing and switching, in order to, respectively, demonstrate that the prototypes are able to correctly share the conducted current and interrupt in the event of a fault thanks to a controller included in the SSBTS. Finally, section V provides similar results in series connected configuration.

II. SSBTS Topology

The proposed and developed SSBTS topology is shown in Fig. 2. The topology is based on a well known four quadrant switch, that is converted into a SSBTS by the addition of a snubber parallel to the active switch, a MOV across the device terminals, and a current rate limiting inductor L_{didt} with a freewheeling diode in antiparallel. Each of these additional devices performs a specific task during the interruption of the

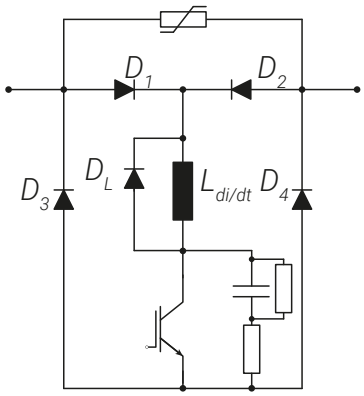

Fig. 2: Single unit of the SSBTS topology. Please note that basic unit is designed to be inserted only between the positive terminals of two different DC buses, allowing for simple parallel or series connection of multiple units.

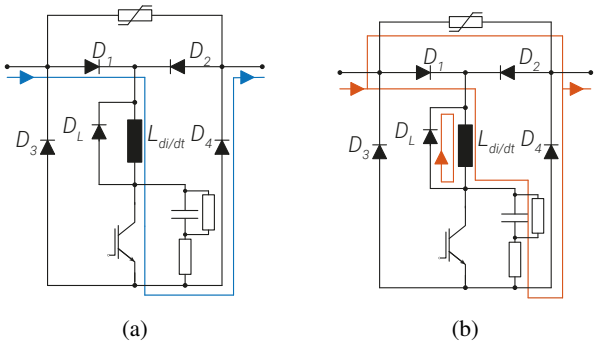

Fig. 3: (a) With the SSBTS *ON*, the current is conducted through D_1, the active switch, L_{didt}, D_4. With an inverted current direction, the active diodes are D_2 and D_3, and the current flow through L_{didt} and the IGBT remains the same; (b) During current breaking, the IGBT goes off and the current takes the path of the metal oxide varistor (MOV), RC snubber and D_L freewheeling diode.

SSBTS current. The RC snubber limits switching overvoltage on the device's active switch by offering an alternative current path to the current in the stray inductance internal to the SSBTS. The MOV clamps the voltage on the device terminals to a known value, and dissipates the stored energy in the DC bus by conducting the bus current with a predetermined voltage at its terminals. As the inductance of the lines may vary for different PDNs designs, multiple MOVs in parallel or with different ratings may be needed in real applications, once the actual system design is known. In this paper, paralleling of MOVs is selected for the presented design. The current rate limiting inductor L_{didt} limits the rate of increase of current in the device and therefore, in the event of a fault, increases the reaction time for the control to switch the device *OFF*. The sizing of such an inductor represents compromise between the time allowed for the control to react to the fault, and the physical dimensions of the device. Additionally, an excessively large inductor will affect the system dynamics by limiting the

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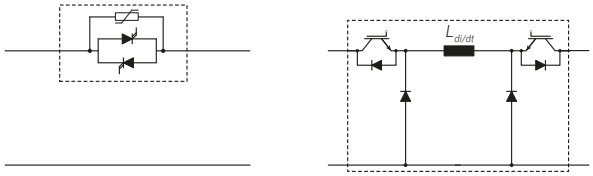


(a) (b)

Fig. 4: (a) Interrupting SSBTS topology [14]; (b) Limiting SSBTS topology [8].

rate of load increase that can be provided by the DC bus. On the other hand, a value of the current rate limiting inductor that is too low would imply reliance on the external stray inductance, which may not be a feasible solution, especially in the case of faults very close to the SSBTS terminals. Consequently, an properly sized, integrated di/dt inductor is deemed to be a safe and effective solution. Finally, the antiparallel diode D_L to L_{didt} provides a freewheeling path to the inductor current once S is turned *OFF*. This prevents the SSBTS from having to dissipate the stored energy in L_{didt} at the time of switching, and allows it to be dissipated in D_L over a longer interval of time. This reduces switching stress on the device and makes switching overvoltage more manageable. Most existing SSBTS topologies can be broadly categorized into two main groups:

- Interrupting topologies, that interrupt the current in both sides of the DC bus upon opening [13]–[17] (Fig. 4a).
- Limiting topologies, that include a current rate limiting inductor and allow freewheeling of the current in one of the two sides of the DC bus [8], [18] (Fig. 4b).

The topology presented in this paper takes the main benefits of both these categories, providing current limiting ability through a current rate limiting inductor, but also interrupting the current on both sides of the DC bus upon opening. The advantages of this topology that make it particularly suitable for series and parallel connected operation are:

- The MOV that provides voltage clamping is placed across the device terminals, rather than across the active switch S. This guarantees that several SSBTS units can be series connected and correctly share the DC bus voltage at the moment of breaking and once the devices are off.
- The freewheeling of the current rate limiting inductor L_{didt} does not requires access to the negative DC bus bar, as it is performed thanks to antiparallel diode D_L. Therefore, when series connecting several units to increase the blocking voltage, each current rate limiting inductor in each SSBTS unit can still freewheel, as its freewheeling path is not blocked by the next series connected unit. This is possible because the current in L_{didt} is unidirectional, thanks to the rectifying action of diodes 1 to 4.
- When series or parallel connected, the current rise rate in the event of a fault is the same in each unit. This is due to the current rise rate being determined by the ratio of the applied voltage to the terminals of the device, and the inductance value of L_{didt}.

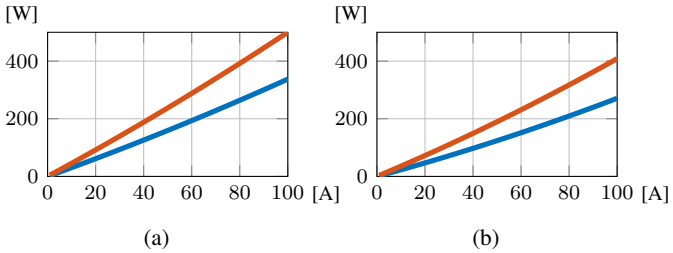
On the other hand, due to the nature of the topology, based on a rectifier structure and an active switching device, there are three semiconductors in the current path when the device is on. This is shown in Figs. 3a and 3b. Fig. 5 shows that this will result in slightly higher conduction losses when compared to other existing or proposed SSBTS topologies like [8], [13], [16], [17]. Nevertheless, the SSBTS is a device the role of which is to provide a first line of defence against faults in the PDN in which it is installed. As the fundamental task of the device is that of providing high reliability and simple operation to dependably separate interconnected buses, the advantages from the point of view of simplicity of connection, scalability and reduced number of active semiconductors make this topology a natural choice for a flexible bus-tie switch solution, in spite of increased conduction losses. Additionally, the scalability of the device means that through parallel and series connection of multiple units, the voltage and power ratings of the SSBTS can be increased while maintaining an unaltered efficiency, as the conducted current of each unit is the same as if it were operated alone.

III. SSBTS Prototype

The need to validate the concept proposed in this paper resulted in the assembly of two SSBTS prototype units, with the goal of verifying their performance in both parallel and series connected configurations. The prototypes, though not thoroughly optimized, serve their purpose of proof-of concept. The presented prototypes are conceived as a scaled down version of an SSBTS intended for operation in a shipboard PDN operating at $1\,\mathrm{kV}$ with a nominal current of $8\,\mathrm{kA}$ and a maximum interruption current of $16\,\mathrm{kA}$. Due to cost reasons, it is chosen to scale down the ratings of the prototypes while maintaining the proportion between nominal and maximum interruption current. Therefore, the final ratings used for the design of the prototypes are:

- A PDN voltage of $500\,\mathrm{V}$.
- A nominal current I_{nom} of $100\,\mathrm{A}$.
- A maximum breaking current I_{max} of $200\,\mathrm{A}$.
- An interruption time of $10\,\mu\mathrm{s}$.

Where the interruption time would normally be selected as a part of system design. Here, it is set to $10\,\mu\mathrm{s}$ to provide ultrafast interruption of the DC current. With the selected



(a) (b)

Fig. 5: In blue, conduction losses in a two-device SSBTS topology as in [8] and in red conduction losses of the presented topology at a semiconductor junction temperature of (a) $25\,^{\circ}\mathrm{C}$ and (b) $125\,^{\circ}\mathrm{C}$.

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ratings, each unit is able to conduct a current of 100 A for an unlimited amount of time. If a fault occurs while the device is conducting, the current will begin to increase as the control needs time to detect the fault and intervene. To account for the control reaction time, the prototype is designed so that it can interrupt a maximum current of 200 A. Since the SSBTS is not a breaker, its current rating needs to be sufficient to interrupt current levels before what is considered to be a dangerous or destructive level. This may vary between different marine PDN designs. The interval of time available for the control to react is determined by both the difference between nominal current $I_{nom} = 100\,\text{A}$ and maximum breaking current $I_{max} = 200\,\text{A}$, and the current rate limiting inductance L_{didt} in the device, according to:

$$t_{reaction} = \frac{I_{max} - I_{nom}}{V_{DC}} L_{didt} \tag{1}$$

Expression 1 gives a general design rule to size the current rate limiting inductor L_{didt} based on the desired $t_{reaction}$, which is determined by the system designer. The value of L_{didt} can be determined as a consequence, as shown in 2:

$$L_{didt} = \frac{V_{DC}}{I_{max} - I_{nom}} t_{reaction} = \frac{500\,\text{V}}{100\,\text{A}} \times 10\,\mu\text{s} = 50\,\mu\text{H} \tag{2}$$

The final selected value of L_{didt} is of 48 µH, due to component availability. It is chosen to use an air core inductor to avoid saturation issues. With the selected inductor, the control has $\approx 10\,\mu\text{s}$ from the time when the fault takes place to open the active switch S of the device. This is considering a worst-case scenario, where the SSBTS prototype is already conducting its nominal current of 100 A. Nevertheless, it is expected that in real applications, times up to 50 µs would be allowed, which can be easily adjusted by the selection of a larger inductor for the SSBTS.

The RC snubber in parallel with S employs a 1 µF capacitor and 1.8 Ω resistor. This is largely sufficient to store the energy contained in the SSBTS internal stray inductance at the moment of breaking. Considering a maximum breaking

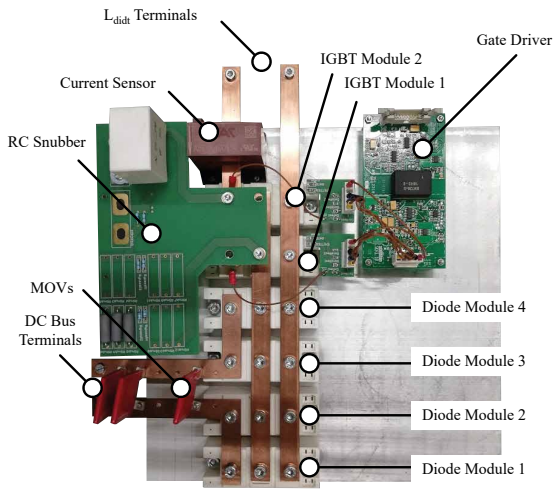

Fig. 6: Assembled SSBTS without external current rate limiting inductor.

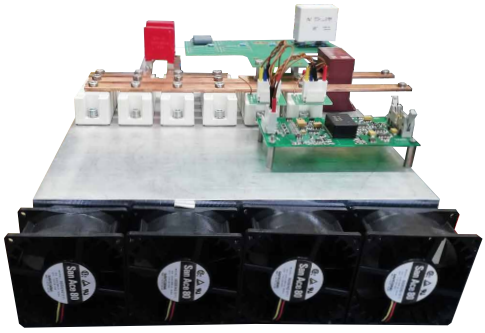

Fig. 7: Location of cooling fans on the SSBTS device during conduction thermal testing.

current of 200 A, a 100 % voltage increase over the DC link voltage of 500 V is sufficient to store the energy contained in

$$L_{stray,max} = \frac{C_{snub} \times 500\,\text{V}^2}{I_{max}^2} \approx 6\,\mu\text{H}, \tag{3}$$

which, considering the size of the device, is larger than the real stray inductance present in the device during testing.

The employed MOVs are *LITTELFUSE V421HG34* with a clamping voltage of 1100 V at 200 A. Three of these MOVs are paralleled at the terminals of each SSBTS unit. The paralleling allows for the dissipation of an increased amount of stored energy in the DC bus inductance, and permits repeated current interruption by the device. Finally, the semiconductor devices are *SEMIKRON SKKD150F12* for the diode modules, and *SKM150GAL12V* for the IGBT modules, all with blocking voltages of 1200 V. All semiconductor positions present in the SSBTS are paralleled to further provide insight, on the basic unit level, on the current scalability to higher current ratings (e.g. several kA), where single module solutions are not feasible, since currents ratings are insufficient.

Before paralleling or series connecting, the SSBTS units are individually stressed in conduction and breaking tests, to verify their correct operation. Fig. 8 provides results for thermal conduction. To evaluate the thermal performance of the device, thermocouples are inserted in channels milled in the SSBTS heatsink to access the semiconductor modules' base plate. The temperature is then sensed as a constant current of 100 A is circulated through the device. Cooling fans were initially *ON*, providing an estimated total air flow of 5.2 $\frac{\text{m}^3}{\text{min}}$

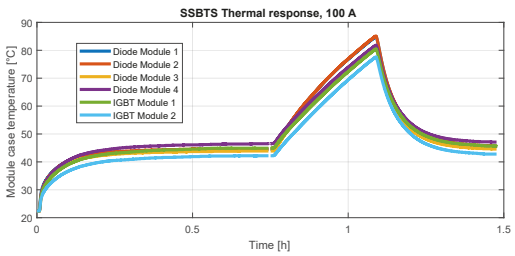

Fig. 8: During thermal testing in conduction of $I_{nom} = 100\,\text{A}$, the device demonstrated good temperature sharing between all modules.

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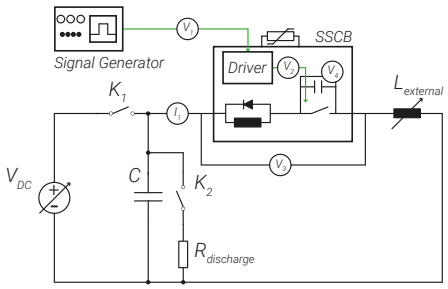

Fig. 9: To test the device in switching, a setup is used in which the SSBTS closes initiating resonance between loaded capacitor $C = 230\,\mu\text{F}$ and $L_{didt} = 48\,\mu\text{H}$ and an external inductance $L_{external} = 5\,\mu\text{H}$. The measurement points are highlighted and the threshold for the control to switch the SSBTS *OFF* is set to $100\,\text{A}$. The DC voltage is $500\,\text{V}$.

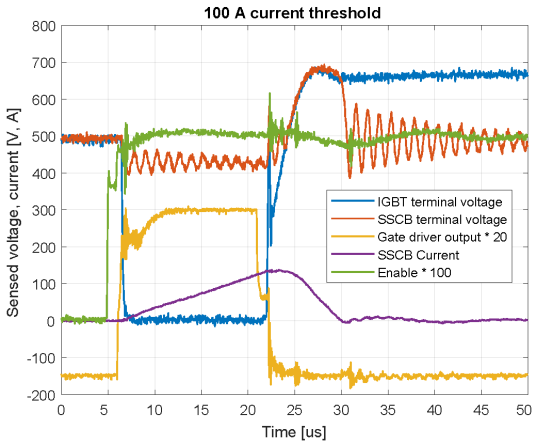

Fig. 10: A single SSBTS unit interrupts the resonant current when the tripping threshold is set at $100\,\text{A}$.

and are then switched off to allow the case temperature of the diode modules to increase to the maximum allowed value of $85\,^\circ\text{C}$. Diode modules represent the thermal threshold of the system, as their junction temperature is estimated to be higher than that of IGBT modules at the measured case temperature and dissipated power. This is due to their higher junction to case thermal resistance. For diode modules, a case temperature of $85\,^\circ\text{C}$ corresponds at $100\,\text{A}$ to a junction temperature of $\approx 105\,^\circ\text{C}$, which is deemed to be sufficient. Once this point is reached, the cooling fans are then again switched on to return the device to the initial operating temperature.

Fig. 9 illustrates the setup employed for switching tests of the single SSBTS units. In this setup, the closing of the SSBTS starts the resonance of capacitor C with inductances L_{didt} and $L_{external}$. Because of the sizing of the component and the short considered time interval, the rise of the current in the device is almost linear. In Fig. 10 an example of interruption of the resonant current is shown where the threshold for SSBTS tripping is set at $I = I_{nom} = 100\,\text{A}$ (considering that the current starts from zero initially, this choice is considered sufficient for the test). In the figure one can see the *enable* pulse that turns on the device, and the corresponding gate driver output. Once the IGBTs have been turned *ON*, the almost linear current rise takes place. The voltage on the device terminals is also visible, together with the IGBT terminal voltage. The latter goes to 0 as the device turns on, while the former is determined by the impedance voltage divider given by $V_{DC}\frac{L_{didt}}{L_{didt}+L_{external}}$. Once the current reaches the threshold of $100\,\text{A}$ the turn *OFF* process begins, and after a delay determined by the control and actuator response, the IGBTs interrupt the current. The current interruption corresponds to a voltage spike on the IGBT terminals due to the commutation of current from the IGBTs themselves to the parallel RC snubber, that begins loading and stops once the current is interrupted. The delay in control and actuation response results in the maximum current in the device being higher than the $100\,\text{A}$ threshold, and is accounted for in the design.

The detection of the fault is performed by the SSBTS controller, a *PLEXIM RT-Box*. The controller accesses the SSBTS onboard measurement of current in the L_{didt} inductor and voltage at L_{didt} terminals with a sampling rate of $1\,\text{MHz}$, and can use three different criteria to determine the presence of a fault. These are based on current magnitude, current rate of increase, and voltage at the current rate limiting inductor terminals. Of these, the latter two in essence measure the same thing: the current rise rate in L_{didt} and the voltage at its terminals are linked by the inductor state equation $\frac{di}{dt} = \frac{V}{L}$. In the event of a fault, a part of the DC bus voltage will be applied to L_{didt}, according to its value relative to that of the DC bus stray inductance and fault impedance. In this context, the presence of a fault can be identified by measuring the value of the voltage at the terminals of L_{didt}, or by computing the current rise rate. This allows, in principle, for a faster response of the controller, as it is not necessary to wait for the current magnitude to increase up to its threshold value. Nevertheless, accurate computation of the current increase rate at a high sampling frequency such at the employed $1\,\text{MHz}$ also presents some challenges. In particular, the computation of the current rise rate as $\frac{di}{dt} = \frac{i_k - i_{k-1}}{1\,\mu\text{s}}$ is particularly sensitive to measurement noise. To prevent unwanted tripping of the device caused by this noise, it was chosen to increase the threshold value for the di/dt threshold to $6.66\,\frac{\text{A}}{\mu\text{s}}$, that is to say $\frac{2}{3}$ of the maximum current rise rate allowed by L_{didt}. This insures that the threshold is only crossed in the event of a particularly high current increase rate, that can only be associated with a fault and not caused by noise, load variations, or capacitive load turn-on. Depending on the employed techniques, the three criteria for the identification of the presence of a fault display different reaction times. This is not only due to the sensed or computed quantity, but also to the different response and rise time of the current and voltage sensor used. As the current rise rate is maintained constant at the value determined by the DC voltage and L_{didt} and $L_{external}$ of:

$$\frac{dI}{dt} = \frac{1}{2} \times \frac{500\,\text{V}}{\frac{48\,\mu\text{H}}{2} + 5\,\mu\text{H}} \approx 8.5\,\frac{\text{A}}{\mu\text{s}}, \tag{4}$$

this results in a different SSBTS current value with different SSBTS switching criteria.

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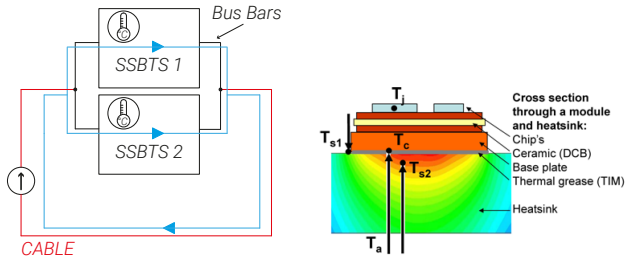

(a) (b)

Fig. 11: (a) The current sharing of parallel SSBTSs is evaluated by circulating I_{nom} through each device and sensing semiconductor module temperature; (b) The temperature of each module is sensed by placing thermocouples in a channel milled in the heatsink allowing access to the device base plate [19].

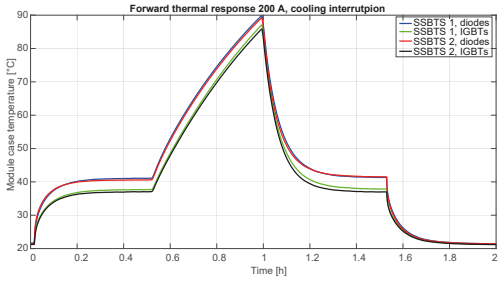

Fig. 12: The thermal conduction test of parallel units shows how the average temperatures of equivalent semiconductor modules in the two paralleled SSBTS units is very well matched.

IV. SSBTS Parallel Operation

While Fig. 8 shows measured temperatures on a single unit, thermal testing of parallel SSBTS units has the goal of determining if the total conducted current is shared properly between the devices operated in parallel. The setup employed in this test is represented in Fig. 11a and is constituted by a low voltage DC source operated in current limiting mode, and circulating the nominal current $I_{nom} = 100\,\text{A}$ through each device. The paralleling of the devices is performed with $15\,\text{mm} \times 3\,\text{mm}$ copper bus bars, the same which are used in the devices themselves. The terminals of the parallel are then directly connected to the DC current source. For this test, the result of which is displayed in Fig. 12, no L_{didt} current rate limiting inductor is employed in the SSBTS. This is because different systems will require different values of inductance, therefore one should not rely on the parasitic resistance of L_{didt} to aid in the current sharing, as this is application dependant.

If the power rating of the marine PDN exceeds the current capacity of a single SSBTS unit, this section also demonstrates that the presented topology provides a simple solution through parallel connection of more than one unit. The switching tests of SSBTSs in parallel operation are performed with the setup

TABLE I: SSBTS unit current and parallel forward voltage during parallel thermal test.

Time	SSBTS 1 Current [A]	SSBTS 2 Current [A]	Forward Voltage [V]
10’	96.6	97.3	3.79
30’	96.7	97.2	3.78
50’	97.1	96.7	4.09
70’	96.6	97.1	3.76
90’	96.5	97.2	3.77

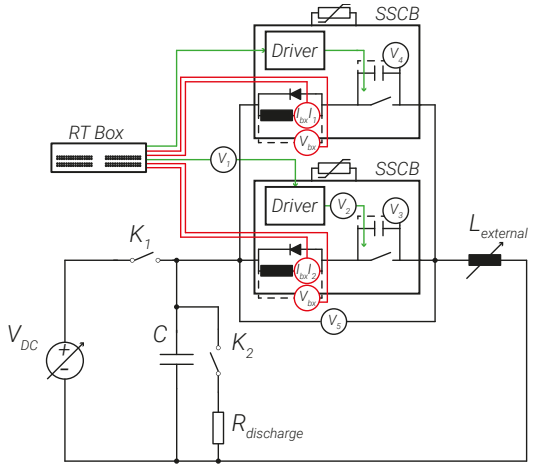

Fig. 13: Test setup for switching of parallel connected SSBTSs. The test parameters are: $V_{DC} = 500\,\text{V}$, $C = 230\,\mu\text{F}$, $R_{discharge} = 480\,\Omega$, $L_{didt} = 48\,\mu\text{H}$ and $L_{external} = 5\,\mu\text{H}$.

in Fig. 13. Similarly to what is shown in Fig. 9 the setup is such that upon the parallel SSBTSs closing, a resonant circuit is formed between C and L_{didt} and $L_{external}$. This causes an almost linear current rise in the current interval of interest for the test, which is between $0\,\text{A}$ and $400\,\text{A}$, as this is the maximum current that can be interrupted by the parallel connection of two units. This linear current rise reasonably represents what is seen in a short circuit fault in a shipboard PDN such as in Fig. 1.

The paralleled switching operation is tested based on the three criteria described in section III. In the first case, in Fig. 14, a current threshold is programmed in the controller. The threshold is selected based on the fact that the nominal thermal current I_{nom} is of $100\,\text{A}$ in each device, or $200\,\text{A}$ for their parallel connection. Therefore, if the current exceeds $100\,\text{A}$ in either of the two devices, the controller will turn *OFF* both devices. In Fig. 14 one can see that the first device to reach the threshold is device 2. This is because, in spite of the two devices showing the same current increase rate, device 2 is turned *ON* approximately $1.5\,\mu\text{s}$ earlier that device 1. This is attributed to an asymmetry in the gate driver power supply. In the second test, in Fig. 15 the voltage on L_{didt} terminals is compared to a programmed threshold value of $300\,\text{V}$. Finally, in the last test, in Fig. 16, the current increase rate is compared to a programmed threshold value of $6.66\,\frac{\text{A}}{\mu\text{s}}$, which is chosen as $\approx \frac{2}{3}$ of the maximum current increase rate at $500\,\text{V}$ limited by $L_{didt} = 48\,\mu\text{H}$. In all three cases, the parallel SSBTSs are

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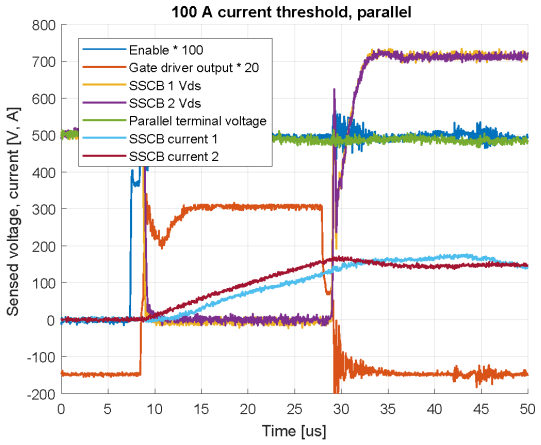

Fig. 14: Parallel connected SSBTS switching results with switching threshold set at 100 A. This threshold results in the longest current rise time, as the current must cross the threshold of 100 A before the turn *OFF* is initiated.

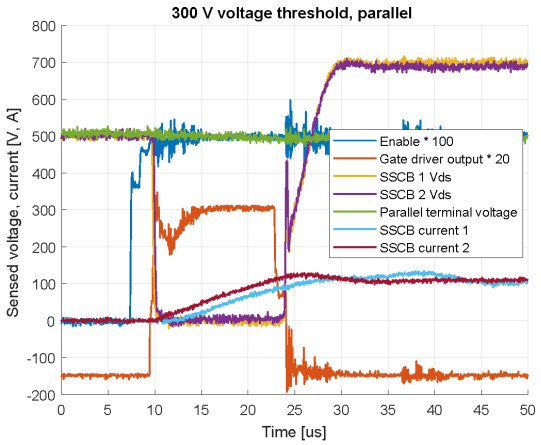

Fig. 15: Parallel connected SSBTS switching results with switching threshold set at 300 V applied to L_{didt}. The method provides a shorter current rise time than what is shown in Fig. 14. This is because in spite of the voltage sensor having longer response and rise time than the current sensor, the voltage on the terminals of L_{didt} is free to immediately rise to its final value at the moment when the SSBTS is turned *ON*.

both turned *OFF* if the threshold value in either of them is reached.

Independently of the employed switching criterion it is observed that the current is correctly shared between the two devices during the transient. This complements what was shown in Fig. 12, where the current sharing was evaluated in steady state, and depends mainly on the equal value of the two L_{didt} inductors used in the two units, both equal to 48 µH. An imbalance in the sizing of the inductors would result in a different rate of increase of the current in the devices, and therefore result in a different breaking current. While this is undesirable, it is tolerable as long as neither device exceeds its rated I_{max}. With the parallel connection of the two units

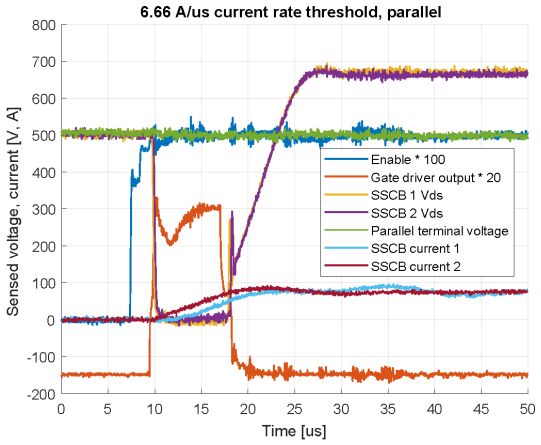

Fig. 16: Parallel connected SSBTS switching results with switching threshold set at 6.66 $\frac{\text{A}}{\text{µs}}$ current rise rate in L_{didt}. This results in the fastest interruption time, as it offers a combination of the faster response of the current sensor, together with the immediate response provided by the rapid increase in $\frac{dI}{dt}$ at the moment the SSBTSs are closed.

presented in this paper, all three criteria for the identification of the fault result in the peak current being kept below the maximum level of 200 A for both units.

By comparing Fig. 10 and 14, in which the performed interruption is based on the same fault identification criterion of 100 A current threshold, one can see that the solicitations undergone in the paralleling of the SSBTSs are almost the same as those of a single device performing the breaking of half the current. These results can be used to confirm that it is possible to conduct and interrupt double the current using a parallel connection of two devices than it is possible to do

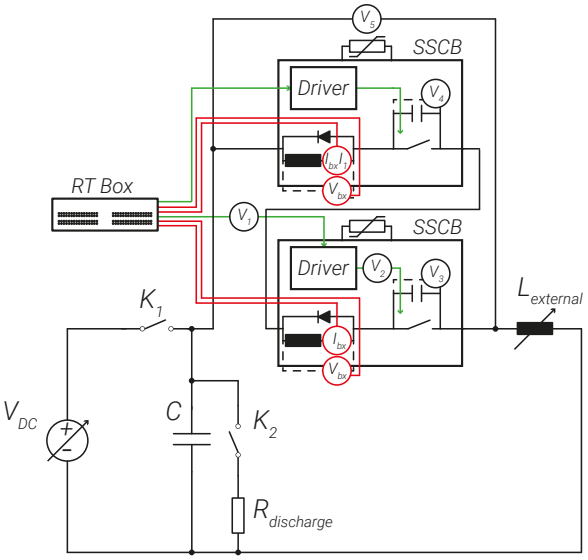

Fig. 17: Test setup for series connected SSBTS switching. All parameters of the circuit remain the same as in Fig. 13, except for the DC voltage that is increased to 1 kV.

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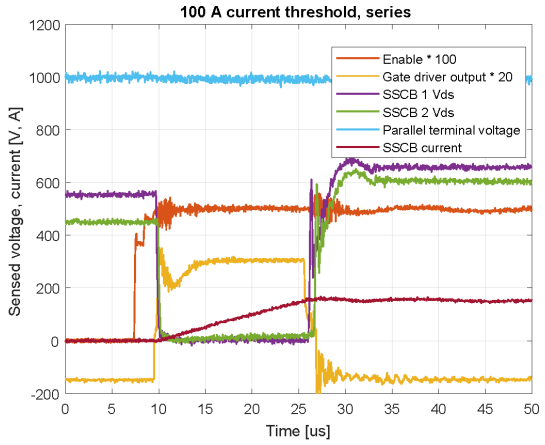

Fig. 18: Series connected SSBTS switching results with switching threshold set at 100 A. Similarly to the parallel connected case, this threshold results in the highest final current level reached by the SSBTSs. The higher breaking current makes the disparity in voltage between unit 1 and 2 more evident compared to the following switching results.

with a single SSBTS unit, and that the paralleling of the units operates as expected.

V. SSBTS Series Operation

As the current trend in shipboard PDNs is towards an increase in nominal voltage to allow for increased system power ratings and efficiency, this section shows that the presented SSBTS topology provides a flexible solution easily adaptable to different power levels. Similarly to what was done in section IV, the section provides results for series connected SSBTSs units switching at a voltage of 1 kV. The same three

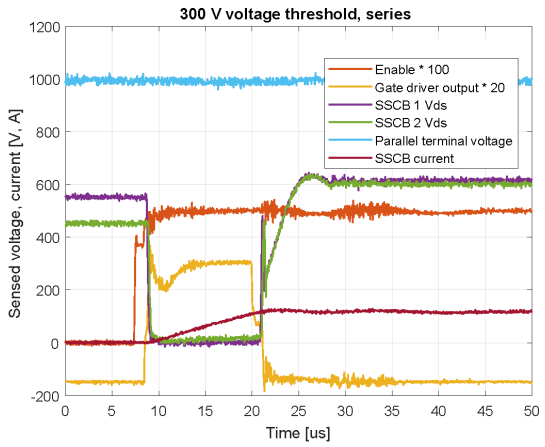

Fig. 19: Series connected SSBTS switching results with switching threshold set at 300 V. A shorter current rise time results in a lower interrupted current compared to Fig. 18. The lower voltage level reached by the SSBTSs snubbers makes the voltage discrepancy less evident, but as the snubber capacitors discharge, the voltages on the two units will settle to the same values as before the devices were closed.

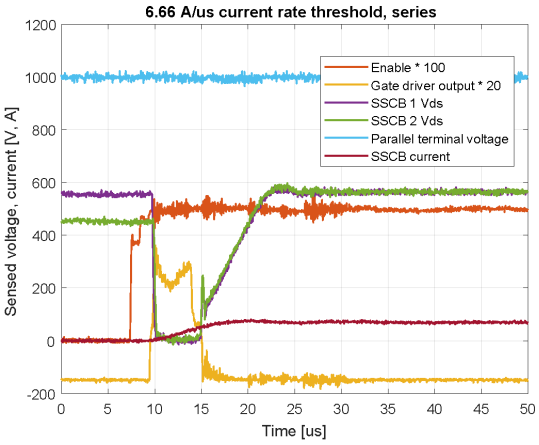

Fig. 20: Series connected SSBTS switching results with switching threshold set at 6.66 $\frac{\text{A}}{\mu\text{s}}$. As for parallel connected units, fault identification based on current increase rate results in the fastest current interruption and lowest final SSBTS current.

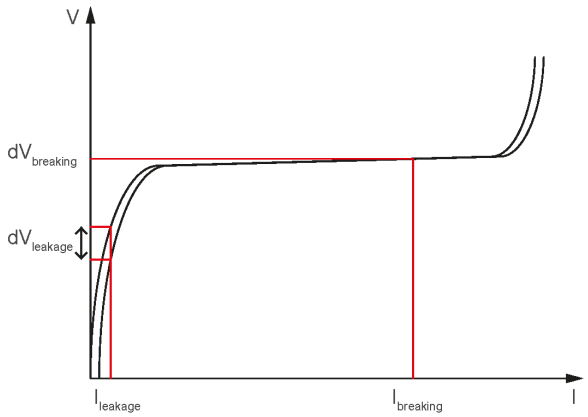

Fig. 21: An idealized MOV schematic shows how a small shift of the characteristic can cause the same leakage current to result in significantly different voltages on two different varistors.

switching criteria are used: should either of the devices exceed the set threshold, both series connected SSBTSs will switch off. This is shown in Figs. from 18 to 20.

The tests provide similar results to what was shown in parallel tests of the devices. The interruption performed based on the current threshold of 100 A is still the one that results in the highest final value of current in the devices. Interruption based on the voltage on the terminals of L_{didt} results in faster switching *OFF*, and finally the di/dt threshold results in the faster interruption. It can be seen in all the figures that a difference in initial voltage is present between the two series connected devices. Also, in Fig. 18 in particular, where the current in the devices is the highest, one can see that the voltage tends again to settle to the initial values as the snubber capacitor discharges. When the devices are *OFF*, the voltage sharing is mainly determined by the MOVs in parallel to the

device terminals. Due to the steepness of the MOV characteristic for low current values, a small discrepancy between the MOV connected in parallel with unit 1 and that connected in parallel with unit 2 may result in a noticeable difference in the voltage partition between the two. A simplified representation of this is provided in Fig. 21. Here one can see how a small shift in the characteristic has very little influence on the performance of the device under breaking, it has a lot more on the leakage current. As the devices are series connected, the same leakage current flows through both SSBTS MOVs, where it can result in different voltages based on the MOV's individual characteristic. Nevertheless, this does not constitute an issue, as a further increase in the leakage current of the MOVs would result in a much more significant increase in voltage of MOV 2 than it would for MOV 1. This can again be seen from Fig. 21. Overall the series connected SSBTSs are able to interrupt their rated current at a voltage level double that of a single unit, while sharing voltage adequately.

VI. Conclusion

This paper presented results on series and parallel connected operation of an SSBTS topology for DC PDNs. The topology, initially designed for LV systems, is ideally suited for scalable operation due to its self contained freewheeling circuit, clamped terminal voltage and two-terminal connection to the DC bus. Results for conduction and switching of a single SSBTS unit are included so as to provide a baseline against which to evaluate scaled performance with the use of multiple units. The comparison between single unit test results and series and parallel connected units demonstrate that electrical and thermal stresses on the devices are not increased in these configurations. These results prove that the SSBTS ratings can be linearly scaled with the number of series/parallel connected units, providing a simple and effective solution to tackle different system voltage levels with a single device.

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