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Solid State Bus Tie Switch for Shipboard Power Distribution Networks

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***Abstract*—Recent trends in shipboard power distribution network design, such as the transition from AC to DC result in new challenges on the issue of distribution network protection. Devices such as a solid state bus tie switch provide a first line of defence against propagation of low impedance faults across the distribution system by quickly separating the faulty portion of the network and preventing additional energy to be fed into the fault. This paper proposes a new topology of solid state bus-tie switch for shipboard power distribution networks. The topology is thoroughly described considering its operating principles, and a small scale prototype has been used to verify its operational performances. Current interruption capabilities are demonstrated, both in open loop and closed loop operation, with fault detection and decision algorithms implemented on a standalone controller.**

I. Introduction

The marine transport sector is under pressure to increase vessel energy efficiency for reasons both economical and environmental [1], [2]. DC distribution in such systems is increasingly employed as it allows for increased efficiency compared to its AC counterparts, while the system flexibility and potential for integration of energy storage systems is increased [3]–[7].

The protection of a shipboard DC power distribution network (PDN) presents additional challenges compared to an AC PDN. This is due to the fast fault dynamics determined by the large amount of DC link capacitors in the system, together with a low bus bar inductance and absence of current zero crossings. The low surge current ability of semiconductors, which play a central role in such DC PDNs, further increases the need for fast fault current interruption. Shipboard PDNs are safety critical installations and redundancy is employed to ensure a single failure does not take the system offline. The system is then partitioned into sectors grouping different power supply and loads that can be reconfigured based on the operating mode of the ship, as shown in Fig. 1. This results in loads and generators clustered into switchboards interfaced by bus tie switches, that offer an additional opportunity for protection of the system. In this context, the ultra-fast operation of a solid state bus tie switch (SSBTS), allows for the separation of different DC buses in the event of a fault, increasing vessel operation safety and flexibility by preventing fault propagation from the affected area to different sections of the PDN [8], [9]. Even though these devices perform the interruption of DC bus current, they are not intended to operate as main circuit breaker (MCB). A MCB and SSBTS are two fundamentally different devices. The first is a final protection device able to interrupt a fault current several times higher than its nominal current, protecting downstream equipment from damage in the event of a fault. Conversely, an SSBTS provides much faster interruption (in the range of tens of µs), but has lower current interruption ability and operates as part of a protection coordination scheme together with other means of system protection, such as high-speed fuses and generator/rectifier fault control [4], [10], [11]. Fig. 2 provides the reaction times of the elements of such protection coordination schemes, including the SSBTS. In the figure it is clear that in such a system, the SSBTS, with its ultrafast opening time, has the role of first line of defence against a system fault. The safety-critical role that this device plays imposes a number of characteristics that the SSBTS must have to perform its task. These are:

- Interruption time in the range of tens of µs.
- Low conduction losses during operation.
- Four-quadrant operation.
- Standalone operation by means of intelligent fault detection.

To achieve this, an SSBTS can operate based on

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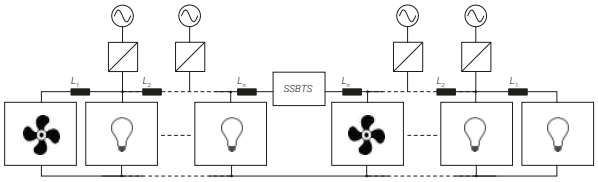

Fig. 1: A DC ship PDN employs redundancy to maintain operation in the event of a fault. Different DC buses are interfaced to allows for reconfiguration of the system depending on ship operating mode. The SSBTS enables system reconfiguration and aids protection coordination.

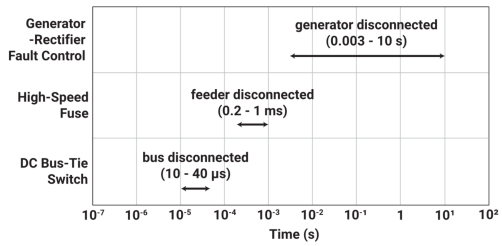

Fig. 2: DC shipboard PDN protection coordination schemes employ multiple means of protection operating in different time scales [4].

different principles. Various proposals can be traced back in literature, relying on different operating principles [12], [13]: i) Interrupting, in which the DC bus current is interrupted upon opening of the device [14]–[17]; ii) Limiting, that allows current freewheeling gradually dissipating inductive energy [11], [18]; iii) Resistive, where current is redirected into a capacitor and energy is discharged in an *ad hoc* resistor [19]; iv) Resonant, in which the interruption is achieved through a capacitive discharge creating an artificial current zero [20]–[22].

Currently, commercial solutions for SSBTSs devices are available in the $1\,\mathrm{kV}$ DC voltage range. ABB offers an IGCT based solution, capitalizing on the low conduction loss of this semiconductor device, while SIEMENS provides an IGBT alternative as part of the *BlueDrive* power solution [11], [23]. This paper presents a novel SSBTS topology taking inspiration from a known four quadrant switch topology extended through several critical elements, to achieve protection functions. A scaled down prototype is developed and thoroughly tested in relevant operating modes, with full set of results presented in the paper.

The main contributions of this paper are: (i) a novel SSBTS topology with a single active semiconductor device; (ii) a comparative analysis of several control methods to identify and interrupt fault currents according to different criteria.

This paper is organized as follows: section II describes the device topology and operating principle. Section III looks at the assembled SSBTS prototype and its rating. Section IV describes the thermal conduction test setup and results, while section V provides current interruption test results. Finally, Section VI provides results of standalone switching tests, where the device autonomously identifies a fault condition and performs current interruption.

II. SSBTS Switch Topology

Shipboard PDNs count several interfaced DC sections. Typical ratings for an individual LV shipboard PDNs section interfaced by SSBTSs devices are in the range of $1\,\mathrm{MW}$ to $5\,\mathrm{MW}$, at a voltage level of $1\,\mathrm{kV}$. This results in their rated current being in the range of a few kA. In the event of a fault, as shown in Fig. 3, the current in the DC bus will increase at a rate determined by the amount of inductance present between the fault location and the capacitance connected to the DC bus, and can reach several times the value of the rated current. Therefore, two values of current are defined for the SSBTS:

1) I_{nom}: The nominal current for which the SSBTS is thermally sized, and that can be conducted indefinitely
2) I_{max}: The maximum value of current that can be interrupted by the SSBTS

While existing semiconductors ratings can be as high as a few kA, the interruption of currents exceeding $10\,\mathrm{kA}$ must rely on paralleling of modules. As the I_{max} current can be several times larger than

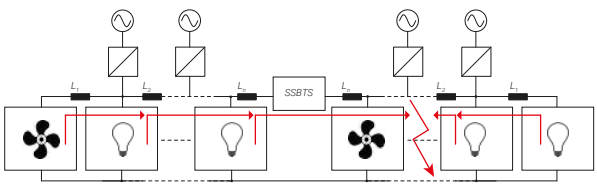

Fig. 3: During faults in the DC bus, the capacitors at the input of connected loads discharge into the fault impedance.

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I_{nom}, one cannot rely on a single semiconductor module to perform the current interruption, as this would be outside the safe operating area (SOA) of the device. Module paralleling is therefore required in these devices, and the same approach is followed during design of the small scale prototype presented in the next section, in order to explore impacts that this may have on the overall performances.

The topology presented in this paper is shown in Fig. 4. It uses the well known four quadrant switch in Fig. 5a as a starting point. To use this topology in the role of an SSBTS, it is modified by adding:

- L_{didt} as a current rate limiting inductor, providing controllable conditions for fault detection and reaction.
- D_L as an antiparallel freewheeling diode for L_{didt}, to allow dissipation of the stored magnetic energy after opening of S.
- RC snubber parallel to S, with the purpose of preventing switching overvoltage on the IGBT.
- A metal oxide varistor (MOV) across the device terminals to limit the voltage across the SSBTS to a known value.

The resulting topology allows for freewheeling of the current rate limiting inductor without access to the negative bus bar, providing increased simplicity of connection. Also, in the event of inversion of the direction of current in the DC bus, as in Fig. 5c, the L_{didt} inductor does not see an inversion in current, and does not need to be discharged and recharged. On the flipside, the topology places three semiconductors in the current path, causing an increase in conduction losses of the device when compared, for example, with that presented in [11]. Yet, this is a small price to pay, considering the simplicity and reliability offered by the use of a single active device.

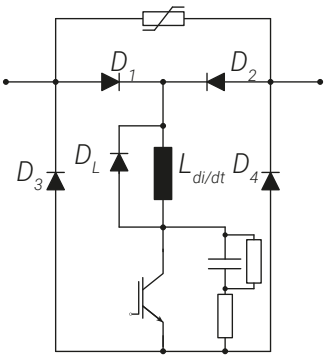

Fig. 4: Proposed SSBTS topology.

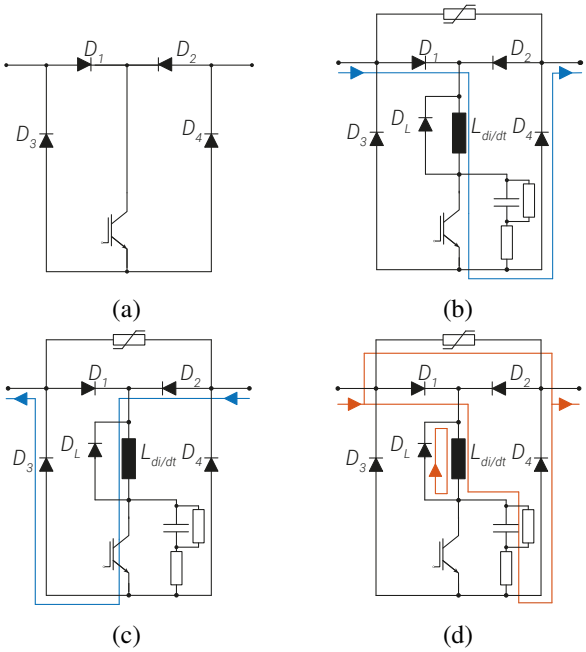

Fig. 5: (a) Original four quadrant switch topology; (b) Current path during conduction from left to right; (c) Current path during conduction from right to left; (d) Current path during breaking.

The operation of the topology during conduction and breaking is shown in Figs. 5 and 6. In Fig. 6 the device is initially *ON* and conducting current. This corresponds to Fig. 5b or 5c, depending on the direction of current. During this time, the value of current in the device is constant, and conducted by the IGBT. The current conducted by the IGBT is the same current conducted by diodes $D_1\&D_4$, or $D_2\&D_3$, depending on the direction of conduction. The voltage drop at the terminals of the device is $0\,\mathrm{V}$ (neglecting semiconductor forward voltage drop).

At time t_0, a fault occurs and the bus voltage at one of the terminals of the device drops to $0\,\mathrm{V}$. As this happens, a voltage drop appears across the terminals of the device. The voltage applied to the SSBTS terminals causes the current in the device to increase, at a rate determined by $\frac{di}{dt} = \frac{v_{SSBTS}}{L_{didt}}$. As the current increases, the device will detect the fault and initiate the interruption of the fault current.

At time t_1, the IGBT turns *OFF* and the interruption of the current begins. The current path in this configuration is that shown in Fig. 5d. The current in the IGBT drops to $0\,\mathrm{A}$ and is shunted to the snubber path. As this happens, the voltage on the

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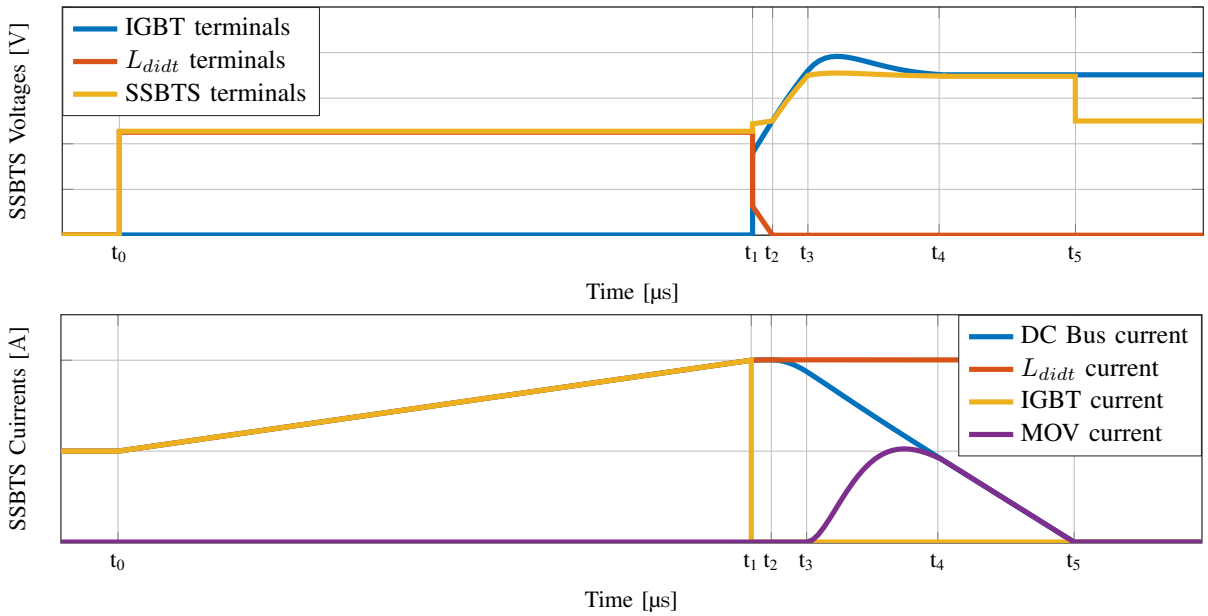

Fig. 6: Voltages and currents in listed SSBTS components during conduction and interruption.

IGBT terminals increase. This reduces the voltage applied at the terminals of L_{didt}, which now is equal to $v_{L,didt} = v_{SSBTS} - v_{IGBT}$. The drop of voltage on the inductor terminals decreases the current increase rate.

At t_2, the snubber capacitor contains enough charge that the total voltage at the IGBT terminals is equal to the voltage at the SSBTS terminals. At this point, the current in the SSBTS ceases to increase, and the freewheeling diode D_L becomes forward biased, maintaining the current in L_{didt} at a virtually constant level.

From t_2 to t_3, the voltage on the snubber, at the terminals of the IGBT, continues to increase until, at t_3, it reaches the clamping voltage of the MOV. At this point, the MOV conducts maintaining the voltage at the terminals of the SSBTS constant.

In the interval between t_3 and t_4, the voltage on the snubber temporarily exceeds that of the device terminals due to the internal stray inductance of the device. Meanwhile, the current in the device continues to drop at a rate which is determined by the the difference between V_{DC}, and the MOV clamping voltage.

At t_4 the MOV has completely taken over the device current. This results in the voltage at the terminals of the device being clamped at the MOV clamping voltage, and the current continues to drop linearly. Meanwhile, the current in L_{didt} continues to freewheel at a virtually unchanged level.

Finally, at t_5, the current is interrupted and the voltage on the device terminals returns to being V_{DC}, as the MOV is no longer conducting any current. The interruption is complete and the current in L_{didt} will gradually decay due to the on-state resistance of D_L.

III. SSBTS Prototype

To verify operational performances of the SSBTS, a small scale prototype is designed and assembled to serve as proof of concept, rather than thoroughly optimized device. This SSBTS prototype has a blocking voltage of $500\,\mathrm{V}$, can conduct up to I_{nom} = $100\,\mathrm{A}$ and has a maximum breaking current I_{max} of $200\,\mathrm{A}$. This gives a ratio of $\frac{I_{max}}{I_{nom}} = 2$ between the maximum interruption current I_{max} and the nominal current I_{nom}. While this would be insufficient for a MCB, it is reasonable for an SSBTS device and results from the scaling down of the respective ratings of the real considered system. The blocking voltage of $500\,\mathrm{V}$ is selected to allow the integration of the device into other laboratory experiments. In terms of semiconductors, two different *SEMIKRON* modules are employed: *SKKD150F12* as diode

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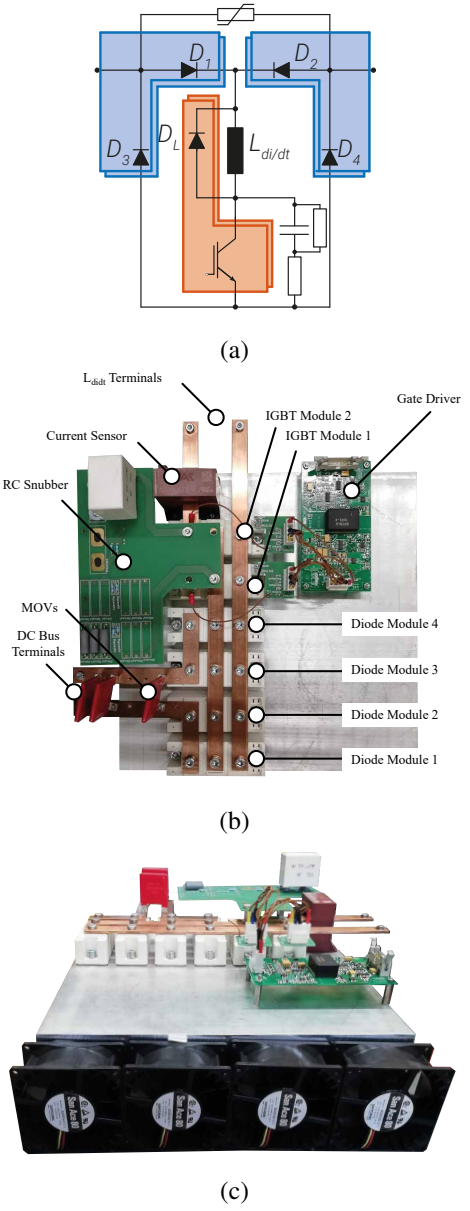

Fig. 7: (a): Diode modules (in blue) and IGBT modules (in red) are paralleled in the SSBTS prototype.; (b): Assembled SSBTS without external current rate limiting inductor; (c): Location of cooling fans on the SSBTS device during conduction thermal testing.

modules, and *SKM150GAL12V* as IGBT modules. These provide a blocking voltage of $1.2\,\mathrm{kV}$ and current conducting ability of $150\,\mathrm{A}$. With the selected modules and a nominal current of $100\,\mathrm{A}$, the expected conduction losses of the device are estimated at different current levels and semiconductor junction temperature. This estimate is based

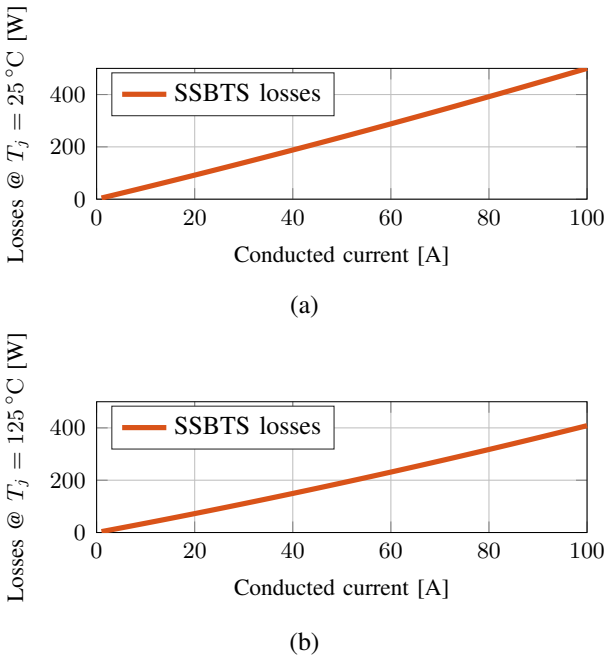

Fig. 8: SSBTS conduction losses as a function of current for different values of junction temperature.

on datasheet parameters and its results are displayed in Fig. 8. It can be seen that the losses at the nominal current of $100\,\mathrm{A}$ are expected to be approximately $400\,\mathrm{W}$ at $T_j = 125\,^\circ\mathrm{C}$. Note that this estimation assumes that the junction temperature of all semiconductor devices is the same. This is shown to be an accurate approximation during testing of the prototype. As the device is only intended to turn *OFF* is the rare event of a fault, switching losses are not relevant to thermal considerations.

Having selected the semiconductor device to be used in the prototype, the SSBTS snubber is sized so as to limit the voltage on the IGBT modules' terminal at the time of switching to a value below that of $1000\,\mathrm{V}$. This leaves a safe margin to the threshold of the device rating of $1200\,\mathrm{V}$. The resistor in the RC snubber is sized so that under the worst case interruption current of $200\,\mathrm{A}$, a voltage of $500\,\mathrm{V}$ is immediately applied to the IGBT terminals, preventing further increase of the current. This is because the voltage on the SSBTS would be equal to the DC bus voltage, which is also 500 V. This results in a snubber resistor of:

$$R_{snubber} = \frac{V_{DC}}{I_{max}} = \frac{500\,\mathrm{V}}{200\,\mathrm{A}} = 2.5\,\Omega \qquad (1)$$

As the voltage at the IGBT terminals should not exceed $1\,\mathrm{kV}$, the snubber capacitor should be sized

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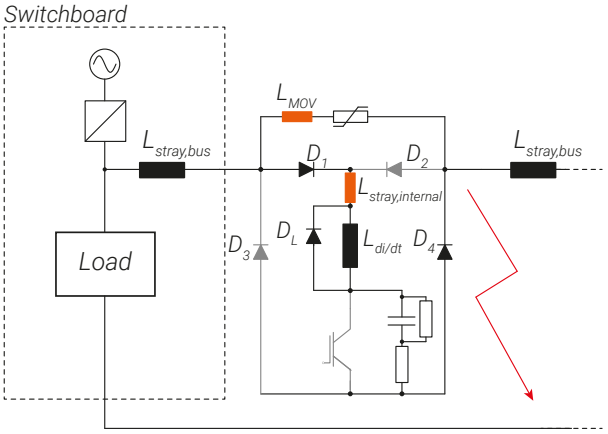

Fig. 9: For the sizing of the snubber, a worst case scenario is considered with a fault at the SSBTS terminals. The stray inductance of the healthy side of the DC bus is modelled with a concentrated value of $5\,\mu\mathrm{H}$, corresponding to approximately $5\,\mathrm{m}$ of length of the DC bus [24].

to store the energy contained in the internal stray inductance of the SSBTS, highlighted in Fig. 9, under the worst case scenario of $I_{max} = 200\,\mathrm{A}$. The MOV should then dissipate the energy stored in the stray inductance of the DC bus ($L_{stray,bus}$ in Fig. 9). This separation of tasks, while valid as a first approximation, does not account for the presence of stray inductance on the MOV current path (L_{MOV} in Fig. 9), that prevent the current in the MOV for increasing rapidly at the time of opening. Because of this inductance, the MOV will only dissipate a part of the energy in the stray inductance of the DC bus, and the rest will be stored in the snubber capacitor upon interruption. It is conservatively estimated that this energy will be shared equally between MOV and snubber capacitor. Estimating a DC bus bar length of $5\,\mathrm{m}$ and an inductance of $1\,\frac{\mu\mathrm{H}}{\mathrm{m}}$ [24], one has that $L_{stray,bus} = 5\,\mu\mathrm{H}$. Neglecting the much smaller internal SSBTS inductance, this results in an energy to be stored in the snubber capacitor of:

$$E_{C,snubber} = \frac{1}{2} L_{stray,bus} I_{max}^2 = \frac{1}{2} * 5\,\mu\mathrm{H} * 200\,\mathrm{A}^2 \approx 100\,\mathrm{mJ} \tag{2}$$

The allowed voltage increase of the capacitor to store this energy is equal to:

$$\Delta V_{C,snubber} = 1000\,\mathrm{V} - V_{DC} = 500\,\mathrm{V} \tag{3}$$

By combining 2 and 3 the snubber capacitor can be sized as:

$$C_{snubber} = \frac{L_{stray,bus} * I_{max}^2}{\Delta V_{C,snubber}^2} = \frac{5\,\mu\mathrm{H} * 200\,\mathrm{A}^2}{500\,\mathrm{V}^2} = 800\,\mathrm{nF} \tag{4}$$

Due to component availability, the final values of the snubber resistor and capacitor are $1.8\,\Omega$ and $1\,\mu\mathrm{F}$, respectively.

The selection of the MOVs is based on the current/voltage characteristic of the device rather than breaking energy dissipation. It is required that the MOVs prevent the terminal voltage of the device from increasing above the switching devices' rated values for a maximum breaking current of $200\,\mathrm{A}$, while not conducting at the rated blocking voltage of $500\,\mathrm{V}$. The selected *Littelfuse V421HG34* provides the required compromise with a clamping voltage of $1100\,\mathrm{V}$ at $200\,\mathrm{A}$, and a conducted current at $500\,\mathrm{V}$ well below $1\,\mathrm{mA}$. The selected MOV can dissipate up to $600\,\mathrm{J}$ per breaking action, which is more than sufficient.

The sizing of the current rate limiting inductor L_{didt} is performed based on I_{max}, I_{nom}, V_{DC} and the required SSBTS reaction time, $t_{reaction}$. The reaction time is a parameter determined by the system designer, and it is the time that it takes the current to rise from the value of I_{nom} to I_{max}, according to:

$$t_{reaction} = \frac{I_{max} - I_{nom}}{V_{DC}} L_{didt} \tag{5}$$

Different system designs might allows for different current rise rates, and L_{didt} can be varied as a consequence, for the device to provide the required performance. In the presented prototype, $t_{reaction}$ was set to $10\,\mu\mathrm{s}$, as this was the required reaction time of the system. From 5 a general design rule can be extracted, providing the sizing of the current rate limiting inductor based on the characteristics of the system. This is:

$$L_{didt} = \frac{V_{DC}}{I_{max} - I_{nom}} t_{reaction} \tag{6}$$

And for the specific system described in this paper:

$$L_{didt} = \frac{500\,\mathrm{V}}{100\,\mathrm{A}} * 10\,\mu\mathrm{s} = 50\,\mu\mathrm{H} \tag{7}$$

The L_{didt} used, due to component availability, is an air core $48\,\mu\mathrm{H}$ inductor.

Finally, it is worth noting that even though semiconductor devices at the rating of the SSBTS are

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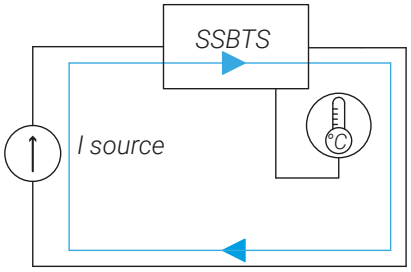
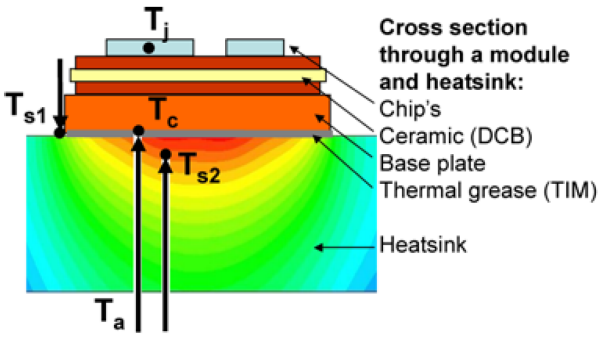


(a)



(b)

Fig. 10: (a): The thermal response of the SSBTS is evaluated by circulating I_{nom} through the device and sensing module temperature; (b): The temperature of semiconductor module case is measured by inserting thermocouples into channels milled in the heatsink allowing access to the modules' base plate [25].

commonly available, it has been chosen to parallel the semiconductors in all positions in order to achieve a more realistic scaled down version of a shipboard PDN SSBTS. Each of the selected modules contains two devices. The IGBT module contains one IGBT and one diode, and the diode module contains two diodes. This is shown in Fig. 7a. The active devices are driven by a commercial *Semikron SKHI 10* gate driver board. The layout of semiconductors on the device heatsink is shown in Fig. 7b and has the goal of compromising between heat distribution, size and ease of assembly/connection.

IV. Thermal Conduction Tests

The goal of thermal testing of the SSBTS is to characterize the thermal performance of the prototype during conduction of its nominal current I_{nom} of $100\,\mathrm{A}$. The test also aims to determine whether there exists a significant difference in temperature between parallel connected semiconductor devices. The principle of this test is shown in Fig. 10a. A low voltage DC supply is operated in current limitation, circulating I_{nom} in the SSBTS. The case temperature of the semiconductors is sensed as in Fig. 10b.

For the purpose of thermal testing, the SSBTS is cooled with forced air cooling provided by fans mounted on the heatsink. No current rate limiting inductor is connected in this test, as it is not relevant for the purpose of evaluating current sharing and temperature among paralleled semiconductor devices. Fig. 11 displays the results of the test with interrupted forced air cooling at $100\,\mathrm{A}$. The test is started with forced active cooling and the semiconductor case temperature allowed to reach and maintain its steady state. Cooling fans are then turned off and the module case temperature increases to its pre-determined upper limit of $85\,^{\circ}\mathrm{C}$. This corresponds to a junction temperature for both IGBTs and diodes of approximately $105\,^{\circ}\mathrm{C}$, which is deemed sufficient to evaluate current sharing over the full range of semiconductor junction temperatures. Cooling is then reactivated and the temperatures settle to the same initial steady state. The test verifies that with the employed forced cooling the temperatures of all semiconductor module do not deviate significantly from one another, and that in the event of cooling interruption, the same steady state can be achieved again through reactivation of the forced air cooling. More importantly, the test shows that there is no divergence in temperature between parallel connected semiconductor modules.

Table I sums up the thermal steady state with forced active cooling during current conduction. The table also includes the measured voltage drop and estimated current of each device. The current estimation is performed by using a precision voltmeter to measure the voltage drop on the bus bar carrying the current of the device. These measurements are taken for both the forward and reverse current direction of the SSBTS, to ensure current is appropriately shared in both directions of conduction.

Table I also allows the computation of the device's conduction losses:

$$P_{loss}^{forward} = \sum I_{module,i}^{forward} * V_{module,i}^{forward} \approx 370\,\mathrm{W} \quad (8)$$

$$P_{loss}^{reverse} = \sum I_{module,i}^{reverse} * V_{module,i}^{reverse} \approx 370\,\mathrm{W} \quad (9)$$

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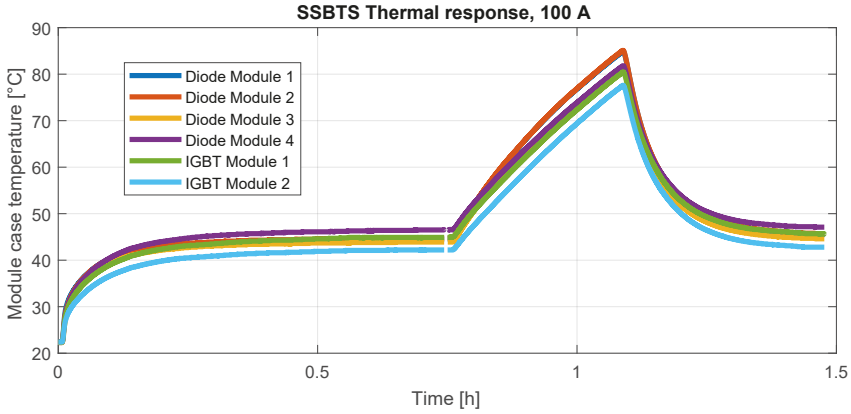

Fig. 11: Temperature of semiconductor module case during thermal conduction test at I_{nom} = 100 A.

TABLE I: Case temperatures, voltages and currents for all semiconductor modules at 100 A steady state.

	Diode module 1	Diode module 2	Diode module 3	Diode module 4	IGBT module 1	IGBT module 2
Case Temperature [°C]	39.2	38.2	38.0	40.7	39.4	36.7
Device current forward direction [A]	50.9	49.1	51.3	48.7	50.8	49.2
Device voltage forward direction [V]	1.21	1.21	1.21	1.21	1.26	1.26
Device current reverse direction [A]	46.5	53.5	49.5	50.5	51.4	48.6
Device voltage reverse direction [V]	1.21	1.21	1.21	1.21	1.26	1.26

Which show that the conduction loss at 100 A is of 370 W in both directions of conduction, resulting in losses of $\approx 0.75\,\%$ for the considered operating point.

V. SSBTS Switching Tests

To characterise the behaviour of the SSBTS during current interruption, several tests were conducted. The test setup principle is shown in Fig. 12 and the physical setup in Fig. 13. Capacitor C is charged to 500 V and then the SSBTS is turned on to create a resonant LC circuit between C and $L_{external}$. This causes the resonant current to rise almost linearly, until it is interrupted after a preset time interval t_{on}. In this initial test, the SSBTS is externally controlled by a signal generator and does not autonomously decide when to interrupt. The signal generator keeps the SSBTS on for t_{on}, which is predetermined based on the test setup and SSBTS parameters, as:

$$t_{on} = \frac{L_{external} + L_{didt}}{V_{DC}} I_{max} \tag{10}$$

The rate of increase of current in the SSBTS is determined by $V_{DC} = 500\,\text{V}$ and the sum of $L_{external}$ and L_{didt}. The switching performance of the device is evaluated with different values of $L_{external}$ of 0 µH, 5 µH and 16 µH. This corresponds to t_{on} equal to 20 µs for both $L_{external} = 0\,\mu\text{H}$ and $L_{external} = 5\,\mu\text{H}$, and $t_{on} = 25\,\mu\text{s}$ for $L_{external} = 16\,\mu\text{H}$. The device is tested with and without RC snubber in parallel with the IGBT modules. The results

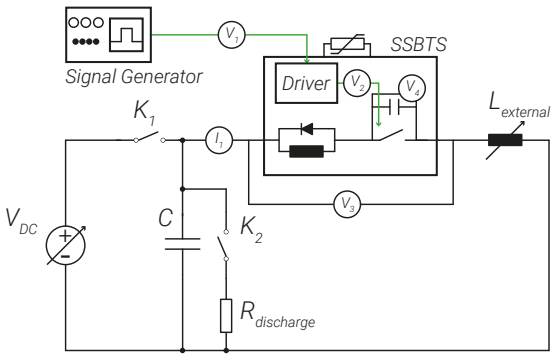

Fig. 12: Switching test setup principle schematic with measurement points of sensed SSBTS quantities. The values of the passive elements are as follows: $V_{DC} = 500\,\text{V}$, $C = 230\,\mu\text{F}$, $R_{discharge} = 480\,\Omega$, $L_{didt} = 48\,\mu\text{H}$ and $L_{external}$ is varied between 0, 5 µH and 16 µH.

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Fig. 13: Switching test setup with, from left to right, DC voltage source, measurement station, SSBTS and signal generator, di/dt limiting inductors.

of the tests are displayed in Fig. 14:

(a) The device is initially tested with no external inductance and without snubber. The SSBTS is turned *ON* at $t = 5\,\mu s$ and the current increases almost linearly for $t_{on} = 20\,\mu s$, after which the device is turned *OFF*. The voltage on C remains virtually unchanged during this process. When the device is turned *OFF*, a voltage spike due to the stray inductance in the current path is measured on both SSBTS and IGBT terminals, the peak of which is limited by the MOVs at the terminals of the device. Once the device is *OFF*, the current is interrupted in approximately $1.5\,\mu s$.

(b) Adding $L_{external} = 5\,\mu H$ in the current path, the time needed for the current to drop to $0\,A$ after the SSBTS goes *OFF* is increased to approximately $3.5\,\mu s$. This is due to the increase in stored energy to be dissipated by the MOVs. It can be seen that the clamping of the voltage by the MOVs is effective by observing that the peak of the voltage remains the same as with no added $L_{external}$

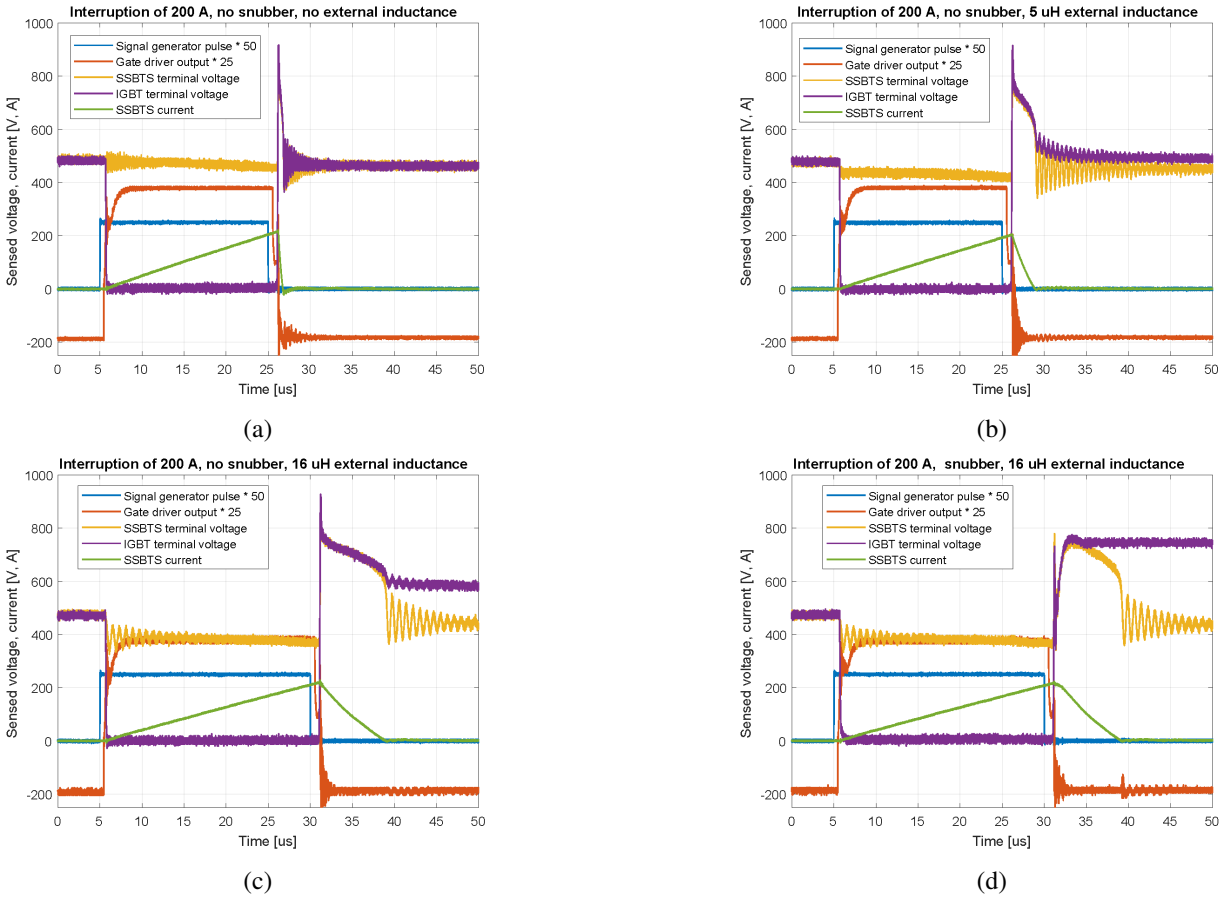

Fig. 14: Switching test results with the SSBTS being externally controlled by a signal generator. The *ON* time of the device, t_{on}, is determined based on the resonant LC circuit formed by C and $L_{didt} + L_{external}$, and preprogrammed into the signal generator.

(c) With $L_{external}$ increased to $16\,\mu H$, t_{on} is increased to $25\,\mu s$. The fall time of the current increases to almost $10\,\mu s$, as the stored energy in $L_{external}$ is further increased.

(d) The addition of the snubber to the SSBTS mitigates the voltage spike at the moment of turn *OFF*. A reduction of this spike could be achieved by redesigning the snubber and further decreasing its stray inductance. The voltage on the IGBT terminals is maintained at peak value after the device is turned *OFF* due to the large discharge capacitor of the snubber. The full discharge of the snubber capacitor is in the range of $10\,ms$. The same goes for the dissipation of the magnetic energy of L_{didt} through the on-state resistance of the antiparallel diode D_L.

The main conclusions to be drawn from the test are:

- The current fall time following the device being turned *OFF* is proportional to the value of inductance $L_{external}$.
- In the absence of a snubber, the switching voltage peak is independent from $L_{external}$. Margin for improvement exists in the design of the RC snubber, minimizing its stray inductance *en lieu* of tunable snubber parameters.

VI. Standalone Switching Tests

The SSBTS device is once again tested in switching, without an external signal generator to turn the device *ON* and the *OFF* after a precomputed time interval. Instead, a controller is used to identify the presence of a fault and switch *OFF* the device. The controller, a rapid control prototyping platform (*RT-Box* from Plexim) is interfaced to the SSBTS through an interface board as in Fig. 16. The interface board allows the RT-Box to access the values of the current in L_{didt} and the voltage at its terminals. Additionally, the board provides a fiber optical interface between the RT-Box and the SSBTS gate driver. The sampling frequency of the controller is of $1\,MHz$. A principle schematic of the modified test setup is shown in Fig. 15.

By accessing the sensed values mentioned above, the controller can identify the presence of a fault through several different criteria, that can be considered independently or jointly:

- Current magnitude in L_{didt} higher than a programmable threshold.
- Rate of increase of current in L_{didt} higher than a programmable threshold.
- Voltage at the terminals of L_{didt} higher than a programmable threshold.

In the first test including the controller, it is chosen to perform switching similarly to what was done in Sect. V with the signal generator. The controller provides an *ON* pulse of the duration of $15\,\mu s$ after which the device is again turned *OFF*. The goal of this test is to visualize the sampled

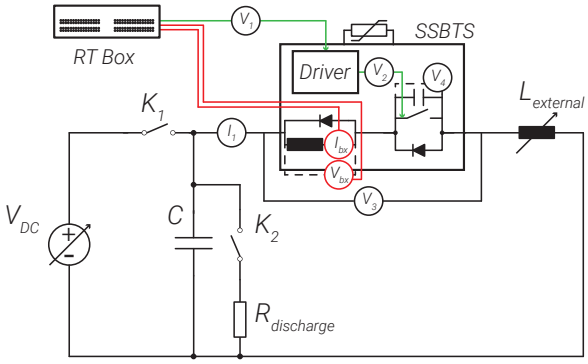

Fig. 15: Principle schematic of the autonomous switching test setup with measurement point of probes and onboard SSBTS sensors.

Fig. 16: An interface board provides interaction between the controller and the SSBTS device.

quantities as recorded by the controller and to evaluate whether the measurement is suitable for reliable fault identification. During tests employing the RT-Box as controller, inductance values are $L_{external}$ = $5\,\mu H$ and L_{didt} = $48\,\mu H$ and the switching snubber is always used. Fig. 17 allows a comparison of the switching as measured externally through the oscilloscope probes, and as recorded by *RT-Box* ADC. The displayed curves are:

(a) Electrical quantities in the test setup as mea-

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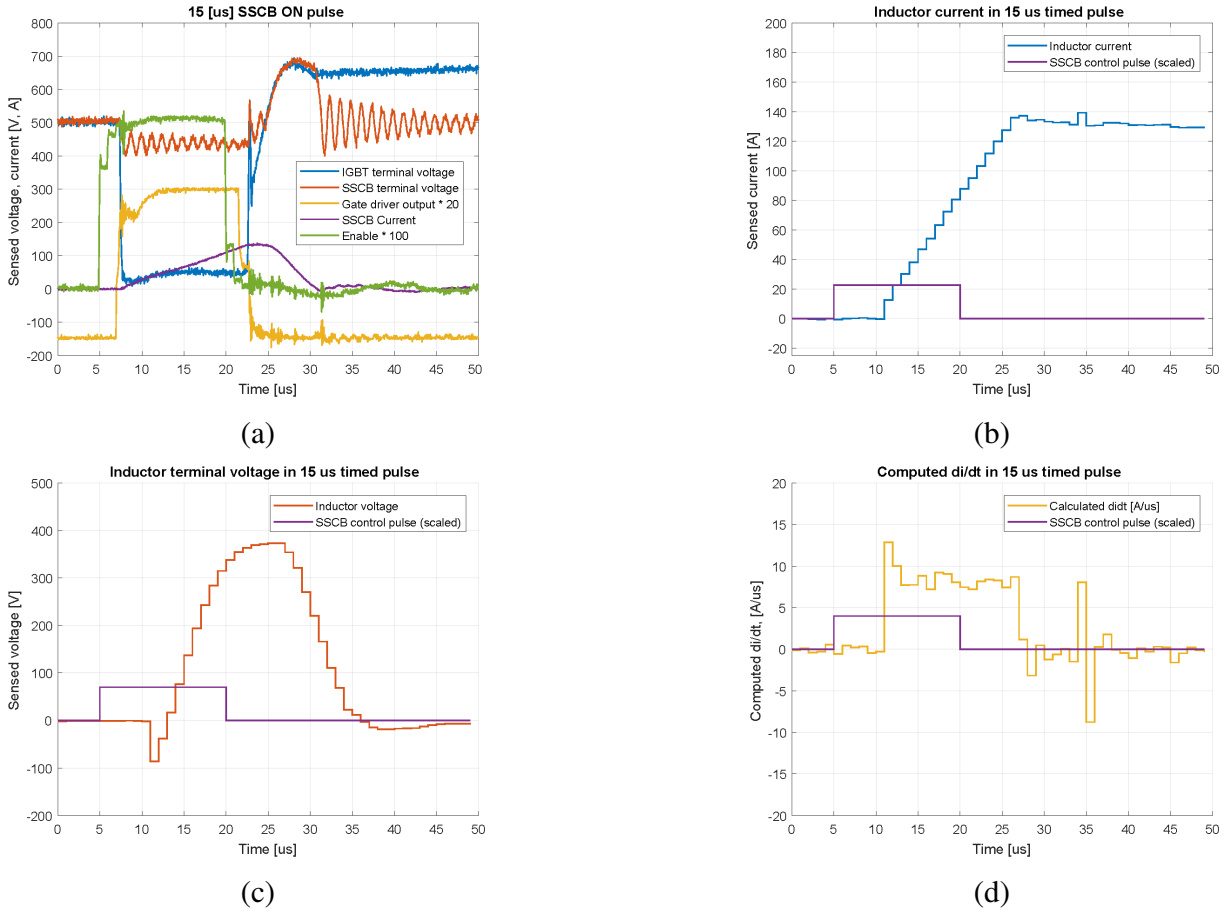

Fig. 17: Time switching test with *RT-Box* providing *ON* and *OFF* signals. The goal of the test is to determine if the quantities sampled by the controller can be used to determine the presence of a fault condition.

sured by oscilloscope connected voltage and current probes. The *enable* signal generated by the RT-Box is visible (green), as is the gate driver output (yellow). The switching performance of the device is equivalent to what was shown in Sect. V.

(b) Sampled current measurement of the SSBTS sensor and RT Box $15\,\mu s$ long *ON* signal. The delay between the signal and the sampled current is clearly visible.

(c) Sampled measurement of the voltage across the terminals of L_{didt}. The response of the voltage sensor is slower than that of the current sensor both in terms of delay and in terms of rate of increase.

(d) The current increase rate is computed as the difference between current in two subsequent samples, considering the RT-Box sampling time of $1\,\mu s$.

These tests show that it is possible to identify a fault based on all three criteria. Nevertheless it should be noted that the prototype has an open-frame structure that leaves sensors, sensor cables and controller interface board poorly shielded. This results in EMI issues at the time of the SSBTS switching *OFF*, visible in the form of measurement noise and spikes in sensed values in Fig. 17 and also later in Fig. 18. No measure was taken in assembling the prototype and test setup to mitigate such effects, as this does not represent an issue in terms of operation of the SSBTS at this proof-of-concept stage. The interference only happens once the device has already switched off, and therefore there is no risk of undesired tripping of the device as a consequence. Upon implementation of fault

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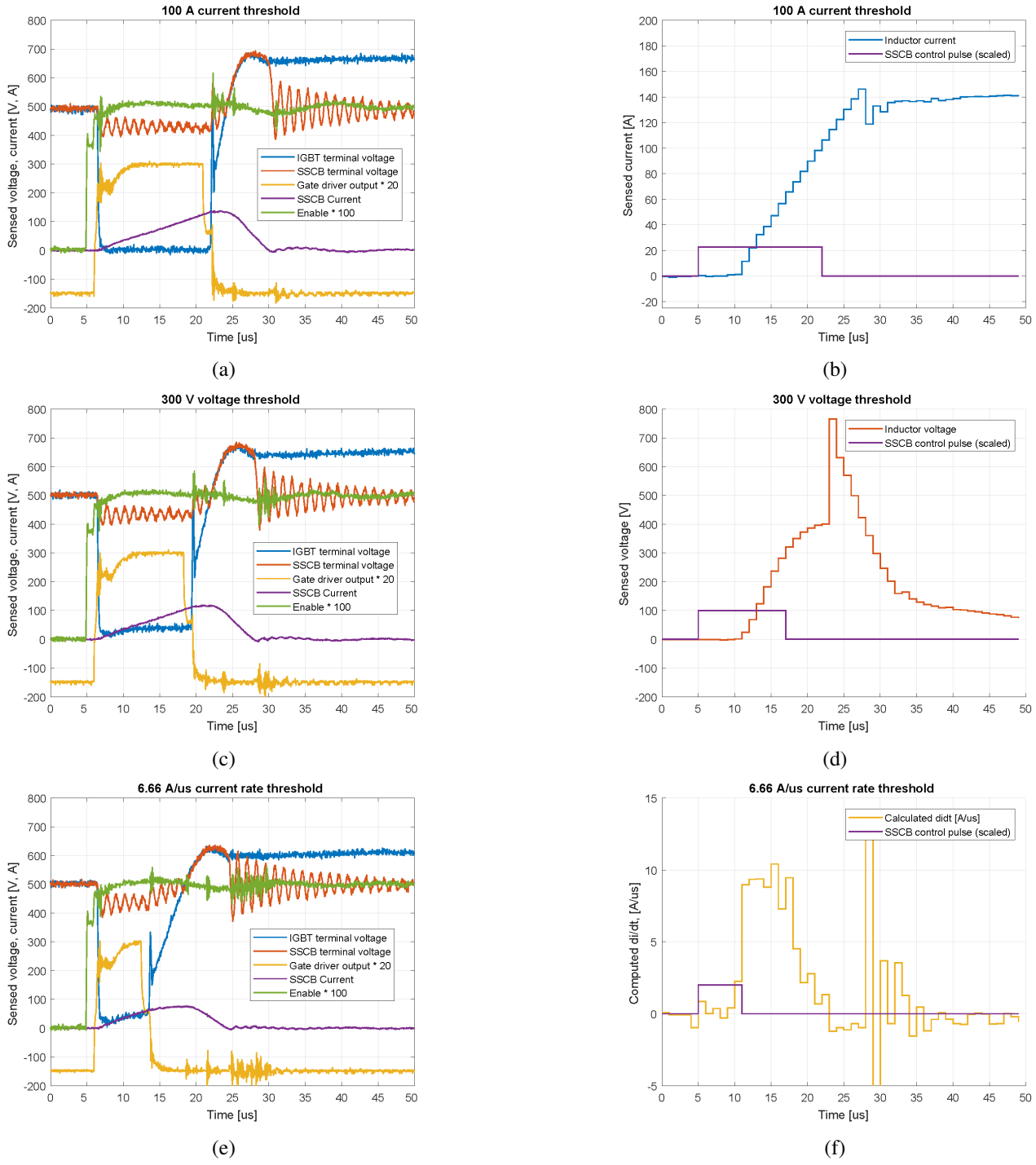

Fig. 18: (a): Performance of the SSBTS when switching based on a current threshold of $100\,\mathrm{A}$. The device switches *OFF* in less than $20\,\mu\mathrm{s}$ resulting in a current overshoot of about $40\,\mathrm{A}$, well below $I_{max} = 200\,\mathrm{A}$; (b): The current measurement based on which the tripping of the device is performed shows some delay with respect to the switching signal, also provided by the device, and displays the effect of EMI at turn

OFF. (c): Switching based on a $300\,\mathrm{V}$ terminal L_{didt} voltage results in faster interruption and lower SSBTS current. (d): The SSBTS voltage measurement show a large peak at the time of turn *OFF*, again attributed to EMI, as the SSBTS terminal voltage remains unaltered in 18c; (e): The computation of $\frac{di}{dt}$ results in the fastest interruption with the lowest value of current in the device; (f): The vulnerability of the calculation of $\frac{di}{dt}$ is visible in the large steps taken by the value in subsequent time intervals.

detection algorithms on the RT-Box, the SSBTS is again tested using the different criteria for interruption. The results of autonomous switching tests are shown in Fig. 18. All three criteria result in successful recognition of faults and opening of the device. The time required to identify the fault depends on a combination of sensor delay, rise time and selected criterion:

- Identification of the fault based on current threshold results in the longest *ON* time and final current in the SSBTS. This is due to the current having to cross the set threshold of I_{mon} = $100\,\mathrm{A}$ before the device is turned *OFF*. As the current initially starts from $0\,\mathrm{A}$, the rise time of the current adds to the total time required to identify a fault.
- The voltage at the L_{didt} terminals allows for the identification of a fault condition regardless of the value of the current. This method is faster in switching the SSBTS *OFF* in this test scenario, in spite of the voltage sensor having larger delay and rise time compared to the current sensor. Nevertheless, in order to set an appropriate L_{didt} voltage threshold (in this case $300\,\mathrm{V}$), it is required to know how aggressive the loads connected to the DC buses interfaced by the SSBTS are, to avoid involuntarily tripping the device.
- Fault identification based on current $\frac{dI}{dt}$ employs a threshold of $6.66\,\frac{\mathrm{A}}{\mu\mathrm{s}}$ and results is the fastest fault current interruption. This is due to the combination of fast reaction and rise time from the employed current sensor, combined with the immediate reaction of the method that does not require the current to reach a specific value before tripping.

Even though fault identification based on current $\frac{dI}{dt}$ results in the fastest interruption, it is particularly sensitive to measurement noise and EMI. To avoid undesired tripping of the device due to measurement noise, it is possible to average the measurement over several samples, or filter the output of the ADC. Nevertheless, both these options increase the reaction time of the SSBTS by inserting additional delays. While this is likely necessary in real applications to prevent the device from tripping due to noise, the solution used by the authors and effective for the sake of testing is to rely on a single $\frac{di}{dt}$ computed sample for optimal speed of fault identification. This is combined with a high current rate of increase tripping threshold. Having a sufficiently high tripping threshold guarantees that measurement noise will not cause unwanted tripping, and neither will load variations. For the presented device the $6.66\,\frac{\mathrm{A}}{\mu\mathrm{s}}$ was chosen as $\frac{2}{3}$ of the worst case scenario current increase rate:

$$\left(\frac{di}{dt}\right)_{threshold} = \frac{2}{3}\frac{V_{DC}}{L_{didt}} = \frac{2}{3} * \frac{500\,\mathrm{V}}{48\,\mu\mathrm{H}} \approx 6.66\,\frac{\mathrm{A}}{\mu\mathrm{s}} \tag{11}$$

While this solution guarantees a strong degree of resilience against unwanted tripping of the device, it best operates in combination with current magnitude threshold fault identification. While the relatively high current rate of increase threshold will only be reached for the most aggressive faults posing an immediate threat to the system, faults resulting in a lower rate of current increase will not be identified through $\frac{di}{di}$ and their detection is left to the current magnitude threshold.

VII. Conclusion

This paper presented a novel SSBTS topology for DC applications and demonstrates its operating principles on the developed prototype. The hardware of the device was successfully thermally tested in regular operation and bus-breaking performances under different circuit conditions. It is also shown how standalone operation can be achieved with a controller being integrated in the SSBTS. Three different fault detection methods, based on device current, inductor voltage and current rise rate are tested, and could be in practice all used jointly. Yet, these considerations are not presented here. The simplicity of the topology, offered by the use of a

single active devices, offers increased reliability for DC applications, such as those found in marine sector. The topology also offers possibilities in terms of scalability to increased power and voltage rating through parallel and series connection of multiple units, respectively. Due to lack of space, this option is not explored in the paper and will be explored in future work.

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