This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JESTPE.2020.2992946, IEEE Journal of Emerging and Selected Topics in Power Electronics

Analysis of Large-Signal Output Capacitance of Transistors using Sawyer–Tower Circuit

Nirmana Perera, *Student Member, IEEE,* Georgios Kampitsis, *Member, IEEE,* Remco Van Erp, Jessy Ançay, Armin Jafari, Mohammad Samizadeh Nikoo, *Member, IEEE,* and Elison Matioli, *Member, IEEE*

***Abstract*— A detailed analysis on the Sawyer–Tower method used in the measurement of large-signal output capacitance (C_o) of power transistors is presented, followed by important design recommendations to obtain accurate results. Key factors affecting the proper implementation of the technique, such as power amplifier characteristics, load slew-rate, reference capacitor (C_{ref}) and reverse conduction of the device are addressed, with accompanying simulation and experimental results for Si, SiC and GaN devices. A thorough investigation on the selection of C_{ref} is presented, with a new equation to correctly determine its value for a given voltage swing and output capacitance range of the Device Under Test (DUT). We report that the Sawyer–Tower circuit impose the DUT to enter steady-state reverse conduction under certain conditions, leading to charge-voltage (QV) hysteresis patterns unrelated to C_o. Our analysis reveals that the origin of this phenomenon is related to DUT's leakage current, and that it could be minimized by proper selection of the excitation frequency. This work intends to provide an effective guide on designing and using the Sawyer–Tower circuit and to induce further scientific insight in characterizing C_o.**

***Index Terms*—C_o, C_{oss}, E_{diss}, Sawyer–Tower, output capacitance, large-signal losses, soft-switching losses, WBG devices.**

I. Introduction

With the emergence of Wide-Band-Gap (WBG) semiconductor devices, high-frequency power converters have gained increased attention [1]–[8]. However, the operation of power electronics in the MHz range is influenced by the power losses associated with device output capacitance, C_o [9]. The observation of hysteresis losses in charging–discharging C_o of Si Super-Junction (SJ) MOSFETs [10]–[13], and WBG devices [13]–[16], initiated increased focus on device C_o and its large-signal behaviour, as the data-sheet provided small-signal capacitance, C_{oss}, is incapable of explaining such behaviour.

One of the main techniques adapted to observe the large-signal behaviour of C_o is the Sawyer–Tower circuit [16]–[20]. The circuit consists of a signal generator, a high-voltage amplifier, a fixed linear reference capacitor, C_{ref}, and the Device Under Test (DUT). The operation of the circuit is heavily dependent on all its parameters. For instance, the output resistance and the current limit of the high-voltage amplifier could distort the excitation signal applied on the DUT. The characteristics of C_{ref} depends on the dc-bias voltage and the excitation frequency, f_e, applied on it, and could compromise the measurement accuracy. A DUT with large C_{oss} could result in a low-impedance load that could exceed amplifier's loading capabilities. Neglecting the effects of these parameters on the circuit inevitably lead to measurement inaccuracies and false conclusions. Therefore, a thorough investigation on the technical aspects of the method is essential.

This work was supported in part by the Swiss Office of Energy (SFOE) Grant Numbers SI501887-01 (MEPCO) and SI501568-01. The authors are with the Power and Wide-Band-Gap Electronics Research Laboratory, École Polytechnique Fédérale de Lausanne, 1015 Lausanne, Switzerland. (e-mail: nirmana.perera@epfl.ch, elison.matioli@epfl.ch)

TABLE I
Important Symbols and Abbreviations Used in the Paper

Symbol	Description
C_o	output capacitance of the Device Under Test (DUT)
C_{oss}	small-signal output capacitance
C_{ref}	reference capacitance
C_{eq}	equivalent load capacitance
Q_o	output charge of the DUT
Q_{oss}	small-signal output charge of the DUT
q_{REF}, Q_{REF}, q_{ref}	total, dc and ac components of C_{ref} charge
ΔQ_+	positive dc charge in C_{ref} due to leakage of the DUT
E_{diss}	energy dissipated in C_o during a charge–discharge cycle
v_S	signal generator output voltage
v_A	voltage amplifier output voltage
v_{IN}, v_{in}	total and ac components of the input voltage to the load
V_p	peak value of v_{in}
v_{DS}, V_{DS}, v_{ds}	total, dc and ac components of drain–source voltage
$V_{DS\text{-}max}$, $V_{DS\text{-}min}$	maximum and minimum of large-signal v_{ds} swing
v_{REF}, V_{REF}, v_{ref}	total, dc and ac components of C_{ref} voltage
V_{ref+}, V_{ref-}	peak values of positive and negative swings of v_{ref}
v_{GS}	gate-source voltage
V_{bus}	bus (or dc-link) voltage
$-V_{FW}$	dc voltage drop during reverse conduction of the DUT
V_{BIAS}	steady-state dc bias voltage in C_{ref}
i_{C_o}	total-instantaneous current through C_o of the DUT
i_{LEAK}, $I_{LEAK\text{-}max}$	total and maximum leakage current of the DUT
i_{LOAD}	total-instantaneous load current
I_{limit}	current limit of the voltage amplifier
G, R_o	gain and output resistance of the voltage amplifier
f_e	frequency of the ac excitation signal
$S.R.\big\vert_{exc}$	slew-rate of the amplified ac excitation signal
$S.R.\big\vert_{amp}$	maximum limit of the slew-rate of voltage amplifier
$S.R.\big\vert_{dominant}$	dominant slew-rate of the equivalent load
$rate_1$	rate of change of voltage across C_{eq} due to I_{limit}
$rate_2$	voltage rise-rate of C_{eq} subjected to RC limitations

This work presents a detailed discussion on the Sawyer–Tower technique for large-signal output capacitance characterization, addressing key factors affecting the accuracy and the range of measurements. Two new equations are given to correctly express output charge, Q_o, versus v_{DS} (QV), and to select C_{ref} in terms of required voltage swings. It is proved that the Sawyer–Tower circuit (under certain conditions) in steady-state could make the DUT enter reverse conduction at the negative peak of the input signal: this could compromise the basic assumptions of the method. The paper is structured as follows. Section II provides important background on large-signal C_o behaviour and motivation for the work. Section III explains the

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operation of the Sawyer–Tower circuit. Section IV addresses the aforementioned key technical aspects. Sections V and VI discuss design recommendations and conclusions.

II. Motivation

In this section, the importance of large-signal C_o and Q_o measurements are discussed with practical examples to provide motivation for the presented work. The Sawyer–Tower method is compared with existing large-signal measurement methods.

A. Small-Signal vs Large-Signal Output Capacitance

To estimate C_o-related losses, conventionally, the device data sheets provide a *small-signal* output capacitance[1], C_{oss}, that is measured by applying a small ac perturbation (limited to 10–200 mV) over a dc bias on the DUT (with $v_{GS} = 0$) [24]. Unlike the real operating conditions in power electronic circuits, these measurements never subject C_o to a large voltage swing. Recent research shows that data-sheet based C_{oss} curves fail to accurately estimate losses related to C_o [17], [25]. Another limitation of this method is that the C_{oss} value is dependent on the model used in the measurement tool for the extraction of the capacitance from impedance [26], [27].

On the other hand, *large-signal* measurements generally estimate C_o (or more often, Q_o) of a power transistor by subjecting the device to large voltages, for instance, between 0 V and bus voltage (V_{bus}), an approach that much better emulates the charge–discharge behaviour of C_o in an actual circuit [16], [17], [28]. Large-signal C_o is then defined as $i_{C_o} = C_o(v_{DS}) \cdot dv_{DS}/dt$, from which we deduce

$$C_o(v_{DS}) = dQ_o(v_{DS})/dv_{DS}. \tag{1}$$

This definition should be used to avoid a common confusion where a non-linear capacitance is defined by the linear equation $C_o(v_{DS}) = Q_o(v_{DS})/v_{DS}$ that fails to capture the device's large-signal variation of its charges [17], [29]. Acknowledging the fact that both large-signal charge and capacitance are functions of v_{DS}, for the remainder of the paper, we use the simple notations $C_o(v_{DS}) = C_o$ and $Q_o(v_{DS}) = Q_o$.

The difference between large and small-signal curves, and hence the severity of the error in actual Q_o (or C_o) and related losses, varies based on the device type. The implications of this in real converter applications are twofold, depending if the device is hard switched or soft switched. If the device is hard switched, for instance in a double-pulse test circuit, the total C_o-related losses occur first in charging C_o through the available circuit path, and then discharging the charge stored in C_o through the device channel itself [30]. The resulting loss is given by the product $Q_o|_{V_{bus}} \cdot V_{bus}$. Therefore, the error in the losses is directly related to the estimated Q_o value at a given V_{bus}. Fig. 1a shows an example for a Si-SJ transistor, where small-signal Q_{oss} value varies by 25 % in comparison to the large-signal value, resulting in a significant error in hard-switched losses. On the other hand, Fig. 1b shows a case for a GaN device, where the large-signal Q_o curve (solid green line) shows less deviation from the data-sheet curve, with negligible hysteresis at 100 kHz.

[1]The following notation is used to refer to a device's output-capacitance-related parameters: output capacitance, C_o; output charge, Q_o; energy stored in the output capacitance, E_o [21]. The corresponding small-signal parameters are denoted, using the conventional method used in device data sheets, as C_{oss}, Q_{oss} and E_{oss} [22], [23].

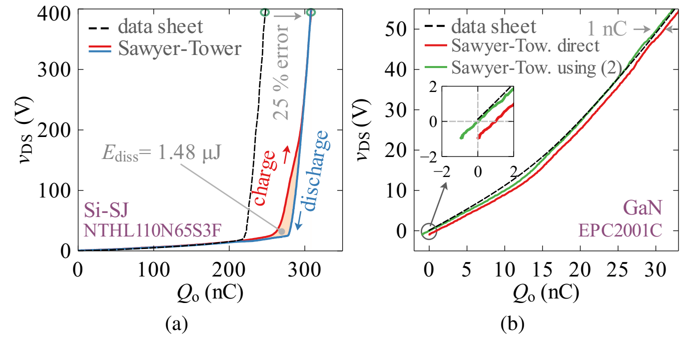

Fig. 1. Large-signal Q_o vs v_{DS} curves obtained from the Sawyer–Tower circuit at 100 kHz for two devices, where the dashed black lines show the small-signal Q_{oss} estimated based on data-sheet C_{oss} curves. (a) The Si-SJ device (650 V) exhibits a large difference in small and large-signal curves, with Q_o at 400 V showing a 25 % increase in the large-signal results. With distinct charging–discharging paths (solid red and blue lines respectively), the Si-SJ device shows a considerable hysteresis loss of E_{diss}= 1.48 μJ. (b) A 100-V GaN device with different small and large-signal curves, but with negligible hysteresis: only the charge path is shown in green as the discharge path coincides with it. The red line shows the direct Sawyer–Tower result without using (2) (see Section III).

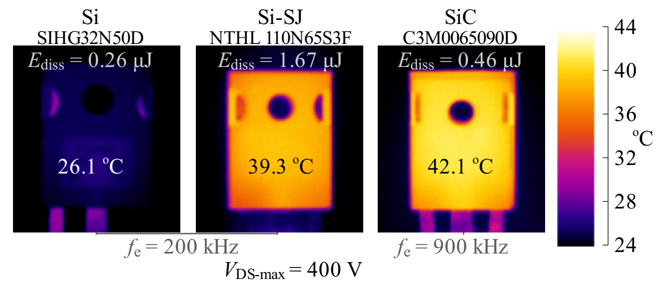

Fig. 2. Thermal images showing the temperature rise of three devices (Si, Si-SJ and SiC) with different E_{diss} values (estimated using the Sawyer–Tower circuit). The devices (at v_{GS}= 0 V) have the same hardware package (TO-247) and were excited sinusoidally in the Sawyer–Tower circuit arrangement at 400 V. The observed losses are not possible to be calculated based on data sheets, and ideally, these devices should not dissipate any power as charging and discharging of C_o is assumed to be lossless. The observed power dissipation reveals the need for a proper C_o characterization.

If the device C_o is resonantly charged and discharged with soft-switching conditions, based on the data-sheet curves, no C_o-related loss should occur [16]. However, the Q_o vs v_{DS} curves of the Si-SJ device in Fig. 1a clearly reveals a difference in the charge–discharge paths, resulting in a hysteresis loss, E_{diss} [20]. Fig. 2 shows three devices with similar hardware packages that were excited with a large-signal sinusoidal signal with a 400-V peak voltage. The Si and Si-SJ devices were excited at 200 kHz. The Si-SJ device exhibits a significant temperature rise, hence much larger power dissipation ($P_{diss} = E_{diss} \cdot f_e$) compared to the Si device. This is due to relatively large (1.67 µJ > 0.26 µJ) E_{diss} of the Si-SJ device. Although the SiC device is switched at a much higher frequency (4.5 times higher), compared to the other two devices, it only shows a temperature 3 °C higher compared to the Si-SJ device: this

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is due to SiC device's lower E_{diss} value of (0.46 μJ < 1.67 μJ). These results show the importance of the large-signal Q_{o} vs v_{DS} measurements in predicting both hard and soft-switching losses, that are not possible to estimate based on data-sheet based small-signal C_{oss} (or Q_{oss}) curves.

B. Measurement Techniques of Large-Signal C_o and Q_o

The Sawyer–Tower technique has traditionally been used for ferroelectric dielectric material characterization [19]; and now has been adapted to characterize large-signal C_{o} of Si, Si-SJ, SiC and GaN power transistors [16]–[18], [20], and very recently of SiC power diodes [15]. It initially obtains the device's output charge characteristic (Q_{o} vs v_{DS}) by applying a large excitation voltage, and subsequently, C_{o} is obtained by taking the derivative of Q_{o} with respect to v_{DS}.

The Sawyer–Tower technique provides several distinct advantages for C_{o} characterization. The DUT (gate and source shorted) and a reference capacitor are the only two electronic devices involved: no external components such as inductors, active switches, gate drivers or control circuitry are required. Only two voltage measurements are involved (v_{IN} and v_{REF} in Fig. 3a): this allows the method to be very accurate even at lower Very-High-Frequency (VHF) levels as there are no current measurements involved, which are prone to higher inaccuracies. The losses in the circuit are only due to Q_{o} hysteresis losses (Section IV-F discusses validity of this): no conduction or any other external losses exist, allowing direct evaluation of E_{diss} by thermal measurements. A large range of voltage-swings across v_{DS} can be achieved: if the voltage is limited due to the amplifier's output voltage rating, a simple High-Frequency (HF) transformer can be used to boost the voltage output, provided that the amplifier's output power capability is not exceeded for the given f_{e}. Moreover, the method can easily perform frequency sweeps, by changing the signal-generator output frequency (=f_{e}).

However, the Sawyer–Tower method has some technical limitations. The maximum voltage swing for a given f_{e} (even with a HF transformer) is confined by the voltage amplifier [20], [28], because the gain of the amplifier degrades with increasing f_{e} as the power output capability of the amplifier is limited. The response due to different excitation signal types offer additional details about a device's C_{o} [16]: for instance, triangular waveforms allow to observe the response due to a constant dv/dt excitation, whereas pulsed excitation creates a very high dv/dt condition. Although near sinusoidal waveforms could be applied at higher frequencies, the application of pulsed waveforms is limited by the bandwidth of the voltage amplifier and the value of the equivalent load capacitance, C_{eq}.

Several alternative methods exist for large-signal Q_{o} (or C_{o}) estimation. A nonlinear-resonance method relies upon the resonance between a pre-calibrated inductor and the device C_{o} [28]. The method only requires a low-voltage dc source as the input, and therefore, eliminates the need for a high-voltage high-bandwidth amplifier. Since the DUT is switched to generate the resonant pulse, the method requires gate driving circuitry and external control signals. Furthermore, it is necessary

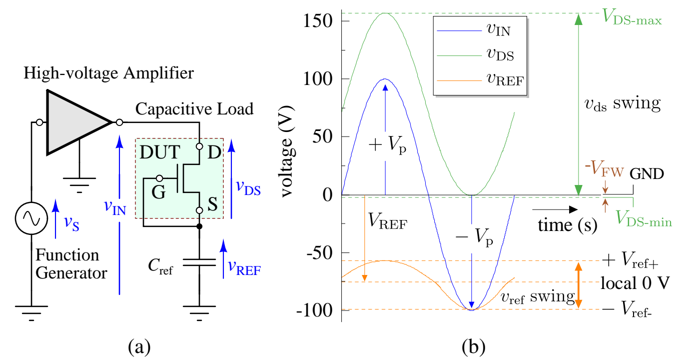

Fig. 3. (a) The Sawyer–Tower circuit, and (b) example of distribution of voltage waveforms in steady state. The *local 0 V* indicates the dc-level (V_{REF}) of v_{REF}, upon which its ac component v_{ref} varies.

to use different inductors for frequency sweeps. A modified version of the Sawyer–Tower circuit with improved bandwidth capabilities [13], involves a switched half-bridge arrangement (as a large-signal trapezoidal source) and an external LC component. Pure thermal/calorimetric measurements provide another way of large-signal C_{o} loss measurement. However, this only gives an estimation for losses at different v_{DS} values, and therefore fails to deliver *CV* or *QV* patterns of the DUT, that are instrumental in understanding large-signal C_{o} or Q_{o} dependence on voltage. In addition, at lower power dissipation levels, the accuracy of this method is compromised [20]. In another method, a soft-switched H-bridge configuration is used [14], with a DC voltage source, two DC chokes and a load inductance, and three dc capacitors. The total losses are estimated with a calorimetric approach, where the separation of C_{o} losses from the total losses is prone to measurement inaccuracies in several stages. Also, the method does not deliver any large-signal *CV* or *QV* patterns.

Although the Sawyer–Tower technique is based on a simple circuit, many factors could affect its valid operating range and subsequent measurements. And discourse on its proper implementation is limited in the technical literature. Recent research on the topic employ the Sawyer–Tower technique [16]–[18], and its variations [13], to demonstrate the difference between large and small-signal C_{oss} curves, however, an in-depth explanation of the circuit operation and its limitations is not given. The recent work in [20] addresses some details of the circuit such as the reference capacitor selection and the body-diode operation to a certain extent. Nevertheless, to the best of our knowledge, an in-depth analysis of the Sawyer–Tower technique for C_{o} measurement is not available in the literature. Our analysis in the next sections reveal important information about the practical operation of the circuit.

III. Operation of the Sawyer–Tower Circuit

The Sawyer–Tower circuit, shown in Fig. 3a, results in the steady-state voltage waveforms shown in Fig. 3b. The fundamental result of this method is a Q_{o} vs v_{DS} curve extracted from measured v_{REF} and v_{DS} data.

To obtain accurate results, a detailed analysis of the circuit is required. We consider a generic field-effect power transistor

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as the DUT whose gate and source terminals are shorted to remove the effects of gate capacitance, C_{GS}, from the circuit. Therefore, the only active part of the DUT is its C_o. The DUT is connected in series to a linear capacitor C_{ref} to form an equivalent load capacitance $C_{eq} = C_o \cdot C_{ref}/(C_o + C_{ref})$. C_{eq} is subjected to an input voltage v_{IN} created by amplifying a low-voltage signal v_S with an excitation frequency of f_e. In steady state, a dc-bias (V_{REF}) is built across C_{ref}, that corresponds to a dc charge, Q_{REF} [16]. Therefore, v_{IN} results only in an ac charge variation on C_{ref}, $q_{ref} = C_{ref} \cdot v_{ref}$, in steady state.

Since the DUT and C_{ref} are in series, the same current flows through them in steady state, leading to equal charge variations: and hence, $Q_o \propto C_{ref} \cdot v_{ref}$. However, the direct use of the expressions $Q_o = C_{ref} \cdot v_{ref}$ and $Q_o = C_{ref} \cdot v_{REF}$, found in the literature [16], [17] could lead to inaccurate estimations, as they do not provide the complete behaviour of Q_o vs v_{DS} variation. The first does not take into account the zero base-lined variation for Q_o, while the latter incorporates the dc-charge within C_{ref}. To address this problem, we introduce (2):

$$Q_o|_{v_{DS}} = C_{ref}\left(v_{ref} - v_{ref}|_{v_{DS}=0}\right), \tag{2}$$

which takes into account the finite reverse voltage of the DUT: the term $v_{ref}|_{v_{DS}=0}$ ensures that $Q_o = 0$ when $v_{DS} = 0$. An example is shown in Fig. 1b for a GaN device, where the red line shows the QV curve obtained directly from the Sawyer–Tower circuit: the zoomed inset reveals that $v_{DS} < 0$ when $Q_o = 0$. By adjusting the results using (2), the QV curve passes through the origin (solid green line), improving the accuracy of the measurement by 3.5 % at 50 V.

IV. Practical Considerations on the Circuit

The Sawyer–Tower setup is a sensitive circuit that can be affected by several parameters of the equipment used and system parasitics. More importantly, no consideration is given in the literature on how the range and behaviour of C_o affect the operation of the entire circuit. These factors are analysed and explained through an experimental setup (listed in Table II), and the detailed circuit in Fig. 4.

A. High-Voltage Amplifier and Equivalent Load

A high-voltage amplifier is required to boost the excitation signal (from a signal generator) to test the devices up to their rated voltages (e.g. 600 V). These amplifiers have two important characteristics that could affect the proper operation of the Sawyer–Tower circuit: 1) *Current Limit*, I_{limit}, and 2) finite *Output Resistance*, R_o. To study these effects independently, we assume the following conditions:

- a sinusoidal excitation signal $v_S = V_s \sin(\omega_e t)$;
- ideal C_{eq} with an infinite parallel resistance;
- output slew-rate of the amplifier (hardware-limited), $S.R.|_{amp}$, is larger than the slew-rate of the amplified v_S, $S.R.|_{exc} = G \cdot 2\pi f_e V_s$. (see Fig. 4).

$$S.R.|_{amp} \geq S.R.|_{exc} \tag{3}$$

TABLE II
List of Equipment Used for Experimental Analysis

Name	Manufacturer	Description
B1505A	Keysight	Power device analyser / Curve tracer
E4990A	Keysight	50-MHz impedance analyser
33600A	Keysight	Trueform waveform generator
WMA-300	Falco Systems	5-MHz high-voltage amplifier
MDO3104	Tektronix	Mixed domain 1-GHz (5 GS/s) oscilloscope

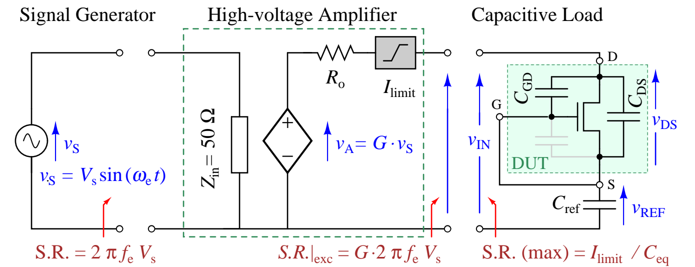

Fig. 4. Detailed Sawyer–Tower circuit highlighting slew-rates at each interface; amplifier output resistance, R_o, and current limit, I_{limit}; and the DUT where, $C_o = C_{GD} + C_{DS}$.

These two factors are directly related to the rate of change of load voltage, and therefore, could result in voltage distortions if overlooked. I_{limit} is a practical limit in commercial amplifiers and defines the maximum current through the load. Then the change in rate of voltage across C_{eq} is limited as given in (4).

$$rate_1 = \frac{dv}{dt} = \frac{I_{limit}}{C_{eq}} \tag{4}$$

The amplifier's R_o determines the RC time constant for the load and results in the following relation:

$$rate_2 = \frac{V_p}{4R_oC_{eq}}. \tag{5}$$

where V_p is the peak of the ac signal v_{in} applied to the load. Here, we have considered four time constants to reach the maximum load voltage. Both of these rates can limit the full propagation of the amplifier output v_A to the load.

- if $rate_2 > rate_1$, $rate_1$ becomes dominant and the maximum load slew-rate is determined by I_{limit} and C_{eq}. At the same time, if $S.R.|_{exc} > rate_1$, the load can't follow the input: v_{IN} becomes distorted as I_{limit} introduces a non-linearity to the circuit.
- if $rate_1 > rate_2$, the resultant load slew-rate is limited by R_o, V_p and C_{eq}. If $S.R.|_{exc} > rate_2$, the load will follow the input voltage shape, but with a gain reduction due to RC limitations.

These distortions are more pronounced when DUTs with large C_{oss} values are tested.

B. Effects of C_{oss} and C_{ref}

We base the following analysis on the small-signal output capacitance C_{oss}. For all commercial power transistors, C_{oss} is a monotonically decreasing function of the applied v_{DS}. Especially, in the "*low v_{DS} range*" (see Fig. 5), it is significantly larger (even an order of magnitude) than in the large v_{DS} range.

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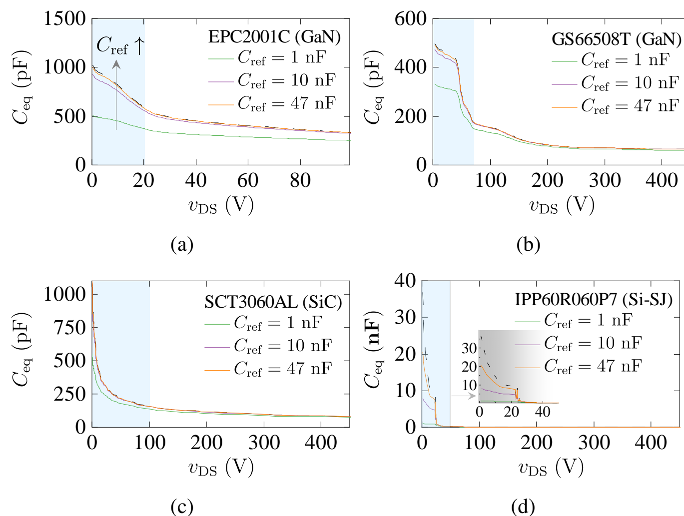

Fig. 5. C_{eq} vs v_{DS} curves of (a) EPC2001C (GaN), (b) GS66508T (GaN), (c) SCT3060AL (SiC), and (d) IPP60R060P7 (Si-SJ) transistors, for different C_{ref} values. The dashed black lines show the data-sheet C_{oss} curves. The shaded blue area highlights the "*low* v_{DS} *region*".

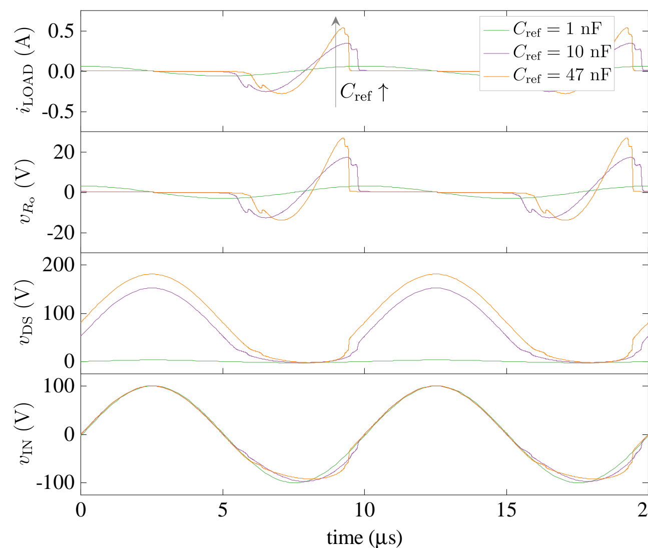

Fig. 6. *LTspice* simulation results showing the effects of having a large C_{oss} value in the low v_{DS} range, for $f_e = 100$ kHz. The DUT is a Si-SJ MOSFET (IPP60R060P7) with $C_{oss}|_{v_{DS}=0} \approx 40$ nF. The distortion in v_{IN} is intensified with increasing C_{ref} as Z_{load} further decreases.

Thus, the load impedance ($Z_{load} = 1/j\omega_e C_{eq}$) reduces greatly in the low v_{DS} range and results in the following implications:

1) v_{IN} gets distorted at the bottom of its negative half cycle (where the low v_{DS} range occurs) as a higher voltage drops across R_o, clearly depicted in Fig. 6.
2) the load current can surpass I_{limit} and alter v_{IN}.
3) exceeding the amplifier's power capability at large f_e values, due to increased load current.

To prevent any signal distortion, a proper C_{ref} value should be selected. As can be seen from Fig. 6, the lower the value of C_{ref}, the lower the distortion. However, excessive reduction of C_{ref} reduces the available share for the v_{DS} swing (as the ac voltage drop across C_{ref} increases), for a fixed V_p. To experimentally support this analysis, Fig. 7 shows v_{IN} for a Si-SJ MOSFET for different C_{ref} and f_e values. For the case

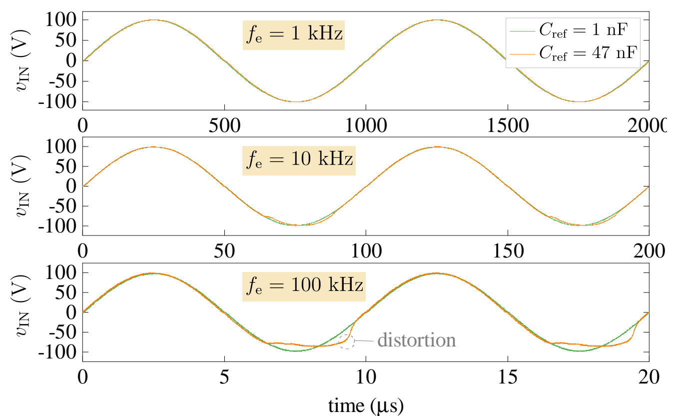

Fig. 7. Experimental waveforms of v_{IN} for the IPP60R060P7 MOSFET (Si-SJ) for different excitation frequencies. v_{IN} gets distorted when C_{ref} is large.

of $C_{ref} = 1$ nF ($\approx 0.025 \times C_{oss}|_{v_{DS}=0}$), no distortion occurs as expected; while a clear distortion in v_{IN} appears for the case of $C_{ref} = 47$ nF ($\approx 1 \times C_{oss}|_{v_{DS}=0}$).

The distortion increases with increasing f_e as the load impedance gets further lowered. Therefore, for a DUT with large C_{oss}, f_e should be chosen adequately low so that the amplifiers output power ($P_{out} \propto f_e \cdot G$) capability is respected. If the power capability is exceeded, then the gain G, and hence the available voltage output $v_A = G \cdot v_S$ will reduce.

C. Calculation of C_{ref}

The selection of C_{ref} is of vital importance for the correct operation of the Sawyer–Tower circuit [17], [18], [20]. Here we present a new equation to calculate C_{ref} based on design requirements. We assume that there is no distortion in v_{IN} due to the slew-rate limitations, and that C_{ref} is ideal and linear.

To derive an equation for the value of C_{ref}, consider C_o characterisation of a DUT for a v_{DS} swing of $V_{DS\text{-}min} = -V_{FW}$ to $V_{DS\text{-}max}$, and an input voltage swing of $\pm V_p$. Considering the load-side circuit; and at $v_{DS} = V_{DS\text{-}max}$, the following holds:

$$+V_p = V_{BIAS} + V_{ref+} + V_{DS\text{-}max}. \tag{6}$$

This equation can be further solved by realising that in steady state, $V_{BIAS} = V_{REF} = (-V_p + V_{FW}) + V_{ref-}$, where $-V_{FW}$ is the device's dc voltage drop during reverse conduction (see Section IV-F). Substituting this into (6) gives,

$$2\,V_p = V_{FW} + V_{DS\text{-}max} + V_{ref-} + V_{ref+}. \tag{7}$$

The term "$V_{ref-} + V_{ref+}$" can be substituted by using (8) and (9), which are easily derived from (2). Simplifying, we get an essential equation in (10) to calculate the value of C_{ref} required for a given v_{DS} swing of $V_{DS\text{-}max}$.

$$Q_{o\text{-}max} = C_{ref}\left(V_{ref+} - v_{ref}|_{v_{DS}=0}\right) \tag{8}$$

$$Q_{o\text{-}min} = C_{ref}\left(-V_{ref-} - v_{ref}|_{v_{DS}=0}\right) \tag{9}$$

$$C_{ref} = \frac{Q_{o\text{-}max} - Q_{o\text{-}min}}{2\,V_p - V_{DS\text{-}max} - V_{FW}} \tag{10}$$

Here $Q_{o\text{-}max}$ and $Q_{o\text{-}min}$ are the minimum and maximum charge stored in the DUT. For practical cases, $Q_{o\text{-}min}$ can be assumed

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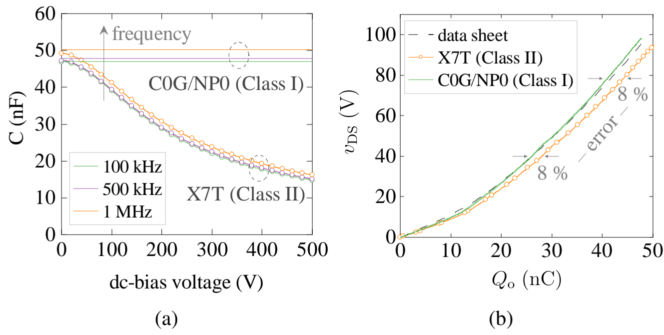

Fig. 8. (a) Capacitance vs bias voltage of C_{ref} measured with a Keysight B1505A curve tracer, and (b) experimental Q_o curves for an EPC2001C transistor at $f_e = 100$ kHz using same C_{ref}. A Class I C0G/NP0 capacitor (TDK CGA8R4NP02J473J320KA) and a Class II X7T capacitor (TDK CGA5L1X7T2J473K160AC) with nominal values of 47 nF are compared.

to be negligible compared to $Q_{o\text{-max}}$: the small-signal $Q_{oss\text{-max}}$ that can be easily estimated from data-sheet C_{oss} curves is a good first approximation for $Q_{o\text{-max}}$. For instance, for an EPC 2001C device subjected to $V_{DS\text{-max}} = 50$ V, (where $Q_{o\text{-max}} \approx$ 30 nC at 50 V), C_{ref} should be higher than 600 pF if V_p is limited to 50 V.

D. Selecting the Type of C_{ref}

There are mainly two commonly used Multi-Layer Ceramic Capacitor (MLCC) types available in the market that are classified upon their dielectric class (of EIA standard): Class I and Class II. Class I dielectric based capacitors, also known as C0G/NP0 temperature compensating capacitors, are based on non-ferroelectric materials and exhibit a fixed capacitance with the bias-voltage: measured characteristics for this type of capacitor is shown in Fig. 8a. On the other hand, the capacitance of Class II capacitors (e.g. X7R, X7T and X5R types) decreases with the bias-voltage as shown in Fig. 8a.

Fig. 8b shows experimental Q_o curves for an EPC2001C transistor using both types of capacitors as C_{ref} (nominal value = 47 nF), where the dashed black line denotes the small-signal Q_{oss} curve. The curve for the X7T type shows a clear deviation from the C0G/NP0 type: an 8% error is observed in Q_o where the deviation reaches up to 3.7 nC for $v_{DS} = 100$ V. C0G/NP0 (Class I) is, thus, the preferred type because C_{ref} should be independent of V_{BIAS} throughout the whole v_{DS} range.

E. Frequency Dependence of C_{ref}

Although C0G/NP0 type has a fixed capacitance throughout the voltage range, both its capacitance and equivalent series resistance, R_{ESR}, are frequency dependent. Thus for a given C_{ref} value and type, f_e has an upper limit.

Measured impedance and capacitance values of two different C0G/NP0 capacitors (C_1 and C_2) are shown in Fig. 9: their impedances exhibit significant decrease when f_e approaches the Self-Resonant Frequency (SRF) of the capacitor. This is due to the increase of both capacitance and R_{ESR} with f_e up to the SRF. This results in an overall increase in the load current,

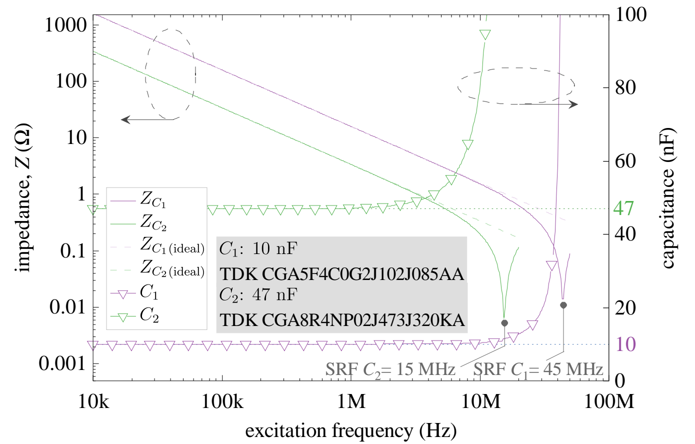

Fig. 9. Variation of impedance and capacitance of two C0G/NP0 capacitors (C_1 of 10 nF and C_2 of 47 nF) measured with Keysight E4990A impedance analyser. The actual impedance values (Z_{C_1} and Z_{C_2}) starts to deviate from their ideal ones (indicated by dashed lines) when approaching their SRFs.

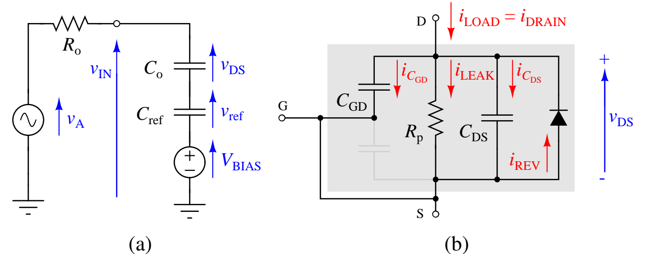

Fig. 10. (a) Sawyer–Tower circuit in steady state where $v_{REF} = v_{ref} + V_{BIAS}$, and (b) a model of the DUT showing the leakage current i_{LEAK}.

and hence, an increase in the voltage drop across R_{ESR}. The measured v_{ref}, in steady state, is now given by (11).

$$v_{ref}\big|_{measured} = v_{ref}\big|_{actual} + i_{LOAD} \cdot R_{ESR} \tag{11}$$

The term $i_{LOAD} \cdot R_{ESR}$ adds an error to the calculated Q_o value that gets higher as f_e approaches SRF. Operation close to the SRF also introduces a deviation of C_{ref} from its nominal value, adding further to the Q_o estimation error. A discussion on the optimal f_e range is given in Section V, showing the upper bound for f_e when selecting a commercial capacitor.

F. Reverse Conduction of the DUT

The Sawyer–Tower circuit is based on the fundamental assumption that the current through C_{ref} and the device's C_o are always equal in steady-state, meaning that there is no reverse conduction (third-quadrant operation) of the DUT [15], [20]. Our investigations show that this does not hold true for all the design/operating conditions.

To elucidate, we consider that the device has reached steady state, where the dc bias in C_{ref} is given in (12), in which V_{FW} is assumed to be a fixed dc voltage drop independent of the level of reverse current.

$$V_{BIAS} = V_{REF} = (-V_p + V_{FW}) + V_{ref\text{-}} \tag{12}$$

The corresponding circuit is given in Fig. 10a, where we get,

$$v_{DS} = v_{IN} - v_{ref} - V_{BIAS}. \tag{13}$$

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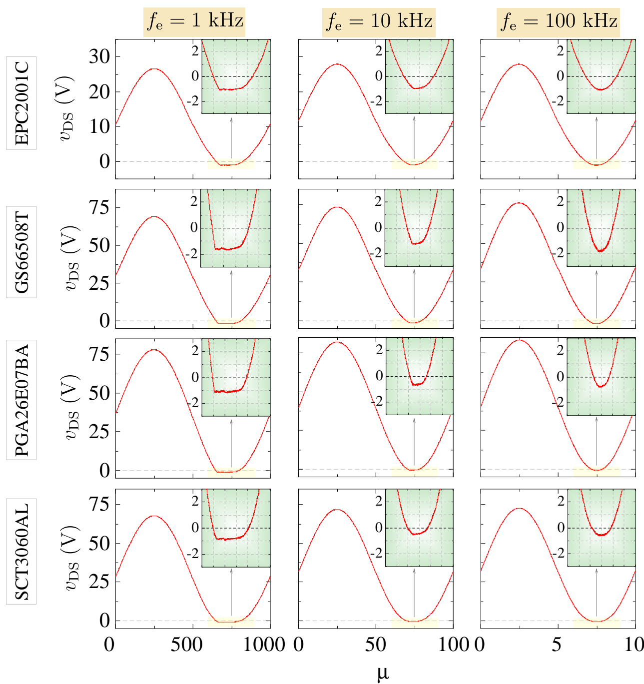

Fig. 11. Experimental waveforms of v_{DS} showing steady-state reverse conduction for DUTs: GaN HEMTs; EPC2001C, GS66508T, PGA26E07BA; and SiC device SCT3060AL. Negative clipping of v_{DS} is clearly seen in all the cases for $f_{\mathrm{e}} = 1$ kHz and 10 kHz. C_{ref} of 1 nF was used.

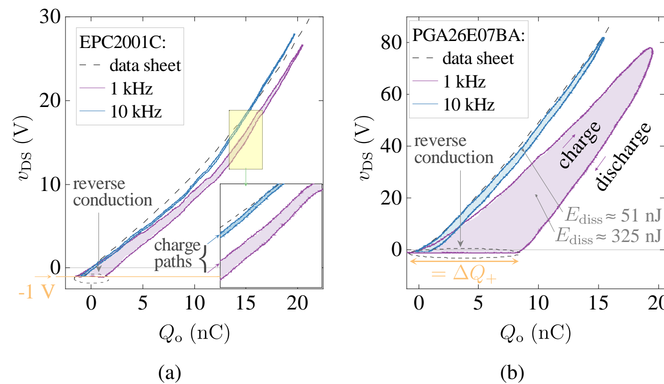

Fig. 12. Experimental v_{DS} vs Q_{o} curves for (a) EPC 2001C, and (b) PGA26E07BA transistors, showing hysteresis paths and E_{diss} losses that are not due to C_{o}, but due to an artefact of the steady-state reverse conduction of the DUT. For the PGA26E07BA device, at 10 kHz, this creates an E_{diss} loss of 51 nJ, while it increases up to 325 nJ at 1 kHz.

Applying (13) for the negative peak of v_{IN}, and substituting V_{BIAS} from (12), we get $v_{\mathrm{DS}} = -V_{\mathrm{FW}}$. This shows that the reverse conduction is inhibited as long as $v_{\mathrm{DS}} \geq -V_{\mathrm{FW}}$.

However, clipping of v_{DS} at $-V_{\mathrm{FW}}$ level was experimentally observed, indicating steady-state reverse conduction of the DUT. This effect is shown in Fig. 11 for several transistors. The three GaN HEMTs show clipped v_{DS} values of -1.1 V, -1.8 V and -1.2 V respectively for $f_{\mathrm{e}} = 1$ kHz, while the SiC device shows clipping at -0.9 V. The clipping period increases with decreasing f_{e} as seen in Fig. 11 for $f_{\mathrm{e}} = 1$ and 10 kHz.

The effect of steady-state reverse conduction on the Sawyer–Tower technique can be directly observed in Fig. 12, that shows the resulting v_{DS} vs Q_{o} curves. For both transistors, Q_{o} curves show a flat region at the bottom of the discharge path, that proves that C_{o} stops discharging and the DUT starts to conduct in reverse mode. During this period the assumption $Q_{\mathrm{o}} \propto C_{\mathrm{ref}} \cdot v_{\mathrm{ref}}$ is no longer valid, leading to false conclusions on existence of hysteresis for Q_{o}. For example, for the GaN device in Fig. 12b, an E_{diss} of 51 nJ is observed at 10 kHz. It increases up to a significant 325 nJ at 1 kHz, where the underlying reasons are discussed in Section V-C. These losses should not be considered as due to C_{o}.

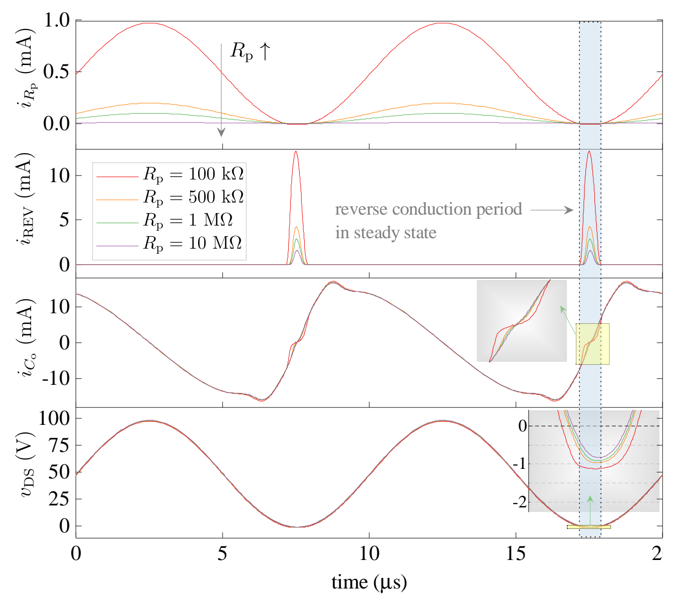

Fig. 13. *LTspice* simulation results showing the effect of device leakage (by changing R_{p}) on creating a reverse conduction period in steady state, in the Sawyer–Tower circuit. v_{DS} clipping at -1.2 V shows clear reverse conduction. The DUT consists of an EPC 2001C device model and an external resistance R_{p}, placed across the device's drain and source, to create different leakage levels. $f_{\mathrm{e}} = 100$ kHz, $v_{\mathrm{A}} = \pm 50$ V, $C_{\mathrm{ref}} = 47$ nF and $R_{\mathrm{o}} = 50\ \Omega$.

This reverse conduction happens because C_{ref} accumulates some positive dc charge, ΔQ_{+}, that results in a slight positive addition to its steady-state dc bias. The new bias can be written as $V_{\mathrm{BIAS}} + \Delta Q_{+} \cdot C_{\mathrm{ref}}$, which results in $v_{\mathrm{DS}} = -V_{\mathrm{FW}} - \Delta Q_{+} \cdot C_{\mathrm{ref}} < -V_{\mathrm{FW}}$, allowing reverse conduction to take place. The small reverse currents, indicated by the small reverse voltages, lead to the conclusion that the slight dc bias $\Delta Q_{+} \cdot C_{\mathrm{ref}}$ is related to the off-state drain–source leakage of the DUT.

To support this theory, a simulation was carried out in which the leakage was modelled by a resistance R_{p}, placed across the device's drain and source, as shown in Fig. 10b. Results for an EPC2001C device are shown in Fig. 13, where R_{p} is changed from 100 kΩ to 10 MΩ to model devices with high-leakage currents (1 mA) and low-leakage currents (50 μA). For low R_{p} values, the leakage current ($i_{\mathrm{LEAK}} = i_{R_{\mathrm{p}}}$) is large enough to cause a clipping of v_{DS} at -1.1 V, as shown in the zoomed inset. The reverse conduction is also confirmed by the flattening of C_{o} current, $i_{C_{\mathrm{o}}}$, during this period.

Therefore, the reverse conduction due to device leakage causes an additional DUT loss that could be misinterpreted as Q_{o} hysteresis loss, thus, compromising the use of the Sawyer–Tower technique. This problem can be mitigated by correctly choosing the range of f_{e} as discussed in Section V-C.

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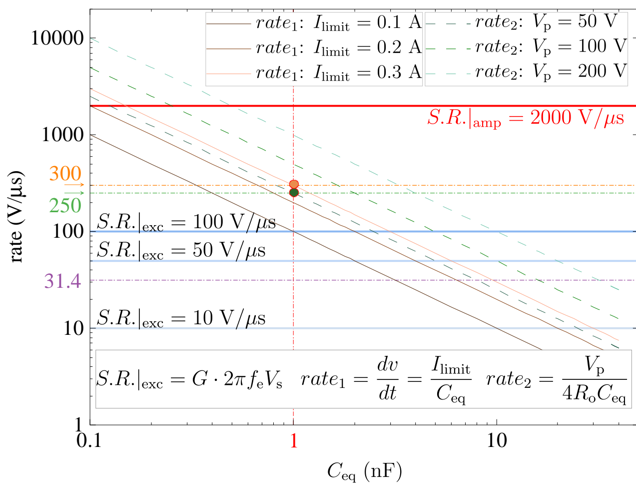

Fig. 14. Variation of $rate_1$ (in solid diagonal lines for different I_{limit}), and $rate_2$ (in dashed diagonal lines for different V_{p}, with R_{o} fixed at 50 Ω) with C_{eq}. Solid blue lines show practical $S.R.|_{\text{exc}}$ values while the solid red line shows $S.R.|_{\text{amp}}$ for WMA-300 amplifier.

V. Discussion and Design Recommendations

A. Voltage Amplifier Selection and Slew-Rate Limitations

For the correct implementation of the Sawyer–Tower circuit, the amplifier slew-rate should satisfy (3). At the same time, the circuit parameters should be chosen such that the dominant load slew-rate, $S.R.|_{\text{dominant}}$, is higher than $S.R.|_{\text{exc}}$.

$$S.R.|_{\text{exc}} < S.R.|_{\text{dominant}} < S.R.|_{\text{amp}} \tag{14}$$

Fig. 14 provides a quick reference chart to evaluate whether the circuit satisfies the slew-rate conditions of (14) for a given C_{eq} value. An example of a good selection is given for an EPC2001C transistor, tested with a WMA-300 amplifier of $S.R.|_{\text{amp}} = 2000$ V/μs and $I_{\text{limit}} = 300$ mA, shown as solid red and orange lines in Fig. 14, respectively: consider a sinusoidal excitation of $f_{\text{e}} = 100$ kHz, $V_{\text{s}} = 1$ V, $G = 50$, $R_{\text{o}} = 50$ Ω, and $C_{\text{ref}} = 47$ nF. Then $S.R.|_{\text{exc}}$ is calculated to be 31.4 V/μs $< S.R.|_{\text{amp}}$. According to Fig. 5a, C_{eq} in the low v_{DS} range is 1 nF. Then, $rate_1$ and $rate_2$ are calculated as 300 and 250 V/μs, respectively (equations given in Fig. 14). Thus, $S.R.|_{\text{dominant}} =$ 250 V/μs , and thus, (14) is satisfied. On the other hand, if f_{e} is increased to 1 MHz, with everything else unchanged, then $S.R.|_{\text{exc}} = 314$ V/μs, and (14) is no longer satisfied.

B. Selection of C_{ref}

A map of possible selections for C_{ref}, based on (10), for a given V_{p} is shown in Fig. 15. Four different families of curves for V_{p} are chosen between 50–300 V. Additionally, five $Q_{\text{o-max}}$ values between 5–120 nC are considered, that corresponds to commercial MOSFETs and GaN HEMTs. For instance, consider $V_{\text{p}} = 100$ V and a 50 % voltage swing across a DUT with $Q_{\text{o-max}} = 50$ nC at $V_{\text{DS-max}} = 100$ V (marked with a red circle): the optimum C_{ref} is then calculated as 500 pF (assume $V_{\text{FW}} \approx 0$).

For a given C0G/NP0 MLC capacitor, f_{e} should be chosen in the flat part of the C vs f_{e} curve (see Fig. 9). This range

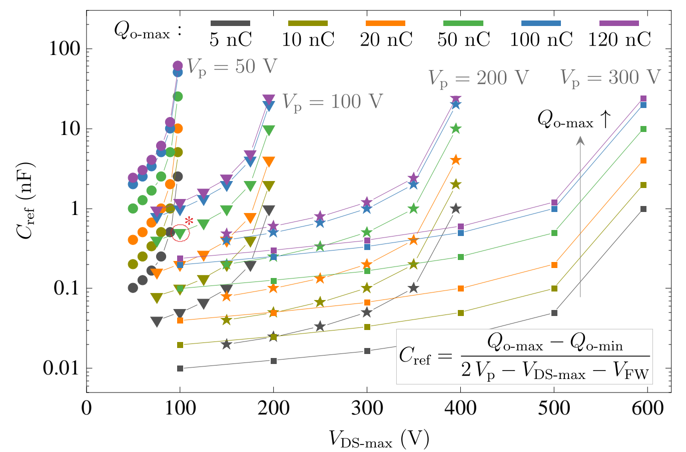

Fig. 15. Selection chart of C_{ref} value for a required $V_{\text{DS-max}}$ based on the input voltage range V_{p} and device's $Q_{\text{o-max}}$. $Q_{\text{o-min}} \approx 0$ for practical cases.

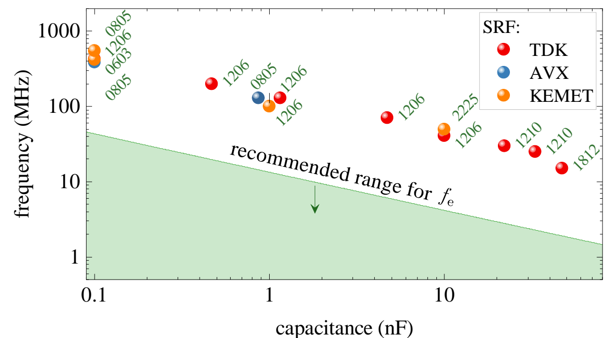

Fig. 16. Self resonant frequency (solid dots) vs capacitance for commercial C0G/NP0 MLC capacitors (500/630 V): green labels indicate the package.

normally extends up to SRF/10. The acceptable range of f_{e} values for a selection of commercial capacitors is shown in Fig. 16.

C. Minimizing Steady-State Reverse Conduction of the DUT

To minimize the effects of the steady-state reverse conduction, f_{e} should be chosen such that the resulting extra positive dc charge, ΔQ_+, due to leakage is at least two orders of magnitudes lower compared to the device's reported Q_{o} range to have an error less than 1 %.

For the worst case, where the leakage current is at maximum, $I_{\text{LEAK-max}}$, the charge ΔQ_+ is written as in (15), where $T_{\text{e}} = 1/f_{\text{e}}$, and T_{rev} is the duration of the reverse conduction.

$$\Delta Q_+ = I_{\text{LEAK-max}} \cdot (T_{\text{e}} - T_{\text{rev}}) \tag{15}$$

For all practical purposes, we can assume $T_{\text{e}} \gg T_{\text{rev}}$, and thus,

$$\Delta Q_+ \propto \frac{I_{\text{LEAK-max}}}{f_{\text{e}}}. \tag{16}$$

This reveals that ΔQ_+ increases with decreasing f_{e}. For low f_{e}, ΔQ_+ becomes comparable to devices' Q_{o} values and could cause significant errors in estimated Q_{o}. This is illustrated in Fig. 17, where $\Delta Q_+ \approx I_{\text{LEAK-max}}/f_{\text{e}}$ is used with practical device leakage currents. For example, if a device with $I_{\text{LEAK-max}} = 100$ μA is subjected to a Q_{o} swing of 100 nC (dashed orange line), the error changes from 1% to 10% when f_{e} changes from 100 kHz to 10 kHz (marked with red circles).

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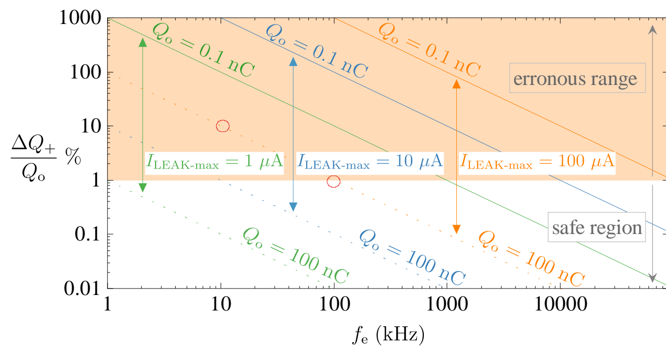

Fig. 17. The variation of the ratio between ΔQ_+ and device Q_o values, with f_e. For each case of $I_{\text{LEAK-max}}$, the dashed and solid lines correspond to a change of Q_o from 100 to 0.1 nC, respectively.

VI. Conclusions

A detailed analysis of the Sawyer–Tower circuit is presented highlighting key design factors. A new equation for the charge-voltage curve variation is introduced. A complete treatment on the selection of the reference capacitor was presented with design recommendations, with a new equation to correctly select its value for a given operating condition. A clear steady-state reverse conduction was proved for the Sawyer–Tower technique, highlighting its adverse effects on the technique and results. We showed that this effect can be minimized by choosing the excitation frequency such that the leakage-related build-up charge is at least two orders of magnitudes lower compared to device's Q_o.

The importance of fully identifying the validity of the measurement methods, and the corresponding mathematical estimation techniques, used in characterizing/modelling the C_o (or Q_o) behaviour and related losses should be emphasized. Ongoing work focuses on the following: 1) effects of the excitation type on the behaviour of large-signal C_o and related losses; 2) circuit-level representations for C_o of different device structures to model the reported large-signal losses.

Acknowledgment

The authors would like to thank Pietro Bianco from Linktronix AG for his kind technical advice and support.

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This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JESTPE.2020.2992946, IEEE Journal of Emerging and Selected Topics in Power Electronics

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