This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2020.2990628, IEEE Transactions on Power Electronics

Comparison of Wide-band-gap Technologies for Soft-Switching Losses at High Frequencies

Armin Jafari, Mohammad Samizadeh Nikoo, *Member*, *IEEE*, Nirmana Perera, *Student Member*, *IEEE*, Halil Kerim Yildirim, Furkan Karakaya, Reza Soleimanzadeh and Elison Matioli, *Member*, *IEEE*

***Abstract*—Soft-switching power converters based on wide-band-gap (WBG) transistors offer superior efficiency and power density advantages. However, at high frequencies, loss behavior varies significantly between different WBG technologies. This includes losses related to conduction and dynamic ON-resistance ($R_{DS(ON)}$) degradation, also charging/discharging of input capacitance (C_{ISS}) and output capacitance (C_{OSS}). As datasheets lack such important information, we present measurement techniques and evaluation methods for soft-switching losses in WBG transistors which enable a detailed loss-breakdown analysis. We estimate the gate loss under soft-switching conditions using a simple small-signal measurement. Next, we use Sawyer-Tower (ST) and Nonlinear Resonance (NR) methods to measure large-signal C_{OSS} energy losses up to 40 MHz. Finally, we investigate the dependence of dynamic $R_{DS(ON)}$ degradation on OFF-state voltage using pulsed-IV measurements. We demonstrate an insightful comparison of soft-switching losses for various normally-OFF Gallium-Nitride (GaN) and Silicon-Carbide (SiC) devices. A p-GaN-gated device exhibits the most severe $R_{DS(ON)}$ degradation and the lowest gate loss. Cascode arrangement increases threshold voltage for GaN devices and reduces gate losses in SiC transistors; however, it leads to higher C_{OSS} losses. The study facilitates the evaluation of system losses and selection of efficient WBG devices based on the trade-offs between various sources of losses at high frequencies.**

***Index Terms*—Soft-switching, GaN, SiC, WBG technology, gate loss, output capacitance loss, C_{OSS}, dynamic $R_{DS(ON)}$ degradation, Sawyer-Tower, nonlinear resonance, Cascode, GIT.**

I. Introduction

THE reduced input capacitance (C_{ISS}) and ON Resistance ($R_{DS(ON)}$) in wide-band-gap (WBG) transistors enable their efficient operation at high frequencies [1], [2], for instance, high-power-density dc-dc conversion [3]–[6], wireless power transfer and radio-frequency amplification [7], [8]. At such frequencies, soft-switched topologies, especially those designed for zero-voltage switching (ZVS), can potentially achieve high efficiencies [5], [9]–[11]. To that end, low levels of electromagnetic interference (EMI) and proper design of passive components, especially the magnetics, become crucial [5], [12], [13]. Furthermore, conduction losses (P_{CON}), Output-capacitance (C_{OSS}) losses (P_O) and gate losses (P_G) reduce the system efficiency and expose the devices to thermal runaway [1], [14]–[17]. Hence, it is important to adhere to accurate methods to extract these losses in different device technologies such as Gallium Nitride (GaN) and Silicon Carbide (SiC).

The authors are with the Power and Wide-band-gap Electronics Research Laboratory (POWERlab), École polytechnique fédérale de Lausanne (EPFL), CH-1015 Lausanne, Switzerland This work was supported in part by the Swiss Office of Energy under Grant SI/501887-01 (MEPCO). (Corresponding author: Armin Jafari, email: armin.jafari@epfl.ch).

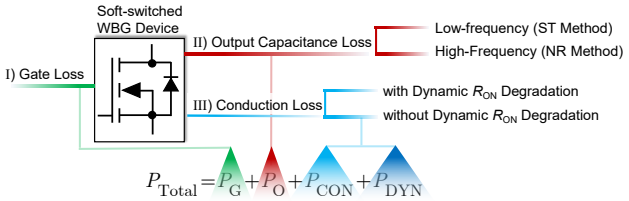

Fig. 1. Major sources of loss in a soft-switched WBG device. Various WBG technologies exhibit significantly different loss behaviors, that are comprehensively analyzed in this letter.

In this letter we demonstrate straightforward measurement methods to compare and break down soft-switching losses in various WBG technologies, as illustrated in Fig. 1. Commercial devices with similar current and voltage ratings (see TABLE I) are compared and their various losses are evaluated up to 40 MHz.

One of the main challenges in loss estimation is the lack of sufficient information from manufacturer datasheets to determine the soft-switching behavior of the devices at high frequencies. For instance, standard methods used in datasheets to report gate-charge (Q_G) are based on hard-switching tests, and using those values for soft-switched transistors may result in large errors in high frequencies [17]–[19]. In Section II, we demonstrate a simple method based on small-signal C_{ISS} measurement to evaluate gate losses and further verify its accuracy with large-signal power measurements.

In Section III, we measure the non-recoverable energy loss due to charging and discharging of the output capacitance of a transistor, which is a major source of loss at high frequencies [1], [14], [20], [21]. In [14], a thermal approach is used to study soft-switching output capacitance losses. However, the existence of additional loss mechanisms and voltage oscillations could significantly limit the method's applicability for high dv/dt values. Sawyer-Tower (ST) circuit employs a power amplifier and a reference capacitor to extract the large-signal charge-versus-voltage curve of C_{OSS}. The related energy loss is extracted by calculating the area of the hysteresis between charging and discharging curves [22]. Despite the simplicity of the ST method, the limited bandwidth of the power amplifier and the risk of device thermal runaway hinder its application in high frequencies and high dv/dt conditions [14], [16]. Measurement of large-signal C_{OSS} losses based on the nonlinear resonance (NR) between the transistor C_{OSS} and a high-quality-factor inductor has been proposed to overcome the aforementioned shortcomings [16]. The NR method can extract P_O for large voltages and dv/dt values as high as 100 V/ns, which are achievable with WBG power transistors [23]. Here, we employ the ST method to extract P_O at low frequencies (<1 MHz) and the NR method to evaluate those losses for higher

"© 2020 IEEE. Personal use of this material is permitted. Permission from IEEE must be obtained for all other uses, in any current or future media, including reprinting/republishing this material for advertising or promotional purposes, creating new collective works, for resale or redistribution to servers or lists, or reuse of any copyrighted component of this work in other works."

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2020.2990628, IEEE Transactions on Power Electronics

TABLE I
CHARACTERISTICS OF THE EVALUATED TRANSISTORS

ID	Part Number (Technology)	V_{BR} (V)	I_D (A)	Q_G (nC)	$R_{DS(ON)}$* (mΩ)	C_{OSS}** (pF)
T_1	GS66508T (p-GaN-gated)	650	30	5.8	50	65
T_2	PGA26E07BA (GaN GIT)	600	31	5	56	71
T_3	TP65H050WS (GaN Cascode)	650	36	16	50	130
T_4	SCT3060AL (SiC)	650	39	58	60	85
T_5	MSC060SMA070S (SiC)	700	37	56	60	138
T_6	UF3C065080K3S (SiC Cascode)	650	31	51	80	62

* Typical value at 25°C ** Reported at 400 V

frequencies (up to 40 MHz).

In Section IV, we compare the dynamic $R_{DS(ON)}$ degradation in WBG transistors. Dynamic $R_{DS(ON)}$ degradation leads to higher resistance values immediately after a turn-ON transition [15], [24]. In [15], large discrepancies between the reported values of dynamic $R_{DS(ON)}$ in the literature are attributed to the standard double-pulse test (DPT) method. Here, we employ pulsed-IV measurements to evaluate of the dynamic $R_{DS(ON)}$ degradation as a function of the OFF-state voltage amplitude. The OFF-state voltage could be regarded as the most impactful parameter in dynamic $R_{DS(ON)}$ degradation [2]. A discussion in Section V summarizes total loss breakdown from 100 kHz up to 5 MHz for the evaluated transistors, which is of key importance for the selection of WBG switches for high frequency applications.

II. GATE LOSS

By modeling the gate as C_{ISS} in series with a gate resistance and a gate driver resistance, for push-pull gate drivers (i.e. hard gating), P_G is equal to the total energy used to charge C_{ISS} from V_{OFF} to V_{ON}, multiplied by f_{SW} as

$$P_G = Q_G(V_{ON} - V_{OFF})f_{SW} \quad (1)$$

where Q_G for soft-switched transistors can be formulated as

$$Q_G = \int_{V_{OFF}}^{V_{ON}} C_{ISS}(v)dv \quad (2).$$

C_{ISS} in (2) is the small-signal capacitance measured versus voltage using an impedance analyzer, when the drain is shorted to the source, to emulate ZVS condition. The reported Q_G in datasheets is measured as the device is subjected to a hard turn ON, and does not represent a soft-switching operation [18], [19]. In Fig. 2a, C_{ISS} is measured at 1 MHz using an E4990A impedance analyzer and a 16047E test fixture, where the shaded areas under C_{ISS}-versus-V_{GS} curves represent the soft-switching Q_G. T_2 is a gate-injection transistor (GIT) whose gate presents capacitive behavior at low drive voltages and behaves as a diode with an ON-state current at higher voltages. To verify the small-signal prediction of gate losses based on (1), we operated the transistors from 100 kHz up to 5 MHz (at 50% duty cycle) with the drain shorted to the source. Fig. 2b presents the time-domain gate-to-source voltages (v_{GS}) at 5 MHz. The real P_G was

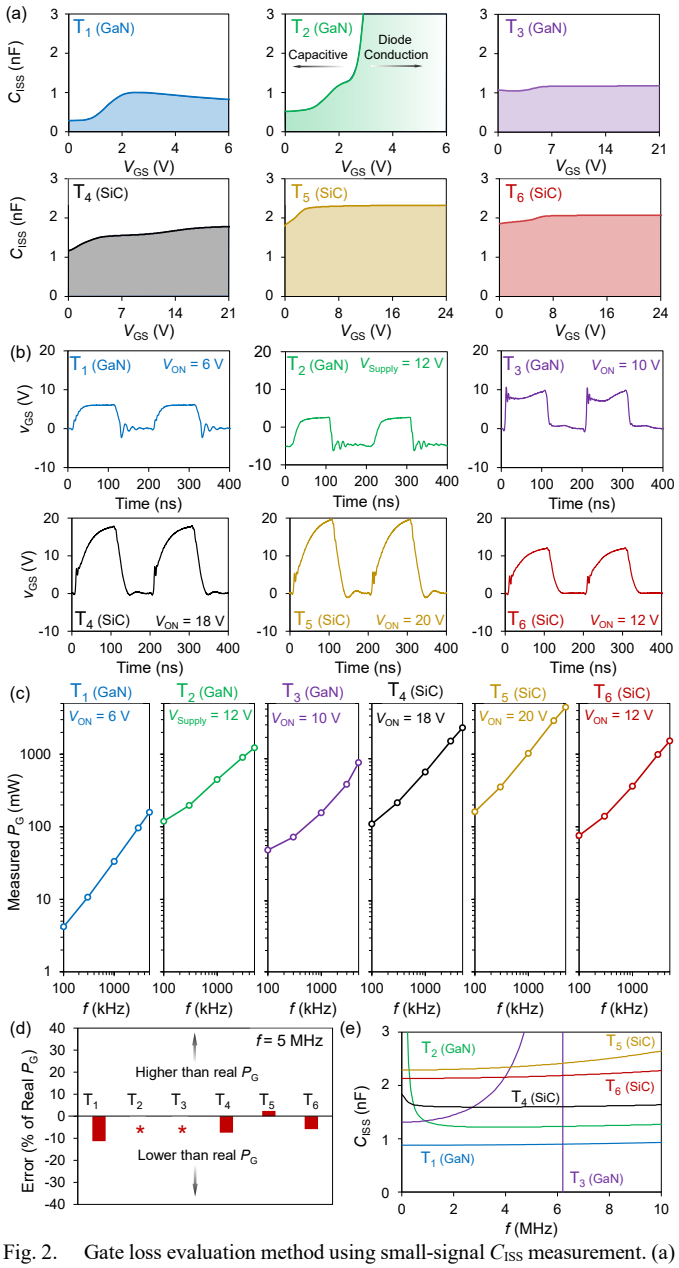

Fig. 2. Gate loss evaluation method using small-signal C_{ISS} measurement. (a) Small-signal C_{ISS} versus V_{GS} for T_1 to T_6 measured at 1 MHz. The gate in most of the transistors can be regarded as an RC circuit. Device T_2 exhibits a capacitive behavior for low drive voltages and as the voltage increases, it performs similarly to a diode with an ON-state current, as indicated by the gradient shading under its C_{ISS}-versus-V_{GS} curve. (b) Time-domain gate-to-source voltages for T_1 to T_6, driven at 5 MHz with nominal gate conditions. (c) Measurement of real P_G versus f from 100 kHz to 5 MHz at nominal gate-driver conditions. (d) The error of using the small-signal Q_G from (2) for P_G evaluation at 5 MHz. The proposed method shows a consistent error of less than 10%. Symbol '*' indicates that the proposed method is not applicable to T_2 and T_3 as their gates cannot be modeled with RC circuits. (e) The frequency dependence of C_{ISS}. T_2 and T_3 devices exhibit a strong variation in C_{ISS}, suggesting that their gate cannot be modeled as RC circuits. T_3 shows a resonance at about 6.5 MHz.

extracted from the cross product of the measured current and voltage of the gate-driver supply (see Fig. 2c). For T_2, a constant current-source driver (AN34092B) recommended by the T_2 manufacturer was used. To drive other transistors, we employed a wide-voltage-range gate driver (SI8271). Fig. 2d presents the error of using Q_G from (2) for P_G evaluation with respect to the

"© 2020 IEEE. Personal use of this material is permitted. Permission from IEEE must be obtained for all other uses, in any current or future media, including reprinting/republishing this material for advertising or promotional purposes, creating new collective works, for resale or redistribution to servers or lists, or reuse of any copyrighted component of this work in other works."

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2020.2990628, IEEE Transactions on Power Electronics

real measured gate losses at 5 MHz. A consistent error of less than 10% was observed for transistors T_1, T_4, T_5 and T_6, whose gates can be modeled as RC circuits. T_2 and T_3 exhibited a frequency-dependent C_{ISS}, as shown in Fig. 2e. The excessive increase of C_{ISS} with V_{GS} in T_2 at higher driving voltages (see Fig. 2a) and the resonance observed at about 6.5 MHz for T_3 suggest that their gates cannot be modeled simply as RC circuits. Hence, the evaluation method is not applicable and one needs a direct loss measurement, as presented in Fig. 2c. T_1 exhibited the smallest P_G and is best suited for very-high-frequency (VHF) operation. The demonstrated method based on C_{ISS}-versus-V_{GS} measurement provides invaluable information for gate loss estimations with low errors in soft-switched transistors. Since the use of the standard gate-charge information in typical datasheets correspond to a hard-switching test and can result in large errors, it is extremely important to include the C_{ISS}-versus-V_{GS} measurement in manufacturer datasheets, especially those of WBG devices.

III. Output-Capacitance Loss

Charging and discharging of C_{OSS} could lead to excessive energy loss in WBG transistors [14], [20], [21]. The overall large-signal C_{OSS} loss can be formulated as

$$P_O = fE_{DISS} \quad (3)$$

where f is the switching frequency and E_{DISS} represents the energy dissipated in each charging/discharging cycle of the C_{OSS}. To measure E_{DISS} over a wide frequency range, we employed a combination of ST and NR methods [16], [22]. For ST experiment, we used a Keysight 33600A function generator, a WMA-300 amplifier and a high-frequency step-up transformer to generate a 400-V peak-to-peak voltage over the device under test (DUT) with its gate shorted to the source, as shown in Fig. 3a. A test board with the DUT in series with high-quality-factor inductors (i.e. quality factors greater than 100 at the test frequencies) were used to evaluate the losses at higher frequencies based on the NR method, as presented in Fig. 3b. Fig. 3c shows V_{DS}-versus-Q curves corresponding to charging and discharging of C_{OSS} measured using the ST method at 100 kHz. The larger the deviation between the charging and discharging curves, the higher E_{DISS}. Fig. 3d illustrates the time-domain v_{DS} waveforms at two very different test frequencies, measured using NR method. The dashed curve is the mirrored rising half of the v_{DS}. The higher deviation between the mirrored curve and the real v_{DS} in the falling half indicates a larger E_{DISS}, which could be extracted as [16]

$$E_{DISS} = \frac{1}{2L}\left(\left(\int_{t_0}^{t_1} v_{DS}(t)dt\right)^2 - \left(\int_{t_1}^{t_2} v_{DS}(t)dt\right)^2\right) \quad (4).$$

In this expression, L is the inductance in series with the DUT and intervals (t_0, t_1) and (t_1, t_2) correspond to the charging and discharging of the C_{OSS}, respectively. By applying the two methods, we measured E_{DISS} over a wide frequency range from 100 kHz up to 40 MHz, as illustrated in Fig. 3e. The ST results correspond to the measurements for $f < 1$ MHz and the NR method was employed for measurements above 1 MHz.

GaN device T_1 exhibited an exponential increase of E_{DISS}, with negligible energy losses at low frequencies. E_{DISS} values

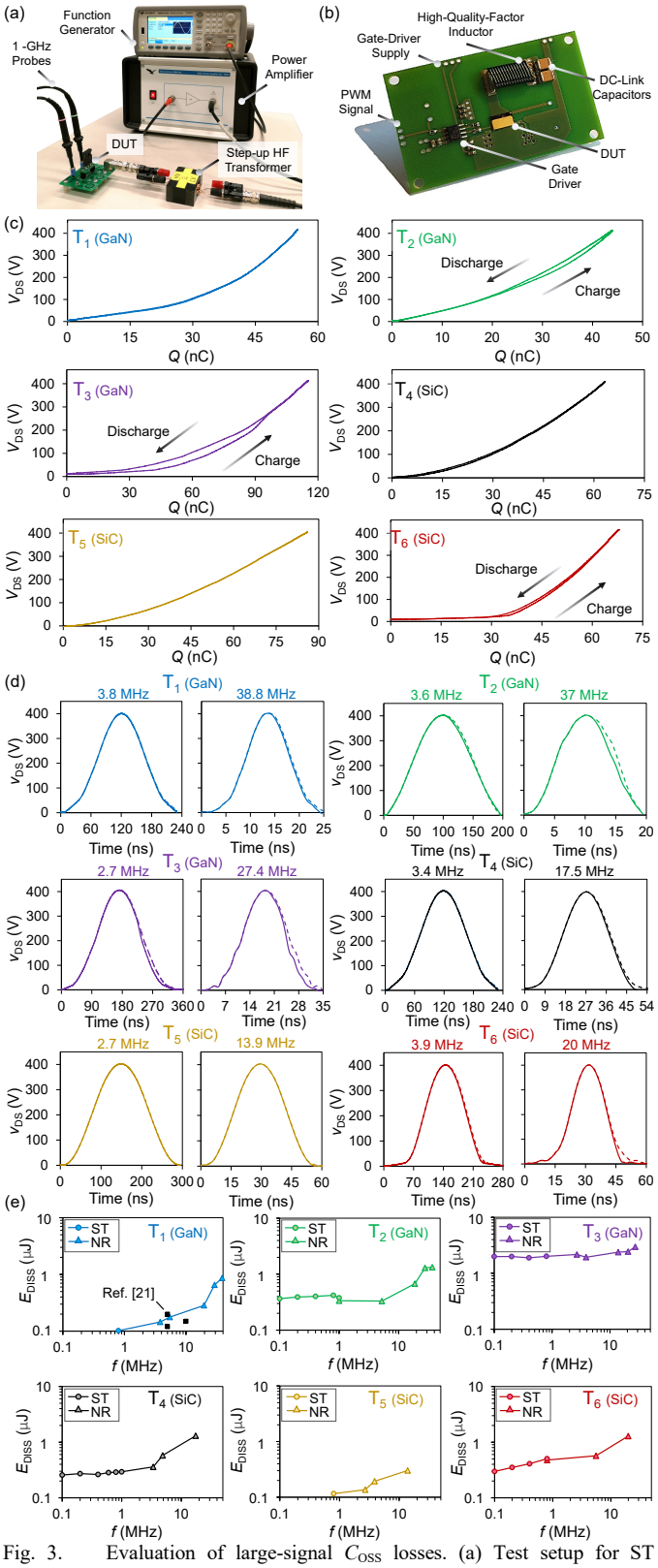

Fig. 3. Evaluation of large-signal C_{OSS} losses. (a) Test setup for ST experiment comprised of a DUT, a high-frequency step-up transformer, a WMA-300 power amplifier and a 33600A function generator. (b) NR test board including a gate drive and a high-quality-factor inductor in series with the DUT. (c) V_{DS}-versus-Q results based on ST measurement for T_1 to T_6 at 100 kHz and 400 V. (d) Time-domain v_{DS} for T_1 to T_6 using NR method at two distant frequencies. The dashed curves are the mirrored of the rising half of the generated pulse. A higher deviation from the solid curve indicates higher E_{DISS}. (e) E_{DISS} versus frequency for T_1 to T_6 measured using ST ($f < 1$ MHz) and NR ($f > 1$ MHz) methods.

"© 2020 IEEE. Personal use of this material is permitted. Permission from IEEE must be obtained for all other uses, in any current or future media, including reprinting/republishing this material for advertising or promotional purposes, creating new collective works, for resale or redistribution to servers or lists, or reuse of any copyrighted component of this work in other works."

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2020.2990628, IEEE Transactions on Power Electronics

from [21] are also presented in Fig. 3e for transistor T_1 for different packages at 5 and 10 MHz. Despite the exponential increase of E_{DISS} in T_1 and T_2 (for T_2, the trend starts after about 5 MHz), the cascode device T_3 has large E_{DISS} values at low frequencies which tend to increase slightly at higher frequencies. Datasheets provide C_{OSS} stored energy (E_{OSS}) which could be useful for evaluation of hard-switching losses; however, E_{DISS} information for soft-switching applications is missing. Hence, the presented results are of great significance for soft-switched VHF designs based on WBG technology and in specific GaN-based applications where the devices can potentially switch at tens of MHz.

IV. Conduction Loss

Dynamic $R_{DS(ON)}$ in GaN devices is susceptible to degradation right after a turn-ON transition [15], [24], [25]. It leads to extra power dissipation referred here as dynamic losses (P_{DYN}). The OFF-state voltage has the highest impact on the dynamic $R_{DS(ON)}$ behavior of soft-switched GaN transistors [2]. To measure this dependency, we used the pulsed-IV system (AMCAD), where the DUT was subjected to V_{GS} (using gate-probe iTest AM213) and V_{DS} (using 1kV/30A drain-probe PIV AM241) excitations as shown in Fig. 4a, with a 5-µs ON time and 15-µs OFF time. Time-domain $R_{DS(ON)}$ measurements for the device T_1 are presented in Fig. 4b for V_{DS} = 0 V, 100 V and 400 V. To capture the actual $R_{DS(ON)}$ and minimize the effect of noise, we averaged the resistance values over a 1-µs interval, after the settling time of the measurement tool had reached (i.e. 2.5 µs after the device was turned ON, as indicated by the measurement windows in Figs. 4a, b). $R_{DS(ON)}$ was measured at

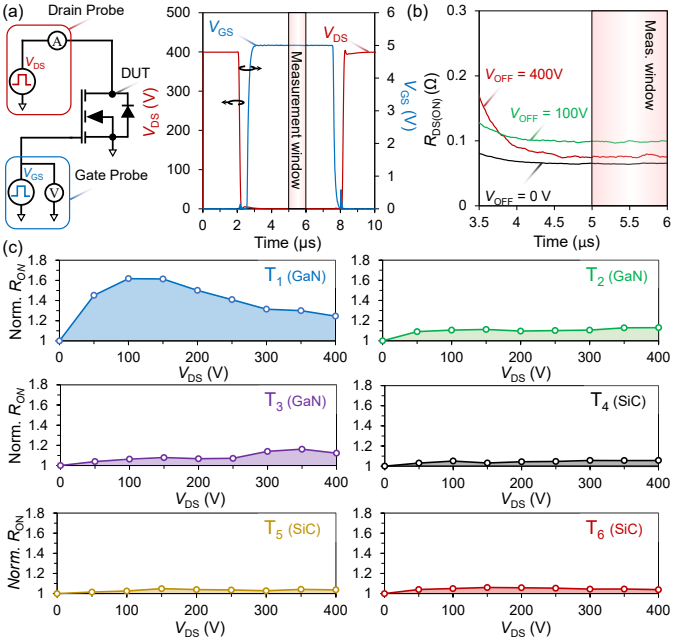

Fig. 4. Dynamic $R_{DS(ON)}$ measurement using pulsed-IV method. (a) The DUT is subjected to V_{GS} and V_{DS} pulses and the resistance was measured after the settling time of the setup was reached. (b) $R_{DS(ON)}$ variation for T_1 at OFF-state V_{DS} of 0 V (no voltage stress), 100 V and 400 V. (c) Normalized dynamic $R_{DS(ON)}$ at different V_{DS} values for transistors T_1 to T_6. $R_{DS(ON)}$-versus-V_{DS} pattern varies between GaN devices. SiC transistors exhibit a negligible increase of $R_{DS(ON)}$. Devices are subjected to 20% of their nominal current. $R_{DS(ON)}$ was captured 2.5 µs after the DUT turns ON, and was averaged over a 1-µs interval to reject noise.

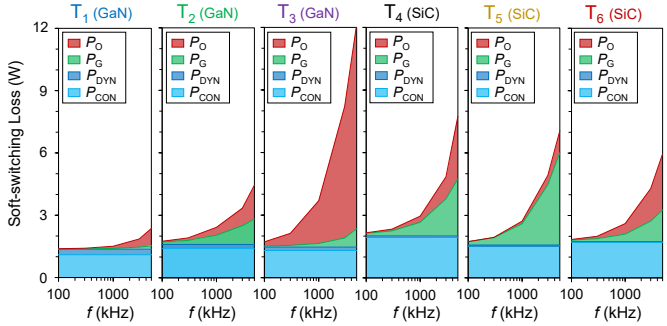

Fig. 5. Soft-switching loss components versus frequency for transistors T_1 to T_6 at nominal V_{GS} when transistors are subjected to a V_{DS} of 400 V and 20% of their nominal current. The comparison is of great significance for selection of WBG devices, efficiency optimization and proper design of cooling systems.

20% of the rated current (i.e. about 6 A). Fig. 4c shows the $R_{DS(ON)}$ normalized by its measured value at V_{DS} = 0. In T_1, we observed a degradation of 25% at 400 V, and even larger at lower voltages, whereas T_2 and T_3 exhibited lower degradations. $R_{DS(ON)}$ degradation was almost absent in SiC transistors T_4 to T_6.

V. Discussion

WBG field-effect transistors based on GaN and SiC enable fast switching speeds for high frequencies, where the elimination of switching losses, especially at turn-ON transients, becomes crucial [9], [23], [26]. Topologies such as phase-shifted full-bridge (PSFB) [12], dual-active-bridge (DAB) [5] and soft-switched boost converters [11] take advantage of ZVS for efficient high-frequency operation. The presented loss measurements in this letter emulate a ZVS operating condition, enabling a detailed comparison of the overall soft-switching losses. Fig. 5 summarizes the soft-switching losses of devices T_1 to T_6 up to 5 MHz, based on the loss breakdown described in Fig. 1. The devices were driven at their respective nominal gate voltages with 50% duty cycle and 20% of their rated currents at V_{DS} = 400 V. The loss due to conduction is divided into P_{CON} and P_{DYN}. P_{DYN} represents only the contribution of the dynamic $R_{DS(ON)}$ degradation, whereas P_{CON} considers the measured value of $R_{DS(ON)}$ at V_{DS} = 0. Although P_{DYN} in GaN devices increases with frequency, the variation is small and negligible within the presented frequency range in Fig. 5 [24], [25].

Fig. 5 illustrates that GaN device T_1 has the lowest overall losses. Despite exhibiting the most severe $R_{DS(ON)}$ degradation at 400 V (also see Fig. 4c), due to its low gate and output capacitance losses, T_1 is advantageous for VHF applications, especially those with low duty cycles or small currents. Relatively higher gate losses and special gate-drive circuitry impose limitations on high-frequency application of GaN transistors such as T_2, whose gate behaves similarly to a diode at large V_{GS} values. A cascode arrangement enables higher threshold voltage in T_3 (compared to GaN devices T_1 and T_2) and lower gate loss in T_6 (compared to SiC devices T_4 and T_5); however, higher output-capacitance losses are observed for these cascode devices, even at low frequencies. Besides, the observed gate resonance in T_3 (see Fig. 2e), together with its negative resistance behavior [27], could result in large-signal instabilities [28].

"© 2020 IEEE. Personal use of this material is permitted. Permission from IEEE must be obtained for all other uses, in any current or future media, including reprinting/republishing this material for advertising or promotional purposes, creating new collective works, for resale or redistribution to servers or lists, or reuse of any copyrighted component of this work in other works."

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2020.2990628, IEEE Transactions on Power Electronics

By combining the estimation methods and measurements presented in the previous sections, one could extend the loss evaluation to higher frequencies (even up to 40 MHz).

VI. Conclusion

We demonstrated a comprehensive loss-breakdown analysis for soft-switching operation of wide-band-gap transistors. A small-signal input-capacitance measurement versus gate-to-source voltage was used to evaluate gate losses under soft-switching conditions, and its accuracy was experimentally verified. By using a combination of ST method (for $f < 1$ MHz) and NR technique (for 1 MHz $< f <$ 40 MHz), we demonstrated the variation of large-signal C_{OSS} losses for different technologies over a wide range of frequency. To obtain an overall view of the losses, we further compared the degradation of dynamic $R_{DS(ON)}$ and its dependence on the OFF-state voltage using a standard pulsed-IV method. Three SiC and three GaN devices were evaluated and compared for their gate losses, output-capacitance losses and conduction losses up to 5 MHz. The most severe $R_{DS(ON)}$ degradation and the lowest gate losses were observed in a p-GaN-gated device (T_1), which is the best choice for VHF applications, especially those with low duty cycles or small currents. The cascode arrangement in SiC and GaN devices offers advantages such as increased threshold voltage and reduced gate loss. However, the output-capacitance losses are aggravated at high frequencies, which limit their high-frequency operation. The demonstrated measurement methods are general and can be used to evaluate the soft-switching losses in other WBG transistors. Given the diversity of WBG technologies, this work addresses the major trade-offs in selecting a power device to maximizing the system efficiency, and to choose a proper thermal design in high-frequency soft-switching applications. This work is also insightful for device engineers to design high-performance power transistors for high-frequency applications.

References

[1] G. Zulauf, Z. Tong, J. D. Plummer, and J. M. Rivas-Davila, "Active Power Device Selection in High- and Very-High-Frequency Power Converters," *IEEE Trans. Power Electron.*, vol. 34, no. 7, pp. 6818–6833, Jul. 2019, doi: 10.1109/TPEL.2018.2874420.

[2] J. Gareau, R. Hou, and A. Emadi, "Review of Loss Distribution, Analysis and Measurement Techniques for GaN HEMTs," *IEEE Trans. Power Electron.*, pp. 1–1, 2019, doi: 10.1109/TPEL.2019.2954819.

[3] C. Armbruster, A. Hensel, A. H. Wienhausen, and D. Kranzer, "Application of GaN power transistors in a 2.5 MHz LLC DC/DC converter for compact and efficient power conversion," in *2016 18th European Conference on Power Electronics and Applications (EPE'16 ECCE Europe)*, Karlsruhe, Sep. 2016, pp. 1–7, doi: 10.1109/EPE.2016.7695529.

[4] M.-J. Liu and S. S. H. Hsu, "A Miniature 300-MHz Resonant DC–DC Converter With GaN and CMOS Integrated in IPD Technology," *IEEE Trans. Power Electron.*, vol. 33, no. 11, pp. 9656–9668, Nov. 2018, doi: 10.1109/TPEL.2017.2788946.

[5] A. Jafari, M. Samizadeh Nikoo, F. Karakaya, and E. Matioli, "Enhanced DAB for Efficiency Preservation using Adjustable-Tap High-Frequency Transformer," *IEEE Trans. Power Electron.*, pp. 1–1, 2019, doi: 10.1109/TPEL.2019.2958632.

[6] C. Fei, F. C. Lee, and Q. Li, "High-efficiency high-power-density 380V/12V DC/DC converter with a novel matrix transformer," in *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Tampa, FL, USA, Mar. 2017, pp. 2428–2435, doi: 10.1109/APEC.2017.7931039.

[7] L. Jiang and D. Costinett, "A High-Efficiency GaN-Based Single-Stage 6.78 MHz Transmitter for Wireless Power Transfer Applications," *IEEE Trans. Power Electron.*, vol. 34, no. 8, pp. 7677–7692, Aug. 2019, doi: 10.1109/TPEL.2018.2879958.

[8] Jungwon Choi, D. Tsukiyama, Y. Tsuruda, and J. Rivas, "13.56 MHz 1.3 kW resonant converter with GaN FET for wireless power transfer," in *2015 IEEE Wireless Power Transfer Conference (WPTC)*, Boulder, CO, USA, May 2015, pp. 1–4, doi: 10.1109/WPT.2015.7140167.

[9] M. Kasper, R. Burkat, F. Deboy, and J. Kolar, "ZVS of Power MOSFETs Revisited," *IEEE Trans. Power Electron.*, pp. 1–1, 2016, doi: 10.1109/TPEL.2016.2574998.

[10] M. H. Rashid, *Power Electronics: Circuits, Devices and Applications (3rd Edition) by Muhammad H. Rashid*.

[11] M. Samizadeh Nikoo, A. Jafari, N. Perera, and E. Matioli, "Efficient High Step-up Operation in Boost Converters Based on Impulse Rectification," *IEEE Trans. Power Electron.*, pp. 1–1, 2020, doi: 10.1109/TPEL.2020.2982931.

[12] A. Jafari and E. Matioli, "High Step-Up High-Frequency Zero-Voltage Switched GaN-Based Single-Stage Isolated DC-DC Converter for PV Integration and Future DC Grids," PCIM Europe 2018; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, Nuremberg, Germany, 2018, pp. 1-6.

[13] M. S. Sanjari Nia, P. Shamsi, and M. Ferdowsi, "Investigation of Various Transformer Topologies for HF Isolation Applications," *IEEE Trans. Plasma Sci.*, vol. 48, no. 2, pp. 512–521, Feb. 2020, doi: 10.1109/TPS.2020.2967412.

[14] M. Guacci *et al.*, "On the Origin of the Coss-Losses in Soft-Switching GaN-on-Si Power HEMTs," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, pp. 1–1, 2018, doi: 10.1109/JESTPE.2018.2885442.

[15] G. Zulauf, M. Guacci, and J. W. Kolar, "Dynamic On-Resistance in GaN-on-Si HEMTs: Origins, Dependencies, and Future Characterization Frameworks," *IEEE Trans. Power Electron.*, pp. 1–1, 2019, doi: 10.1109/TPEL.2019.2955656.

[16] M. Samizadeh Nikoo, A. Jafari, N. Perera, and E. Matioli, "Measurement of Large-Signal C_{OSS} and C_{OSS} Losses of Transistors Based on Nonlinear Resonance," *IEEE Trans. Power Electron.*, pp. 1–1, 2019, doi: 10.1109/TPEL.2019.2938922.

[17] Y. Chen, F. C. Lee, L. Amoroso, and H.-P. Wu, "A Resonant MOSFET Gate Driver With Efficient Energy Recovery," *IEEE Trans. Power Electron.*, vol. 19, no. 2, pp. 470–477, Mar. 2004, doi: 10.1109/TPEL.2003.823206.

[18] "Measuring MOSFET Gate Charge with the 4200A-SCS Parameter Analyzer." Tektronix Application Note.

[19] "MOSFET Gate-Charge Origin and its Applications (AND9083/D)." ON Semiconductor, Feb. 2016.

[20] M. Samizadeh Nikoo, A. Jafari, N. Perera, and E. Matioli, "New Insights on Output Capacitance Losses in Wide-Band-Gap Transistors," *IEEE Trans. Power Electron.*, vol. 35, no. 7, pp. 6663–6667, Jul. 2020, doi: 10.1109/TPEL.2019.2958000.

[21] G. Zulauf, S. Park, W. Liang, K. N. Surakitbovorn, and J. Rivas-Davila, "C_{OSS} Losses in 600 V GaN Power Semiconductors in Soft-Switched, High- and Very-High-Frequency Power Converters," *IEEE Trans. Power Electron.*, vol. 33, no. 12, pp. 10748–10763, Dec. 2018, doi: 10.1109/TPEL.2018.2800533.

[22] C. B. Sawyer and C. H. Tower, "Rochelle Salt as a Dielectric," *Phys. Rev.*, vol. 35, no. 3, pp. 269–273, Feb. 1930, doi: 10.1103/PhysRev.35.269.

[23] M. Samizadeh Nikoo, A. Jafari, N. Perera, M. Zhu, G. Santoruvo, and E. Matioli, "Nanoplasma-enabled picosecond switches for ultrafast electronics," *Nature*, vol. 579, no. 7800, pp. 534–539, Mar. 2020, doi: 10.1038/s41586-020-2118-y.

[24] D. Jin and J. A. del Alamo, "Methodology for the Study of Dynamic ON-Resistance in High-Voltage GaN Field-Effect Transistors," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3190–3196, Oct. 2013, doi: 10.1109/TED.2013.2274477.

[25] R. Li, X. Wu, S. Yang, and K. Sheng, "Dynamic ON-State Resistance Test and Evaluation of GaN Power Devices Under Hard- and Soft-Switching Conditions by Double and Multiple Pulses," *IEEE Trans. Power Electron.*, vol. 34, no. 2, pp. 1044–1053, Feb. 2019, doi: 10.1109/TPEL.2018.2844302.

[26] J. A. Anderson, C. Gammeter, L. Schrittwieser, and J. W. Kolar, "Accurate Calorimetric Switching Loss Measurement for 900 V 10 mΩ SiC mosfets," *IEEE Transactions on Power Electronics*, vol. 32, no. 12, pp. 8963–8968, Dec. 2017, doi: 10.1109/TPEL.2017.2701558.

[27] M. Samizadeh Nikoo, A. Jafari, N. Perera, and E. Matioli, "Negative Resistance in Cascode Transistors," *IEEE Trans. Power Electron.*, pp. 1–1, 2020, doi: 10.1109/TPEL.2020.2978658.

[28] X. Huang, W. Du, F. C. Lee, Q. Li, and W. Zhang, "Avoiding Divergent Oscillation of a Cascode GaN Device Under High-Current Turn-Off Condition," *IEEE Trans. Power Electron.*, vol. 32, no. 1, pp. 593–601, Jan. 2017, doi: 10.1109/TPEL.2016.2532799.

"© 2020 IEEE. Personal use of this material is permitted. Permission from IEEE must be obtained for all other uses, in any current or future media, including reprinting/republishing this material for advertising or promotional purposes, creating new collective works, for resale or redistribution to servers or lists, or reuse of any copyrighted component of this work in other works."