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Design Optimization of Two-Quadrant High-Current Low-Voltage Power Supply

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***Abstract*—The high-current delivered by a dedicated power supply is the *condicio sine qua non* to obtain the strong magnetic field produced by superconducting magnets. The end goal of such power supply is to control the current, very precisely, across this distinctive kind of load. To this extent, the topology and a specific mode of operation that fit the requirements is analysed and presented in this paper. To obtain a contemporary power supply design, a design optimisation of the overall system with respect to efficiency and volume is carried out. Considering the modularity specification, the system is split into elementary building blocks and one optimally designed unit is practically implemented and verified against predictions from the design tool. In sum, this paper provides the comprehensive design process for a modern 2-quadrant high-current low-voltage DC/DC power supply.**

***Index Terms*—Power supply, DC/DC, high-current, low-voltage, design optimisation, prototype.**

I. Introduction

FEEDING the most cutting-edge superconducting magnets requires equally modern and optimised power supplies. As the magnetic field intensity and requirements for such magnets becomes more and more advanced, the superconducting magnet power supply that feed them with the adequate current should be improved as well. One of key aspect is for the power supply to gain in efficiency and current accuracy.

The case study of this paper relates to European Organisation for Nuclear Research (CERN), and a particular set of new focusing superconducting magnets. By their nature itself, those magnets can reach very large magnetic field and have zero resistivity, lowering the voltage needs of the power supply. The improved focusing magnets are designed to produce a high magnetic field in order to increase the performances of the Large Hadron Collider (LHC) [1], [2] within the frame of the High Luminosity LHC (HL-LHC) project [3]–[6].

In the CERN's existing installation, the superconducting magnet power supply has an output characteristics which is only 1-quadrant. This is a viable solution when the equivalent resistance of the cables connecting the power supply to the load is significant enough to dissipate the energy during the demagnetisation phase. In the new installation, the global layout of the power circuit reduces the length of copper cable between the power supply and superconducting interface to its minimum. The equivalent resistance provided by the shorter cables is not sufficient anymore to keep the 1-quadrant operation, because the procedure requires a demagnetisation of the load in a well defined duration. In order to ramp down the current in the superconducting magnet, a 2-quadrant (2Q) operation is mandatory to satisfy the time related operational constraint. This offers the opportunity to recover locally the energy during demagnetisation of the load. As a result, this solution allows for the integration of storage elements in the power supply, which is a novelty in a CERN design.

There is not only improvements to be done on the efficiency and modes of operation, there is also room for control and integration upgrades as well as improvement of the power supply stability to a record $0.1\,\mathrm{ppm}$ corresponding to $1.8\,\mathrm{mArms}$. Specifically, for this improved and modernised version of superconducting magnet power supply being designed, the output ratings are $18\,\mathrm{kA}$, $\pm 10\,\mathrm{V}$. The structure of the whole power supply is split in nine sub-converters, not including the *N+1* redundancy, rated for $2\,\mathrm{kA}$, $\pm 10\,\mathrm{V}$, which is the focus of this paper. From now on, the term *converter* refers to this $2\,\mathrm{kA}$ power supply.

The area of high-current low-voltage power supply remains obscure because of the very few applications that can take benefit from such power supply. One of the main application of such niche power supplies is the electro-magnets based domain [7]–[10]. The range of operation can be for medical, nuclear or, as already mentioned, research purposes in the case of fundamental physics. Depending on the specific application the voltage level can vary. Another field of application is for welding [11]. In this case the power supply classically uses an inverter, followed by a transformer for galvanic insulation and a simple diode rectifier as output stage [12]. Those kind of power supply relies on special transformer structure and requires strong filtering needs [13].

The main contributions of this paper are: (i) an optimisation algorithm that is considering multi-objectives design criteria, namely efficiency and volume, on the complete $2\,\mathrm{kA}$ assembly. (ii) the design, optimisation and implementation of a compact, thermally stable and high DC current biased powder core inductor. (iii) the realisation of a $250\,\mathrm{A}$, $\pm 10\,\mathrm{V}$ elementary building block of the optimised design.

This paper is organised as follows. Section II defines the requirements based on CERN and project specifications; it also details the mode of operation of the selected topology and the modularity structure of the complete power supply. Sections III and IV present the modelling and optimisation routine where the objective is to reach the most efficient yet compact solution and analyses its set of results. Section V contains the selection of the optimal design based on a figure of merit. It also covers the elementary building block prototype realisation. Section VI details the tests results obtained from the prototype.

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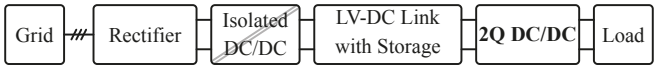

Fig. 1. Overall structure of a superconducting magnet power supply.

TABLE I
2Q DC/DC RATINGS.

Input voltage range	v_{LV}	[18 V; 30 V]
Rated output current	i_{load}	2 kA
Rated output voltage	v_{load}	±10 V
Allowed output current ripple	Δi	1 %
Allowed output voltage ripple	Δv	5 %

II. REQUIREMENTS

The overall structure of the superconducting magnet power supply is given in Fig. 1. The first stage consists of a diode rectifier (Rectifier) and a phase shifted DC/DC converter (Isolated DC/DC) whose purpose is to create a Low-Voltage (LV) DC link, fed from the CERN utility grid. This link (LV-DC Link with Storage) is the interface for the local storage within the power supply, that is used for the energy recovery from the load. The main focus of the paper is the 2Q DC/DC power supply which is fed from the same LV-DC link, and is used to provide the 2Q operation. The 2Q DC/DC ratings and output characteristics are gathered in Table I. Those are the requirements to be met, where the objective is to reach the most efficient yet compact solution.

In Fig. 2 is depicted a conceptual representation of the typical output mission profile, simplification of the real cycle. The nominal cycle is divided in three phases where initially the current in the load (superconducting magnet) is ramped-up to a steady-state value in around 20 min. After that, the output current is precisely regulated at 18 kA over the several hours of operation, before being brought back to zero in 20 min as well.

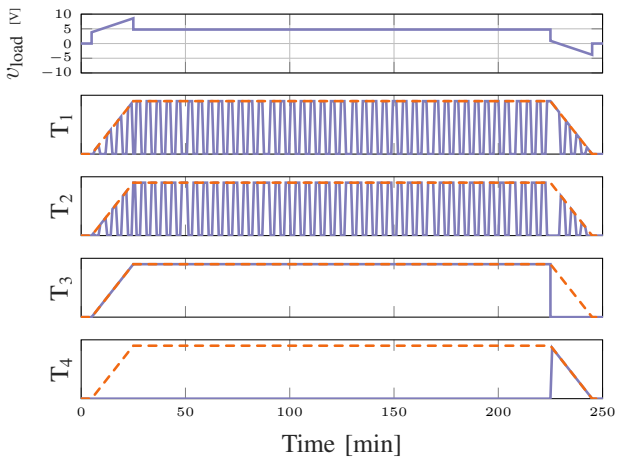

Fig. 2. Load voltage on a typical mission profile and current in the devices where the reference is the dashed line. The figure is only conceptual, it relies on a typical operation cycle and the presented duty-cycle is only qualitative. Switching, blocking or conducting states of the four semiconductors are presented, highlighting the switching and conducting behaviour of each leg.

On the one hand, the positive voltage output or *feeding mode* is applied during the initial magnet magnetisation and the steady phase, while the current is ramped-up to the nominal value and kept constant. On the other hand, to achieve the targeted 20 min demagnetisation, a negative voltage is applied during the recovery phase in order to bring the current down to zero; this is the *recovering mode*.

In the first case, the power flows from the LV-DC link to the load, in the second, the power flows from the load to the LV-DC link, the energy stored in the load is recovered locally in the power supply integrated energy storage. The actual implementation of the energy management system is outside the scope of this work and details are available in [14].

A. Mode of Operation

The simple full-bridge topology presented in Fig. 3 is selected for the output DC/DC stage, yet it is operated in an unconventional fashion in order to achieve the 2Q operation. For a positive voltage output: T_4 is turned-on constantly and consequently T_3 remains turned-off, while the pair T_1/T_2 is driven by a complementary Pulse Width Modulation (PWM) with adequate dead-times, as in synchronous rectification (cf. Figs. 3a and 3b). The topology generates a positive voltage on its output. In this mode, the operation is similar as a buck converter, where the duty-cycle is defined as the ON time of the MOSFET T_1.

For a negative voltage output, the switches operation is changed: T_4 is turned-off, T_3 is turned on, and the pair T_1/T_2 keeps being driven in PWM mode (cf. Figs. 3c and 3d).

The characteristic for the selected mode of operation is that in every case, only two devices are switching, one is conducting and one is blocking. In essence, one leg is constantly switching while the other is used as a polarity changer. The topology can be seen as two nested buck converters that allow voltage reversibility. The resulting output voltage is given in (1), where D_{T_1} is the duty cycle of the switch T_1.

$$v_{\text{load}} = \begin{cases} D_{T_1} \times v_{\text{LV}} & \text{for the } \textit{feeding mode}. \\ (D_{T_1} - 1) \times v_{\text{LV}} & \text{for the } \textit{recovering mode}. \end{cases} \quad (1)$$

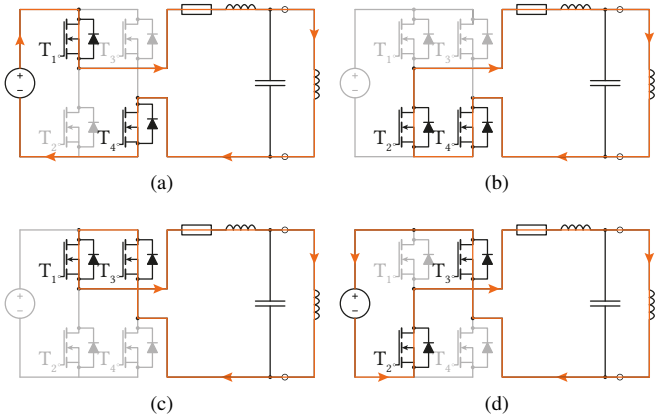

Fig. 3. Switching states of the topology: (a) *feeding mode* with T_1 ON and T_2 OFF, (b) *feeding mode* with T_1 OFF and T_2 ON, (c) *recovering mode* with T_1 ON and T_2 OFF and (d) *recovering mode* with T_1 OFF and T_2 ON.

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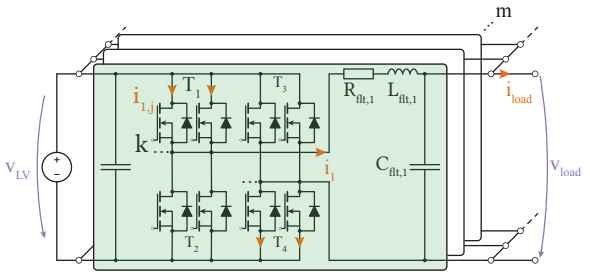

Fig. 4. Modularity of the DC/DC *converter*, split in m parallel *branches*. Within the *branch* (in green), the switches $T_{\#}$ are composed by k parallel devices arranged in a full-bridge topology. It is then followed by the single stage LC output filter. At the input side all of them share the same LV-DC link, the outputs are then all paralleled, in an IPOP configuration.

B. Modularity Considerations

In order to realise the output rating of $2\,\mathrm{kA}$, and considering the limited current rating of low voltage semiconductors, there is a need to either parallel many semiconductors devices or converter stages. The adopted structure of the 2Q DC/DC *converter* is presented in Fig. 4, where the *converter* is split in *branches*, composed by a full-bridge semiconductor stage followed by a single LC filtering stage.

The way to split the $2\,\mathrm{kA}$ *converter* into elementary building blocks (*branches*) should be evaluated in a rigorous manner, and it represents a design optimisation problem. The goal is to determine the optimal number m of parallel *branches* and/or the number k of parallel semiconductor devices for every switch position. Thanks to the input-parallel output-parallel (IPOP) configuration, the individual current seen by every semiconductors is the load current divided by $m \times k$.

The filtering stage is composed by a simple LC structure. Thanks to the large inductance of the load, in the order of few hundreds of mH, and the low-voltage on the DC bus, the single LC stage is sufficient to reach the ripple requirements. Considering the large current rating expected at the level of each branch, the filter inductor is considered as a discrete component for the design optimisation. Taking into account requirements from Table I, the actual values of the LC filter are adjusted for every possible design configuration, as it will be shortly explained in Section IV.

TABLE II
EQUATIONS FOR THE LOSSES EVALUATION IN THE SEMICONDUCTOR STRUCTURE.

Current (rms values)	switching	$i_{\text{out}}\sqrt{D_{T_\#}}\sqrt{1+\frac{1}{3}\left(\frac{\Delta i}{i_{\text{out}}}\right)^2}$
	conducting	i_{out}
	blocking	0
Conduction losses	$i^2_{h,j,\text{rms}} R_{\text{DS}_\text{on}}$	$h \in [1,\ k];\ j \in [1,\ m]$
Switching losses	$(E_{\text{on}} + E_{\text{off}})\ f_{\text{sw}}$	
Dead time losses	$2V_{\text{f}}\ t_{\text{dead}}\ f_{\text{sw}}\ i_{h,j,\text{dc}}$	
Rev. rec. losses	$Q_{\text{rr}}\ V_{\text{LV}}\ f_{\text{sw}}$	
Gate driver losses	$Q_{\text{g}}\ V_{\text{gs}}\ f_{\text{sw}}$	

III. Components Modelling

To carry out design optimisation, there is a need to identify suitable electrical and thermal models of the relevant components of the system. In the present case of the 2Q DC/DC converter, the key elements are the full-bridge based switching cell, the magnetic design of the filter inductor and the selection of the filter capacitor. Those elements should be optimally determined at the system level. Additionally, the efficiency (losses), the thermal constraints and gravimetric ($\mathrm{kW\,kg^{-1}}$) and volumetric ($\mathrm{kW\,dm^{-3}}$) power density of every possible design are of interest and require special attention.

A. Semiconductor Part

Considering that the converter structure and modes of operation are well defined, it is relatively easy to estimate the relevant semiconductor losses. This is summarised in Table II and implemented inside the design optimisation routines. The electrical quantities are calculated from the relevant operating points of the system, while the MOSFET parameters are extracted from the data-sheet of the selected device and scaled to include temperature dependency [15].

Once the losses are calculated, they are fed into the relatively simple thermal model which checks for steady-state maximum temperatures, considering device packaging and ambient conditions, using available thermal resistances in the model. To obtain the temperatures of the devices and define the cooling requirements, (2) is used. The P_{losses} are the sum of the relevant losses for a given device and the thermal equivalent resistance $R_{\text{th,eq}}$ is deducted from the MOSFET thermal model.

$$\Delta T = P_{\text{losses}}\ R_{\text{th,eq}} \tag{2}$$

A given MOSFET package implies a specific integration. An example for a surface mounted package is given in Fig. 5. As the heat should be evacuated from the chip, the good heat dissipation management of the Insulated Metal Substrate (IMS) Printed Circuit Board (PCB) technology is used. From this sequence of layers, a dedicated thermal model is created, from the junction down to the ambient environment.

B. Filter Inductor

The target value for the filter is considered at the worst operating point, when the duty-cycle is minimal. The minimal value of inductance to satisfy the requirements is then expressed in (3).

$$L_{\text{flt},j,\text{target}} = (v_{\text{LV,max}} - |v_{\text{out}}|)\frac{D_{\text{min}}}{f_{\text{sw}}\Delta i} \tag{3}$$

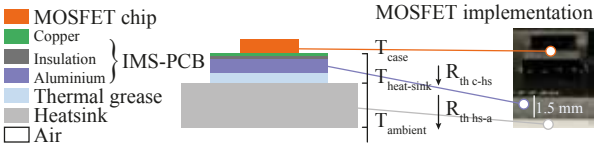

Fig. 5. Example of a thermal model linked to a surface mounted MOSFET and its implementation. Every layer is taken into the computation of the equivalent thermal resistance, from the junction to the ambient temperature.

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Two types of cores are considered, EQ and EE, based on ferrite and powder core materials. The EE cores give more freedom as they give the possibility to be stacked for a larger core cross section. To design the copper flat wire windings, the window geometry is scaled with the appropriate correcting factors for winding insulation and utilisation factor [16].

The process iterates on the number of turns of the inductor, which is expected to be rather low. For a given cross section of winding conductors, current density is evaluated considering predefined limit value that include the temperature dependence and respect the norm [17]. Then, if this criterion is respected, the A_L value is adjusted to the DC value thanks to the data-sheet Ampere-turn characteristics as expressed in (4). Finally the inductance value is computed with (5).

$$A_{L,\mathrm{DC}} = \mathrm{stack}\left(A_{L0} + N_l \; i_{\mathrm{pk}} \; \mathrm{slope}_{\mathrm{DCbias}}\right) \tag{4}$$

$$L_{\mathrm{design}} = A_{L,\mathrm{DC}} \; N_l^2 \; 10^{-9} \tag{5}$$

In this set of equations, N_l is the number of turns considered in the l^{th} iteration, stack is the number of stacked cores and $\mathrm{slope}_{\mathrm{DCbias}}$ is a negative value corresponding to the decrease of A_L when the DC bias increases in the core. For ferrite cores, the A_L also allows to compute the value of the air gap. The 10^{-9} scaling factor is used in (5) because $A_{L,\mathrm{DC}}$ is expressed in $\mathrm{nH/turns^2}$.

At the end of the process, a set of parameters defining the core combination and windings is retrieved. Additionally, when inputting the electrical set point into the calculations, the core and winding losses, taking into account the skin effect, are computed [16]. The overall mechanical properties in terms of volume and weight complete the set of output parameters of the design.

C. Filter Capacitor

The target value for the output capacitor is given by (6), based on the Buck converter output capacitor sizing, and scaled to the m branches in parallel.

$$C_{\mathrm{flt},j,\mathrm{target}} = \frac{1}{m} \times \frac{1 - D_{\mathrm{min}}}{8 \; L_{\mathrm{flt},j,\mathrm{target}} \; f_{\mathrm{sw}}^2 \; \Delta v} \tag{6}$$

TABLE III
ALLOWED RANGE OF VARIABLES FOR THE CONVERTER DESIGN.

m	f_{sw}	k	MOSFET
[4; 30]	[1 kHz; 500 kHz]	[1; 20]	[●; ●; ●; ●; ●]

The losses in the filter capacitors come from the Equivalent Series Resistance (ESR) Ohm losses, scaled to the switching frequency, as detailed in (7).

$$R_{\mathrm{ESR}} = \frac{\tan(\delta(f_{\mathrm{sw}}))}{2\pi \; f_{\mathrm{sw}} \; C_{\mathrm{flt},j}}; \quad P_{\mathrm{cap}} = N_{\mathrm{cap}} \; R_{\mathrm{ESR}} \left(\frac{\Delta i_{j,\mathrm{rms}}}{N_{\mathrm{cap}}}\right)^2 \tag{7}$$

Where $\tan(\delta(f_{\mathrm{sw}}))$ is the dissipation factor of the capacitor, at the frequency f_{sw}, and N_{cap} the total number of parallel capacitors in the converter. Once again, the design of this part is characterised by its losses and mechanical dimensions.

IV. Converter Design Optimisation

A design process is implemented in order to determine the best compromise between efficiency and volume for the power supply design. A sweep is performed over several degrees of freedom: the number of branches m, the switching frequency f_{sw}, the number of parallel devices k and considering suitable MOSFETs devices. A summary of the parameters and their variation is presented in Table III.

The general routine of the algorithm is depicted in Fig. 6. The first step *Initialisation* allows to gather the data from the various database and shape the structures that are containing the data used throughout the process. The next step is to generate the set of combinations within the range of the swept parameters for a given operational point, that happens during the *Compute combinations*. One combination gathers the critical parameters of the design, which makes it unique: the number of branches m, the selected MOSFET device, the switching frequency f_{sw}, the current per branch i_j ($j \in [1; \; m]$), the ripple allowed in the branch Δi_j, the target inductance and capacitance $L_{\mathrm{flt},j,\mathrm{target}}$ and $C_{\mathrm{flt},j,\mathrm{target}}$ respectively and the number of parallel devices k. The conditions for continuous conduction and current below the rating of the semiconductors need to be fulfilled in order for the combination to be saved and evaluated further.

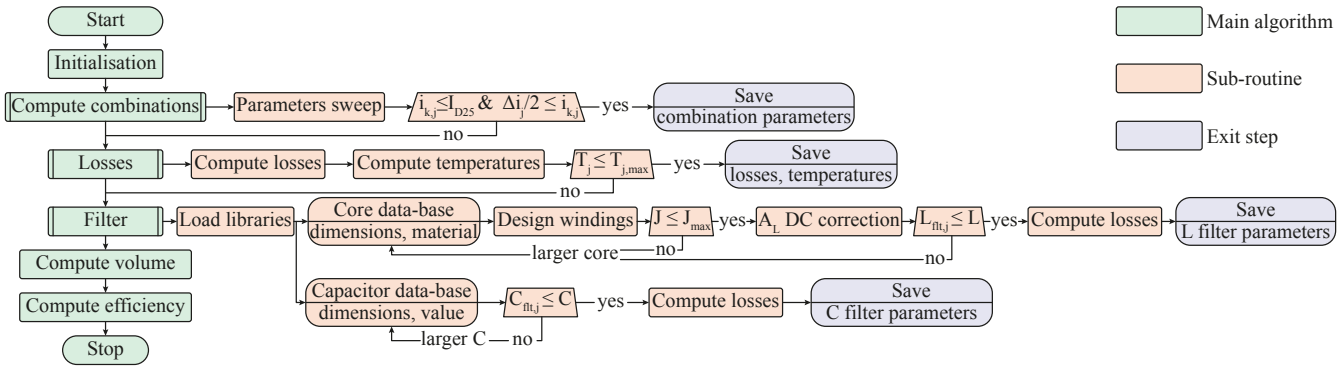

Fig. 6. Optimisation flow with the main routine on the left hand side (in green) and the details of the subroutines expanded horizontally (in orange). The final step of each sub-routine (in blue) is to save the meaningful parameters computed in every sub-routine.

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TABLE IV
SELECTED MOSFETS DEVICES.

Name	i_{D25}	v_{DSS}	$R_{DS_{on}}$	Identifier
IRFP4468PbF	290 A	100 V	2.6 mΩ	●
IXFN300N10P	295 A	100 V	5.5 mΩ	●
MMIX1F520N075T2	500 A	75 V	1.6 mΩ	●
STL220N6F7	260 A	60 V	1.4 mΩ	●
IPB015N08N5	180 A	80 V	1.5 mΩ	●

The selection of MOSFETs is reduced to five candidates which respect the following constraints: $V_{DSS} = 50 - 100\,\text{V}$; $I_{D25} \geq 180\,\text{A}$; low $R_{DS_{on}} \simeq 1\,\text{m}\Omega$; and different packages for different mechanical integration approaches. Namely the shortlist is presented in Table IV. From the generated designs the semiconductor losses are computed and the junction temperatures are estimated, and those which remain within acceptable limits are kept to the following steps. The input and output voltages are only related through duty-cycle, without any correction due to the voltage drop on the semiconductors.

The following step considers the passive LC filter design for both L and C elements. From there, every design is augmented by all the possible filters that reach the minimum $L_{\text{flt},j,\text{target}}$, making several filters possible for one combination.

The design of the filter inductor relies on a data-base of cores. For every m, different inductor current is implied, which modifies substantially the windings cross section. Consequently, the data-base is established with large ungapped ferrite and powder cores from two manufacturers [18], [19].

In order to define a design for the capacitive part of the filter, a film capacitor data-base is created from *Vishay MKT180* product line. It includes several capacitance values and their associated package for 63 V rated DC voltage. The input DC bus capacitors relies on the same set of components.

Finally the overall volume and efficiency are computed for every design that reaches this last step. The volume estimation takes into account an additional space corresponding to the mechanical parts needed around those essential elements such as the PCB or the bus-bars which is included through additional scaling factors.

A. Design Optimisation Results

Out of more than 12 000 electrically valid combinations and an ensemble of 4000 realistic filters, only in the family of stacked EE cores in powder material, more than 85 000 solutions are obtained. The set of solutions for the considered operating point of 2 kA and 10 V is plotted in Fig. 7a, where the distinction between the various MOSFETs is highlighted by the colour of the dots (cf. Table IV for the reference, column Identifier). A zoomed version on the area of interest is given in Fig. 7b, it corresponds to the most efficient combinations with the lowest volume.

B. Design Performances

The clearest trend in Fig. 7 is about the distinction between the five types of MOSFETs directly depending on their package, highlighted by different colours in the plot. The two smaller ones (● and ●), which are surface mounted on a PCB, lead to the most compact designs. Similarly, the largest is the MOSFET package, the more the design is shifted towards large volume; on the plot it means a shift to the right. To illustrate this better, a detailed plot is given in Fig. 8 (a) . For a given combination of $m = 8$, $k = 6$, $f_{sw} = 37.5\,\text{kHz}$ and the same filter, the five designs have very different volume and efficiency solely because of the MOSFET choice.

The apparent trajectories of points that appear in Fig. 8 (b), are actually several numbers of k for the same combination of all other parameters. The selected combination is with $m = 7$, $k \in [2;\ 20]$, $f_{sw} = 42.8\,\text{kHz}$ and the device ● with only a variation on the number of parallel MOSFETs k. Keeping $k \leq 10$ in Fig. 7 allowed to reduce the number of combination while keeping the local optimum of each combination. This parabola shape comes from the adaptation of external gate resistor that imposes a constant switching speed for all MOSFETs independently of the k.

Another analysis, illustrated in Fig. 8 (c), concerns the filter, where for one given electrical combination, several filter inductors are possible. This spreads the dots according to the volume and losses in the designed inductor. As an example, a configuration with $m = 15$, $k = 4$, $f_{sw} = 30\,\text{kHz}$ and the device ● can be achieved with 21 different filters.

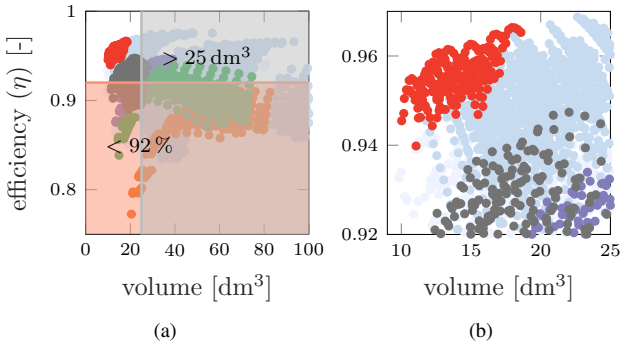

Fig. 7. Efficiency versus volume of the converter at 2 kA, 10 V output: (a) entire set of designs, with an highlight on $k \leq 10$ and $m \leq 8$, and (b) zoomed version on the promising solutions. Grey area covers the volume above 25 dm³, red area covers efficiency below 92 %. ● thermaly not viable design; ● k > 10; Cf. Table IV for the colour identifying the MOSFET.

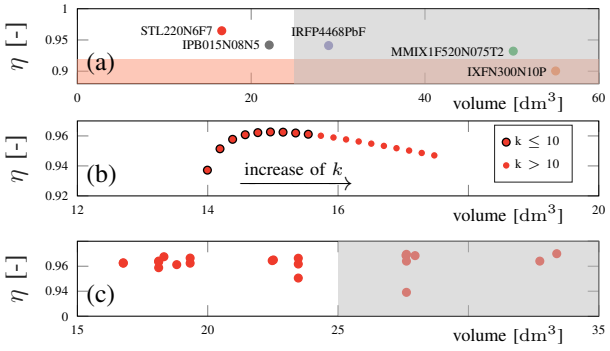

Fig. 8. Detailed efficiency versus volume: (a) change of MOSFET for $m = 8$, $k = 6$, $f_{sw} = 37.5\,\text{kHz}$, (b) variation of $k \in [2;\ 20]$ for the same combination of all other parameters $m = 7$ and $f_{sw} = 42.8\,\text{kHz}$ and (c) various filters with $m = 15$, $k = 4$, $f_{sw} = 30\,\text{kHz}$ and the same MOSFET.

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The superimposition of those three trends applied to the ensemble of electrically valid combination leads to the complete set of designs plotted in Fig. 7. From this ensemble of points, the most optimal design with respect to efficiency and volume is selected in the following Section V.

V. Selected Design and Realisation

In order to account for the volume as well as the efficiency of the system a figure of merit is introduced. It is defined according to (8), where weighting factors that manage the trade-off, can be associated with the efficiency w_η and the volume w_V.

$$\psi_{\text{design}} = \frac{w_V \times \frac{V_{\text{design}}}{V_{\max}}}{w_\eta \times \left(1 - \frac{P_{\text{losses}}}{P_{\text{out}}}\right)} \times 10^{-5} \tag{8}$$

As already highlighted in Fig. 7b, a selection of attractive designs with the MOSFET ●, $m \leq 8$, and $k \leq 10$ is located at the upper left corner of the efficiency versus volume plots. They are displayed in Fig. 9, where a front is defined thanks to the figure of merit ψ_{design} and the sweep of the associated coefficients w_η and w_V.

With $w_\eta = 2$ and the volume $w_V = 1$, a unique design can be selected. Out of the two competing solutions which are only differing by k, the one with the lower utilisation factor is preferred. The combination circled in Fig. 9 is the chosen design, where $m = 8$. Those eight parallel branches rely on the design detailed hereafter.

A. Full-Bridge Switching Cell

The design of the a basic branch includes $k = 6$ MOSFETs devices in parallel, that are switched at 50 kHz and used at a conservative utilisation factor, around 20 %. The summary of the semiconductor part of the design is given in Table V. Unfortunately, at the time of the design, the MOSFET reference of the optimisation was not available, imposing a change to a very similar one, whose characteristics are very close but differs for some parameters, *e.g.* $R_{\text{DS}_{\text{on}}}$ is 15 % larger.

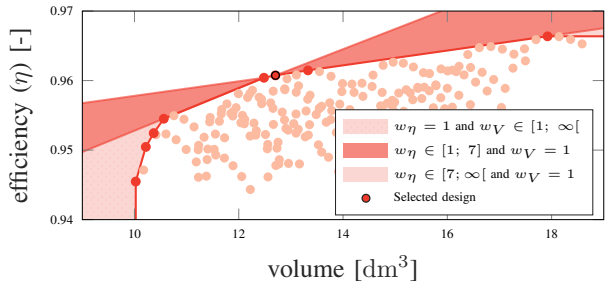
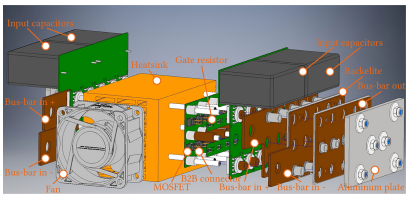


Fig. 9. Optimal designs front highlighted by the red line. Three areas are then filled depending on the weight given to the efficiency w_η and the volume w_V. On the one hand, when the focus is on the weight ($w_V > w_\eta$) the preferred designs are compact but their efficiency is 2 % lower than the most efficient designs. On the other hand, when the efficiency weight is preponderant ($w_\eta > w_V$), the designs are in the most efficient but almost two times larger than the most compact designs. The selected design is a compromise where the efficiency is advantaged with $w_\eta = 2$ and $w_V = 1$.

TABLE V
Semiconductor Characteristics of the Selected Branch Design.

Device	FDMS86550
Parallel devices	$k = 6$
Switching frequency	$f_{\text{sw}} = 50\,\text{kHz}$
Utilisation factor	0.179

Branch ripple	$\Delta i_j = 16\,\text{A}$
Branch current	$i_j = 250\,\text{A}$
Device current	$i_{l,j} = 42\,\text{A}$



(a) (b)

Fig. 10. Detailed views of the semiconductor assembly (a) exploded view on the heat-sink and (b) realisation of the full-bridge switching cell.

Additionally, some limitations in the availability of the film capacitors enforced some changes in the final implementation compared to the theoretical design. Nevertheless, the realised semiconductor module is a half-bridge and is represented in Fig. 10. The module is constituted of a stack comprised of (from left to right) the power PCB hosting the MOSFETs, the gate accessing PCB with the gate resistors and connectors, and the copper bus-bars for DC in plus and minus polarities and the middle point, isolated with Bakelite. The assembly is pressed against the heat-sink with an additional aluminium plate that comes to close the stack, as detailed in Fig. 10a.

The assembly of two semiconductor modules into the full-bridge topology of the branch is shown in Fig. 10b, where each of them is pressed on opposite sides of a square profiled heat-sink. An additional fan forces the air through the heat-sink, to bring the thermal resistance below $0.20\,\text{K}\,\text{W}^{-1}$. The full-bridge gate driver is not shown in this Fig. 10, but it is mounted on top of the assembly, sitting above the input film capacitors. It is the interface with the controller, embedding protection features, additional logic for the operation of the switches and that is connected through cables to the gate accessing PCB.

B. Filter Characteristics

The values of the branch LC filter to design are: $L_{\text{fltr},j} = 8.3\,\mu\text{H}$ and $C_{\text{fltr},j} = 800\,\mu\text{F}$. The core, winding characteristics are gathered in Table VI, and the implemented capacitor part is detailed in Table VII.

TABLE VI
Filter Inductor Characteristics of the Selected Design.

Core reference	00K114LE060	Peak flux density	$B_{\max} = 0.22\,\text{T}$
Permeability	$60\,\mu_0$	A_{L0}	$445\,\text{nH/turns}^2$
Core stack	3	$A_{\text{L,DC}}$	$330\,\text{nH/turns}^2$
Dim. E core	$114\times46\times35$ mm^3	Number of turns	$N = 3$
Core material	Powder *Kool Mu*	Winding resistance	$R_{\text{DC}} = 80\,\mu\Omega$
Core shape	EE	Winding width	16.7 mm
Inductance	8.9 µH	Winding thickness	14.3 mm

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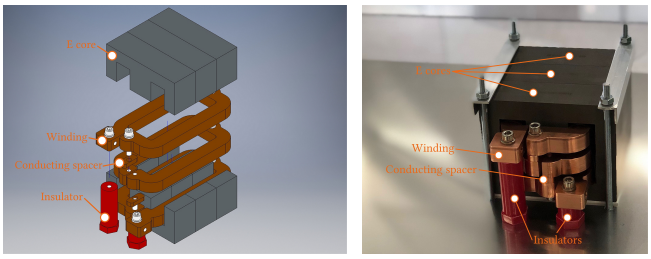
TABLE VII
FILTER CAPACITOR CHARACTERISTICS OF THE SELECTED DESIGN.

Reference	MKT1820733015
Manufacturer	*Vishay*
Dimensions	$35.0 \times 50.0 \times 57.5$ mm^3
Capacitance	330 µF
Parallel capacitors	3
Total capacitance	990 µF



(a) (b)

Fig. 11. Details of the inductor implementation (a) exploded view and (b) isometric view of the final assembly.

The capacitors are paralleled on a PCB which is directly interfaced to the output bus-bars of the branch.

For the inductor part, the windings are machined from a thick copper plate. Two standoff copper pieces allow the electrical connection between the turns, which are are linked to the base-plate through insulators. The assembly of cores is held together by aluminium clamps, and a sheet of Kapton isolates the windings from the core. Its overall volume is $1.45\,\mathrm{dm}^3$ and a detailed representation is given in Fig. 11.

C. Overall Losses and Volume

At the considered operating point applying 10 V on the load, the losses in the 2 kA converter sum up to 820 W, with a losses breakdown given in Fig. 12 (a) considering semiconductor and filter losses, and resulting in an efficiency of 96 %. The adaptation of the gate resistance value is the key element to establish the ratio between conduction and switching losses [20]: the switching time is defined constant at 300 ns for the switch, then depending on the MOSFET characteristics and number in parallel k, the external gate resistor is computed to obtain such switching time. This method allows to compare semiconductors on a fair basis.

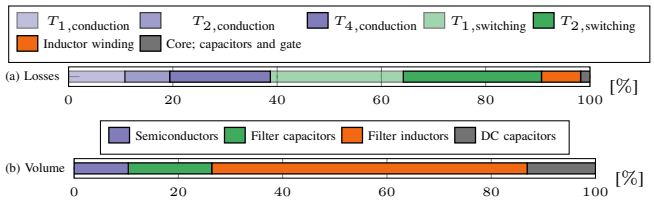
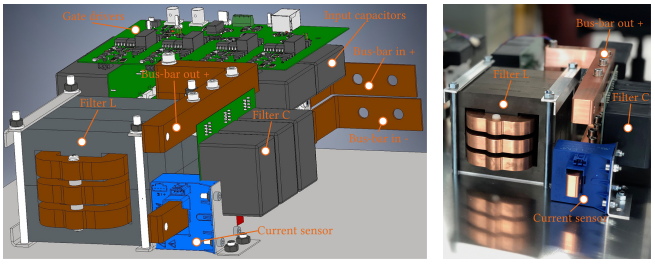


Fig. 12. Detailed breakdown of the branch (a) losses and (b) volume.



(a) (b)

Fig. 13. Details of the branch implementation (a) CAD rendering and (b) final implementation. It includes every element of the design and all the mechanics required to tied it to the base plate in a compact layout: it includes the gate driver, the output capacitor bank, the bus-bars and the current sensor.

The total volume estimation of the components of the converter is around $13\,\mathrm{dm}^3$, with a sharing given in Fig. 12 (b). The main element of this design is the filter inductor which occupies 60 % of the total volume.

With the adopted branch implementation, whose detailed assembly is given in Fig. 13, the global footprint of the branch is $210 \times 360 \times 115$ mm^3, summing up to $70\,\mathrm{dm}^3$ for the whole converter. That end result deviation from the original estimation comes from adding essential elements such as the appropriate heat-sink, some additional bus-bars to interconnect with the source and the load cables or mechanical pieces to tied the assembly together.

VI. EXPERIMENTAL RESULTS

Several tests are conducted to verify the performances of the prototyped branch. The first test consist in verifying the inductance value at 250 A. To this extent, the inductor is tested with the power choke tester *DPG10* [21]. The result of the test is provided in Fig. 14, where the measured inductance is 8.41 µH at the rated current for a target value of 8.9 µH, which is less than 10 % of deviation from target value.

In order to test the branch at its nominal current, and voltage a load composed of several high-current air cooled inductors is wired with adequate cross section cables, for a total equivalent inductance around 254 µH, with a current rating above 750 A and three different configuration with either an equivalent resistance of $R_{\mathrm{loadA}} = 25\,\mathrm{m\Omega}$, $R_{\mathrm{loadB}} = 44\,\mathrm{m\Omega}$ or $R_{\mathrm{loadC}} = 31\,\mathrm{m\Omega}$, it can be seen in Fig. 15a.

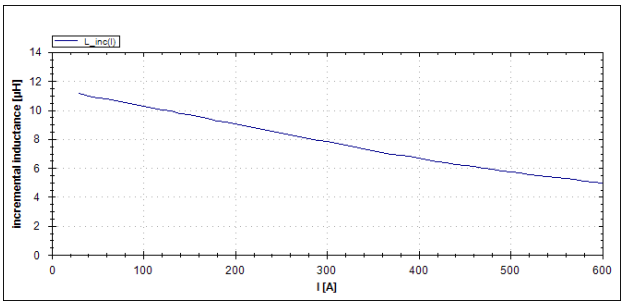


Fig. 14. Test result plot from the power choke tester, inductance L as a function of the current. The test sweep the current from 0 A to 600 A. The target value to be reached is 8.9 µH at 250 A.

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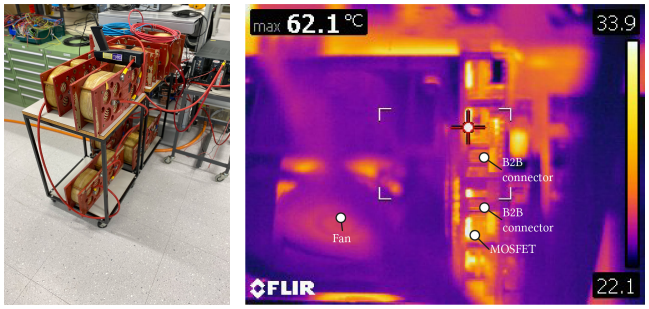

(a) (b)

Fig. 15. Details of the test setup (a) inductive load and (b) infrared capture of the switching module at the operating point 6.5 V, 255 A. One of the switching MOSFET can be seen warmer where the target points.

Fig. 16. Oscilloscope capture for the branch operating at 6.5 V, 255 A output. C1: load current i_{load} in A; dark blue; C2: T_1 Gate signal in V; pink; C3: input voltage v_{LV} in V; green. C4: output voltage v_{load} in V; red; C6: input current i_{in} in A; blue. The bandwidth is limited to 1 MHz for all the signals.

At the entry side of the the branch, a DC power supply rated at a maximum of 20 V and 2250 A [22] is connected. Finally, in terms of instrumentation, a wide-band power analyser *D6100* [23], with an external tri-axial shunt resistor rated for 300 A for the load side and 100 A for the source side, a 500 A current probe [24] in combination with a 500 MHz digital oscilloscope [25] are employed to extract efficiency and waveforms from the functioning prototype.

The semiconductor stage is tested using an open-loop control, where the degree of freedom is the modulation index set by the controller, similar as the duty-cycle of the PWM modulating the switching leg. The set-point to reach the nominal current is defined considering the DC power supply at its 20 V maximum, a duty-cycle around 40 % for T_1, and using the load in configuration A with the low resistance $R_{\text{loadA}} = 25\,\text{m}\Omega$. It leads to an output voltage of 6.5 V and an output current of 255 A. The nature of the power supply makes the losses in the topology very current-driven, the voltage having only a lesser impact on them, that is why this operating point is legitimate to evaluate experimentally the prototyped design at its nominal current.

An infrared picture of the switching stage is captured during the test at this operating point and shown in Fig. 15b, where the semiconductors can be identified in the stack, still the temperature of their case remains in an acceptable range.

Additionally, an outlook of the measured data at this operating point are provided in Fig. 16. The oscilloscope capture allows to visualise the evolution of the input voltage among others, where spikes can be identified when the switching events are happening, this is due to a weak DC bus capacitance, but their amplitude remains below 20 % of the 20 V input which is acceptable. Also, it can be seen that for the given operating conditions the peak-to-peak output current ripple is very low, and measure to be 1.9 A peak-to-peak thanks to the power meter, which is respecting the 1 % constraint given in Table I.

The power meter allows to get a precise reading on the input and output power as well as a verification of the average values that can be read on the oscilloscope. From this, and for several operating points, the practical efficiency is computed and plotted in Fig. 17. For the 224 A operating point with load B, the efficiency is $\eta_{\text{prototype}} = {}^{2248\,\text{kW}}/_{2516\,\text{kW}} = 89\,\%$.

In order to reach the nominal 10 V operation, the resistivity of the load should be increased. In this specific case, as only discrete elements are available for the wiring of the load, the reached value is $R_{\text{loadB}} = 44\,\text{m}\Omega$. This is not exactly matching the nominal current, leading to a second considered operating point at 10 V, 224 A. The waveforms are very similar to the one presented in Fig. 16, with the main change being the duty-cycle. The data provided by this second load configuration are also plotted in Fig. 17.

There is quite a difference between the theory and the reality of implementation where the efficiency is lower than expected. This can be explained by several factors, the first one is the equivalent resistance of the circuit, that is higher than the predicted one, when considering the whole conducting path including bus-bars, connections and interfaces. The second factor is the change in the selected MOSFET for the implementation whose $R_{\text{DS}_{\text{on}}}$ is 15 % higher than the modelled one. The third one is the model implemented into the design optimisation process that considers ideal devices, without any correction due to the voltage drop on the components, and the last factor is the addition of aluminium electrolytic capacitors on the DC bus.

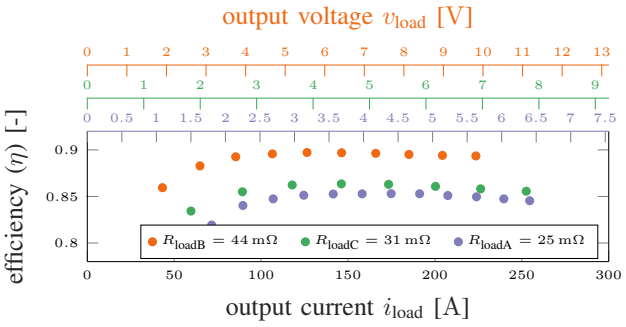

Fig. 17. Efficiency versus output current for several operating points. As the load is passive with an equivalent resistance of 25 mΩ, 31 mΩ or 44 mΩ, the corresponding output voltage v_{load} is indicated on the upper axis.

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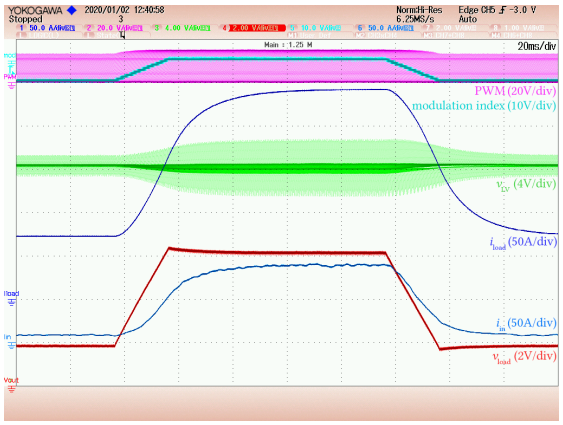

Fig. 18. Oscilloscope capture with the following configuration: C1: load current i_{load} in A; dark blue; C2: T_1 PWM gate signal in V; pink; C3: input voltage v_{LV} in V; green. C4: output voltage v_{load} in V; red; C5: modulation index; light blue; C6: input current i_{in} in A; blue. The bandwidth is limited to 1 MHz for all the signals.

In short, this variance in numbers between the theoretical prediction of Fig. 9 and the experimental results come from several losses that are not covered in the design phase. The extra $3.9\,\text{m}\Omega$ in the current path, measured during an additional continuous conduction test, represents an additional $250\,\text{W}$ of losses, impacting the negatively the efficiency figures obtain in the design optimisation process. The very nature of the power supply makes every parasitic resistance a source of disturbance on the low voltage output as well as additional losses because of the high current.

A dynamic test can also be conducted, in a very primitive way to mimic the nominal cycle of the converter. A rate-limited change between $15\,\%$ and $39\,\%$ duty-cycle is performed and the waveforms are given in Fig. 18, it corresponds to a change between $72\,\text{A}$ and $240\,\text{A}$ in $20\,\text{ms}$.

The same parameters as before are kept for the acquisition, in order to get the key variations of the signals of interest that are the input and output voltages and currents. The response is as expected with a smooth transition between the two operating points.

VII. Conclusions

In this paper, the path from the specifications, to the practical realisation of a high-current, low-voltage power converter elementary brick is defined. Once the requirements defined, the adopted topology and mode of operation are established. In order to fulfil the 2-quadrant operation, a full-bridge topology is used, with a peculiar modulation using one leg as switching and the other as polarity changer. Then, in order to defined the most suited structure of the whole converters, the key elements are modelled and used within an optimisation algorithm that defines a whole set of designs, according to the swept parameters. From this multiple possibilities, a figure of merit is constructed to highlight the best design accommodating the volume and efficiency constraints. After the characterisation of this optimal design, an implementation that takes into account the reality of component sourcing and machining capabilities is realised. Finally, tests are conducted in order to verify the implementation against the expectations, in a set of satisfying outcomes.

Acknowledgement

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