Efficient High Step-up Operation in Boost Converters Based on Impulse Rectification

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***Abstract*—Conventional boost converters, while having a high level of simplicity and robustness, are known to have a poor efficiency at high step-up regime. More complicated topologies have been extensively explored to increase the step-up ratio while keeping a high-efficiency, however, an efficient regulated dc-dc power conversion at high step-up regime still remains a challenge. In this work we demonstrate fully soft-switched operation of boost converters based on impulse rectification, which results in an efficient power conversion at very high step-up regime. Contrary to the conventional analysis of boost converters which seeks to minimize conduction and switching losses, our approach considers reactive power as the key parameter limiting efficiency. A theoretical basis for this operation mode enabled an appropriate design resulting in power conversion efficiencies above 90% for voltage gain values of 5, 10, 25, and 50, with a peak efficiency of 97%. The guidelines to design boost converters based on the proposed approach are discussed. The simplicity and high performance of this approach opens new avenues in designing regulated dc-dc converters with a high step-up.**

***Index Terms*—Boost converters, high efficiency, high step-up, impulse rectification, reactive power, E_{OSS}, C_{OSS}.**

I. Introduction

CLEAN energy resources such as photovoltaic (PV) and fuel cell (FC), exhibit low unregulated output voltage, which requires a dc-dc converter with a high voltage step-up ratio [1]-[6]. Several approaches including inductive switching (*e.g.* boost converters [1]), transformer-based topologies (*e.g.* dual active bridge (DAB) [2] and flyback converters [3]) and voltage multipliers [4] have been explored for efficient power conversion. Nevertheless, maintaining both high efficiency and regulation at high voltage gain values is still a challenge. For instance, the conventional boost converter, as one of the simplest step-up topologies, is known to be inefficient for large gain values [5]. Transformer-based topologies can potentially provide high voltage step-up, however, their soft-switching operation severely depends on the load condition. Voltage multipliers are typically unregulated and exhibit lower performance at high step-up regime, as the output voltage does not further scale with number of stages [7].

In this work, by utilizing a novel and unconventional approach considering the reactive power as a key parameter limiting efficiency, we theoretically and experimentally demonstrate efficient and regulated operation of standard boost converters (without any additional components) at very high step-up regime. Our approach treats the operation of the converter based on the generation and rectification of repetitive impulses resulting from resonance of the inductor and output capacitance (C_{OSS}) of the switch [8]. A theoretical basis is presented which shows guidelines to obtain high efficiency at high gain values. The high performance of this approach, together with its simplicity, open new pathways for the future dc-dc converters operating at high voltage gain values.

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II. Operation Principle

Fig. 1a shows a boost converter topology separated into two main stages. The first stage, including an inductor and a field-effect transistor (FET), converts the input dc voltage to a stream of high-voltage repetitive impulses. As shown in Fig. 1b, when FET is ON ($t_0 < t < t_1$), the inductor is smoothly charged by the input voltage V_{in}. At $t = t_2$, the FET is turned OFF. The resonance between L and C_{OSS} provides a zero turn-OFF loss (ZTL) [9]: because the switching time (Δt_{SW}) is much faster than $\sqrt{LC_{OSS}}$ time constant, the cross product of the channel current (i_{ch}) and drain-source voltage (v_{DS}) is completely negligible. The resonance between L and C_{OSS} results in the formation of an impulse waveform over drain-source terminals of the FET, as

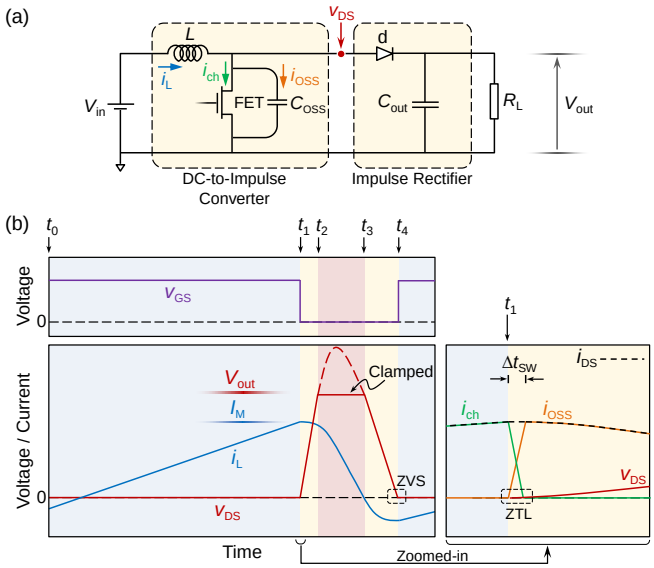

Fig. 1. (a) Boost converter topology, together with (b) illustration of the main waveforms v_{GS}, v_{DS}, i_L, and $i_{DS} = i_{ch} + i_{OSS}$.

TABLE I
Operation Principle Summary

Interval	FET	Diode d	Description
$t_0 < t < t_1$	ON	OFF	Inductor L is being charged
$t_1 < t < t_2$	OFF	OFF	Drain-source impulse starts to build-up (Energy transfer from inductor to C_{OSS})
$t_2 < t < t_3$	OFF	ON	Power transfer period (the impulse is clamped at V_{out})
$t_3 < t < t_4$	OFF	OFF	Restoring the energy of C_{OSS} resulting in a negative inductor current

the inductor current passes through C_{OSS} ($i_L = i_{OSS}$) [8]. The drain-source impulse gets clamped at $t = t_2$, when the voltage level reaches the output dc link voltage level V_{out}. During $t_2 < t < t_3$, the second stage shown in Fig. 1a rectifies the impulse and the inductor energy is injected to the output dc link. At $t = t_3$, when the inductor current reaches zero, the output voltage starts reducing. During $t_3 < t < t_4$, the energy stored in C_{OSS} is restored, which results in a negative current in the inductor. At $t = t_4$, the v_{DS} reaches zero and the FET turns ON, resulting in a zero voltage switching (ZVS). If the FET turns ON after $t = t_4$, then the inductor current flows through the body diode of the FET, resulting in a higher power dissipation due to reverse conduction losses. A turn-ON switching before $t = t_4$ is not favorable as it leads to a hard switching. Table I summarizes the discussed operation principle.

This operation principle, on one side, provides a soft switching, therefore it is not similar to the continuous conduction mode (CCM) operation mode. On the other side, the inductor has no discontinuation, hence, it cannot be considered as the conventional discontinuous conduction mode (DCM) operation. We refer to this operation mode as the impulse-rectification mode (IRM). In fact, IRM provides aspects from both conventional operation modes CCM and DCM: there is no interruption of the inductor current (as in CCM) and the converter is fully soft-switched (as in DCM). If the switch turns ON before t_4, the converter operates in the CCM mode, and if it turns ON long after t_4 (resulting a discontinuation in the inductor current), the converter will operate in the DCM mode.

III. Theory

In this section we present a theory describing the operation of the boost converter based on impulse rectification. First we focus on the impulse generator circuit and then we analyze the overall performance of the converter.

A. Impulse generator circuit

Here we consider the DC-to-impulse converter shown in Fig. 1a, when diode d is always in the OFF state. At $t = t_1$, a resonance between L and C_{OSS} starts, and the energy stored in L is transferred to C_{OSS}, as a high-amplitude impulse signal. Considering I_M as the maximum current of the inductor, and neglecting C_{OSS} losses [10] and the energy dissipated in the inductor series resistance (R_{ind}), the amplitude of the impulse waveform can be written as

$$V_M = I_M Z, \tag{1}$$

with

$$Z = \sqrt{L/C_{OSS}^{er}}, \tag{2}$$

where C_{OSS}^{er} is the energy-related effective C_{OSS}, which is a fixed equivalent capacitance that would give the same stored energy as C_{OSS} for v_{DS} rising from 0 V to the stated V_M (or V_{out}, in case of connecting the output dc link). The maximum current flowing through the inductor, under the assumption of operation in the linear regime, is

$$I_M = V_{in} T_{ON} / L \tag{3}$$

where T_{ON} is ON-state time duration of the FET switch. To obtain an energy-efficient charging of inductor, T_{ON} should be lower than the charging time-constant of the inductor $\tau = L/(R_{ind} + R_{ON})$, where R_{ON} is the ON-resistance of the FET.

B. Rectification of repetitive impulses

The second stage rectifies the repetitive impulses into the output dc link. In the no-load condition, the output voltage equals to V_M. Therefore, using (1) and (3), and considering $T_{ON} = \tau$, the maximum voltage gain $M_{max} \triangleq V_M/V_{in}$ is

$$M_{max} = \frac{Z}{R_{ind}+R_{ON}}. \tag{4}$$

In the presence of a load, however, the generated impulses get clamped to the output dc link V_{out}. A part of the inductor energy is consumed to charge the C_{OSS} up to V_{out}

$$E_{OSS} = \tfrac{1}{2} C_{OSS}^{er} V_{out}^2. \tag{5}$$

Therefore, the injected energy per pulse into the output dc link is $E_{out} = \frac{1}{2} L I_M^2 - \frac{1}{2} C_{OSS}^{er} V_{out}^2$, which using (1) and (2) results in

$$E_{out} = \tfrac{1}{2} C_{OSS}^{er} (V_M^2 - V_{out}^2). \tag{6}$$

Considering $V_M = M_{max} V_{in}$ and $V_{out} = M V_{in}$, where M is the voltage gain in the presence of the output dc link, one can rewrite (6) as $E_{out} = \frac{1}{2}(M_{max}^2 - M^2) C_{OSS}^{er} V_{in}^2$. As a result, the output power is

$$P_{out} = \tfrac{1}{2}(M_{max}^2 - M^2) C_{OSS}^{er} V_{in}^2 f_{SW}. \tag{7}$$

Using (1), (2), and (7), we write

$$P_{out} = [1 - (\frac{M}{M_{max}})^2] P_{max}, \tag{8}$$

where

$$P_{max} = \tfrac{1}{2} L I_M^2 f_{SW}. \tag{9}$$

Equation (8) shows a high power conversion for $M \ll M_{max}$. In other words, considering the reactive power $Q_r = E_{OSS} f_{SW}$, the condition $M \ll M_{max}$ is satisfied for $Q_r \ll P_{max}$, which is equivalent to $E_{OSS} \ll \frac{1}{2} L I_M^2$. On the other hand, I_M should be

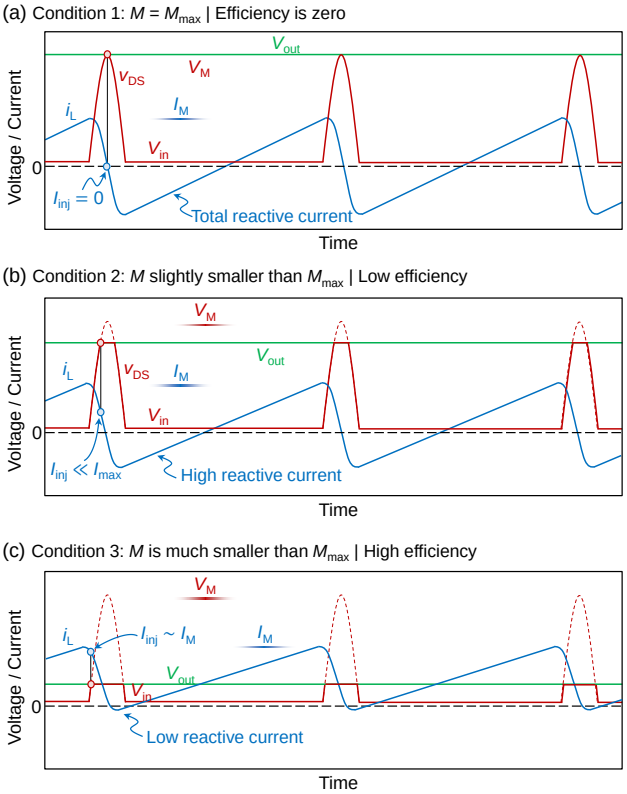

Fig. 2. Operation of boost converter in thee conditions (a) $M = M_{max}$, (b) $M \lesssim M_{max}$, and (c) $M \ll M_{max}$.

significantly lower than the saturation current I_{sat}, so that charging and discharging of the inductor is efficient (considering core losses, etc). In summary, to obtain a high efficiency, the following inequalities should be achieved

$$E_{OSS} \ll \frac{1}{2} L I_M^2 \ll E_{ind}^{sat}, \quad (10)$$

where E_{ind}^{sat} is the energy of inductor at its saturation. Equation (10) shows the ideal range of inductor current to obtain a high efficiency. Based on this analysis, the inductor current I_M is the main parameter determining the efficiency of the converter. Obviously, the necessary condition to achieve (10) is

$$E_{OSS} \ll E_{ind}^{sat}. \quad (11)$$

Equation (11) is a guideline to choose the inductor and FET to achieve a high-efficiency power conversion. It is indeed this condition that is the missing point in the design of boost converters. Traditionally, devices with low R_{ON} are favored for decreasing conduction losses, but a low R_{ON} comes with a high C_{OSS} and E_{OSS}, which does not necessarily satisfy (11). On the other side, R_{ON} lower than R_{ind} does not lead to a considerable reduction in conduction losses, so the efficiency becomes worse.

In particular, for an efficient power conversion at high-step-up regime, the importance of designing the circuit to obtain a high M_{max} can be seen in (8). Fig. 2 shows three possible conditions according to M and M_{max}. For $M = M_{max}$, the power transfer is zero and all the power is reactive (Fig. 2a). If M is close to M_{max}, then the output power is very limited while the reactive power is high, as a significant portion of inductor energy just charges C_{OSS} up to V_{out}, and only a small current $I_{inj} \ll I_M$ is injected to the output dc link (Fig. 2b). This results in a high reactive-power in the circuit, and consequently high conduction-losses and a low efficiency. As shown in Fig. 2c, for $M \ll M_{max}$, the injected current into the output dc link is almost equal to the maximum current of inductor, resulting in a low reactive power and thus in a high efficiency. The most important point deduced from (8) is that a high step-up voltage gain M has no independent meaning, since it should be considered with respect to M_{max}. For instance, with a design corresponding to $M_{max} = 100$, it is not possible to have a high efficiency at $M = 70$, while with $M_{max} = 1000$, the obtained efficiency can be much higher. Based on (4), selecting a MOSFET with very low R_{ON} is not beneficial as the high C_{OSS} decreases Z, while R_{ind} becomes dominant in the denominator.

IV. Design Aspects and Experimental Results

We experimentally demonstrate an efficient high-step-up power conversion using boost converters based on the proposed operation (Fig. 3a). The key point is to achieve the condition in (11) with a large M_{max}, while keeping the conduction losses small. Here we separately discuss the different design aspects:

1) A high quality (Q) factor and low core-losses are required for the inductor, as all the power is transferred through this component. A higher Q-factor (lower R_{ind}) not only decreases the conduction losses, but also enlarges M_{max}, which is beneficial for high step-up operation. For a more precise description, one can combine the winding series resistance and core losses to define an effective R_{ind}, and determine its effect on M_{max} [11]. Although Q-factor and core-losses are potentially very important for an efficient power conversion, they are not typically given in datasheets, especially for power magnetics. Therefore, after measuring several different commercial inductors, a high Q-factor (Fig. 3b) inductor (L = 10 μH) with low core-losses (Fig. 3c) was selected. In fact, the efficiency of the converter can be further improved by using well-design inductors that provide Q-factors as large as 1000 [12]. Another important point about the high step-up operation is that, because of a large duty cycle values, the difference between f_{SW} and the resonance frequency (f_{RES}) becomes large, so the inductor should provide a high Q-factor for two very different frequencies (f_{SW} and f_{RES}). For the selected inductor, the Q-factor is larger than 100 for a large range of frequencies, starting from 100 kHz up to higher than 10 MHz (Fig. 3b).

2) Large E_{ind}^{sat} is beneficial for an efficient power conversion according to (11). Considering several datasheets of commercial inductors, it can be seen that within a same family, the I_{sat} drops as the value of L increases, so that LI_{sat}^2 remains almost constant. Therefore, the value of L is not critical by itself, however, an inductor design providing higher saturation current at a constant inductance (either by employing ferrite materials with higher magnetic permeability or by increasing the effective core cross-section) is beneficial [12], [13]. The selected inductor in this work has a large I_{sat} ~ 20 A, however, due to the core losses, the charging and discharging becomes inefficient after about 5-A, corresponding to E_{ind} = 125 μJ.

3) The last step is to choose the FET switch, by considering the trade-off between R_{ON} and E_{OSS}. Wide-band-gap transistors typically have a lower E_{OSS} at a same R_{ON}, so they are more appropriate for this application. An 80-mΩ SiC MOSFET with E_{OSS} = 7 μJ was selected. The value of E_{OSS} is significantly lower than E_{ind}. On the other side the R_{ON} is about the same as R_{ind} at 100 kHz. Therefore, this is a proper switch based on the proposed theory.

An 8-A SiC schottky diode with low forward voltage (IDDD08G65C6) and an isolated gate driver (SI8271) were used. The input and output dc-link capacitors were mounted on

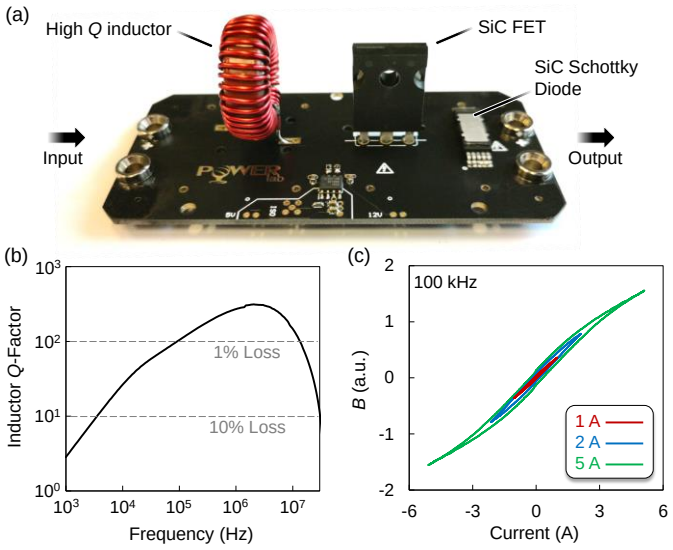

Fig. 3. (a) Prototype of an ultra-high step-up boost converter, together with (b) Q factor of the used inductor (L = 10 μH) measured with a Keysight E4990A impedance analyzer, and its (c) large signal hysteresis characterization.

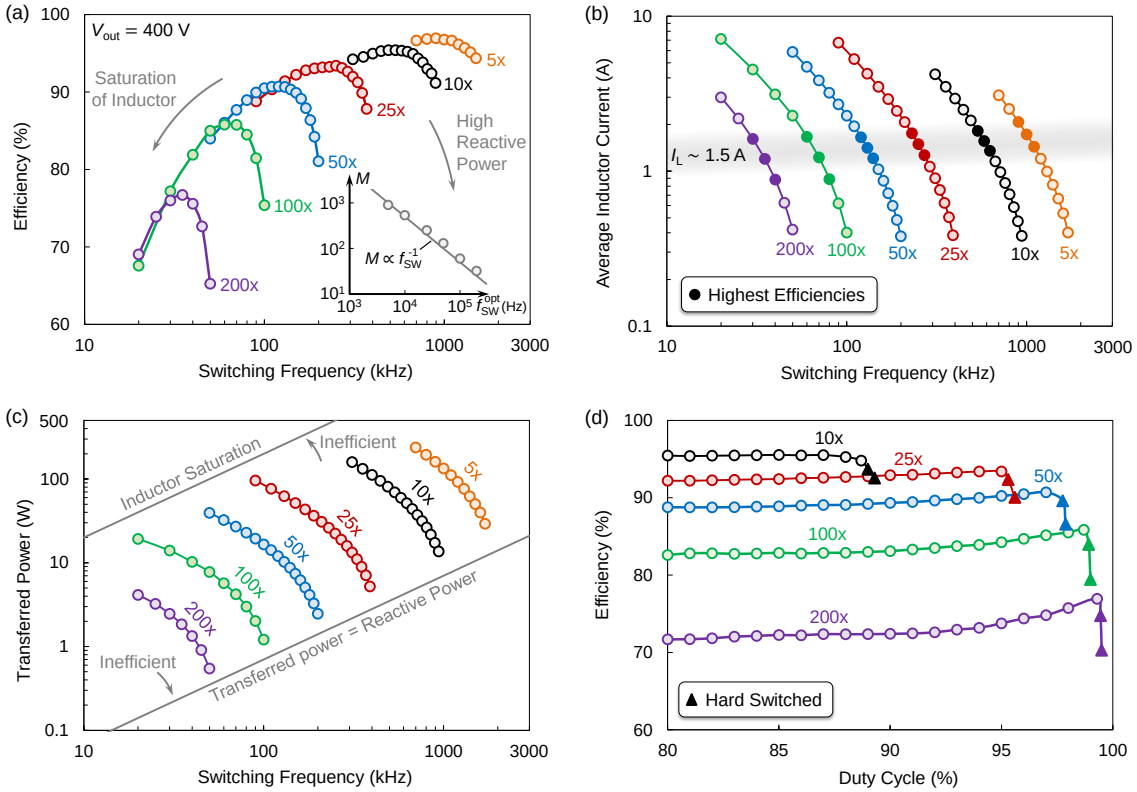

Fig. 4. (a) Power conversion efficiency, (b) average inductor current, and (c) transferred power, versus switching frequency for different voltage gain values. (d) Efficiency versus duty cycle at the optimum switching frequency, for different voltage gain values.

the backside of the printed circuit board (PCB). The measured results are presented in Fig. 4. For all of the experiments, the output voltage is fixed at 400 V. Fig. 4a shows 97% efficiency power conversion at 5-time step-up (V_{in} = 80 V), while the converter keeps a high efficency for higher voltage gains. Power conversion efficiencies of 95.4% and 93.4% have been achieved for 10-times and 25-times voltage gain values. For higher step-up gain values, based on (3), T_{ON} should be higher, resulting in a lower switching frequency. This eventually results in a lower Q-factor for the used inductor (Fig. 4a). For very high step-up voltage gain values of 50, 100, and 200, power conversion efficiencies of 91%, 86% and 77% were achieved, respectively. It should be noted that the proposed operation mode has the potential to be combined with voltage multiplier circuits (*e.g.* hybrid switched capacitor converters [14]) which enables a high-voltage level at the output. This could provide more efficient solutions than current ultra-high step-up dc-dc converters [15], with applications in electron gun drivers, terahertz vacuum electron devices, x-ray sources, and pulsed-power [16], [17].

The inset in Fig. 4a, shows the optimal switching frequency f_{SW}^{opt} (corresponding to the highest efficiency), which is inversely proportional to step-up gain. This is well-matched with the theory, since considering $T_{ON} \sim 1/f_{SW}$ and $V_{in} = V_{out}/M$, we can rewrite (3) as $f_{SW} \times M \approx V_{out}/LI_M$. Assuming fixed values for L and V_{out}, the optimal switching freuquency is inversely proportional to step-up gain

$$f_{SW}^{opt} \times M \approx \frac{V_{out}}{LI_M^{opt}} = \text{const.} \qquad (12)$$

Fig. 4b shows that for all voltage gains, the maximum efficiency occurs at an almost indentical inductor current. This is in agreement with the proposed theory, since based on (10), I_M is the main parameter that determines the efficient operation of the converter, which here occurs at the average current of ~1.5 A. Considering the current waveform shown in Fig. 2c, this average current corresponds to the optimal I_M of $I_M^{opt} = 3\ A$. To compare this value with the ideal efficiency range presented in (10), one can calculate the energy of inductor for I_M^{opt}: $E_{ind} = \frac{1}{2}(10\ \mu H)(3\ A)^2 = 45\ \mu J$. This energy is significantly larger than E_{OSS} = 7 µJ (at 400 V), showing that the active power is much larger than the reactive power (or equivalently $E_{OSS} \ll E_{ind}$). The optimal current I_M^{opt} is also much lower than the saturation current of inductor (~20 A), showin that the condition $E_{ind} \ll E_{ind}^{sat}$ is obtained.

Fig. 4b also demonstrates how the input current (∝ power) can be regulated by the switching frequency, resulting in a regulation of output power (Fig. 4c). Based on (10), the efficient region of P_{out} is determined by the reactive power level and saturation of the inductor, which are shown by two lines in Fig. 4c. The converter provides a higher power conversion at higher input voltages (lower voltage gain). At 5x-step-up it can deliver 240 W with an efficiency of 96.6%, and an average input current of 3 A. The 240-W measurement point in Fig. 4c is still far from the inductor saturation limit. Furthermore, the employed FET is 30-A rated, and therefore, has the capacity to extend the input current. As a result, a higher power conversion, in the kW can be achieved with a proper cooling. Eq. (9) shows the guidelines to increase the power rating of the converter, which relies on increasing the LI_M^2 term (inductor design) and

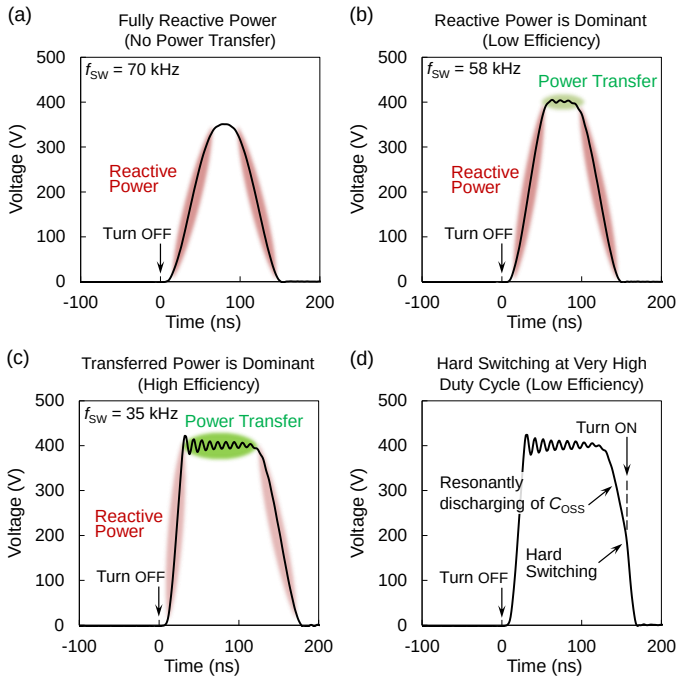

Fig. 5. Drain-source voltage waveforms showing the generated impulses for the case of 200-times step-up. (a) $V_M < V_{out}$ resulting in zero power transfer. (b) V_M is slightly larger than V_M. (c) V_M is considerably larger than V_M. (d) In the case of very large duty cycle, the FET loses ZVS and it turns ON before the impulse resonantly reaches zero ($t = t_4$ in Fig. 1), and therefore, a part of the energy stored in C_{OSS} is dissipated in the FET channel. This results in lower efficiencies (Fig. 4d).

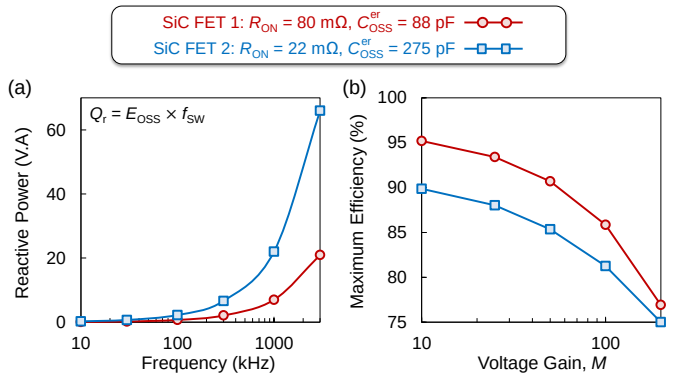

Fig. 6. (a) Reactive power versus switching frequency for two different devices FET1 and FET2. (b) Maximum obtained efficiencies versus voltage gain, for converters utilizing FET1 and FET2. Although FET2 has a lower R_{ON}, it corresponds to a lower efficiency because of higher reactive power.

also f_{SW}. Another possible approach to increase the power delivery is by stacking several converters in parallel. In this case one can consider a phase-shift between the gate signals of different converter blocks for smoothing the output voltage and reducing conduted EMI.

The converter perfomance is insensitive to the duty cycle, except at very high duty cycles, where the FET operates in hard switching and forces the impulse to zero (Fig. 4d). Just before the hard-switching, a relatively higher efficiency can be obtained (especially for the case of M = 200). In this case, just after the generation of impulse, the FET turns ON again, so the residual energy of inductor is restored through the FET channel, instead of body diode, resulting in a higher efficiency. This is more critical for higher step-up gain values, as the transferred power is lower while the reactive power is fixed.

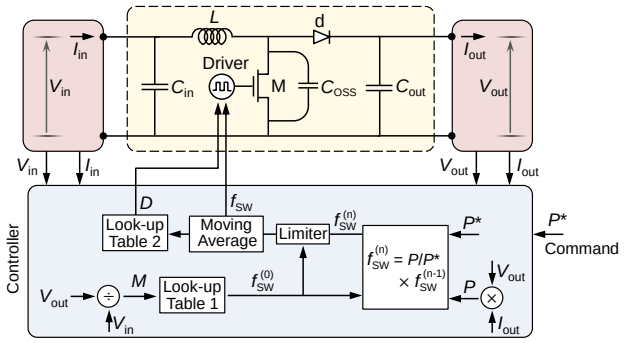

Fig. 7. Scheme for controlling power transfer in IRM boost converter.

Fig. 5 shows four drain-source voltage waveforms, corresponding to different operation conditions of the circuit, all captured for V_{in} = 2 V. In Fig. 5a, due to the high switching frequency (low I_M), the impulse amplitude, V_M, is lower than V_{out}, resulting in zero power transfer. In Fig. 5b, the converter starts to inject power to the output dc link, but still the reactive power is dominant. At 35 kHz, the amount of transferred power is large, resulting in a considerably higher efficiency. At lower switching frequencies, the inductor charging becomes less efficient due to the lower Q-factor and higher core losses, which decreases the power conversion efficiency.

As discussed, in the impulse-rectification operation, balancing the trade-off between R_{ON} and E_{OSS} is crucial. Whereas R_{ON} contributes to conduction losses, selecting a device with a very small R_{ON} (lower than ac resistance of the inductor) results in a high E_{OSS} and high reactive-power (Fig. 6a) which limits the efficiency on (11). Fig. 6b shows the measured efficiency of the circuit shown in Fig. 4a, for two SiC switches within a same family but with two different R_{ON}. The classic view of the circuit may predict a higher efficiency for SiC FET2, which has a lower R_{ON}. However, SiC FET1 shows a consideably higher efficiency which is due to its lower E_{OSS}. It should be noted that lower efficiency in case of SiC FET2 is not due to additional switching losses (as ZVS is achived in the turn-ON), but because of the higher reactive power in the circuit.

As presented in Fig. 4, switching frequency is the main control parameter in the proposed operation mode. Considering a constant output dc link voltage, the required voltage gain M directly determines the optimal switching frequency f_{SW}^{opt}. This could be done by using a look-up table (data shown in the inset of Fig. 4a), or by using the approximate relation (12). By tuning the switching frequency around f_{SW}^{opt}, one can adjust the power level (Fig. 4c). Fig. 7 shows a simple realization of the proposed control strategy. The look-up table 1, determines f_{SW}^{opt} based on M. This is used as the initial switching frequency of the converter ($f_{SW}^{(0)}$). The required power level (P^*) is compared to the actual power level (P). Replacing (3) in (9) with $T_{ON} \sim 1/f_{SW}$ and also neglecting the reactive power in the circuit results in

$$P = \frac{V_{in}^2}{2Lf_{SW}}. \qquad (13)$$

Therefore, the converted power level is inversly proportional to f_{SW}. This can also be observed in Fig. 4c. As a result, in order to reach the power level P^*, one can use $f_{SW}^{(n)} = f_{SW}^{(n-1)} \times P/P^*$,

as a sequence converging to the proper f_{SW} that provides $P = P^*$. One can use extra considerations for this control strategy. For instance, $f_{SW}^{(n)}$ should not be too far from f_{SW}^{opt}, this can be done by a limiter that constantly compares $f_{SW}^{(n)}$ and f_{SW}^{opt} (Fig. 7). One can consider a maximum allowed deviation from f_{SW}^{opt}, which corresponds to the maximum tolerable loss in the converter. A moving average block can also be used to smoothly change the switching frequency. In case of non-fixed input/output dc link voltages, one can update the value of M, after a certain number of iterations n, so that the recursive sequence $f_{SW}^{(n)} = f_{SW}^{(n-1)} \times P/P^*$ starts again with an updated initial value $f_{SW}^{(0)}$. Adjusting the duty cycle is not crutial in the converter, however, it should not exceed a critical value to avoid hard switching (Fig. 5d). As a result, a look-up table can be used to determine D based on the switching frequency.

V. Conclusion

The operation of standard boost converters based on rectification of repetitive impulses was proposed, and theoretically and experimentally studied. The approach enables an efficient power conversion at high step-up gains. The main outcomes can be highlighted as:

1) IRM is a novel operation mode, as it is fully soft-switched (unlike CCM), and there is no interruption in the inductor current (unlike DCM). In this operation mode, the output power can be regulated by the switching frequency, and is barely sensitive to the duty cycle.

2) We derived the maximum possible voltage gain (M_{max}) that offers guidelines to design high-step up converters. M_{max} just depends on selection of inductor (L and R_{ind}) and transistor (C_{OSS} and R_{ON}). Based on these guidelines, we experimentally demonstrated high-step up operation with a high efficiency.

3) Although the converter is fully soft-switched, the amount of reactive power in the circuit (corresponding to charging and discharging the C_{OSS}) should be considered in its design. In particular, (11) shows the required inequality to obtain high efficiencies. Based on this guideline, using an 80-mΩ SiC MOSFET with C_{OSS} = 88 pF, a peak efficiency of 97% was obtained, while with another SiC MOSFET with much lower ON-resistance 22-mΩ (much lower conduction losses) but a higher C_{OSS} = 275 pF, the obtained efficiency was much lower (Fig. 6b).

This achievement is of great importance for the future high step-up dc-dc converters.

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