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IGCT Low-Current Switching – TCAD and Experimental Characterization

Dragan Stamenković, *Student Member*, Umamaheswara Reddy Vemulapati, *Member, IEEE*, Thomas Stiasny, Munaf Rahimo, *Member, IEEE*, Dražen Dujic *Senior Member, IEEE*

Abstract—Utilization of the Integrated Gate Commutated Thyristor as a semiconductor switch in the Series Resonant Converter for isolated medium voltage DC-DC conversion offers an opportunity for high conversion efficiency while operating at the high switching frequency. Low conduction losses of the switch as well as decreased switching losses due to zero-voltage turn-on and low current turn-off in the sub-resonant operating regime are reflected in the efficiency increase of the converter. This paper explores the switching behavior of the semiconductor device under low currents while giving insight into the achievable turn-off energy losses and duration of the turn-off transients, as information required during the design process of series resonant converter. Experimental measurements confirm trends observed with simulation results related to turn-off delay process, providing further understanding of the switching losses and achievable performances under resonant mode of operation.

Index Terms—DC transformer, MVDC, IGCT, resonant DC-DC converter

ABBREVIATIONS

DAB	Dual-Active Bridge
HVDC	High Voltage Direct Current
IGBT	Insulated Gate Bipolar Transistor
IGCT	Integrated Gate-Commutated Thyristor
MVDC	Medium Voltage Direct Current
NPC	Neutral Point Clamped
RC-IGCT	Reverse Conducting Integrated Gate-Commutated Thyristor
SOA	Safe Operating Area
SRC	Series Resonant Converter
TCAD	Technology Computer Aided Design

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I. INTRODUCTION

Medium Voltage Direct Current (MVDC) distribution networks are lately in the focus of research interest both in academia and industry [1]–[3]. The topic of the DC transformer, the key missing element in the system, offers the opportunity for further experimentation and analysis of the isolated medium voltage DC-DC converters that could take over this role in the future.

The decrease of the system components required for the operation, plus the high efficiency and space utilization makes the MVDC distribution very attractive in the marine applications as presented in [4]–[6]. One variant of the Series Resonant Converter (SRC) described and discussed in [7] and [8] is used as the backbone of the MVDC grid based offshore wind farm energy collection. AC transmission has already

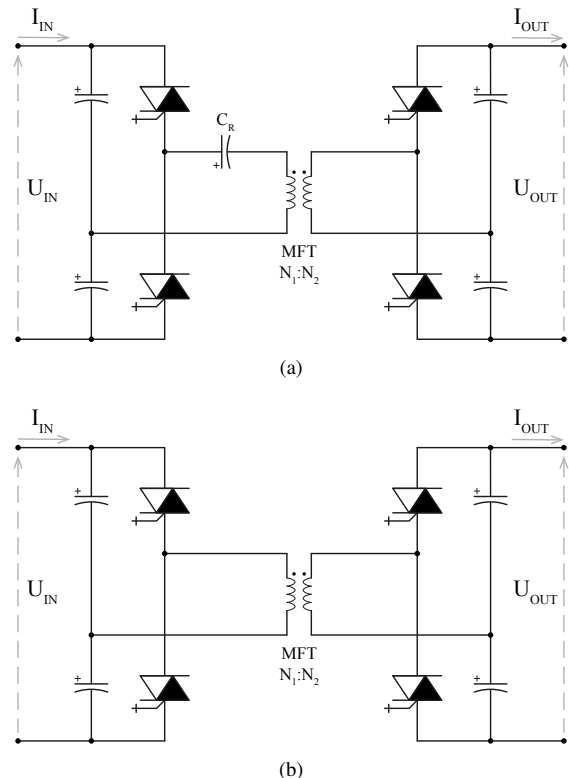


Fig. 1: Two popular isolated DC-DC converter topologies with an RC-IGCT as a switching element a) series resonant converter b) dual-active bridge

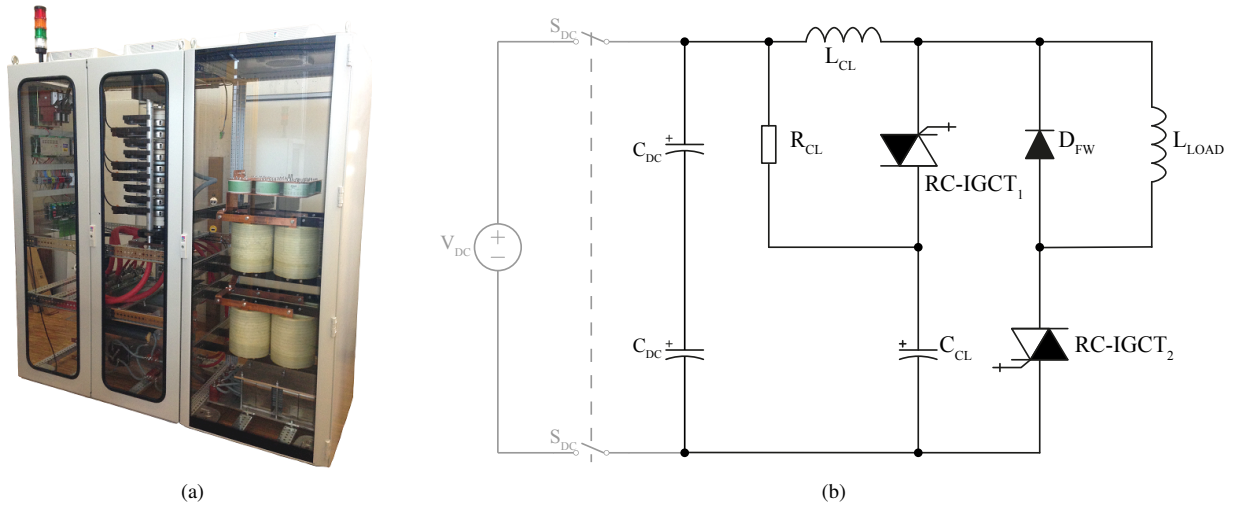


Fig. 2: a) Multifunctional test setup used for performing double-pulse tests b) Schematic of the test setup when used for double-pulse test

been surpassed by the High Voltage Direct Current (HVDC) transmission for connecting on-shore loads to off-shore power generation as well as for very long interconnections. As the HVDC networks grow in size and availability, there will be the need for direct transformation of the voltage levels between HVDC transmission and MVDC or LVDC distribution for bringing power to various industrial and residential consumers. Various high power DC-DC converter topologies have been proposed recently [9]–[12], capable of easily achieving the interface requirements.

Insulated Gate Bipolar Transistor (IGBT) technology is very popular in MVDC related conversion field because of its availability and popularity and a lot of research has already been reported, e.g. [12], [13]. Dual-Active Bridge (DAB) [14], [15] with its single and three phase variants and SRC [10], [16] are the two prevailing circuit topologies which are frequently reported in the literature. The Integrated Gate-Commutated Thyristor (IGCT), which is an alternative to the IGBT for hard switching applications, has already been tested in the DAB configuration [9] whereas resonant topologies open the opportunity for further research in the field. Typical single phase, half-bridge configurations of the isolated SRC and DAB converter configurations are shown in Fig. 1a and Fig. 1b respectively. Reverse Conducting Integrated Gate-Commutated Thyristor (RC-IGCT) (IGCT and an anti-parallel free-wheeling diode sharing the same wafer in one common package) is used as a switching element in both topologies.

At present, IGCT is a mature technology generally used in applications involving grid inertias, solid state circuit breakers [17], medium voltage rectifiers [18] and drives [19] etc. with over 1GW of installed power in various pieces of equipment [19]. Common aspects of the semiconductor operation in these applications is hard switching under large current loads and relatively low switching frequencies of up to 900Hz. Generally, the IGCT has been optimized over the years for high current hard switching applications [20]–[22].

The isolated SRC is one attractive DC-DC converter topology, offering the stiff output voltage characteristic in operation mode where the switching and resonant frequencies are close in value. The converter can be operated in above- or sub-resonant switching mode with sub-resonant operation offering the advantage of relatively lower turn-off losses. In case when the switching frequency is lower than the resonant, semiconductor devices in a bridge or half-bridge configuration of the converter are always turned off at the current level that is independent of the load but is only dictated by the magnetizing inductance of the transformer. Typical current and voltage waveforms for this operation mode are shown in the Fig. 3. By carefully tailoring the magnetizing inductance of the transformer, the turn-off current can be held low enough so that turn-off losses are kept at minimum.

In this mode of operation, turn-on is executed in a zero voltage switching manner, practically leading to zero turn-on losses. Considering two level switching cell, as an example, at the moment of turning off the top IGCT, conducting the positive output current (magnetizing current of the transformer only since the resonance has finished), the current is commutated to the anti-parallel diode of the bottom RC-IGCT (negative RC-IGCT current in Fig. 3). At this moment, resonance is started and the bottom diode current starts falling towards zero with relatively low di/dt . Output current is still positive but falls towards zero as well in order to change sign after the zero crossing. After the output current becomes negative, it is taken over by the bottom IGCT. This process causes the voltage drop over the whole switch to be equal to the forward voltage drop of the diode, so when the bottom IGCT starts to conduct current (negative output current), voltage across it is very low (e.g. -2V), practically leading to zero voltage turn-on.

In the hard switching applications, the turn-on losses are practically zero due to the clamp circuit necessary for the safe operation. One common application is the voltage sourced, 3-level Neutral Point Clamped (NPC) inverter, where two clamp

TABLE I: Double pulse test circuit parameters

Parameter	Value	Parameter	Value
D_{CL}	5SHX 1445H	C_{DC}	2.6mF
C_{CL}	8 μ F	L_{LOAD}	5.4mH
R_{CL}	2 Ω	IGCT	5SHX 1445H
L_{CL}	9 μ H	D_{FW}	5SDF 0545F
		L_{σ}	500nH

TABLE II: Reverse conducting IGCT data

	IGCT	Reverse Diode
Manufacturer	ABB	ABB
Model	5SHX 1445H	5SHX 1445H
Forward blocking voltage	5500V	5500V
V_{DC}	3300V	-
I_{TGQM}	900A	-
I_{FAVM}	-	170A
Threshold Voltage	1.65V	2.53V
Slope Resistance	2m Ω	4.3m Ω

circuits can be found: one for positive output voltage switching and the other for the negative (an example can be found in [23]). During the turn-on process, clamping inductor takes over the full DC-link voltage and the current rises at practically zero voltage drop over the IGCT.

As a conclusion, the turn-on losses of the IGCT can be neglected in both SRC and hard-switching operations. Added value of the SRC topology is that it doesn't require a clamping circuit for the protection of the diodes but the di/dt is naturally limited by the resonant tank present at the output of the bridge.

The remaining losses in the switches are conduction losses where the IGCT, being a thyristor type of semiconductor switch, offers the best performance i.e. much lower conduction losses than the IGBT of similar ratings [24].

Other than low conduction losses, the IGCT offers some more advantages over the IGBT [20], [25] which is currently preferred device in the majority of the proposed converter topologies. Higher short circuit failure mode protection capa-

bility in terms of limiting load integral and non-repetitive peak forward surge current, high reliability, large Safe Operating Area (SOA) and better utilization of the silicon wafer area (e.g. press-pack devices where the full circular silicon surface is covered by the IGCT, as opposed to the number of rectangular IGBT dies across the round surface of the package) allowing for the homogenous temperature distribution and thermal contact with the cooling surface. Some general aspects of the IGCT application in the future DC grids was presented in [26].

In order to fully utilize and successfully integrate an IGCT switch into the SRC topology working in the sub-resonant operating conditions, it is of great importance to know the IGCTs behavior when switching at relatively low currents. Knowledge regarding switching energy losses is important for overall efficiency estimations and the design of suitable cooling system. Turn-off power losses are one of the critical factors for defining the maximum switching frequency of the converter and the duration of the on/off transitions has the essential contribution in defining respective dead-times for avoiding the DC-link short-circuit.

Manufacturer datasheets contain very little to no information regarding the low current switching behavior. Turn-off delay time is given as a worst case scenario value. While this is acceptable for the turn-on delay time, turn-off delay time needs to be characterized for the purpose of future designs of the IGCT based SRC. Switching energy losses, although clearly defined for higher current levels, are sometimes missing information for the load currents much lower than the nominal value.

Low current switching behavior of the RC-IGCT device under hard-switching circuit conditions is presented and discussed in this paper. Firstly, waveforms are obtained using the Technology Computer Aided Design (TCAD) model of the semiconductor switch surrounded by the SPICE test circuit model. General behavior of the model representing the IGCT under the product name of 5SHX 1445H is observed and influence of the turn-off current and temperature is discussed. Energy losses and turn off delay time parameters are extracted, offering the extended information of the device under test.

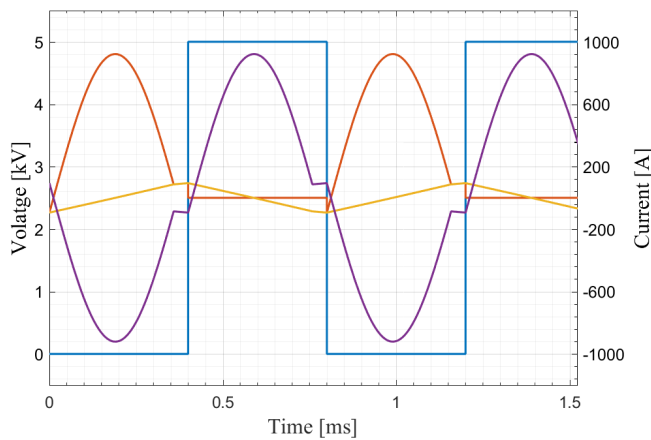


Fig. 3: Typical waveforms for the circuit in Fig. 1a; blue -RC-IGCT voltage, red - RC-IGCT current, purple - inverse resonant inductor current, yellow - MFT magnetization current

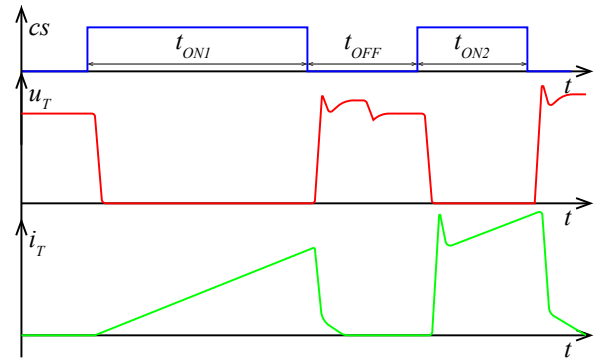


Fig. 4: Typical double pulse transient waveforms: cs - command signal, u_T - IGCT voltage with short commutation spike and longer clamping capacitor over-voltage, i_T - IGCT current with a diode reverse recovery spike

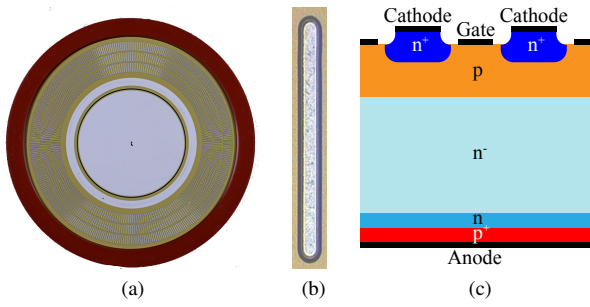


Fig. 5: a) RC-IGCT wafer b) single GCT finger c) vertical cross section of the GCT part. [20]

Validity of the TCAD transient model is confirmed using the experiment and the measured waveforms and estimated parameters are presented.

Section II describes the test setup with its detailed operation followed by Section III where a TCAD simulation model and simulation results are presented. Measured waveforms and experimental results are reported and discussed in Section IV. Finally, Section V summarizes the main findings of the paper.

II. TEST SETUP

The laboratory IGCT characterization test setup is shown in Fig. 2a. The complexity and the size of the test rig are explained by the fact that the setup is being used for (a) double-pulse, (b) single and double resonant-pulse as well as (c) for continuous resonant operation tests. The above test can be carried out under DC-link voltages of up to 5kV, a maximum continuous resonant current of 2.25kA for single and series connected IGCT devices with water cooling of the main switching elements.

The heart of the test setup is a 3-level NPC IGCT stack typically used in the medium voltage converters for industrial applications. It comprises of four press-pack RC-IGCTs and two external, press-pack diodes sandwiched together with water cooled heat-sinks in an alternating manner. The whole stack uses deionized water for cooling its elements. All the semiconductor switches are interchangeable, depending on the experiment that should be performed.

The right side of the cabinet is reserved for the air-cooled passive components required for different test conditions (variable resonant tank, variable load inductance, variable resonant capacitor) whereas the left cabinet contains device under test, DC-link capacitors with the protection circuit, IGCT clamp circuit and accompanying auxiliaries for power, control, monitoring and protection of the setup. The AC 800PEC, ABB's industrial controller unit with accompanying peripherals is used for the pulse generation, general monitoring and safety. Its interface with a PC allows for a safe and reliable way for the operator to define the pulse pattern and control the pulse release.

An industrial standard for characterizing the semiconductor switching devices is the double pulse test where the device under test can be turned on or off in a controlled and safe manner. Turn-on and turn-off waveforms of the current and

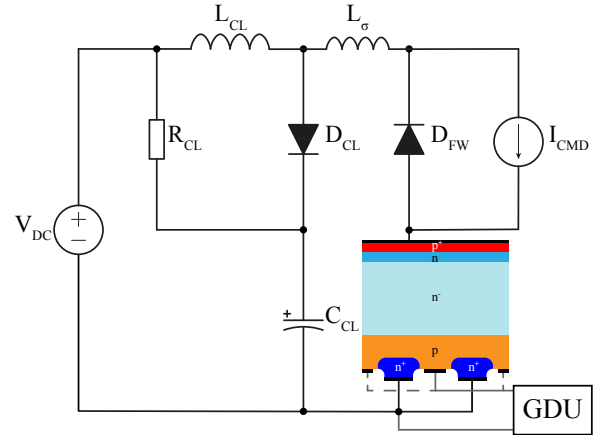


Fig. 6: Setup for multi-mode simulation: IGCT is simulated in a TCAD finite element manner while the circuit is being solved in a common SPICE environment

voltage of the switch are transformed by the means of respective high-precision transducers to the voltage signals ready to be fed into high-bandwidth high-resolution oscilloscope where digital data is acquired and saved for further analysis. Rate of the rise of current and voltage, respective overshoots, SOA conformity trajectories, switching losses and delay times are just some of the parameters that can be obtained with this test.

The circuit diagram for this particular test is presented in Fig. 2b with the parameters of the different components listed in the Table I and the details regarding the device under test given in Table II.

A typical pulse pattern for the double-pulse test is shown in the Fig. 4 with expected current and voltage waveforms of the device under test. Before applying the pulse pattern, DC-link capacitors (C_{DC}) and the clamp capacitor (C_{CL}) are charged to 2.5kV, the voltage level used for single device tests. The first, long turn-on pulse is then applied to the IGCT under test in order to build up the current through the load inductor (L_{LOAD}) to the level of interest for the experiment.

Duration of the first on pulse, t_{ON1} in Fig. 4, is calculated based on the desired test current level and should be long enough so that the carrier distribution along the semiconductor reaches equilibrium. The IGCT is then turned off, and the current of its branch is commutated to the free-wheeling diode D_{FW} to support the load current. In the same time, clamp inductor (L_{CL}) current starts to flow through the series connection of the clamp diode (D_{CL}) and clamp capacitor (C_{CL}). This fast transient results in the over-voltage (first over-voltage spike, Fig. 4) caused by the discharge of the magnetic energy stored in the parasitic inductance of the commutation loop. The process is then followed by the clamp inductor magnetic energy being transferred to the clamp capacitor (C_{CL}), increasing its voltage above the DC-link voltage level. The second and slower over-voltage transient measured across the IGCT is due to the C_{CL} charging and D_{CL} being forward biased until the current through the clamp inductor falls to zero. At this moment, D_{CL} becomes reverse biased by the difference in voltages between C_{CL} and the DC-link and

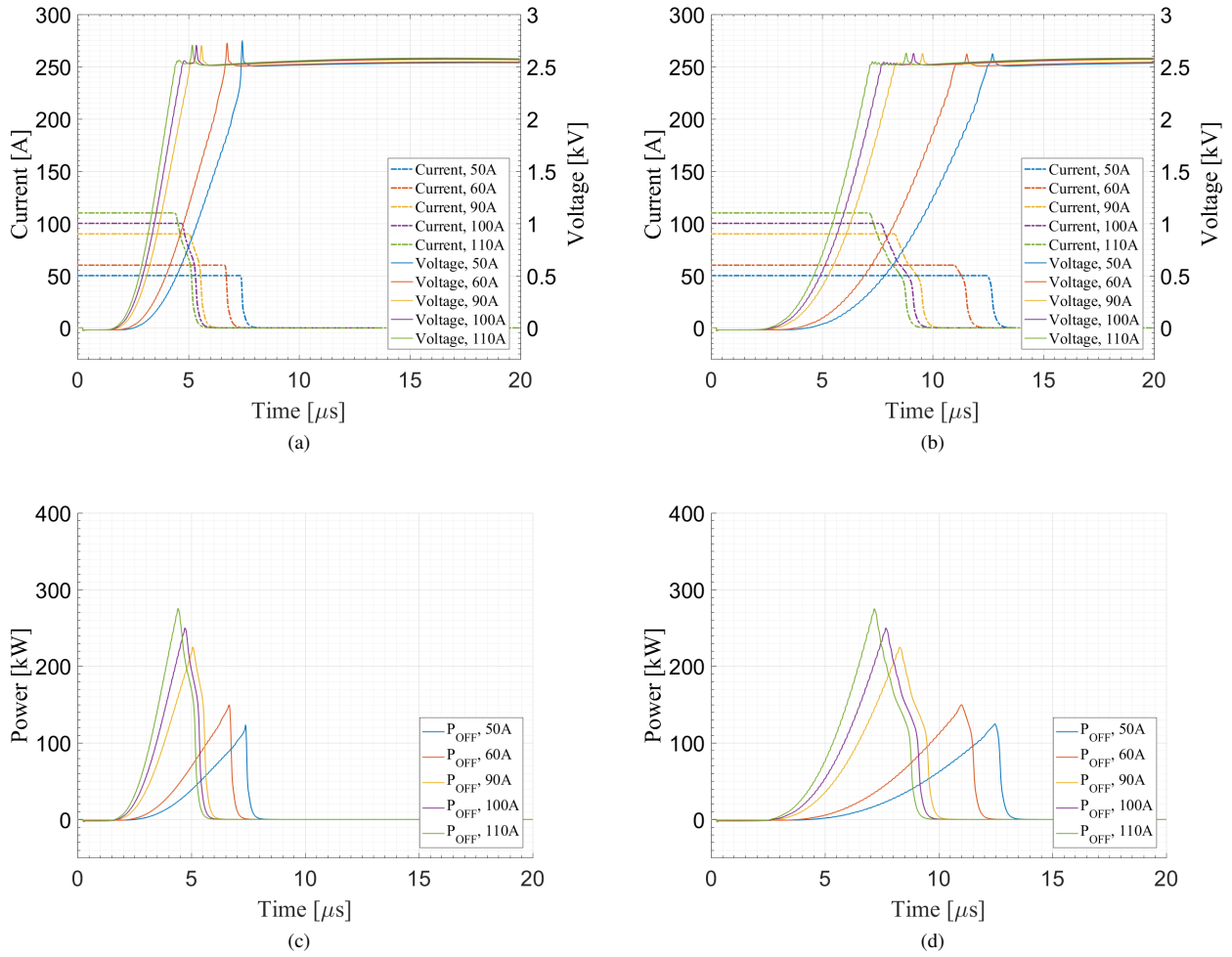


Fig. 7: a) TCAD simulated IGCT turn-off current and voltage waveforms at 30°C and 2.5kV b) TCAD simulated IGCT turn-off current and voltage waveforms at 115°C and 2.5kV c) TCAD simulated IGCT turn-off power losses at 30°C and 2.5kV d) TCAD simulated IGCT turn-off power losses at 115°C and 2.5kV

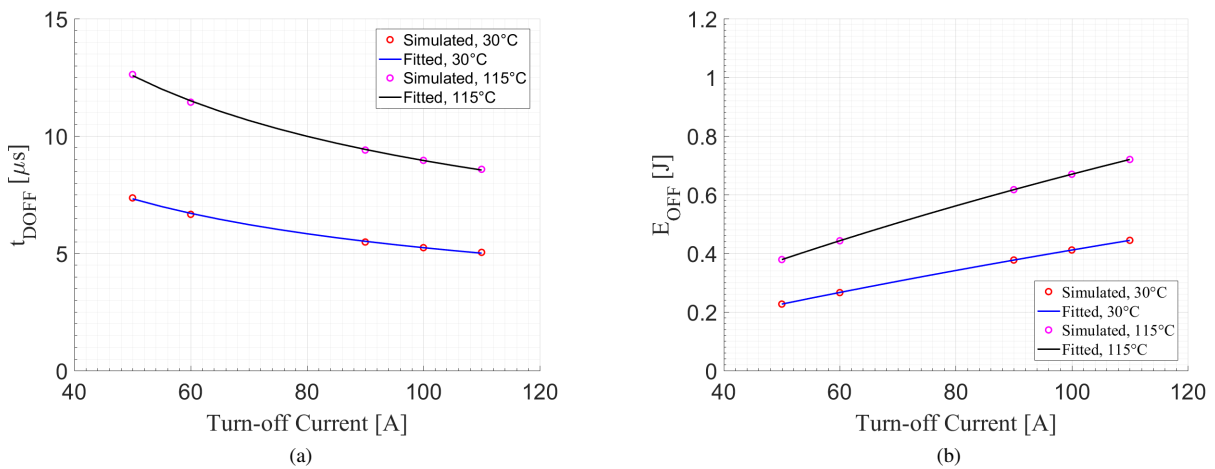


Fig. 8: a) t_{DOFF} estimated from the TCAD simulations at 2.5kV b) IGCT turn-off energy losses calculated from the TCAD simulations at 2.5kV

IGCT voltage becomes equal to the DC-link voltage while the C_{CL} continues to discharge to the DC-link capacitors through resistor R_{CL} , recovering some of the switching energy. The turn-off transient of the IGCT is recorded during the short commutation period.

After the IGCT turns off, the current of the load inductor flows through the free-wheeling diode (D_{FW}) and the IGCT is kept in the off state for a certain amount of time which is much shorter than the turn-on period. The duration of the off period, t_{OFF} , should be long enough so that the clamp circuit reaches steady state i.e. current through L_{CL} is zero and C_{CL} voltage is equal to the DC-link voltage. The minimum off time of the integrated gate driver unit should also be respected when defining the t_{OFF} (usually $40\mu s$). The IGCT is then turned on again for the predefined amount of time, t_{ON2} in order to record the turn-on transient as well. The turn-on current at this moment is practically equal to the turn-off current.

The current rise through the IGCT is limited by the clamp inductor (it cannot be controlled by the gate unit) and at the same time, through the free-wheeling diode D_{FW} protecting it from an excessive di/dt. The voltage across the IGCT falls to zero much before its current builds up since all of the DC-link voltage is present across the clamp inductor, providing nearly zero turn-on losses. When the IGCT takes over the load current, the diode D_{FW} starts its reverse recovery process which is observed as a current spike in the IGCT's current waveform. After D_{FW} turns off, current through the load inductor starts rising again during the period t_{ON2} . Minimum on time of the integrated gate driver unit should be respected here to allow for the safe turn-off (usually $40\mu s$, same as minimum off time). After the second turn-off, the IGCT is not pulsed again, and the load inductor's (L_{LOAD}) magnetic energy is dissipated on the free-wheeling diode (D_{FW}) and its internal resistance.

The described test, when executed for a predefined set of switching currents, different temperatures or different DC-link voltages, is a very safe and practical way for obtaining the device switching characteristics before implementing it in a final design.

III. TCAD SIMULATIONS

Along with the test setup, a TCAD simulation model of the IGCT, corresponding to the device in the test setup, was developed and provided by the industrial partner. This software simulation tool uses the finite element method for solving the fundamental partial differential equations (transport and diffusion equations) that model the silicon wafer of the switching device. Additionally, it is possible to interface the TCAD model of the IGCT with the SPICE model of the surrounding circuit of interest which provides great insight into the internal semiconductor behavior under the given circuit conditions.

Geometry of the finite element problem is based on the simplified geometry of the IGCT device, part number 5SHX 1445H, later employed in the physical test setup. Fig. 5a shows the typical IGCT wafer outside of its press-pack package with its surface covered by many stripe-like GCT fingers, and the gate drive contact ring at half a radius distance from center.

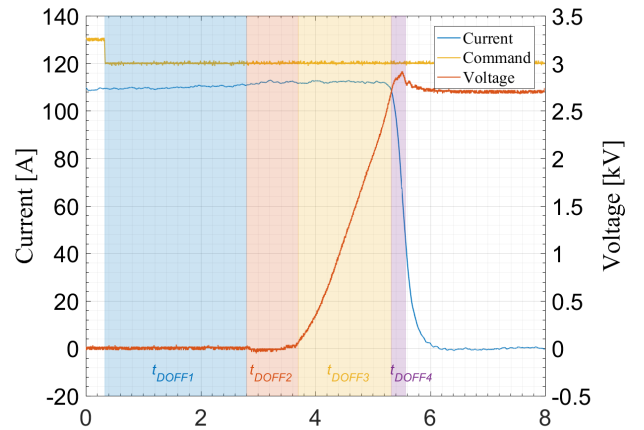


Fig. 9: Definition of the t_{DOFF} sub-periods.

Fig. 5b shows one of these fingers zoomed in, where the metal contact of the cathode terminal can be identified. Vertical cross section of two adjacent fingers is presented in Fig. 5c which was used as the base for the development of the TCAD model. In order to decrease the execution time of the TCAD model, only one half of the finger's vertical cross section is considered. Implementation of the full IGCT geometry would be very time consuming in terms of implementation and execution, without considerable gain in the model's accuracy. Only one quarter of the geometry presented in Fig. 5c is implemented in the 2D model, with symmetrical boundary conditions defined along the left and right edges. Final values of the full IGCT wafer are then obtained by using proper upscale coefficients.

It should be noted here that Fig. 5c shows only the basic idea of the IGCT cross section and is not to scale with the actual device. True geometry and doping profiles of the switch could not be presented due to the confidentiality of the data.

The TCAD model is later nested within the SPICE circuit as shown in Fig. 6, simulating the typical double-pulse behavior. As mentioned earlier, parameters for the TCAD modeled IGCT are set to correspond to the actual device used in the test setup with its basic details given the Table II. In order to resemble the actual test setup, SPICE model parameters are matched to the actual test setup parameters as listed in Table I. The diodes D_{FW} and D_{CL} are defined as ideal diodes in the SPICE model since the TCAD versions were unavailable, limiting the simulation to obtaining only the turn-off waveforms of the IGCT. IGCT turn-on current waveform, simulated with the ideal free-wheeling diode, would miss the typical current overshoot coming from the reverse recovery of the D_{FW} . Absence of the reverse recovery spike would provide wrong current waveform and cause an underestimation of the turn-on losses (which are already low due to zero-voltage turn-on).

The load inductor is modeled as a constant current source I_{CMD} , which is a good approximation for the time scales of interest. The commutation loop inductance is simulated by placing a lumped inductor L_{σ} in the commutation loop and

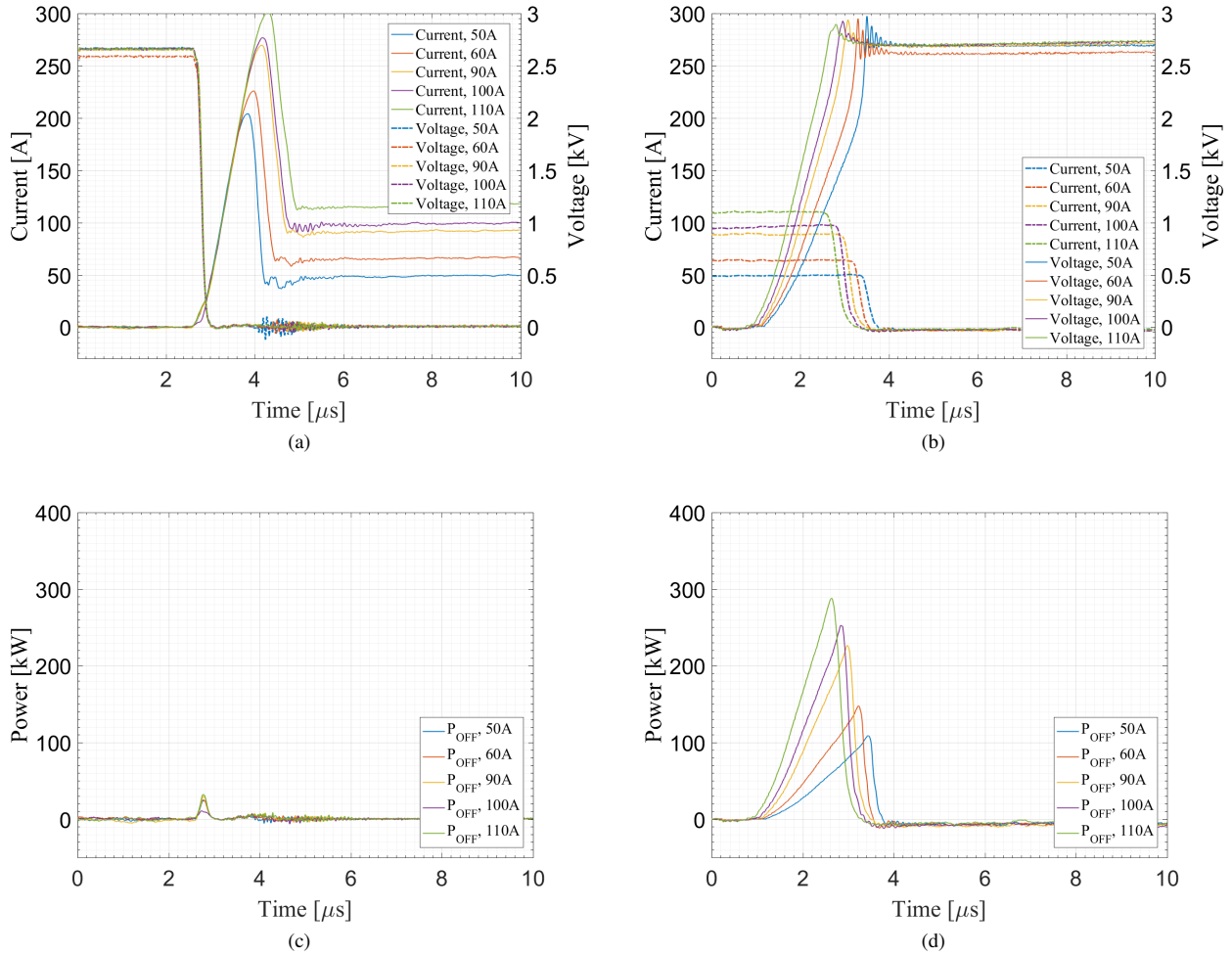


Fig. 10: a) Measured IGCT turn-on current and voltage waveforms at 30°C and 2.5kV b) Measured IGCT turn-off current and voltage waveforms measured at 30°C and 2.5kV c) Measured IGCT turn-on power losses calculated from the measured waveforms at 30°C and 2.5kV d) IGCT turn-off power losses calculated from the measured waveforms at 30°C and 2.5kV

its value is set to reflect the conditions of the actual test setup. Clamp circuit parameters also correspond the test setup and are summarized in the Table I. The DC-link is modeled as a constant voltage source, with a 2.5kV output voltage.

During the simulation runs, the turn-off current of the IGCT is varied under the two operating temperatures, 30°C and 115°C. The former initial condition is used to simulate the process under the start-up phase of the converter, later, to simulate device's behavior during the steady state operation. The DC-link voltage level is kept constant at 2.5kV in all cases.

Hard switched IGCT turn-off current and voltage waveforms are shown in Fig. 7a at 30°C and Fig. 7b at 115°C. These waveforms, representing one turn-off process at the particular switching current value, are plotted using the same color, offering easier identification to the reader. Both figures show the trend of prolongation of the turn-off process with the decrease in turn-off current value and generally slower turn-off transients at the higher temperature. Lower currents tend

to extract the charges from the drift region slower, whereas at higher temperature, extraction is slower due to the decreased mobility of charges. At the lowest value of 50A it can be noticed that the voltage increases its dv/dt abruptly due to the fast increase of the electric field in the n-drift region which happens due to the fact that low number of stored charge carriers from this region get extracted/recombined before the commutation of load current takes place.

Duration of the IGCTs turn off is described with the parameter t_{DOFF} - turn-off delay time, defined as the period of time between the moment of application of the turn-off command at the gate driver's optical input and the moment of the IGCT current falling to the 40% of the conduction current value at the time of the turn-off command application. The definition of the t_{DOFF} is set forth in the manufacturer's IGCT application note [27]. It should be noted that the t_{DOFF} period, as defined, includes four sub-periods, depicted on the experimental example waveform in Fig. 9:

- t_{DOFF1} is the period between moment when optical

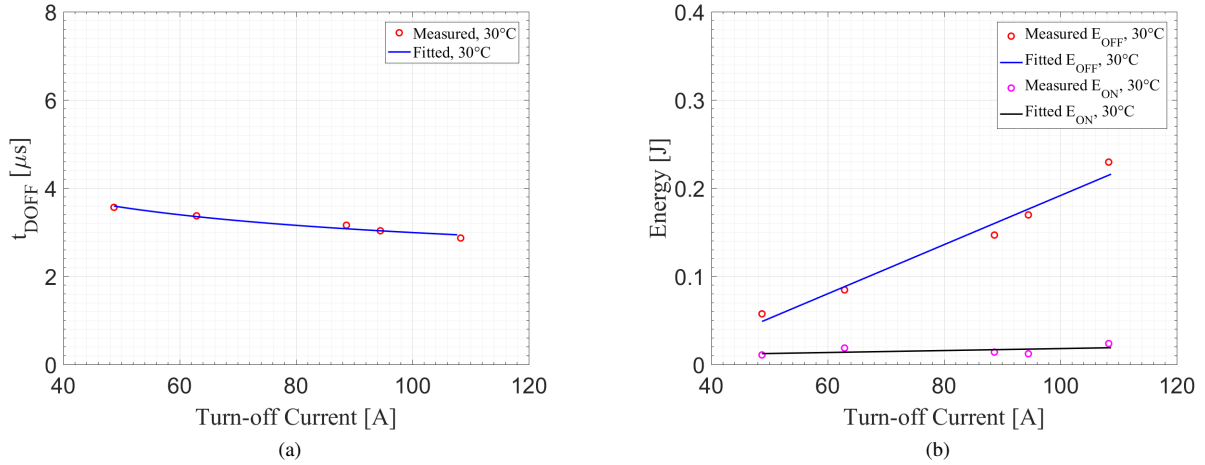


Fig. 11: a) t_{DOFF} estimated from the experimental waveforms at 30°C and 2.5kV b) IGCT turn-on and turn-off energy losses estimated from the experimental waveforms at 30°C and 2.5kV

- signal goes low until the gate unit applies a negative bias between the gate terminal and cathode (typically -20V);
- Second sub-period, t_{DOFF2} , is characterized by sweeping of the charges from the gate-cathode p-n junction until it becomes reverse biased and the whole cathode current is commutated to the gate driver. This period is usually called storage time and is characterized by the reverse recovery of the p-n junction followed by the tailing current that slowly decreases towards the load current value and the period ends when the gate current becomes equal to the load current;
 - After the storage time period is over, IGCT starts to behave as an open base transistor and depletion region starts forming in the central p-n junction expanding into the n-drift region. During this sub-period, t_{DOFF3} , a voltage starts to build up across the IGCT with dv/dt strongly dependent on the load current (capacitive behavior). The period ends when the IGCT voltage reaches the DC-link value;
 - Fourth and last sub-period, t_{DOFF4} , starts after the IGCT has reached the DC-link value and the anode current has started to decrease. di/dt of the anode current causes the over-voltage spike across the IGCT and the period ends when the anode current has reached 40% of the conduction current [27].

The turn-off current value mostly influences the third sub-period - t_{DOFF3} , recombination and/or carrier extraction, while the others are relatively independent of the turn-off current. Fig. 8a shows the t_{DOFF} graphs for both 30°C and 115°C temperature values.

The transient turn-off power losses of the IGCT, calculated as the product of the anode current and anode-cathode voltage drop, are shown in Fig. 7c and Fig. 7d for 30°C and 115°C respectively. The trend of increase of the power losses with the increase of the turn-off current is also evident. The turn-off energy lost during one turn-off transition is calculated by integrating the power loss curves from Figs. 7c and 7d, and

the results are presented in Fig. 8b for the two temperatures of interest.

IV. EXPERIMENTAL RESULTS

All the experimental data regarding the turn-on and turn-off switching is gathered at a temperature of 30°C and DC-link of 2.5kV. Higher test temperatures could not be achieved because of the lacking of the heating elements on the device under test. The test waveforms are organized in a way so that they correspond as close as possible to the TCAD simulation waveforms.

Turn-on current and voltage waveforms are presented in Fig. 10a with the zero on the time axis representing the moment of the turn-on signal being applied to the IGCT gate driver input. Transient voltage behavior in terms of delay and fall time, shows no correlation with the value of the current being turned on. Same is observed with the rate of change of current, being limited only by the clamping inductor (L_{CL} , Fig. 2b). A relatively high current spike is observed due to the reverse recovery of the free-wheeling diode (D_{FW} , Fig. 2b), which is slowly increasing in value as the turn-on current increases. The turn-on power losses shown in Fig. 10c are negligible due to the clamp circuit slowing down the turn-on process in order to protect the free-wheeling diode during its turn-off.

In the hard switching applications of the IGCT, a clamping circuit is required. During the turn-on of the IGCT, its gate driver is unable to control the di/dt of the anode current, in contrast to that of the IGBT. The excessive di/dt during the IGCT turn-on in a clamp-less circuit would be fatal for the free-wheeling diodes which turn-off during this time. The role of the external clamping inductor L_{CL} is to lower the di/dt value to an acceptable level that free-wheeling diodes are designed for. Since all the DC-link voltage appears across the clamp inductor during the IGCT turn-on process (Fig. 10a), IGCT's voltage is practically zero during this period and the zero-voltage switching is achieved.

Fig. 10b shows the low current turn-off event of the IGCT. Correlation between turn-off current and the rate of change of the IGCT blocking voltage is evident and positive in this case i.e. higher the turn-off current, higher the rate of change of the blocking voltage. High frequency ringing is present in the voltage waveforms at very low turn-off current levels due to the abrupt build-up of the electric field in the n-region of the IGCT body (dv/dt suddenly increases) caused by fast extraction/recombination of relatively low number of stored charge carriers. The overall duration of the turn-off process shortens as the turn-off current increases. This behavior is described by the turn-off delay time graph, t_{DOFF} in the Fig. 11a. Power losses of the switch are presented in Fig. 10d, increasing as the turn-off current increases.

Energy losses during the turn-off and turn-on period are plotted as graphs in Fig. 11b where a positive correlation between turn-off current and the turn-off energy losses is clearly visible. The same figure shows the turn-on energy losses being significantly lower than the turn-off losses, justifying the fact that the turn-on losses could be neglected during the design phase of the SRC including the IGCT as the switching element.

Analyzing the obtained results in contrast with a typical hard switched application of the IGCT under test (4.6J for 900A turn-off), it can be noticed that much lower values of the energy losses are obtained. Even though the switches in the SRC turn-off in a hard switching manner, the load current in that instant is much lower than typical and significantly brings down the turn-off energy losses. Further, this means that by predefining the low turn-off current in the design stage of the SRC, low turn-off energy losses are to be obtained during the normal operation of the converter and depending on the application requirements of the SRC, low switching losses present the designer opportunity to have a very efficient circuit switching at a relatively low frequency, or a very compact converter switching at a relatively high frequency. Increase of the switching frequency, offered on the account of low turn-off energy losses, is also limited by the turn-off duration of the IGCT. As the turn-off period of the switch (t_{DOFF}) increases, maximum switching frequency of the SRC decreases so the trade-off between the high switching frequency and low turn-off energy losses has to be made. This discussion goes beyond the scope of this work and will be presented in the future.

Comparing the experimental results and the TCAD simulation data, differences in the parameters are clearly noticed. It should be noted that the simulations are to provide a qualitative trend of the IGCT performance at low currents and not quantitative i.e. it was never intended to perfectly match the two sets of the results. Qualitatively, the trends match and very close estimate of the device behavior through simulations is achieved. The charge in the models depends on the anode injection efficiency and its temperature coefficient and lifetime model which will be very hard to match under all operating conditions. To get the exact match, the model will have to be re-calibrated only for lower currents.

V. CONCLUSION

Hard switching behavior at low currents of the IGCT is presented in this work inspired by the need to understand performance of the device under these particular conditions. TCAD simulation results are backed up by the experimental data obtained from the dedicated test setup. Simulation waveforms correctly predict the semiconductor's behavior with more conservative parameters extracted. Turn-on and turn-off transients are discussed along with its impact in the application of the IGCT in the SRC. Very low turn-off losses coupled with zero voltage turn-on allows for the increase of the switching frequency of the prospective SRC used as a DC-DC transformer. On the other hand, low current in combination with high temperature prolongs the turn-off period rendering increased requirements for dead time selection in the final converter design, potentially limiting the increase of the switching frequency. During the converter design process, the worst case scenario t_{DOFF} and E_{OFF} curves should be used while the typical ones should be used for the efficiency estimation. Technology curve of the IGCT can also be tailored in collaboration with the device manufacturer to meet the design requirements. Further work will report on IGCT performances in the high power resonant DC-DC converter, currently undergoing design.

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