Negative Resistance in Cascode Transistors

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***Abstract*—Cascode topology which includes a high-voltage GaN and a low-voltage Si transistor is an attractive device concept, which uses the low ON-resistance of GaN while still being compatible with Si gate drivers. It demonstrates the highest threshold voltage among normally-OFF GaN devices, which is a favorable feature in power electronics. However, the observation of instability in power circuits using cascode devices highlights the need for a careful analysis to reveal the origins of this phenomenon, to fulfill the unique feature of these devices in high efficiency and reliable power converters. In this letter, we demonstrate the presence of negative resistance in cascode devices, which explains the previously reported large-signal instabilities. We describe a theory to characterize this negative resistance behavior based on the sub-threshold-voltage operation of the high-voltage GaN transistors, and propose guidelines to resolve this issue in cascode devices. Negative resistance behavior, although not favorable for a power transistor, is of great importance in high-frequency electronics, with applications in reflection-type power amplifiers. These results, together with the presented analysis, could inform the development of high-stability, low-loss devices for future efficient power converters.**

***Index Terms*—Cascode, normally-OFF, GaN, Si, negative resistance, divergent oscillations, instability.**

I. Introduction

HIGH-ELECTRON-MOBILITY transistors (HEMTs) based on AlGaN/GaN heterostructures offer an outstanding potential for power applications, thanks to superior material properties such as a large critical electric field and high electron saturation velocity. These properties lead to design of power devices with high voltage ratings and low ON-resistance (R_{ON}) [1]. AlGaN/GaN power HEMTs, however, are naturally normally-ON (d-mode), which is not favorable in power electronics. Therefore, several techniques – such as fluorine plasma treatment [2], p-GaN gate [3], gate recess [4] – have been proposed to achieve normally-OFF (e-mode) operation. Decreasing the ON-state current and increasing the R_{ON} are potential drawbacks of these techniques. Furthermore, the threshold voltages of e-mode GaN transistors are considerably smaller than those of Si and SiC devices, which is unfavorable for safe operation, and also requires adapted gate drivers.

Cascode configuration that includes a high-voltage, post-process-free, normally-ON GaN HEMT and a low-voltage, Si MOSFET enables normally-OFF operation, with a high threshold voltage compatible with Si and SiC gate drivers [5].

Recently, dynamic measurements have revealed some potential drawbacks of cascode configuration, such as higher charging/discharging output capacitance (C_{OSS}) losses [6], [7], and instabilities under high-switching currents [8], [9]. These issues must be resolved to fulfill the attractive aspects of these devices in efficient power converters. In particular, Huang *et al.* [8] reported amplification of ringing voltage, so called *divergent oscillations*, following turning-OFF switching events of the cascode transistors, which eventually causes device failure due to overvoltage.

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In this work, we demonstrate negative resistance in the OFF-state of cascode GaN devices, which causes large-signal instabilities in the device operation. We also show how the frequency range of negative resistance changes with device area (*i.e.,* current capability). Finally, we provide an explanation for this negative resistance, and present guidelines for eliminating the issue. These observations are also of great interest for new device concepts featuring negative resistance, and for applications such as reflection-type RF amplifiers [10].

II. Experimental Observations

Impedance of several commercial 650-V and 900-V-rated cascode transistors (Table I) was measured using a Keysight E4990A 50-MHz high precision impedance analyzer (Fig. 1a). The tool biases the device under test (DUT) at a certain DC level, and using phase-sensitive voltage and current measurements, measures the impedance of the DUT. The method can be used for circuit modeling of any active or passive components [7]. The devices were characterized in their OFF-state by shorting gate and source. Based on the measured impedance, we extracted the output capacitance (C_{OSS}) and series resistance (R_S) of devices at different frequencies and voltage biases.

Fig. 1b shows C_{OSS} versus drain-source voltage (V_{DS}) measured at 1 MHz, although measurements at other frequencies (100 Hz to 10 MHz) yield almost the same results. From $V_{DS} = 0$ up to $V_{DS} \sim 20$ V, the high-voltage GaN transistor (HV-GaN) is ON (Fig. 1c) and the voltage stress is held by the low-voltage Si MOSFET (LV-Si), resulting in a gradual reduction of its output capacitance (C_{OSS}^{Si}). Just after $V_{DS} \sim 20$ V, the positive bias at source of the GaN transistor builds a negative bias on its gate-source voltage, which is large enough to turn OFF the transistor. At this point, the output capacitance of the GaN transistors (C_{OSS}^{GaN}) acts in series with C_{OSS}^{Si} (Fig. 1d),

TABLE I
SPECIFICATIONS OF EVALUATED CASCODE GAN/SI TRANSISTORS

Device	Voltage and current rating		R_{ON}**
	Voltage (V)	Current* (A)	(mΩ)
A	650	35	35
B	650	50	50
C	650	72	72
D	650	150	150
E	900	170	170

* Continues current at 25 ºC. ** Effective dynamic R_{ON} (typical)

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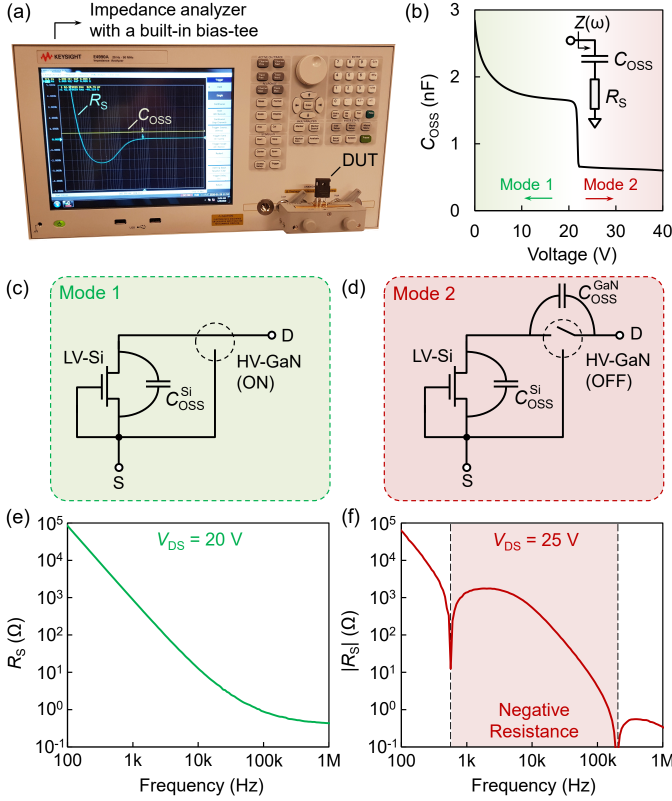

Fig. 1. (a) Measurement setup for acquiring the impedance under DC bias, utilizing a 50-MHz impedance analyzer. (b) Measured output capacitance of a 36 A cascode transistor (device B) versus bias level (V_{DS}). The measurements are very consistent with frequency (the plotted data corresponds to a 1-MHz measurement). The inset shows the device model that includes a capacitance C_{OSS} in series with a resistance R_S. (c) At zero gate voltage, for $V_{DS} < 20$ V (mode 1) the GaN transistor is still ON, and (d) it turns OFF for $V_{DS} > 20$ V (mode 2). (e) R_S versus frequency at $V_{DS} = 20$ V (mode 1). (f) Absolute value of R_S versus frequency at V_{DS}=25 V (mode 2). R_S is negative for the shown frequency range, however, the absolute values are plotted as a log scale is used.

resulting in an abrupt reduction in the total C_{OSS}. Figs. 1e and 1f show the real part of the measured impedance (R_S) versus frequency for V_{DS} = 20 V and 25 V, respectively. The device shows normal behavior up to V_{DS} ~ 20 V, when the GaN transistor is ON. The anomalous behavior of the device starts just after the GaN transistor turns OFF. As shown in Fig. 1f, the device displays normal behavior at very low frequencies, since C_{OSS} is almost open impedance, and the leakage current determines the R_S. For the considered transistor at V_{DS} = 25 V, for frequencies starting from 560 Hz, the device showed a negative series resistance, where the absolute values are shown in Fig. 1f. In this case, the negative resistance mechanism is observed up to 200 kHz. Such a negative resistance window could lead to circuit-level instabilities, since the device amplifies any oscillations in the aforementioned frequency range.

The negative resistance frequency window can vary at different bias voltages. The measured resistances of the device in the OFF-state for different bias voltages, from V_{DS} = 20 V to 28 V, are shown in Fig. 2a. The device starts showing a negative resistance from V_{DS} = 21 V (corresponding to a relatively small frequency window), and then it shows almost the same negative frequency window for larger voltages. The utilized impedance

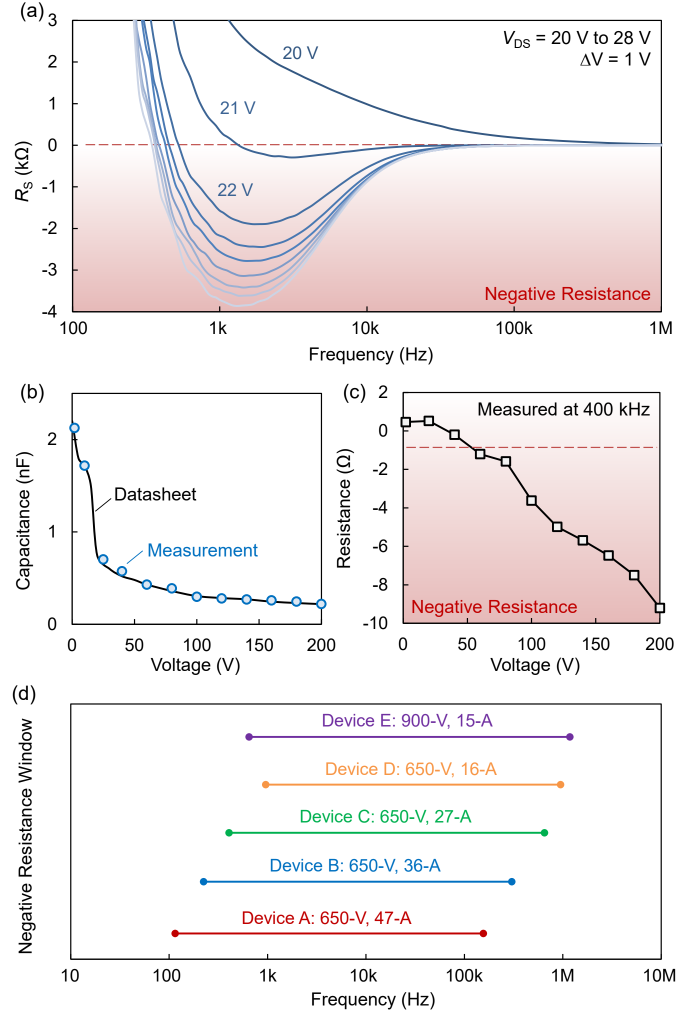

Fig. 2. (a) Measured R_S versus frequency for device B at different bias voltages V_{DS} = 20 V to 28 V (ΔV = 1) in linear scale. (b) Measured output capacitance at higher voltages up to 200 V using an external bias-tee together with reported data in datasheet. (c) Measured R_S at 400-kHz for voltages up to 200-V. The device exhibits a negative resistance with a higher magnitude for higher V_{DS}. (d) Negative frequency window measured at V_{DS} = 40 V for cascode devices with different voltage ratings and current capabilities (Table I).

analyzer can internally apply DC bias voltages up to 40 V. To perform measurements at higher voltages, we employed an external bias-tee. As shown in Fig. 2b, the measured capacitance up to 200 V is in agreement with data reported in datasheet, which shows the validity of measurements. The device exhibits an increased negative resistance at larger voltages (Fig. 2c). This is in agreement with the trend of R_S shown in Fig. 2a.

The negative resistance is observed for devices with different current rating values. Generally, devices with lower current capability show negative resistance behavior at higher frequencies. Fig. 2d presents the negative resistance window for devices with three different voltage and current rating values. For 650-V-rated devices, the frequency window shifts to higher frequencies as the current capability decreases. Comparing devices D and E – which have almost the same current capabilities, but different voltage rating values – shows a larger negative frequency window for the 900-V-rated device (E).

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III. Circuit-Level Consequences

The negative resistance observed in cascode devices potentially causes instability in electronic circuits. Fig. 3a shows a simple circuit including a cascode transistor connected to the voltage source V_{DD} through an inductor L, representing the parasitics outside and inside the package. The transistor is initially ON and it turns OFF (by grounding the gate electrode). After the switching event, the transistor can be modeled by a capacitance C_{OSS} in series with resistance R_S. After the switching event, the resonance frequency of the circuit (in this case $\omega_{res} = \sqrt{LC_{OSS}}$) is excited, resulting in a voltage ringing. For a cascode transistor, two scenarios might happen:

1) ω_{res} is outside of the negative-resistance frequency window. In this case R_S is positive (like a normal transistor) and the oscillations get damped [see Fig. 3b, top].

2) ω_{res} is inside of the negative-resistance frequency window. The negative value of R_S results in amplification of the oscillations, leading to self-generation of high-voltages over drain-source terminals [see Fig. 3b, bottom], and potentially to the device failure.

It should be noted that at $\omega = \omega_{res}$, the impedance of the RLC network is equal to R_S, resulting in a pure negative resistance. If there is a load R_L in series, the value of $R_L + R_S$ should be considered, which could be positive (stable performance) or negative (divergent oscillations).

Fig. 3c shows drain-source voltage and drain current of a cascode transistor, presented in [8]. This measurement clearly shows the negative resistance behavior for two main reasons. First, the oscillations get amplified, which corresponds to the scenario of $R_S < 0$ represented in Fig. 3b. Second, the local peaks in the voltage waveform and the local valleys in the current waveform happen at the same time. This shows that the transistor does not exhibit any capacitive or inductive impedance, but rather a pure negative resistance behavior.

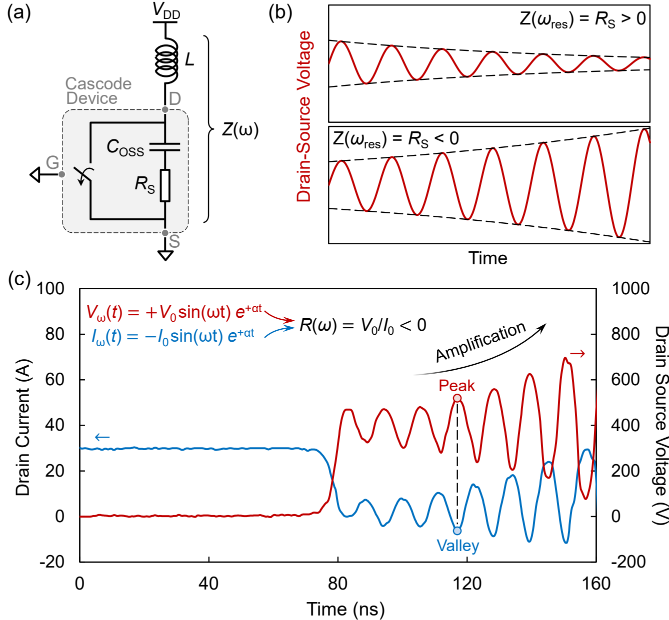

Fig. 3. (a) Circuit schematic to demonstrate the effect of negative resistance. (b) Drain-source voltage after switching event. In case of $R_S > 0$, the oscillations are damped, while for $R_S > 0$ divergent oscillations are observed. (c) Measured drain-source voltage and current of a cascode transistor [8]. The theory of negative resistance completely describes the previous large-signal observations.

IV. Theory

Fig. 4a shows a cascode transistor in the OFF-state, where the drain terminal is biased at voltage V_{DD}. A sinusoidal excitation at the frequency ω is applied to the drain terminal ($v_\omega = A\sin(\omega t)$) to extract the real part of the device output impedance (R_S). We assume that V_{DD} is high enough so that the GaN device is in the OFF-state. The pumping current from the sinusoidal excitation can be written as:

$$i_{pump} = \underbrace{\frac{A}{R_P^{Si} + R_P^{GaN}} \sin(\omega t)}_{\substack{\text{ohmic current} \\ \text{(real part of impedance)}}} + \underbrace{A\, C_{OSS}\, \omega \cos(\omega t)}_{\substack{\text{displacement current} \\ \text{(imaginary part of impedance)}}} \quad (1)$$

where R_P^{Si} and R_P^{GaN} are the parallel resistances of Si and GaN transistors (corresponding to leakage current), respectively. Since the current capabilities of the two devices are very close, their output capacitances are also in the same range. This can be observed in Fig. 1b, where after turning OFF the GaN device, the total capacitance drops to one-half. As a consequence, a considerable portion of v_ω (almost one-half) appears at the floating node (source of the GaN transistor). Therefore, the gate-source voltage of the GaN transistor can be presented as:

$$v_{GS} = -V_F - \frac{A}{2}\sin(\omega\, t) \quad (2)$$

where V_F is the DC potential at the floating point. Fig. 4b shows an equivalent circuit of the aforementioned structure, where the Si transistor is modeled by a high-impedance load Z_{Si}. As shown in this figure, and based on (2), the GaN transistor is biased at $-V_F$ and an excitation AC signal $-½A\sin(\omega t)$ is seen

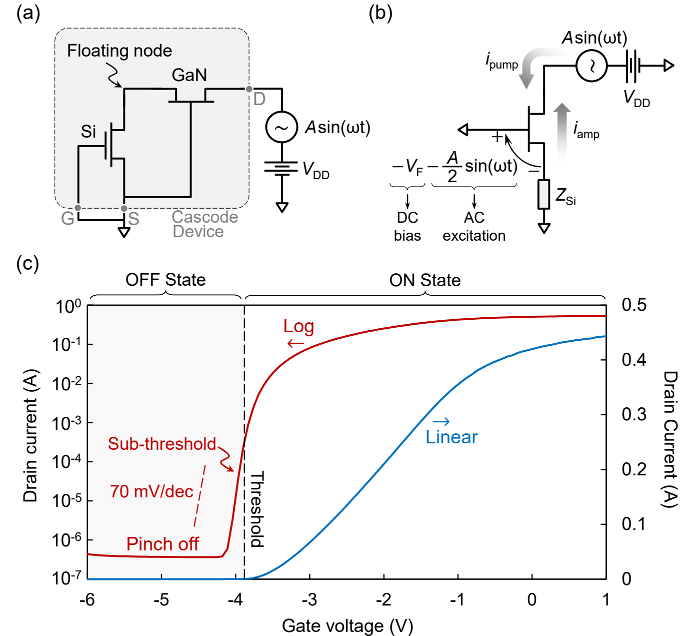

Fig. 4. (a) Cascode transistor in the OFF-state with output excitation. (b) Circuit model to evaluate the output impedance. (c) Transfer characteristics of a normally-ON GaN transistor presented with linear or log scales, showing the sub-threshold regime.

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over the gate-source terminals. The negative sign shows that the AC signal over gate-source opposes the applied signal to the drain terminal.

Fig. 4c presents the transfer function of a normally-ON GaN transistor, showing the threshold voltage of $V_{\mathrm{TH}} = -3.9$ V. As shown in this figure, the gate still has control of the drain current for voltages lower than V_{TH} (a so called sub-threshold operation) [11]. The operation point of the transistor is determined by matching the leakage currents in two transistors, since they are in series. Assuming the GaN transistor operates in the sub-threshold regime, and using (2), the drain current can be presented as:

$$i_{\mathrm{amp}} = I_{\mathrm{leak}} \exp(-\frac{A/2}{nV_{\mathrm{T}}}\sin(\omega t)) \tag{3}$$

where V_{T} is the thermal voltage, n is subthreshold swing coefficient, and the leakage current is equal to $I_{\mathrm{leak}} = V_{\mathrm{F}}/R_{\mathrm{P}}^{\mathrm{Si}}$. At room temperature, nV_{T} is larger than 60 mV, and typically lower than 100 mV. Considering a small-signal behavior for $A\sin(\omega t)$ with respect to nV_{T}, we write:

$$i_{\mathrm{amp}} = I_{\mathrm{leak}} - \frac{A/2}{R_{\mathrm{P}}^{\mathrm{Si}}}\frac{V_{\mathrm{F}}}{nV_{\mathrm{T}}}\sin(\omega t) \tag{4}$$

By comparing (1) and (4) and considering $nV_{\mathrm{T}} \ll V_{\mathrm{DD}}$, one can conclude that i_{amp} (which has a negative sign) is much larger than i_{pump} in amplitude. As a result, the summation of the two currents opposes the polarity of the sinusoidal voltage source, which corresponds to a negative resistance observed at the output terminals. In other words, the AC signal at the drain terminal of the cascode configuration appears on the gate-source of the GaN transistor through a capacitive feedback (C_{OSS}) and gets amplified by the GaN transistor.

Based on the presented analysis, one fundamental approach for mitigating the negative resistance is to match the leakage currents in the two transistors, so that the GaN device operates in the pinch-off region. Fig. 5 shows the drain current of GaN and Si transistors versus the voltage of the floating node. The intersection of two curves determines the voltage of the floating point. One GaN device together with three different options for the Si device have been considered. For Si MOSFET 1, the intersection point A shows that the GaN device operates in the sub-threshold regime, leading to negative resistance. By decreasing the leakage current in the Si device (or equivalently increasing the leakage current in the GaN device), an appropriate match between leakage currents can be achieved (Si MOSFET 2 with operation point B in Fig. 5). In this case, both devices operate at pinch-off. It is also possible for the Si device to operate at very shallow avalanche. Further decrease in the leakage current of Si device leads to a deep avalanche for this device, which is not favorable (Si MOSFET 3 with operation point C in Fig. 5).

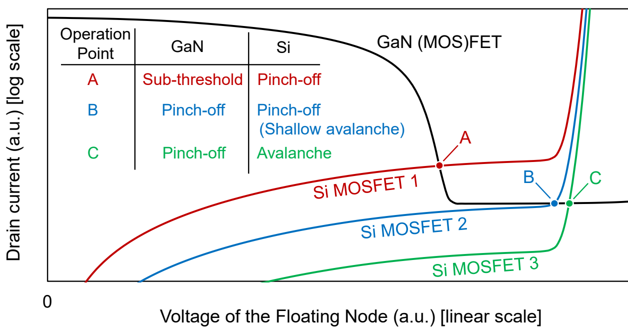

Fig. 5. Illustration of drain current of GaN and Si transistors, demonstrating different operation points for two transistors. The intersection point A shows that the GaN device operates in the sub-threshold regime, with a potential consequence of negative resistance. With an appropriate match of the leakage currents, both devices operate at pinch-off (point B).

V. Conclusion

We have demonstrated negative resistance in cascode GaN transistors, and showed its consequence in amplifying oscillations, which potentially leads to device instabilities and failure. According to our proposed theory, matching the leakage currents between two transistors (Si and GaN) to ensure that the GaN transistor operates at the pinch-off regime is a viable way to resolve the issue in the case of power converters. The results and considerations about leakage currents can be applied to any cascode-configured transistor. The presented behavior could be useful as an alternative approach to other negative resistance device concepts for achieving negative resistance behavior at much higher voltage levels, which is of extreme importance for high-power RF electronics.

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