Multi-channel AlGaN/GaN in-plane-gate field-effect transistors

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***Abstract*—In this letter, we present a multi-channel in-plane-gate field effect transistor (MC-IPGFET). In the proposed device, multiple vertically stacked two-dimensional electron gases (2DEGs) are simultaneously controlled by lateral in-plane gates formed with the same multi-2DEG stack. The multi-channel heterostructure allows to increase carrier density in the channel while keeping high electron mobility. Besides, the in-plane gate geometry provides an effective control of multiple channels with a smaller intrinsic gate capacitance. As compared to single-channel IPGFETs, multi-channel structure resulted in a three-time enhancement in current density and transconductance, offering opportunities for efficient scaling up of in-plane gate devices. High current density of 4.35 A/mm along with 2.05 S/mm transconductance are achieved in an optimized device. The effective control of the multiple high-mobility channels along with the reduced intrinsic capacitance of the in-plane gate open a pathway for new device concepts.**

***Index Terms*—In-plane gate, multi-channel, nanowires, GaN, III-Nitrides, HEMTs, 2DEG**

I. Introduction

MULTI-CHANNEL high-electron mobility heterostructures with low sheet resistance offer a promising platform for decreasing the on-resistance of high electron mobility transistors (HEMTs) without increasing the device footprint [1]–[4]. However, efficient electrostatic control of multiple channels by conventional top-gate structures is quite challenging and usually comes at the expense of low transconductance values due to a large negative V_{th} required to turn off all the channels by the top gate [2]. Thus, alternative gate geometries able to control and take advantage of high conductivity of multiple two-dimensional electron gases are of interest. In addition to the tri-gate [8], [9] (castellated FET [3], [4]) and double gate (BRIGEFET [5], [6]) structures reported in literature, we present a device that combines highly conductive multi-channel structure with in-plane gate geometry employing a pure lateral control of the channel: multi-channel in-plane-gate field effect transistor.

In an in-plane-gate field-effect transistor (IPGFET) [10]–[17], the 2DEG channels in a nanowire are actuated by means of an electric field applied on the sidewalls of the nanowire by lateral in-plane 2DEG gates (Fig. 1). All the metallic contacts are ohmic. In-plane-geometry offers an advantage in terms of lower intrinsic gate capacitance compared to planar, double- and tri-gates, and is proposed for high-frequency applications [10]–[14].

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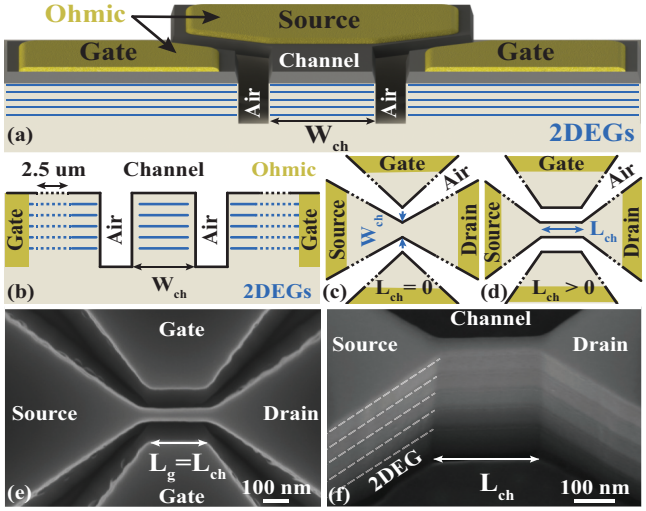

Fig. 1. (a) 3-dimensional schematic and (b) cut perpendicular to the channel of the multi-channel IPGFET; (c) top-view schematic of a 0 nm -long IPGFET and (d) top-view schematic of an IPGFET with non-zero channel length; (e) top-view and (f) 30°-tilted SEM image of a 250 nm-long and 60 nm-wide multi-channel IPGFET showing five stacked 2DEGs.

Single-channel IPGFETs based on III-V and III-N semiconductors reported in literature demonstrated efficient control of the channel by the side gates, along with high normalized transconductances (g_m) and current densities (I_d) [10]. For practical applications, the limited absolute current and transconductance in a single nanowire require a large number of parallel devices connected by air-bridges [25], which may lead to high parasitics. One of the ways to address this issue is by vertically stacking multiple 2DEGs within the same device channel which increases I_d and g_m of an individual device and thus reduces the amount of parasitics due to the interconnections.

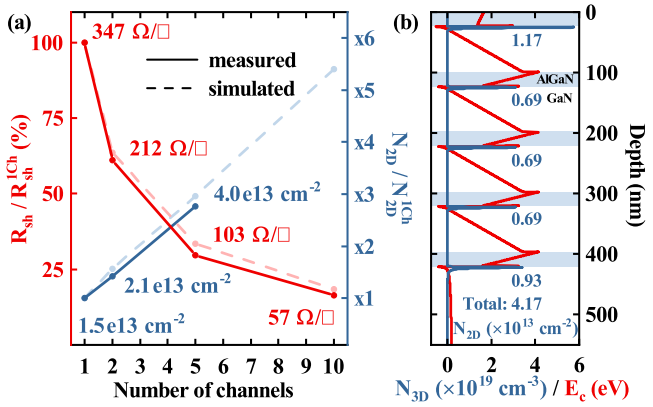

Fig. 2. (a) Measured (solid) and simulated (dashed) carrier concentrations and sheet resistances in different multi-channel structures. (b) Simulated band structure and carrier concentration (N_{3D}) of the five-channel wafer chosen for device fabrication. Sheet carrier concentration in each channel (N_{2D}) obtained by integrating N_{3D} in the quantum well is indicated.

In this work, we present a multi-channel in-plane-gate field effect transistor to efficiently and simultaneously control multiple parallel 2DEG channels. Optimized devices demostrated a 3-time increase in on-current density with almost no shift in threshold voltage compared to the best reported single-channel IPGFET [10], leading to 3.7x-gain in normalized peak transconductance. In addition, we numerically analyse the precise mechanism of the gate control in IPGFETs and identify the lateral electric field as the main source of the channel control in MC-IPGFETs.

II. Heterostructure Design and Device Fabrication

A series of multi-channel wafers with 1, 2, 5 and 10 periods of 23 nm $Al_{0.3}Ga_{0.7}N$ /1 nm AlN/ 75 nm i-GaN were grown over templates of 1.6 um i-GaN/ 300 nm AlN on 2-inch sapphire substrates. The sheet resistance (R_{sh}) was reduced from 347 Ω/sq for the one-channel structure to 57 Ω/sq for the ten-channel one, while preserving mobilities over 1400 $cm^2/V\times s$ for multi-channel structures.

Sheet carrier concentrations scaled linearly with the number of channels (Fig. 2(a)). Numerical simulations performed using material parameters from [18] and surface Fermi level from [19] revealed 3 types of channels present in each structure: top channel (influenced by the top surface, $N_{2D}=1.17\times10^{13}$ cm^{-2}), bottom channel (influenced by the buffer, $N_{2D}=0.93\times10^{13}$ cm^{-2}) and middle channels that always had the same $N_{2D}=0.69\times10^{13}$ cm^{-2} in each structure as no intentional doping is present (Fig. 2 (b)). The linear dependence of N_{2D} on the number of channels can be given by $N_{2D}(N)=[1.17+0.93+0.69\times(N-2)]\times10^{13}$ cm^{-2} from the simulated data, which is within 5% agreement with the experimental values (Fig. 2(a)).

The five-channel wafer offered a good compromise between total depth of the structure (500 nm) and low sheet resistance (103 Ω/sq) and has been chosen for device fabrication. Total N_{2D} of 4.03×10^{13} cm^{-2} along with mobility of 1650 $cm^2/V\times s$ were extracted from Hall measurements.

The IPGFET fabrication consists of only 2 major steps, resulting in inherently self-aligned structure. First, nanowire channel and gates are defined by electron beam lithography using 6% hydrogen silsesquioxane (HSQ) resist followed by Cl_2-based inductively coupled plasma (ICP) etching to isolate the gate mesas from the channel. The second step consists of deposition of ohmic contacts for source, drain and gate electrodes by one optical lithography followed by metal deposition, lift-off and annealing. A metal stack consisting of Ti (200Å) /Al (1200Å) /Ti (400Å) /Ni (600Å) /Au (500Å) is deposited by electron-beam evaporation and annealed at 860°C resulting in contact resistance of 0.6 Ω·mm extracted by transmission line method (TLM).

III. Experimental Results

A series of devices with nanowire lengths (L_{ch}) of 0 nm, 50 nm, 250 nm were fabricated. The gate length is always equal to channel length, as the access regions are much wider than the channel. All the devices show excellent simultaneous control

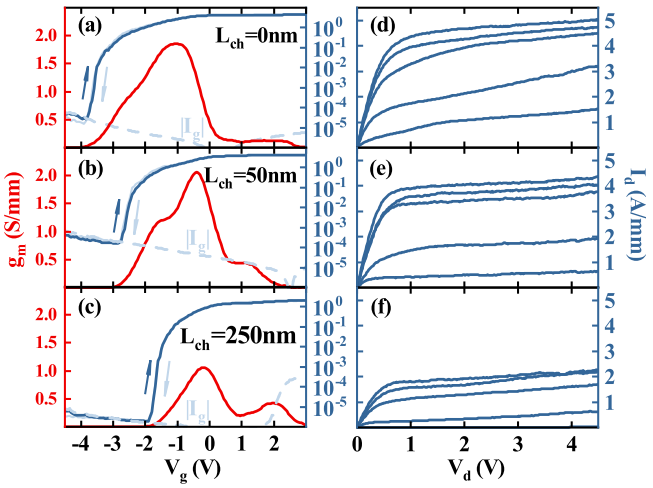

Fig. 3. Logarithmic scale double sweep transfer and transconductance at V_d = 5 V ((a) - (c)) and output characteristic at V_g = - 2 V: 1 V: 2 V ((d) - (f)) of devices with L_{ch} of 0 nm, 50 nm and 250 nm normalized to the nanowire width (63 nm, 35 nm and 67 nm correspondingly). Short (0 nm, 50 nm) channel devices show saturation current densities above 4 A/mm along with tranconductances above 2 S/mm.

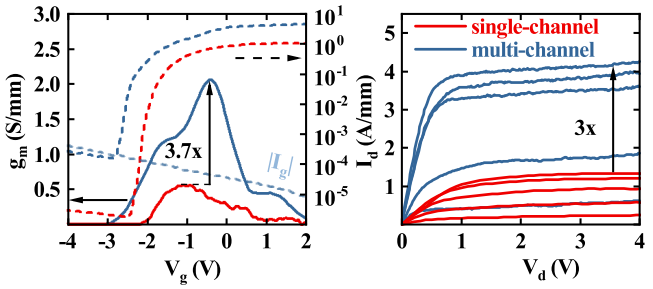

Fig. 4. Comparison between transfer (a) and output (b) characteristics of single- and multi-channel devices with L_{ch}=50 nm and W_{ch} of 40 nm and 35 nm correspondingly. Multi-channel device offers a 3.7-time gain in tranconductace and 3-time gain in saturation current density.

of all five channels with only one major transconductance peak (Fig. 3 (a) - (c)). Minor transconductance shoulders probably come from three different types of channels present in the structure (see section IV). A separate peak in 250 nm-long device at 2 V could come from one of the channels or might be caused by gate leakage that increases close to this point. The On/Off ratios for these devices were 10^5, 10^4, 10^6 respectively, and off-current was equal to the gate leakage, indicating good gate control at all lengths (Fig. 3 (a) - (c)). Even though no passivation or surface treatement was used, the hysteresis in all the devices was very small ($<$ 0.1 V, Fig. 3 (a) - (c)). The maximum drain current was reduced as wire length was increased, from 5.07 A/mm for a 0 nm-long channel to 2.27 A/mm for a 250 nm-long one (Fig. 3 (d) - (f)) as expected in a usual HEMT. The 50 nm-long device offers a good compromise between high current density and transconductance and serves for comparison with the reference single-channel IPGFET with the same dimensions from [10]. Multi-channel device delivered a 3-time increase in on-current (Fig. 4(b)) without major (less than 1V) shift in threshold voltage (Fig. 4 (a)) as compared to the equivalent single channel device. This increase corresponds to the 3.4x smaller sheet resistance observed in multi-channel wafer with respect to the single-channel one. A 3.7x increase in transconductance with respect to the equivalent single channel device (Fig. 4

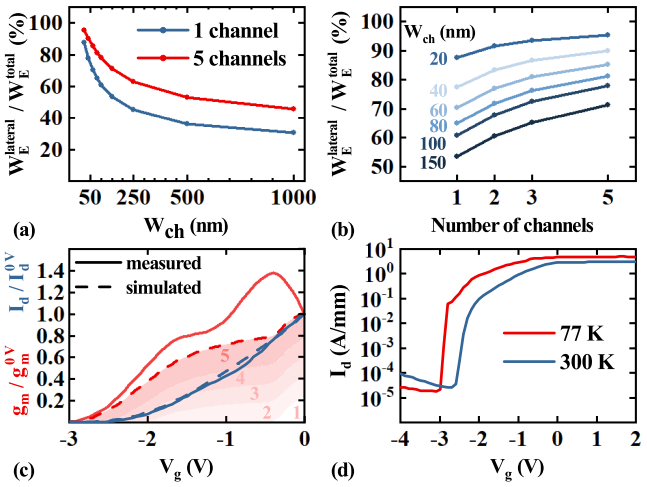

Fig. 5. (a) Fraction of the total electrostatic energy used for lateral control as a function of channel width for single- and multi-channel IPGFETs with gate to channel separation of 60 nm. (b) Fraction of the total electrostatic energy used for lateral control as a function of number of channels for different W_{ch} and gate-to-channel separation of 60 nm. (c) Simulated and measured transfer characteristics and transconductance of 50 nm-long and 40 nm-wide IPGFET normalised to the values at V_g = 0 V. The split of the total simulated transconductance in separate channels (1 - the bottom-most) is shown. (d) Transfer characteristic of a MC-IPGFET at room temperature and 77 K.

(a)) indicates no loss in gate control efficiency with respect to single channel. As compared to the best device reported in literature [10] (20 nm wide, 50 nm long, shallow etched), a 3-time gain in transconductance is observed.

The maximum absolute current of 320 μA and transconductance of 120 μS were achieved for a 0 nm-long 63 nm-wide device, which is 3.2- and 4- times higher than in a best single-channel IPGFET [10], which reduces by 4 the number of the devices needed for a given output current.

IV. Simulation Results

The possible mechanisms behind the control of IPGFETs include: in-plane field from gate 2DEGs [12]–[14], surface trap assisted control [20] and back-gating through the traps from the bottom [22]. The former is a quick mechanism giving rise to low capacitance of in-plane gates [11], while the others may lead to undesirable slow charging/discharging of buffer traps in poorly designed devices [23] and even to the total loss of control at low temperatures [20].

In a multi-channel IPGFET, bottom control should be less pronounced as the bottom-most channel screens the upper ones from a potential back gate. Moreover, vertical depletion of multiple channels is impossible with voltages below several tens of volts according to experimental data from [2]. To confirm this hypothesis we performed a numerical estimation of the fraction of electrostatical energy stored in the lateral part of device (mainly between gate and channel) $W_E^{lateral}$ to the total electrostatic energy (including the portion stored in the buffer and used for backgating) W_E^{total}. The ratio of the two above-mentioned energies is equal to the ratio of lateral-to-total capacitance coupling the gate and the channel, and quantifies the part of the control due to lateral field. As expected, the part of lateral control decreases with the channel width (for a fixed gate-to-channel distance of 60 nm in this case). However, as shown in Fig. 5 (a), over 80% of electrostatic energy is used for lateral control in five-channel IPGFETs with $W_{ch} \leq$80 nm. For single-channel devices only the 20 nm-wide device has the same ratio. For a given channel width, increasing the number of channels leads to an increase of the lateral control (Fig. 5 (b)). These results suggest that MC-IPGFETs are less prone to backgating from the buffer.

Furthermore, to prove that the pure lateral field-effect control can fully explain the performance of multi-channel IPGFETs, we have performed a 3D TCAD simulation using Silvaco ATLAS with the gate completely insulated from the channel by an ideal dielectric (no leakage allowed) eliminating the possibility of back gating. Previously used heterostructure parameters were unchanged except for the piezoelectric polarization that was adjusted to accommodate the strain relaxation occurring in small AlGaN/GaN nanowires [21], [24]. The average N_{2D} in the nanowire channel was monitored as a function of gate voltage (V_g) and normalized to the value at V_g = 0 V in order to compare with experimental data. Full depletion of the nanowire gives a linear scale V_{th}=-2.85 V, very close to the one observed in the experiment (Fig. 5 (c)). Moreover, we also simulated the variation versus V_g of the carrier density and transconductance due to each channel separately. When decreasing V_g the channels turn-off from top to bottom. The first one is the top-most (1st, V_{th}=-0.35 V), then comes the 2nd (V_{th}=-2.05 V), then very soon and simultaneously the 3d and the 4th (V_{th} = -2.3 V) , and, finally, the 5th (the bottom-most, V_{th}=-2.85 V, equal to the V_{th} of the device). The carrier distribution among channels at zero gate voltage was different due to the presence of the sidewalls that influence strongly carrier concentrations in such a small nanowire, but still 3 groups of channels were present: top, bottom and three very similar middle ones.

To exclude the surface trap assisted mechanism we have measured transfer characteristic of a MC-IPGFET at 77 K (Fig. 5 (d)). As opposed to [20] no loss of control was observed, only a slight shift of threshold voltage and a steeper subthreshold slope. A good agreement between experiment and simulation data allows us to conclude that the behavior of the multi-channel IPGFET can be explained by the lateral field-effect control of the channel.

V. Conclusion

In this work, we demonstrated multi-channel single nanowire IPGFETs. The multi-channel heterostructure provided increased carrier density while preserving high mobility, leading to current densities as high as 4.35 A/mm. The efficient control of the multiple-2DEG-channel by the in-plane gate resulted in 2.05 S/mm peak transconductance. The proposed device led to a 3-time increase in maximum current density and peak normalized transconductance as compared to the best previously reported IPGFETs. Numerical simulations and low temperature characterization suggest that observed behavior comes from the side field-effect control with no trap-related effects involved. Multi-channel IPGFETs offer an alternative way to control multiple highly conductive 2DEG channels and open a promising opportunity for new devices with increased current density and reduced intrinsic gate capacitance.

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