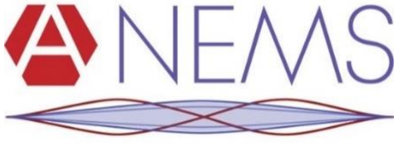

Fabrication and Characterization of MEMS Piezoelectric Accelerometers

Projet de Master – 2020 – Section de Microtechnique

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Lausanne – January 17, 2020
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Project Description

Vibration sensors (aka vibrometers) are essential components to keep safety and reliability of different types of machines, e.g. plane engines. A vibrometer is able to detect very small vibrations, coming from either acceleration caused at the clamp or by pressure variations in the environment. In the frame of aerospace industry, the extremely strict requirements for safety, resolution, endurance and lifetime have caused the technology to evolve very slowly. The idea of the project is to analyze if a MEMS based device would be of interest as the next generation vibrometers. Analysis of the different transduction possibilities, design and fabrication in the CMi cleanroom at EPFL will be performed.

Abstract

In this master thesis, the use of MEMS technology to miniaturize existing accelerometers used for vibration sensing is demonstrated. An updated process flow was established and carried out in the cleanrooms. MEMS piezoelectric accelerometers were fabricated and known fabrication issues were successfully avoided. A first characterization of the fabricated devices was done, and results show a strong agreement with the FEM simulations done during and before this project. FEM simulations were done for alternative designs and showed a possibility to almost double the charge generation of the accelerometers.

Acknowledgments

I would like to thank my supervisor, Prof. Guillermo Villanueva, for his support and guidance during this semester. His enthusiasm, humor and availability played a big role in making this project a great experience.

I am very grateful to all the members of the Advanced NEMS group; each one of them has helped me at some point during the semester and they made me feel very welcome in the group.

Jialiang and Maria Vittoria have been great fellow master students and I would like to thank them for their help and for keeping me company during long hours in the cleanroom and in the lab.

I also want to thank the CMi staff for their help during the fabrication and especially Adrien Toros for doing wire-bonding several times for me.

Lastly, I would like to thank my family and friends for their support, not only during this semester but also throughout my entire studies at EPFL.

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1 Introduction

1.1 State of the Art

Mechanical systems, especially rotating machinery like turbines, compressors and pumps are subject to a number of vibrations coming from their different parts which over time lead to mechanical failure. Condition monitoring of those systems, using vibration sensing, is necessary to predict failure and schedule maintenance before it happens. Measurements of those vibrations is often done using conventional piezoelectric accelerometers. In these accelerometers, a seismic mass moves when subjected to an acceleration and creates a proportional force on a piezoelectric element, deforming it. When deformed, the piezoelectric material will generate an electrical charge proportional to the force applied. Measuring the generated charge will then allow to know the corresponding acceleration [1].

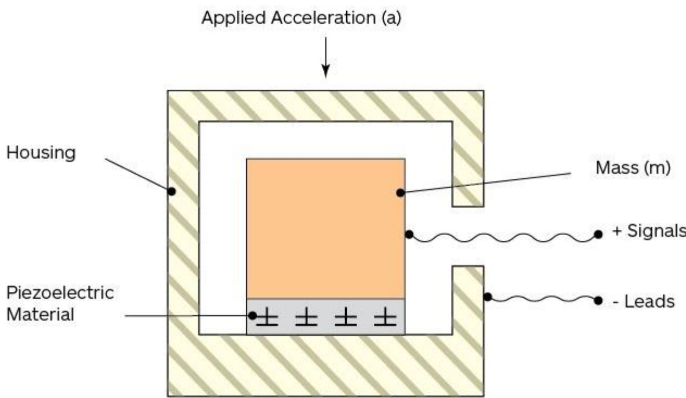

Figure 1: Representation of a piezoelectric accelerometer where the piezoelectric material is deformed in compression [16]

However, the cost of those accelerometers is high and they could be replaced by MEMS (Micro-Electro Mechanical Systems) accelerometers for an estimated 10 % of their cost [2]. This cost reduction is made possible by the fact that, due to their small size, MEMS can be microfabricated in large quantities at once [3]. Their size also allows to use them in applications where space is limited and may even allow for better sensing performances, namely a higher signal-to-noise ratio [4].

MEMS accelerometers, mainly piezoresistive and capacitive ones, are commonly used for vibration sensing in automotive and manufacturing industries. In piezoresistive accelerometers, a proof mass is accelerated and deforms a piezoresistor, provoking a change of resistance that can be measured (see Figure 2). Piezoresistive sensors are easy to manufacture and to use, but their sensitivity is small, meaning that a large proof mass is required, which limits their integrability. For capacitive accelerometers, the acceleration is known by measuring the change in capacitance between a fixed point and a proof mass (see Figure 3). Capacitive sensors have a high sensitivity and good noise performances and stability; however, they are susceptible to electromagnetic interferences [3] and often need to be vacuum sealed, which complicates the fabrication process [5].

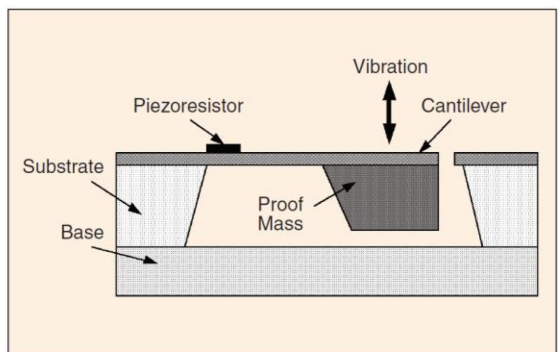

Figure 2: Piezoresistive accelerometer, with a cantilever configuration [3]

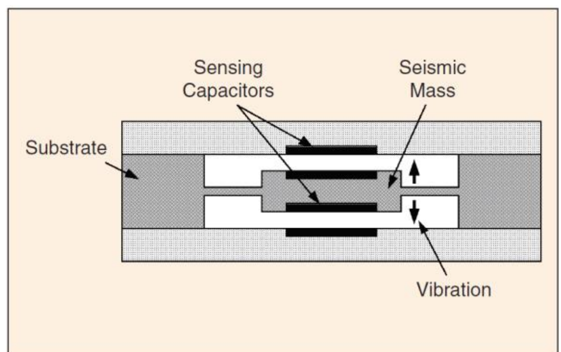

Figure 3: Capacitive accelerometer, with a membrane configuration [3]

MEMS piezoelectric accelerometers are of interest for vibration sensing application because of their large frequency response and linear amplitude ranges and their low power consumption [6]. Despite these advantages, piezoelectric MEMS have not yet been widely commercialized as their fabrication still poses some challenges. Depositing piezoelectric thin films with properties approaching those of the bulk material is one of them [7].

1.2 Context

Meggitt Switzerland, formerly Vibro-meter, has been producing piezoelectric accelerometers for over 50 years to serve as vibration sensors [8]. These sensors are used in several aerospace-related applications, like engine monitoring and gearbox analysis [9]. Miniaturization of this technology, while keeping the same performances, could allow for more precise monitoring and help reduce the manufacturing cost. This is achievable using MEMS technology, as we demonstrate in this project.

The overall project was started by Bradley Petkus during the spring semester of 2019 in his Master project [10], where he designed, simulated and fabricated MEMS piezoelectric accelerometers. However, he was unable to do any characterization as he encountered unexpected issues during the fabrication process.

Therefore, the project presented here continues this work by focusing on the updated fabrication and characterization of MEMS piezoelectric accelerometers.

Based on the fabrication issues presented in [10], a new process flow was established. Three wafers were processed and characterized. All the fabrication steps as well as most of the measurements done during the fabrication were done in the cleanrooms of the CMi (EPFL Center of MicroNanoTechnology). Characterization of the fabricated devices was done in the laboratory of the Advanced NEMS group.

In order to validate the use of FEM (Finite Element Modelling) as a reliable tool to design the accelerometers in this project, new simulations were done with the exact parameters of the fabricated devices to allow for direct comparison. Simulations for alternative designs were also conducted.

1.3 Previous Work

What was done in the work preceding this one can be summarized in 3 main parts: Study of the state of

the art, Finite Element Modelling and fabrication.

1.3.1 Study of the State of the Art

Existing MEMS accelerometer technology was studied to determine the best transduction method and geometry for the accelerometer. This led to choose piezoelectric transduction with charge output. The chosen geometry is a circular membrane with a centered proof mass that utilizes the bending mode for sensing. Figure 4 shows the design that was chosen.

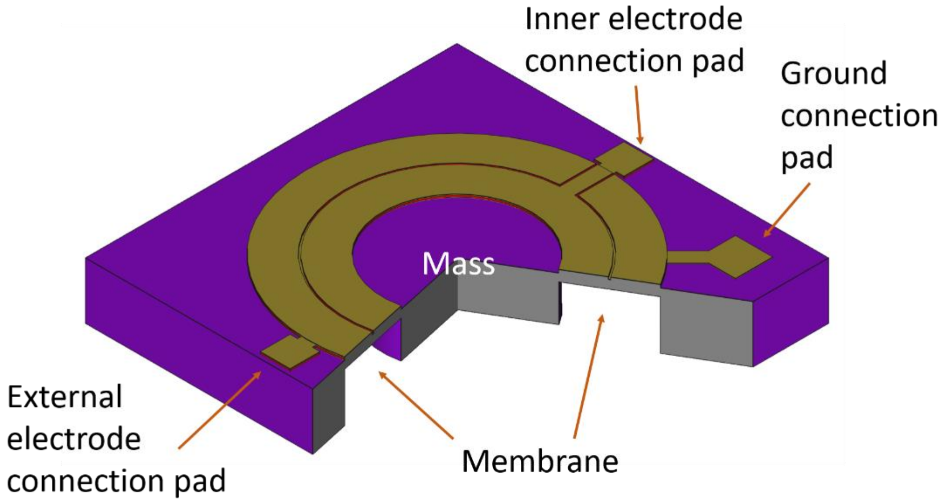

Figure 4: 3D cut view of the design of one accelerometer (thickness is scaled up for visibility). The purple color represents the patterned silicon substrate. The gold color represents the electrodes that are on top of the piezoelectric layer, as well as the pad of the ground electrode situated below it.

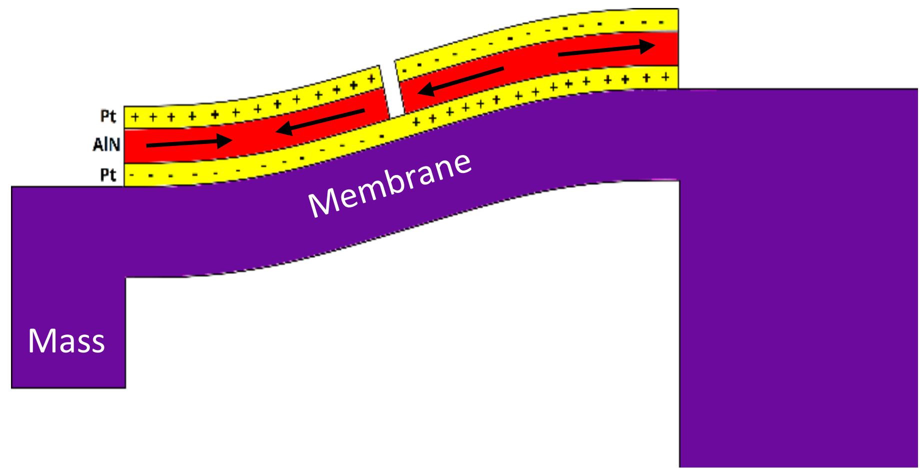

Figure 5: Cut view of half of the accelerometer. The yellow zone represents the platinum electrodes, the red zone the aluminum nitride piezoelectric layer. Arrows show the directions of the constraints on the piezoelectric layer. The generated charges are of opposite sign on each side due to the curvature of the membrane constraining the piezoelectric layer in opposite directions.

The working principle of this accelerometer is as follows:

When the device is subjected to an acceleration, the mass moves, which deforms the membrane. In turn, the deformation of the membrane constraints the piezoelectric layer, generating electrical charges that accumulate on the electrodes.

The ground electrode covers the whole surface of the membrane whereas the top electrode is separated in two inner and outer regions (see Figure 4). This design was chosen to avoid cancellation of charge as the inner and outer part of the electrode are constrained in opposite directions (tension and compression) when the membrane deforms and generate charges of opposite sign (see Figure 5).

This study also allowed to select aluminum nitride (AlN) as the material for the piezoelectric layer.

1.3.2 Finite Element Modelling

Finite element modelling was done in COMSOL to determine the optimal dimensions necessary to achieve the following performances:

- Low frequency applications: A resonant frequency of 1 kHz and a charge generation of 1 pC/g
- High frequency applications: A resonant frequency of 100 kHz and a charge generation of 1 fC/g

The parameters and resulting performances presented in the following table were found:

Parameters/Performance	Low Frequency Case	High Frequency Case
Membrane Thickness [um]	14	120
Mass Thickness [um]	350	350
Membrane Radius [um]	2000	2000
Electrode Thickness [nm]	50	50
AlN Thickness [nm]	100	100
b/a ratio [unitless]	0.5	0.5
Charge Generation [fC/g]	1068	21.2
Resonant Frequency [kHz]	6.42	115.1
Displacement Sensitivity [m/g]	6.12e-9	2.2e-11
Dynamic Range [g]	500	2000
Linearity [%]	3.03	0.01
Cross Axis Sensitivity [%]	< 0.01	< 0.01

Figure 6: Optimal parameters and resulting performances found by using FEM [10]. The b/a ratio is the ratio between the mass and the membrane radius. The charge generation gives the quantity of charges generated when the device is subjected to an acceleration of 1 g (9.81 m/s^2). The displacement sensitivity gives the displacement of the mass for 1 g

1.3.3 Fabrication

A process flow was established (Figure 7) and four wafers with different membrane thicknesses (to have

(a) Start	(b) Front side: Photolithography of GND Electrode Layer

different performances) were processed.

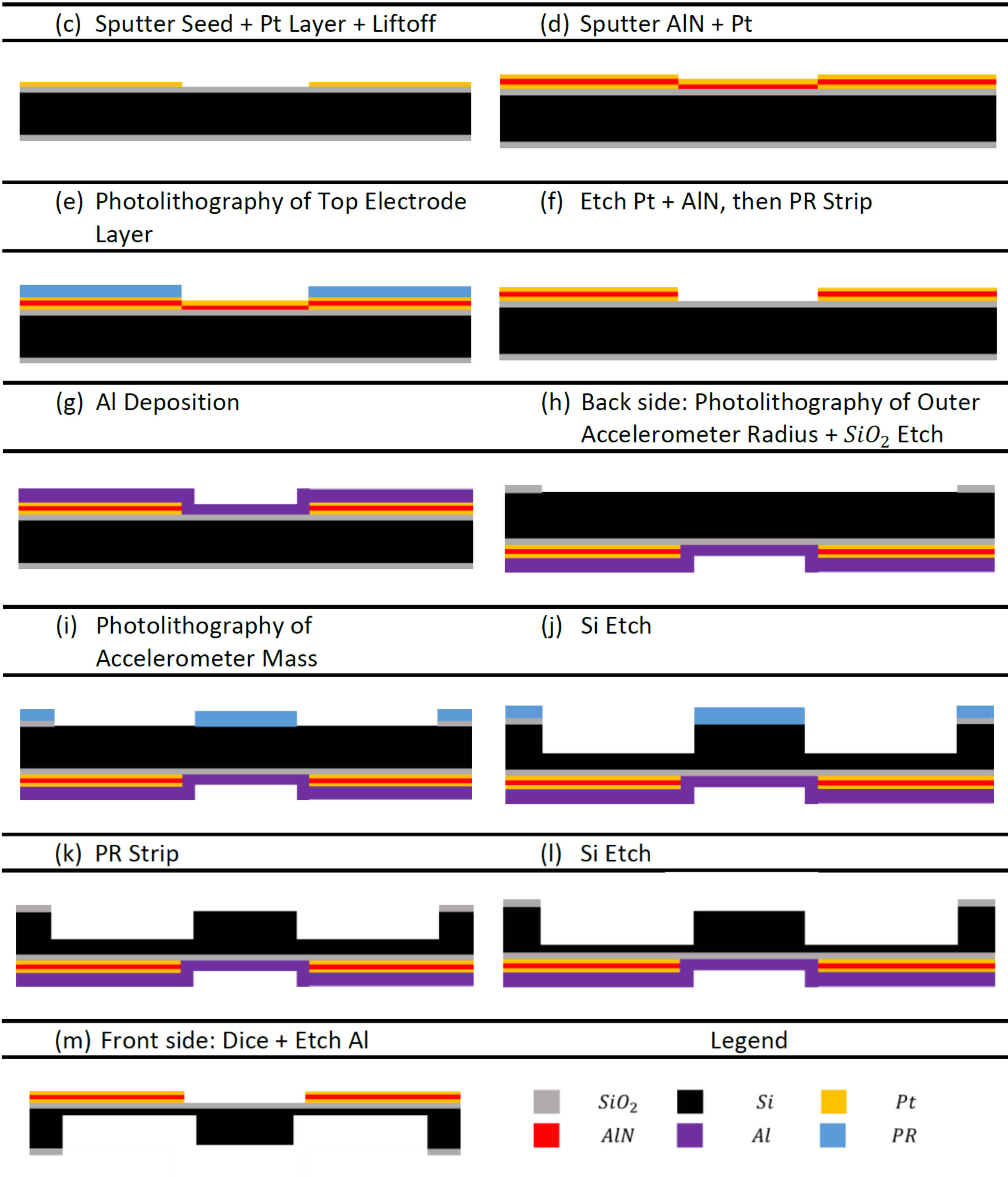

Figure 7: Process flow of the previous work [10]. The specifics of each step are detailed later

Some problems were encountered during the fabrication, resulting in none of the devices being characterizable. Issues reported are:

- Fencing, occurring during steps (c) to (f), resulting in a short circuit between the top and bottom electrodes.
- Over etching of silicon during steps (j) and (l) resulting in some devices being destroyed.
- Delamination of the top platinum layer after etching of the aluminum at step (m)

These issues, as well as the solutions implemented to avoid them, are explained in more detail in the next section.

2 Microfabrication

2.1 Known Issues

The main issue that made it impossible to characterize the devices fabricated by Petkus was the presence of short-circuits between the top and bottom electrodes. Those short-circuits were due either to fencing or to the presence of aluminum residues left after etching the protective layer at the end of the process.

Fencing is a phenomenon where fence-like structures remain on the edge of a structure patterned using dry etching (see Figure 8) or lift-off (see Figure 9 (a)). There are two steps in processing the accelerometers where the observed fencing could have occurred; when patterning the ground electrode (Figure 7, Step (c)) and when patterning the AlN layer and the top electrode (Figure 7, Step (f)).

Prior experience in the group [11] has shown that using reactive ion etching (RIE) to pattern the ground electrode results in fences that might create a contact between the ground and top electrode. Those fences are created by the etched material redepositing on the sidewalls of the photoresist mask, as illustrated in Figure 8.

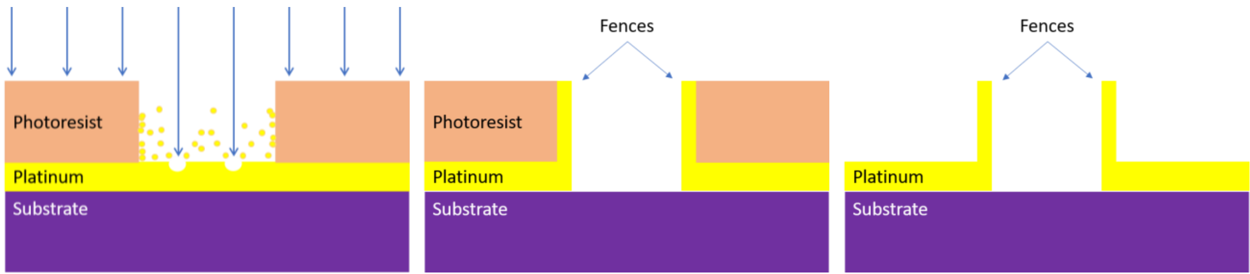

Figure 8: Fencing phenomenon during dry etching. During etching the etched material (here platinum) redeposits on the resist sidewalls, creating fences which remain when the photoresist is removed.

It is to avoid this issue that lift-off is used to create the ground electrode, allowing to do one less step of dry etching. But, as explained in [12], fences can also appear when lift-off is used in combination with sputtering and the sidewalls are coated during the deposition. To reduce the probability of fencing, a bilayer lift-off process, as illustrated in Figure 9, is used.

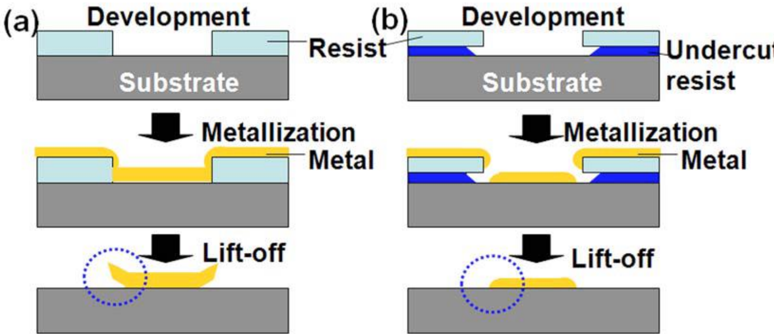

Figure 9: Single layer lift-off process (left) compared with bilayer lift-off process (right) [3]

In the bilayer process, two layers of resist are deposited, with the first one being a sacrificial resist that will get etched by standard developer, and the second one a normal photoresist. In our case AZ 1512 on LOR 5A[1] is used, as it is a standard process available at CMi. This process should help create fences-free structures. However, sputtering is the main issue and fences may still occur even with the bilayer lift-off process.

The fences observed in the previous work might also be due to the dry etching step coming after (Figure 7, Step (f)) and not to the lift-off. This etching step cannot be replaced by a lift-off step as the AlN layer has to be deposited at high temperature (Figure 7, Step (d)), which would damage the photoresist.

An important parameter in the creation of fences during dry etching is the resist used as a mask, especially the verticality of its sidewalls. Having walls that are less vertical helps to avoid the presence of fences because films redeposited on sloped walls tend to be thinner and will get etched away quicker as they are facing more towards the etching chamber [13, 14]. This explains why fences were observed in [10] as the resist used was AZ 9260, which has very vertical sidewalls. In this work, it was switched for AZ ECI 3007 which has sidewalls with an initial inclination of around 70-75 % and has been used before in the group with satisfying results.

The other possible cause for the short-circuits could be residues left behind after the etching of the aluminum layer used to protect the frontside (Figure 7, Step (m)). This potential problem will be avoided by using a parylene layer instead. This change might also help avoid delamination of the electrode when removing the protective layer.

Another critical step is the etching of the silicon in order to create the membrane and mass. In [10], it was observed that the etch rate was not uniform across the wafer and for different feature sizes. The average measured difference was a 6%[2] higher etch rate for a small feature on the edge of the wafer compared to a big feature in the center. This resulted in several devices being destroyed.

To avoid etching completely through the wafer when attempting to fabricate thin membranes, the etch duration will be calculated using the maximum etch rate measured during a first calibration etch.

2.2 Photolithography Layout

The layout used to expose the photoresist in this project was created by Petkus and is presented in his work [10]. The general layout can be seen in Figure 11. It is made of 21 repetitions of the 9 chips shown in Figure 10. These 9 chips contain accelerometers with different membrane radius, ranging from 500 µm to 2250 µm with a 250 µm increment.

There are four photolithography steps in this process, and the role of each layer will be detailed in the

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[1] Description of the LOR (Lift-Off Resist) 5A polymer on the CMi website (viewed 26.11.2019): https://cmi.epfl.ch/photo/photo_process/files/LOR_prep_new.html

[2] Average etch rate reported in [10] for a device with a 2000 µm radius in the center of the wafer : 4.29 µm/min; and for one with a 500 µm radius on the edge : 4.55 µm/min

next section. Direct laser writing with the MLA 150[3] is used for all photolithography steps in this project.

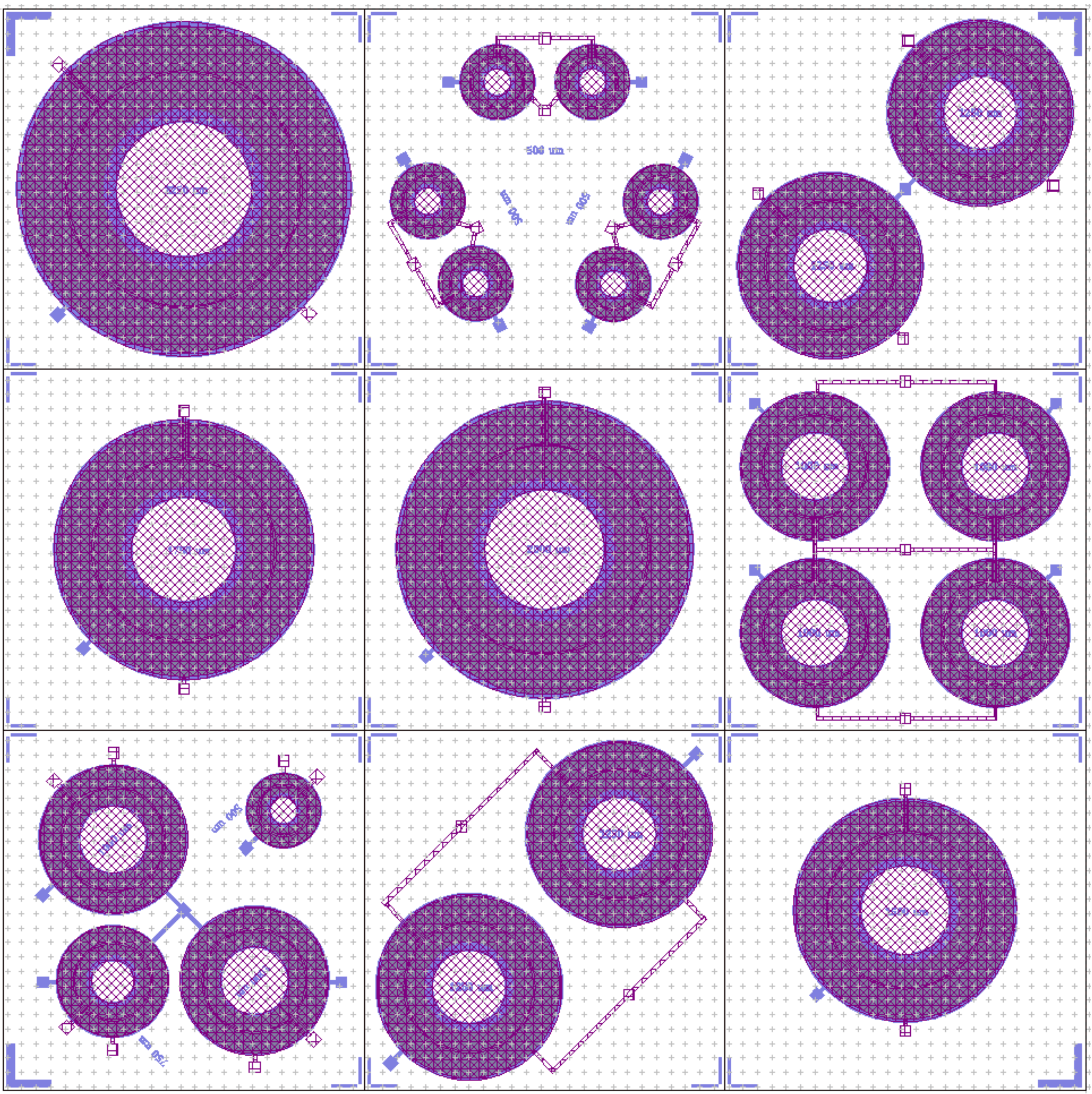

Figure 10: 15x15 mm square containing 9 5x5 mm chips. Repartition of devices by radius, from left to right and from top to bottom is as follows: 2250 µm, 6x 500 µm, 2x 1250 µm, 1750 µm, 2000 µm, 4x 1000 µm, 2x 1000 µm + 500 µm + 750 µm, 2x 1250 µm, 1500 µm.

[3] MLA 150 – Maskless Aligner (viewed 23.12.2019): https://cmi.epfl.ch/photo/MLA150.php

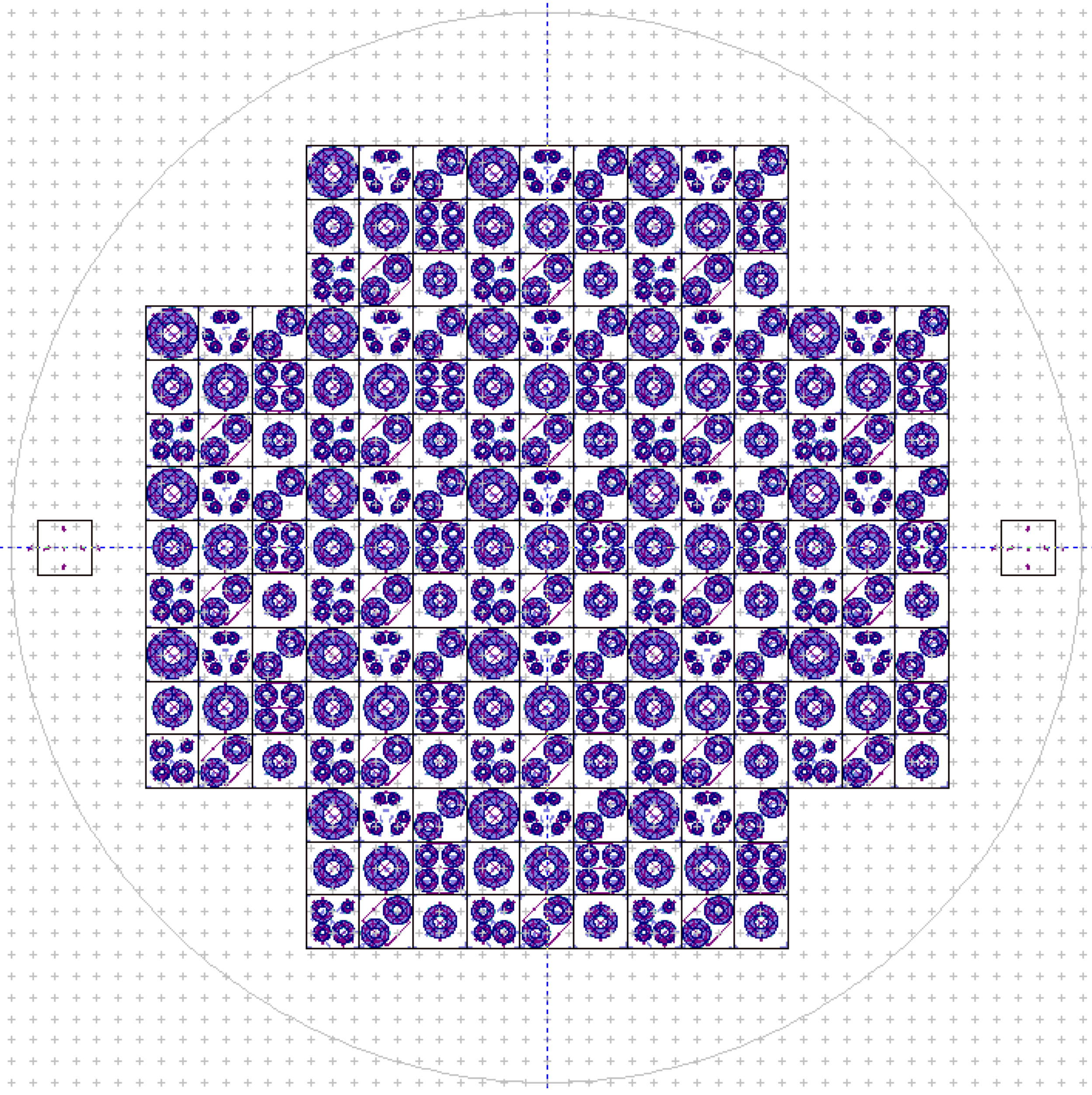

Figure 11: General photolithography layout for one wafer. The layout is made of 198 5x5mm chips.

2.3 Process Flow

A new process flow, which includes the changes presented in section 2.1, was established. It can be divided in two main parts. First, the electrodes and piezoelectric layer are deposited and patterned on the frontside and then the backside is etched to create the membrane and the mass.

The complete process flow can be found in the appendix.

2.3.1 Frontside: Electrodes and Piezoelectric Layer

Ground Electrodes

As mentioned previously, a bilayer lift-off process is used to create the ground electrode:

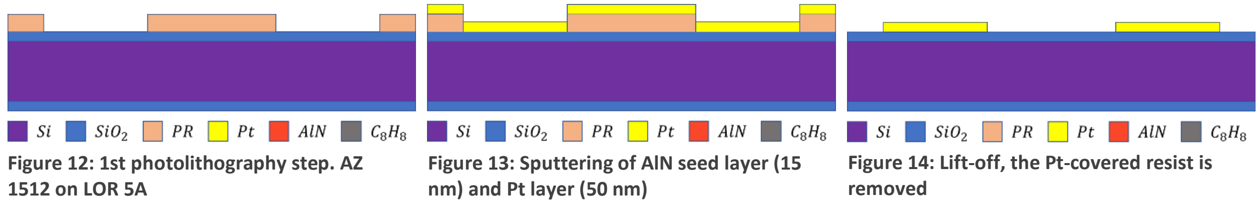

Figure 12: 1st photolithography step. AZ 1512 on LOR 5A

Figure 13: Sputtering of AlN seed layer (15 nm) and Pt layer (50 nm)

Figure 14: Lift-off, the Pt-covered resist is removed

First, a photolithography step is done using the EVG 150[4] to coat and develop the resist (Figure 12). The resists used are the positive resist AZ 1512 on top of the LOR 5A polymer, used as a sacrificial layer. Part of the layout used for the exposure with the MLA 150 is presented in Figure 15. As a positive resist is used, the regions exposed are where the resist will be removed and where the ground electrodes will be created.

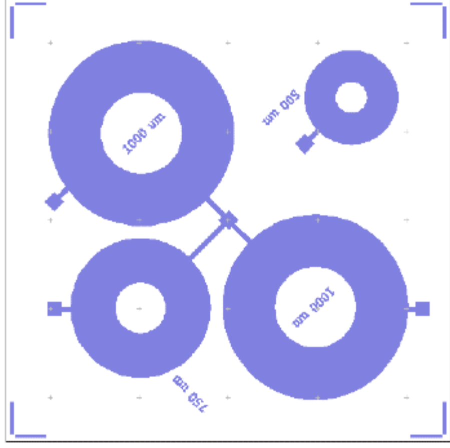

Figure 15: First layer of the photolithography layout. The blue shapes are exposed. The segments in the corner are there to create marks for dicing

To ensure that this bilayer lift-off process prevents the creation of fences, the duration of the development step of the resist is doubled compared to the standard duration proposed by the CMi.

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[4] EVG 150 – Automatic resist processing cluster (viewed 23.12.2019): https://cmi.epfl.ch/photo/EVG150.php

Then, 15 nm of AlN and 50 nm of platinum are sputtered using the SPIDER 600[5] (Figure 13). The AlN layer is a seed layer whose purpose is to ensure a correct crystalline growth of the piezoelectric layer that will later be deposited on top of the platinum layer. The thicknesses of the various layers sputtered with the SPIDER as well as the parameters used on this machine are parameters that were developed and optimized by the Advanced NEMS group.

Finally, the resist is removed using the solvent mixture MICROPOSIT Remover 1165 (Figure 14).

Piezoelectric Layer and Top Electrodes

The AlN piezoelectric layer and the top platinum layer are deposited by sputtering and patterned using dry etching:

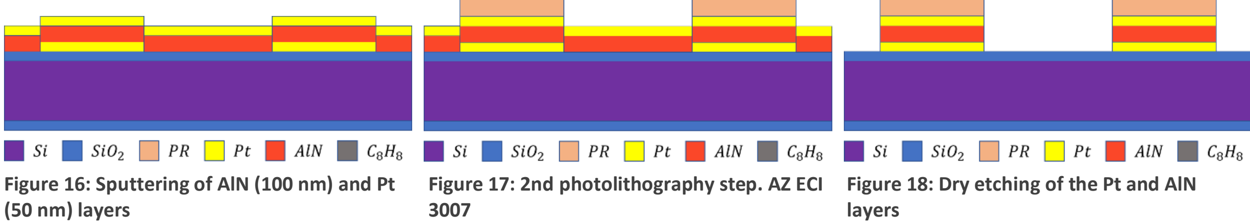

Figure 16: Sputtering of AlN (100 nm) and Pt (50 nm) layers

Figure 17: 2nd photolithography step. AZ ECI 3007

Figure 18: Dry etching of the Pt and AlN layers

First, a 100 nm-thick layer of AlN and a 50 nm-thick layer of platinum are deposited by sputtering with the SPIDER 600 (Figure 16).

Then, a photolithography step is done using the ACS 200[6] (Figure 17). The resist used is the AZ ECI 3007, which allows to obtain sidewalls that are not too steep (70-75°), which should prevent the creation of fences during the dry etching step. This is a positive resist, which means that the exposed region will get etched during the next step. Therefore, the layer illustrated in Figure 19 must be inverted when exposing with the MLA.

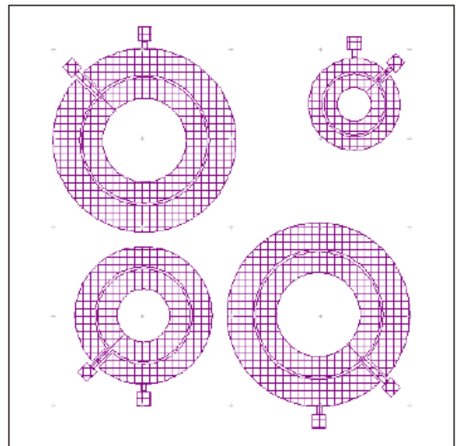

Figure 19: 2nd photolithography layer, the outside of the purple shapes is exposed

[5] SPIDER 600 – Dépôt par pulvérisation (viewed 26.12.2019): https://cmi.epfl.ch/thinfilms/Spider600.php
[6] ACS 200 Gen3 – Photolithography system for coating and development (viewed 27.12.2019): https://cmi.epfl.ch/photo/ACS200Gen3.php

The unprotected regions of the platinum and AlN layers are then dry etched with the STS Multiplex ICP[7] (Figure 18).

Finally, the resist layer is removed using a combination of oxygen plasma in the Tepla GiGAbatch[8] and the MICROPOSIT Remover 1165.

Resistance Check

In order to ensure that there are no fences at this point, the electrical resistances between the top and bottom electrodes are measured to verify that there are no short-circuits.

Protective Layer

Finally, before starting work on the backside of the wafer, the frontside is protected by depositing a parylene layer (Figure 20). This is done by the CMi staff using the Comelec C-30-S[9].

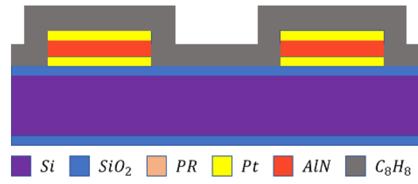

Figure 20: Deposition of a parylene layer

2.3.2 Backside: Mass and Membrane

SiO_2 Etch

The SiO_2 layer on the backside of the wafer is etched where the membrane and mass will be created in later steps.

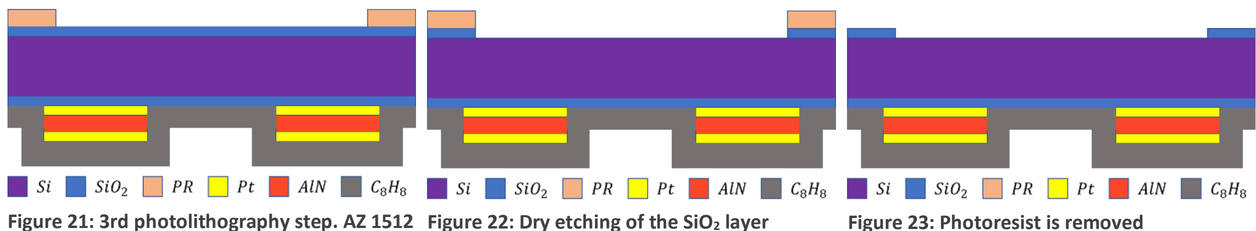

Figure 21: 3rd photolithography step. AZ 1512 **Figure 22: Dry etching of the SiO_2 layer** **Figure 23: Photoresist is removed**

First, a photolithography step is done using the EVG 150 (Figure 21) and the positive resist AZ 1512. The resist is exposed where the SiO_2 will be removed (see Figure 25).

The SiO_2 layer is dry etched in the SPTS APS[10].

Then the photoresist is removed with the MICROPOSIT Remover 1165.

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[7] STS Multiplex ICP – Dry etcher (viewed 26.12.2019): https://cmi.epfl.ch/etch/STS.php
[8] Tepla GiGAbatch – Plasma stripper (viewed 27.12.2019): https://cmi.epfl.ch/etch/GiGAbatch.php
[9] Comelec C-30-S (viewed 27.12.2019): https://cmi.epfl.ch/thinfilms/comelec.php
[10] STPS APS – Dielectric etcher (viewed 27.12.2019): https://cmi.epfl.ch/etch/APS.php

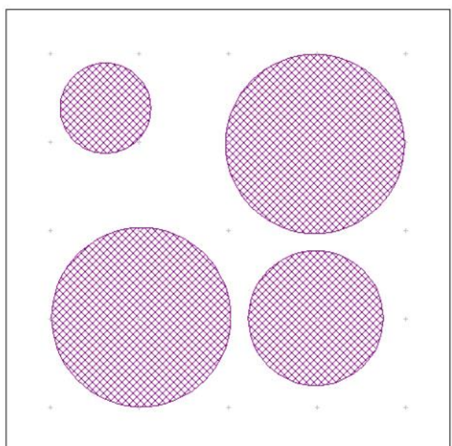

Figure 25: 3rd photolithography layer. The purple shapes are exposed. Note that the pattern is mirrored compared to the previous layer (Figure 19) as we are working on the backside now.

Silicon Etching – Membrane

A first etching of the Si substrate is done to pattern the membrane.

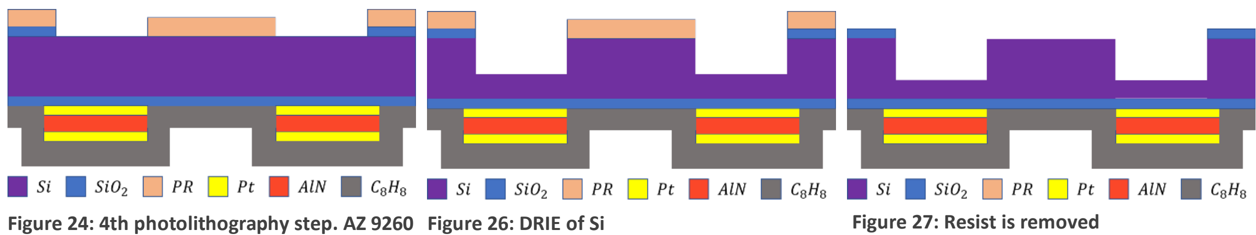

Figure 24: 4th photolithography step. AZ 9260 Figure 26: DRIE of Si Figure 27: Resist is removed

The last photolithography step is done using the EVG 150 and the positive resist AZ 9260 (Figure 24). The resist is exposed where the Si will be etched (see Figure 28).

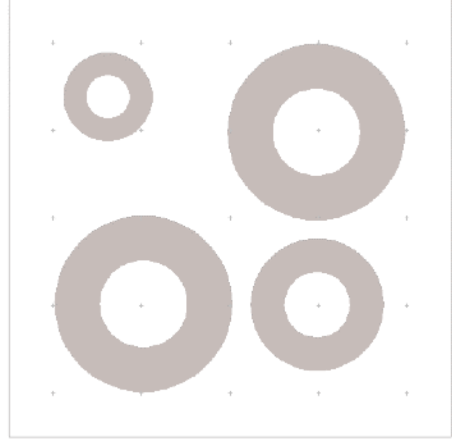

Figure 28: 4th photolithography layer. The grey regions are exposed

The silicon substrate is etched using deep reactive ion etching (DRIE) in the AMS 200[11] (Figure 26). As

[11] AMS 200 SE – Silicon etcher (viewed 27.12.2019) : https://cmi.epfl.ch/etch/AMS200.php

discussed previously, the etching should be done in several steps to be able to measure the etch rate and its non-homogeneity across the wafer before etching too much.

The resist is removed with O_2 plasma in the Tepla GiGAbatch and with the MICROPOSIT Remover 1165.

Silicon Etching – Mass and Membrane

Using the previously patterned SiO_2 layer as a mask, the Si substrate is etched a second time using DRIE in the AMS 200. This time, both the mass and the membrane are etched. The mass is thinned in order to have space to move without collision. The membrane is etched until the desired thickness of the membrane is reached.

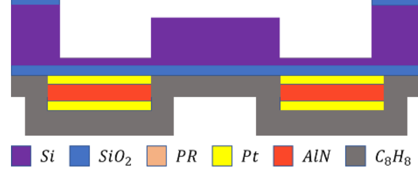

Figure 29: DRIE of Si

Removal of the Protective Layer

Finally, the protective parylene layer is removed with O_2 plasma in the Tepla GiGAbatch.

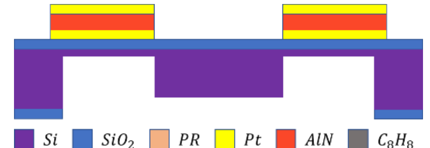

Figure 30: The parylene layer is removed

3 Finite Element Modelling

3.1 General Model

In order to compare the results obtained during characterization with the simulations done in the previous work, new simulations were done in COMSOL, using the simulations done by Petkus as a basis.

The exact dimensions used for fabrication were used to create a model of the accelerometer. With the mass and membrane thickness as well as the radius as parameters, the model can be easily modified to match the accelerometer being characterized.

To model the accelerometer the 2D axisymmetric space dimension of COMSOL is used. This allows to reduce computation time. The model is illustrated in Figure 31, with the *axial symmetry* boundary condition represented by the red dashed line. The rectangle on the left models the mass and the one on the right side models the wafer, with a *fixed* boundary condition applied to its right and bottom edges

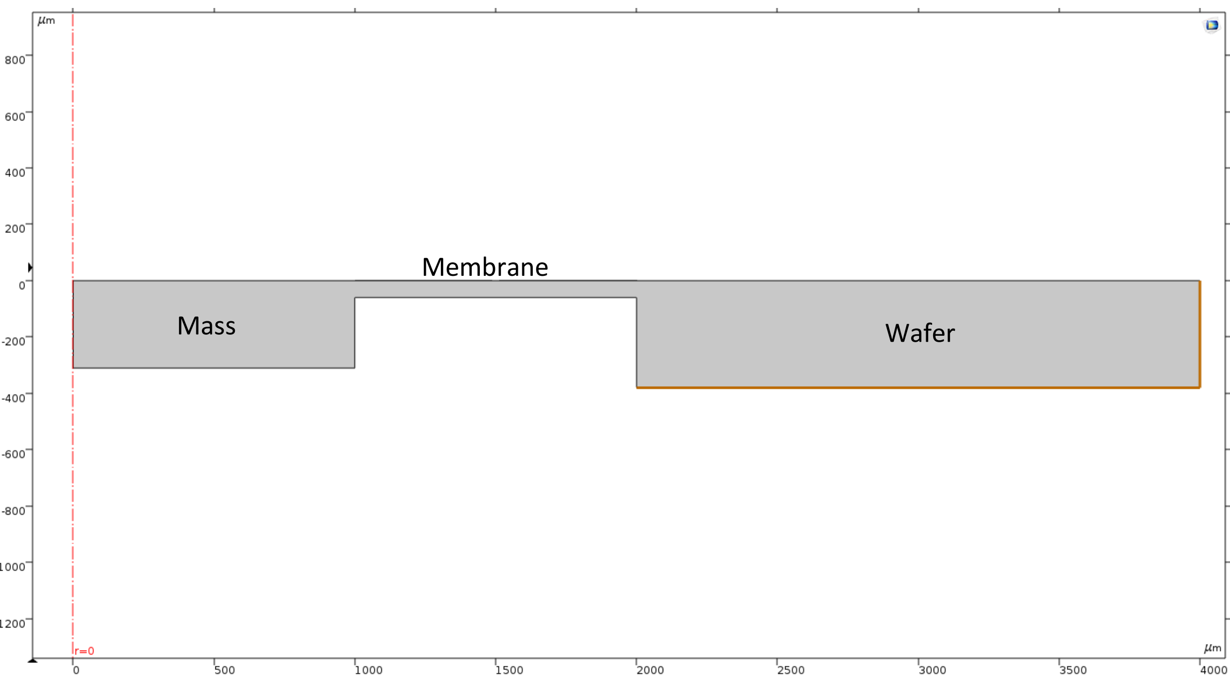

Figure 31: Geometry of the COMSOL model used to simulate the accelerometers

(orange lines).

The only parameters that are varied during this work are the thickness and radius of the membrane and mass (with $r_{mass} = \frac{1}{2} r_{membrane}$). The other parameters are fixed and correspond to the fabrication parameters presented before.

Two types of analysis were done: A dynamic eigenfrequency study to obtain the resonant frequency and a static analysis with an applied acceleration to get the charge generation.

In order to obtain the charges generated, boundary conditions must be set on the electrodes. In [10] it

was found that the best way to obtain those charges was to use a *ground* boundary condition on one side of the piezoelectric material and a *circuit* terminal on the other and to then use the COMSOL built-in *Terminal Charge* function. The result obtained this way showed good agreement with theory.

However, as characterization of the devices was done by electrically driving them (see section 5.1), another model with a *Voltage* terminal instead of the *Circuit* terminal was implemented in order to simulate this case. This allows to know the static displacement when a known voltage is applied to the electrodes.

3.2 Alternative Designs

3.2.1 Alternative Design 1

Two other designs were simulated. The first one was the same design with an added layer of piezoelectric material and an additional electrode layer, as shown in Figure 32.

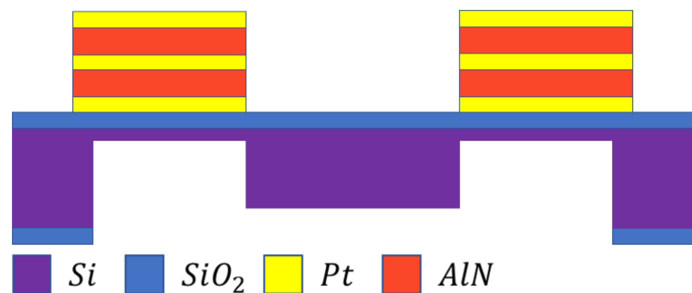

Figure 32: Drawing of the first alternative design. A second piezoelectric layer and a third platinum electrode layer are added to the initial design.

In order to simulate this design, the *ground* boundary condition was applied to the central electrode and *circuit* terminals were applied on the top and bottom electrode (the bottom electrode was separated in two to avoid charge cancellation). The charges were then obtained using the *Terminal Charge* function.

This configuration should allow to increase the charge generation while keeping changes of other characteristics, like frequency response, at a minimum.

3.2.2 Alternative Design 2

The second alternative was to replace the SiO_2 with a silicon nitride (SiN) layer and add a thick SU-8 layer with another SiN layer on top. This is illustrated in Figure 33.

The maximum thickness of SU8 available at the CMi is 300 µm. Given the configuration of this design, the neutral axis would be near of the center of the SU8 layer, which means that by putting a thick layer of SU8 we would increase the constraint on the piezoelectric layers, and in turn the charge generation. And, as SU8 is a material that is not too stiff, it would be possible to still have interesting mechanical characteristics.

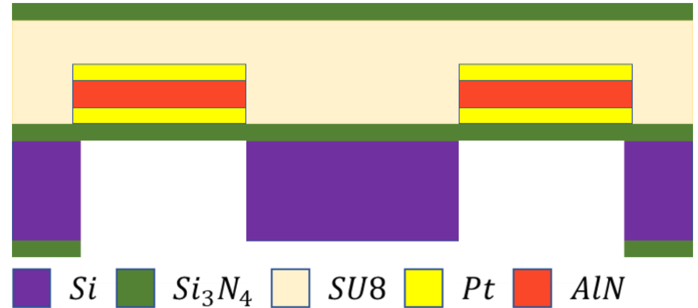

Figure 33: Drawing of the second alternative design. An SU8 layer between two layers of SiN replaces the Si membrane

To simulate this design the same boundary conditions are used as in the general model. However, initial stress must be added to the SU8 and SiN layers to have material properties corresponding to reality.

3.2.3 Results

The first design was simulated and compared to the standard model for two membrane thicknesses: 14 and 120 µm. The following changes were observed when adding a second piezoelectric layer:

- 14 µm membrane:
  - Generated charges: + 89 %
  - Resonant frequency: + 2.4 %
- 120 µm membrane:
  - Generated charges: + 98 %
  - Resonant frequency: + 0.3 %

The charge generation is practically doubled while the resonant frequency does not change significantly. The change in frequency is lower for a thicker membrane, which makes sense as the thickness and stiffness added by the additional layers is relatively lower than for a thinner membrane.

This alternate configuration could easily be manufactured by adding a photolithography, sputtering and dry etching step to the existing process.

The second design could not be studied enough due to issues with the application of initial stress resulting in the model behaving in unexpected ways. Due to lack of time, this issue could not be resolved, and this option was not studied further.

4 Experimental Process and Results

The wafers used for this process are double sided polished silicon wafers[12] with a thickness of 380 ± 5 µm. The thickness of the wafer defines an upper limit for the thickness of the mass. As the mass needs space to move, a mass thickness of 300 µm was chosen.

Three wafers were processed following the process flow presented in the previous section. A different membrane thickness was chosen for each wafer, in order to have accelerometers with various characteristics.

The target thicknesses are presented below with their resulting simulated characteristics:

Wafer n°	Membrane thickness [µm]	Resonant frequency [kHz]		Charge generation [fC/g]	
		r = 500 µm	r = 2250 µm	r = 500 µm	r = 2250 µm
6615	20	175.14	9.70	2.012	705.97690
6781	60	647.08	43.78	0.311	100.85546
6782	120	1231.19	99.67	0.099	32.45267

Frequencies are higher and charge generation is lower than the values shown in Figure 6 due the thickness of the mass being 300 µm instead of 350 µm.

4.1 Frontside Processing: Electrodes and Piezoelectric Layer

4.1.1 Ground Electrode – Lift-off

1st Photolithography Step – AZ 1512 on LOR

There are two standard recipes available at CMi on the EVG 150 to coat a wafer with AZ 1512 on LOR; one with 400 nm of LOR and 1.1 µm of AZ 1512 and the other with 700 nm of LOR and 1.6 µm of AZ 1512. According to the CMi staff, the rule of thumb is that the LOR layer should be at least three times as thick as the layer to be deposited. As the platinum layer to be deposited is 50 nm thick, the recipe with 400 nm of LOR was selected. The parameters used for exposure with the MLA where the following:

- Dose: 75 mJ/cm^2
- Defocus: -2

Those parameters are based on the CMi recommendations for AZ 1512 on LOR[13].

In order to ensure that there would be no fences, the development step of the standard recipe was run twice to double the development time. Figure 34 shows the result of this photolithography step.

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[12] CMi reference is 100/P/DS/1-10 TTV5, characteristics of this wafer are given here (viewed 02.01.2020): https://cmi.epfl.ch/organisation/files/100_p_ds_1_10.pdf

[13] LOR 5A exposure (viewed 06.01.2019): https://cmi.epfl.ch/photo/photo_process/files/LOR_exposure.php

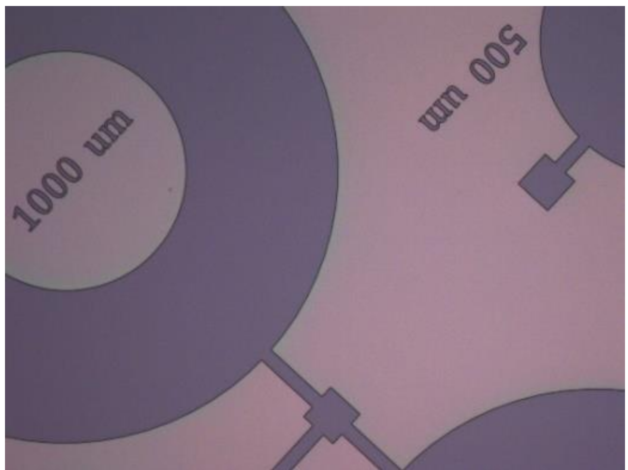

Figure 34: Wafer 6615 after the first step of photolithography. The darker regions are the SiO_2 layer. The lighter regions are where there is LOR and AZ 1512.

Sputtering – 15 nm AlN and 50 nm Pt

The AlN seed layer and the platinum layer were deposited with the SPIDER 600, using the following parameters:

Layer	T [C°]	P [W]	Time [s]
AlN – 15 nm	Room temp.	1500	23
Pt – 50 nm	Room temp.	1000	13

The sputtering must be done at room temperature as there is resist on the wafer that would be damaged if exposed to high temperatures.

Lift-off

The wafers were placed for 1 minute in an ultrasonic bath of remover 1165 before being left in another bath of remover 1165 for 20h. After that, most of the platinum covered resist was removed but some residues were left in the center of the electrodes. To remove them, the wafers were placed again in the ultrasonic bath for 1 minute. They were immersed in IPA to stop the lift-off process and rinsed with DI

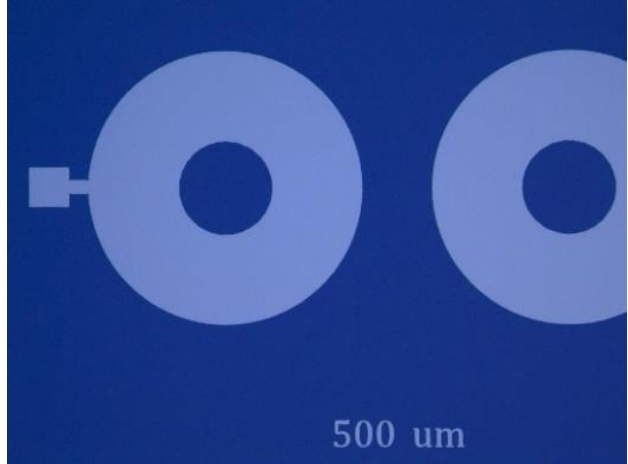

Figure 35: Wafer 6615 after the lift-off step. The lighter parts are where the platinum is

water following the standard CMi procedure[14]. Optical inspection (see Figure 35) confirmed that the resist was removed and that no fences seemed to be present.

4.1.2 Piezoelectric Layer and Top Electrodes

Sputtering – 100 nm AlN and 50 nm Mo

Initially, platinum was chosen as the material for the bottom and top electrode. For the bottom electrode, platinum is necessary to have a good crystalline growth of the AlN layer that will be sputtered on top. For the top electrode, the only constraint is that the material used must be a good conductive material. This is the case for platinum but also for molybdenum which is also available to be sputtered in the SPIDER. Molybdenum also has the advantage of being less expensive than platinum. However, the drawback of using molybdenum is that it oxidizes more easily than platinum.

For this reason, platinum was selected at first. But, when it was time to do the sputtering of the AlN and platinum layers, the target for sputtering available in the SPIDER was molybdenum and not platinum. To avoid losing time by waiting for the targets to be switched, it was decided to use molybdenum for the top electrodes.

The parameters used were the following:

Layer	T [C°]	Power [W]	Time [s]
AlN – 100 nm	300	1500	120
Mo – 50 nm	Room temp.	250	59

Optical inspection after sputtering of those layers showed the presence of some sharper edges that might be due to fences created during lift-off (see Figure 36).

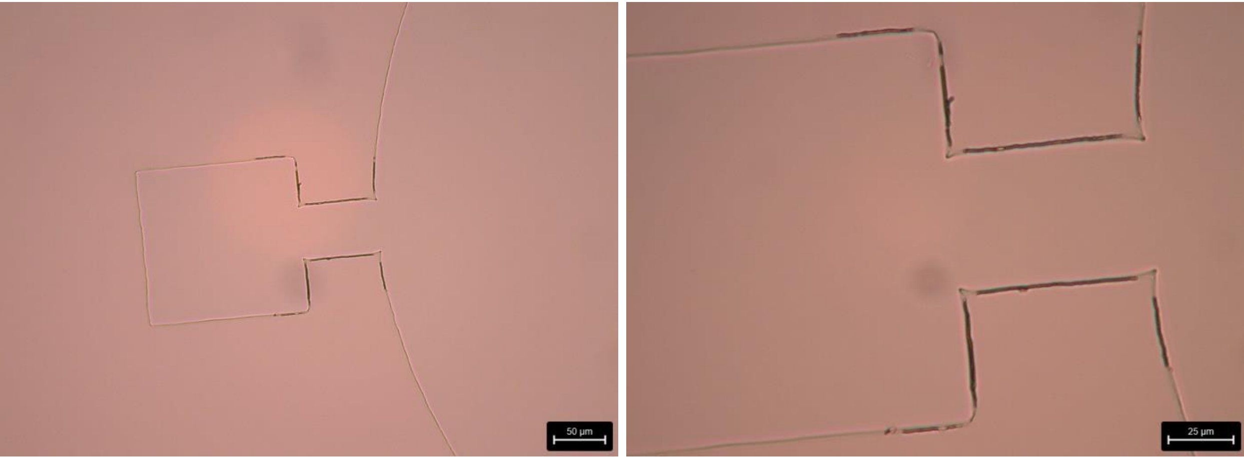

Figure 36: Wafer 6782 after sputtering of AlN and Mo. Black lines on the edges of the junction from the pad to the rest of the structure might indicate the presence of fences.

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[14] « Plade Solvent » Wet bench for solvents – Procedure for Lift-off (viewed 29.12.2019): https://cmi.epfl.ch/photo/PladeZ1.php#Liftoff_proc

However, these potential fences are not a great cause for concern, as they seem to always be localized on edges of the ground electrodes that will not be covered by the top electrodes (See Figure 39 with the resist corresponding to the place where the top electrodes will be), which means that they will not create any short-circuits.

2nd Photolithography Step – AZ ECI 3007

A 1.5 µm thick layer of AZ ECI 3007 was coated with the ACS 200, using a recipe including a HMDS priming step and EBR (Edge Bead Removal).

The parameters used to expose the resist on the MLA 150 for this step were:

- Dose: 200 mJ/cm^2
- Defocus: -1

The dose was found by adding 20% to the dose of 165 mJ/cm^2 recommended when coating on silicon[15].

For this step, the photolithography layout must be inverted on the MLA before converting the .cif file.

An unexpected issue was encountered after this step, as some tracks showed a kind of cut, shown in Figure 37. Upon inspection of the .cif file created by Petkus, it was found that there was a small space between the track and the rest of the device (see Figure 38).

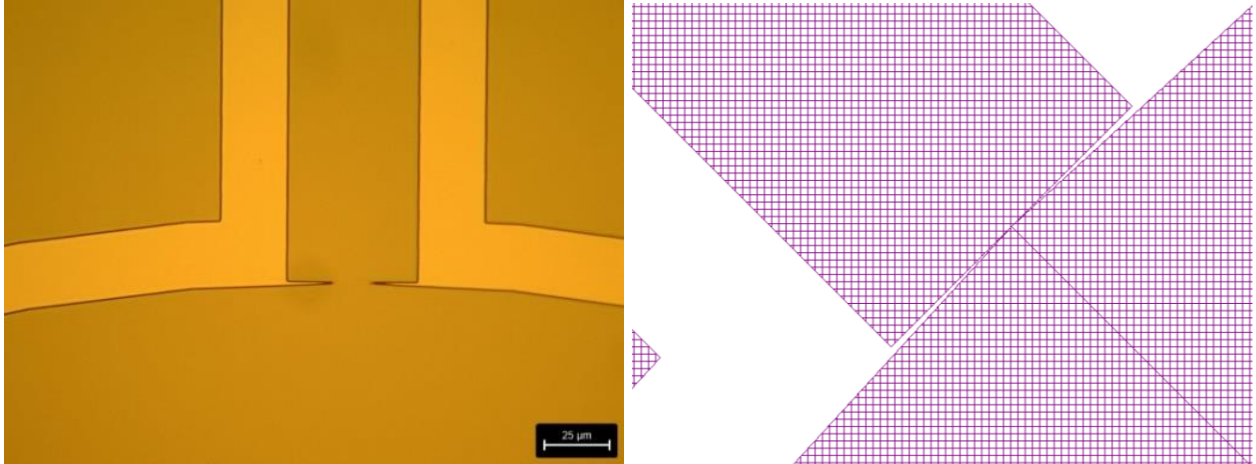

Figure 37: Wafer 6615 with AZ ECI 3007 (darker) on top of Mo. All devices with r = 1000 µm had the defect shown in this picture

Figure 38: Defect on the .cif file, the shapes do not overlap, leaving a small space.

The file was modified, and the resist was stripped from the wafers with remover 1165. The photolithography step was redone with the same parameters and the result, shown in Figure 39, was satisfactory.

[15] AZ ECI 3000 Exposure (viewed 14.01.2020): https://cmi.epfl.ch/photo/photo_process/files/AZ_ECI_3000_exposure.php

Figure 39: Wafer 6782 with AZ ECI 3007 (darker) on top of Mo. On the left, dark edges around the pad might indicate the presence of fences created during the lift-off step

Etching of Mo and AlN Layers

The molybdenum and AlN layer were then etched in the STS using the CMi recipe to etch AlN. This recipe uses a Cl/Ar chemistry and the indicated etch rates for Mo and AlN are 0.037 µm/min and 0.3 µm/min respectively. This results in a total etch time of 1min41s (1min21s+20s). The etching could be done for longer without damaging the SiO_2 layer on top of the wafer, however the platinum ground electrodes will get etched at a 0.037 µm/min rate.

The STS Multiplex at CMi is equipped with an optical endpoint detection system where a laser is reflected off the wafer and allows to follow the changes in reflected intensity during the etching process.

Wafer number 6781 was the first to be processed. The first etching process was stopped after 1min20s as the intensity reflected as well as the color of the substrate had changed (the substrate can be seen both

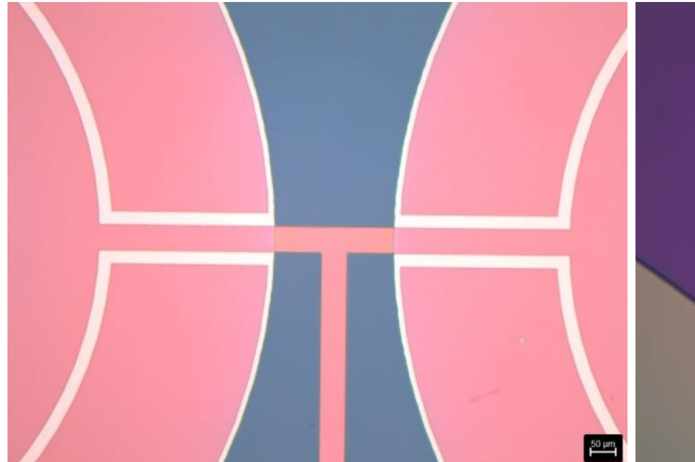

Figure 40: Wafer 6782 after etching of Mo and AlN. White is the platinum ground electrode; pink is the resist-covered Mo layer and blue is the SiO_2 layer

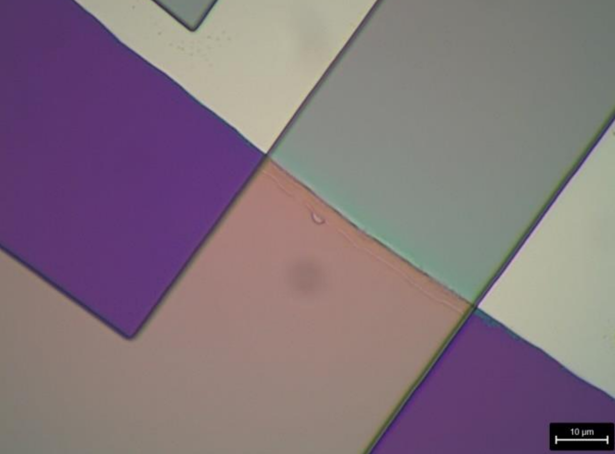

Figure 41: Wafer 6781 after etching of Mo and AlN. Shown is a spot were the top electrode track crosses over the edge of the ground electrode. Green and orange regions are the resist-covered Mo layer, white the Pt and purple the SiO_2

through a small window on top of the machine and on a camera feed). However, a circular color gradient could be seen on the wafer when getting it out of the machine, with only the center having both layers etched and the edges still having some color, probably corresponding to molybdenum, visible.

The wafer was etched again for 20s, this resulted in a uniform colored substrate on the whole pattern, with some gradient on the edges, outside of the layout.

The two other wafers were etched for 2min straight, resulting in a completely uniform substrate color. Based on the etch rate given on the CMi website the AlN layer would have been completely removed after 1min41s, meaning that the exposed regions of the ground electrodes may have been etched during the additional 19 seconds. This would result in losing 11.7 nm of thickness of the 50 nm of the Pt layer.

Figure 40 and Figure 41 show the result after this step.

Resist Stripping

The photoresist was then stripped using O_2 plasma and the remover 1165. The *PR_strip_high* setting was used on the Tepla GiGAbatch for 1 minute and then the standard CMi procedure for resist stripping was followed[16]. The result after stripping is shown in Figure 42.

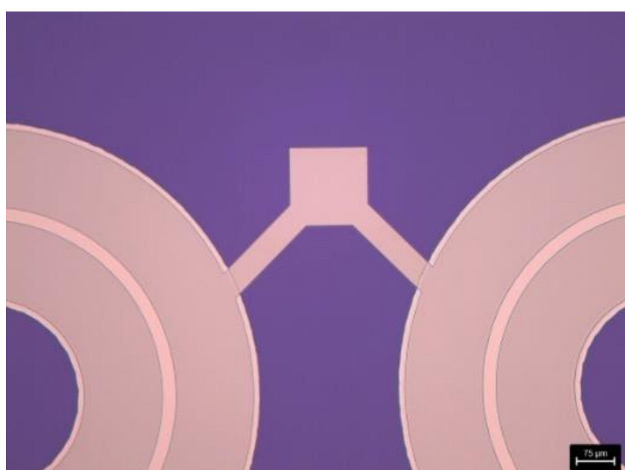

Figure 42: Wafer 6615 after stripping the resist. The purple region is the SiO_2 layer, the grey is the Mo layer and the lighter regions are the Pt layer.

4.2 Short-circuit Check

Before starting fabrication on the backside of the wafers, it is necessary to check if the ground and top electrodes are well isolated from each other, as there is no point in continuing the fabrication process if most of the devices are shorted. This was done using the probe station in the NEMS lab to measure the electrical resistances.

The top electrode to ground resistance of 31 randomly chosen electrodes on the three wafers was

[16] Manual for ultrafab wetbench - Photosensitive resist stripping with Remover 1165 (viewed 29.12.2019): https://cmi.epfl.ch/etch/UTF.php#remover

measured. Most of the resistances measured where equal to 10^8 Ω or higher. Only two of the measured resistances were in the kΩ range or lower. Excluding those two outliers, the average top to bottom resistance measured is 7.89 x 10^9 Ω or lower.
Given those results, the process was continued as planned.

4.3 Backside Processing: Mass and Membrane

4.3.1 Protective Layer, SiO_2 Etch, Photolithography

Parylene coating

In order to protect the frontside while processing the backside and to ensure that the membranes will not get damaged by the vacuum chucks of the machines used, a 3 µm thick parylene layer was coated on the wafers. This step is done by the CMi staff. In order to have parylene on only one side of the wafer, the other side can be protected by putting UV tape on it before coating or the parylene can be removed on one side after the coating. The second option was used in this case, due to lack of knowledge about the first option at the time.

The parylene layer on the backside was removed in the SPTS using the recipe *PI_vertical*.

3rd Photolithography Step – AZ 1512

A 1.5 µm thick layer of AZ 1512 was coated on the backside of the wafer using the EVG 150. As there is no HMDS priming included in the EVG 150, the primer oven YES III[17] was used to do an HMDS priming of the wafers before coating.

The standard recipe for this resist was used for coating and development, with the *no EBR* option (as the machines used from this point on use electrostatic clamping, EBR is not needed).

The parameters for the exposure with the MLA were the following:

- Dose: 123 mJ/cm^2
- Defocus: -2

The dose was calculated by adding 30% to the recommended dose of 75 mJ/cm^2 for exposure on silicon[18]. The dose must be increased when exposing on SiO_2, as the reflected power was measured as being at a minimum for λ=405 nm, the wavelength of the MLA laser. The measurement of the reflected power was done with the Filmetrics F20 UV[19]

The result of the photolithography step can be seen in Figure 43.

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[17] Primer Oven YES III (viewed 14.01.2020): https://cmi.epfl.ch/photo/Yes_primer.php

[18] AZ 1512 HS Exposure https://cmi.epfl.ch/photo/photo_process/files/AZ1512_exposure.php

[19] Filmetrics F20 UV – Spectroscopic reflectometer (viewed 14.01.2020): https://cmi.epfl.ch/metrology/F20-UV.php

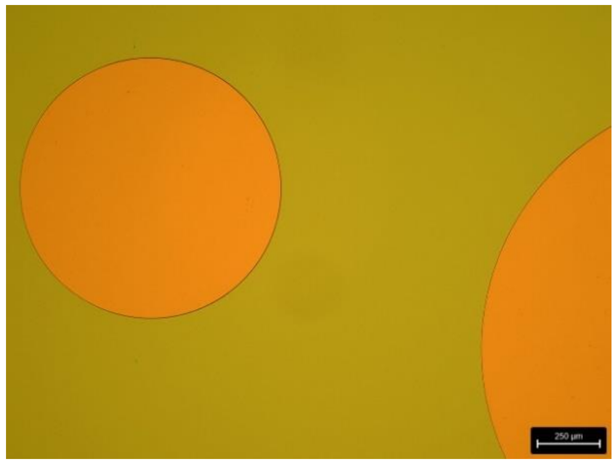


Figure 43: Wafer 6615 after the 3rd photolithography step. The resist is in green and the orange circles are the exposed SiO_2.

SiO_2 Etching

The 500 nm thick SiO_2 layer was etched using the SPTS APS etcher. Several different processes are proposed to etch SiO_2 on the CMi website[20]. The *SiO2 PR 3:1* process was selected because it has a fairly high etch rate for wet oxide and a much lower one for Si which is good in this case as we do not want to etch the silicon under the oxide layer. The etch rate of SiO_2 given for this process is 345 nm/min, which results in 1min27s needed to etch 500 nm. The SPTS has on optical spectroscopy-based end point detection system.

Following the advice of the CMi staff, the process was left to run 10s after end point detection, to ensure that the SiO_2 layer be completely etched. This resulted in the following duration for the three wafers:

- Wafer 6615: 1min37s
- Wafer 6781: 1min37s
- Wafer 6782: 1min34s

Visual inspection confirmed that the SiO_2 was completely removed.

Resist Stripping

To try to protect the parylene layer on the frontside, no O_2 plasma was used to remove the resist. However, one standard cycle with the remover 1165 in the resist stripping wet bench was not enough to remove the resist. The process was repeated twice with little improvement. But it was observed that the parylene layer was starting to detach from the wafer and some folds were visible on the parylene layer.

As the parylene layer was too damaged to keep, it and the photoresist on the backside where removed with O_2 plasma in the Tepla GiGAbatch (*PR_strip_high_10min)* and a new parylene coating was requested.

[20] Manual for SPTS APS – Processes available (viewed 29.12.2019): https://cmi.epfl.ch/etch/APS.php#processes

Second Parylene Coating

For this coating, the frontside was covered beforehand with UV tape. The thickness was 7 µm because it was the thickness available that given week. Given the large areas of the membranes, a parylene layer of at least 5 µm should be used if possible. The UV tape and parylene on the frontside were removed without any issue.

4.3.2 Si Etching

The etching of the membrane and mass is done in two steps. First, only the membrane region is etched and then both the mass and membrane are etched. The etch depth of each step is given by:

$$d = t_{Si} - t_{memb} = d_1 + d_2 \quad (1)$$

$$d_2 = t_{Si} - t_{mass} \quad (2)$$

$$d_1 = d - d_2 = t_{mass} - t_{memb} \quad (3)$$

With d the total etch depth, d_1, d_2 the depths of each step and $t_{Si}, t_{memb}, t_{mass}$ the thicknesses of the silicon layer, the membrane and the mass.

As the wafers are 380 µm thick, the mass thickness was chosen as 300 µm to leave 80 µm free for the mass to move. This means that $d_2 = 80\ \mu m$ for all three wafers.

To etch the silicon, the Bosch process is used in the AMS 200. The etch rate is design dependent and it is advised to run a short etch process at first to measure it. Based on the etch rates measured by Petkus in [10] for this design, a difference of etch depth of around 6% can be expected depending on the size and localization on the wafer of the etched structure. For the wafer number 6615, where the target membrane thickness is 20 µm – 360 µm of etch depth total, it means that there could be up to 21.6 µm of additional etching, which would result in the silicon layer being completely etched. To guarantee that there is still some silicon left, a minimal thickness of 10 µm was chosen. For the two other wafers, a minimal thickness 10 µm lower than the target thickness was chosen as well. Meaning that the maximum etch depth is given by $d_{max} = d + 10\ \mu m$. This results in the following etch depths for each wafer:

Wafer n°	t_{memb} [µm]	d [µm]	d_{max} [µm]	d_1[µm]	$d_{1,max}$[µm]	d_2[µm]	$d_{2,max}$[µm]
6615	20	360	370	280	287.78	80	82.22
6781	60	320	330	240	247.5	80	82.5
6782	120	260	270	180	186.92	80	83.08

With the maximum first and second etch depths calculated as follows:

$$d_{1,2,max} = \frac{d_{max}}{d} \times d_{1,2}$$

Focusing on attaining the maximum depths listed above should result in having a range of membrane and mass thicknesses spread around the target values.

The etch depths are measured with and optical microscope, by focusing successively on the edge of the device and the bottom of the etched region and retrieving the z-difference of focus. This measurement technique lacks accuracy but has the advantages of being easy to do and of allowing to quickly check the

advancement of the etching between two runs in the AMS.

When using the AMS 200, two main parameters can be chosen, the type of process and the etch duration. The process used to etch silicon is the one labeled *SOI_accurate* on the CMi website[21]. This process exists with different pulse length, labeled from *SOI_accurate----* to *SOI_accurate++++* with the former having the lowest etch rate and the latter the highest. Using one of the slower processes results in smoother sidewalls with less notching.

The etch rate is given as being between 3 and 4.5 µm/min, which allows for as first estimation of the etch time:

$$time = \frac{d_{max}}{ER_{max}} \tag{4}$$

$$time_{1,2} = \frac{d_{1,2}}{d} \times time \tag{5}$$

With $time$ the total etch time, ER_{max} the maximum etch rate and $time_{1,2}$ the etch times for the first and second step.

The calculations are done using the maximum etch rate to ensure that the wafers are not etched too much. With $ER_{max} = 4.5\ \mu m/min$ this gives us the following etch times:

Wafer n°	$time$ [min]	$time_1$ [min]	$time_2$ [min]
6615	82.22	63.95	18.27
6781	73.33	55.00	18.33
6782	60.00	41.54	18.46

The values presented in this table allow to get an idea about the etch time needed but, as mentioned above, the etch rate is design- and process-dependent and must be measured for every new process. The method followed was to etch for a given time before measuring the etch depth at several points on the wafer to establish the maximum etch rate. Then, a new etch time was calculated and the wafer was etched for the remaining duration.

However, measurements made during the first etching step, after different etch times, showed that the etch rate decreased with the increasing total etch time. Meaning that the deeper a structure becomes, the slower the etching gets. The measured etch rates as a function of total etch time are presented in Figure 44.

This poses a problem for the second etching step, as the center of the structure (the mass) will probably get etched faster than trench surrounding it (the membrane). Taking this into account, the first and second etch times were adjusted by making the first etch step longer. The new etch times were calculated as follows:

[21] Manual for AMS 200 SE – Standard processes (viewed 30.12.2019): https://cmi.epfl.ch/etch/AMS200.php#standards

$$\text{time}_1 = \text{time} - \text{time}_2 \quad (6)$$

$$time_2 = \frac{80\ \mu m}{ER_{80}} = \frac{80\ \mu m}{4.89\ \mu m/min} = 16.36\ min \quad (7)$$

With time_2 the time needed to etch the depth needed off the mass (80 µm) and ER_{80} the mean etch rate when etching 80 µm. It was evaluated and adjusted using the measurements made during the first etching step. The total etch time, time, was also adjusted as the process went.

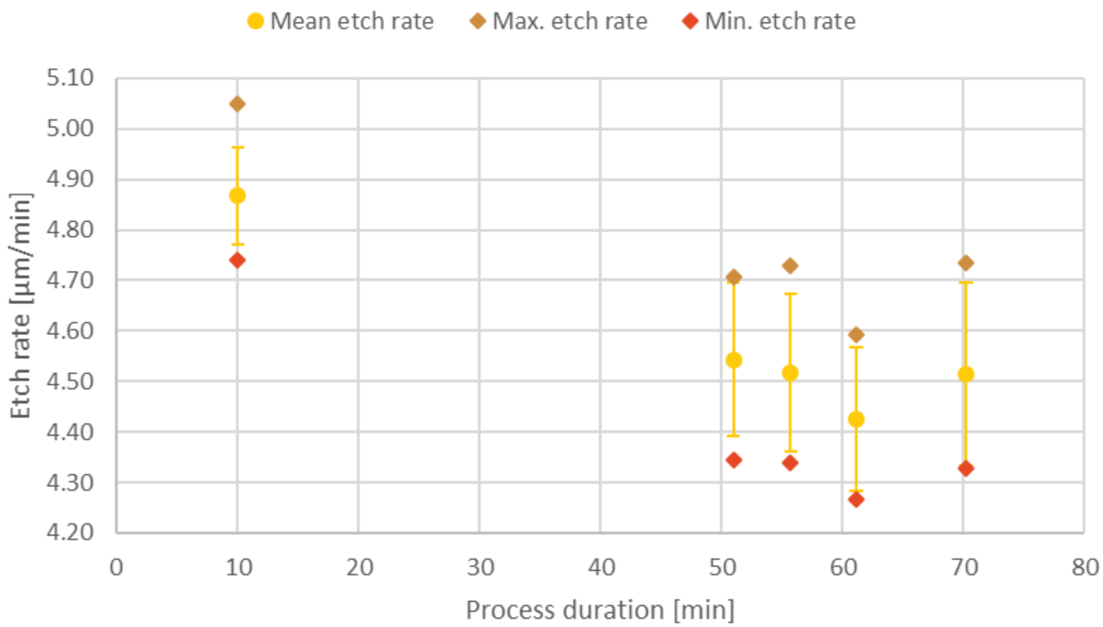


Figure 44: Etch rate as a function of process duration for the SOI_accurate++ process. The mean etch rate values are based on 16 measurements of the etch depth for the 10 min point and 8 measurements for the other points. Error bars show the standard deviation of the measured etch rate.

4th Photolithography Step – AZ 9260

After and HMDS priming step using the YES III primer oven, a 5 µm thick layer of AZ 9260 was coated on the backside of the wafers, using the EVG 150. The exposure of the resist was done with the MLA using the following parameters:

- Dose: 350 mJ/cm^2
- Defocus: 2

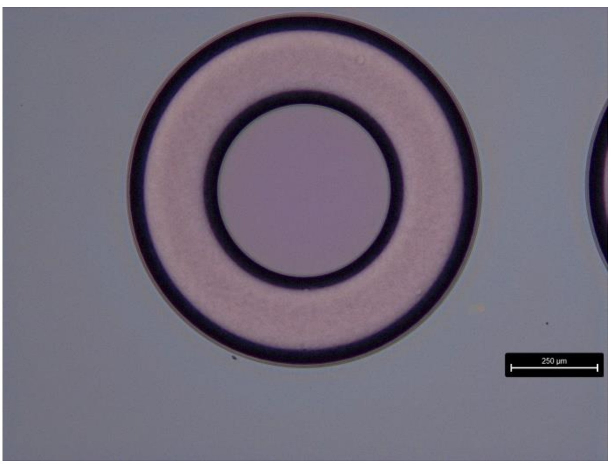
These parameters are based on CMi recommendations that are not available anymore as the AZ 9260 resist has been discontinued.

After development in the EVG 150, the wafers were put in an oven at 85°C overnight. This is necessary to ensure that the photoresist layer is stable during the following etching step.

Si Etching – First Step

Wafer n° 6782 – t_{memb} = 120 µm

At first, the *SOI_accurate*-- process was used for 35 min on wafer 6782 (see Figure 45). This process was chosen because it was presented as being the "standard" one and it was done for the longest duration possible given equipment availability. The result after this etch time is shown in Figure 45.



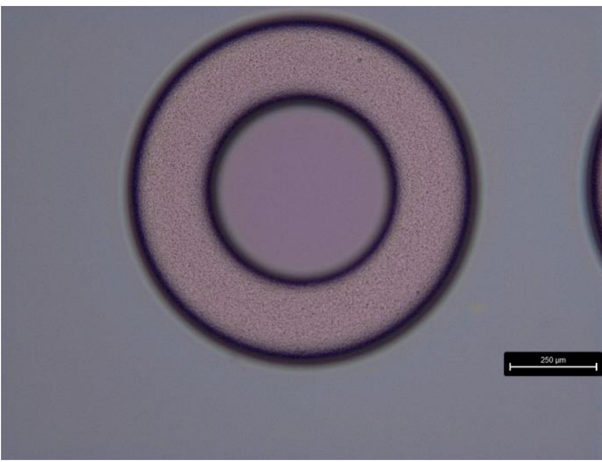


Figure 45: Wafer 6782 after 35 min of etching with *SOI_accurate*--. The grey region is the resist-covered SiO_2 layer, the pink region in the center of the circle is resist-covered silicon, the orange ring is the etched silicon. On the left, the focus is on the edge of the device, on the right, the focus is on the bottom of the etched ring.

Measurement of the etch depths after 35 min of the *SOI_accurate*-- process allowed to calculate the following etch rates:

Position on the wafer	Radius [µm]	Etch rate [µm/min]	SD (Etch rate) [µm/min]
Center	500	4.09	0.03
Center	2250	4.05	0.02
Edge	500	4.19	0.09
Edge	2250	4.21	0.11

With the etch rates calculated using 16 measurements of the etch depths, 4 for each position/radius combination.

As can be seen in the table above, the position of the etched structure seems to have a significant impact on the etch rate. However, contrary to what was reported in [10], the size of the feature does not seem to impact the etch rate.

To ensure that no feature is etched deeper than the chosen maximum depth $d_{max} = 270\ \mu m$, the highest measured etch rate, $ER_{max} = 4.34\ \mu m/min$, is used to calculate the required etch time. This gives us, using equations 4 and 5:

$$time = \frac{270}{4.34} = 62.21\ min$$

$$time_1 = \frac{180}{260} \times 62.21 = 43.07\ min$$

The wafer was then etched 8 more minutes in order to reach 43 minutes. This resulted in an etch depth ranging from 168.5 to 184.7 µm, which is around the value of the first etch depth, $d_1 = 300 - 120 = 180\ \mu m$.

Due to observations of the decreasing etch rate made while etching the other wafers and for reasons explained above, this wafer was later etched 3 more minutes using the *SOI_accurate++* recipe. This resulted in etch depths ranging from 185.7 to 198.1 µm.

Wafer n° 6781 – t_{memb} = 60 µm

To reduces the time needed for the etching, it was decided to use the *SOI_accurate++* for the remaining etch steps. Wafer n° 6781 was first etched for 10 minutes to measure the etch rate. The maximum etch rate found was 5.05 µm/min, which results, using equations 5 and 6 in:

$$time = \frac{330}{5.05} = 65.35\ min$$

$$time_1 = \frac{240}{320} \times 65.35 = 49.01\ min$$

Due to some calculation mistake, the wafer was etched for 51 minutes. However, measurements at this point showed that the etch rate was decreasing with increasing etch depth. This led to using equations 6 and 7 to calculate the etch time and to adjust the value of the etch rate as new values were measured.

Etch depths ranging from 241.7 to 253.3 µm where obtained by etching for 56 minutes total. As expected, these etch depths are higher than the target first etch depth, $d_1 = 240\ \mu m$.

Wafer n° 6615 – t_{memb} = 20 µm

Based on the results obtained on wafer n° 6781, wafer n° 6615 was first etched for 61 minutes. The insufficient etch depths confirmed the observed trend that the etch rate was decreasing with the increasing depth. The wafer was etched for 9 more minutes. However, the etch rate was higher than

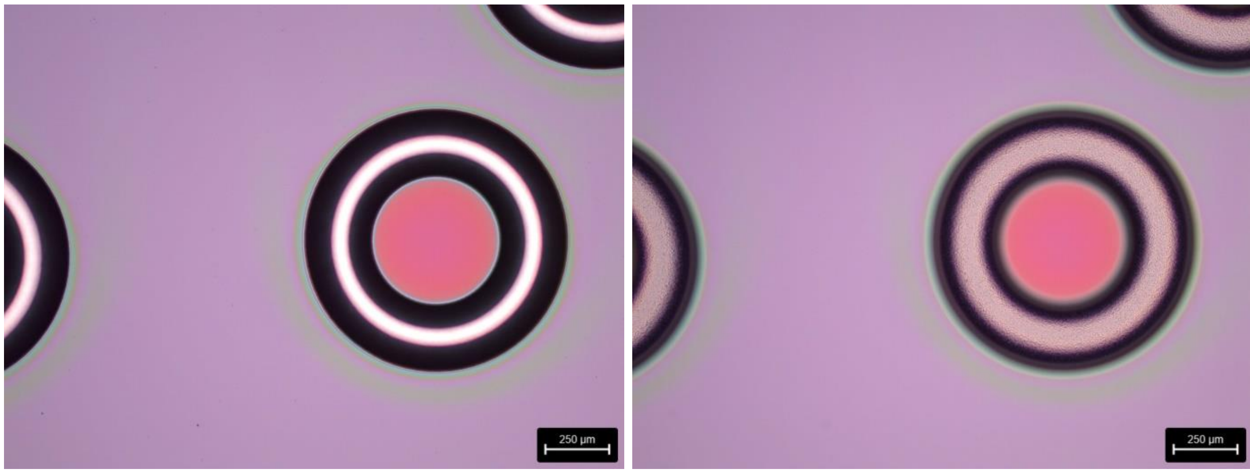


Figure 46: Wafer 6615 after the first Si etching step. The purple region is resist-covered SiO_2, the red region is resist-covered Si. The light and dark circles are the etched region. On the left the focus is on the edges of the structures; on the right it is on the bottom of the etched region. The dark circles around the mass and on the periphery of the etch show that the bottom of the etch is not flat. A height difference of around 10 µm between the edge and the center of the etch has been measured.

expected and the resulting etch depths are in a range of 303.7 to 332.3 µm, which is much higher than the target first depth $d_1 = 300 - 20 = 280$ µm. This can be compensated by etching less on the second step, but this will result in a thicker mass than planned. The result after 70 minutes of etching can be seen in Figure 46.

Summary

The table below shows the etch times and process used for each wafer as well as the depths obtained.

Wafer n°	Process	Duration [min]	Min etch depth [µm]	Max etch depth [µm]
6615	SOI_accurate++	70.18	303.7	332.3
6781	SOI_accurate++	55.70	241.7	253.3
6782	SOI_accurate-- SOI_accurate++	43.00 3.00	185.7	198.1

Resist Stripping

After the first etching step, the resist is removed with O_2 plasma and remover 1165. The result after resist stripping is shown in Figure 47.

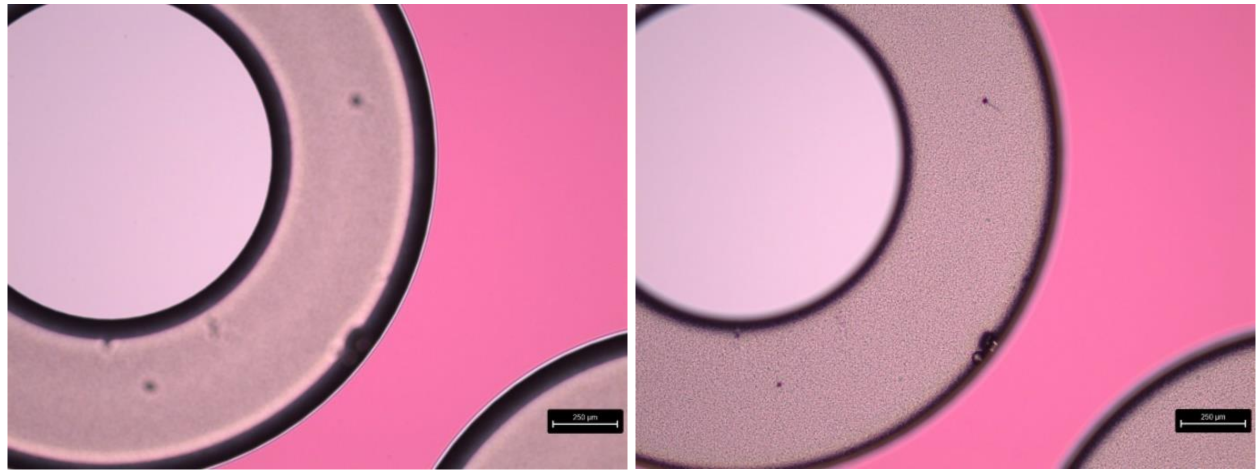


Figure 47: Wafer 6615 after resist stripping. Light pink is the unetched Si, pink is the SiO_2 layer, brown is the etched Si. On the left the focus is on the edge of the etch, on the right the focus is on the bottom.

Si Etching – Second Step

For the second etching step, the recipe *SOI_accurate++* was used for all wafers. Wafers 6781 and 6782 were both etched for 10 minutes then 6 minutes. Figure 48 shows the result after the first 10 minutes etch.

The etch rate in the center was lower than expected, meaning that the masses ended up being thicker than planned. This should not be an issue however, as the thickest masses were measured on wafer n° 6615 as being 344 µm thick, which still leaves 36 µm for the mass to move.

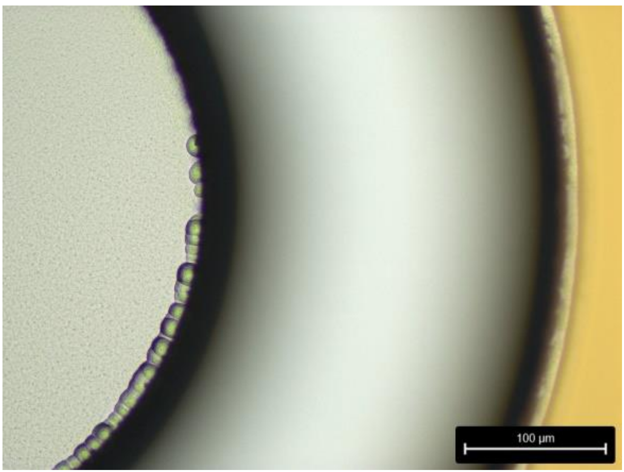


Figure 48: Wafer 6781 after 10 minutes of the second etch. On the left is the mass, on the right, in yellow is the SiO_2 layer. The focus is on the mass, which at this point is around 50 µm deeper than the surface of the wafer.

Wafer 6615 was first etched for 5 minutes, then 2.5 minutes and finally for 2 minutes. Even though it was etched for only 9.5 minutes total, the silicon layer was completely etched through for twelve of the chips situated in the corners of the layout. One of those destroyed device can be seen in Figure 49.

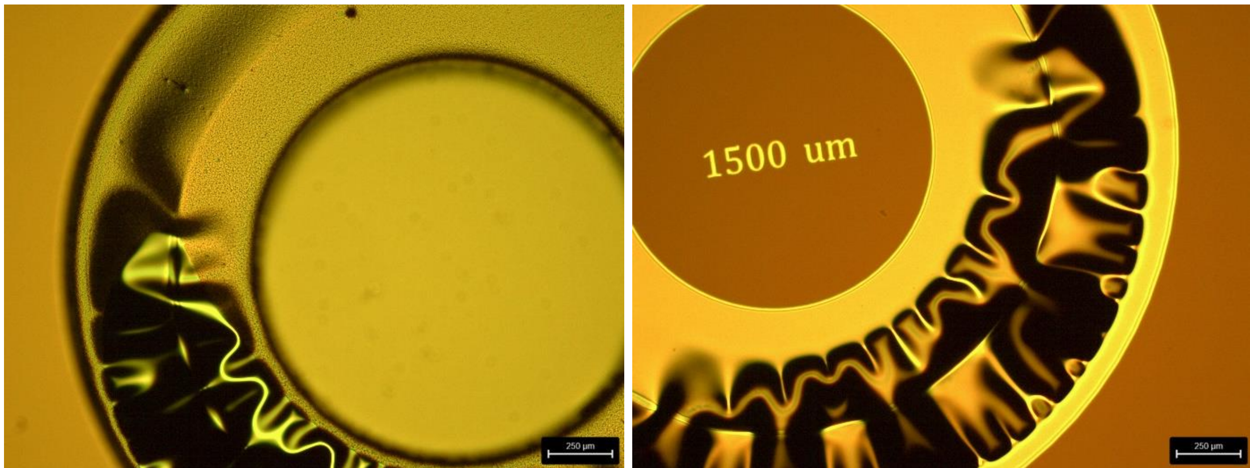


Figure 49: Destroyed device on wafer 6615. On the left the backside is shown, with the folded metal layer showing through the silicon. On the right the frontside of the same device is shown, with the electrodes folding were the silicon has been completely etched. The destroyed side is facing the edge of the wafer.

The fact that only one side of the device is etched through shows the non-homogeneity of the etch rate depending on the position. Measurements of etch depths across the wafers showed that this non-homogeneity of the etch rate is more important closer to the edges of the wafers.

The etch times for this second step and resulting etch depth extremums are shown below:

Wafer n°	Process	Duration [min]	Etch depth membrane [µm]			Etch depth mass [µm]		
			Target	Min	Max	Target	Min	Max
6615	SOI_accurate++	9.5	360	348	382	80	36	57
6781	SOI_accurate++	16.0	320	311	344	80	57	80
6782	SOI_accurate++	16.0	260	256	272	80	67	79

4.4 End of Processing

4.4.1 Parylene Removal

Finally, the parylene layer is removed with the Tepla using the recipe *PR_strip_high*. This recipe was used for the following duration for each wafer:

- Wafer 6615: 7 minutes + 30 seconds + 30 seconds = 8 minutes
- Wafer 6781: 7 minutes + 30 seconds + 30 seconds = 8 minutes
- Wafer 6782: 7 minutes + 1 minute + 1 minute + 30 seconds + 30 seconds = 10 minutes

As some small parylene residues were still left on the wafers after that (see Figure 50), the wafers were subjected to two runs of resist stripping procedure in the remover 1665. This allowed to remove most of the parylene residues (see Figure 51).

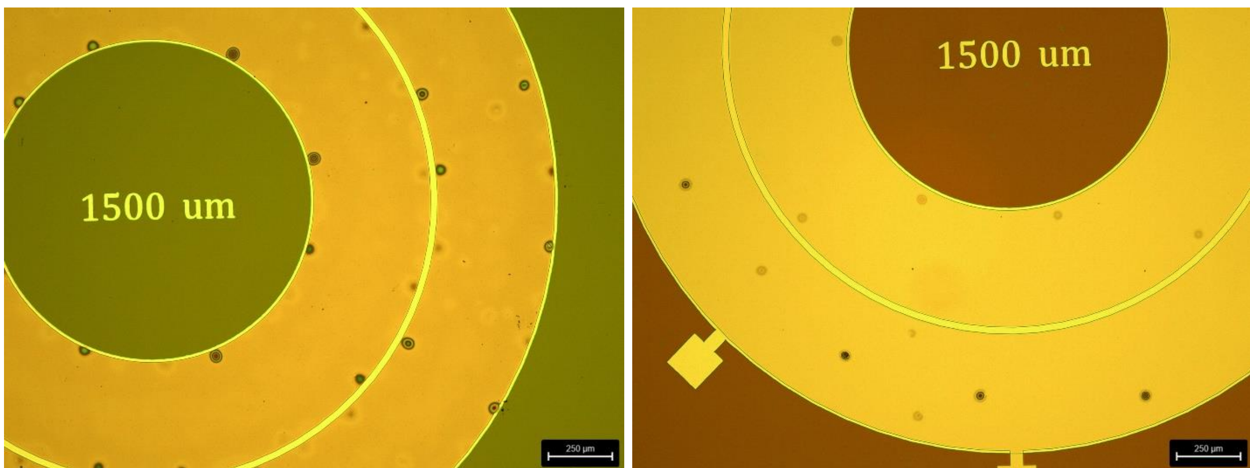


Figure 50: Wafer 6781 after 8 minutes in the Tepla. Circular residues are visible one the electrodes, discolored spots show were parylene has been removed last.

Figure 51: Wafer 6781 after 8 minutes in the Tepla and 2 runs in the remover 1665. Most of the residues have been removed.

4.4.2 Oxidation

Inspection of the frontside of the wafers while and after the parylene was removed showed that in some regions of the wafer the molybdenum top electrodes had oxidized, as can be seen in Figure 52.

This non-uniform oxidation must have happened when the first parylene layer was removed, as the parylene layer was folded, meaning that some regions were already unprotected when the wafers were subjected to O_2 plasma for 10 minutes. This would also explain the patterns appearing on the electrodes on the right picture of Figure 52, as the parylene layer was displaced before being removed in the Tepla.

However, this oxidation was limited to the outer regions of the wafer n° 6781 and was almost absent on the other wafers.

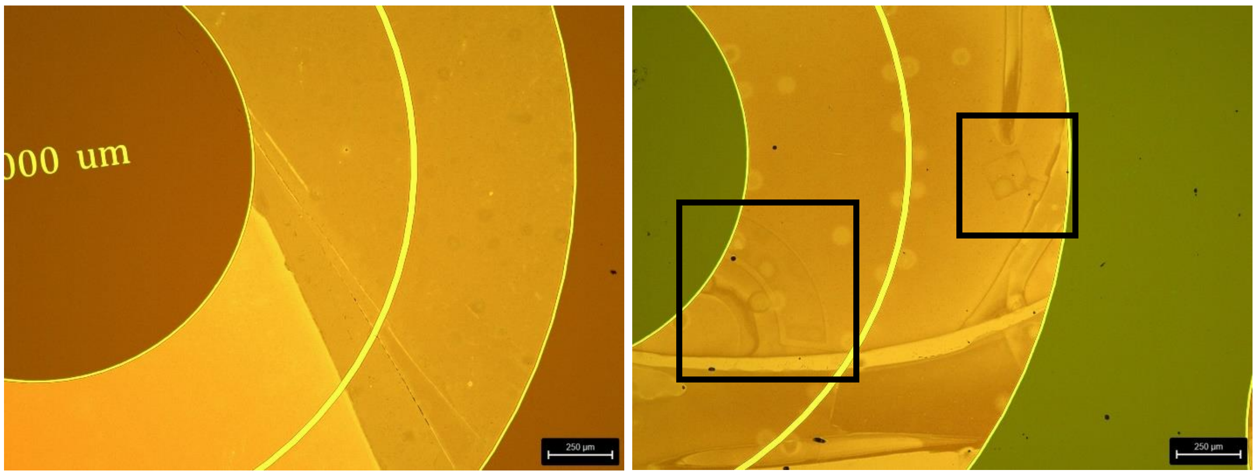


Figure 52: Wafer 6781 after O_2 plasma for parylene removal. The non-uniform color of the molybdenum top electrodes suggests that only some regions of the wafer were oxidized. On the right patterns of smaller electrodes are visible (in the black squares).

4.4.3 Second Resistance Check

Before dicing the wafers, the resistances of several devices were checked. Resistance of the top layer was checked as well as the one between the bottom and the top because of the oxidation issue. Where oxidation was obviously visible on the contact pad, top to top resistance was very high or not measurable. Otherwise, the measured resistances were in the same range as during the first resistance check.

4.4.4 Dicing

Before dicing is done by the CMi, the wafers must be protected from the process. The backside is protected anyway by the UV tape used as a support during the dicing, but the frontside must covered as well.

For wafers n° 6781 and 6782 UV tape was put on the frontside as well. However, for wafer n° 6615, which has very thin membranes, using UV tape seemed too risky. Therefore, a layer of photoresist was coated manually.

At first, to ensure the survivability of the process, only wafer n° 6781 was protected and diced as it was the one with the most devices oxidized. After the dicing, there was one crack spanning across 5 chips on the wafer, cutting them in half. All the other chips were intact.

The dicing was done on the two other wafers, where all chips survived. Acetone was used to remove the photoresist from the chips of wafer 6615.

5 Characterization

5.1 Characterization Method

The main objective of the characterization is to validate the results obtained by simulations, as this would allow to use the simulations as a reliable way to further optimize the design before starting a new fabrication.

Measuring the resonance frequency was done using a laser doppler vibrometer (LDV) and a digital holographic microscope (DHM), as both those tools are available in the NEMS lab. Using both allows to confirm the validity of the measurements.

To measure the charge generation, the ideal way would be to subject the accelerometer to a known acceleration and measure the charge generated. However, using the inverse piezoelectric effect to measure the sensitivity of the device is easier to do, as one just has to input a known electrical potential and optically measure the corresponding displacement. To do that, the chips to be measured were glued and wire-bonded to a PCB. This then allowed to input an electrical signal with a known frequency and amplitude to one of the two top electrodes of the device. The resulting displacement can then be measured with the DHM or the LDV.

The setup is shown in Figure 53.

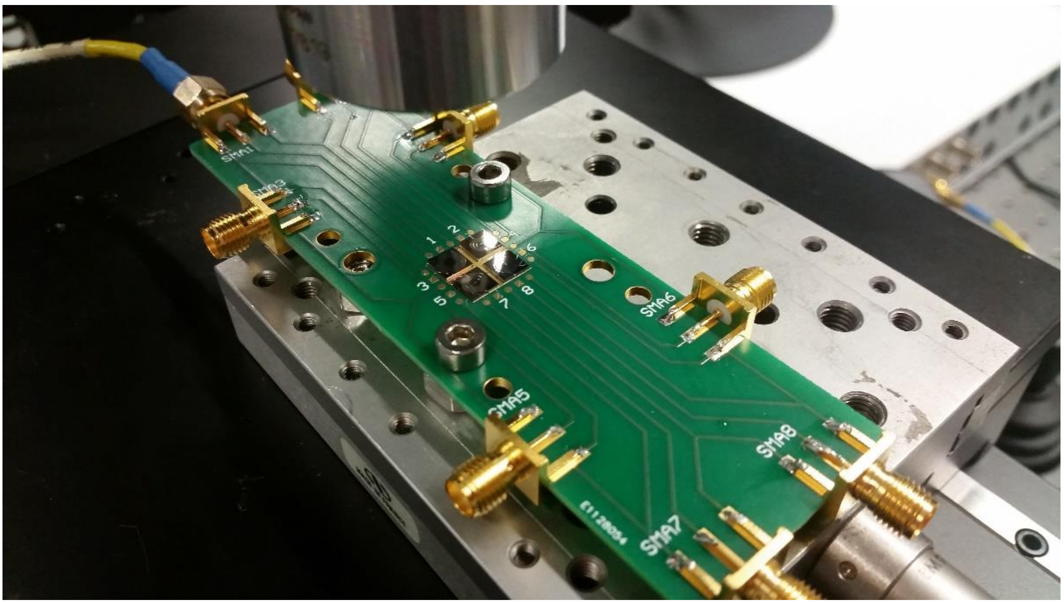


Figure 53: PCB with 4 wire-bonded devices. Each connector is connected to one of the top electrodes and to the ground of a device. In this picture a cable connects the connector 1 to the DHM.

Before being glued to the PCB, each chip was checked for short-circuits or for damaged top electrodes due to oxidation, and then the thickness of the silicon membrane was measured.

5.2 Device Selection

The first chip to be measured was from wafer n° 6781 as it was the first ready. One of the chips with three different membrane radii was chosen as it allowed to measure devices with the same membrane thickness. Four chips were checked for resistances, two of them had satisfactory bottom to top isolation and top to top contact. The selected chip, after wire-bonding, can be seen in Figure 54.

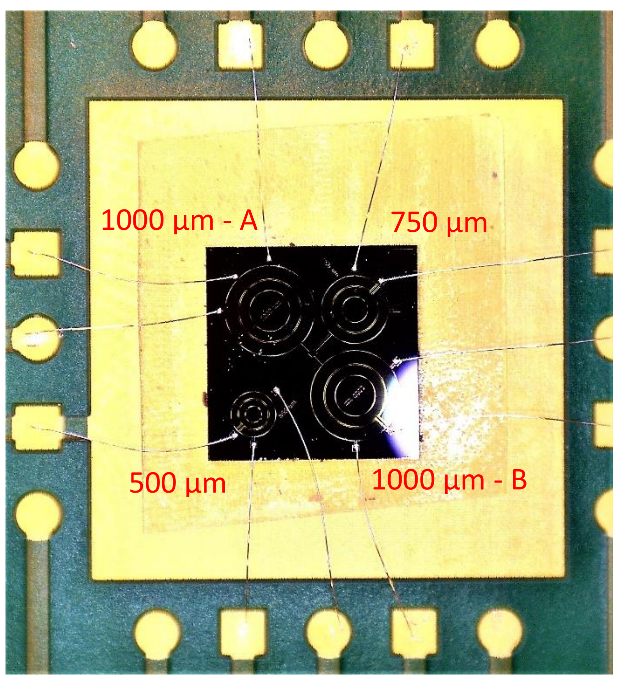


Figure 54: Chip from wafer n° 6781 on a PCB. The round pads of the PCB are connected to the ground, the square ones to the input. There are four devices on this chip, identified by their radius and by a letter for the 1000 µm ones.

The thicknesses of the membranes of this chip were obtained by subtracting the measured depths from the wafer thickness, which is 380 ± 5 µm. The etch depths are measured on 6 points on the membrane and on 6 points on the mass. The incertitude of the thicknesses is given by the standard deviation of this measurement added to the incertitude of the wafer thickness.

The result of those measurements is shown in the table below:

Device	t_{memb} [µm]	t_{mass} [µm]
500 µm	58 ± 8	306 ± 7
750 µm	52 ± 8	304 ± 7
1000 µm – A	55 ± 8	308 ± 8
1000 µm – B	54 ± 7	308 ± 8

In order to observe the effect of varying the radius of the devices, four devices with similar membrane thicknesses and larger radii – 1500 to 2250 µm – were selected. As they were all on different chips the membrane thicknesses can vary a lot.

The thicknesses of the selected devices are shown in this table:

Device	t_{memb} [µm]	t_{mass} [µm]
1500 µm	56 ± 6	308 ± 6
1750 µm	55 ± 7	307 ± 11
2000 µm	50 ± 10	302 ± 10
2250 µm	55 ± 7	308 ± 6

These thicknesses are in the same range as those of the first four devices which should allow to compare them. On average the membranes of the eight measured devices are 54 ± 8 µm thick and the masses 306 ± 8 µm.

The four chips were then wire-bonded as shown in Figure 55.

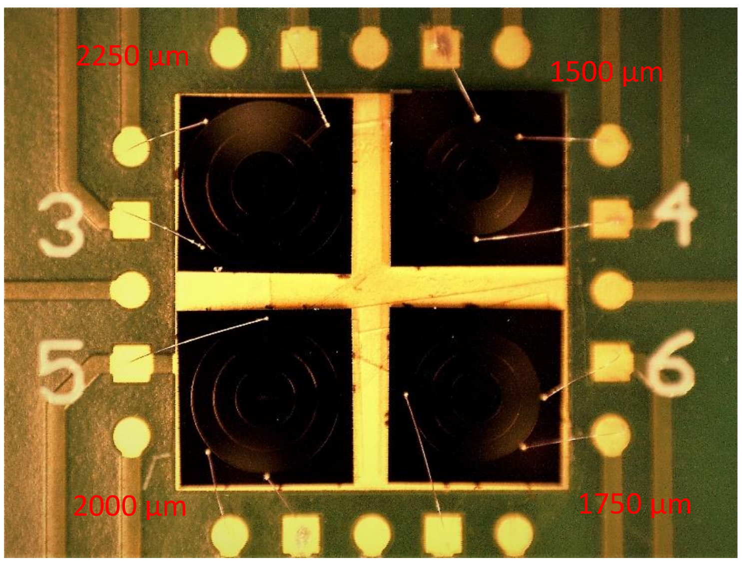


Figure 55: 4 chips with devices of different radius; 1500, 1750, 2000 and 2250 µm. Each one is connected has its two top electrodes connected to a square pad on the PCB and the ground connected to a circular pad.

6 Results and Discussion

6.1 Fabrication

The complete process was carried out for the three wafers with satisfactory results. Of the 594 chips, only 17 chips were damaged; 12 were etched through on wafer n° 6615 and 5 were broken during dicing on wafer n° 6781.

Most of the resistances measured showed a good isolation between the top and bottom electrodes, proving that the changes made to the process flow were effective in reducing the number of short-circuits.

Oxidation of the top electrodes resulted in some devices being uncharacterizable, as no electrical contact could be made on the top electrode. This issue is due to having molybdenum instead of platinum and exposing the wafers to too much O_2 plasma. However, the issue was very localized and could be avoided by reducing as much as possible the time during which the molybdenum is exposed to O_2 plasma.

6.2 Resonant Frequency

The resonance frequency of the eight devices was measured with the DHM and LDV which gave the same results.

The resonances frequencies of the devices were measured by driving the devices with an increasing frequency over a range. This allows to find a resonance peak, as shown in Figure 56.

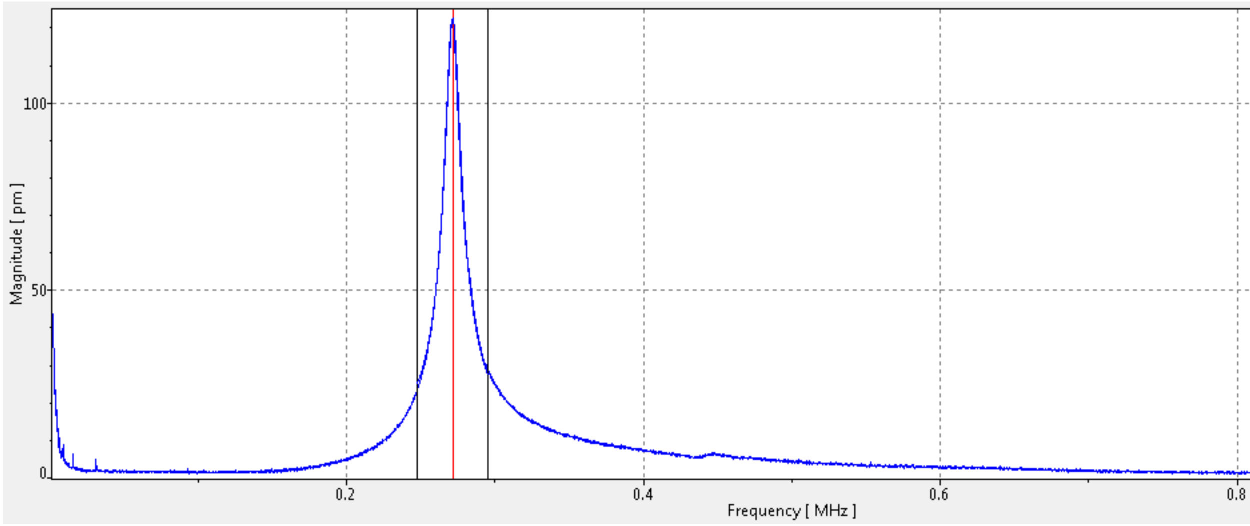


Figure 56: Response of the 750 µm device measured on the LDV. The measured frequency is in agreement with the one found with the DHM. The magnitude however is orders of magnitude smaller than what is expected

With the thicknesses of the measured chips known, it was possible to simulate the same devices on COMSOL to compare the FEM with the measurements. Simulations were done for all radii for three different thickness sets, which were chosen based on the average measured thicknesses, t_{memb} = 54 ± 8 µm and t_{mass} = 306 ± 8 µm:

- Average case: t_{memb} = 54 µm and t_{mass} = 306 µm

- Extreme case 1 (results in lower frequencies): t_{memb} = 46 µm and t_{mass} = 314 µm
- Extreme case 2 (results in higher frequencies): t_{memb} = 62 µm and t_{mass} = 298 µm

The measured and simulated frequencies are shown in Figure 57.

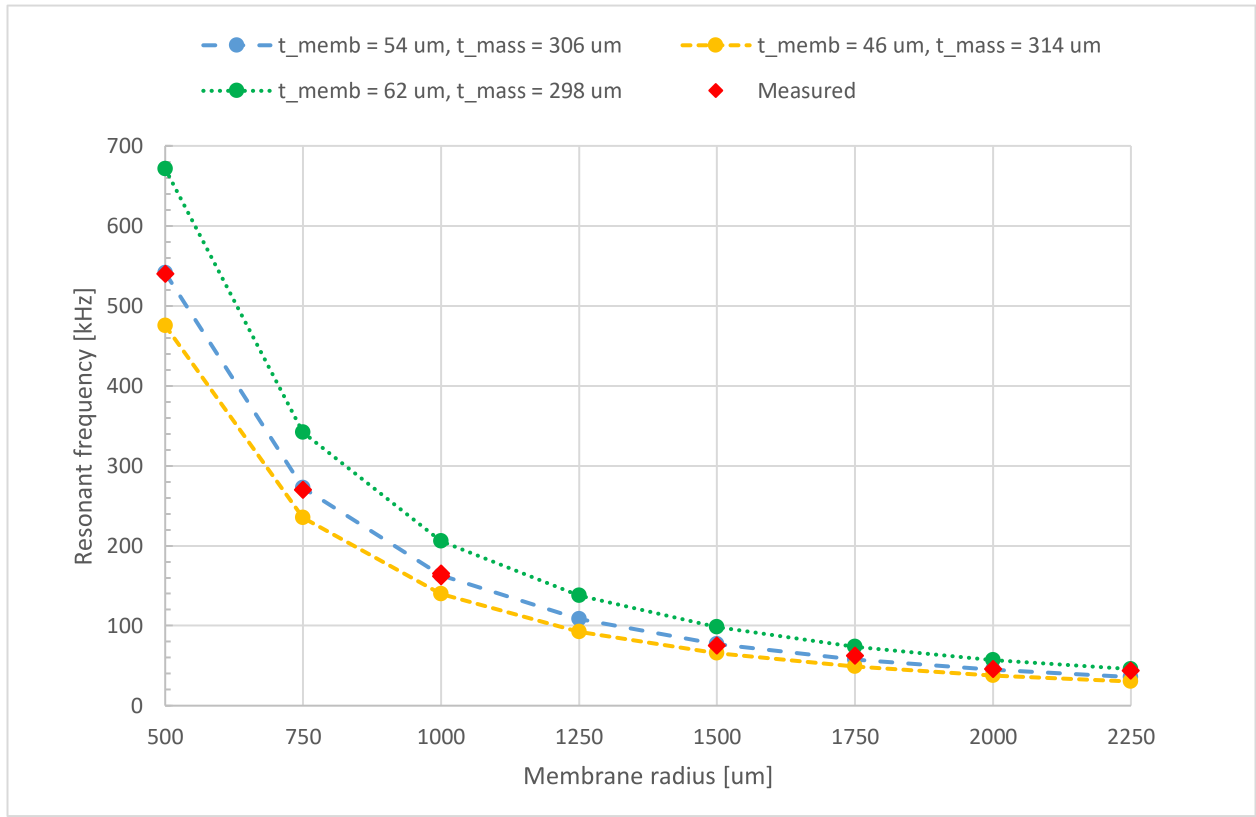


Figure 57: Resonant frequency as a function of membrane radius. Values simulated with the average and extreme membrane and mass thicknesses are presented with the measured values.

The measured values are very close to the simulated values, which means that the COMSOL model is a reliable tool to predict the resonant frequency and that the measurements of the thicknesses were accurate enough to find a corresponding model.

6.3 Displacement

The DHM allowed to get the amplitude of displacement for all the devices except for the 2250 µm one. It was not possible to measure the displacement with this tool, as the device is too big for the mass and the non-moving edge to be visible at the same time by the microscope, even when using a x5 objective. As the displacement on a DHM is obtained by using the phase shift of the reflected light between a reference point and the measured point, this made the measurement impossible.

The displacement amplitudes given by the LDV made no sense as they were all under 150 pm and orders of magnitude lower than the results found with the DHM.

The LDV allowed, however, to measure the quality factor of the devices in air.

In order to compare the measured displacement amplitude at resonance with the static displacement

simulated with COMSOL, the displacement at resonance is divided by the quality factor. The resulting values as well as the corresponding simulated displacement are shown in Figure 58.

To simulate the displacement, the following thicknesses were used: t_{memb} = 54 µm and t_{mass} = 306 µm. Three cases were simulated, one case with 1 V and -1 V applied to both electrodes respectively and two cases were only one electrode has a voltage applied to it.

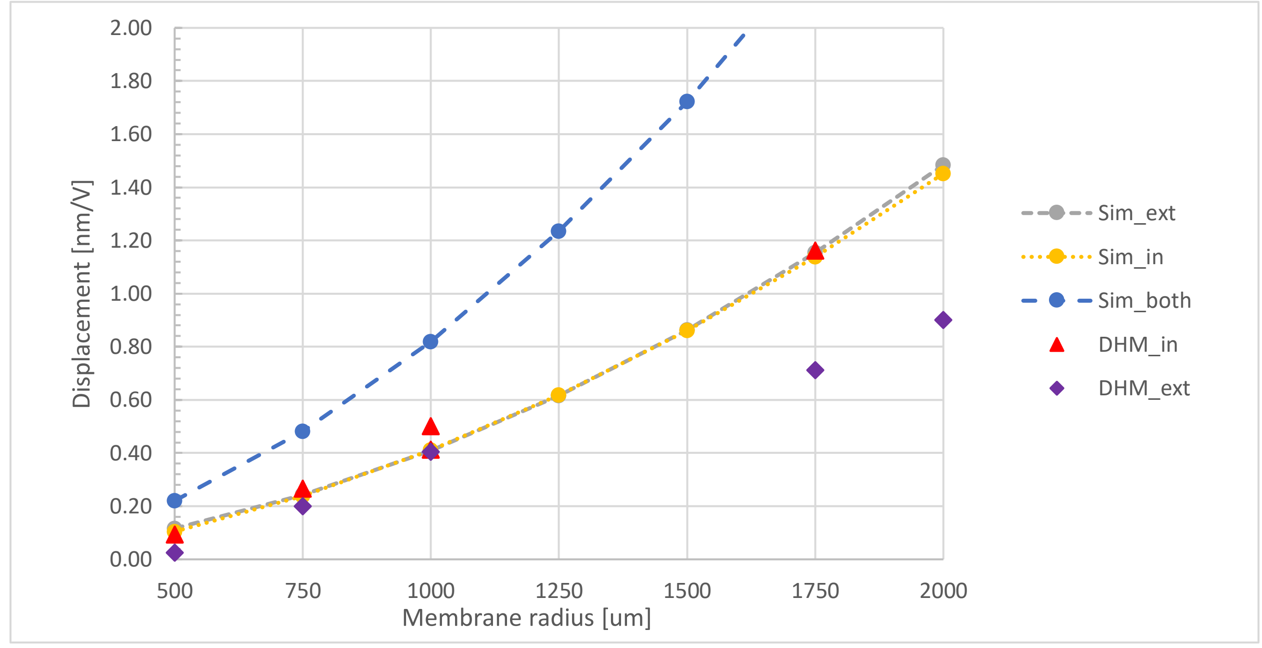


Figure 58: Displacement to voltage sensitivity as a function of membrane radius. Sim_in and Sim_ext are the simulated displacements when 1V is applied to the inner and external electrode respectively, Sim_both is when voltage is applied to both. DHM_in and DHM_ext are the displacements when a voltage is applied to the corresponding electrode, divided by the quality factor measured with the LDV.

Values for both electrodes of the 1500 µm device are not shown here, because the displacement was measured for the wrong frequency. The frequency response for the 2000 µm was very noisy and in the case where the internal electrode was driven, it was impossible to measure the displacement. The external electrode of the "1000 µm – B" device was damaged during measurements by applying a too high voltage by mistake (10 V), which is why only the result for the internal electrode is shown.

The results presented in Figure 58 show that the COMSOL model accurately predicts the electrical sensitivity of the devices.

However, this characterization step has shown that a DHM is not the most suited tool to measure this displacement, especially when the area of the device to be measured is large. The reason for the unexpectedly small amplitudes measured with the LDV should be investigated as using it would be much more efficient than using a DHM.

7 Conclusion

This project showed the possibility of using MEMS technology to miniaturize existing vibration sensors while keeping the same performances and confirmed the use of FEM as a suitable tool for designing those new sensors.

Based on previous experience, a new process flow was established and carried out, allowing to successfully fabricate MEMS piezoelectric accelerometers. Potential causes of process failures were also identified.

Characterization of the fabricated devices was started, and the measurements obtained showed a strong agreement with the values simulated with FEM. Characterization of more of the devices would allow to further confirm this observation.

Other designs were explored using FEM and would allow to increase the charge generation of the devices without changing the other characteristics.

Future work should be focused on finding a reliable way to measure the charge generation of the devices. The photolithography layout should be redone with characterization concerns in mind (Placement of electrical connections, size of the chips adapted to existing PCBs, identification numbers…). To make the fabrication of the devices repeatable and more precise, another way of creating the membranes should be used.

Myriam Käppeli

8 References

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9 Appendix

The following documents can be found here:

- Complete process flow
- Cleanroom runcard of the process

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☐ Semestral Project ☑ Master Project ☐ Thesis ☐ Other

Piezoelectric MEMS for Vibration Sensing

Description of the fabrication project

This fabrication project is to generate a prototype for a piezoelectric MEMS vibration sensor. Models in COMSOL will be used to finalize device layout and thicknesses, thus thicknesses provided below are subject to change. To start the process, we begin with a Si handle layer with SiO2 encapsulating this layer. The first step is the pattern a positive PR on the front side and then sputter AlN as a seed layer followed by Pt. Liftoff is conducted on the wet bench in Z1 and then sputtering of AlN and then Pt is conducted to complete the piezoelectric-electrode layer. The next step is to pattern PR again and use the STS to etch the Pt and AlN layers to open up the middle of the device to gain access to the original SiO2 layer. PR is stripped and a new PR layer is spun and patterned with holes on the outside of the SiO2 opening. SPTS is used to etch the SiN layer through the exposed holes in the PR. The PR is then stripped and a 5 um parylene layer is added to the front side to protect it during later process steps. The wafer will now be processed on the backside. First, PR is patterned to create a circular SiO2 opening. SPTS is used to etch the oxide layer to expose the Si handle layer. Next, 5 um thick PR is patterned with a 185 um diameter of PR in the middle of the Si opening. AMS 200 SE is used to etch the Si layer until approximately 20 um is left. The PR is then stripped and then AMS 200 SE is used to etch the rest of the Si layer. We then return to the front side to remove the protective parylene layer.

Technologies used *!! remove non-used !!*
Sputtering, evaporation, positive resist, Lift-off, Dry etching, Wet etching, Direct laser writing, Dicing

Ebeam litho data - Photolitho masks - Laser direct write data			
Mask #	**Critical Dimension**	**Critical Alignment**	**Remarks**
1st layer	**50 um**	-	Lift-off Pt, ground electrode
2nd layer	**25 um**	10 um	AlN+Pt structuration, top electrode
3rd layer	**1000 um**	10 um	Oxyde structuration, backside accelerometer radius
4th layer	**250 um**	10 um	Si structuration, membrane and mass

Substrate Type
100/P/DS/1-10 TTV5 – Wet oxide 500 nm

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Interconnections and packaging of final device

Thinning/grinding/polishing of the samples is required at some stage of the process.

☑ No ☐ Yes => confirm involved materials with CMi staff

Dicing of the samples is required at some stage of the process.

☐ No ☑ Yes => confirm dicing layout with CMi staff

Wire-bonding of dies, with glob-top protection, is required at the end of the process.

☑ No ☐ Yes => confirm pads design (size, pitch) and involved materials with CMi staff

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Step-by-step process outline

Step	Process description	Cross-section after process
00	**Start:** 500 nm oxide (SiO_2), 380 µm handle layer (Si)	Si SiO_2 PR Pt AlN C_8H_8
01	*Frontside* **Photolithography 1st layer** Machine: *EVG 150 + MLA 150* PR : *0.4 µm LOR A5 + 1.1µm AZ1512*	Si SiO_2 PR Pt AlN C_8H_8
02	*Frontside* **Sputtering:** *Seed layer (AlN) + 50 nm Pt* Machine: *Spider 600 + Plade «Solvent» Z1 Wet Bench LOR*	Si SiO_2 PR Pt AlN C_8H_8
03	*Frontside* **Lift-off** Equipment: *Plade «Solvent» Z1 Wet Bench LOR*	Si SiO_2 PR Pt AlN C_8H_8
04	*Frontside* **Sputtering:** *100 nm AlN + 50 nm Pt* Machine: *Spider 600*	Si SiO_2 PR Pt AlN C_8H_8
05	*Frontside* **Photolithography 2nd layer** Machine: *ACS 200 + MLA 150* PR : *AZ ECI 3007 – 1.5 µm*	Si SiO_2 PR Pt AlN C_8H_8

06	*Frontside* **Plasma etching:** *50 nm Pt + 100 nm AlN* Machine: *STS Multiplex ICP*	Si SiO_2 PR Pt AlN C_8H_8
07	*Frontside* **Resist stripping** Equipment: *Tepla GiGAbatch (60s resist strip high), Remover 1165 UFT wetbench Z2*	Si SiO_2 PR Pt AlN C_8H_8
08	*Frontside* **Evaporation deposition:** *5+ µm parylene*	Si SiO_2 PR Pt AlN C_8H_8
09	*Backside* **Photolithography 3rd layer** Machine: *EVG 150 + MLA 150* PR: *1.5 µm AZ 1512*	Si SiO_2 PR Pt AlN C_8H_8
10	*Backside* **Plasma etching:** *500 nm SiO2* Machine: *SPTS APS*	Si SiO_2 PR Pt AlN C_8H_8
11	*Backside* **Resist stripping** Equipment: *Remover 1165 UFT wetbench Z2*	Si SiO_2 PR Pt AlN C_8H_8

12	*Backside* **Photolithography 4th layer** Machine: *EVG 150 + MLA 150* PR: *5 µm AZ 9260*	Si SiO_2 PR Pt AlN C_8H_8
13	*Backside* **Plasma etching:** *260 - 370 µm Si* Machine: *AMS 200*	Si SiO_2 PR Pt AlN C_8H_8
14	*Backside* **Resist stripping** Equipment: *Remover 1165 UFT wetbench Z2*	Si SiO_2 PR Pt AlN C_8H_8
15	*Backside* **Plasma etching:** *80 µm Si* Machine: *AMS 200*	Si SiO_2 PR Pt AlN C_8H_8
16	*Frontside* **Plasma etching:** *5+ µm parylene* Machine: *Tepla GiGAbatch*	Si SiO_2 PR Pt AlN C_8H_8

Remarks:

Projet : PDM
Operator : Myriam Käppeli
Created : 18.09.2019 **Last revision** : 06.11.2019
Substrates : Silicon 100/P/DS/1-10 TTV5 - Wet Oxide 500nm

Step N°	Description	Equipement	Program / Parameters	Target	Remarks	Duration
0	**WAFER PREPARATION**					
0.1	Stock out					
0.2	Check					
1	**PHOTOLITHOGRAPHY 1st layer - GND Electrode Front Side Mask**					
1.1	LOR + AZ 1512 Coating	Z6/EVG150	AZ1512_on__LOR_400nm			18 min
1.2	PR expose	Z5/MLA150	Kaeppeli_FirstLayer, Dose: 75 mJ/cm2 Defocus: -2, fast			
1.3	PR develop	Z6/EVG150	Lift-Off_LOR_Std 2x Dev_AZ1512onLOR_400nm		x2	5x2 =10 min
1.4	Rinse	DI water				
1.5	Back-side cleaning	IPA				
1.6	Inspection	Z1-Z6/Microscope				
2	**SPUTTERING**					
2.1	AlN Deposition	Z4/SPIDER600	1500 W, 23 sec (Room temp)	15 nm		
2.2	Pt Deposition	Z4/SPIDER600	1000 W, 13 sec (Room Temp)	50 nm		
2.3	Inspection	Z6/uScope				
3	**LIFT-OFF**					
3.1	Remover 1165 + US	Z1/Plade_Solvent	Bac US	1 min		
3.2	Remover 1165	Z1/Plade_Solvent	PT 1	20h		
3.3	Remover 1165 + US	Z1/Plade_Solvent	Bac US	1 min		
3.4	IPA	Z1/Plade_Solvent	PT 2	2 min		
3.5	Fast Fill Rinse	Z1/Plade_Solvent	DI Rinse			
3.6	Trickle tank	Z1/Plade_Solvent	DI Rinse			
3.7	Optical Inspection	Z1,Z6/Microscope				
4	**SPUTTERING**					
4.1	AlN Deposition	Z4/SPIDER600	1500 W, 120 sec (300 C)	100 nm		
4.2	Pt Deposition	Z4/SPIDER600	(Room Temp)	50 nm		
4.3	Inspection	Z6/uScope+Z4/Profilometer				
5	**PHOTOLITHOGRAPHY 2nd layer - Top electrode**					
5.1	Coating AZ ECI 3007	Z1/ACS200	Recipe 0325: AZ ECI 3007:1.5um with HMDS and EBR			<5 min
5.2	Exposure	Z16/MLA150	200 mJ/cm^2, defocus -1, fast			
5.3	Development	Z1/ACS200	Recipe 0825			
5.4	Cleaning backside DI	Z1,Z2/Wetbench	SRD - program 1			
5.5	Inspection	Z1,Z6/Microscope	Resolution and alignment			
6	**PLASMA ETCHING**					
6.1	Pt + AlN etch	Z2/STS	AlN_etch, 2 min (1m20+20s=1m40)	50nm + 100nm	Wait until 2nd color change	
6.2	Inspection	Z15/Filmetrics	SiO2 on Si	<500 nm		
7	**RESIST STRIPPING**					

7.1	Plasma O2 clean	Z2/Tepla GiGAbatch	PR_strip_high_1min			
7.2	Remover 1165	Z2/UFT_Resist	Bath 1 : main remover	5min, 70°C		
7.3	Remover 1165	Z2/UFT_Resist	Bain 2 : clean remover	5min, 70°C		
7.4	Fast fill rinse	Z2/UFT_Resist	DI Rinse			
7.5	Trickle tank	Z2/UFT_Resist	DI Rinse			
7.6	Inspection	Z6/Microscope				
7b	**CHECK ISOLATION AND RESISTANCE**					
7b.1	Remove wafers from the cleanroom					
7b.2	Measure resistance top-bottom	Probe station ANEMS		> 10^4 Ohm		
7b.3	Measure resistance top-top and bottom-bottom	Probe station ANEMS		< 10^4 Ohm		
7b.4	Bring wafers back					
7b.5	Clean wafers	Z2/Wetbench	SRD - program 1			
8	**PARYLENE COATING - FRONTSIDE**					
8.1	Apply UV tape	Z11/UV tape equipment	Put UV tape on frontside			
8.2	Parylene coating	Z10/Comelec-C-30-S	5+ um, done by CMi thursdays/fridays			1 day
8.3	Remove UV tape	Z11/UV tape equipment				
9	**PHOTOLITHOGRAPHY 3rd layer - SiO2 backside opening**					
9.1	HMDS	Z6/HMDS oven				23 min
9.2	AZ 1512 coating	Z6/EVG150	AZ1512_1to2um_Std_NoDehydrate --> AZ1512_1um5_NoEBR	1.5 um		
9.3	Exposure	Z16/MLA150	123 mJ/cm^2, defocus -2		Mirror the layer	13 min/w
9.4	Development	Z6/EVG150	Dev_AZ1512_1um3to1um7			<5 min/w
9.5	DI rinse	Z2/Wetbench	SRD - program 1			
9.6	Inspection	Z6/Microscope				
10	**PLASMA ETCHING**					
10.1	SiO2 etching	Z2/SPTS	SiO2 PR 3:1	500 nm	endpoint+10s	1m37s
11	**RESIST STRIPPING**					
11.2	Remover 1165	Z2/UFT_Resist	Bath 1 : main remover	5min, 70°C		
11.3	Remover 1165	Z2/UFT_Resist	Bain 2 : clean remover	5min, 70°C		
11.4	Fast fill rinse	Z2/UFT_Resist	DI Rinse			
11.5	Trickle tank	Z2/UFT_Resist	DI Rinse			
11.6	Dry	Z2/Wetbench	SRD - program 2			
11.6	Inspection	Z6/Microscope				
12	**PHOTOLITHOGRAPHY 4th layer - Si first etch**					
12.1	HMDS	Z6/HMDS oven				23 min
12.2	AZ 9260 coating	Z6/EVG150	AZ9260_5um_NoEBR	5um	8min rehydr. time before exposure	
12.3	Exposure	Z16/MLA150	350 mJ/cm^2, defocus 2		Mirror the layer	13 min/w
12.4	Development	Z6/EVG150	SprayDev_5um_AZ9260			5 min/w
12.5	DI rinse	Z2/Wetbench	SRD - program 1			
12.6	Post-bake	Z16/Oven	85°C 3 hours			
12.7	Inspection	Z6/Microscope				
13	**PLASMA ETCHING**					

13.1	Si etching	Z2/AMS 200	SOI_accurate++	wafer dependent		
13.2	Inspection	Z15/Filmetrics	Si			
14	**RESIST STRIPPING**					
14.1	Plasma O2 clean	Z2/Tepla GiGAbatch	PR_strip_high_1min			
14.2	Remover 1165	Z2/UFT_Resist	Bath 1 : main remover	5min, 70°C		
14.3	Remover 1165	Z2/UFT_Resist	Bain 2 : clean remover	5min, 70°C		
14.4	Fast fill rinse	Z2/UFT_Resist	DI Rinse			
14.5	Trickle tank	Z2/UFT_Resist	DI Rinse			
14.6	Inspection	Z6/Microscope				
15	**PLASMA ETCHING**					
15.1	Si etching	Z2/AMS 200	SOI_accurate++	wafer dependent		
15.2	Inspection	Z15/Filmetrics	Si			
16	**PLASMA ETCHING**					
16.1	Parylene	Z2/Tepla GiGAbatch	PR_strip_high, >5min	5 um	takes more time than 1 min/um	
16.2	Inspection	Z6/Microscope	Si			