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Steep Slope Transistors for Quantum Computing

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Abstract

In this paper we will present and discuss the potential of steep slope transistors to serve at cryogenic temperature: (i) the electronic design that is needed for qubit error correction and/or interfacing and (ii) to serve as ultra-sensitive charge detectors and potentially replace single electron transistors and/or CMOS for certain electronic functions.

We suggest that among the various categories of steep slope devices, the heterojunction tunnel FETs compatible with CMOS platforms form a class of device candidates capable to play an important role in the future quantum computing (QC) down to cryogenic temperatures. The paper will investigate and discuss the potential merits of these devices.

(Keywords: *Steep slope devices, Tunnel FETs, CMOS, charge sensor, qubit, quantum computing*)

Introduction: the future of computation platforms and the role of steep slope devices

Today, three main computation platforms are envisioned to address the Internet of Things (IoT) needs for the future [1]: (i) nanoscale CMOS, (ii) neuromorphic computing [2] and quantum computing [3]. Fig. 1 depicts a vision in which all the three will coexist while taking particular tasks at three different levels: cloud, fog and edge computing, according to their particular merits. CMOS remains the only mature computation platform capable to address all these levels but it may be complemented and, potentially, overpassed in efficiency at some particular tasks including intense computations for physics and mathematical, pattern recognition, artificial intelligence, personalized and preventive smart healthcare, etc., by quantum or neuromorphic computing platforms.

In the quest for more energy efficiency based on beyond CMOS, steep slope transistors form a new class of devices capable to achieve subthermionic inverse subthreshold slopes (i.e. less than 60mV/decade at room temperature, T=300K), being considered an enabling technology for scaling the voltage supply down to 100mV and providing better energy efficiency in digital and analog IC design [1,4]. Among them, tunnel FETs [5], negative capacitance FETs [6] and Nano-Electro-Mechanical switches [7] are the most advanced and have been demonstrated in many experimental embodiments. The main considered applications are usually in the digital ICs with substantially reduced energy consumption per switched/computed bit of information. Among these categories, Tunnel FETs have the particular property of having little dependence on the temperature of their subthreshold slope since the dominant current component is the band-to-band tunneling (BTBT). Moreover, in tunnel FETs having high direct BTBT rates of tunneling it is expected that the BTBT current component will provide a transistor operation down to deep cryogenic temperatures. At such low temperatures, the detrimental trap-assisted tunneling (TAT) is inhibited and a steep slope behavior would be easier to achieve. Recent claims that cryogenic CMOS can support the quantum computing down to temperatures of 30mK would then greatly benefit from including tunnel FETs fabricated on CMOS platforms to serve various QC tasks.

Moreover, a tunnel FET switch that has a steep slope would also have *both* the great potential to become an ultra-sensitive charge sensor and the capability to offer excellent analog amplification at ultra-low voltage (below 500mV) and current levels down to the picoAmpere, where CMOS is usually facing big difficulties.

Tunnel FETs at Cryogenic Temperatures

According to [3, 8] a digital platform for controlling and reading-out of a quantum processor is made of a front-end for multiplexing and demultiplexing, amplification, analog-to-digital conversion (ADC) and digital-to-analog conversion (DAC). In principle, QC implementations prefer to have quantum processors and interfacing electronics operating on the same chip, therefore at similar temperatures, in order to reduce off-chip interconnects. However, for practical reasons, the current strategies are based on semiconductor qubits operated at sub-100 milliK while the electronic circuitry operates between 1 and 10K. This sets a feasibility and optimization technological target for cryogenic CMOS chips.

In Fig. 2, we report the experimental transfer characteristics of a Ge-source Tunnel FET device (fabricated by Jülich Research Centre, [9]) measured from room temperature down to 300K. The tunnel FETw investigated here were previously reported by Blaeser et al. [9] and has 5 nm SiGe grown on 15 nm silicon-on-insulator (SOI) substrate. Due to the ultra-thin silicon thin and oxide, the substrate can be used for efficient back gating, like in a fully depleted SOI double gate tunnel FET.

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The figure shows that once the trap-assisted-tunneling (TAT) degrading effect on the subthreshold is removed by lowering the temperature, the transistor swing, defined as $(d\log I_D/dV_G)^{-1}$, becomes quasi-independent of temperature and very abrupt as confirmed by the plot of Fig. 3 (the plots at 180K and 80K, last one close to liquid nitrogen, have almost identical swings), which shows that the swing could reach subthermionic values at low values of the drain current. The only remaining dependence of the BTBT current on temperature is via the semiconductor band gap small quasi-linear variation with T. The combined abruptness and stability of the swing at cryogenic temperatures makes tunnel FETs an excellent candidate for interfacing electronics with qubits. In Fig. 4 we report such SiGe/Si tunnel FET, operating at 10K and achieving a steep slope a low current levels. This demonstrates the capability of the tunnel FET family of devices to answer the needs of building interfacing low power electronics operating in the low Kelvin range of temperatures for QC.

Qubit sensing with a steep slope Tunnel FET

We are reporting that in a double gate configuration, a tunnel FET can be transformed in a highly sensitive charge sensor [1, 10] by biasing one gate in the subthreshold regime of operation (where the steep slope occurs) while the opposite gate is coupled capacitively to a quantum dot that serves to sense the qubit state. In such charge-sensing configuration a tunnel FET could finally replace other solutions proposed in the past such as single electron transistors [11] or multi-gate SOI MOSFETs [8]. In Fig. 5 we report low temperature characteristics of a tunnel FET when the front gate voltage is swept at various back gate voltages. It is clearly demonstrated that the threshold voltage of the tunnel FET is modulated by the back gate used here as a sensing gate. The sensing capability can be significantly improved by the appropriate design of the gate stacks and of their electrostatic coupling to achieve sensitivity and gain at very low currents and voltages, surpassing the SET and MOSFET capabilities.

Conclusion

In this paper, we have reported and discussed for the first time the tunnel FET capability to operate at cryogenic temperatures and to serve as a device building blocks for both interfacing electronics and as highly sensitive charge sensor. This opens a completely new field of applications for tunnel FETs and other steep slope devices.

Acknowledgments

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Fig. 1: Role of *CMOS and Beyond*, *Quantum Computing* and *Neuromorphic Computing* versus the demands of Edge, Fog and Cloud Internet of Things applications, supporting a vision of the future based on the co-existence of these three advanced computation platforms, with different computational tasks and time horizons.

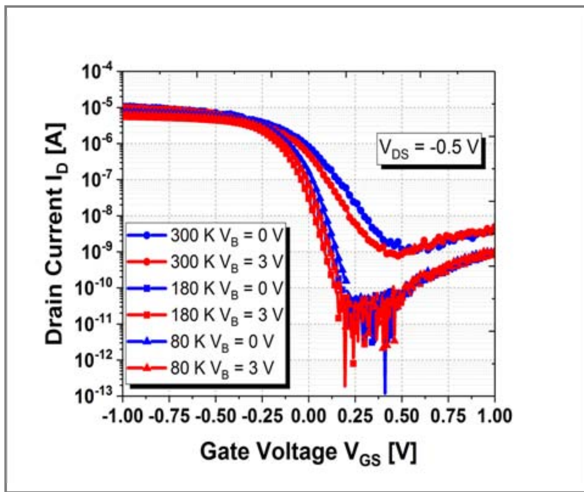

Fig. 2 Experimental transfer characteristics of a DG tunnel FET with Ge source at 300K, 180K and 80K. At cryogenic temperature the TAT is removed and only BTBT exists.

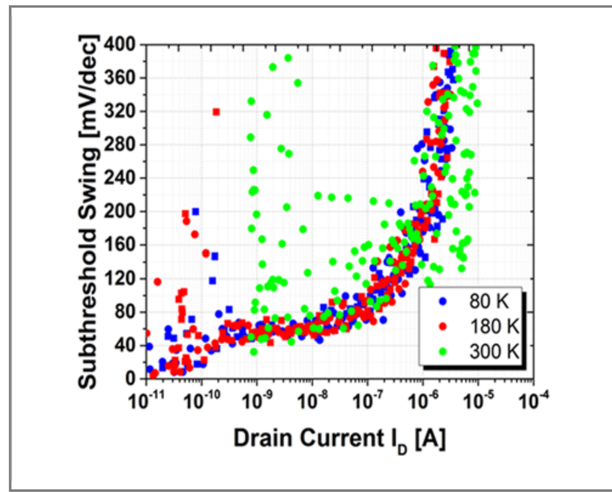

Fig. 3 Subthreshold slope of the device reported in Fig.1: BTBT offers step slope and temperature quasi-independent swings at cryogenic temperatures (180 and 80K, in our experimental investigation).

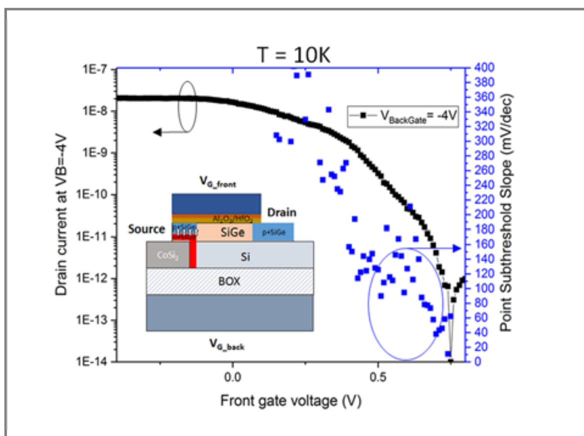

Fig.4 Experimental transfer characteristics of a tunnel FET with Ge source demonstrating operation at 10K and the corresponding subthreshold swing.

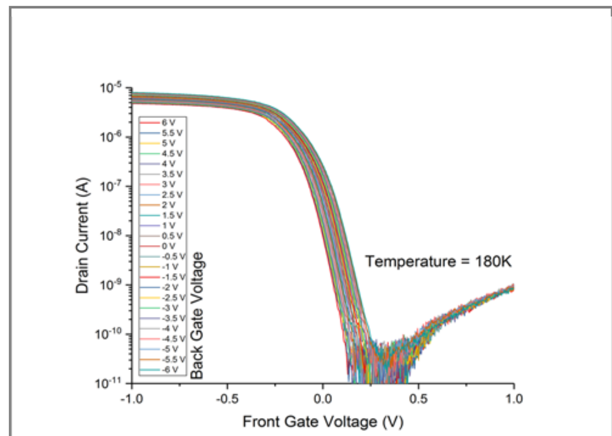

Fig 5. Experimental front gate transfer characteristics of a tunnel FET at 180K with the back gate bias as a parameter, suggesting the use as a charge sensor.