Experimental Details of a Steep-Slope Ferroelectric InGaAs Tunnel-FET with High-Quality PZT and Modeling Insights in the Transient Polarization

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***Abstract*—The steep-slope ferroelectric tunnel-FET (SS-FeTFET), consisting of an InGaAs TFET with sub-60 mV/dec subthreshold swing (SS) at room temperature and an externally connected high-quality single-crystalline PZT capacitor, displays improved SS compared to the standalone TFET. In our manuscript, we describe the measurement procedure and measurement results of this SS-FeTFET in great detail. To quantitatively extract the ferroelectric polarization during voltage sweeps, device simulations of the TFET are combined with the SS-FeTFET measurement results. Finally, qualitative insight in some pecularities of the experimental observations are given, like the apparent coercive voltage which is larger in the SS-FeTFET than in the standalone ferroelectric, the shape of the polarization during voltage sweeps and the small polarization hysteresis loop at voltages close to the apparent coercive voltage.**

***Index Terms*—Tunnel-FET (TFET), III-V semiconductor, ferroelectric (FE), steep-slope.**

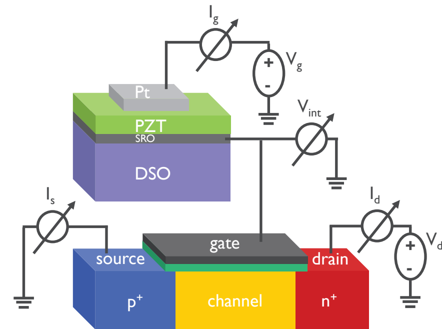

Fig. 1. Schematic of the measurement setup consisting of an external FE (PZT) connected to the gate of an InGaAs TFET. The source and drain current (I_s and I_d) of the TFET are monitored, together with the 'gate' current I_g of the ensemble device and the internal voltage V_{int}.

I. Introduction

ENERGY-EFFICIENT logic devices are desired in many application areas, both in conventional hybrid logic applications as well as in internet-of-things applications [1]. Among the candidates to decrease the energy consumption below MOSFET levels, the tunnel-FET (TFET) is a promising device [2]–[4]. It can achieve sub-60mV/dec subthreshold swing (SS) by using the forbidden bandgap to remove the thermal tail of carriers injected in the channel. Ferroelectrics (FE) used as gate dielectric promise to decrease the SS of a FET too, when the FE polarization switching results in larger channel potential changes than the externally applied gate voltage changes [5]–[9]. Both mechanism have been combined successfully in a steep-slope FE TFET (SS-FeTFET), and the figures of merit have been focused on extensively in Ref. [10].

In this manuscript, we provide full detail in Section II to IV on the experimental results and the experimental procedure used to extract the slope steepening behavior of a planar $In_{0.53}Ga_{0.47}As$ TFET connected to a high-quality PZT FE. The transient polarization extraction is for the first time based on full TCAD simulations, making the values more quantitative, as discussed in Section V. Finally, in Section VI, a more simplified simulation setup is used to give qualitative insight (1) in the expected value of the apparent coercive voltage of a FE embedded in a device, (2) in the change of the transient FE polarization with transient FE voltage, and (3) in the expected hysteresis.

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II. Experimental setup

The SS-FeTFET consists of an externally connected FE to the gate of a TFET (see Fig. 1). The FE stack consists of (110) $DyScO_3$ (DSO) as insulating substrate, a 20 nm thick $SrRuO_3$ (SRO) bottom electrode, 46 nm of high-quality FE $Pb[Zr_xTi_{1-x}]O_3$ (PZT) with up to 300 nm×1000 nm single domain sizes, and a 50 nm thick Pt top electrode with area $15 \times 15\,\mu m^2$. The fabrication flow of the FE stack is detailed in Ref. [10], together with results of material characterization techniques supporting the high quality of the PZT. The TFET is a planar all-$In_{0.53}Ga_{0.47}As$ p-i-n structure with a 0.8 nm EOT oxide stack and a metal gate. The active gate area is $2400\,\mu m^2$. Details of the fabrication flow are in Ref. [11].

To facilitate the description of the SS-FeTFET measurement procedure, the characteristics of the FE only (without connection to the TFET) are first detailed. In Fig. 2(a), the σ_{FE}-V_{FE} loops, as measured with a precision FE tester [12] at a cycle frequency of 100 Hz, are shown for applied voltage-extremes of V_{FE} = ±1.5 V and ±1.8 V. The surface charge density σ_{FE} is determined by the total polarization P_{FE} and the electric field E_{FE} across the FE as follows:

$$\sigma_{FE} = P_{FE} + \epsilon_o E_{FE} \quad (1)$$

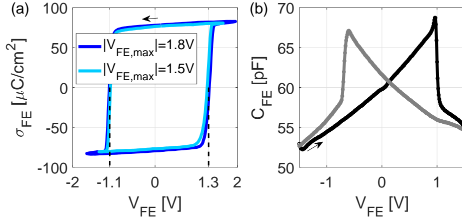

Fig. 2. (a) σ_{FE}-V_{FE} measurement, with σ_{FE} extracted as the integral of the measured current. Positive and negative coercive voltage V_c are indicated with a dashed vertical line. (b) C-V measurement of a $50{\times}50\,\mu m^2$ sample at 50 kHz (30 mV ac). The arrows indicate the starting point of the measured data and the direction of the sweep.

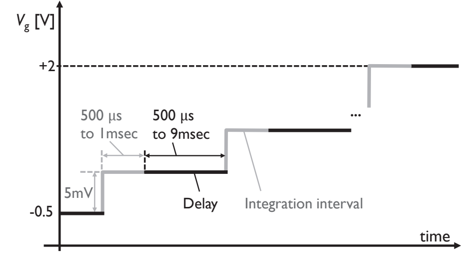

Fig. 3. Applied V_g-t during a forward sweep. The value of measured currents is determined as the average value over the integration interval. Measurement results are not observably affected by variations within the specified boundaries of delay or integration interval.

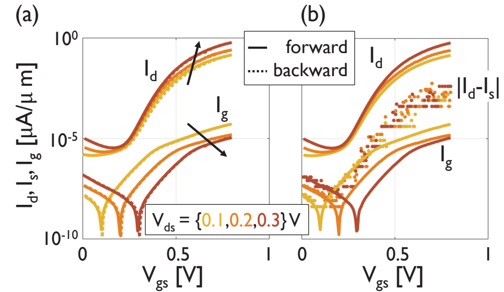

Fig. 4. Standalone TFET data: (a) drain and gate current for varying drain bias. Negligible difference between forward and backward sweep. (b) Comparison of the difference between source and drain current with I_d and I_g, indicating a small difference $|I_d$-$I_s|$ relative to I_d.

with ϵ_o the dielectric constant of free space. Given the very small contribution of the last term in Eq. 1 ($\leq 0.04\,\mu C/cm^2$), σ_{FE} is representative for P_{FE}. A remanent polarization $P_{FE,r}$ close to $\pm 80\,\mu C/cm^2$ is measured, the coercive voltages V_c are -1.1 V and +1.3 V, and the capacitance in the non-switching regime is about 6 μF/cm^2. Note that P-V loops at higher voltage extremes suffer too much from leakage currents to still be reliably representing the polarization. Fig. 2(b) shows the C-V measurement of the PZT sample. The leakage current at 1 V corresponds to a resistance of $10\,k\Omega$ (not shown).

The SS-FeTFET measurement procedure is as follows. First, the FE is separately cycled 20 times at 100 Hz and voltage-extremes of V_{FE} = $\pm$2 V, to ensure a uniform polarization throughout the sample. The pre-cycling is stopped after V_{FE} = -2 V, with a negative remanent polarization. The FE is then immediately connected to the TFET. Large gate voltage sweeps are applied to the FeTFET, which are expected to affect the starting FE polarization, until SS steepening is observed, after which the SS-FeTFET measurement is recorded. The latter consists of adjusting the drain voltage V_d to the desired voltage, followed by a step-wise (5 mV steps) increase in gate voltage V_g, as detailed in Fig. 3 for the forward sweep. The measurement data presented are stable for multiple sweeps. The device currents (I_g, I_s, I_d) and internal voltage V_{int} (see Fig. 1) are measured during forward and backward sweep.

Fig. 4 shows the characteristics of the $In_{0.53}Ga_{0.47}As$ TFET, subjected to a voltage sweep as in Fig. 3. The negligible clockwise hysteresis of the forward-backward loop of the I-V curves of Fig. 4(a) is a signature of very limited trap response at the time scale of the measurement. This observation is in agreement with our previous findings of significantly lower impact for TFET than for MOSFET of the high interface trap density D_{it} usually present at the midgap of InGaAs [13].

III. Standalone TFET characteristics

The difference between drain current I_d and source current I_s is small compared to the value of I_d or I_s itself, as illustrated in Fig. 4(b). In the off-state, the difference corresponds to the gate current I_g, indicating gate leakage, while in the on-state, the difference is proportional to the value of I_d.

IV. SS-FeTFET measurement results

The I-V characteristics of the SS-FeTFET, subjected to the voltage sweep of Fig. 3 after precycling the FE itself (see details in Section II), are shown in Fig. 5 for 2 values of V_{ds}. The figure also shows the I-V characteristics referenced to the internal voltage, for which an excellent match with the I-V characteristics of the standalone TFET can be seen. This match at multiple V_{ds} supports the credibility of the experimental data. The difference between I_d and I_s (not shown) is comparable to the data in Fig. 4(b) and always at least 1 order of magnitude smaller than I_d (except in a 200 mV voltage range around the current minimum in the forward sweep, where the difference decreases to minimally a factor 2).

As indicated in Fig. 5, the voltage across the FE, V_{FE}, is the voltage difference between the left and right I_d-V characteristics (see also Fig. 1). The change of V_{FE} and V_{int} with applied V_{gs} is shown in more detail in Fig. 6(a). Steepening of the SS-FeTFET versus the standalone TFET characteristics occurs, when V_{FE} decreases while V_{gs} is increasing, or vice versa. These voltage ranges during which steepening is expected are indicated in Fig. 6(a) for both forward and backward sweep. The same voltage ranges are indicated in Fig. 6(b), referenced to the standalone TFET characteristics (V_{gs} of the standalone TFET corresponding to V_{int} of the SS-FeTFET). As can be seen, there is steepening in the forward sweep up to higher currents than in the backward sweep. The amount of steepening can be seen from the overlay of the standalone TFET with the shifted I_d-V_{gs} characteristics in Fig. 6(b). Note that the backward sweep shows slope steepening, while V_{FE} remains close to the positive coercive voltage. A possible explanation is given in Section VI-C.

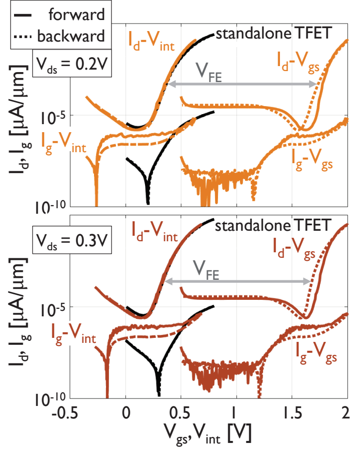

Fig. 5. Comparison of the standalone TFET data (black) with the SS-FeTFET data (brown) for V_{ds} = 0.2 V (top) and V_{ds} = 0.3 V (bottom). The I-V characteristics of the TFET inside the SS-FeTFET are identical to the standalone TFET data, which supports the correctness of the experiment. Currents are normalized to TFET device width.

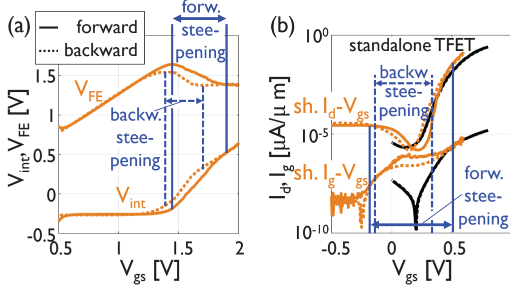

Fig. 6. (a) V_{FE} and V_{int} during the V_{gs} voltage sweep of the SS-FeTFET at V_{ds} = 0.2 V. Voltage ranges of forward and backward steepening are indicated. Note that the maximum achieved V_{FE} value is larger than in Fig. 2(a). A possible explanation for this observation is given in Section VI-A. (b) Standalone TFET and shifted I_d-V_{gs} characteristics of the SS-FeTFET (currents of 1×10^{-3} μA/μm coinciding in forward sweep), illustrating the steepening of the SS-FEFET with respect to the standalone TFET.

V. Polarization Extraction

The σ_{FE}-V_{FE} (P_{FE}-V_{FE}) data during a V_{gs} sweep of the SS-FeTFET are determined from a combination of the experimentally extracted V_{FE} value (see Fig. 6(a)) and the simulated average charge density $\overline{\sigma}_{TFET}$ on the TFET. The latter is linked to σ_{FE} as follows:

$$A_{FE}\sigma_{FE} = A_{FE}\sigma_{FE,initial} + A_{TFET}\epsilon_{ox}\left(\overline{E_{ox}} - \overline{E_{ox,initial}}\right) \quad (2)$$

with A_{FE} the area of the FE capacitor, A_{TFET} the active gate area of the TFET, $\overline{E_{ox}}$ the electric field at the metal-oxide interface of the TFET averaged over the gate area, ϵ_{ox} the dielectric constant of the TFET oxide and $\overline{\sigma}_{TFET} = \epsilon_{ox}\overline{E_{ox}}$. Note that leakage through the FE or the TFET's gate has been neglected [14], as the change in σ_{FE} during the steepening due to these leakage currents is estimated to be ≤ 0.02 μC/cm^2.

The TFET simulations are performed with the TCAD package SDevice from Synopsys [15]. Fermi levels in $In_{0.53}Ga_{0.47}As$ are based on the effective masses of the (valence band) heavy-hole, light-hole and split-off band and the effective masses of the (conduction band) Γ-band, L-valley and X-valley, including non-parabolicity corrections for all bands. Fermi-Dirac statistics are used. Apart from the drift-diffusion equations and a basic carrier mobility model, only the dynamic non-local band-to-band tunneling (BTBT) model is included. Details of trap-assisted tunneling and Shockley-Read-Hall generation-recombination, which are expected to dominate the ambipolar current, are not included in the simulation, as no reliable calibration data are available for the given process flow. To take into account quantization effects in the conduction band at the semiconductor-oxide interface near the tunnel junction, the InGaAs TFET is implemented with an oxide thickness equal to the measured CET (1.8 nm, resulting in C_{ox} = 46 pF) instead of to the EOT (0.8 nm). This approach leads to a good match of the simulated data with the BTBT-dominated experimental I-V characteristics up to V_{gs} = 0.4 V (see Fig. 7). Capturing the full drain-voltage dependent I-V characteristics of a TFET is not straightforward, given the strong dependence of the tunneling process on the 2-dimensional doping profile at the source-channel interface. A good match of the onset region of tunneling ensures that the band bending at the source-channel region and hence the conduction band level in the channel is well captured. The latter remains fairly constant throughout the entire channel and determines the electric field across the TFET's oxide.

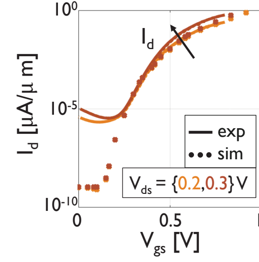

Fig. 7. Comparison of the experimental (solid) and simulated (symbols, band-to-band tunneling only) I-V characteristics of the InGaAs TFET. The agreement is very good in the onset region of tunneling up to V_{gs} = 0.4V.

The simulation platform is used to extract $\overline{E_{ox}}$ for all values of V_{int} (see Fig. 8(a)), measured at the gate electrode of the TFET during the forward and backward V_{gs} sweep of the SS-FeTFET (see Fig. 8(b)). The simulated $\overline{E_{ox}}$ values, transformed into σ_{FE} variations using Eq. 2, and the experimentally measured V_{FE} data of Fig. 8(c), allow to determine σ_{FE} versus V_{FE} during the V_{gs} sweep of the SS-FeTFET (see Fig. 8(d)). Note that in Ref. [10], a more primitive polarization extraction had been used, which was therefore less quantitative.

Fig. 8(d) shows that during the initial part of the forward sweep between V_{FE} = 0.6 V and 1.5-1.6 V, and during the final part of the backward sweep between 1.4-1.5 V and 0.6 V, σ_{FE} is quasi constant, similar to the nearly-fixed σ_{FE} of the σ_{FE}-V_{FE} loop between negative and positive coercive voltage, shown in Fig. 2(a). During this part of the sweep, the V_{gs} voltage drop is almost entirely taken by the FE, as is also reflected in the experimental data of e.g. Fig. 6(a), which suggests a smaller variation of $A_{FE}\sigma_{FE}$ with V_{FE} than of $A_{TFET}\sigma_{TFET}$ with V_{int}. The maximum change in surface charge density σ_{FE} during the SS-FeTFET sweep is about 10% of the remanent

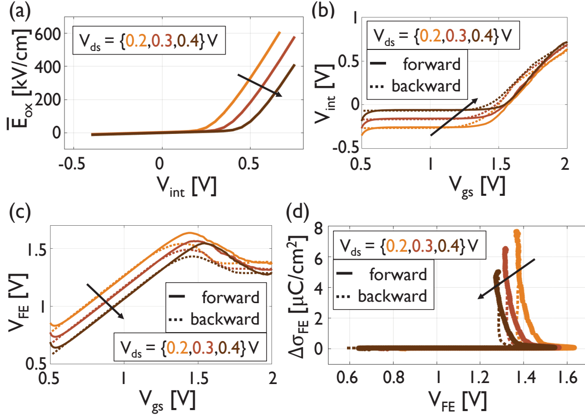

Fig. 8. (a) Simulated $\overline{E_{ox}}$ versus V_{int}, the latter covering the experimental range of V_{int} values for the different applied drain voltages (see (b)). (b) Experimentally measured V_{int} values during the V_{gs} sweep of the SS-FeTFET. (c) Experimentally measured V_{FE} values during the V_{gs} sweep of the SS-FeTFET. (d) Change in surface charge density on the FE, based on TFET device simulations, versus the experimentally extracted V_{FE} shown in (c).

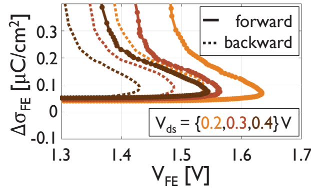

Fig. 9. Zoom-in around the value of voltage reversal of Fig. 8(d).

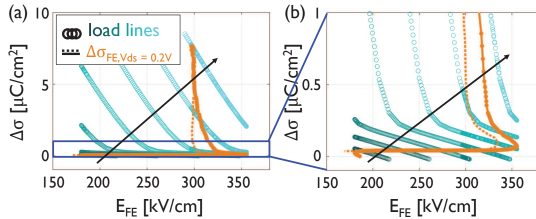

Fig. 10. Comparison of the area-renormalized TFET load lines (bluish circles) to the change in σ_{FE} (brown). A load line represents the $(\Delta\overline{\sigma}_{TFET}A_{TFET}/A_{FE})$-$E_{FE}$ variation for a given V_{gs}. The considered values of V_{gs} are V_{gs} = {0.6V:0.2V:2V}, with V_{ds} = 0.2 V. (a) Full view on $\Delta\sigma_{FE}$, (b) zoom-in on the nearly-constant initial and final variation of $\Delta\sigma_{FE}$.

polarization of $P_{FE,r} = 80\,\mu C/cm^2$. This change is smaller for larger V_{ds} values, because of the smaller average electric field over the gate area with increasing V_{ds} (see Eq. 2). The forward-backward sweep shows counter-clockwise hysteresis, which is a signature of FE polarization changes (as opposed to charge trapping), and a return at the end of the backward sweep to the initial V_{FE} and V_{int} values.

A zoom-in around the voltage reversal point of Fig. 8(d) is shown in Fig. 9. The maximum V_{FE} reached (the apparent V_c) is larger than the V_c observed in the σ_{FE}-V_{FE} loop of Fig. 2(a). A possible explanation is given in Section VI-A. Fig. 9 further shows that the initial V_{FE} decrease (forward sweep) occurs with very limited polarization increase, and the final V_{FE} increase (backward sweep) occurs with very limited polarization decrease. A possible explanation is given in Section VI-B.

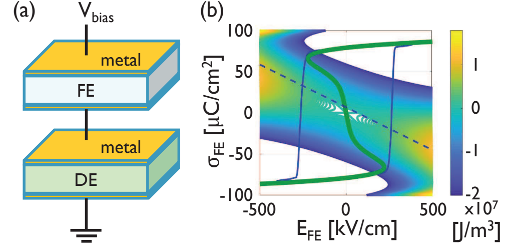

Fig. 11. (a) Schematic of a FE capacitor with 2 metal plates in series with a pure paraelectric capacitor (DE for dielectric) with 2 metal plates. (b) Corresponding solutions (σ_{FE}, E_{FE}) (solid green for stable solutions) of the setup of (a). The parameters of the FE have been adjusted to match the σ_{FE} - V_{FE} data of Fig. 2(a). The latter curve is repeated (solid blue), after a shift to make it symmetric with respect to E_{FE}, to illustrate the match. The dashed blue curve represents the load line of the DE capacitor. The underlying contour plot shows the energy of the setup in (a) for every (σ_{FE},E_{FE}) combination. It confirms the stability of the solid green curve.

Finally, the load lines of the TFET are compared to the change in FE surface charge density, $\Delta\sigma_{FE}$, for V_{ds} = 0.2 V in Fig. 10. The load lines give the set of ($\Delta\overline{\sigma}_{TFET}A_{TFET}/A_{FE}$, E_{FE}) values for a given V_{gs} applied to the SS-FeTFET, and are a combination of the constant displacement field equation at the node V_{int} and the conservation of voltage equation (V_{gs} = V_{FE} + V_{int}). The ($\Delta\overline{\sigma}_{TFET}A_{TFET}/A_{FE}$, E_{FE}) value at which a load line crosses the (brown) ($\Delta\sigma_{FE}$, E_{FE}) curve, corresponds to the V_{FE} value shown in Fig. 8(c) for the considered V_{gs}. The load lines cross the ($\Delta\sigma_{FE}$,E_{FE}) curve beyond the maximum E_{FE} value (forward sweep) with a less steep angle than the (brown) ($\Delta\sigma_{FE}$,E_{FE}) curve itself. If a uniform single domain is assumed, as well as a constant external capacitor, this requirement would result in stabilization of the FE polarization during the transition from -$P_{FE,r}$ to +$P_{FE,r}$, based on a feedback action of the external capacitor [5].

VI. Qualitative Insight in Polarization Variation

Based on a more simplified structure, a possible explanation for some qualitative trends, observed in the SS-FeTFET, is given. The simplified structure consists of a single-domain FE in series with a capacitor with fixed capacitance value (pure paraelectric component) (see Fig. 11(a)). The capacitor therefore replaces the TFET in the SS-FeTFET structure.

A. Increase in apparent coercive voltage inside SS-FeTFET

As discussed in literature [5], a capacitor in series with a FE (see Fig. 11(a)) induces a hysteresis-free FE transition from positive to negative polarization (green curve in Fig. 11(b)) or vice versa if $|d\sigma_{FE}/dV_{FE}| > C_{DE}$, provided a uniform (defect-free) single-domain FE material and a uniform thermal energy distribution is assumed, with coherent changes in the polarization over the entire domain. In the derivation made here, it is further assumed, as is typically done, that the steady-state double-well energy-polarization relation also holds during the polarization sweep. For simplicity, the area of the FE and DE capacitors are assumed to be the same. The load line shown in Fig. 11(b) then represents the (σ_{DE}, E_{FE}) combinations corresponding to a slightly positive V_{bias}. The slope of the load line with respect to the green curve in the

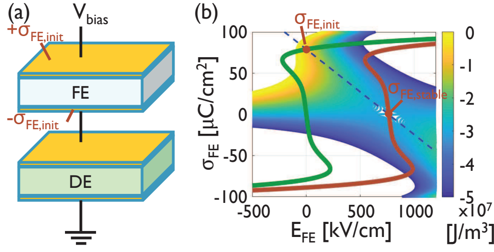

Fig. 12. (a) Schematic of a FE capacitor, which has an initial surface charge density $\sigma_{FE,init}$, equal to the $+P_{FE,r}$ value, in series with a DE capacitor. (b) Corresponding solutions (σ_{FE}, E_{FE}) (solid brown) of the setup of (a). The green curve is repeated from Fig. 11(b) for comparison. The underlying contour plot shows the energy for every (σ_{FE},E_{FE}) combination. It shows that if a FE capacitor, polarized to $+P_r$ (= with initial $\sigma_{FE,init}$ as indicated in the figure), with no voltage across, is connected to a DE capacitor with no voltage across, the system will evolve towards a positive voltage across the FE and therefore a negative voltage across the DE. The dashed blue curve represents the load line ($\sigma_{DE}+\sigma_{FE,init}$,$E_{FE}$) of the DE capacitor at V_{bias} = 0 V. The system will evolve along the load line to the more stable (σ_{FE},E_{FE}) combination.

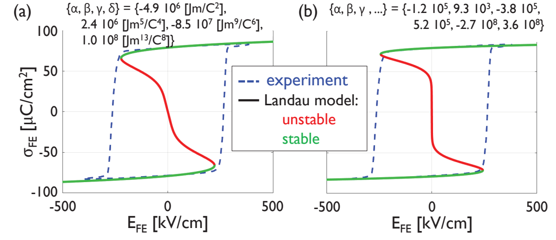

Fig. 13. (a) Landau model (solid, parameters as shown) matched to the experimental σ_{FE}-V_{FE} data (dashed), (b) Landau model (solid, parameters as shown) with a flatter section between $-E_{FE,c}$ and $+E_{FE,c}$, which results in a flatter section of the initial transient (red) part of the polarization. A standalone FE capacitor is considered, such that the (σ_{FE}, E_{FE}) curve has stable and unstable sections. The experimental data are shifted to make them symmetric with respect to E_{FE}.

polarization transition region reflects that $|d\sigma_{FE}/dV_{FE}| > C_{DE}$. (Note that a load line through the origin would correspond to V_{bias} = 0 V.) However, transition along the green curve of Fig. 11(b) only applies to a system where the total charge on the top plate of the DE capacitor has the same absolute value and opposite sign from the total charge on the bottom plate of the FE capacitor.

In Fig. 12, the same system is considered again, but now with an initial charge on the plates of the FE capacitor, such that the total charge on the top plate of the DE capacitor ($\sigma_{DE,init}$ = 0 C/cm^2) is no longer the same as on the bottom plate of the FE capacitor ($-\sigma_{FE,init}$ = $-P_{FE,r}$). We derived that the stable solutions of a system with $\sigma_{FE,init}$ on the FE capacitor, when assuming equal area and dielectric thickness of the FE and DE capacitor, are given by:

$$\begin{aligned}&(P_{\text{FE with }\sigma_{\text{FE,init}}}, E_{\text{FE with }\sigma_{\text{FE,init}}})\\&=(P_{\text{FE w/o }\sigma_{\text{FE,init}}}, E_{\text{FE w/o }\sigma_{\text{FE,init}}}+\sigma_{\text{FE,init}}/(\epsilon_o+\epsilon_{\text{DE}}))\end{aligned} \quad (3)$$

with ϵ_{DE} the dielectric constant of the DE capacitor. Eq. 3 is the result of an energy minimization of the Gibbs free energy:

$$\alpha P_{\text{FE}}^2+\beta P_{\text{FE}}^4-E_{\text{FE}}P_{\text{FE}}-\epsilon_o E_{\text{FE}}^2/2-\epsilon_{\text{DE}}E_{\text{DE}}^2/2 \quad (4)$$

with boundary conditions:

$$P_{\text{FE}}+\epsilon_o E_{\text{FE}}=\epsilon_{\text{DE}}E_{\text{DE}}+\sigma_{\text{FE,init}} \quad (5)$$

$$V_{\text{bias}}=(E_{\text{FE}}+E_{\text{DE}})\,t_{\text{FE}} \quad (6)$$

The stable solutions of the system are shown in Fig. 12(b) (brown curve), for the same DE capacitor settings as in Fig. 11 (see same slope of load line). The energy of the total system at a given V_{bias} is minimized by storing more energy in the DE capacitor while increasing the energy of the FE capacitor. The contour plot, which shows the Gibbs free energy per unit volume of the system in Fig. 12(a), supports the stability of the brown curve: the load line drawn, corresponding to V_{bias} = 0 V, crosses the brown curve at an energy minimum, while it crosses the green curve, representing the initial configuration when connecting the FE and DE capacitor (both biased at 0 V), at a higher energy and therefore the green curve does not represent the stable steady-state solution. Note that for $\sigma_{FE,init}$ = $-P_{FE,r}$, the stable solution would be the green curve shifted to the left with $P_{FE,r}/(\epsilon_o+\epsilon_{DE})$.

The findings of Fig. 12 are also valid for a device consisting of a bottom electrode, pure paraelectric layer, FE layer, top electrode (the same as in Fig. 12(a) but without the central metal electrodes), as long as the assumption of a single-domain FE is enforced. The initial charge will then correspond to e.g. trapped charge.

The data in Fig. 9 have shown that the apparent V_c (the maximum V_{FE} reached) when the FE is connected to the TFET is larger than the V_c value reached during the σ_{FE}-V_{FE} measurement on the FE capacitor only. Fig. 12(b) illustrates that this would be expected if (1) the FE behaves like a uniform defect-free single-domain material with coherent changes in polarization over the entire domain, (2) the dielectric constant of the DE capacitor (or equivalent capacitor of the attached component) is small enough, such that the DE load line doesn't have multiple crossing with the original (σ_{FE}, E_{FE}) curve (green curve in Fig. 12(b)), and (3) there is an initial positive charge on the FE. The cycling of the PZT has been stopped at negative V_{FE}, implying a negative initial surface charge density. However, not only the larger maximum V_{FE}, but also the negative V_{int} for a positive V_{FE} and small V_{gs} (see e.g. Fig. 6(a)) are suggestive for a positive initial surface charge density. This could result from differences in ground between different setups or from leakage currents over a long time.

B. Impact of squareness σ_{FE}-V_{FE} on transient polarization

A standalone FE capacitor is considered for this illustration. Fig. 13(a) shows the (σ_{FE}, E_{FE}) curve of Fig. 11(b). The curve has stable and unstable regions, as the FE is not connected to an external capacitor. Fig. 13(b) shows flatter sections between $-E_{FE,c}$ and $+E_{FE,c}$ (more square-like (σ_{FE}, E_{FE}) curve) for the same $P_{FE,r}$ and $E_{FE,c}$ values as in Fig. 13(a). Note that higher order values (up to P^{12}) are needed in the Gibbs free energy description to produce the latter curve.

The extreme flatness of the curves in Fig. 8(d) up to V_{gs} $\approx$ 1.3 V, suggests that the transient polarization will look more like Fig. 13(b) than like Fig. 13(a). This is indeed observed in Fig. 9, where the initial V_{FE} decrease in the forward

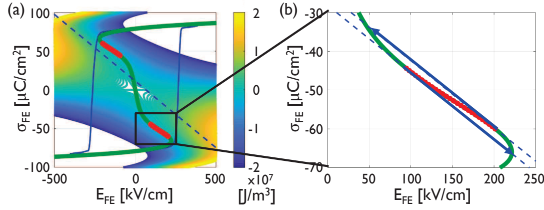

Fig. 14. (a) Solutions (σ_{FE}, E_{FE}) (solid green for stable solutions, solid red for unstable solutions) of the setup of Fig. 11(a) but now with a larger value of C_{DE} than in Fig. 11(b). The parameters of the FE are matched to the experimental data, which are again plotted for reference. The dashed blue curve represents the load line of the DE capacitor. The underlying contour plot shows the energy for every (σ_{FE},E_{FE}) combination. (b) Zoom-in on the unstable section of the (σ_{FE}, E_{FE}) curve, which results in hysteresis as indicated with the blue arrows: up-left pointing arrow corresponding to the forward loop, down-right pointing arrow corresponding to the backward loop.

sweep occurs with very limited polarization increase. Note that this transient polarization behavior has also been predicted assuming domain wall formation in small structures [16].

C. Impact of squareness σ_{FE}-V_{FE} on hysteresis

The (σ_{FE}, E_{FE}) curve of Fig. 2(a) is rather flat. To get a good match with a Landau model, higher order values (up to P^8 for Fig. 11(b)) are needed in the Gibbs free energy description. As a result, the transient curve is a bit more complex than a smooth S-shape. This further implies that small hysteresis loops are feasible, as will be illustrated now. Fig. 14(a) is the same as Fig. 11(b), except that the dielectric constant of the external capacitor is larger, such that the load line crosses the transient part of the (σ_{FE}, E_{FE}) curve at a steeper angle. As can be seen in Fig. 14(b), the load line crosses the initial (final) part of the transient section at such a steep angle, that unstable sections appear in the transient curve, and hence hysteresis occurs. The hysteresis covers a much smaller voltage range than the hysteresis in the σ_{FE}-V_{FE} loop of the FE capacitor only (Fig. 2(a)). The corresponding polarization change is also limited and doesn't correspond to a full polarization switch, rather to a decrease in polarization. As a result, the electric field does not need to go to near - $E_{FE,c}$ to close the hysteresis loop, which is expected when the polarization switches completely. The data presented in Fig. 8(d), and a zoomed-in version shown in Fig. 9, are in qualitative agreement with Fig. 14: hysteresis is seen, while the electric field remains close to $+E_{FE,c}$.

VII. Conclusion

We have detailed the transient polarization of an SS-FeTFET, whereby the embedded TFET behaves exactly as the standalone TFET, making the analysis of the overall device behavior less prone to error. By combining experimental voltage data with simulated surface charge values for the TFET, the FE polarization during the voltage sweeps is made quantitative. We show that the transient polarization change is smaller right beyond the coercive voltage if the P-V loops of the FE are more square-like. We illustrate how FE hysteresis loops which occur at positive (negative) coercive voltage only can be understood from the squareness of the FE P-V loop. Finally, the initial surface charge upon connecting the FE to the FET, determines the apparent coercive voltage of the FE in the SS-FEFET: we show that it can be higher or lower than in the standalone FE.

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