Near Hysteresis-Free Negative Capacitance InGaAs Tunnel FETs with Enhanced Digital and Analog Figures of Merit below V_{DD}=400mV

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Abstract*—** We report the universal boosting impact of a true negative capacitance (NC) effect on digital and analog performances of Tunnel FETs (TFETs), mirrored for the first time in near hysteresis-free experiments and exploiting the S-shaped polarization characteristics. Well behaved InGaAs TFETs with a minimum swing of 55 mV/dec at room temperature are combined with high-quality single crystalline PZT capacitors, placed in series with the gate. When fully satisfying the exact NC matching conditions by a single crystalline ferroelectric that can perform a mono-domain state, ***a hysteresis-free (sub-10 mV over 4 decades of current) NC-TFET with a sub-thermionic swing and an SS_{min} of 40 mV/dec is demonstrated. In other devices, improvement in the subthreshold swing, down to 30 mV/dec, and analog current efficiency factor, up to 180 V^{-1}, are achieved in NC-TFETs with a hysteresis as small as 30 mV. Importantly, the I_{60} FoM of the TFET is improved up to 2 orders of magnitude. The supply voltage is thereby reduced by 50%, down to 300 mV, providing the same drive current. Our results show that NC can open a new direction as a ***universal performance booster*** in the FET design by significantly improving the low I_{60} and low overdrive of TFETs.

I. Introduction

Energy-efficient logic devices are required for the enablement of the Internet of Things (IoT) platform. However, the Boltzmann electron energy distribution imposes a fundamental limit to lowering the power dissipation of conventional MOS devices: a minimum increase of the gate voltage, i.e. 60 mV at room temperature, is required to have a 10-fold increase in the current. Among alternative structures, Tunnel Field-Effect Transistors (TFETs) [1] and Negative Capacitance (NC) MOSFETs [2] have attracted a great deal of attention for achieving a sub-60 mV/dec subthreshold swing (SS). TFETs go sub-60 mV/dec by using quantum mechanical band-to-band tunneling (BTBT), rather than thermionic injection, to inject charge carriers into the channel. Meanwhile, the NC of ferroelectric materials is proposed as an important way to bypass the noted fundamental limit. Ferroelectrics are traditionally modeled with a double well energy function (Fig. 1). In equilibrium, the ferroelectric resides in one of the wells and gives rise to a positive capacitance ($C_{FE}^{-1} = d^2U_{FE}/dQ_{FE}^2$). Nevertheless, it shows an effective NC while switching from one stable polarization state to the other one [3]. It has been proposed that the concept of NC when integrated into the gate stack of TFETs, would be highly beneficial for energy band bending due to the internal voltage amplification, enhancing the BTBT probability. Previous works have mainly focused on the theoretical investigation of NC-TFETs and there are few experimental demonstrations, showing a limited performance [4].

A major drawback of most reported NC devices is that they show large hysteresis, as little effort was dedicated to the analytical design to correctly fulfill the conditions of negative capacitance, which in theory should provide hysteresis-free characteristics. Many of the reported hysteretic and claimed NC devices are, in fact, exploiting a ferroelectric polarization switching and do not meet the initial NC theory of Salahuddin [2], later refined by our group [5]. The important value of the NC effect, with a proper design and matched conditions, is that it can act *as a universal swing and on-current booster for any Field-Effect Device*.

In this report, we have combined the tunneling of carriers as the operation principle with a NC gate and experimentally demonstrated NC-TFETs. InGaAs ring TFETs are investigated as the baseline transistors with a sub-thermionic swing down to 55 mV/dec at RT. Single crystalline PZT capacitors with the ability to form a mono-domain state are employed as the NC booster. Firstly, a NC-TFET with a hysteresis as small as 30 mV shows a significant performance boosting in NC operation conditions. An improved SS down to 30 mV/dec together with an enhanced current efficiency factor, g_m/I_d, up to 180 V^{-1} highlights the important point that the NC effect simultaneously enhances both digital and analog performances of TFETs. In a fully matched design of capacitances, a hysteresis-free NC-TFET with a sub-60 mV/dec swing down to 40 mV/dec, an enhanced g_m/I_d factor with a maximum value of 120 V^{-1}, and an improved I_{60} by nearly 2 orders of magnitude, is achieved.

II. Experimental

The experimental configuration of the NC-TFET of this work is depicted in Fig. 2a where a ferroelectric capacitor is externally connected to the gate of a TFET. To ensure a sufficient enhancement together with a non-hysteretic characteristic, the negative value of the ferroelectric NC (C_{FE}) should be close to the gate intrinsic capacitance of the baseline TFET (C_{MOS}) while the total capacitance of the structure should remain positive in the whole range of operation [4, 6].

For this experiment, 46 nm of high-quality epitaxial $Pb(Zr,Ti)O_3$ (PZT) was grown by pulsed laser deposition on a (110) $DyScO_3$ (DSO) substrate. A 20 nm $SrRuO_3$ (SRO) layer was grown between the substrate and PZT film to serve as the bottom electrode. A 50 nm Pt layer is sputtered and patterned using shadow masking technique. Fig. 3a depicts the schematic of the PZT capacitor (top) along with the crystal structure of PZT in its two stable polarization states (bottom). Reflection high-energy electron diffraction (RHEED) (Fig. 3b) and XRD (Fig. 3c) analysis of the deposited layer confirm the crystallinity as well as the coherency of the epitaxial interface, without any grain boundaries or other extended defects. The polarization hysteresis loop measured at 100 Hz shows a remanent polarization of 80 μC/cm^2 and coercive voltages of ±1.2 V (Fig. 3d). The surface of the PZT layer is conformal and the polarization in all c-domains is oriented from bottom to top interface as confirmed by piezoelectric force microscopy (Fig. 3e).

InGaAs homojunction TFETs with 53% In content and a sub-60 mV/dec swing are used as the baseline devices [7]. The fabrication process starts with the Metal Organic Chemical Vapor Deposition (MOCVD) growth of the III-V stack on an InP substrate. The stack consists of a 10 nm InP seed layer, a 90 nm thick doped $In_{0.53}Ga_{0.47}As$ layer as the channel material, 3 nm of InP etch stop layer, and a 50 nm $n+$ $In_{0.53}Ga_{0.47}As$ drain layer. A SiO_2 layer is then deposited as the hard mask and the drain is defined through wet etching (Fig. 4a). The gate stack is deposited next with ALD and consists of a bilayer

Al_2O_3 (1 nm) and HfO_2 (2 nm) (Fig. 4b). The EOT for the gate stack is about 0.8 nm. A 100 nm TiN layer is then deposited as the gate metal and is etched to define the source, which is doped via Zn diffusion. The room temperature transfer characteristic and the gate current on the same plot are depicted in Fig. 4c. The TFET achieves a sub-thermionic swing, down to 55 mV/dec, for all drain voltages.

III. Results and Discussions

A. *Sub-30 mV Hysteretic Negative Capacitance TFET*

In this section, we report a hysteretic NC-TFET where the gate stack of the reference TFET (L_g = 6 µm and W_g = 4×94 µm) is loaded with a PZT capacitor with an estimated area of 15×15 µm^2. The V_g is swept from -1 V to 2 V and back to the starting point while the drain voltage is set to 200 mV. In order to decouple the effect of the threshold voltage (V_{TH}) variation, curves are plotted with respect to the effective gate voltage: $V_{gs\_eff} = V_{gs} - V_{TH}$. Fig. 5a illustrates the I_d-V_g plot of the NC-TFET compared to the baseline device. The NC of the ferroelectric is partially stabilized, as is schematically explained in Fig. 1, leading to a small hysteresis (ΔV_{TH}) of 30 mV, while V_{TH} is extracted at $I_d = 10^{-3}$ µA/µm (the positive going branch is considered for the NC-TFET). The small hysteresis of 30 mV suggests that this condition is not fulfilled only in a limited region [4]. The subthreshold swing is significantly lowered, down to 30 mV/dec, and a sub-60 mV/dec swing over about 3 decades of current is obtained (Fig. 5b).

The I_{60} FoM, which is the maximum current below which the TFET still has a sub-60 mV/dec swing, is improved by more than one decade. Fig. 5c demonstrates that the transconductance (g_m) also has a steeper transition and its maximum value is improved by a factor of 10. The extracted g_m/I_d factor, an analog FoM, is remarkably improved and reaches a maximum value of 180 V^{-1} (Fig. 5d). To quantitatively determine the voltage amplification of the NC, the internal node is measured and the dV_{int}/dV_g curve, defined as the internal gain of NC, is plotted in Fig. 5e. A voltage amplification up to 2 with an average of 1.5 is observed over 40% of the operation range. This internal amplification allows the surface potential to change faster than the gate voltage, leading to an enhanced tunneling probability and reduced subthreshold swing. Due to the voltage amplification, the NC-TFET can demonstrate the same output current at a supply voltage of 0.3 V, which is 50% lower than the one of the reference TFET. The existence of NC effect is confirmed by extracting the P-V characteristic of the PZT capacitor during the NC-TFET operation, which displays a clear S-shape (Fig. 5f). Fig. 5g and 5h summarize the impact of the source-to-drain electric field on the electric performance of the same NC-TFET. The drain voltage is varied from 200 mV to 400 mV while the source contact is grounded. Besides the common impact of V_d on the increase of *on*-current, it does not severely affect the electrical properties of the NC-TFET. Generally, the variation of V_d changes the operation point of the transistor, the intersection of the TFET charge line and the negative slope of the polarization, which is expected to affect the NC-TFET electrical properties [8]. However, opposite to polycrystalline ferroelectrics, the employed single crystalline PZT capacitor provides a uniform NC over a wide range of applied gate voltages. Therefore, the variation of the operation point does not change the value of the ferroelectrics NC which leads to similar subthreshold swing and voltage gain for different drain voltages.

B. *Hyteresis-Free (sub-10 mV) Negative Capacitance TFET*

In a different structure, the gate stack of the InGaAs planar TFET is loaded with a PZT capacitor, having the same thickness with a smaller area of 10×10 µm^2, close to the ideal NC matching conditions, supposing a negligible effect of interface trap capacitance [9]. Thereby, a hysteresis-free transfer characteristic of the NC-TFET, around 5 mV at $I_d = 10^{-2}$ µA/µm, is achieved (Fig. 6a). A sub-10 mV hysteresis over the whole range of operation is evidenced (Fig. 6b). A single crystalline ferroelectric that can exhibit a mono-domain state is essential to fulfill the matching conditions. The gate voltage was swept from -1 V to 2 V and back to -1 V at the drain voltage of 400 mV. The gate leakage is negligible compared to I_d and is not impacting the reported effects.

Fig. 6c compares the I_d-V_g curves of the NC-TFET and its baseline transistor, showing a remarkable improvement in the steepness of the *off*-to-*on* transition, which allows to reduce the supply voltage by 50%. Fig. 6d depicts the SS, showing a sub-60 mV/dec swing down to 40 mV/dec. The I_{60} parameter is improved by 2 orders of magnitude and reaches a value of 10 nA/µm. The transconductance of the NC-TFET exhibits an improvement in the overdrive region, up to 6 times of its original value (Fig. 6e). The internal node measurement confirms the non-hysteretic operation of PZT as the step-up voltage transformer (Fig. 6f). The internal gain, dV_{int}/dV_g, demonstrates an effective gain higher than 1 over 50% of the NC-TFET operation range (Fig. 6g). The polarization characteristic of the PZT capacitor is extracted (Fig. 6h), showing an effective NC over a wide range of operation.

Overall, NC effect can be employed as an effective universal performance booster of FETs, significantly improving the SS and overdrive. By properly satisfying the matching condition, a hysteresis-free NC-TFET, suitable for logic applications, can be achieved. A well-designed negative capacitor integrated to the gate stack of a TFET significantly increases both I_{60} and the drive current, which are the main challenges involved in the fabrication of TFETs (see Table 1). Extrapolating the improvements to state-of-the-art TFETs [10], the NC effect brings a MOSFET competitive I_{60} = 10 µA/µm within reach. The novelty and universality of this approach relate to the fact that the gate stack is not anymore a passive part of a field-effect transistor and contributes to the signal amplification. Therefore, a NC booster can be applied in parallel with other conventional performance boosters of TFETs.

IV. Conclusion

Near hysteresis-free NC-TFETs with a sub-thermionic swing over about 4 decades of current and a minimum of 30-40 mV/dec are experimentally demonstrated by fulfilling the NC matching conditions. The supply voltage can be reduced by 50%, down to 0.3-0.4 V, as a result of the overdrive improvement by NC. The NC effect also enhances the analog FoM of TFETs, in addition to digital performances, showing a new path to advance the performance engineering of TFETs for improved efficiency.

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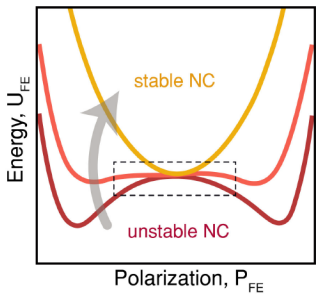

Fig. 1. Energy density of a ferroelectric. NC is unstable by itself, but it can be partially or fully stabilized if it is placed in series with a positive capacitor of proper value.

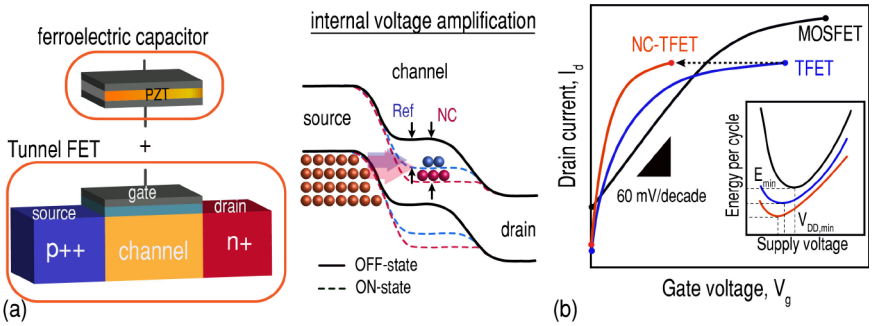

Fig. 2. (a) Schematic of an NC-TFET (left) where a ferroelectric capacitor is connected to the gate of a conventional TFET. This series connected NC booster amplifies the gate voltage and increases the tunneling probability (right). (b) I_d-V_g plot and energy efficiency of a MOSFET, a TFET, and a NC-TFET.

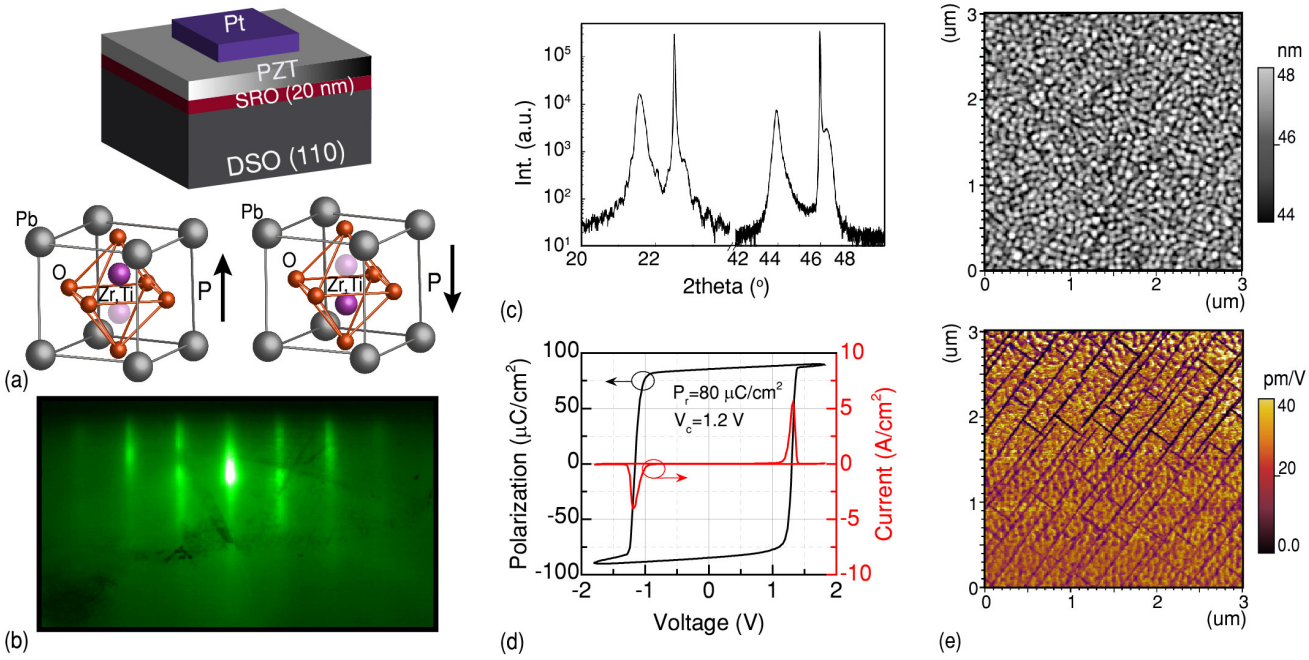

Fig. 3. (a) Schematic of a PZT capacitor (top) and the two stable polarization states of PZT, which occur due to ionic movement (bottom). 46nm of PZT was grown on a (110) $DyScO_3$ (DSO) substrate. RHEED (b) and XRD (c) analysis of the surface of the deposited PZT confirm the crystallinity of the layer as well as the coherency of the epitaxial interface. (d) The P-V and I-V curves of the PZT capacitor show a sharp and coherent switching. (e) The AFM measurement demonstrates a smooth surface (top) and the piezo-force microscopy confirms that the polarization in all c-domains of PZT are oriented from bottom to top interface (bottom).

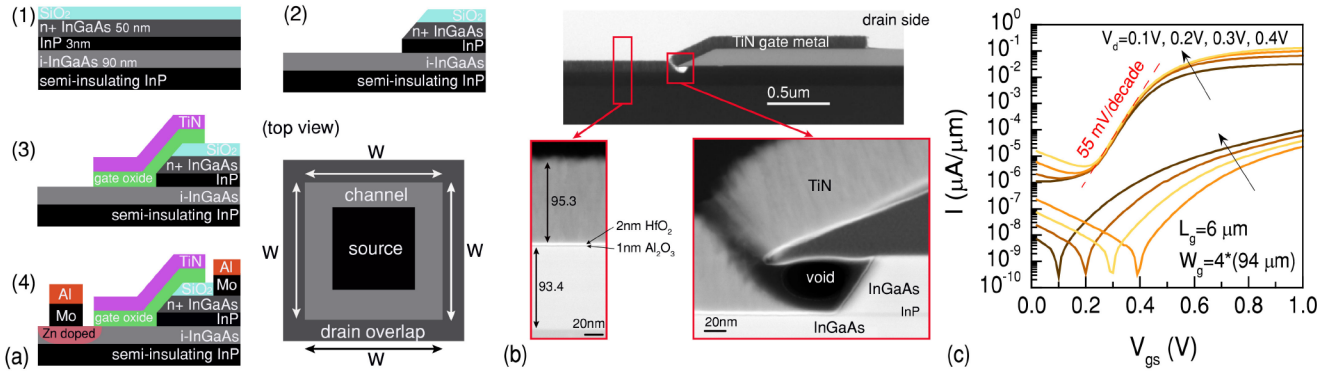

Fig. 4. (a) Process flow and the cross section schematic of the baseline TFET: 1) MOCVD growth and SiO_2 deposition. 2) Drain isolation etch. 3) gate stack (1 nm Al_2O_3 + 2 nm HfO_2) ALD deposition and patterning. 4) Zn diffusion from the gas phase @ 500 °C for 60 s and source/drain contacts with lift-off process. Finally, devices are annealed in forming gas at 400 °C for 15 minutes. (b) TEM image of the cross-section of the TFET, showing a clean surface along the channel and source and a void at the drain to avoid ambipolar current. (c) I_d-V_g and I_g-V_g plots of a TFET with a gate length of 6 μm for different drain voltages, showing a sub-thermionic swing down to 55 mV/decade at 300 °K.

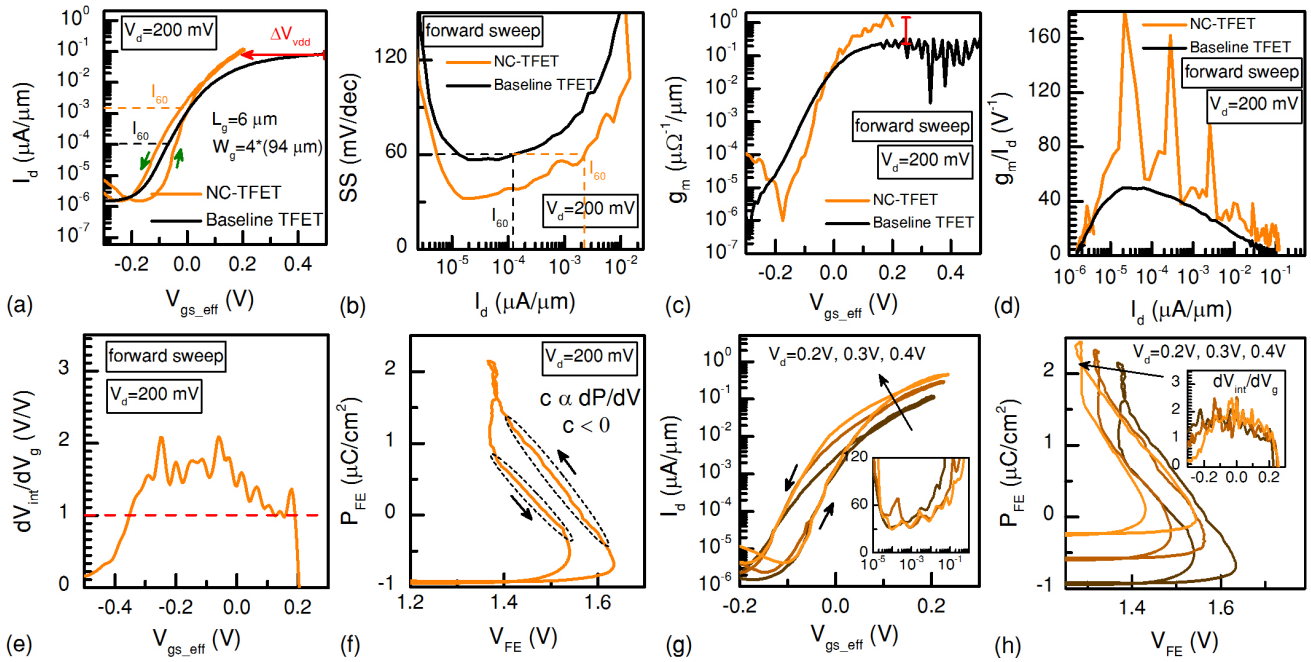

Fig. 5. **Small-hysteresis NC-TFET.** (a) I_d-V_g curve of the NC-TFET compared the base TFET (V_d=200 mV). (b) The SS is significantly reduced, down to 30 mV/dec. (c) g_m is enhanced, up to 10 times of its original value. (d) g_m/I_d is also improved, having a peak of 180 V^{-1}. (e) A voltage gain, dV_{int}/dV_g >1, over about 50% of the device operation range is observed. The extracted S-shaped P-V of the PZT capacitor confirms the existence of an effective NC (f). The variation of V_d on the NC effect shows no major impact on the I_d-V_g (g) and P-V (h) curves of the NC-TFET, confirming a sub-60 mV/dec swing over almost 4 decades of current.

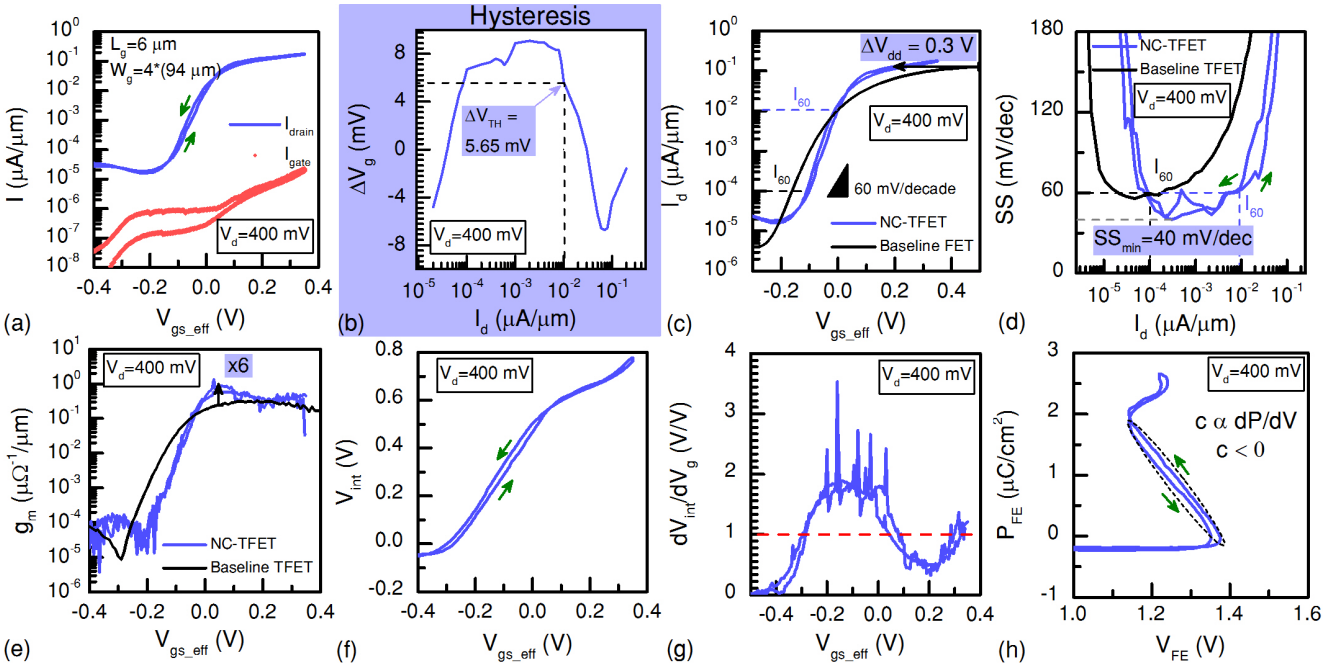

Fig. 6. **Hysteresis-free NC-TFET.** (a) I_d-V_g and I_g-Vg curves of the NC-TFET at a drain voltage of 400 mV, showing a sub-10 mV hysteresis over the whole range of operation (b). Transfer characteristic of the NC-TFET is compared with the base device (c), confirming a significant improvement in the swing (d). Transconductance is also improved (e). The voltage of the internal node is measured (f) and a clear voltage gain over 50% of the operation range is observed (g). The extracted P-V plot confirms the existence of an effective NC with a negligible hysteresis (h).

Table 1. Boosting of digital and analog performances of the hysteresis-free NC-TFET compared the baseline TFET at V_d = 400mV.

	SS_{min}	sub-60mV/dec range	Hysteresis, ΔV_g (10^{-5}-10^{-1} μA/μm)	V_{dd} (I_{on}=0.1 μA/μm)	I_{60}	$(g_m)_{max}$	$(g_m/I_d)_{max}$
TFET	55 mV/dec	10^{-5}-10^{-4} μA/μm	-	0.6 V	0.1 nA/μm	0.18 μΩ^{-1}/μm	50 V^{-1}
NC-TFET	40 mV/dec	8×10^{-5}-10^{-2} μA/μm	±10 mV	0.3 V (1/2)x	10 nA/μm 100x	1.0 μΩ^{-1}/μm 6x	120 V^{-1} > 2x