Double gate n-type WSe_2 FETs with high-k top gate dielectric and enhanced electrostatic control.

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***Abstract*—We propose and experimentally demonstrate double-gated n-type WSe_2 FETs with excellent top gate high-k dielectric layer. Under back gate control, the devices behave as n-type enhancement transistors, with ON/OFF current ratios larger than 6 orders of magnitude and a ON current close to 1 µA/µm under a drain bias of 100 mV. Negative top gate biases determine a much steeper turn-on of the back gated transfer characteristic and a reduction of the hysteresis. Top gated device behaves as n-type depletion FETs, exhibiting a I_{ON}/I_{OFF} ratio larger than 10^6 under positive bias applied to the back gate. A minimum hysteresis of 40 mV and an average subthreshold slope close to 100 mV/dec prove the high quality of the deposited top gate dielectric. The electron mobility has been extracted using the Y-function method, obtaining 22.15 $cm^2V^{-1}s^{-1}$ under a drain bias of 1 mV.**

Keywords*—WSe_2, double-gated FETs, 2D materials, field-effect devices, atomic layer deposition.

I. Introduction

Two-dimensional (2D) materials have attracted a huge research interest in recent years due to the unique electrical properties and the possibility of isolating atomically thin flakes. The transition metal dichalcogenide (TMDCs) family of material exhibit large band gaps, enabling the realization of field-effect devices with excellent ON/OFF current ratios [1, 2]. WSe_2 in particular shows ambipolar conduction, with demonstrated high hole and electron mobilities [2-4]. This feature combined with the possibility of controlling the device polarity by either the choice of the metal contacts workfunction or electrostatic doping make this material promising for the realization of a complementary 2D technology [4, 5].

Typically, 2D FETs are realized by relying on a back gate architecture [2-6]. The realization of high performance top gated devices has been prevented by the challenges related to dielectric deposition on 2D materials. Good results in terms of degradation prevention and field-effect mobility have been obtained capping WSe_2 with hBN flakes [6, 7], but because of this material low-k and the complexity introduced by the deterministic assembly of 2D/2D heterojunctions this solution is unpractical for the production of high performance, standardized devices. The direct deposition of high-k dielectrics on 2D materials results in either discontinuous, leaky films or a large density of interfacial traps determining huge hysteresis windows [8]. Here, we report the realization of high performance double gated n-type WSe_2 FETs with excellent top gate subthreshold slope (*SS*) and reduced hysteresis. The gate dielectric is obtained by stacking a thin Al_2O_3 seed layer, resulting from the oxidation of 1.5 nm of evaporated Al [9], and a 5 nm thick HfO_2 film deposited by atomic layer deposition (ALD).

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II. Device Fabrication

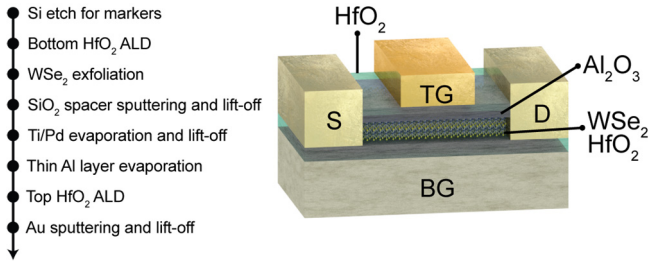

Fig. 1. Schematic view of the realized double gate devices and summary of the proposed process flow.

The proposed device consists of an asymmetrical double-gated WSe_2 FET, with a common bottom gate and a top gate covering only the central part of the semiconducting channel. A schematic of the complete device is shown in Fig. 1, together with the summary of the proposed process flow. The starting substrate consists of a low resistivity p-doped Silicon wafer. ALD in a BENEQ TFS 200 reactor at 200 °C, using TEMAH and H_2O as precursors was performed to deposit the 10 nm thick HfO_2 layer that serves as bottom gate dielectric. Next, WSe_2 flakes were mechanically exfoliated from a bulk crystal sample (synthetized by *hq graphene*) using the scotch taping technique. Thin flakes were then identified by inspecting the sample with an optical microscope.

In order to reduce the back gate leakage current in the final device, a 50 nm thick SiO_2 film was deposited by sputtering and lift-off around the flakes to increase the dielectric thickness between the contact pads and the Si substrate. The source and drain contacts were deposited on the flakes with an electron-beam lithography (EBL) step performed on a PMMA/MMA bilayer resist followed by evaporation and lift-off of a Ti (1.5 nm)/Pd (100 nm) stack. Devices were then completed with a top gate dielectric and metal. In order to improve the quality of the dielectric, we deposited a seed layer consisting of 1.5 nm of evaporated Al prior to the ALD step. The Al layer was then oxidized in air to obtain a thin Al_2O_3 film on which 5 nm of HfO_2 were deposited using the same reactor and recipe exploited for the bottom gate. Finally, the top gate metal was deposited by sputtering and lift-off of a Ni (80 nm)/Au (40 nm) stack after a last EBL. A colorized SEM image of the complete device is shown in Fig. 2a. The WSe_2 flakes thickness was measured using atomic force microscopy (AFM) in contact mode, as shown in Fig. 2b. The results reported in the following have been obtained from devices realized with 3.2 nm thick flakes.

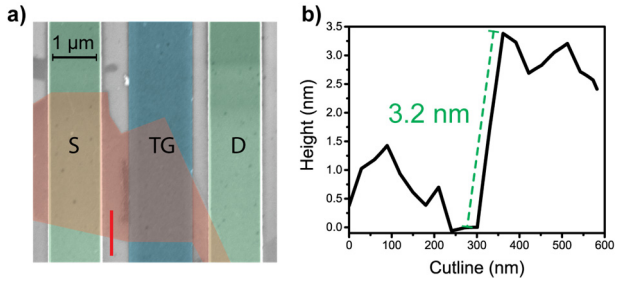

Fig. 2. a) False colored SEM image of a device after the deposition of the top gate contact. The red line shows the cutline along witch the AFM profile in b) was measured. The estimated thickness of the flake is 3.2 nm.

III. RESULTS

All the electrical measurements were performed at ambient conditions and room temperature using an HP 4156C semiconductor parameter analyzer. We focused our analysis on the electrons conduction in the channel to reduce the gate bias window and consequently the measurements stress on the device. The reported transistor is 2.6 µm long and 2 µm wide.

A. Bottom gated and top gated transfer characteristic

In order to study the impact of the bottom and top gates on the WSe_2 channel conductance we measured the double-sweep transfer characteristics and output characteristics sweeping one of the gates potential while maintaining the second at a fixed bias. The results are reported in Fig. 3. By comparing the two $I_D(V_G)$ curves (Fig. 3a and c) it is clear how the back gated device behaves as an enhancement mode FETs, while when operated under the top gate control the device operates in depletion mode. The drain current of the top gated FET tends to saturate under positive gate bias because of the reduce control of the top gate on the ungated WSe_2 flake areas close to the source and drain contacts (see Fig. 2a). The hysteresis can be evaluated by comparing the threshold voltage of the up and down sweeps. The bottom gated FET exhibits a 272 mV hysteresis while when controlled by the top gate sweep, the device hysteresis is reduced to 70 mV, a value that suggests a good quality of the deposited Al_2O_3/HfO_2 dielectric stack.

The back gate output characteristic in Fig. 3b exhibits current saturation and negative differential resistance is observed at large V_{BG} values, because of self-heating in the WSe_2 flake [7]. The $I_D(V_D)$ curve for the top gate FET is reported in Fig. 3d, and shows how current saturation is achieved for drain biases below 1 V.

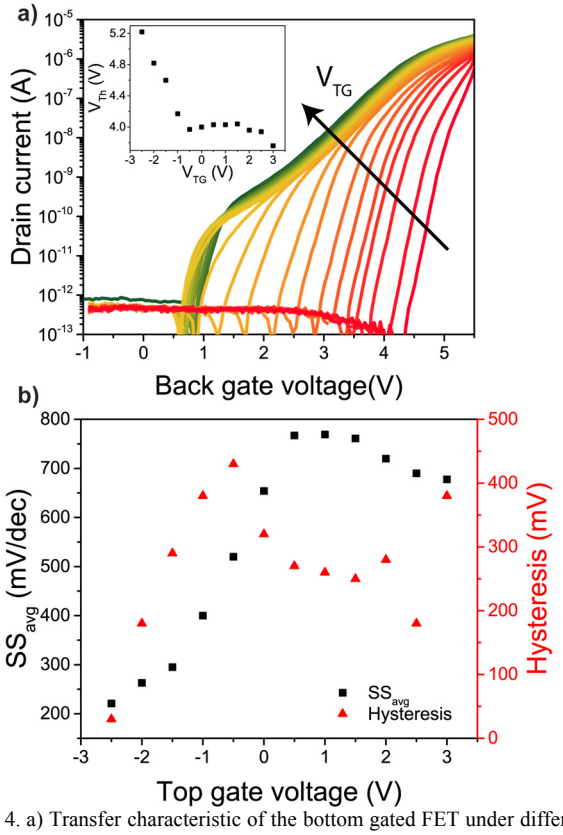

Fig. 4. a) Transfer characteristic of the bottom gated FET under different top gate biases, in the +/- 3 V range. Inset: evolution of the threshold voltage as a function of V_{TG}. b) Negative top gate biases result in a decrease of both the average subthreshold slope and the hysteresis. All the measurements were performed at V_{DS} = 100 mV.

B. Impact of top gate bias on bottom gated FET characteristic

In order to study the impact of the top gate bias on the bottom gated device conduction, we measured the bottom gate transfer characteristic under different top gate voltages (V_{TG}) in the +3 V/-3 V bias window, applying a drain bias of 100 mV. The results are shown in Fig. 3. Sweeping the top gate bias from positive to negative values determines a positive shift of the threshold voltage (inset of Fig. 3a). A positive V_{TG} favors the accumulation of electrons under the top gate. As a result, two channels contribute to the conduction in the flake: the top one constituted by accumulated electrons while the bottom one is an inversion channel controlled by the back gate. The resulting subthreshold current shows two different slopes, corresponding to the onset of these two conduction paths. The bottom gate threshold voltage saturates under positive bias being limited by the potential required to electrostatically dope the flake area not covered by the top gate. Under negative top gate bias, the WSe_2

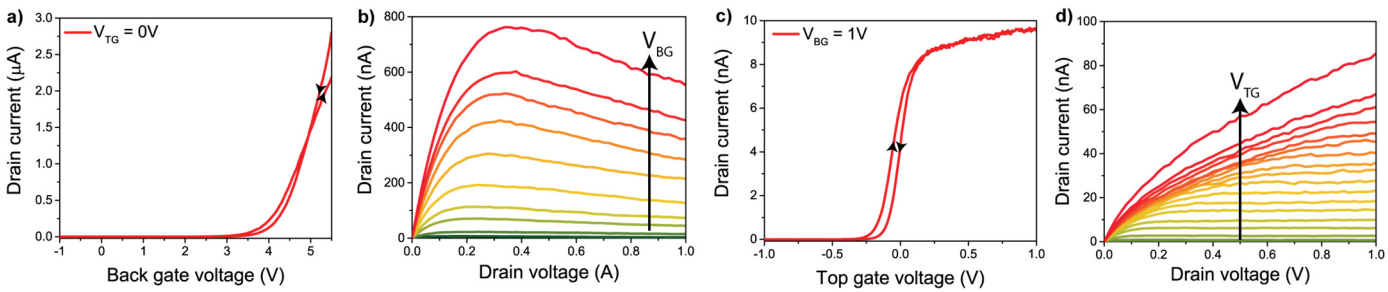

Fig. 3. Double sweep transfer characteristic $I_D(V_G)$ and output characteristic $I_D(V_D)$ of the fabricated WSe_2 FET. a) Double sweep back gate $I_D(V_G)$ curve measured at V_{DS} = 100 mV applying 0 V to the top gate. b) Back gate $I_D(V_D)$ characteristic measured under a top gate bias of -2 V and for back gate bias in the -1/+6 V range. c) Double sweep top gate $I_D(V_G)$ curve measured at V_{DS} = 100 mV applying 1 V to the back gate. b) Top gate $I_D(V_D)$ characteristic measured under a back gate bias of +3 V and for a top gate bias in the -2/+1 V range.

area below the top gate is fully depleted of electrons and only the inversion channel formed by the back gate dictates the conduction in the flake. This mechanisms translates in a unique and steeper subthreshold slope as well as the observed positive shift of the threshold voltage.

The I_{ON}/I_{OFF} ratio remains larger than 6 orders of magnitude for all the top gate bias values, despite a small decrease in I_{ON} observed for negative V_{TG} biases. The OFF state current is limited by the back gate leakage, which remains below 0.5 pA/μm for all the measurements reported thanks to the SiO_2 layer deposited below the source and drain contact pads. Moreover, a clear increase of the steepness of the subthreshold current is observed, as reported in other implementations of double-gated WSe_2 FETs [7]. Fig. 3b summarizes the evolution of both the average subthreshold slope over 5 orders of magnitude of the output current and the bottom gate hysteresis with the applied bias to the top gate.

We report in Fig. 5 the bottom gated transfer characteristic measured at different values of the drain-to-source bias and under V_{TG} = -2V. For drain voltages larger than 100 mV, the I_{ON}/I_{OFF} ratio exceeds 6 orders of magnitude, while the average subthreshold slope does not vary significantly.

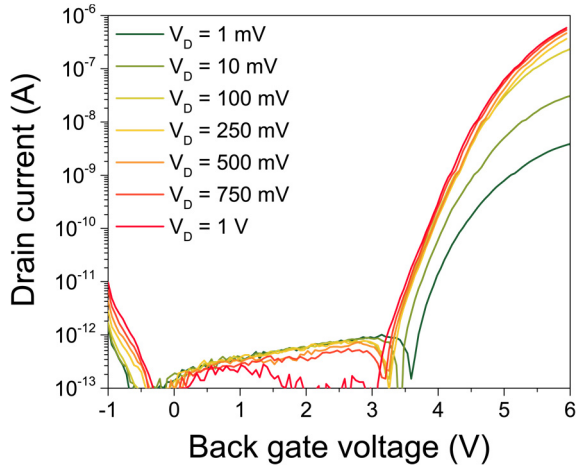

Fig. 5. Transfer characteristic $I_D(V_G)$ of the back gated FET at different V_{DS} biases in semi-log scale, measured with V_{TG} = -2 V. For drain voltages larger than 100 mV, the device exhibits a I_{ON}/I_{OFF} ratio larger than 6 orders of magnitude. The average subthreshold slope does not vary significantly with respect to the drain bias.

C. *Impact of back gate bias on the top gated FET.*

In order to study the impact of the back gate bias on the bottom gated device, we measured the top gate transfer characteristic under different bottom gate voltages (V_{BG}) in the 0V/+3V bias window, applying a drain bias of 100 mV. The results are shown in Fig. 6. The increase of the bottom gate bias determines a negative shift of the top gated FET threshold and a clear increase of the I_{ON}/I_{OFF} ratio. The top gate leakage current remains below 50 fA/μm for all the reported measurements. Positive V_{BG} values determine an n-type electrostatic doping of the entire WSe_2 channel that can be then depleted of electrons in the central section by applying a negative bias to the top gate. The inset of Fig. 6a shows how the threshold voltage decreases linearly with the increase of the back gate bias, with an extracted -0.2 V shift for applied volt to the bottom gate. The evolution of both the average subthreshold slope and the I_{ON}/I_{OFF} ratio is reported in Fig. 6c. For back gate biases larger than 2 V, the ON/OFF current ratio exceeds 6 orders of magnitude, and the top gated FET reaches performance equivalent to the bottom gated device while maintain a steeper turn-on characteristic. The average subthreshold slope over 4 orders of magnitude of the output current reaches values close to 100 mV/dec, and degrades only slightly with the increase of the bottom gate bias.

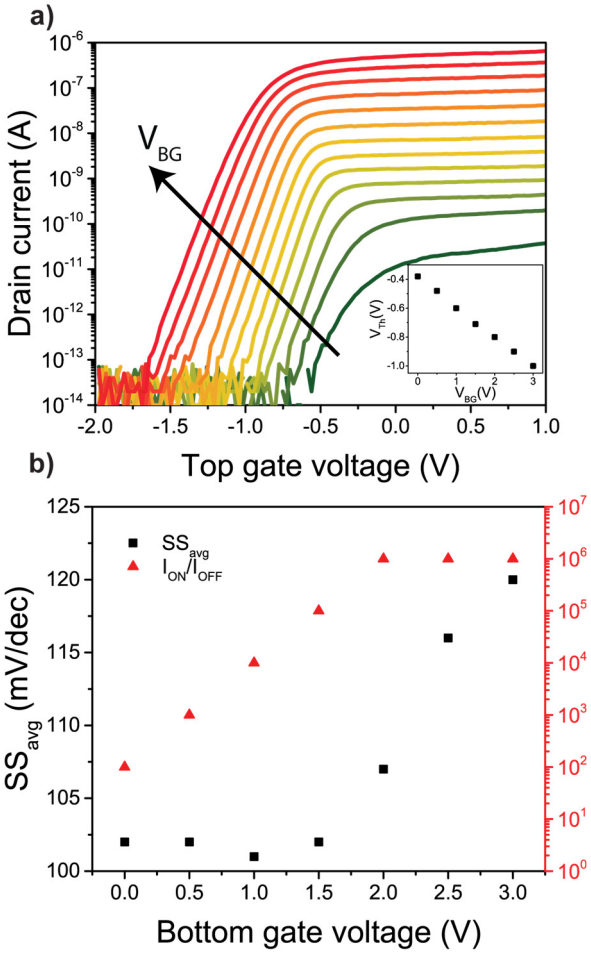

Fig. 6. a) Transfer characteristic of the top gated device under different back gate voltages in the 0/+3V bias range measured at V_{DS} = 100 mV. Inset: threshold voltage as a function of the applied V_{BG}. c) I_{ON}/I_{OFF} ratio and average subthreshold slope over four orders of magnitude as a function of V_{BG}.

In Fig. 7 we show the top gated transfer characteristic measured under increasing values of the drain-to-source bias and applying a 3 V back gate voltage. Similarly to what observed for the back gated characteristic, a drain voltage of 100 mV is sufficient to obtain an ON/OFF current ratio larger than 10^6. Remarkably, the average subthreshold slope is not affected by the increase of V_{DS}.

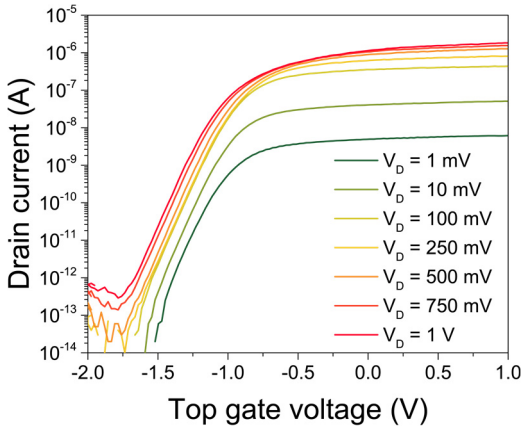

Fig. 7. Transfer characteristic $I_D(V_G)$ of the top gated FET at different drain-to-source biases in semi-log scale, measured at V_{BG} = 3V. For drain voltages larger than 100 mV, the device exhibits a I_{ON}/I_{OFF} ratio larger than 6 orders of magnitude.

D. Field effect mobility extraction.

We extracted the two-terminal effective field effect mobility, μ_{FE}, using $\mu_{FE} = g_m L/WC_{ox}V_{DS}$, where g_m is the transconductance extracted from the linear part of the top gated $I_D(V_G)$ curve, W is the channel width and C_{ox} is the top gate capacitance per unit area, that has been directly measured by characterizing MIM structures included on the same wafer of the devices. The obtained electron mobility at V_{DS} = 1 mV and V_{BG} = 3 V is 10.74 $cm^2V^{-1}s^{-1}$.

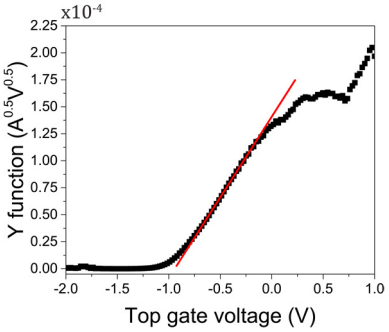

Fig. 8. Extracted Y function vs top gate voltage for the top gated FET at V_{DS}= 1 mV and V_{BG}= 3 V. The mobility can be extracted from the fitting of the linear part of the curve, shown in red in the figure.

In order to obtain a more accurate estimation of the carriers' mobility by decoupling part of the impact of the contact resistance, we applied the so-called (Ghibaudo) Y function method [10, 11]. Assuming that the contact resistance is not dependent on the gate bias, the Y function expression reduces to:

$$Y = \frac{I_D}{\sqrt{g_m}} = \sqrt{\frac{\mu C_{ox}|V_{DS}|W}{L}}(V_G - V_T) \qquad (1)$$

where V_T is the threshold voltage.

Fig. 8 shows the extracted Y function for the reported top-gated FET, obtained with V_{DS} = 1 mV and V_{BG} = 3 V. From the fitting of the linear region, in red in the figure, it is possible to extract the low field electron mobility, estimated to be 22.15 $cm^2V^{-1}s^{-1}$, in line with the two-terminals mobility reported in other works on WSe_2 FETs [3-6].

IV. CONCLUSION

In summary, we have demonstrated double gate n-type WSe_2 FETs with excellent high-k top gate dielectric obtained combining an evaporated and oxidized thin Al_2O_3 seed layer and the ALD of a 5 nm thick HfO_2 film. The resulting device can be controlled by either the top or the bottom gate, using the opposite gate to finely tune the FET performance. When back gated, the device behaves as an enhancement FET, whose hysteresis and subthreshold slope can be greatly improved by applying a negative voltage to the top gate. An average subthreshold slope close to 200 mV/dec and a hysteresis below 100 mV have been achieved. Conversely, the top gated transistor works in depletion, and the back gate bias can be exploited to enhance the ON/OFF current ratio and shift the threshold voltage. As a result, the device exhibits an I_{ON}/I_{OFF} ratio larger than 10^6 and an average subthreshold slope approaching 100 mV/dec, which is independent from the drain bias. Both the top and the bottom gate are characterized by a leakage current below 0.5 pA/μm in all the reported electrical measurements.

We believe that the proposed approach for the deposition of high-k dielectrics on WSe_2 provides a promising path for the development of high performance top-gated FETs. Given the small leakage current measured, the dielectric stack could be subject to a further scaling of the HfO_2 layer thickness while seed layers with better dielectric performance than Al_2O_3 could contribute to an enhanced top gate control. An improvement of the drive current and ON/OFF current ratio requires the reduction of the contact resistance, achievable by an annealing of the contacts prior to the deposition of the top gate dielectric.

REFERENCES

[1] G. Fiori, et al., "Electronics based on two-dimensional materials," *Nat. Nanotechnol.*, vol. 9, no. 10, pp. 768–779, 2014.

[2] S. Das, et al., "Toward low-power electronics: Tunneling phenomena in transition metal dichalcogenides," *ACS Nano*, vol. 8, no. 2, pp. 1681–1689, 2014.

[3] W. Liu, et al., "Role of metal contacts in designing high-performance monolayer n-type WSe2 field effect transistors," *Nano Lett.*, vol. 13, no. 5, pp. 1983–1990, 2013.

[4] A. Allain and A. Kis, "Electron and hole mobilities in single-layer WSe2," *ACS Nano*, vol. 8, no. 7, pp. 7180–7185, 2014.

[5] G. V Resta, et al., "Polarity control in WSe2 double-gate transistors," *Sci. Rep.*, vol. 6, no. July, p. 6, 2016.

[6] D. J. Groenendijk, et al., "Photovoltaic and photothermoelectric effect in a double-gated WSe2 device," *Nano Lett.*, vol. 14, no. 10, pp. 5846–5852, 2014.

[7] H. C. P. Movva, et al., "High-Mobility Holes in Dual-Gated WSe2 Field-Effect Transistors," *ACS Nano*, vol. 9, no. 10, pp. 10402–10410, 2015.

[8] S. McDonnell, et al., "HfO2 on MoS2 by atomic layer deposition: Adsorption mechanisms and thickness scalability," *ACS Nano*, vol. 7, no. 11, pp. 10354–10361, 2013.

[9] S. Kim, et al., "Realization of a high mobility dual-gated graphene field-effect transistor with Al2O3 dielectric," *Appl. Phys. Lett.*, vol. 94, no. 6, p. 62107, 2009.

[10] H. Y. Chang, W. Zhu, and D. Akinwande, "On the mobility and contact resistance evaluation for transistors based on MoS2 or two-dimensional semiconducting atomic crystals," *Appl. Phys. Lett.*, vol. 104, no. 11, 2014.

[11] N. Oliva, E. A. Casu, W. A. Vitale, I. Stolichnov, and A. M. Ionescu, "Complementary black phosphorous FETs by workfunction engineering of pre-patterned Au and Ag embedded electrodes," *Eur. Solid-State Device Res. Conf.*, pp. 102–105, 2017