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Hysteresis Dynamics in Double-Gated n-Type WSe_2 FETs With High-k Top Gate Dielectric

NICOLÒ OLIVA [1], YURY YU ILLARIONOV [2,3], EMANUELE A. CASU [1], MATTEO CAVALIERI [1], THERESIA KNOBLOCH [2], TIBOR GRASSER [2], AND ADRIAN M. IONESCU [1]

1 Nanoelectronics Devices Laboratory, École Polytechnique Fédérale de Lausanne, 1015 Lausanne, Switzerland
2 Institute for Microelectronics, TU Wien, 1040 Vienna, Austria
3 Division of Solid State Electronics, Ioffe Physical-Technical Institute, 194021 St. Petersburg, Russia

CORRESPONDING AUTHOR: N. OLIVA (e-mail: nicolo.oliva@epfl.ch)

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ABSTRACT We propose double-gated n-type WSe_2 FETs with low leakage, low hysteresis top gate high-k dielectric stack. The top gate dielectric layer is deposited by HfO_2 ALD on an Al_2O_3 seed layer obtained from the evaporation and oxidation by air exposure of a 1.5 nm Al layer. When operated under back gate control, the fabricated WSe_2 FETs behave as n-type enhancement transistors with ON/OFF current ratios exceeding 6 orders of magnitude and a ON current close to 1 μA/μm at a drain bias of 100 mV. An applied negative top gate bias determines a much steeper turn-on of the back gated transfer characteristic and a reduction of the observed hysteresis. Top gate devices behave as n-type depletion FETs, reaching a I_{ON}/I_{OFF} ratio larger than 10^6 under positive bias applied to the back gate. The electron mobility, extracted using the Y-function method, was estimated to be 22.15 $cm^2V^{-1}s^{-1}$ under a drain bias of 1 mV. We characterize the hysteresis dynamics in our devices, demonstrating a substantial improvement with respect to comparable top gated MoS_2 FETs.

INDEX TERMS WSe_2, double-gated FETs, 2D materials, field-effect devices, atomic layer deposition.

I. INTRODUCTION

Two-dimensional (2D) materials recently attracted a remarkable research interest due to their unique, number of layer dependent electrical properties [1]–[3]. The possibility of isolating atomically thin flakes by either mechanical exfoliation or direct growth by CVD provided access to peculiar physical phenomena [4]–[6]. Differently from graphene, the transition metal dichalcogenide (TMDCs) family of materials comprises semiconductors exhibiting large band gaps, enabling the realization of field-effect devices with excellent ON/OFF current ratios [1], [3]. Most of the currently reported semiconducting TMDCs exhibits prevalent electronic conduction, resulting typically in n-type depletion mode FETs, as it is the case for MoS_2. Undoped WSe_2 interestingly shows ambipolar conduction, with demonstrated high hole and electron mobilities [2], [7]–[10] and the possibility of fabricating enhancement mode FETs. This feature combined with the possibility of controlling the device polarity by either the choice of the metal contacts work function or electrostatic doping make this material promising for the realization of a complementary 2D technology [8], [9].

Usually, 2D FETs are realized by relying on a back gate architecture [2], [7]–[11]. The realization of high performance top gated devices has been generally prevented by several challenges related to dielectric deposition on 2D materials. Excellent results in terms of degradation prevention and field-effect mobility have been obtained by capping WSe_2 with hBN flakes [11]–[13], but because of this material low-k and the complexity introduced by the deterministic assembly of 2D/2D heterojunctions this solution is unpractical for the production of high performance, standardized and scaled devices. The direct deposition of high-k dielectrics on 2D materials would be the preferred approach, but it results in either discontinuous, leaky films or a large density of border traps determining huge hysteresis windows [14]–[16].

In a recent work presented at ESSDERC 2018, we reported high performance double gated n-type WSe_2 FETs with excellent top gate subthreshold slope (*SS*) and reduced

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hysteresis [17]. The gate dielectric in our devices consists of a stack of an Al_2O_3 seed layer and a 5 nm thick HfO_2 dielectric layer. The alumina seed layer is obtained from the oxidation of 1.5 nm of evaporated Al [18]–[22], and a 5 nm thick HfO_2 film is deposited by atomic layer deposition (ALD). The fabricated devices were electrically characterized with particular focus on the different impact of the two gates on the channel conduction.

Here, we include a more detailed discussion of both the back gate and top gate hysteresis, characterized as a function of the measurement frequency and the bias window width. We also compare the hysteresis results with those measured for top gated MoS_2 FETs with Al_2O_3 insulator [23] and observe a considerable improvement.

II. DEVICE FABRICATION

The proposed device consists of an asymmetrical double-gated WSe_2 FET, with a common back gate and a top gate overlapping the central part of the semiconducting channel. A schematic of the complete device is shown in Fig. 1 together with the summary of the proposed process flow. The starting substrate consists of a low resistivity p-doped Silicon wafer. ALD in a BENEQ TFS 200 reactor at 200 °C, using TEMAH and H_2O as precursors was performed to deposit the 10 nm thick HfO_2 layer that serves as back gate dielectric. Next, WSe_2 flakes were mechanically exfoliated starting from a bulk crystal sample (synthetized by *hq graphene*) using the scotch taping technique. Thin flakes of appropriate size were then identified by inspecting the sample with an optical microscope.

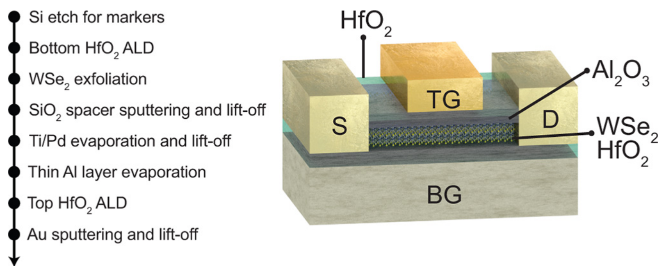

FIGURE 1. Schematic view of the realized double gate devices and summary of the proposed process flow.

Since the back gate is extended over the entire back side of the wafer, if the source and drain contacts were to be deposited directly on the HfO_2 layer the resulting leakage would be considerably larger than the leakage coming from the channel. Consequently, a 50 nm thick SiO_2 film was deposited by sputtering and lift-off on the areas around the flakes so to greatly increase the dielectric thickness between the contact pads and the Si substrate. The source and drain contacts were deposited on the flakes using an electron-beam lithography (EBL) step performed on a PMMA/MMA bilayer resist followed by evaporation and lift-off of a Ti (1.5 nm)/Pd (100 nm) stack. Devices were then completed with the top gate dielectric and metal contact. In order to improve the quality of the dielectric grown on the WSe_2 flake, we deposited a seed layer consisting of 1.5 nm of evaporated Al prior to the ALD step. The Al layer was then oxidized in air to obtain a thin Al_2O_3 film on which 5 nm of HfO_2 were deposited using the same reactor and recipe exploited for the back gate. Finally, the top gate metal was deposited by sputtering and lift-off of a Ni (80 nm)/Au (40 nm) stack after a last EBL step. A colorized SEM image of the complete device is shown in Fig. 2a. The WSe_2 flakes thickness was measured using atomic force microscopy (AFM) in contact mode, as shown in Fig. 2b. The results reported in the following have been obtained from devices realized with few layers flakes.

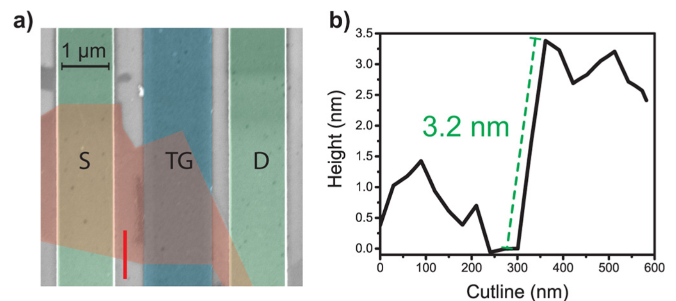

FIGURE 2. a) False colored SEM image of a device after the deposition of the top gate contact. The top gate is extended only over the center of the channel, resulting in a limited control of the ungated regions between the gate and the source/drain contacts. The flake lateral dimension tends to decrease moving from the source to the drain contact, with an average width of 2 μm. The red line shows the cutline along which the AFM profile in b) was measured. The estimated thickness of the flake is 3.2 nm.

III. RESULTS

All the electrical measurements reported in this section have been performed in EPFL at ambient conditions and room temperature using an HP 4156C semiconductor parameter analyzer on a representative device. We focused our analysis on the electron conduction in the channel to reduce the measurements stress on the device. Therefore, in most measurements the gate bias window is asymmetrical with respect to 0 V. The reported transistor is 2.6 μm long and presents an average width of 2 μm, with a channel thickness of 3.2 nm.

A. BACK GATED AND TOP GATED TRANSFER CHARACTERISTIC

In order to study the impact of the back and top gates on the WSe_2 channel conductance we measured the double-sweep transfer characteristics and output characteristics sweeping one of the gates potential while maintaining the second at a fixed bias. The results are reported in Fig. 3. Looking at the two $I_D(V_G)$ curves on a linear scale (Fig. 3a and c) it is clear that the back gated device behaves as an enhancement mode FETs, while when operated under the top gate control the device operates in depletion mode. The drain current of the top gated FET tends to saturate under positive gate bias because of the reduced control of the top gate on the ungated WSe_2 flake areas close to the source and drain

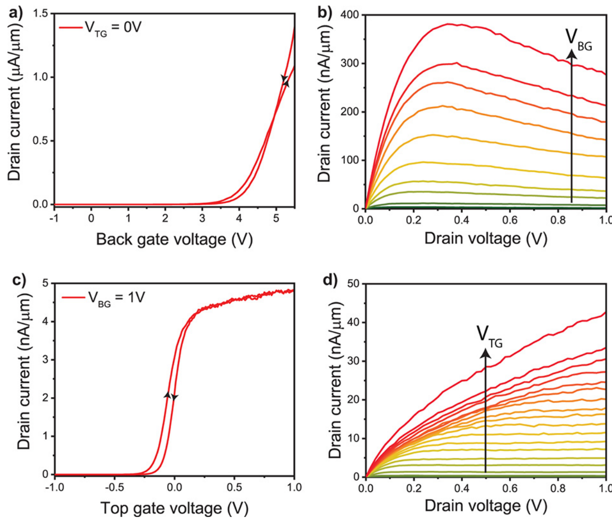

FIGURE 3. Double sweep transfer characteristic $I_D(V_G)$ and output characteristic $I_D(V_D)$ of the fabricated WSe_2 FET. a) Double sweep back gate $I_D(V_G)$ curve measured at $V_{DS} = 100$ mV applying 0 V to the top gate. The sweep rate is 5.2 V/s. b) Back gate $I_D(V_D)$ characteristic measured under a top gate bias of −2 V and for back gate bias in the −1/+6 V range. c) Double sweep top gate $I_D(V_G)$ curve measured at $V_{DS} = 100$ mV applying 1 V to the back gate. The top gate sweep rate is 1 V/s. d) Top gate $I_D(V_D)$ characteristic measured under a back gate bias of +3 V and for a top gate bias in the −2/+1 V range.

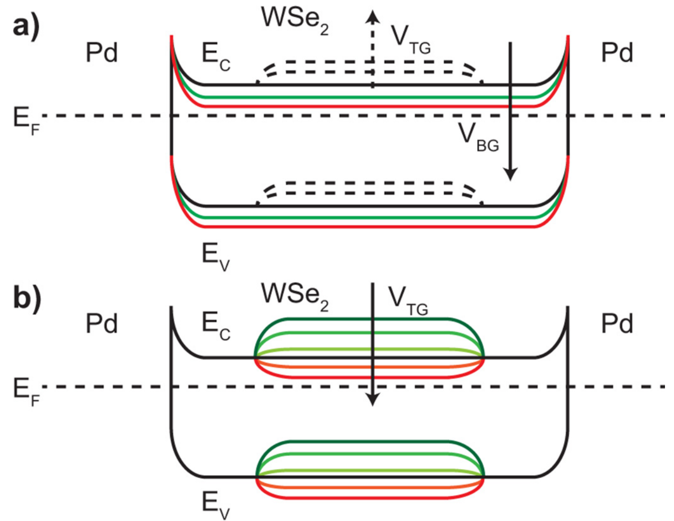

FIGURE 4. Band diagrams of the double-gated WSe_2 FET. a) Band diagram of the back gated FET. Positive back gate biases determine a n-type electrostatic doping, and therefore an increase of the drain current. A fixed bias applied to the top gate modifies the bands at the center of the channel (dotted lines). b) Top gated band diagram. Negative top gate biases determine a depletion of the central part of the channel, turning off the transistor.

contacts (see Fig. 2a). The series resistance offered by these regions is set by the fixed bias applied to the back gate. The hysteresis can be evaluated by comparing the threshold voltage (V_{th}) of the up and down sweeps. The V_{th} value was estimated by the intercept of the linear part of the $I_D(V_G)$ curve. As explained in Section IV, the actual value of the threshold voltage shift between forward and backward sweep is strongly dependent on the gate bias sweep rate (S). The back gated FET exhibits a 272 mV hysteresis when measured with a 5.2 V/s sweep rate. When controlled by the top gate sweep, the device hysteresis is reduced to 70 mV tested sweeping the gate bias at 1 V/s.

The back gate output characteristic in Fig. 3b exhibits current saturation and negative differential resistance is observed at large V_{BG} values, likely because of self-heating effects in the WSe_2 flake [12]. The I_D (V_D) curve for the top gate FET is reported in Fig. 3d, and shows how current saturation is achieved for drain biases below 1 V.

Fig. 4 shows the qualitative band diagram of both the back and top gated WSe_2 FET, including the Pd metallic contacts. Under back gate control, a positive bias determines a lowering of the bands in the channel, resulting in a n-type electrostatic doping and an increase of the current. In this configuration, a fixed bias applied to the top gate affects the center of the channel, contributing to depleting or accumulating it (dotted curves in Fig. 4a). When operated using the top gate, the WSe_2 FET can be set to be normally ON by applying a fixed positive bias to the back gate. By sweeping the top gate voltage towards negative values, the central part of the channel is gradually depleted of electrons and the transistor can be turned OFF. Conversely, setting the top gate bias at positive values, the electron density in the gated section of the channel increases. However, the limited electrostatic control on the ungated sections of the channel determines the already discussed current saturation (see Fig. 3c).

B. IMPACT OF TOP GATE BIAS ON BACK GATED FET CHARACTERISTIC

In order to study the impact of the top gate bias on the back gated device conduction, we measured the back gate transfer characteristic under different fixed top gate voltages (V_{TG}) in the +3 V/−3 V bias window, applying a drain bias of 100 mV. The results are shown in Fig. 5. Sweeping the top gate bias from positive to negative values determines a positive shift of the threshold voltage (inset of Fig. 5a). A positive V_{TG} favors the accumulation of electrons under the top gate. As a result, two channels can contribute to the conduction in the flake: the top one constituted by accumulated electrons while the back one is an inversion channel controlled mainly by the back gate. The resulting subthreshold current shows two different slopes, corresponding to the onset of these two conduction paths. The back gate threshold voltage saturates under positive bias being limited by the potential required to electrostatically dope the flake area not covered by the top gate. Under negative top gate bias, the WSe_2 area below the top gate is fully depleted of electrons and only the inversion channel formed by the back gate dictates the conduction in the flake (see Fig. 4a). This mechanism translates in a unique and steeper subthreshold slope as well as the expected positive shift of the threshold voltage.

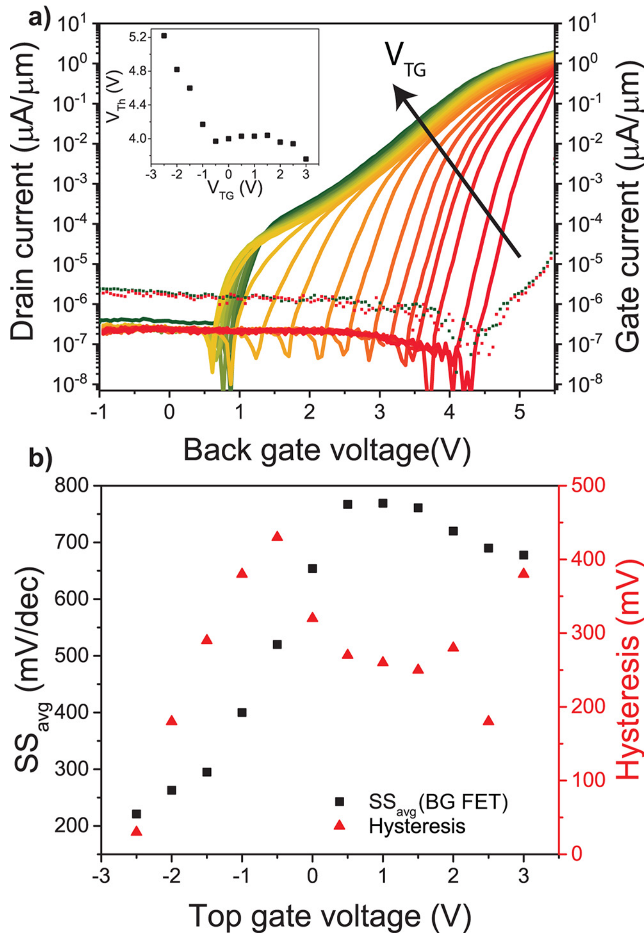

FIGURE 5. a) Normalized transfer characteristic of the back gated FET under different top gate biases, in the +/ − 3 V range. The dotted curves represent back gate leakage current measured at V_{TG} = 3V (green) and V_{BG} = −3V (red). Inset: evolution of the threshold voltage as a function of V_{TG}. b) Negative top gate biases result in a decrease of both the average subthreshold slope of the back gated transfer characteristic and the hysteresis. All the measurements were performed at V_{DS} = 100 mV. The reported transfer characteristics were measured applying a fixed bias to the top gate and sweeping the back gate at a rate of 5.2 V/s.

The I_{ON}/I_{OFF} ratio remains larger than 6 orders of magnitude for all the top gate bias values investigated, despite a small decrease in I_{ON} observed for negative V_{TG} biases. The OFF state current is limited by the back gate leakage, which remains around 1 pA/μm for all the measurements reported thanks to the mentioned SiO_2 layer deposited below the source and drain contact pads. Moreover, a clear increase of the steepness of the subthreshold current is observed, as reported in other implementations of double-gated WSe_2 FETs [12]. Fig. 5b summarizes the evolution of both the average subthreshold slope over 5 orders of magnitude of the output current and the back gate hysteresis with the applied bias to the top gate.

We report in Fig. 6 the normalized back gated transfer characteristic measured at different values of the drain-to-source bias and with $V_{TG} = -2$V. For drain voltages larger than 100 mV, the I_{ON}/I_{OFF} ratio exceeds 6 orders of magnitude, while the average subthreshold slope does not vary significantly with the drain bias.

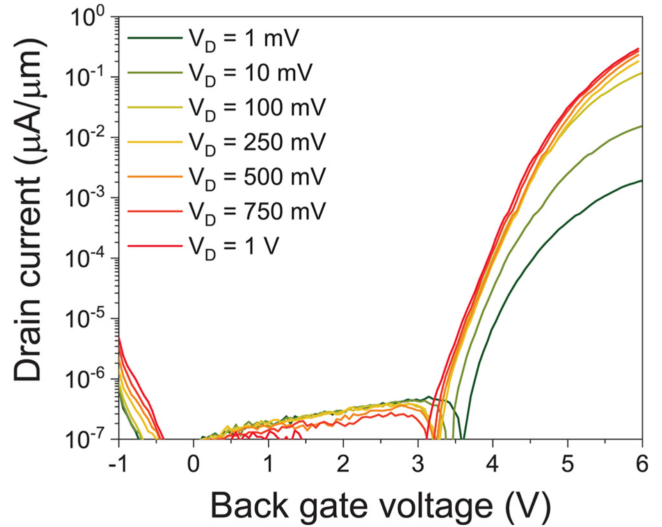

FIGURE 6. Normalized transfer characteristic $I_D(V_G)$ of the back gated FET at different V_{DS} biases in semi-log scale, measured with $V_{TG} = -2$ V. For drain voltages larger than 100 mV, the device exhibits a I_{ON}/I_{OFF} ratio larger than 6 orders of magnitude. The average subthreshold slope does not vary significantly with respect to the drain bias.

C. IMPACT OF BACK GATE BIAS ON THE TOP GATED FET

In order to study the impact of the back gate bias on the top gated device, we measured the top gate transfer characteristic under different back gate voltages (V_{BG}) in the 0V/+3V bias window, applying a drain bias of 100 mV. The results are shown in Fig. 7. The increase of the back gate bias determines a negative shift of the top gated FET threshold and a clear increase of the I_{ON}/I_{OFF} ratio. The top gate leakage current remains below 1 pA/μm for all the reported measurements. Positive V_{BG} values determine an n-type electrostatic doping of the entire WSe_2 channel that can be then depleted of electrons in the central section by applying a negative bias to the top gate. The inset of Fig. 7a shows how the threshold voltage decreases linearly with the increase of the back gate bias, with an extracted −0.2 V shift for applied volt to the back gate. The evolution of both the average subthreshold slope and the I_{ON}/I_{OFF} ratio is reported in Fig. 7b. For back gate biases larger than 2 V, the ON/OFF current ratio exceeds 6 orders of magnitude, and the top gated FET reaches performance equivalent to the back gated device while maintaining a steeper turn-on characteristic. The average subthreshold slope over 4 orders of magnitude of the output current reaches values close to 100 mV/dec, and degrades only slightly with the increase of the back gate bias. Fig. 7c shows the subthreshold slope as a function of the drain current for both the upward and the downward sweep, measured under V_{BG} = 3 V and V_{DS} = 100 mV. The extracted top gate SS is quite independent from the direction of the top gate bias sweep.

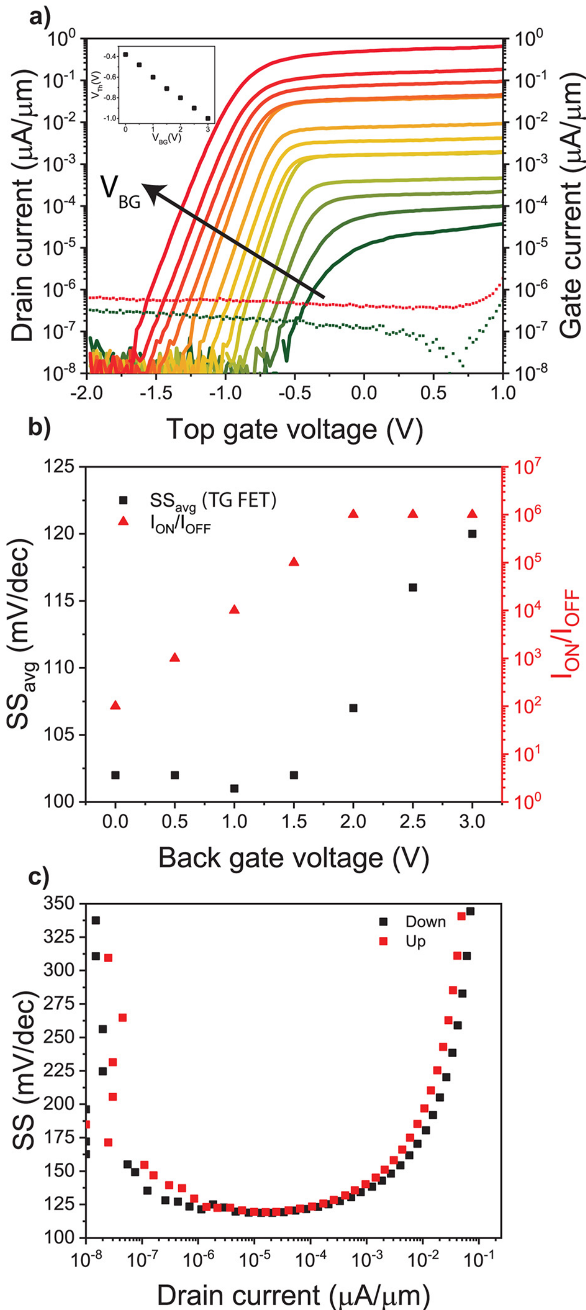

FIGURE 7. a) Normalized transfer characteristic of the top gated device under different fixed back gate voltages in the 0/+3V bias range measured at V_{DS} = 100 mV. The dotted curves represent the top gate leakage currents measured at V_{BG} = 0V (green) and V_{BG} = 3V (red). Inset: threshold voltage as a function of the applied V_{BG}. b) Evolution of I_{ON}/I_{OFF} ratio and average subthreshold slope over four orders of magnitude of the output current of the top gated FET as a function of the fixed bias on the back gate (V_{BG}). c) Subthreshold slope as a function of the drain current for both the upward and downward cycles, measured applying V_{BG} = 3V and V_{DS} = 100 mV. A good match is observed between the two sweeps, with a minimum SS below 125 mV/dec. All these results have been obtained sweeping the top gate bias at 2.4 V/s and applying a fixed bias to the back gate.

In Fig. 8 we show the top gated normalized transfer characteristic measured under increasing values of the drain-to-source bias and applying a 3 V back gate voltage.

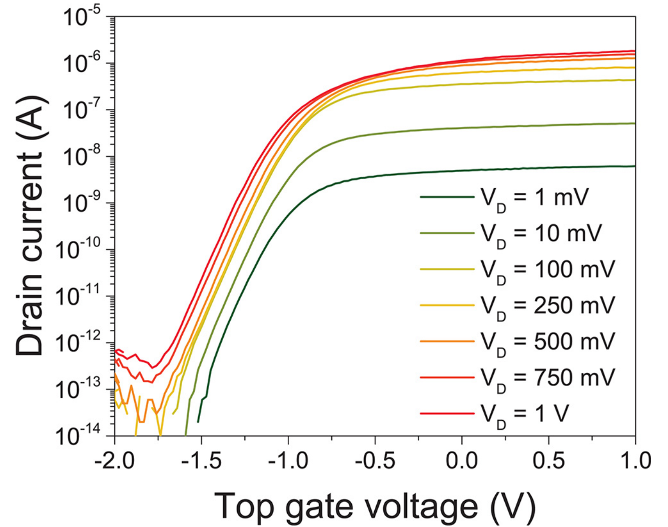

FIGURE 8. Normalized transfer characteristic $I_D(V_G)$ of the top gated FET at different drain-to-source biases on the semi-log scale, measured at V_{BG} = 3V. For drain voltages larger than 100 mV, the device exhibits a I_{ON}/I_{OFF} ratio larger than 6 orders of magnitude.

Similarly to what was observed for the back gated characteristic, a drain voltage of 100 mV is sufficient to obtain an ON/OFF current ratio larger than 10^6. Remarkably, the average subthreshold slope is not affected by the increase of V_{DS}.

D. FIELD EFFECT MOBILITY EXTRACTION

We extracted the two-terminal effective field effect mobility, μ_{FE}, using $\mu_{\mathrm{FE}} = g_{\mathrm{m}} L / W C_{\mathrm{ox}} V_{\mathrm{DS}}$, where g_{m} is the transconductance extracted from the linear part of the top gated $I_{\mathrm{D}}(V_{\mathrm{G}})$ curve, W is the channel width and C_{ox} is the top gate capacitance per unit area, that has been directly measured by characterizing MIM structures included on the same wafer of the devices. The obtained electron mobility at $V_{\mathrm{DS}} = 1$ mV and $V_{\mathrm{BG}} = 3$ V is 10.74 $\mathrm{cm^2V^{-1}s^{-1}}$.

In order to obtain a more accurate estimation of the carriers' mobility by decoupling part of the impact of the contact resistance, we applied the so-called (Ghibaudo) Y function method [16], [24], [25]. Assuming that the contact resistance is not dependent on the gate bias, the Y function expression reduces to:

$$Y = \frac{I_{\mathrm{D}}}{\sqrt{g_{\mathrm{m}}}} = \sqrt{\frac{\mu C_{\mathrm{ox}} |V_{\mathrm{DS}}| W}{L}} (V_{\mathrm{G}} - V_{\mathrm{T}}) \tag{1}$$

where V_T is the threshold voltage.

Fig. 9 shows the extracted Y function for the reported top-gated FET, obtained with $V_{\mathrm{DS}} = 1$ mV and $V_{\mathrm{BG}} = 3$ V. From the fitting of the linear region, in red in the figure, it is possible to extract the low field electron mobility, estimated to be 22.15 $\mathrm{cm^2V^{-1}s^{-1}}$, in line with the two-terminals mobility reported in other works on WSe_2 FETs [7]–[10], [26].

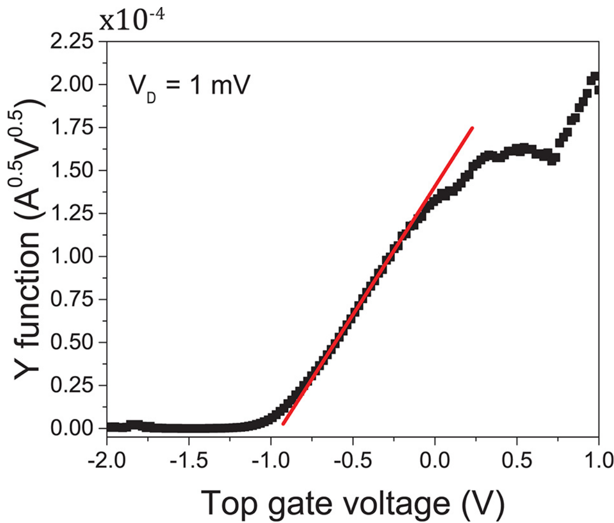

FIGURE 9. Extracted Y function vs top gate voltage for the top gated FET at $V_{DS} = 1$ mV and $V_{BG} = 3$ V. The mobility can be extracted from the fitting of the linear part of the curve, shown in red in the figure.

IV. HYSTERESIS DYNAMICS

Finally, we perform a detailed study of the hysteresis dynamics in our devices by measuring the gate transfer characteristics using different sweep rates and, consequently, sweep times t_{sw}. The results presented in this section have been obtained at TU Wien measuring under vacuum conditions. Two few-layers representative devices (flake thickness around 3 nm) were tested, indicated in the following as Device 1 and Device 2. In order to correctly represent our results, we extract the hysteresis width ΔV_H near the threshold voltage and plot it versus the measurement frequency $f = 1/t_{sw}$, as was suggested in our previous work [23].

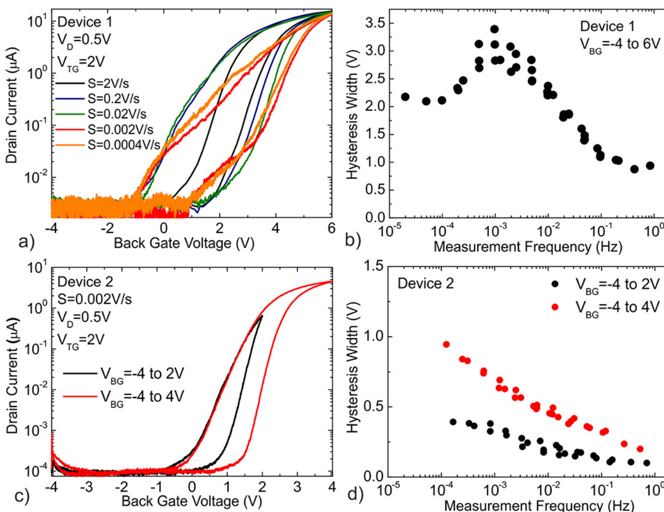

FIGURE 10. a) The back gate transfer characteristics of the Device 1 measured using different sweep rates. b) The corresponding $\Delta V_H(f)$ dependence exhibits a maximum. c) The back gate transfer characteristics of the Device 2 measured using very slow sweep rates and different sweep ranges. d) The corresponding $\Delta V_H(f)$ dependences exhibit an increase of the hysteresis for slower sweeps.

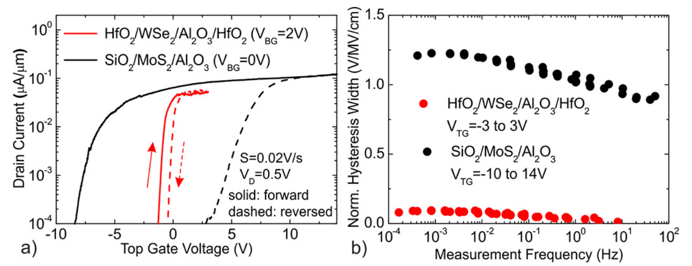

FIGURE 11. a) Comparison of the top gate transfer characteristics for our devices and their counterparts with MoS_2 channel and Al_2O_3 (23.5nm) top gate insulator [23]. The current is normalized by the channel width. b) When normalizing ΔV_H to the oxide field factor, the hysteresis in our devices appears considerably smaller.

In Fig. 10 we show that the dynamics of hysteresis observed on the back gate transfer characteristics can be different for different devices. For instance, Device 1 exhibits some saturation in the hysteresis for very slow sweeps (Fig. 10a), which leads to a clear maximum of the $\Delta V_H(f)$ dependence (Fig. 10b). This behavior is very similar to our predictions [27] and means that a considerable number of oxide defects contributing to the hysteresis have enough time to become charged during the slow sweeps. The latter also affects the shape of the gate transfer characteristics, as we see in Fig. 10a. In contrast, for the Device 2 (Fig. 10c, d) we observe an increase of the hysteresis width for slow sweeps, while the maximum is not reached. At the same time, the hysteresis becomes larger for wider sweep ranges, which indicates that a larger amount of oxide defects comes into play [23].

In Fig. 11a we show the hysteresis on the top gate transfer characteristics of our devices and CVD-grown MoS_2 FETs with 23.5nm thick Al_2O_3 as a top gate insulator reported in our previous work [23]. For a proper comparison of the hysteresis in different technologies, we normalize ΔV_H by the oxide field factor $K = \Delta V/d_{ox}$, where ΔV is the sweep range width and d_{ox} is the oxide thickness. Thus, in Fig. 11b we show that in our devices with scaled top gate insulator the hysteresis is over an order of magnitude smaller. At the same time, the dependence versus the measurement frequency is similar in both cases, which suggests that the hysteresis is caused by similar oxide defects in Al_2O_3 which present a fundamental property of this material.

V. CONCLUSION

In summary, we have demonstrated double gate n-type WSe_2 FETs with excellent high-k top gate dielectric obtained combining an evaporated and oxidized thin Al_2O_3 seed layer and the ALD of a 5 nm thick HfO_2 film. The resulting device can be controlled by either the top or the back gate, using the opposite gate to finely tune the FET performance. When back gated, the device behaves as an enhancement FET, whose hysteresis and subthreshold slope can be greatly improved by applying a negative voltage to the top gate. An average subthreshold slope close to 200 mV/dec has been achieved. Conversely, the top gated transistor works in depletion, and

the back gate bias can be exploited to enhance the ON/OFF current ratio and shift the threshold voltage. As a result, the device exhibits an I_{ON}/I_{OFF} ratio larger than 10^6 and an average subthreshold slope approaching 100 mV/dec, which is independent from the drain bias. Both the top and the back gate are characterized by a leakage current below 1 pA/μm in all the reported electrical measurements. Finally, the hysteresis of the top gate transfer characteristics is considerably improved compared to previously reported top-gated MoS_2 FETs with thicker Al_2O_3 insulator [23].

We believe that the proposed approach for the deposition of high-k dielectrics on WSe_2 provides a promising path for the development of high performance top-gated FETs. Given the small leakage current measured, the dielectric stack could be subject to a further scaling of the HfO_2 layer thickness while seed layers with better dielectric performance than Al_2O_3 could contribute to an enhanced top gate control. Readily oxidized thin metallic layers have been reported to greatly influence the quality of dielectric ALD on 2D materials [21]. An improvement of the drive current and ON/OFF current ratio requires the reduction of the contact resistance, achievable by an annealing of the contacts prior to the deposition of the top gate dielectric [27], [28].

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