Fast-switching Tri-Anode Schottky Barrier Diodes for monolithically integrated GaN-on-Si power circuits

Luca Nela, Georgios Kampitsis, *Member, IEEE,* Jun Ma, and Elison Matioli, *Member, IEEE*

Abstract—**Tri-Anode GaN Schottky Barrier Diodes (SBDs) have recently shown excellent DC performance with low turn-on voltage and large breakdown thanks to their 3D contact structure around the two-dimensional electron gas (2DEG) channel. However, the 3D nature of the Tri-Anode structure is also often believed to hinder the device switching performance. In this work, we demonstrate that, on the contrary, the Tri-Anode architecture significantly enhances the device switching performance with respect to conventional planar SBDs, as shown by a substantial decrease in the recovery charge and an improvement in frequency response. The Tri-Anode SBDs excellent static and dynamic performance is then applied to a real circuit to demonstrate a monolithically integrated high-frequency Full Bridge Rectifier. These results show the potential of Tri-Anode SBDs for high-efficiency and fast-switching power integrated circuits.**

Index Terms— **GaN SBD, Tri-Anode, SBD recovery charge, Power ICs, Diode Bridge Rectifier.**

I. Introduction

GaN-on-Si devices are widely envisioned as promising candidates for ultra-fast, compact, and high-efficiency future power electronics applications, thanks to the superior GaN properties [1]–[3]. In addition, lateral GaN technology allows the monolithic integration of several devices on the same chip, enabling the beginning of a new era of power integrated circuits (ICs). While significant progress has been made on High-Electron-Mobility Transistors (HEMTs) and integrated gate driver solutions are already commercially available [4], [5], the development of lateral GaN SBDs has faced a more challenging path. In particular, the high electron concentration of the two-dimensional electron gas (2DEG) results in a large electric field peak at the Schottky barrier, drastically limiting the device blocking capabilities.

Recently, several works have shown significant improvement in the SBDs performance by relying on different architectures such as recessed anodes [6]–[8], field plates [9], [10] and Tri-Gate / Tri-Anode hybrid structures [11]–[15]. In particular, GaN SBDs adopting a Tri-Gate architecture have

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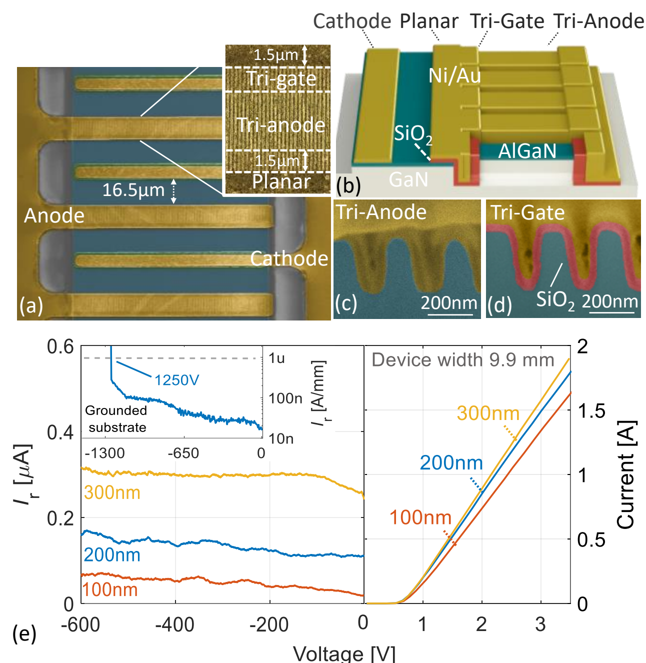

Fig. 1. (a) SEM image of the scaled up SBD fingers. The right-hand inset zooms on the anode finger, highlighting the Tri-Anode, the Tri-Gate, and the planar region. The Tri-Gate and the Planar length is 1.5 µm. For the planar device, no nanowire is etched and the planar MOS region is 3 µm-long (b) Device schematics (c-d) Focused Ion Beam (FIB) cross section of the Tri-Anode and the Tri-Gate structure for 100 nm-wide nanowires with 100 nm spacing. (e) I-V characteristic and reverse leakage curve for Tri-Anode anode devices with different width (at 150ºC, an increase in the reverse leakage lower than 5 times was observed with respect to the room temperature measurements). The total device width is 9.9 mm. In the inset, the SBD breakdown curve is shown.

demonstrated large breakdown voltage (V_{BR}) up to 2 kV with low turn-on voltage and on-resistance [14]. In addition, the Tri-Gate technology provides several other advantages such as Enhancement-mode operation by tuning the nanowire width [16]–[18], high transconductance [19], small subthreshold swing (SS) [20], high ON/OFF-state current ratio [21], diminished short channel effects [21], [22], and the ability to control multiple channel heterostructures [13], [23], [24].

Despite these remarkable results, the effect of the Tri-Gate 3D architecture on the switching behavior of lateral AlGaN/GaN based devices has not yet been investigated and there are concerns about the possible capacitance increase due to its 3D nature, as it has been reported for other technologies such as bulk FinFETs [25].

To address this question, this work aims to provide a thorough switching performance characterization of scaled-up hybrid Tri-Anode SBDs, which are compared to conventional GaN diodes based on a planar architecture and typical fast-

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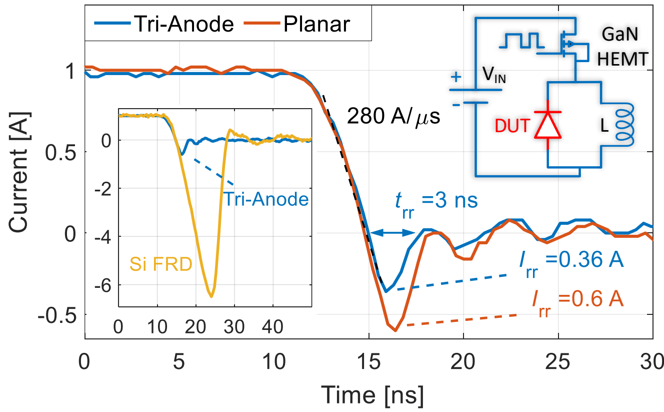

Fig. 2. Reverse recovery measurement for a planar GaN SBD and a Tri-Anode SBD with *w* of 200 nm. The *di/dt* was set to 280 A/µs and the reverse voltage to -100 V. The double pulse circuit used in the experiment is show on the top right. The left-hand inset shows the reverse recovery for Tri-Anode GaN SBDs compared with a commercial Si FRD (600 V rated [27]). A significant Q_{rr} reduction is observed for the Tri-Anode device with respect to the Si-based diodes.

	Si FRD	Planar	W300	W200	W100
t_{rr} [ns]	15	4	3.5	3	3
I_{rr} [A]	5	0.5	0.44	0.3	0.25
Q_{rr} [nC]	41	1.02	0.9	0.5	0.3
$R_{ON}{\cdot}Q_{rr}$ [nC·Ω]	14.3	3.5	1.3	0.62	0.49

Table 1. t_{rr}, I_{rr}, Q_{rr}, and $R_{ON}{\cdot}Q_{rr}$ comparison for planar and Tri-Anode diodes with different fin width, and Si FRD [26]. The forward current (I_F) was set to 1 A and the reverse voltage (V_{rr}) to -50 V.

recovery Si diodes. The results from recovery charge characterization, capacitance measurement and AC rectification demonstrate, instead of a degradation, a significant enhancement in switching performance for the Tri-Anode architecture. Finally, the promising potential of this technology for future power ICs was unveiled by demonstrating a monolithically integrated, scaled-up diode bridge rectifier.

II. Device structure

The devices were fabricated on a GaN-on-Si heterostructure consisting of 4.2 µm of buffer, 420 nm of unintentionally doped GaN (u-GaN) channel, 20 nm of $Al_{0.25}Ga_{0.75}N$ barrier and 2.9 nm of u-GaN cap-layer. The electron concentration and mobility of the two-dimensional electron gas (2DEG) from Hall measurements at room temperature were 1.25×10^{13} cm^{-2} and 1700 cm^2/V·s, respectively. The fabrication process started with electron-beam lithography to define the mesa and nanowires in the anode region. The sample was then etched by Cl_2-based inductively coupled plasma etching (ICP) to a depth of 220 nm. The width of the nanowires in the anode was varied from 100 nm to 300 nm (W100, W200 and W300), while the nanowires spacing was fixed to 100 nm. The cathode contact was formed by a stack of Ti (20 nm)/Al (120 nm)/Ti (40 nm)/Ni (60 nm)/Au (50 nm) and annealed at 780 °C for 30 s. 20 nm-thick SiO_2 was conformally deposited over the nanowires by atomic layer deposition (ALD) and then removed in the Tri-anode region by wet etching with HF 1%. A Ni/Au metal stack was then evaporated to form the anode contact (50 nm/150 nm) followed by 1 µm-thick metal pads. No passivation layer was

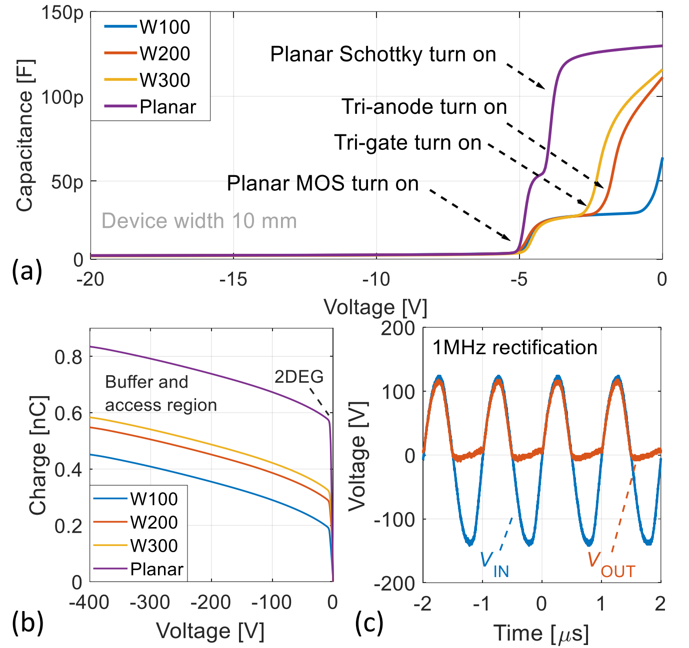

Fig. 3. (a) Capacitance versus reverse voltage (V_R) curve for Tri-Anode and Planar diodes. (b) SBD reverse charge obtained by integrating the capacitance curve for $V_R \in [-400 ; 0]$ V. (c) Half-wave rectification for a Tri-Anode SBD with fin width of 200 nm for a 1 MHz input signal with peak-to-peak amplitude of 250 V.

deposited on top of the devices. A Scanning Electron Microscope (SEM) image of the SBD is shown in Fig. 1(a) while the Focused Ion Beam (FIB) cross section of the Tri-Anode and Tri-Gate region is presented in Fig. 1(c-d).

The cathode to anode distance was set to 16.5 µm and 50 alternating anode-cathode fingers were integrated for a total device active width of 9.9 mm. Scaled devices are desirable for a proper measurement of the switching properties of the devices, to reduce the effect of the measurement circuit parasitics, which are typically comparable to the capacitance value of small area devices and may lead to erroneous results. Planar diodes without Tri-Anode structure were co-fabricated on the same chip and used as reference devices. To ensure a fair comparison, the same total field plate length of 3 µm was designed for both the Tri-Anode and the planar devices, with the only difference between the two structures consisting in the 1.5 µm-long Tri-Gate region and Tri-Anode contact (Fig. 1(b)).

III. Device Characterization

The I-V characteristics and the reverse blocking performance of the diodes under investigation are shown in Fig. 1(e). The Tri-Anode architecture leads to significant enhancement in the DC performance thanks to the side Schottky contact to the 2DEG and the Tri-Gate control over the channel, which effectively reduces the reverse leakage [15], [27] and operates as a field plate to achieve large breakdown voltage (V_{BR}) [12], making the diodes suitable for 600 V rating.

Fig. 2 shows the reverse recovery curve for the Tri-Anode SBD and the planar reference, measured with a double-pulse tester (DPT) circuit, able to provide high *di/dt* transitions (Fig.2 right-hand inset). A first pulse charges the inductor to the desired current, which is then forced through the diode during

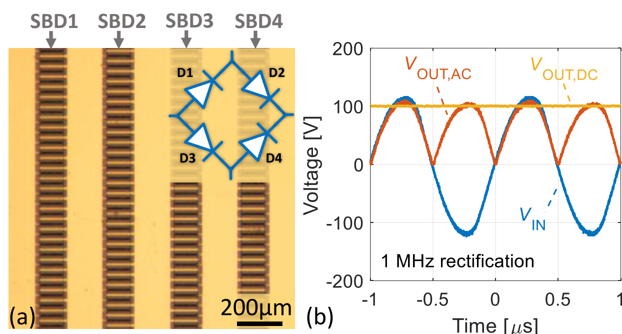

Fig. 4. (a) Optical microscope image of the integrated full bridge rectifier and corresponding circuit schematics (b) Full-wave rectification for a 1MHz input signal with a peak-to peak amplitude of 250 V. Full AC-to-DC conversion is achieved by the addition of a smoothing capacitor.

the *dead time*. A second pulses then causes the SBD abrupt transition to the off-state, allowing the measurement of the recovery time and charge. The diode forward current (I_F) was set to 1 A, the reverse voltage to -100 V and the *di/dt* to 280 A/µs, determined by the gate resistor of the top-side transistor.

A significant reduction in the reverse recovery charge (Q_{rr}) and current undershoot (I_{rr}) is observed for the Tri-Anode SBDs with respect to the planar reference, resulting in a 40% decrease in I_{rr} and a two-fold reduction in Q_{rr}. This is of fundamental importance as it shows that the Tri-Anode architecture leads to faster devices with lower switching losses. In addition, a major improvement is observed for the Tri-Anode SBDs with respect to a commercial 600V-rated fast-recovery (FRD) Si diode [26] with similar current rating (Fig. 2, left inset).

To understand the advantageous switching characteristics of the Tri-Anode architecture, the off-state *C-V* curve of the SBDs under study was experimentally extracted using a Keysight B1505 analyzer (Fig. 3(a)). This shows a first step at V_G=-5 V, in correspondence to the planar region depletion, and a second and third steps, close together, corresponding to the depletion of the Tri-Gate and Tri-Anode regions, which move to smaller V_G as the fin width is reduced and result in a significant capacitance decrease.

This behavior, which is in contrast with the results from doped bulk Fin-FETs, originates from the conduction through the 2DEG and the absence of accumulation/inversion charge at the nanowire/oxide interface, and can be readily understood by considering the total charge (Q_{CV}) stored in the reverse region. Fig. 3(b) presents the Q_{CV} obtained from the integration of the *C-V* curve (Fig. 3(b)) which shows a consistent decrease in value as the width of the Tri-Anode is reduced. Such a result is caused by the partial removal of the 2DEG due to the nanowire etching in combination with the fin sidewalls depletion and the AlGaN barrier strain relaxation [28], [29] which lead to a charge decrease in the nanowire, reflected in the shift of the second capacitance step towards 0 V. The capacitive charge reduction with the fin width is consistent with the Q_{rr} trend extracted from the reverse recovery measurement (Table 1). However, while the capacitive charge is a precious tool to gain insights on the Tri-Anode physics, Q_{rr} better reflects the device operation in a real circuit as it also takes into account the charge stored during forward conduction.

It is moreover noteworthy that the Tri-Anode architecture leads to a major reduction in the $R_{ON}{\cdot}Q_{rr}$ figure-of-merit (Table 1) compared to planar devices, and nearly a threefold decrease when reducing the nanowire width from 300 nm to 100 nm. Such an improvement is achievable thanks to the substantial charge decrease for smaller Tri-Anode widths (Fig. 3(b)), which leads to only a minor degradation of the on-resistance (Fig. 1(d)). The slight increase in the diode R_{ON} is due to the partial 2DEG removal in the Tri-Anode region and it can be overcome by employing a high-conductivity heterostructure such as the Multi-Channel platform [13]. The reduced Q_{rr} is highly beneficial for the diode frequency operation as illustrated in Fig. 3(c) which shows the half-wave rectification with minimum signal distortion during zero crossing for a 250 V peak-to-peak signal at 1 MHz. Further measurements at higher voltages to investigate the device switching behavior in the full operating range are the subject of our future work.

To demonstrate the potential of this technology for integrated power ICs topologies, four of the presented diodes were monolithically integrated to form a Full Bridge Rectifier (FBR). Fig. 4(a) shows a picture of the fabricated device and the corresponding circuit schematics. A proper full wave rectification is obtained at a frequency of 1 MHz, as shown in Fig. 4(b). The slight input signal distortion is caused by the frequency limitation of the source used in this experiment. This operating frequency compares very well with other GaN-based integrated circuits presented in the literature [30]–[33] and shows the promising potential of GaN for fast-switching power ICs. In addition, a complete AC to DC conversion is achieved by the addition of a smoothing capacitor in parallel with the load, demonstrating a monolithically integrated AC-to-DC GaN power converter.

IV. Conclusions

In this work, we presented the promising potential of Tri-Anode SBD for fast switching power application which is highlighted by the reduced reverse recovery charge and capacitance with respect to the planar architecture, leading to high-frequency half-wave rectification. The Tri-Anode SBDs were monolithically integrated in a diode bridge rectifier to realize AC-to-DC integrated power converter at high switching frequencies. These results demonstrate that the Tri-Anode SBDs combine excellent static and dynamic characteristics and can be a fundamental building block for future power GaN ICs.

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