Material and Electrical study of HfO2-Based Resistive Random Access Memories (ReRAMs)

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par

Behnoush ATTARIMASHALKOUBEH

Acceptée sur proposition du jury

Prof. G. De Micheli, président du jury
Prof. Y. Leblebici, Prof. P. Muralt, directeurs de thèse
Dr M. Shayganpoor, rapporteur
Dr N. Raeishosseini, rapporteuse
Prof. C. Dehollain, rapporteuse

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As you start to walk out on the way,
the way appears.
— Rumi

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My siblings, who are the best one can ask for. My brother *Babak* who from his childhood always looked out for me, motivated and when it was needed pushed me even if it means setting a password on the TV during my exam time in the high school to force me to study! My sister, *Bahareh* and her calming, loving character, made me feel not far from home, thank you Bahareh for being my best friend and all those nights you slept with the lights on in our bedroom when I studied late at night. My amazing brother-in-law *Farshid*, who joined later to our family and became my second brother, not by blood but by love.
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Lausanne, 20 September 2019 Behnoush Attari

Abstract

Resistive Random Access Memories (ReRAMs) have been researched intensively in the last past decades as a promising alternatives technology for the next generation non-volatile memory (NVM) devices. ReRAM's excellent performance with high switching speed, excellent scalability, and low power consumption, together with accessible fabrication techniques have raised increasing interests and encourages further studies.
A ReRAM device in its most basic structure consists of a thin layer of a transition metal oxide (TMO) sandwiched between two metal layers (Top and Bottom Electrodes). ReRAMs could be categorized into different groups regarding the implemented materials and their performance.The concept of switching mechanism is straightforward; the as-fabricated devices appeared to be highly resistive (HRS); when the top electrode (TE) is biased, the resistance state of the devices switched to the lower resistance level (LRS) in an operation called SET. This process is commonly reversible through the application of proper negative external stimuli, which can change back to the high resistance state of the device from LRS to HRS.
Oxygen vacancies are recognized as the main elements controlling the device performance. During the set process, the oxygen vacancies rearrange to form conductive bridges between the TE and bottom electrode (BE). Further application of negative biases can partially/ fully dissolve the conductive filaments and led to HRS by disconnecting the two metallic electrodes from one the other.
The switching mechanism is due to relocation and movement of oxygen vacancies, but the stochastic nature of the formation of filament also makes it hard to control this phenomenon precisely. As a result, the reported variation issue in the key switching parameters of ReRAMs, lessens the reliability of this technology and hinders its commercialization.
To suppress the variability hurdle in ReRAMs, it is crucial to have a better understanding of the switching mechanism. Hence, the interaction between deposited materials in the as-fabricated devices and during electrical measurements under external stimuli needs to be intensely studied to obtain an in-depth knowledge of the behavior of the oxygen vacancies.
The first purpose of this research is to overcome the variation in the key switching parameters of stand-alone ReRAMs to be used in cross-point structures. Among various TMO materials, Hafnium oxide (HfO_2) is considered as a promising oxide due to its excellent performance results (i.e. : high switching speed, endurance, on/off ratio) and accessibility of deposition tools.
In this work, we implemented two main approaches to improve the reliability and uniformity of HfO_2-based ReRAMs; the structural engineering, and post-fabrication thermal treatment

and studied the effect of each method on the performance of HfO_2-based fabricated ReRAMs. ReRAMs due to their simple structure can be implemented to the cross-point Configuration. The simple but yet effective cross-point design, allows an effective cell area of $4F^2$ in 2D, while the feasibility of achieving 3D configuration by stacking multiple 2D layers, brings down the cell area to $4F^2/n$ and leads to the remarkably high integration density. However, the sneak current through unwanted neighbor cells significantly decreases the system efficiency, deteriorates the read margin, and limits the maximum size of a cross-point array. To overcome the sneak path issue, different strategies could be implemented; among all, serially connecting each memory element to an additional selection device in a 1S1R con
figuration is an active way to introduce selectivity to the cross-point arrays.
In the second part of this work, we introduced a novel one-selector one-resistor (1S1R) configuration, which eliminates the need for the physical wiring and provides valuable information on isolated selector/resistor and the integrated 1S1R.

Résumé

Les Resistive Random Access Memories (ReRAM) ont fait l'objet de nombreuses recherches au cours des dernières décennies en tant qu'alternative technologique prometteuse pour la prochaine génération de dispositifs à mémoire non-volatile. Les excellentes propriétés des ReRAMs telles que la vitesse de commutation élevée, la scalabilité, la faible consommation énergétique ainsi que les techniques de fabrication accessibles ont suscité un intérêt croissant et encourage à de nouvelles recherches.

Un dispositif ReRAM dans sa structure la plus simple consiste en une fine couche d'oxyde de métal de transition (TMO) intercalée entre deux couches métalliques (électrodes du haut et du bas). Les ReRAMs peuvent être catégorisées en différents groupes en fonction des matériaux mis en œuvre et de leur performance. Le concept du mécanisme de commutation est simple ; les dispositifs tels que fabriqués apparaissent comme étant hautement résistifs (HRS) ; lorsque l'électrode supérieure (TE) est polarisée, l'état de résistance des dispositifs passe au niveau de résistance inférieur (LRS) dans une opération appelée SET. Ce processus est généralement réversible par l'application de stimuli externes négatifs appropriés, qui peuvent changer l'état de résistance du dispositif de LRS à HRS.

Les vides d'oxygène sont reconnus comme les principaux éléments contrôlant les performances du dispositif. Pendant le processus de réglage, les vides d'oxygène se réorganisent pour former des ponts conducteurs entre les électrodes supérieure et inférieure qui, en appliquant des tensions négatives supplémentaires, peuvent les dissoudre partiellement ou totalement et conduire à un état hautement résistif (HRS) en séparant les deux électrodes métalliques l'une de l'autre.

L'excellente performance des ReRAMs est rendue possible grâce à leur mécanisme de commutation qui est basé sur le déplacement et le mouvement des vides d'oxygène à l'échelle nanométrique. Cependant, la nature stochastique de la formation du filament rend difficile le contrôle précis de ce phénomène. Par conséquent, les problèmes de variations signalés dans les principaux paramètres de commutation des ReRAMs réduisent la fiabilité de cette technologie et entravent sa commercialisation. Pour faire face à cet obstacle, il est crucial de mieux comprendre le mécanisme de commutation. Ainsi, les interactions entre les matériaux déposés dans les dispositifs fabriqués et pendant les mesures électriques sous stimuli externes doivent être intensément étudiées pour obtenir une connaissance approfondie du comportement des vides d'oxygène. Le premier objectif de cette thèse est d'éliminer la variation des principaux paramètres de commutation des ReRAMs autonomes à utiliser dans les structures à points de croisement. Parmi les différents oxydes de métal de transition (TMO), l'oxyde

d'hafnium (HfO_2) est considéré comme un oxyde prometteur en raison de ses excellentes performances et de l'accessibilité des outils de déposition.
Dans cette thèse, nous avons mis en œuvre deux approches principales pour améliorer la fiabilité et l'uniformité des ReRAMs à base de HfO_2 : l'ingénierie structurale et le traitement thermique post-fabrication.
Grâce à leur structure simple, les ReRAMs peuvent être implémentés dans les structures à points de croisement. La conception simple mais efficace de cette structure permet d'obtenir une surface efficace de $4F^2$ en 2D, tandis que la possibilité d'obtenir une configuration 3D en empilant plusieurs couches 2D, ramène la surface à $4F^2/n$ et conduit à une densité d'intégration remarquablement élevée. Cependant, le courant de fuite à travers les cellules indésirables voisines diminue considérablement l'efficacité du système, détériore la marge de lecture et limite la taille maximale d'un réseau de points de croisement. Pour surmonter le problème du courant de fuite, différentes stratégies pourraient être mises en œuvre. Parmi toutes celles envisagées, relier en série chaque élément de mémoire à un dispositif de sélection supplémentaire dans une configuration 1S1R est un moyen actif d'introduire la sélectivité dans les tableaux à points de croisement.
Dans la deuxième partie de cette thèse, nous avons introduit une nouvelle configuration avec un seul sélecteur et une seule résistance (1S1R), qui élimine le besoin de câblage physique et fournit des informations précieuses pour le sélecteur/résistance isolé et le 1S1R intégré.

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1 Introduction

1.1 Semiconductor Timeline

In 1833, English scientist Michael Faraday's discovery of benzene resulted in the first observation of semiconductor materials. He noticed the electro-conductivity of "silver sulfide" increased with increasing temperature. He wrote: "I have lately met with an extraordinary case ... which is in direct contrast with the influence of heat upon metallic bodies ... On applying a lamp ... the conducting power rose rapidly with the heat ... On removing the lamp and allowing the heat to fall, the effects were reversed."
In 1874 German physicist Ferdinand Braun probed a lead sulfide using thin metal wire; he noticed the current flowed freely in just one direction which today is recognized as the rectification effect in diodes. The Braun's semiconductor didn't have any useful application until early 1900 when it was used in radio as a signal detector.
In the early 1900s, electrical engineer Greenleaf W. Pickard working in American Telephone and Telegraph tested thousands of mineral samples to study their rectification properties and discovered Silicon crystals to demonstrate the best results. Later in 1906, he founded the first company to produce and sell silicon-based semiconductor devices, which was "cats's-Whisker" a crystal radio detector (Figure 1.2). The German word "halbleiter" translated in English as "semiconductor" was first used in 1911 to describe materials with electro-negativity in middle of metals and insulators.
In 1926, Polish-American physicist and inventor Julius Lilienfeld introduced a field-effect transistor using copper-sulfide semiconductor (Figure 1.3). In 1931, Alan Wilson, a British physicist working in Leipzig Germany, created a model semiconductor behavior. In his paper, he proposed the semiconductor behavior was due to the presence of impurities in pure crystals of the materials. Later he tried to explain the diode effect using quantum-mechanical tunneling between metal and semiconductor materials, but it was not till 1938, which a proper explanation of rectification phenomenon finally emerged. Several scientists from different countries independently attributed the rectification phenomenon to a correlation between the concentration of electrons and setting up an asymmetric barrier to current flow.
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transistor using copper-sulfide semiconductor. In 1931, Alan Wilson, a British physicist working in Leipzig Germany, created a model semiconductor behavior. In his paper, he proposed the semiconductor behavior was due to the presence of impurities in pure crystals of the materials. Later he tried to explain the diode effect using quantum-mechanical tunneling between metal and semiconductor materials (see Figure 1.4, but it was not till 1938, which a proper explanation of rectification phenomenon finally emerged. Several scientists from different countries independently attributed the rectification phenomenon to a correlation between the concentration of electrons and setting up an asymmetric barrier to current flow. In 1940, Russell Ohl in Bell Telephone Labs in NJ introduced the concept of n-type (for negative) and p-type (positive) semiconductor. He exposed a small piece of silicon to bright light and noticed different parts of the pieces of silicon responded differently regarding the type of impurities it is containing. The part with phosphorus yielded more electrons comparing to the part with boron, led to to the deficiency of electrons and introduced the interface of those two parts as a p-n junction. In 1947, in BELL labs, the use of various impurities in providing the n-type or p-type of semiconductor through the implementing the elements of the fifth column of the periodic table (n-type: phosphorus) and third column (p-type: boron) had been investigated. Finally, in 1948, William Shockley introduced the junction transistor based on Ohl's discovery. On June 30, 1948, the first "transistor" implementing gold and germanium has been introduced by Shockley at a press conference in New York.
In 1957, Fairchild semiconductor started its work in Palo Alto followed by many other high-tech companies such as Intel and AMD as the first silicon-based company in Silicon-Valley.
In 1960 the first concept of MOSFET (Metal Insulator Semiconductor Field Effect Transistor), which is widely used by now in all manufactured microchips, has been introduced (Figure 1.8.
By 1952, after a few intensive years of research on semiconductors, the "Sonotone" a hearing aid including a germanium transistor has been introduced to the market with the value of 229.50 USD (Figure 1.7).
Eventually, the semiconductor transistors replaced vacuum tubes in digital computers, in 1956 Bell Labs introduced a computer using 700 point-contact transistors and more than 10,000 diodes. On April 1954, the silicon transistors dominated the markets over the germanium transistors. The accidentally discovered silicon dioxide (SiO_2) layer, soon became essential to protect the silicon wafers during manufacturing. Since 1955 and the first attempts in employing photolithography tools to define small designs on a silicon wafer (200 micrometers was achieved by 1957), up to now (below 0.1micrometer), the photolithography process has been considered as an essential step in semiconductor industries.
In 1973, the Fairchild Lab. introduced the first CMOS design, using p and n-channel MOSFET with almost zero power in standby mode, what is known as CMOS nowadays. By 1964, achieving a higher density of MOSFETs with low cost of production, due to complicated manufacturing and reliability appeared more difficult than predicted earlier.Finally, in 1965, Gordon Moore, the R D head of Fairchild and later the co-founder of Intel, published an internal paper and predicted that the number of integrated components on a chip would double every year[56].
In 1975, at the IEEE Electron Device Meeting, Moore announced a modification in his previous

prediction, he slowed the predicted rate of increase in complexity to be " doubling every two years" taking into account the new data. In 1995, Moore announced that "The current prediction is that this is not going to stop soon."
Moore's prediction known as "Moore's Law" is considered as the standard principles of the semiconductor industries have attempted to achieve ever since.
Despite, the achievement of the industry staying faithful (and predicted to be for few more years to come) to Moore's law, but several limiting factors have appeared and are believed to prevent the industries in following the predicted growing pace, the economical [64] and physical limitation[57].
In spite of lower end-consumer prices for higher density components, the production costs have increased significantly. The costs of research, development, manufacturing, fabrication, and tests have increased continuously by introducing each new generation, known as Rock's law[63].
The Moore's law from 1965 when there were less than 100 transistors in an integrated circuit, has stayed valid till now with millions of transistors on a single chip. In an interview in 2007 at Intel's twice-annual technical conference, Moore stated: "another decade, a decade and a half I think we'll hit something fairly fundamental," he quoted Stephen Hawking says: "When Stephen Hawking was asked what the fundamental limits to microelectronics are, he said the speed of light and the atomic nature of matter" [51]. Therefore, considering an ultimate physical limitation to Moore's law would set a future boundary to electronics miniaturization[61].
By continuous miniaturization, the quantum mechanical effects start to show significant effects as quantum tunneling is considered to be as one of those phenomena. In quantum tunneling, when barriers reach a thickness of below 1-3nm, the electrons can pass through the electric field[44] with higher probability, this effect has been already seen for a while and has gotten worse by lower scaling. The quantum tunneling is an origin of leakage current that disturbs the scaling down the transistors, which causes significant power waste and the heating issues for semiconductor industries. Besides, the memory technologies which uses capacitors for bit-storage suffer from non-quantum based leakage current troubles. Notably, the dielectric leakage current caused by manufacturing material imperfections in the dialectic material insulator is considered to be a major problem. As the density of defects increases with the miniaturization of transistors, the problem gets more severe[81] [52].
In 2015, the CEO of Intel, Brian Krzanich, has noted that: " Brian would say that the difference between seven and five nm technologies is that it's only going to get harder, and there will be fewer and fewer people able to do it." He predicted which we can expect the 5 nm technology to arrive around 2020, then continued with two years of the product cycle, and be produced by 2022; but after that, Moore's law will reach its logical end. Recently, in April 2019, the Taiwanese Semiconductor Manufacturing Co. (TSMC) and Samsung announced their achievement in reaching to 5 nm technology. The new 5nm technologies are claimed to offer a 15 percent higher speed and a 30 percent gain in power efficiency. Interestingly, as Brian predicted, among all semiconductor manufacturer just TSMC and Samsung are offering the 5nm technology, they can afford the immense investment and are expecting reasonable profits.

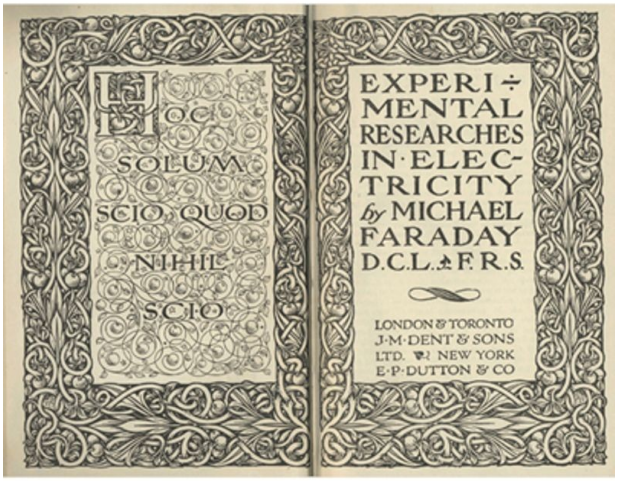

Figure 1.1 – A 1914 reprint of Faraday's 1839 publication of "Experimental Researches in Electricity", adapted from [1].

Figure 1.2 – A commercialized crystal detector introduced in early 1900s, picture courtesy of : John D. Jenkins, www.sparksmuseum.com.

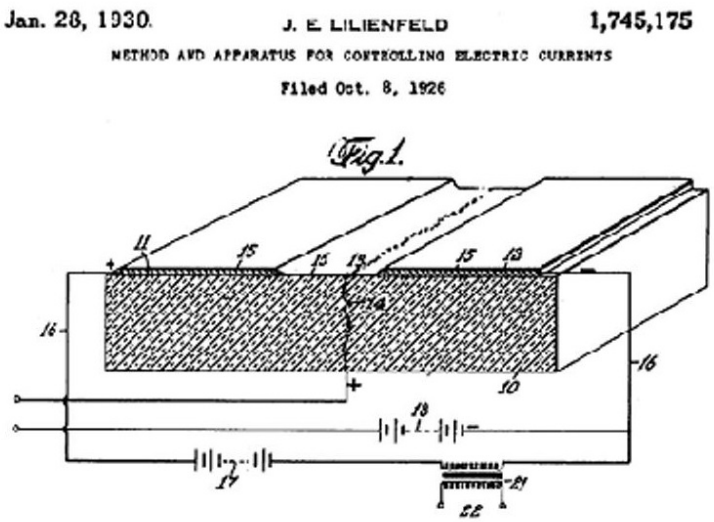

Figure 1.3 – An illustration from the original Lilienfeld's patent depicting a field-effect transistor.

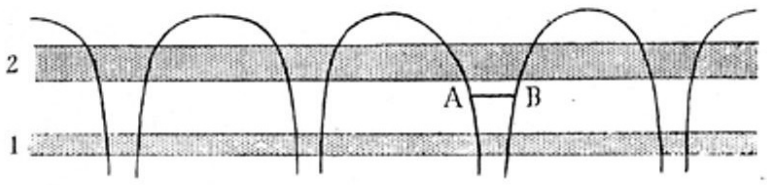

Figure 1.4 – Wilson's sketch depicting energy band gap with impurity level, Courtesy of Siemens Corporate Archive, Munich.

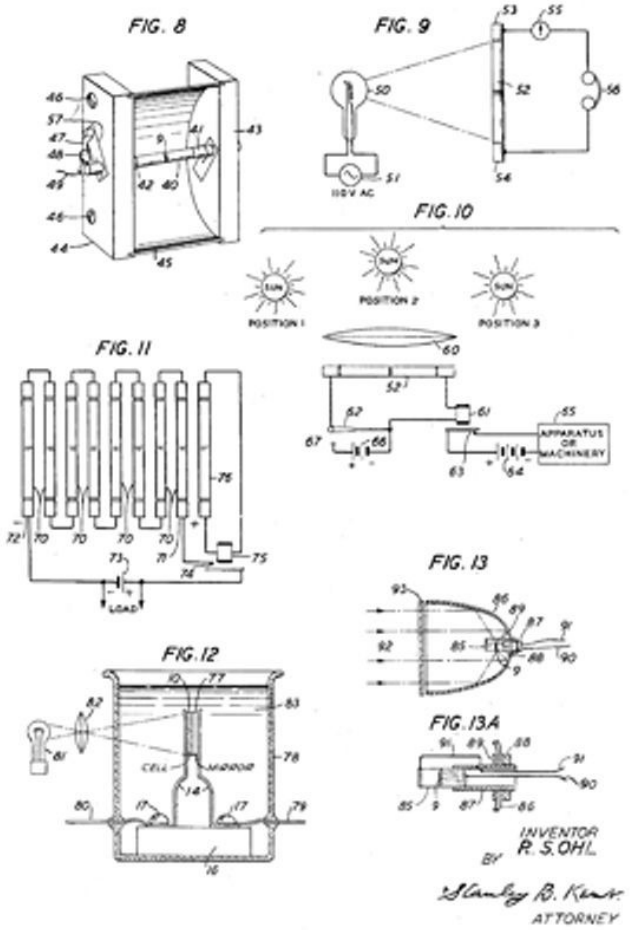

Figure 1.5 – A page of Ohl's patent field in 1941.

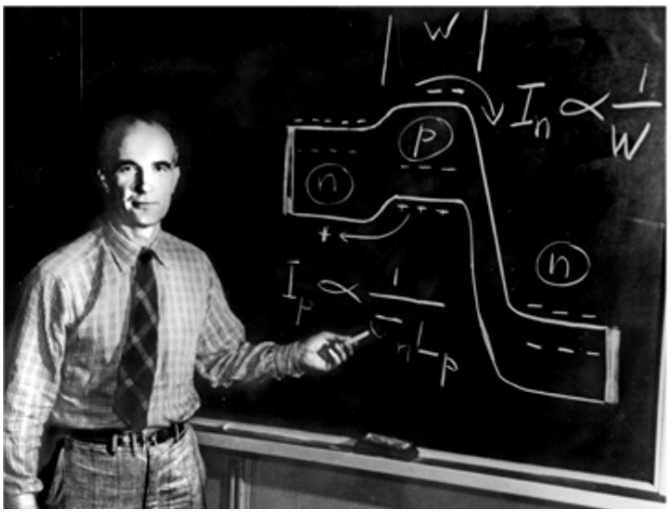

Figure 1.6 – A 1948 image which shows Shockley describing his junction transistor based theory, © 2006-2007 Alcatel-Lucent. All rights reserved.

Figure 1.7 – The Sonotone hearing aid, the device contains one germanium transistor and two tubes, Courtesy of Bob McGarrah.

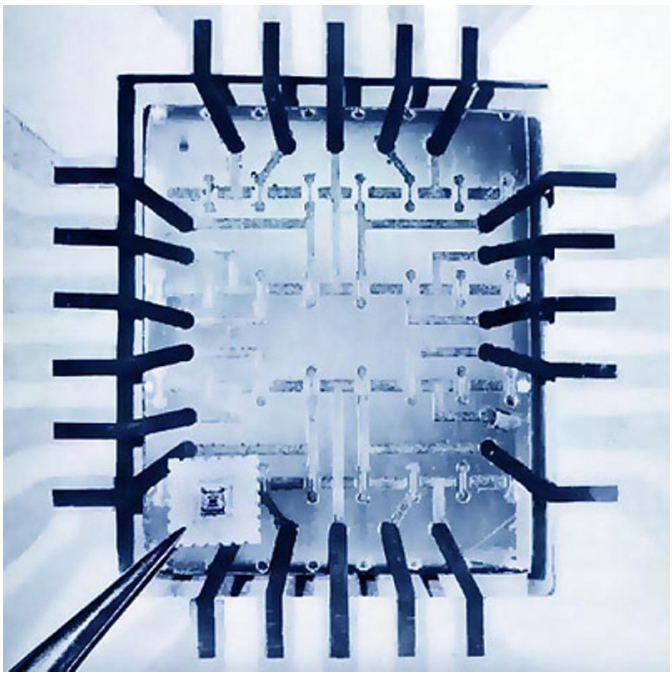

Figure 1.8 – RCA 16-transistor MOSFET circuit demonstrated in front of an enlarged image of it, credits:RCA Incorporated.

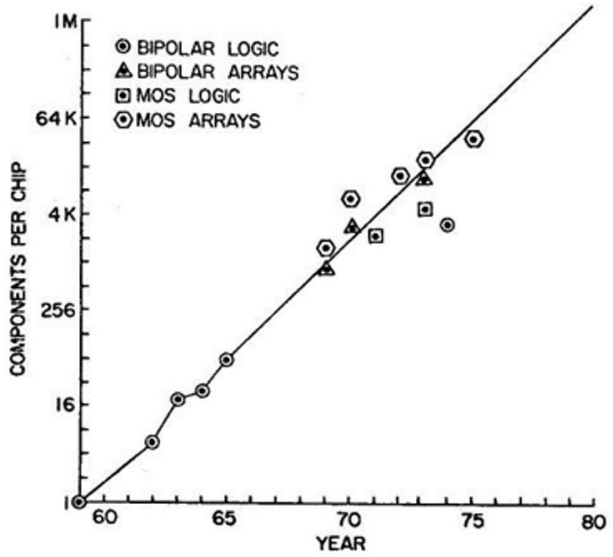

Figure 1.9 – Dr. Moore's prediction of number of integrated components on a chip.

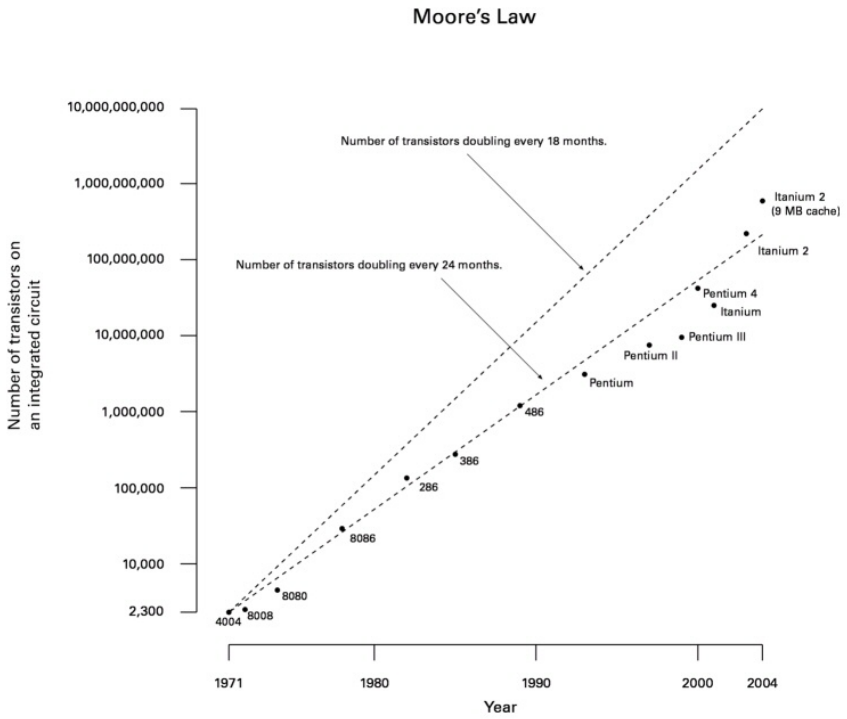

Figure 1.10 – Dr. Moore's Law, the first and second edition.

1.2 Classification of Semiconductor Transistor-based Memory Technologies

Semiconductor memories can be classified based on many functional criteria. As one of the major classification, silicon-based semiconductor memories can be categorized according to the number of times they can be re-written to random access memories (RAMs) and read-only memories (ROMs); unlike ROMs, in RAMs there is no limitation in the number of reading or writing cycles to any cell, in almost identical time.
The memory technologies could also be categorized to volatile and non-volatile[10]. In volatile memories, the stored information/data will be erased when the power supply turned off [52], while the non-volatile memories (NVM) retain the data even in the absence of power supply.

1.2.1 Volatile Memory

Dynamic RAMs (DRAM) and Static RAMs(SRAM) are considered as the two main technologies of volatile memories, whose need voltage supply to retain their information, while Flash technology is nonvolatile and hold their information without one. SRAMs are very fast (write/erase time : approximately 0.3ns) while the speed is more than 10ns for DRAM, also each SRAM cell includes 4 to 6 transistors, with $140F^2$ feature size ("F" is the minimum feature size), while DRAM has a smaller configuration of one-transistor and one-capacitor (1T1C) with $6F^2$ minimum cell size (Figure1.11. Therefore, SRAMS are used as cache (the access time is the main criteria), where the main memories benefit from high-density DRAM technologies.

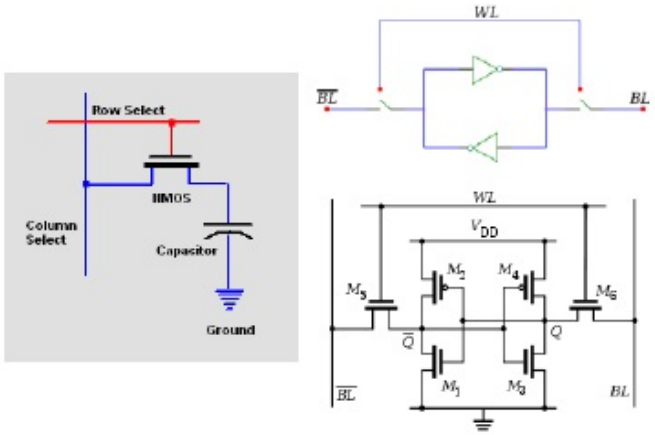

Figure 1.11 – DRAM (left) and SRAM (right) cells, adapted from[75].

By scaling down the transistors, the electric field barrier becomes smaller, and the electrons can cross it with higher probability. The resulted leakage current becomes more noticeable for the thickness below 3 nm[44]. As mentioned earlier, both DRAM and SRAM consist of

transistors in their structure; therefore scaling down is considered as a significant problem in these technologies.

1.2.2 Non Volatile Memory

Today, the nonvolatile memories, especially hard disk drives, are generally used for the long term storage. The reliable hard disk technology offers high endurance but is considered to be quite slow with the access latencies around few milliseconds [60], hence is being gradually replaced with flash-based technology.
Flash memory is a nonvolatile MOSFET, using a floating gate and tunneling current to write/erase the information. Flash technology comes in NAND or NOR technologies, offering high capacities, small size (2-10F^2) and relatively low cost of production, however, suffers from the low speed much slower than DRAM (microsecond) and low endurance. The average endurance of high-density flash memories are generally around 10^4-10^5 (few specific researches reported 10^6 for NAND and 10^7 for NOR)[60][11], which is not able to fulfill the industry demanded endurance.
Table1.1 adapted from [47], provide a comparison between the leader of conventional memory technologies.

Table 1.1 – A comparison between conventional memory technologies

Factors	SRAM	DRAM	Flash (NOR-NAND)
Feature size	50-120	6-10	10, 2-5
Read time(ns)	1-2	10-60	10,50
Write/erase Time(ns)	1-2	10-60	10^5-10^7, 10^4-10^6
Endurance	10^{16}	10^{16}	10^5,10^5
Power Consumption(read/write)	Low	Low	High,High
Power Consumption(Other)	Leakage Current	Refresh Power	No,No
Data Retention	No	No	Yes,Yes

1.3 Emerging Memory Technologies

Recently, the memory industries have an increasing demand for scaling down the feature size in microelectronic products, but the conventional charge-based memory technology have limitation of 8 nm tunnel oxide layer thickness to make 10 years data retention and prevent the charge loss, therefore new technologies have been introduced as intensively studied to overcome the scaling hurdle. The emerging NVM technology includes resistive RAM (i.e., PCRAM and ReRAM) and magnetoresistive RAM (i.e., STT-RAM) are yet in their early stages and require further studies. The tables 1.2 adapted from [47], provides an overview over comparison of all emerging memory technologies.

Comparing Table1.1 and 1.2, it can be concluded which the emerging NVM are relatively better

Table 1.2 – A comparison between emerging memory technologies

Factors	STT-RAM	PCRAM	ReRAM
Feature size (F^2)	4-20	6-12	<4
Read time (ns)	2-20	20-60	10-50
Write/erase Time (ns)	2-20	50-120	10-100
Endurance	10^{15}	10^{10}-10^{12}	10^{15}
Power Consumption (read/write)	Read Low, Write High	Med	Low
Power Consumption (Other)	No	No	No
Data Retention	Yes	Yes	Yes

than conventional memory technologies with lower cell size and power consumption. To gradually replace the conventional memory technologies, the emerging technologies must have low power consumption, high read/write speed, small feature size, and high density[47].

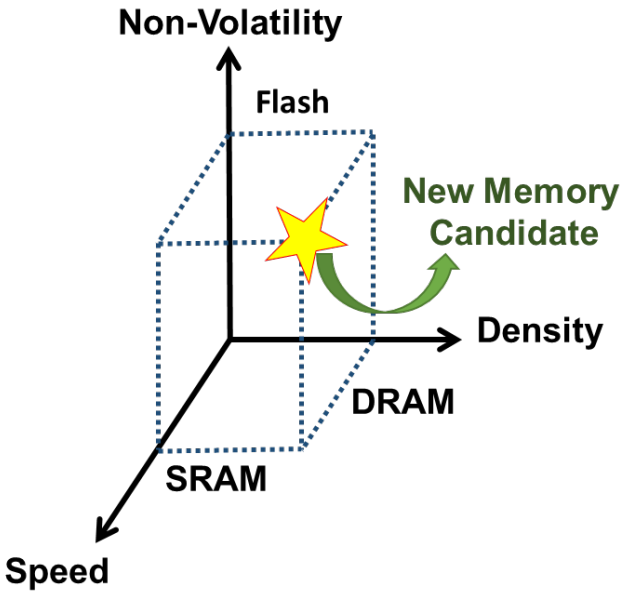

Figure 1.12 – The emerging memory technology must provide a proper trade-off between required properties of industries

Figure1.12 schematically demonstrates how the emerging memory technology should provide a proper trade-off between three main criteria of 1-Non-volatility, 2-density, and 3-Speed.

Among all candidates, the Resistive Random Access Memory (ReRAM) are considered as a promising candidate with low memory size feature (4 F^2), low power consumption and high endurance and retention time. In following the ReRAM technology, working mechanism, the

material selection will be explained in more details.

2 Resistive Random Access Memory (ReRAM)

As the conventional charge-based memory technologies have failed to fulfill the constantly increasing demand of industries for further miniaturization, the researches are intensively focused on the emerging memory technologies including ferroelectric RAMs (FRAMs), magnetic RAMs (MRAMs), phase-change RAMs (PRAMs) and resistive RAMs (RRAMs). FRAMs and MRAMs have faced limitation in miniaturization regarding their large memory cells, while PRAM has faced a hurdle in its commercialization due to the large power needed to switch between amorphous and crystalline phases[32].
The discovery of resistive switching (RS) is dated back to 1962 when Hickmott[31] first observed large negative differential resistance in thin oxide films such as SiO_x, $Al2O_3$, ZrO_2, Ta_2O_5 and TiO_2, followed with the same observation for more materials in a capacitor-like structure[29][22]. The strong interests in RS had declined over time in competition with Si-based memories but have raised again in the late 1990s when Zhuang et al.[90] introduced a 64-bit $Pr_{0.7}Ca_{0.3}MnO_3$ ReRAMs array using a 0.5CMOS process for NVM application. The Zhuang et al.'s research demonstrated relatively low operation voltage (<5 V), on/off ratio of more than 10^3 and fast switching speed (10 ns). Introducing the first organic-based ReRAM in 2002 [50] followed by exciting demonstration[8] of the first transition-metal-oxide based ReRAM with improved switching properties (operating voltage<3 V, set/reset operation of 10^6, and 10^{12} reading endurance) have boosted the research on ReRAMs and opened up new perspectives to explore different materials and structures to improve the ReRAM device performance.
Today, ReRAMs are considered as the fourth fundamental passive circuit elements also known as memristors (predicted in the early 1970s by L. Chua [20]) and are proposed to be implemented for a wide range of applications including neuromorphic and stochastic computing circuit for unconventional computing (used for multi-parallel computing[37][27]) and FPGA (as re-configurable switches[72]).

Figure2.1 shows the number of publications per year (2004-2013) adopted from[58]

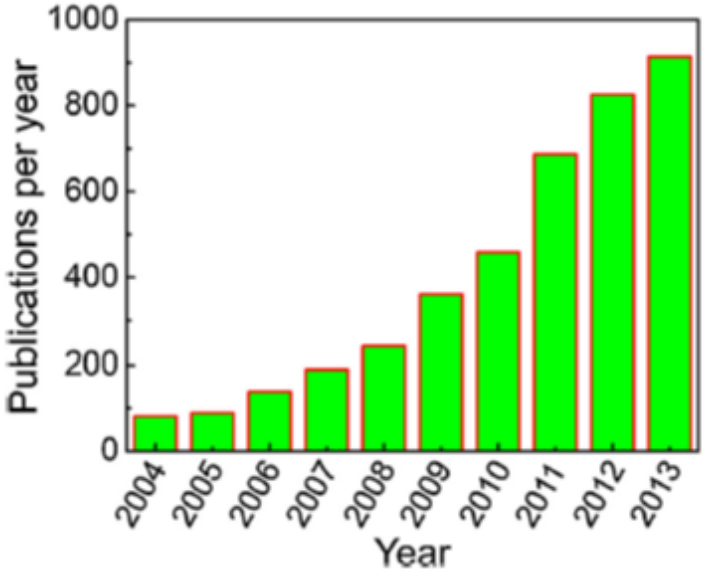

Figure 2.1 – the increasing number of publications per year between 2004 to 2013 highlights the role of ReRAM as a promising NVM.

2.1 The structure

ReRAMs, with their low-cost fabrication and compatibility with conventional semiconductor processes, are believed to have the potential to be used as a universal memory technology. ReRAM is a two terminal device that consists of a metal oxide layer sandwiched between two metal electrodes(top and bottom electrodes), also known as metal-insulator-metal (MIM). The resistance of ReRAMs can be precisely modulated via the application of external stimuli between at least two different levels.

2.2 Classification of ReRAMs

The conductivity can be electrically switched between high resistance state (HRS, "0") and Low resistance state (LRS, "1") through "Set" and "Reset" operations. The specific resistance state of the device could be maintained after the electric stimulus is canceled, which is the indication of non-volatility of the ReRAMs.

2.2.1 Classification based on the Type of Resistive Switching

According to the device performance under electrical characterization, the ReRAMs can be classified into two groups: unipolar and bipolar. In unipolar devices, the set and reset operations happen regardless of the polarity of the applied voltage. In contrast, in bipolar ReRAMs, the switching property depends on the polarity of the applied voltage with set and reset operations happening in different polarities. Figure 2.2 shows b) MIM structure working

with a) unipolar, and c) bipolar operation modes.

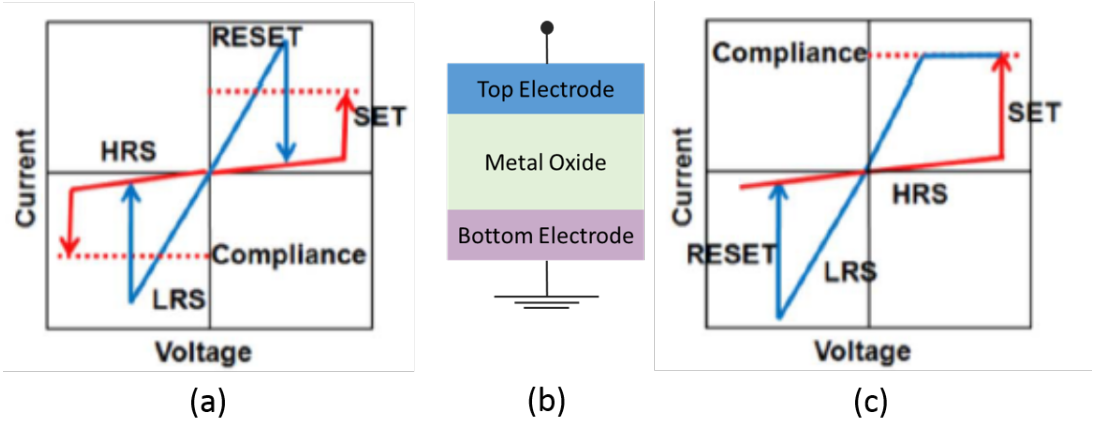

Figure 2.2 – Schematic demonstration of a) I-V switching of a unipolar ReRAM, b) MIM structure, and c) I-V switching of a bipolar ReRAM.

2.2.2 Classification based on the Mechanism of Resistive Switching

The ReRAMs can be categorized into two groups of filamentary and interface switching by the conduction mode in their LRS[25].

Interface switching-Type ReRAMs

In this category, the filaments can not form between the two electrodes; therefore, the contact resistance of the interface controls the switching performance of the device. This type of switching is normally observed in structures with one ohmic and one Schottky-like interface[25] (considering a three-layer structure).

Filamentary-Type ReRAMs

In this category, formation and annihilation of conductive local filaments (CF) determine the resistance state of the device. The CFs are composed of metallic nano-bridges[86] or oxygen ions[84] depending on the choice of materials for ReRAMs. Formation of CFs can bridge between two metal electrodes and the current in LRS can flow through these confined path within the insulator layer. In this category, Zhang et al has reported[89] that the LRS resistance is independent of the device size while the resistance in HRS is depending on its size and increases when the size decreased. Figure 2.3 schematically demonstrate the filamentary and interface-type mechanism of resistive switching.
Further mentioning of ReRAMs refers to the filamentary type oxide- based ReRAMs (OxRAMs).

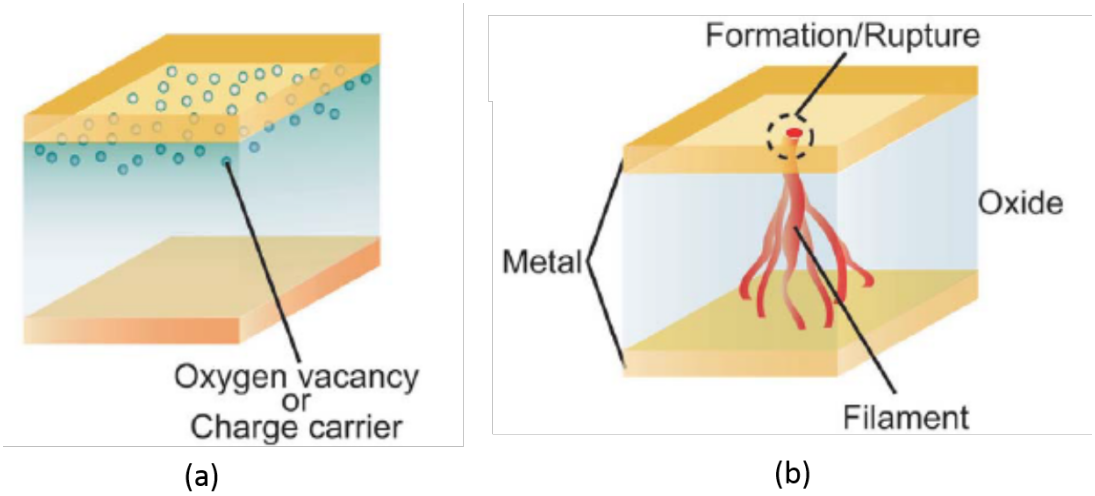

Figure 2.3 – Schematic demonstration for a) A Filamentary ReRAM,and b) An interface-type ReRAM, adopted from [65].

2.3 Mechanism of Resistive Switching in ReRAMs

The switching mechanism in ReRAM is depicted schematically in Figure 2.4 in the following. In general, the as-fabricated ReRAM device (pristine state) are considered to be highly resistive. The device undergoes electrical characterization as the TE is biased while the BE is grounded. During the first sweep of positive voltage (also known as electro-forming and forming voltage), the dielectric goes through a soft breakdown and oxygen ions drift to TE by the applied electric field. If the TE is a noble material, the migrated oxygen vacancies remain there as neutral non-lattice oxygen, while they react with oxidable TE and form an interfacial oxide layer. Noble metals form very robust and dense chemisorption bonding with oxygen atoms instead of forming metal-oxide oxides[46]. However, if an oxygen-reactive metal such as Al is used as TE, a very thin layer of highly insulating oxide will be formed at the interface which can hinder the forming process[21].
In ReRAMs in the LRS state, the current flows through CF within the insulator layer. As the formation of CFs is reversible via application of negative polarity biases, the oxygen ions drift back from the TE to the insulator layer and recombine with the oxygen vacancies and return the ReRAM device to the HRS. Lower set voltage (V_{set}) can be expected to be seen for following cycles as the reset might not dissolve all formed CFs.

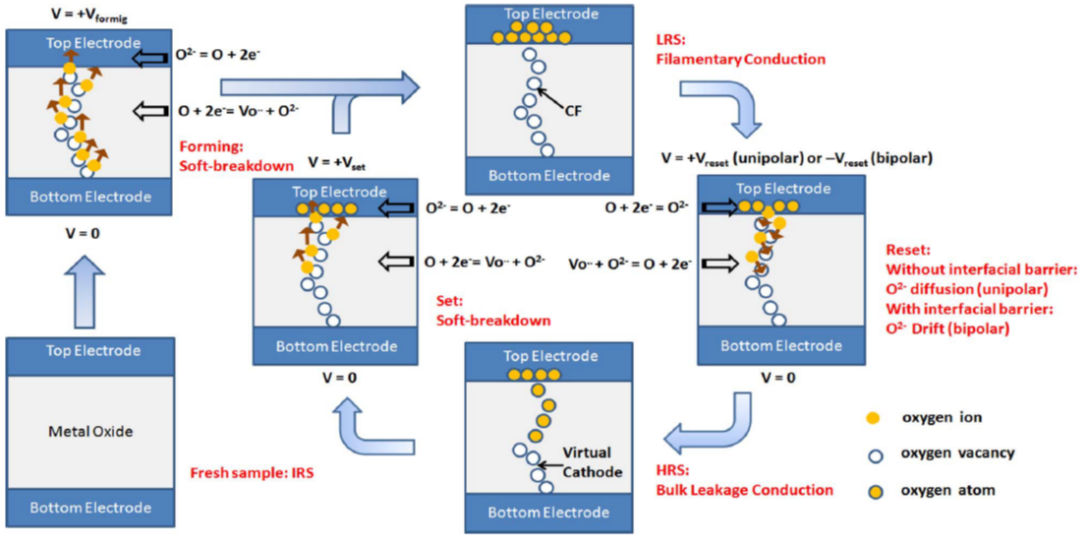

Figure 2.4 – Schematic demonstration of the resistive switching process, including electro-forming, set, and reset steps for a simple binary metal-oxide ReRAM device, adopted from[88].

2.4 The Choice of Material and the Device Properties

As mentioned earlier, ReRAM devices are usually composed of a metal-oxide or dielectric layer sandwiched between two metal-electrodes.

Metal-Oxide or Storage Media

Over the last decades, numerous oxide materials have been studied as dielectric/storage media for ReRAMs. Generally, the organic materials show a highlighted better stability in switching properties over inorganic materials [65].
Among all introduced materials, HfO_2 appeared as a superior candidate for the storage media of ReRAMs. As it is depicted in Table 2.1, HfO_2-based ReRAMs show a proper trade-off between different parameters of resistive switching.
Recently, *Atomic Layer Deposition tool* (ALD) is considered as a promising tool for deposition of the storage media of ReRAMs as this technique provides reproducible and precise control over thickness, uniformity and stoichiometric of deposited materials[70][14].

Table 2.1 – A short list of studied materials for the storage media in ReRAMs, adopted from[58].

Dielectric layer	On/Off ratio	Operation Speed	Endurance
Binary Oxide			
MgO_x	$>10^5$	-	$>4*10^2$
AlO_x	$>10^6$	<10 ns;<10 ns	$>10^4$
TiO_x	$>10^5$	<5 ns;<5 ns	$>2*10^6$
MnO_x	$>10^4$	<100 ns;<200 ns	$>10^5$
NiO_x	$>10^6$	<10 ns;<20 ns	$>10^6$
GaO_x	$>10^2$	<400 ns;<600 ns	$>10^4$
GeO_x	$>10^9$	<20 ns;<20 ns	$>10^6$
HfO_x	$>10^5$	<300 ps;<300 ps	$>10^{10}$
GdO_x	$>5 * 10^5$	<1 ns;<1 ns	$>10^7$
Complicated and Ternary oxides			
$BaTiO_3$	$>10^4$	<10 ns;<10 ns	$>10^5$
PCMO	$>10^3$	<8 ns;<8 ns	$>10^10$
Chalcogenides			
Cu_2S	$>10^6$	<100 μs;< μs	$>10^5$
Ge_xSe_y	$>10^6$	<100 ns;<100 ns	$>10^{10}$
Nitrides			
AlN	$>10^3$	<10 ns;<10 ns	$>10^8$
SiN	$>10^7$	<100 ns;<100 ns	$>10^9$

3 Cross-Point Array

3.1 Introduction

Cross-point array architectures based on resistive switching elements, because of their ultimate scalability have been considered for the next generation non-volatile memory devices and re-configurable logic circuit[80]. A cross-point array consists of parallel interconnects (word and bit lines) perpendicular to each other at two different planes. The simple yet effective cross-point array architecture, allows an effective cell area being $4F^2$ in 2D design. The feasibility of achieving 3D configuration by stacking multiple 2D layers reduces the minimal feature size further to $4F^2/n$ and leads to very high integration density (>1Tb as it is required for high-density NVM applications)[4]. However, the sneak current through unwanted neighbor cells, significantly *decreases* the system efficiency, deteriorates the read margin, and limits the maximum size of a cross-point array[26].

3.2 Sneak Path Current Issue

Considering the line resistance, the IR voltage drop on the interconnecting lines are significant, it decreases the accessibility to the target cell, especially during the write operation where high currents are involved (higher IR drop). This leakage currents also raise the total power consumption. Now considering the needs for a bigger array, the array performance degradation is getting even worse due to the higher available paths for the leakage.
As it is demonstrated in the Figure 3.1, three different zones (R1, R2 and R3) will be defined in a cross-point system depending on the selected word line(WL) and Bit Line(BL).

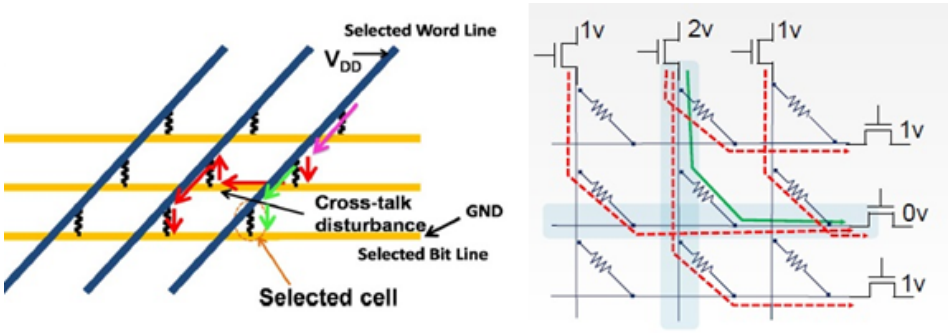

Figure 3.1 – a) Illustration of sneak current in a cross-point array with nearly linear RS during the read operation [23], b) circuit schematic of cross-point array[4]. Red dashed lines: sneak current, solid green line: actual readout signal.

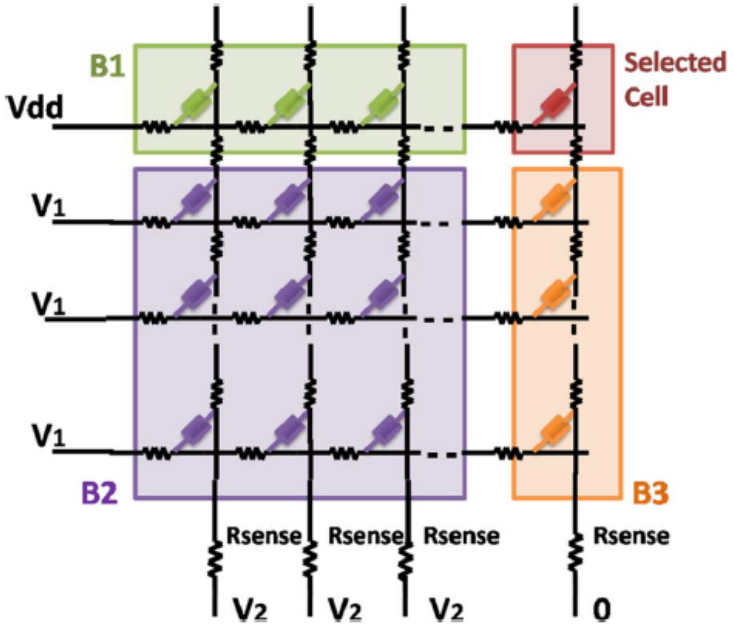

Figure 3.2 – Schematic of the cross-point array circuit. V1 and V2 represent the applied voltage on the un-selected word and bit lines[23]

To overcome the sneak path issue, a separate non-linear RS device could be connected with each resistive memory element in series.
An ideal non-linear element candidate to optimally operate with ReRAM should fulfill requirements such as high on-off ratio, scalability, switching speed, endurance compatibility with RS element, low variability and current density, these properties are summarized in 3.1. Several

Table 3.1 – A summary of required properties for selector device for suppression of the sneak path, adopted from [4]

Parameters	Required Value
ON current (I_ON)	>10 MA/cm^2
On/Off Ratio	>10^6
Processing Temperature	<400° C
Operation Temperature	85° C
Switching Speed	<50 ns
Operation Polarity	Compatible with memory element
Scalability	Compatible with memory element

device structures compatible with the cross-point array have been studied, such as: One-diode One-Resistor(1D1R), Complementary RS (CRS), One-MOSFET transistor One-Resistor (1T1R), One-Bipolar junction transistor One-Resistor (1BJT1R), and One-Bipolar selector and One-Bipolar resistor (1S1R); all structures are shown schematically in Figure3.3 and their properties are compared in the Table 3.2

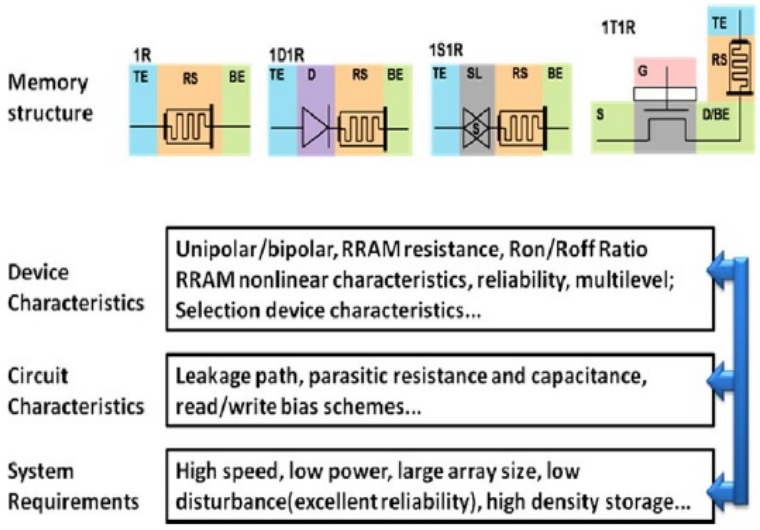

Figure 3.3 – Different cell structure, device and circuit characteristics and their impacts on system performance[23]

Table 3.2 – A comparison between different structural solution of the sneak-path issue, adopted from [33].

Device Structure	Cell Size	Destructive Read	Process Temperature
1T1R	>8 F^2	No	**High**
1BJT1R	4 F^2	No	**High**
CRS	4 F^2	**Yes**	Low
1D1R	4 F^2	No	**High**
1S1R	4 F^2	No	Low

3.3 One selector-One resistor (1S1R)

Serially connecting each memory element to an additional selection device in a 1S1R configuration is an effective way to introduce selectivity to the cross-point arrays. This method permits optimizing of every individual component separately to reach the device performance requirements. Therefore, it is believed that the 1S1R RRAM cross-point array is suitable for the potential storage class memory (SCM) applications.
When both selector and resistor elements are wired together and are biased, the resulted behavior of the system is different from of each single components.
Figure 3.5 schematically demonstrates a conventional 1S1R cross-point array with selector and resistor elements integrated between word and bit lines.

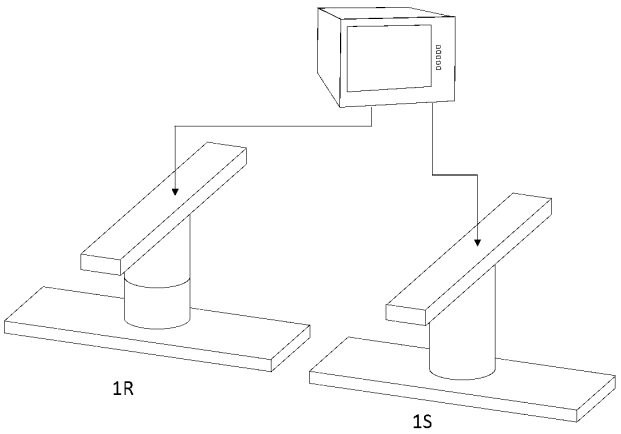

Figure 3.4 – Schematic demonstration of 1S1R on different substrate.

For the ultra-high density non-volatile memory applications (>1Tb), 3D-stackable structures are needed; therefore, more studies over the 1S1R structure are encouraged.

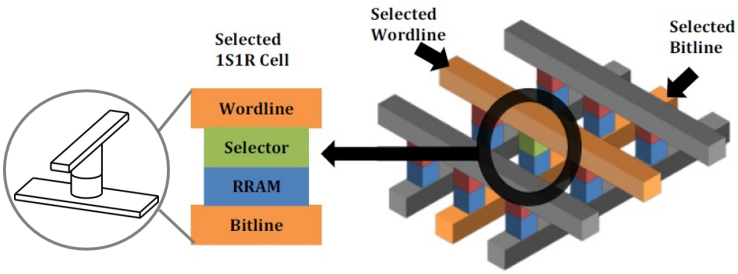

Figure 3.5 – Schematic demonstration of a 1S1R cross-point array[34].

4 Effect of Hf Metal Layer on the switching characteristics of HfO_x-based resistive Random Access Memory

Authors: ***Behnoush Attarimashalkoubeh*** [1], *Jury Sandrini* [1], *Elmira Shahrabi* [1], *Mario Barlas* [2], *Yusuf Leblebici* [1]

[1] Microelectronic Systems Laboratory, EPFL, Lausanne, Switzerland.
[2] Advanced Memory Group CEA-LETI Grenoble, France.

Authors contribution: B.A. Performed the research, including the fabrication process, electrical characterization, data analysis, and wrote the manuscript. J.S. has contributed to the development of the process flow and was involved in the fabrication steps. E.S. revised the manuscript. M.B. has helped in the development of a few steps of the fabrication process, and Y.L supervised the research and revised the manuscript.

Effect of Hf Metal Layer on the switching characteristics of HfO_x-based resistive Random Access Memory

Authors: *Behnoush Attarimashalkoubeh* [1], *Jury Sandrini* [1], *Elmira Shahrabi* [1], *Mario Barlas* [2], *Yusuf Leblebici* [1]

[1] Microelectronic Systems Laboratory, EPFL, Lausanne, Switzerland
[2] Advanced Memory Group CEA-LETI Grenoble, France

Abstract

In this study, we propose the insertion of an ultra-thin Hf layer at the interface between TiN (top electrode) and HfO_x (electrolyte), and the study of its effect on the device electrical properties. In order to obtain the desired switching characteristics, the Hf layer thickness must be precisely engineered. The device with optimized Hf layer thickness exhibits better uniformity and lower forming voltage. This improvement could be explained by the role of the Hf layer in the creation of permanent oxygen vacancies in the oxide layer, which facilitates the switching phenomena.
Keywords: Resistive Random Access Memory (ReRAM), Oxygen reservoir, Oxygen vacancy.

4.1 Introduction

The abundance of difficulties and hurdles in scaling down conventional memory devices necessitated developing alternative candidates, which provide high performance and reliability[32]. Memory technologies have undergone explosive growth from Static Random Access Memory (SRAM), Dynamic Random Access Memory (DRAM), NAND, and NOR to nano-scale non-volatile memory (NVM). Resistive Random Access Memory (RRAM) with its comparatively easy structure and fabricating method[7] recent resurgence of researches and seems to be a leading candidate to replace the conventional flash memory for the future computing system. RRAMs (identified as the fourth fundamental passive element in circuits[73]) are usually composed of an electrolyte layer sandwiched between two electrodes and are presenting an appropriate trade-off between expected specifications like density, scalability, low power, high endurance, random access and read/ write throughput[19][43]. In ITRS categorization, depending on the different physical mechanism, Oxide based RAMs (OxRAM) are included in the Redox memory category. OxRAMs working mechanism is based on formation/annihilation of conductive nano-filaments, composed by oxygen vacancies, by biasing the cell due to redox reaction[79]. In OxRAM, different oxides such as Hafnium Oxide (HfO_2), Aluminum Oxide (Al_2O_3), Tantalum Oxide (Ta_2O_5, Titanium Oxide (TiO_2) and their sub-oxides are considered as conventional

candidates for the electrolyte layer[6]. Among all, HfO_x based RRAMs show promising characteristic by a proper trade-off between operating speed, data retention, endurance, and switching window[55][40]. In the present work, we show the device properties before and after adopting a reactive metal interfacial layer (Hf) in TiN (TE)/HfO_x/Pt (BE) ReRAM devices. The devices were fabricated with a specific process flow to achieve precise control over the patterning of the vias.

4.2 Materials and Methods

4.2.1 Fabrication Process 3low

The “in-via” memory structure was patterned by effectively stacking the memory element(s) vertically between two metal lines as the scheme of the process flow shown in Figure4.1 and explained comprehensively below. All memories were fabricated on the top 4" Si test wafers pre-oxidized with 500 nm silicon oxide. In order to fabricate the bottom electrode (BE), 100 nm Pt was grown using D.C. sputtering (1000 W) after deposition of a thin layer of Ti to enhance the adhesion between sputtered Pt and the Si wafer. The BE was spin-coated with AZ3007 positive resist and shortly soft baked to reduce the solvent content and increase adhesion to the substrate. The resist is patterned by using an optical lithography tool (10 mW/cm^2) and developed afterward. The BE etched with STS ICP dry etch system (Ar/Cl_2) using laser end-point detection. Next, 100 nm thick LTO was grown by LPCVD at 425 °C as a passivation layer to act as the shaping matrix for the “in-via” memories. LTO was chosen regarding its relatively low deposition temperature, excellent insulation characteristic and simplicity of etching by BHF at room temperature. Next, the second level lithography process was performed with the same procedure described before. The lithography followed by BHF bath etching to remove the LTO in the selected area in order to achieve the via shape to deposit the switching elements afterward. A 5 nm layer of Hafnium oxide (the resistive oxide) deposited by mean of Atomic Layer Deposition (ALD) at 200 °C using TEMAH and H_2O as precursors. ALD tool was selected for the deposition of switching material due to its superior ability in controlling the thickness and uniformity of the thin films[70][83]. After the resistive layer deposition, the sample was removed from the reactor and introduced to the sputtering chamber to deposit a 50 nm TiN layer as Top Electrode (5E^{-3} mbar, 200 W). Next, in order to define the top electrode, we performed the third level photolithography (including resist coating, exposure, and developing) as it is described earlier for the previous photolithography steps. Etching of the top electrode was performed following the same protocol as the one described earlier. The resist was stripped away by utilizing Acetone, IPA, and DI water. The whole fabrication procedure with the dimensions information is demonstrated in the Figure4.2.

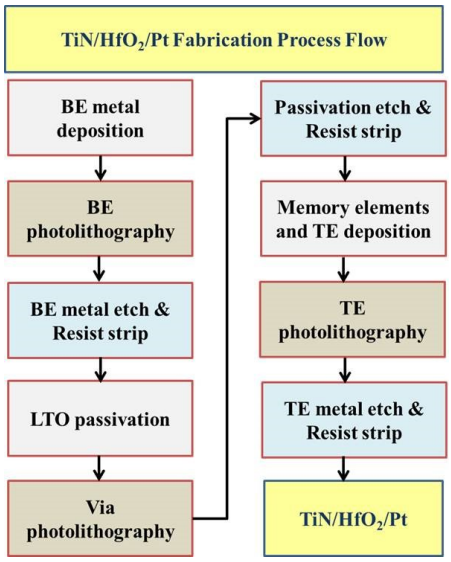

Figure 4.1 – Schematic demonstration of the process flow used for fabrication of HfO_x-based ReRAMs.

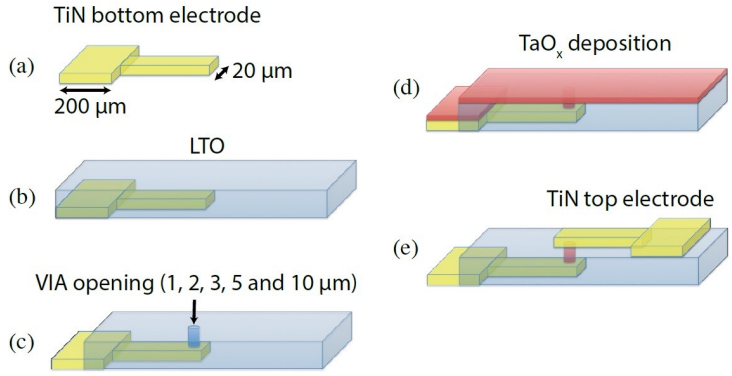

Figure 4.2 – A schematic demonstration of a single cell fabrication with its dimension.

4.2.2 Electrical Measurement

The electrical characterizations of the device were studied by using Agilent B1500 parameter analyzer. The bias was applied to the top electrode (TE), while the bottom electrode (BE) was grounded during measurement. To protect the device from hard breakdown, a compliance current of 150 μA was forced to the sample throughout the measurement steps.

4.3 Results and Discussion

When a positive increasing voltage is applied from 0 to 5 V on the top metal electrode, the current first gradually increases as its result. If the positive voltage applied on the top metal electrode is larger than a certain threshold voltage (V_{TH}), the resistance of the device is

suddenly reduced, the device is turned on, and the current reaches the compliance current. Besides, applying a negative voltage on the top metal electrode led the device to the high resistance level (off state). The electrical characteristic of the TiN (TE)/HfO_x (5 nm)/Pt (BE) device is shown in Figure4.3. The resulted typical bipolar resistive switching cycles (I-V characteristic) are shown in Figure4.3a. As it is demonstrated, the as-fabricated device showed high resistance and negligible current (around 5 nA) between the top and bottom electrode (plotted in red). The device demonstrated a sudden increase in the current value at 3.3 V (considered to be V_{TH}) and reached the compliance current. In Figure4.3a, the broad fluctuation of the key switching parameters is noticeable; the HRS and LRS level values are plotted more clearly in the Figure4.3b (read in 0.25 V).
The electrical characteristics of the TiN/HfO_x(5 nm)/Pt cell structure show that there are several issues to be solved in order to successfully achieve a high-density cell array. The forming voltage is relatively high ($V_{forming}$=3.3 V), in addition, the key switching parameters such as V_{set}, switching window(on/off ratio) and I_{Reset} demonstrate a wide variation during switching. Altogether, these characteristics can result in poor reliability, endurance, and retention. Without applying a high forming voltage or a high enough compliance current, the device in HRS could not completely convert to LRS, causing a reset failure. It is assumed to be due to the unsuccessful attempt in the formation of conductive filament under this situation[53]. Considering the urge to improve the switching variability, adding a layer of a reactive metal (e.g., Ti, Ta, Hf) to increase the oxygen vacancies in the switching layer have been proposed previously[54][42][38]. It is been already reported that the selected metal layer has an important influence on ReRAM performance. The best metal layer to optimize OxRAM is believed to be the metal electrode with the comparable oxygen affinity to the metal in the memory at the oxide interfaces[48]. The resistive switching properties of the device with a reactive layer can be precisely controlled by optimizing the reactive layer features[38].
In this work, in order to investigate the effect of the reactive metal layer on the key switching parameters, a reactive layer of Hf has been introduced between HfO_x and the TiN(TE). HfO_x has been selected as the most compatible electrode with HfO_x layer. Different HfO_x /Hf-based bi-layer OxRAM were fabricated to examine the resistive switching characteristics. The thin Hf layer was deposited using R.F. sputtering (5E-3 mbar, 500 W). Accordingly, different device structures with different Hf thicknesses have been fabricated.
Table 4.1 presents two of the fabricated devices with Hf layer with their structures and also the device without the Hf layer as the reference device. All three devices have been biased for 50 cycles as described earlier. Figure4.4 presents 20 typical cycles for each device (D1, D2, and D3) under 150 μA compliance current. The device with 3 nm Hf in TiN/HfO_x interface (D2) comparing to the device without Hf layer (D1) shows significantly lower forming voltage and, in general, better characteristics. It is believed that the 3 nm Hf leads to the formation of a thin interfacial layer in Hf/HfO_x interface, which generates the appropriate amount of oxygen vacancies in the HfO_x layer. In the D2 device, during the switching cycles, this interfacial layer serves as oxygen ions reservoir[17]. The generated oxygen vacancies facilitate the set process accordingly and lower switching parameters. The switching mechanism is demonstrated schematically in the Figure4.5. The device with 3 nm Hf in TiN/HfO_x interface

Table 4.1 – The fabricated devices and their structures. D1 representing a hfO_x-alone device, D2 and D3 the HfO_x-based devices with Hf=5 and 3 nm, accordingly.

ID	Device Structure
D1	TiN/HfO_x-5 nm/Pt(BE)
D2	TiN(TE)/Hf-3 nm/HfO_x-5 nm/Pt(BE)
D3	TiN(TE)/Hf-5 nm/HfO_x-3 nm/ Pt(BE)

(D2) comparing to the device without Hf layer (D1) shows significantly lower forming voltage (accordingly: 2.45 V and 3.30 V), V_{set} and V_{reset}, and the switching window (on/off ratio) is improved. The 3 nm thickness seems to be optimized thickness for Hf, the device with 1.5 nm Hf (not shown in this work) did not demonstrate any improvement compared to D1. It is assumed that a 1.5 nm Hf layer is not thick enough to forms a uniform layer and probably just is deposited in the island shape in the interface. The device with 5 nm Hf (D3), as demonstrated in Figure4.4, shows higher on/off ratio but also large overshoot has been observed in every reset cycles. A comparison between all the characteristics of D2 (Hf=3 nm) with the other examined devices with different Hf thickness (Hf=1.5 and 5 nm), D2 is proved to be the best candidate by its enhanced switching parameters, and 3 nm seems to be the optimized thickness for Hf reactive layer.

4.4 Conclusion

In this work, we demonstrated the fabrication and electrical characteristic of a HfO_x based bi-layer OxRAM. A thin layer of Hf was inserted between TE and the switching oxide to enhance the switching reliability and uniformity. The reactive Hf layer acts as an oxygen reservoir and creates permanent oxygen vacancies inside the oxide, which has a significant role in lowering forming voltage and switching properties of the device. For the device with TiN(TE)/HfO_{x-5} nm/Pt(BE) structure, it is shown 3 nm is the optimized thickness for Hf layer which could result in a proper trade-off between forming voltage and the switching properties.

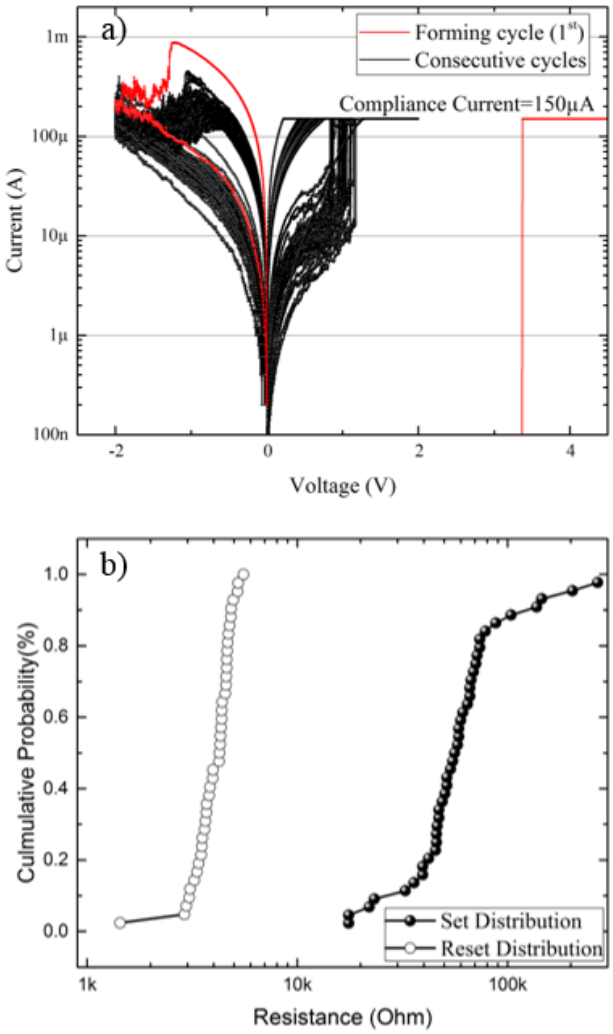

Figure 4.3 – I-V characteristic for Device 1, b) the HRS and LRS distribution.

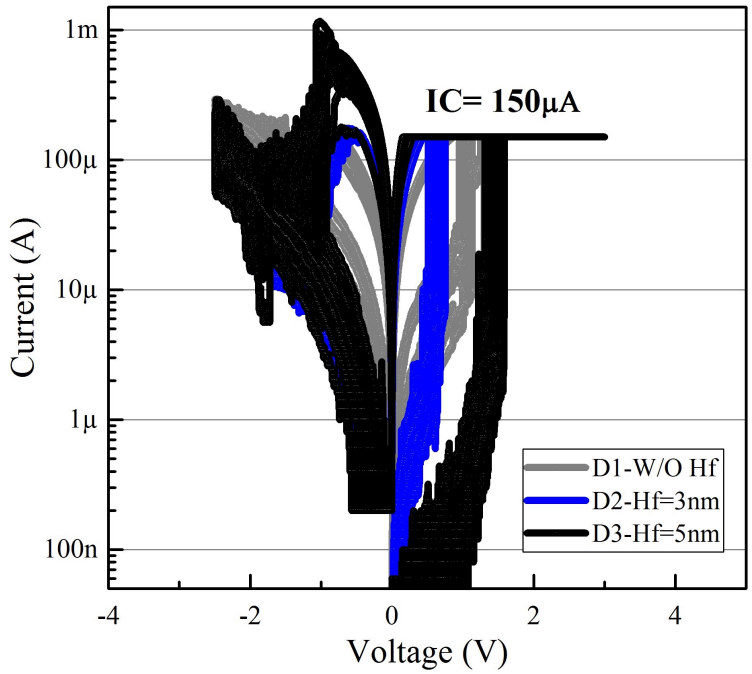

Figure 4.4 – I-V characteristics the devices D1, D2, and D3 after their forming cycles

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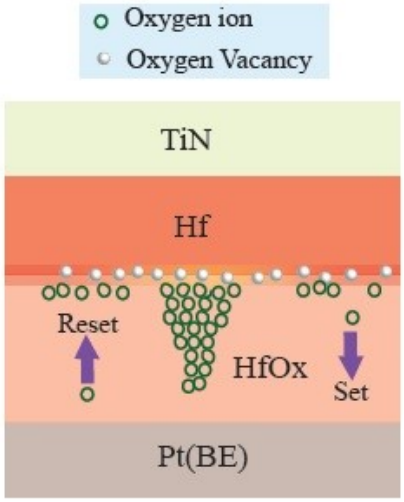

Figure 4.5 – Schematic switching mechanism demonstrating the role of Hf as reactive metal in creation of oxygen vacancies.

5 Effect of metal buffer layer and thermal annealing on HfO_x-based ReRAMs

Authors: *Jury Sandrini,* ***Behnoush Attarimashalkoubeh****, Elmira Shahrabi, Igor Krawczuk, and Yusuf Leblebici* [1]

Swiss Federal Institute of Technology (EPFL)
Lausanne, Switzerland

Authors contribution: B.A. was involved in the fabrication of devices, electrical characterization, and revised the manuscript.

Effect of metal buffer layer and thermal annealing on HfO_x-based ReRAMs

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Swiss Federal Institute of Technology (EPFL)
Lausanne, Switzerland

Abstract

In this paper, we investigate different methods and approaches in order to improve the electrical characteristics of Pt/HfO_x/TiN ReRAM devices. We discuss the improvement of the ReRAM electrical characteristics after the insertion of a Hf, and Ti buffer layer. As a result, the resistance window increases more than 10 times, and the set and reset voltages decrease both in absolute value and variability. Furthermore, we show the influence of an annealing step at different temperatures on the Pt/HfO_x/Hf/TiN memory devices on forming voltage and HRS. Considering the importance of achieving high-density memory, we demonstrated the possibility of multi-level resistance state in the fabricated devices by controlling the enforced compliance current. In addition, we show the endurance characteristic of the fabricated memories and their error rate. Finally, we report the transient behavior of the memory devices, investigating the device speed and switching mechanism.

5.1 Introduction

Resistive Random Access Memories (ReRAMs) are a class of emerging non-volatile memory devices that store the data information based on the difference between defined resistance states[87]. The interest in these emerging technologies is driven by the challenges that mainstream memories are facing for highly scaled technological nodes, such as the degradation of performance, reliability, and noise margin. In this context, ReRAMs are extremely attractive due to simple structure, low programming voltage[15], fast writing speed [74], high endurance[36] and high scalability[45]. Those characteristics make ReRAM a potential candidate to revolutionize the present memory hierarchy, creating a new memory class, also referred as storage class memory, in between the main memory and the SSDs.
ReRAM can be categorized based on their switching characteristics into two main groups: unipolar and bipolar. In this work, we discuss about bipolar oxide ReRAMs. These devices are generally composed by a dielectric layer in between a Bottom Electrode (B.E.) and a Top Electrode (T.E.). The resistance of the dielectric layer can be switched between a High Resistance State (HRS) and a Low Resistance State (LRS) by applying a positive or negative voltage on the T.E. The transition between the LRS to the HRS is the set operation, while the

opposite one is referred as the reset operation. The memory working mechanism relies on the generation or rupture of a conductive filament composed of oxygen vacancies due to the applied electric field and the thermal effects resulting from the device current. The material used as the dielectric layer is usually a metal oxide, such as TaO_x, TiO_x, AlO_x, and HfO_x. In this work, we study the influence of the device structure and Post Metallization Annealing (PMA) on the electrical characteristics of HfO_x-based ReRAM devices. We show furthermore that by the precise modulation of the test conditions, it is possible to achieve multiple intermediate resistance states, allowing to store multiple bits per device. We also report the cell transient behavior, that can give insights into the cell switching mechanisms.
This work differs from other works as it presents, with the same test structures and within the same testing conditions, the engineering of key fabrication parameters and their effect on the ReRAM electrical behavior. Furthermore, compared to[12] and[67], this study shows the impact of a PMA annealing on the final cell structure at relatively low temperatures, which main effect is the controlled oxidation of the metal buffer layer. The optimization of the fabrication parameters allowed to obtain a ratio between HRS and LRS of more than a decade over more than $8{\times}10^3$ cycles at low write voltage (-2.25 V and 1.15 V). The transient cell switching speed was faster than 400 ns and 7μs for the set and reset operation, respectively. The remainder of the paper is organized as follows. In Section 5.2, the fabrication process for the ReRAM devices is described. In Section 5.3, we present the influence of two important optimizations of ReRAM fabrication. We show the effects of memory stack engineering and post metallization annealing on the device electrical characteristics. In Section 5.4, a more exhaustive characterization of the fabricated devices is presented. We show the device endurance, the possibility to achieve multiple resistance states by modulating the test conditions, and the ReRAM transient behavior. Finally, the conclusion of the paper is given in Section 5.5.

5.2 ReRAM Fabrication Process

The reference memory cell used for this work is a Pt/HfO_x/TiN ReRAM. This device will be used to compare the effects of the device adjustments described in the following section. The device fabrication process flow is summarized in Fig. 5.1(a). First the 50 nm Pt B.E. is deposited by room temperature sputtering on a thermally passivated Si wafer. The Pt film is patterned by optical lithography and a subsequent Ar/Cl_2-based Reactive Ion Etching (RIE). Then, the wafer is passivated by a *Low Temperature Oxide* (LTO) film deposited by *Plasma Enhanced Chemical Vapor Deposition* (PECVD) with SiH_4 and O_2 precursors at 425° C. Next, a lithography and a Buffered Oxide Etch (BHF) wet etching define the area for memory cells by selectively removing the passivation. The ReRAM devices are confined by an oxide VIA opening with a diameter that range from 800 nm to 10 μm. Afterward, a 5 nm-thick HfO_2 layer as switching material is deposited by *Atomic Layer Deposition* (ALD) at 200 ° C from TEMAH and H_2O. Then, a 50 nm thick TiN layer is deposited by room temperature sputtering. Finally, last lithography and a Ar/Cl_2/BCl_3-based RIE defines the top electrode. The final devices are shown in Fig. 5.1(b). The Pt/HfO_x (5 nm)/TiN memories are accessed by metal pads used for

the electrical characterization.

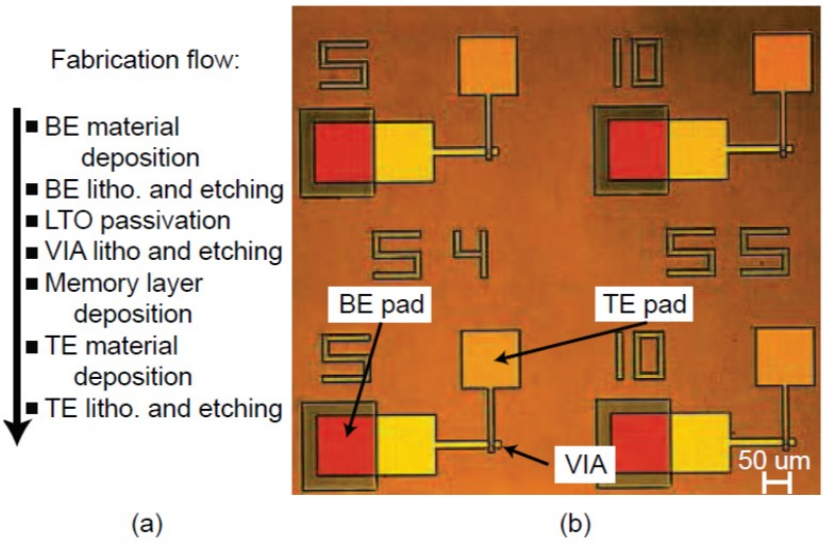


Figure 5.1 – (a) Schematization of the ReRAM fabrication process flow and (b) device micrograph. The device diameters range from 800 nm to 10 μm.

5.3 Fabrication Process Optimization

The process flow described in Section 5.2 was modified to study the effect the memory stack composition and the annealing the full memory device stack. The two following subsections describe the effects of these process modifications on the ReRAM electrical characteristics.

5.3.1 Metal Buffer Effect

As a first step in engineering the device performance, the memory stack was modified by studying the addition of two different metal layers. We utilized a D.C. sputtering tool in order to insert a 3 nm thin layer of Hf or Ti between HfO_x (switching material) and TiN (TE), obtaining Pt/HfO_x/Hf/TiN and Pt/HfO_x/Ti/TiN devices. Figure 5.2 show the differences in the electrical characteristics between Pt/HfO_x/TiN and the devices with the metal buffer layer (Pt/HfO_x/Ti/TiN and Pt/HfO_x/Hf/TiN). In the image, we reported only the most representative cycles to clarify the representation. The analysis is based on the statistics over 100 memory operations, and the variation of the measured quantities are reported in the following text in square bracket notation. If we compare the devices with the Hf layer to the reference, we observed a significant drop in forming voltage from 3.5 V (in the device without Hf layer) to 2.5 V. Moreover, the LRS decreases from 5 kΩ to 2 kΩ, and this drift, together with the increase in HRS value from 20 kΩ to [0.1 MΩ, 1 MΩ], led to noticeable enhance in switching window for more than 10 times. After insertion of the Hf layer, we observe a reduction of both the set

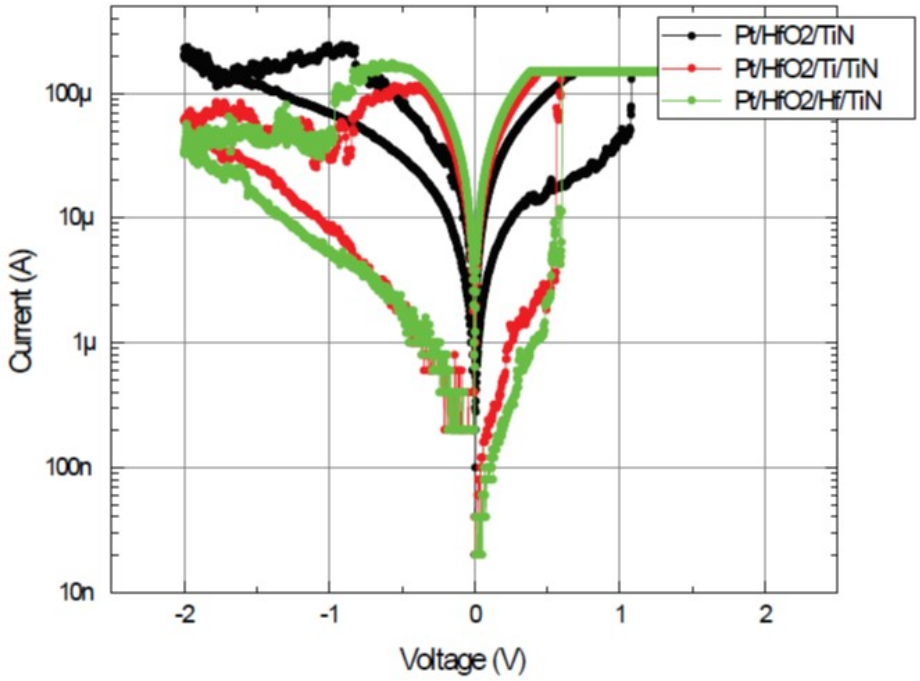


Figure 5.2 – Influence of different metal buffer layers on the ReRAM electrical characteristics. The figure shows the test result for Pt/HfO_x/TiN, Pt/HfO_x/Ti/TiN and Pt/HfO_x/Hf/TiN devices.

and reset voltages as well. The set voltage dropped from [0.75 V, 1.2 V] to [0.3 V, 0.9 V], the reset voltage decreased, in absolute value, from [0.6 V, 1 V] to [0.4 V, 0.65 V].
In case of Ti as the buffer layer, the results are comparable to the Hf ones. We obtained a forming voltage of 3 V, with a LRS of 3 kΩ and a HRS of [90 kΩ, 2 MΩ]. The set and reset voltages are [0.5 V, 0.9 V] and [0.45 V, 0.7 V], respectively.
This increase of performance can be explained by the oxygen scavenging action of the metal buffer layer. The metal layer (in this case Hf or Ti) reacts with HfO_x by partially depleting it from oxygen. This lowers the number of new vacancies that need to be created to reach the critical defect density to form a conductive path. Therefore, the electric field needed during the forming operation decreases, which results in a lower forming voltage. As a consequence, the cells suffer from a lower current overshoot, which allows a better control of the HRS and the improvement of the other electrical characteristics.
The main difference between the Hf and Ti devices is the forming voltage. Because the HfO_x/Hf/TiN one is lower, we chose to use the devices with the Hf layer to investigate the stack annealing effects and for the electrical characterization presented in Section IV.

5.3.2 Post Metallization

We studied the influence of thermal treatment on the electrical characteristics of the device with the Hf layer using a *Rapid Thermal Processing* (RTP) machine. The annealing temperature

ranged from 200° C to 400° C, and the annealed devices were tested under the same conditions used earlier. The comparison between the I-V curve of the HfO_x/Hf/TiN annealed devices is shown in Fig. 5.3. By increasing the annealing temperature, the forming voltage first drops from 2.5 V to 1.85 V, then, for high-temperature treatments, it raises again to 3.5 V. The LRS value remains quite constant, while the HRS value is degraded more and more for high temperature treatments. This trend is explained by the formation of permanent vacancies in the film due to the thermally activated oxidation of the Hf buffer layer. The set and reset voltages remains quite constant, except for high-temperature treatments, which requires a higher voltage in order to build up a field high enough to trigger the resistance switch.

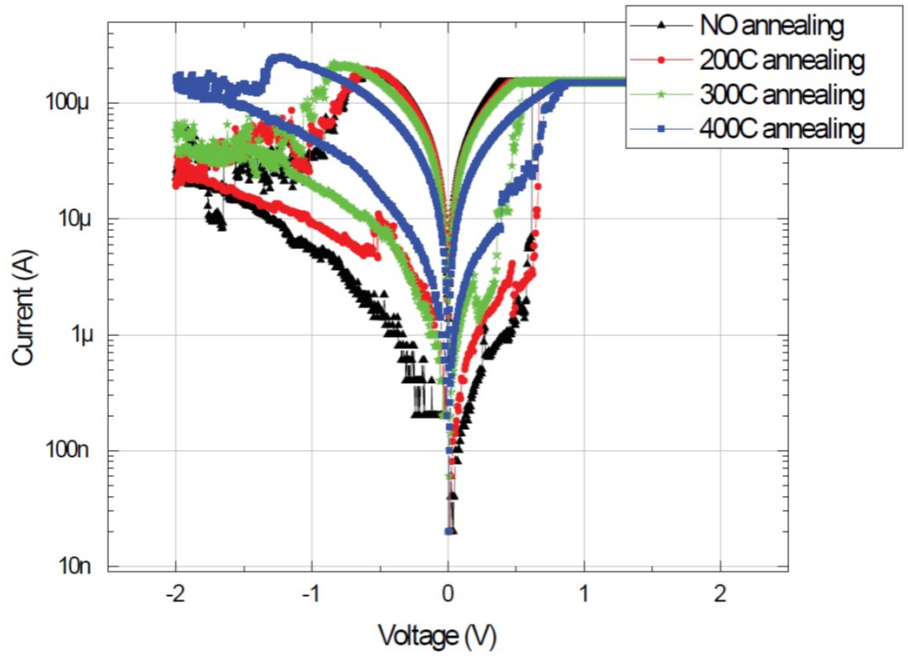


Figure 5.3 – Effects of thermal annealing at 200° C, 300° C and 400° C on Pt/HfO_x/Hf/TiN ReRAMs.

5.4 Device Characterization

We showed the possibility to obtain multiple resistance stated by modulating the set current compliance for Pt/HfO_x/Hf/TiN devices (Fig. 5.4). We obtained four different LRS states by setting the current at 18 μA, 52 μA, 97 μA and 180 μA. The obtained LRS states corresponding to the previously mentioned compliance currents are 11 Ω, 7.2 Ω, 5.3Ω and 2 Ω. The LRS decreases for higher compliance currents because it is proportional to the physical dimension of the conductive filament. After a critical vacancy density is created as a result of the applied voltage, the current flowing through the device generates enough heat to accelerate the vacancy creation, enlarging the plug cross section. This positive feedback needs to be controlled by a current compliance that, as a matter of facts, defines the plug dimensions, and thus its resistance.

On the same devices (Pt/HfO_x/Hf/TiN), we performed an endurance analysis to access the

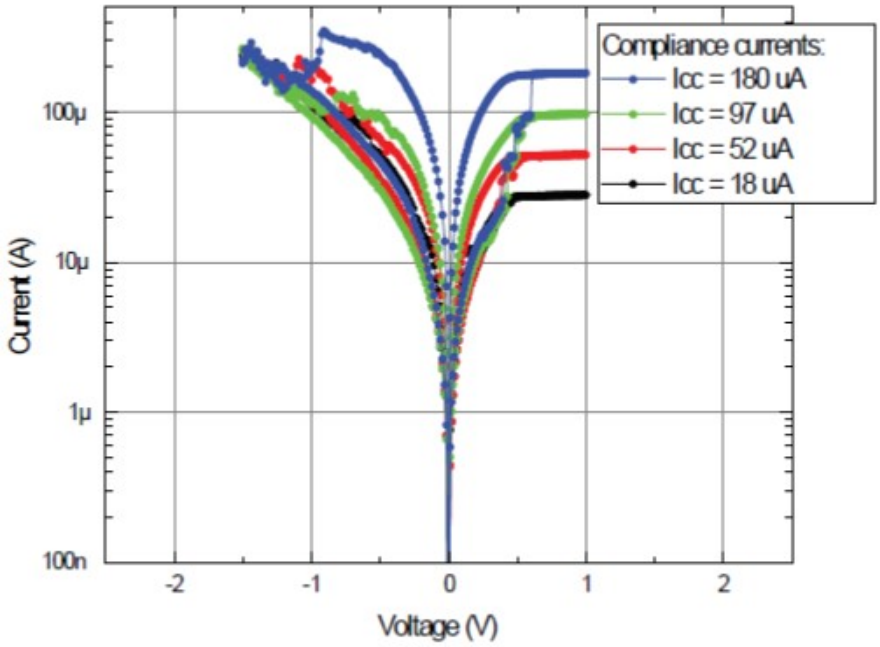


Figure 5.4 – Different LRS stated obtained by modulating the current compliance for the HfO_x/Hf/TiN devices at 18 μA, 52 μA, 97 μA and 180 μA.

stability and the reproducibility of the resistance states. The devices showed almost no failure for more then $8{\times}10^3$ cycles, as shown in Fig. 5. The results were obtained by applying 1 ms voltage pulses to the memory cells at -2.25 V and 1.15 V for the reset and set operation, respectively. The pulse rising and falling time were 200 μs, while the set current compliance was limited to 210 μA by a series transistor. The LRS has an average value of 4 kΩ, while the HRS was 50 kΩ. The test performed without any error correction strategy or read and verity scheme, showed an error rate below 1%. It worth noticing that the resistance values are different from the ones obtained from the D.C. tests for the same devices. This is due to the different setup used for the pulse measurement: in order to observe the transitory current flowing through the ReRAM, we added a resistor in series to the device. The drawback of this method is the difficult control of the actual voltage that operates the device. This affects predominantly the reset phenomena, because the ReRAM starts from a LRS. An important amount of the applied reset pulse voltage drops on the resistor, lowering the effective memory applied voltage on the memory device and lowering the resulting HRS.
Finally we investigated the current transient behavior of the cell during the pulse analysis. Fig. 5.6a and Fig. 5.6b show the device transient current for the set and reset transition, respectively. The current was obtained from the voltage drop across a 1 kΩ resistor placed in series with the fabricated ReRAM device. This analysis allows to investigate the switching speed of the device and the variability of the cell behavior in between the cycles. The data showed a switching speed for the set transition of 400 ns, and a 10 μs reset transition. From the image it is possible to notice the actual set voltage (0.8 V), reset voltage (0.9 V), and the current behavior during

the reset.

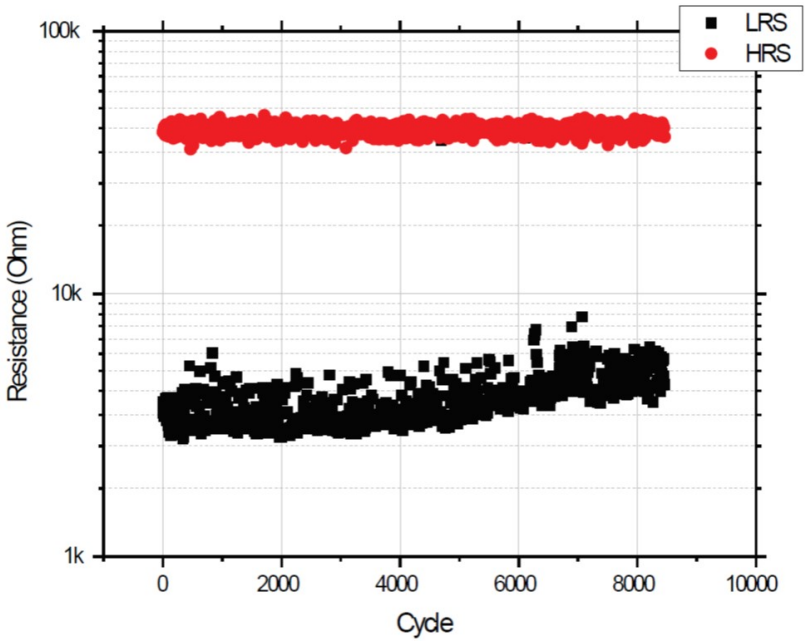
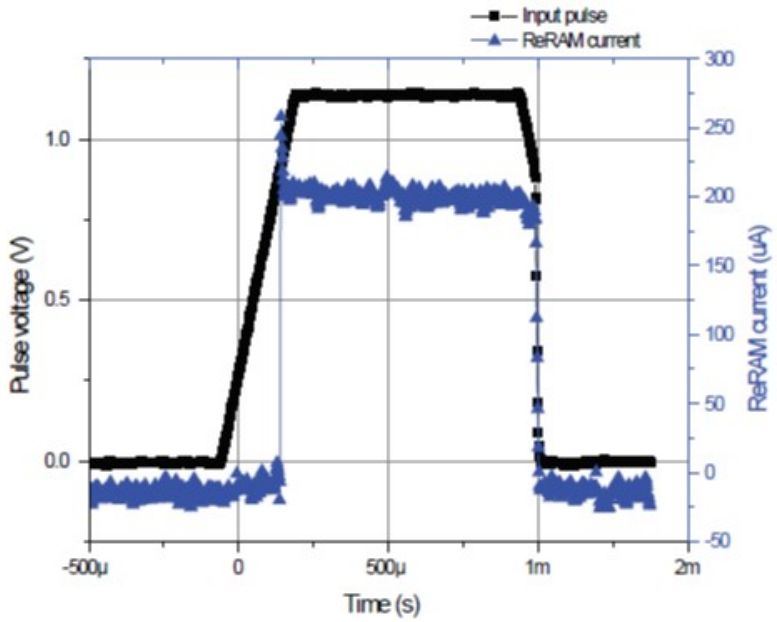


Figure 5.5 – Electrical behavior Pt/HfO_x/Hf/TiN devices. The input voltage pulses are at 2.25 V and 1.15 V with a length of 1 ms. The set current is limited to 210 μA.



(a) Set operation.

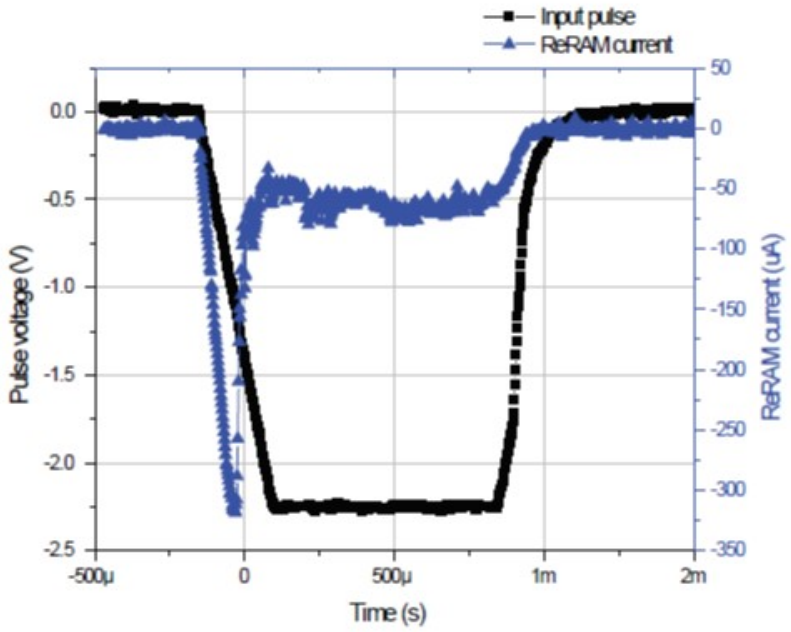


Figure 5.6 – Current transient behavior for Pt/HfO_x/Hf/TiN ReRAM devices. The current is measured from the voltage drop of a series 1 kΩ resistor. The device set and reset time are 400 ns and a 10 μs, respectively. The test conditions are the same as the one used for the voltage pulse test (2.25V and 1.15V, 1ms, 210 μA).

5.5 Conclusion

In this paper, at first we explained the fabrication of Pt/HfO_x/TiN) device as a reference sample, then we investigated different methods and approaches in order to improve its electrical characteristics. After, we discussed the improvement of the ReRAM electrical characteristics after the insertion of a Hf and Ti buffer layer. Furthermore, we showed the influence of an annealing step at different temperatures on the Pt/HfO_x/Hf/TiN memory devices. Considering the importance of achieving high-density memory, we conducted a series of electrical characterization by simply controlling the enforced compliance current during measurement to study the possibility of multi-level resistance state in the fabricated devices. In addition, we demonstrated the endurance characteristic of the fabricated memories and their error rate. Finally, we showed the transient behavior of the memory devices, investigating the device speed and variability.

Acknowledgment

The authors would like to thank the CMI staff of EPFL for the help with the fabrication together with Marios Barlas and Dr. Michail Zervas for the useful discussions for the fabrication processes. This work has been supported by Samsung Electronics.

6 Evolution of oxygen vacancies under electrical characterization for HfO_x-based ReRAMs

Authors: ***Behnoush Attarimashalkoubeh***, Jury Sandrini, Elmira Sharabi, and Yusuf Leblebici*

Microelectronic Systems Laboratory, EPFL, Lausanne, Switzerland.

Authors contribution: B.A conceived the research, developed the fabrication process, produced the samples, performed the electrical characterization, analyzed the data, and wrote the manuscript. J.S was involved in the development of the process flow and revised the manuscript. E.S revised the manuscript. Y.L supervised the research and revised the manuscript.

Evolution of oxygen vacancies under electrical characterization for HfO_x-based ReRAMs

Authors: *Behnoush Attarimashalkoubeh*, Jury Sandrini, Elmira Sharabi, and Yusuf Leblebici*

section*Abstract Recently, studies on ReRAMs and their reliability have received increased attention. The reliability issue is due to the nature of oxygen vacancies behavior under biasing conditions, which necessitate further studies to achieve an in-depth understanding of them. In this work, we fabricated several HfO_x ReRAM devices with different structure, material, and thickness, followed by a study of their electrical characteristics under DC bias. We show an improvement in the switching parameters through the engineering of the device structure. Moreover, we demonstrate a certain required thickness for the oxide layer for the ease of oxygen vacancies relocations, the thinner oxide layer led to the common ReRAMs performance failure in the low resistance state.

6.1 Introduction

Memory technologies have significantly changed from Static Random Access Memory (SRAM) to relatively recent nanoscale Non-Volatile (NVM) devices. The need for developing alternative candidates to replace conventional charge-based memories for future computing system has brought noticeable attention to Resistive Random Access Memory (ReRAM) with its comparatively easy fabrication methods and structure[7]. The simple ReRAM structure consists of a metal-oxide layer sandwiched between two electrodes and exhibits appropriate trade-off between the most important memory specifications such as density, scalability, high endurance, low power, random access and read/ write throughput[19],[43].
According to ITRS, Oxide based RAMs (OxRAM) are considered as one of the major categories of ReRAM which operate based on the formation and annihilation of conductive paths composed of oxygen vacancies through their oxide layer [4]. In OxRAMs the resistance states could drift from high resistance state (HRS) to low resistance state (LRS) during a process called set and from LRS to HRS during reset process. For OxRAMs, different metal oxides (i.e., Hafnium oxide, Aluminum oxide, Tantalum oxide, Titanium oxide, etc.) , and electrodes (Hafnium, Tantalum, etc.) have been studies as conventional materials[79].
Besides all highlighted advantageous of OxRAM, the reliability is thought to be the main hurdle on its way to replace conventional technologies[53]. The reliability issue is due to the nature of the switching mechanism that is based on the random formation of conductive filaments -with different shapes and sizes- through insulator layer which necessitates further studies to improve it. Solving the reliability issue is possible through a better understanding of ReRAMs switching mechanism. For OxRAMs, it involves in-depth knowledge about oxygen vacancies as the responsible elements for the resistive switching.
In this study, we fabricated different HfO_x-based memory devices and studied their character-

istics under DC measurement condition. The HfO_x as the oxide material was chosen due to its reported proper trade-off endurance and switching window[55].
Several devices with different structure have been fabricated, and their electrical characterizations have been studied.

6.2 Materials and Methods

6.2.1 Fabrication Process Flow

The "in-via" design is implemented to create the memory element(s) stack vertically between the two metal electrodes; Figure 6.1 schematically demonstrates the information of patterning steps for the fabrication process including the size and shape of the electrodes while the details of fabrication are been thoroughly explained in following. After deposition of a thin layer of Ti on top of 4-inch conventional test wafers with 500 nm silicon oxide, 100 nm Pt metal was grown using DC sputtering (1000 W). The wafers are spin-coated with the positive resist of AZ3007, soft baked to reduce the solvent content and increase its adhesion to the substrate, exposed by using an optical lithography tool (20 mW/Cm^2) and finally developed.
The bottom electrode (BE) etched with STS-ICP dry etch system (Ar/Cl_2 chemistry) using laser end-point detection for optimizing the process time. Next, 100 nm LTO was grown by LPCVD at 427° C as a passivation layer separating the electrodes, and in order to achieve the in-via shape.
The second level photolithography process was performed as has been described earlier, followed by BHF bath etch to remove LTO inside the vias for the further deposition of memory element materials.
Varied thicknesses of memory elements were deposited for different devices, the HfO_x layer

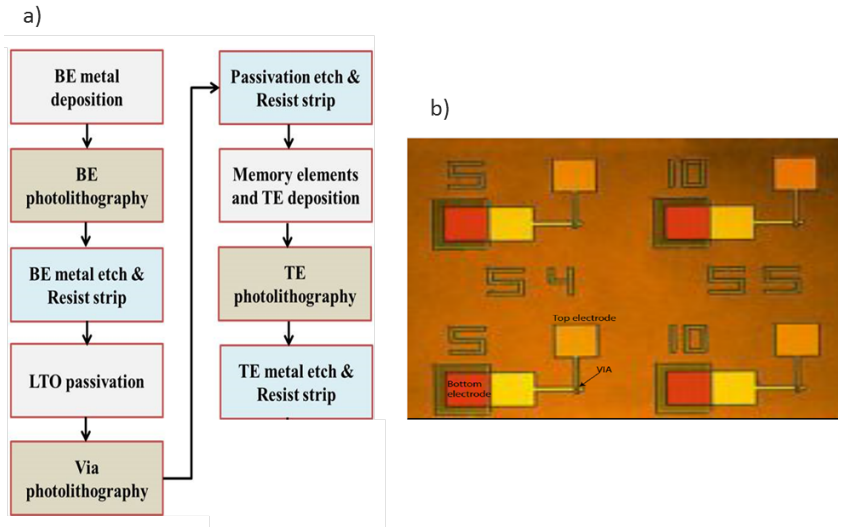


Figure 6.1 – a)Schamatic summary of the process flow steps, b) Optical picture of the ReRAMs cells before measurement, demonstrating the TEs, BEs and the vias.

for all samples were deposited by ALD (200° C using TEMAH precursors), TiO_2, Ti and Pt layers were deposited by DC sputtering using TiO_2, Ti and Pt targets at the room temperature. A thick layer of noble Pt metal has been utilized as the capping layer to prevent further oxidation of switching materials after deposition and to protect the electrodes in contact with the probe tips during the measurement. Next, the top electrode (TE) after resist coating, exposure, and development was defined, and the resist stripped away through the conventional procedure. Figure6.2a shows a schematic demonstration of the fabrication process flow and optical picture exhibiting access pads for further electrical measurement.
Several devices were fabricated with different structure as are listed in Table6.1

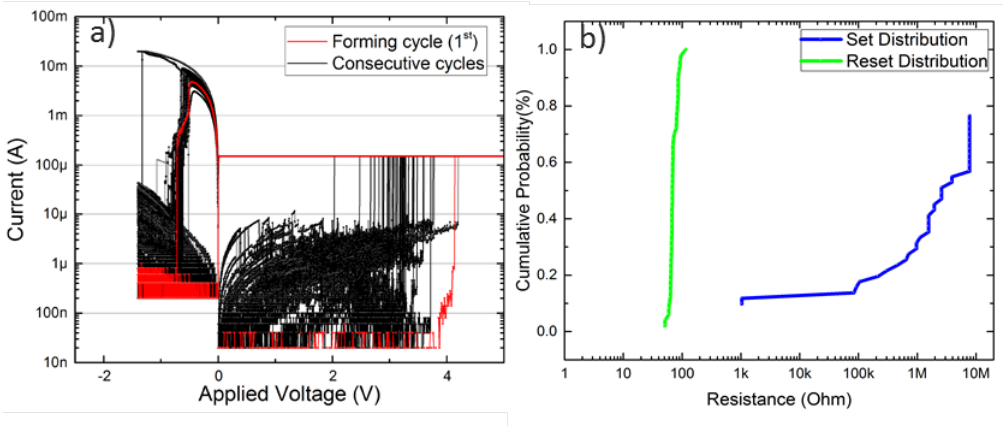


Figure 6.2 – Device No.1 with Pt(BE)/ HfO_2(5 nm)/ Pt(TE) structure: a) I-V characteristic for first 100 cycles, b)Set and reset distribution.

Table 6.1 – A summary of the fabricated devices with their stack structures

Device No.	Device Stack
1	Pt(BE)/**HfO_2(5 nm)**/ Pt(TE)
2	Pt(BE)/ **HfO_2(5 nm)**/ TiO_2(3 nm)/ Pt(TE)
3	Pt(BE)/ **HfO_2(5 nm)**/ TiO_2(5 nm)/ Pt(TE)
4	Pt(BE)/ TiO_2(3 nm)/ **HfO_2(5 nm)**/ Pt(TE)
5	Pt(BE)/ **HfO_2(5 nm)**/ TiO_2(3 nm)/Ti(5 nm)/ Pt(TE)
6	Pt(BE)/ **HfO_2(5 nm)**/ TiO_2(5 nm)/Ti(5 nm)/ Pt(TE)

6.2.2 Electrical Setup and Measurement

The electrical characteristics of the devices were studied by using Agilent B1500 parameter analyzer. The bias was applied to the top electrodes (TE) while the bottom electrodes (BE) kept were grounded during the measurement. To protect the devices from hard breakdown, a compliance current of 150 μA was forced to the samples during measurement.
All devices have been measured under the same electrical conditions; when the first bias swept on the TE from 0 to 7 V, the current in all the devices appeared to be few A and gradually

increased as the voltage increased, at a specific voltage (V_{TH}), the resistance level of the devices was suddenly reduced, the current reached the compliance currents value and the device reached to its low resistance state (LRS-on state). In addition, applying a negative voltage on the top metal electrode gradually led the devices to the high resistance state (HRS-off state).

6.3 Results and Discussions

For the device No.1 with HfO_2=5 nm, when first the fresh device cell is biased by positive sweeps from 0 to 7 V, the V_{TH} appears to be 4.1 V, and the device switched back to high resistance state (HRS) simply by negative bias (Fig.6.2a). The first cycle (plotted in red and called forming cycle) as expected shows to have a higher value (~ 4.1 V) comparing to the next cycles (1-2 V).
For the device No.1, the wide variations in the switching parameters were observed during the next 100 cycles (Fig.6.2b), which is related to the random nature of formation of filament inside the insulator layer. To overcome the variation in the switching parameters, the devices No.2 and 3 with the extra layer of TiO_x have been fabricated to suppress random formation of the filament, as a result, they both performed with the lower variation in the switching parameters but gradually their switching window degraded. Next, device No.4 with a different order of oxide layer (TiO_2/HfO_2 rather than HfO_2/TiO_2) fabricated and measured, the device shows to have high forming voltage (~ 8 V),a large overshoot (~ 15 mA) and within next few cycles the device failed in the LRS.
Device No.4 performance is attributed to the difference in the oxide quality deposited by different tools (sputtering and ALD system), higher forming voltage is needed to form the first step of the filament in the high-quality HfO_2 and the device failed quickly regarding the defective and leaky oxide as the switching material.
In the previously reported studies[54],[42],[38], the addition of an extra metal layer has been proven to have a significant effect in lowering variation in the key switching materials, hence devices No.5 and 6 with a thin layer of Ti (as the most compatible metal with the layer underneath has been recommended[48]) were fabricated and their electrical characteristics have been studied as their I-V characteristics for the first 100 cycles are shown in Figures 6.3 and 6.4.

Comparing two devices with 3 nm and 5 nm TiO_2 layer, the device with thicker TiO_2 (device No.6) as expected shows higher forming voltage, followed with a significant overshoot in the reset as its consequences Fig.6.4). Moreover the device No.5 has a smaller switching window (on/off ratio) which is a result of oxygen vacancies accumulation in the thin layer of TiO_2. Figure 6.5 schematically explains the difference between the switching mechanisms of device No.1, No.5 and 6. Device No.1, as explained before, has a wide variation in switching mechanism due to the uncontrolled formation of filaments with different shape and size (Fig.6.5a), while in the devices No.5 and 6, this issue has effectively improved by utilizing bi-oxide structure with an added extra layer of reactive metal Ti. During fabrication of the devices No.5 and 6, the reactive metal of Ti scavenged oxygen ions from the oxide layer below

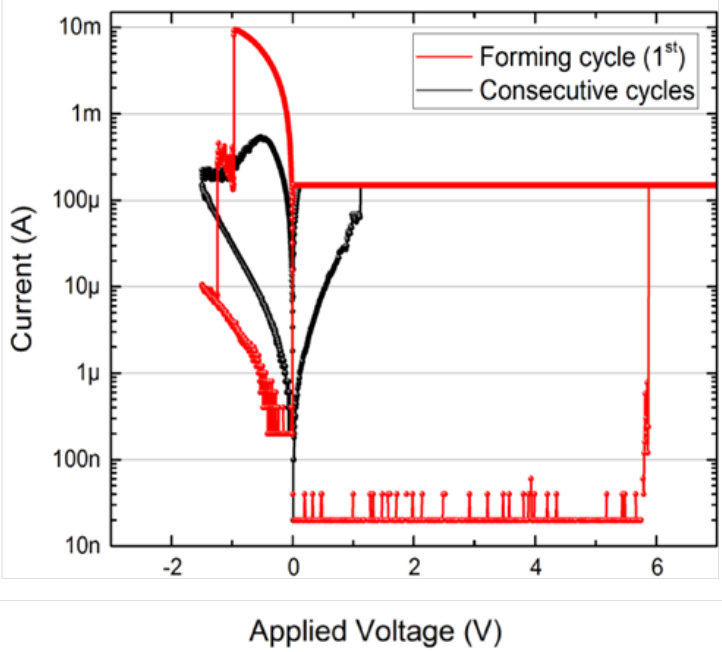


Figure 6.3 – I-V characteristic for the first 100 cycles of the device No.5 with Pt(BE)/ HfO_2(5 nm)/TiO_2(3 nm)/Ti(5 nm)/Pt(TE) structure.

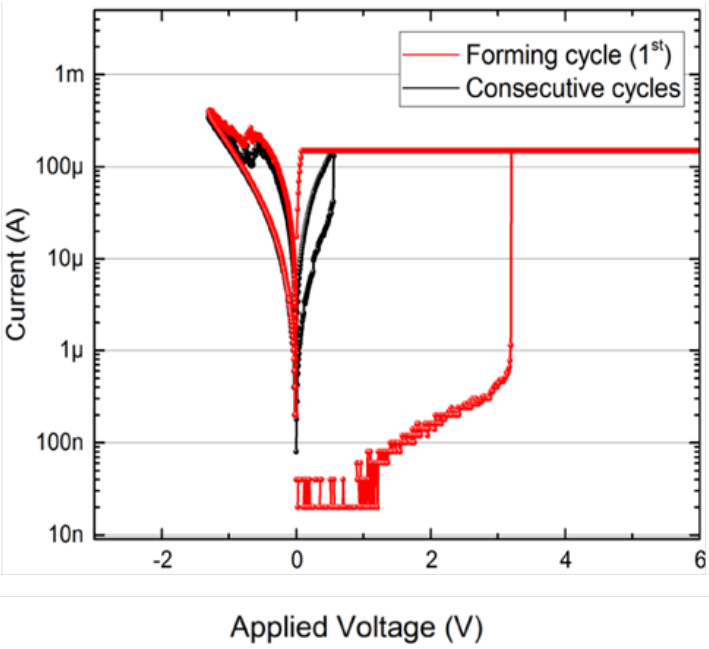


Figure 6.4 – I-V characteristic for the first 100 cycles of the device No.6 with Pt(BE)/ HfO_2(5 nm)/TiO_2(5 nm)/Ti(5 nm)/Pt(TE) structure.

and left permanent oxygen vacancies inside the oxide underneath, during the forming process more oxygen vacancies are created and bridged between TE and BE and caused the drift between HRS and LRS. Negatively biasing of these samples led to back diffusion of oxygen ions from Ti/TiO_2 to HfO_2/Pt interface and rupture the CF .

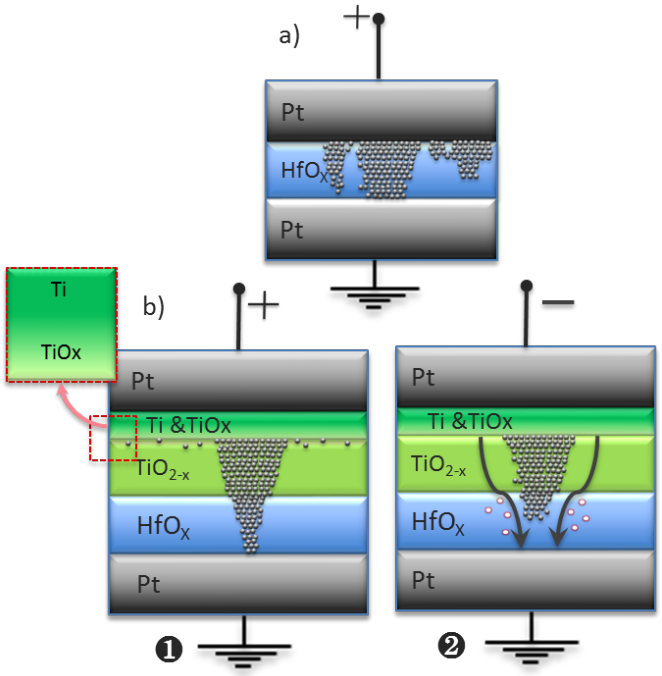


Figure 6.5 – a) Device No.1 with $Pt(BE)/HfO_2(5\ nm)/Pt(TE)$, b) Switching mechanism for the devices No.5 and 6 with $Pt(BE)/HfO_2(5\ nm)/TiO_2(3$ and $5\ nm)/Pt(TE)$ (accordingly)during: 1- set and 2- reset processes.

6.3.1 Electrical Setup Engineering

In order to achieve stable resistive switching, it is crucial to obtain a sound understanding of the behavior of oxygen vacancies as the main element responsible for the switching mechanism. Therefore, we implemented different measurement experiments to study oxygen vacancies evolution during the electrical measurement. Among fabricated devices, No.5 and 6 have been chosen for further study due to their stable resistive switching. Hence, immediately after the first 100 cycles with TE biased and BE grounded (fig.6.3 and 6.4) were finished, the direction of the bias was reversed, as the BE biased for the next 100 consecutive cycles while TE was grounded (figure 6.6a for device No.5 and figure 6.7a for device No.6). Next, to investigate the reversibility of the occurred oxygen vacancies relocation, immediately after the reversed 100 cycles were finished, the direction of the bias was reversed and the next 100 cycles applied as the same setup with the initial original measurement setup (TE biased, BE grounded) to each device (figure 6.6b for device No.5 and figure 6.7b for device No.6). When the biased was reversed for the devices No.5 and 6, both successfully switched for the next 100 cycles

without any significant change compared to their performance in the previous original biasing, whereas they exhibited highlighted response to the change in the measurement setup as it turned back to the original one. When the measurement setup for the device No.5 changed back to its original form, the device did not reset and failed at LRS state, while device No.6 successfully switched for the next 100 cycles (TE biased, BE grounded).
Moreover, during all bias direction variations, we assume that the TiO_x layer is not thick enough for the relocation of oxygen vacancies, therefore the filaments changed from the cone shape to pillar and form robust filaments which are impossible to be dissolved even by high reset voltage (~ -9 V), consequently the device No.5 when reversed back to the original measurement setup failed and could not be reset.

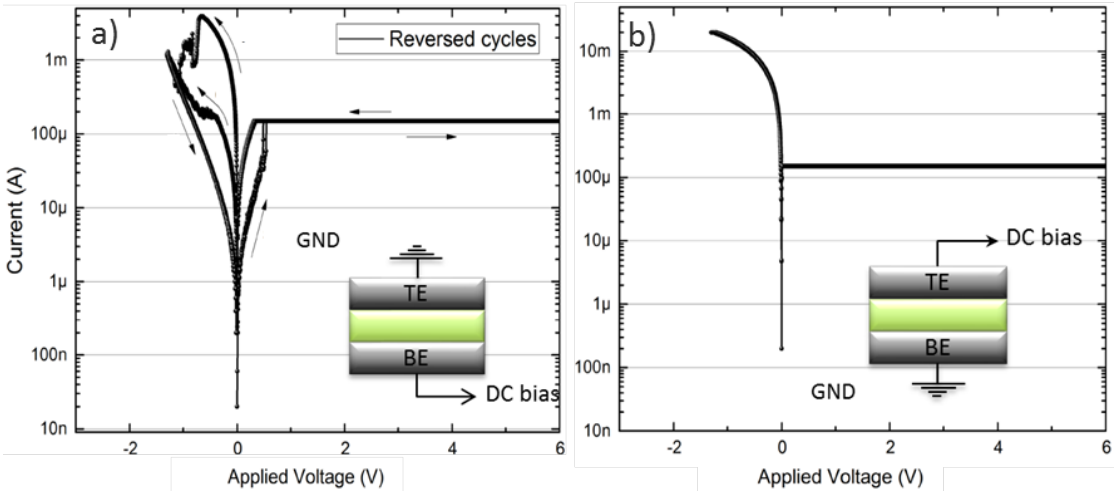


Figure 6.6 – a) Device No.5 Pt(BE)/HfO_2(5 nm)/TiO_2(3 nm)/Ti(5 nm)/Pt(TE) for: a) Reversed measurement setup (BE biased, TE grounded), b) back to original (TE biased, BE grounded)

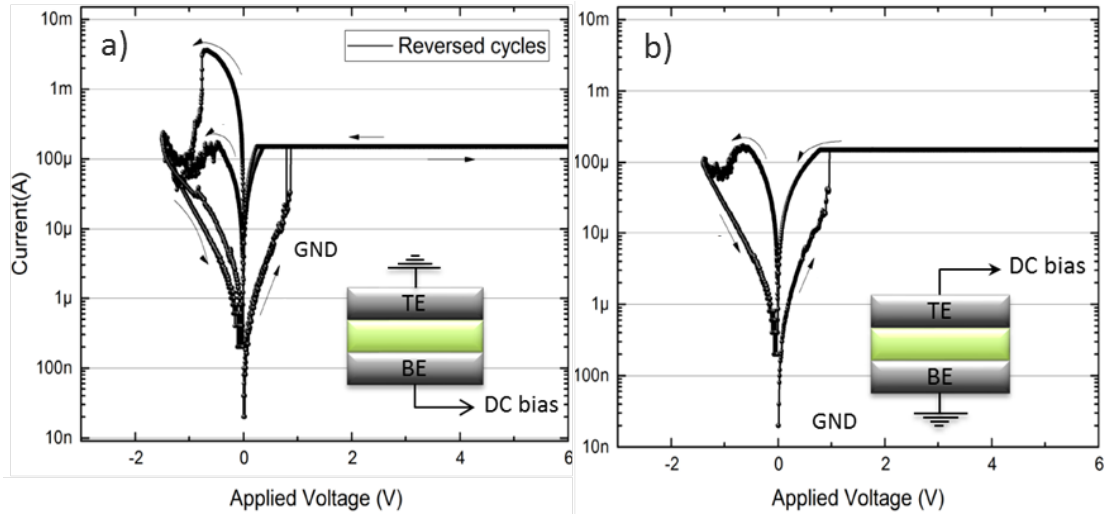


Figure 6.7 – a) Device No.6 Pt(BE)/HfO_2(5 nm)/TiO_2(5 nm)/Ti(5 nm)/Pt(TE) for: a) Reversed measurement setup(BE biased, TE grounded), b) back to original (Te biased, BE grounded).

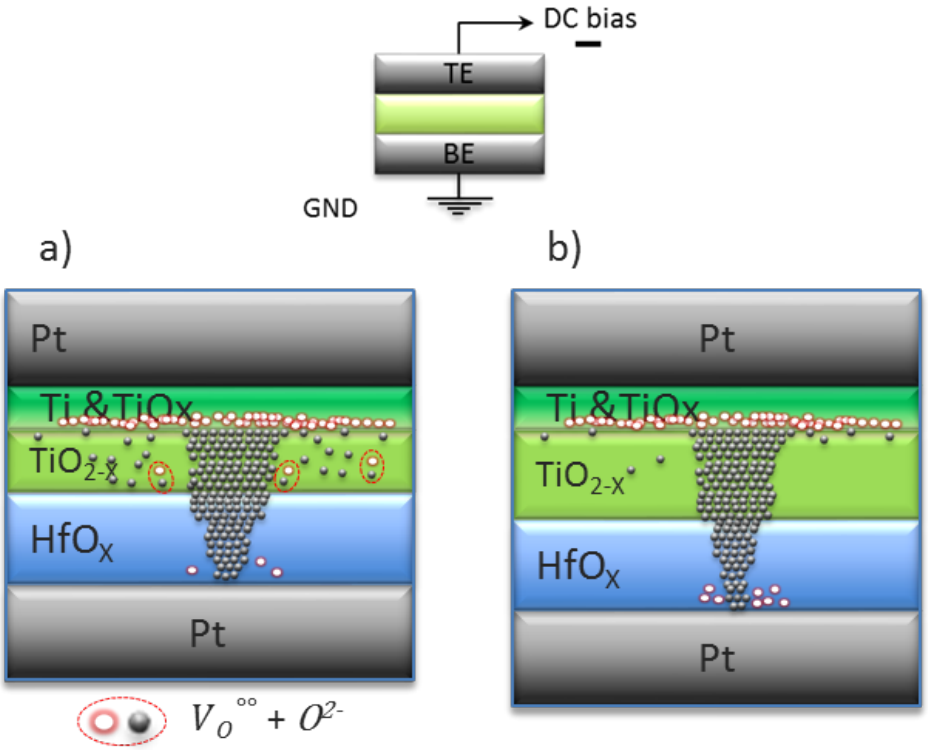


Figure 6.8 – Schematic demonstration of reset process after switching back to original measurement setup for (Te biased, BE grounded) for: a) Device No.5, b) Device No.6.

6.4 Conclusion

In this work, we demonstrated fabrication steps and electrical characterizations of different HfO_2 ReRAMs. In the first part of the work, the impact of changes in device stack structure on the electrical properties of the samples been discussed. In the second part of the work, the devices have been investigated by reversed measurement setup which has been followed immediately by the original measurement setup. The observed I-V characteristics have been explained by the proposition of a switching mechanism. We realized the movements of oxygen vacancies are reversible for oxide thickness values that are larger than a certain limit value, which allows proper migration of vacancies. The proposed switching mechanism explains this phenomena through oxygen vacancies movement.

7 Relationship between the Gibbs free energy of oxidation with the resistive switching properties of bi-oxides memristors

Authors: ***Behnoush Attarimashalkoubeh***[*,a], *Igor Krawczuk*[a], *Paul Muralt*[b], *and Yusuf Leblebici*[a]

[a] Microelectronic Systems Laboratory, EPFL, Lausanne, Switzerland [b] Ceramics Laboratory, EPFL, Lausanne, Switzerland

Authors contribution: B.A. conceived the research, developed the fabrication process, produced the samples, performed the electrical characterization, analyzed the data, and wrote the manuscript. I.K. revised the manuscript. P.M co-supervised the research, helped with the switching mechanism explanation, and revised the manuscript. Y.L supervised the research and revised the manuscript.

Relationship between the Gibbs free energy of oxidation with the resistive switching properties of bi-oxide memristors

Authors: *Behnoush Attarimashalkoubeh*, Igor Krawczuk, Paul Muralt, and Yusuf Leblebici*

Abstract

The increasing interest in memristors urges overcoming the reliability issue concerning their performance. Bi-oxide configuration of memristors has been proposed as a promising approach. In this work, we implemented several secondary oxides for HfO_2-based memristors. The implemented fabrication steps and electrical performance under D.C. measurement have been explained in details. We demonstrate a connection between the difference of the Gibbs energy of primary and secondary oxide with the resistive switching, especially for the negative polarity (reset process). We proposed, the different competition of secondary oxide with HfO_2 in oxidation leads to different formation of conductive filament (for various secondary oxides) in the ultra-thin structured memristors, which eventually affects the performance of the devices. textbfKeywords: Memristors, ReRAMs, Bi-Oxide Memristors, Oxygen Vacancies, Conductive Filaments, Gibbs Free Energy of Oxidation.

7.1 Introduction

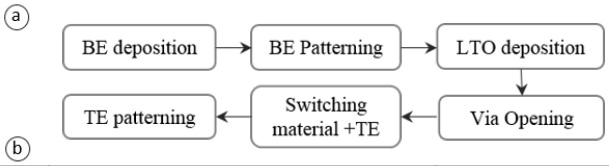
The urge to introduce new candidates to replace conventional flash-based non-volatile memories -having physical limits in down-scaling- has caused increasing attention to emerging memory technologies[58][2]. Among all candidates, Resistive Random Access Memories (ReRAMs) or memristors are most interesting due to their excellent performance in scalability, endurance, data retention, speed, and low power consumption[80][43]. The basic structure ofmemristors consists of a metal-oxide layer (storage layer) sandwiched between two metal layers to form a "Metal/Insulator/Metal" (MIM) device. The memristors have shown a promising potential to be used in different applications besides data storage, such as pattern-recognition in neuromorphic circuits[28][68]. Memristors are two terminal non-volatile devices, whose resistance can be tuned by application of an external voltage stimuli through set and reset processes[77]. The resistive switching (R.S.) mechanism of memristors is strongly dependent on the composition and microstructure of the oxide material, and the nature of the electrode interfaces. The RSM based on formation/annihilation of conductive filaments (C.F.s)[79] is recognized as a major category. Generally, the application of positive voltage to the top electrode harvests oxygen ions from the oxide layer to the top electrode (T.E.), leaving behind oxygen vacancies in the oxide. If the applied voltage is sufficiently high, the oxygen vacancies create C.F.s through the complete oxide layer, forming conductive bridges between the two metal

layers. This brings the device from an initially high resistive state (HRS) to a low resistance state (LRS). This switching from HRS to LRS in a set process, is reversible in bipolar devices by application of a negative voltage to the top electrode (T.E.) - the reset process - through partial or full rupture of C.F.s. Studies have proposed numerous candidates for the oxide layer, such as HfO_2, Al_2O_3, NiO, Ta_2O_5, TiO_2, and more complex oxides such $PrCaMnO_3$, $SrLaTiO_3$ and furhter more[58]. Among all oxides, HfO_2 is considered as one of the most promising candidates, as it enables a high switching speed and a stable endurance[55]. The challenge of implementing HfO_2-based memristors is considered to be the large variation of key switching parameters such as set and reset voltage, and current levels (I_{HRS}, I_{LRS}). The narrowing down of these variations necessitates major research efforts to reach a better understanding of the R.S. mechanism, and the evolution of C.F.s throughout a large number of R.S. processes[9][5]. Several post fabrication approaches have been proposed to overcome the variability issue (such as the addition of resistors in parallel or series), but it has been shown that they are not as effective as material/structure methods in the improving the performance of memristors[30]. Various bilayer structures have been studied including the implementation of a bilayer structure consisting same metal oxide but with different stoichiometric (i.e. Ta_2O_{5-x}/TaO_{2-x}[43]) or two different metal-oxide layers such as ZrO_x/HfO_2 [41][42] or Al_2O_3/TiO_{2-x}[3]. The studies generally looked into bi-layer oxide memristors with an additional metal-like layer thought to act as oxygen reservoir. Interestingly, the performance of the bioxide structure itself (without the extra oxygen reservoir) is less investigated. In this work, we studied the effect of various oxide layers in combination with a HfO_2 layer, to form bi-oxide HfO_2-based memristors. We proposed a switching mechanism explaining observed differences in R.S. behavior. The results can likely be extended to other ReRAM materials.

7.2 Fabrication and electrical measurement

The implemented "in-via" design in this work provides devices with the switching materials that are vertically stacked between top and bottom electrodes (T.E., B.E.). Figure7.1 provides more detail on the fabrication steps, as Fig.7.1a, schematically demonstrates the fabrication steps and Fig.7.1b provides an overview over the configuration of devices, and also the deposition of their switching materials. 100 nm Pt metal was deposited using D.C. sputtering (1000 W) on 4" Si/SiO_2 test wafers with a thin layer of Ti as an adhesion layer. The wafers were spin-coated with AZ3007 positive resist, soft baked (to enhance the adhesion of P.R. to the wafer), exposed (20 mW/Cm^2), and developed. Next, the devices have been etched using reactive ion etching with Cl_2/Ar chemistry chemistry, followed by 100 nm LPCVD deposition of LTO at 425° C (insulator layer). The vertical vias have been patterned through LTO in the second photolithography step followed by wet etch in buffered hydrofluoric acid (BHF) at 20° C. Atomic layer deposition (ALD) with TEMAH and H_2O precursors has been used to deposit HfO_x layer for all memory devices at 200° C. Al_2O_3, TiO_2, and Ta_2O_5 were deposited using sputtering tool (see Fig7.1b for deposition details). Finally, without breaking the vacuum, the Pt T.E. has been deposited and patterned. We utilised an Agilent B1500 parameter analyser to

study the electrical characteristics of all fabricated devices. The biases were applied to the T.E. while the bottom electrode was grounded during the measurement. A compliance current of 150μA was enforced via an external transistor during forming and SET. This is required to limit the flow of current in the LRS and protect the devices from damage.



b

ID.	Device Configuration	Fabrication remarks
H5	Pt(BE)/HfO_2(5nm)/Pt(TE)	HfO_2 ALD@200°C
H5Al3	Pt(BE)/HfO_2(5nm)/Al_2O_3(3nm)/Pt(TE)	Al_2O_3 deposition: 1000W, Ar/O2:30/3.0
H5Ta3	Pt(BE)/HfO_2(5nm)/Ta_2O_5(3nm)/Pt(TE)	Ta_2O_5 deposition: 700W, Ar/O2:30/2.0
H5Ti3	Pt(BE)/HfO_2(5nm)/TiO_2(3nm)/Pt(TE)	TiO_2 deposition: 500W, Ar/O2:15/1.0

Figure 7.1 – a) Brief schematic demonstration of process flow, b) Device name, their material configurations and fabrication details.

7.3 Result and Discussion

The devices were biased from 0 to 5 V and back to 0 V for (set) and 0 to -1.5 V and back to 0 V (reset). The resistance of the devices switched from HRS to LRS (set process) in positive polarity and from LRS back to HRS (reset process) in negative polarity demonstrated the bipolar switching properties for all devices. Figure7.2a exhibits the I-V characteristics of H5 for 100 consecutive DC cycles. The as-fabricated device proved to be highly resistive and required a relatively high voltage (V_f -plotted in red) as compared to the switching voltage for consecutive cycles (V_{set} -plotted in black) to initiate the switching. The H5 showed an undesired wide variation in the key switching parameters (V_{set}, V_{reset}, I_{HRS}) due to the random nature of filament formation with varied shape and geometry. Part b,c,d of Fig.7.2 presents the electrical response of H5Al3, H5Ta3, and H5Ti3 devices to the DC measurements (forming cycles are not plotted here). As evidenced in the I-V diagrams of Fig.7.2, the ultra-thin secondary metal oxide layers (Al_2O_3, Ta_2O_5 and TiO_2) have a significant influence on the RS properties comparing to HfO_2-alone device (H5). Figure7.3 provides a summary of the switching parameters for the fabricated devices. The added extra oxide layers not only reduce the width of the variation range in the switching parameters, but also lower the operation voltages (V_f, V_{set}, and V_{reset}) as is shown in the Figure7.3b. The difference between the switching performance of H5Al3, H5Ta3, H5Ti3 together and with H5 could be explained by their ability to form an oxide in competition with HfO_2. The Ta (in Ta_2O_5) has a lower standard Gibbs free energy of formation (ΔG) comparing to the HfO_2 layer beneath it. Therefore, oxygen is more strongly bound in the latter than in the first. Ta_2O_5 is therefore preferentially reduced

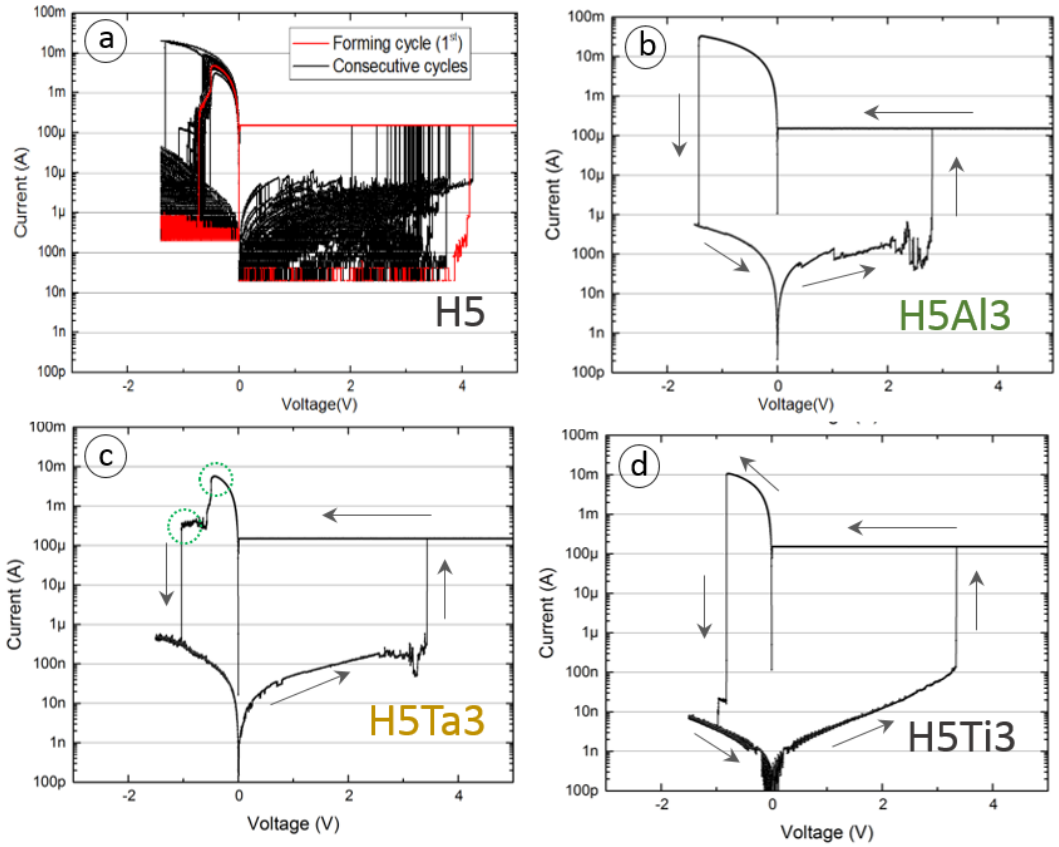


Figure 7.2 – The I-V characteristics of a) Pt(BE)/HfO_2(5 nm)/Pt(TE), b)Pt(BE)/HfO_2(5 nm)/Al_2O_3(3 nm)/Pt(TE), c)Pt(BE)/HfO_2(5 nm)/Ta_2O_5(3 nm)/Pt(TE), and d)Pt(BE)/HfO_2(5 nm)/TiO_2(3 nm)/Pt(TE).

during the filament formation. There will be more oxygen vacancies in the thin Ta_2O_5 layer, especially near their interface. In contrast, the oxygen deficient Al_2O_3 with its higher ΔG near will rather reduce the HfO_2 at the HfO_2/Al_2O_3 interface. Application of external stimuli (D.C. measurement) will create more oxygen vacancies (together with as-fabricated oxygen vacancies) for forming the C.F.s within both oxide layers as is schematically shown in Figure7.4 When the randomly created filaments in metal-oxide# 1 aligned with some of metal-oxide# 2, their connection/disconnection determines the resistance state of the device. Taking into account the different ability of oxidation of Ti, Ta, and Al in H5Al3, H5Ta3, H5Ti3 devices in competition with Hf, different R.S. properties were expected as are confirmed with their I-V diagrams (Fig.7.4) and presented in more details in Fig.7.3. Moreover, we noticed the different reset behavior of H5Ta3 (two steps reset process marked in Fig.7.3c) ultimately evolved to be similar to H5Al3 and H5Ti3. During the set/reset cycling, the oxygen vacancies drift back and forth at the HfO_2/Ta_2O_5 interface, and eventually the shape of the C.F.s changes. We assume that through continuous cycling of H5Ta3 devices, the oxygen vacancies existing in the Ta_2O_5 layer moved to the HfO_2 layer, the robustness of the formed C.F.s through HfO_2 layer

ID.	Forming Voltage (V)	Set Voltage (min , max)	Reset Voltage (min, max)
H5	4.2	2 , 4.2	-0.5, -1.38
H5Al3	3.4	1.6 , 4.1	-0.4 , -1.4
H5Ta3	4.1	2 , 4.15	-0.34 , -0.59
H5Ti3	3.9	1.8 , 3.9	-0.45 , -1.16

Figure 7.3 – Summary of switching parameters values for fabricated devices.

has increased and that the filaments got thinner in Ta_2O_5 layer to comply with their higher conductance (similar to what we expect in H5Al3 and demonstrated in Fig.7.4c). Therefore, ultimately the rupture of C.Fs in Ta_2O_5 layer (thin filament) are assumed to be responsible of the observed "one-step" reset (the robust filaments in HfO_2 will not disconnect from the interface) which disconnect the C.Fs from the T.E. and is observed as a sudden drop of current in I-V diagram in lower V_{reset} value (-0.59 V), similar to what had been seen previously for its first step of reset(-0.56 V).

7.4 Conclusion

In this work, we provide fabrication details and electrical characterization of HfO_2(5 nm)-based memristors (HfO_2-only, and bi-oxide structures). Different metal oxides have been

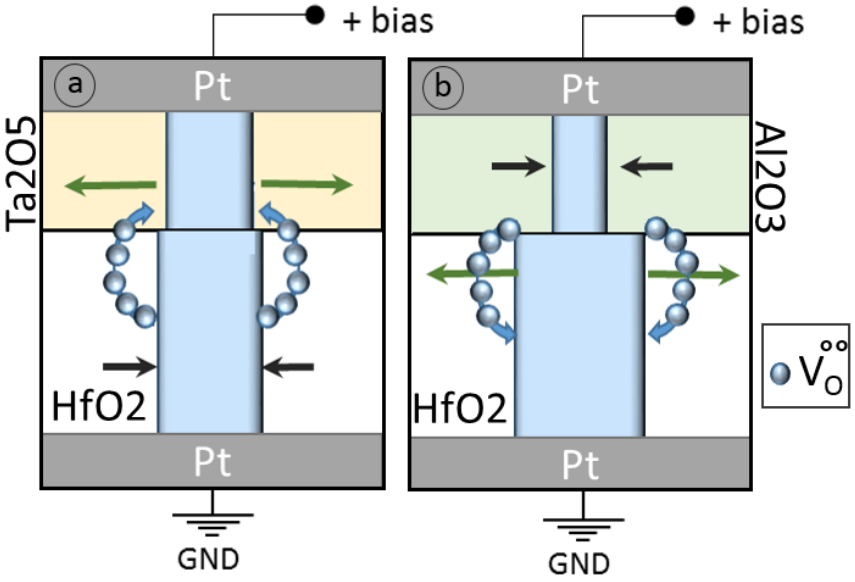


Figure 7.4 – Schematic demonstration of switching mechanism for H5Al3 and H5Ta3.

deposited in contact with HfO_2 layer and their electrical R.S. has been studied. The I-V characteristics obtained from D.C. electrical measurements provide an interesting insight into the switching mechanism of bi-oxide HfO_2-based memories regarding their choice of secondary oxide. Furthermore, the switching mechanism for the bi-oxide memristors based on their ability in oxide formation in competition with HfO_2 layer has been proposed, which is in agreement with their switching parameters obtained from I-V diagrams. Moreover, the effect of continuous cycling on the evolution of C.F.s device has been explained.

8 In-depth Structural and Electrical Characteristics Study of HfO_X-based resistive Random Access Memories (ReRAMs)

Authors: ***Behnoush Attarimashalkoubeh***, and Yusuf Leblebici*

Microelectronic Systems Laboratory, EPFL, Lausanne, Switzerland

Authors contribution: B.A. conceived the research, developed the fabrication process, produced the samples, performed the electrical characterization, analyzed the data, and wrote the manuscript. Y.L supervised the research and revised the manuscript.

In-depth Structure and Electrical Characteristics Study of HfO_X-based resistive Random Access Memories (ReRAMs)

Authors: *Behnoush Attarimashalkoubeh*, and Yusuf Leblebici*

Abstract

The variation issue has been known as the main hurdle in the commercialization of ReRAM technology, which encourages further studies to find a solution to resolve this issue. Less variation in switching parameters meaning better switching uniformity is only possible through precise control over formation/annihilation of filaments during the set and the reset process. In this work, we investigated more than 18 different HfO_2-based ReRAMs to control the variation issue, and different structural modification approaches have been studied. In the implementation of bi oxide HfO_2-based ReRAMs, the competency of the secondary oxide information of oxide in competition with Hf ions have been investigated and proved to affect the resistive switching significantly. Besides, the effect of the Ti buffer layer on the performance of HfO_2-based ReRAMs have been investigated.

Keywords: Resistive Random Access Memory (ReRAM), Variation issue, HfO_x-based ReRAM, Bi-Oxide, buffer layer, oxygen reservoir, oxygen vacancies.

8.1 Introduction

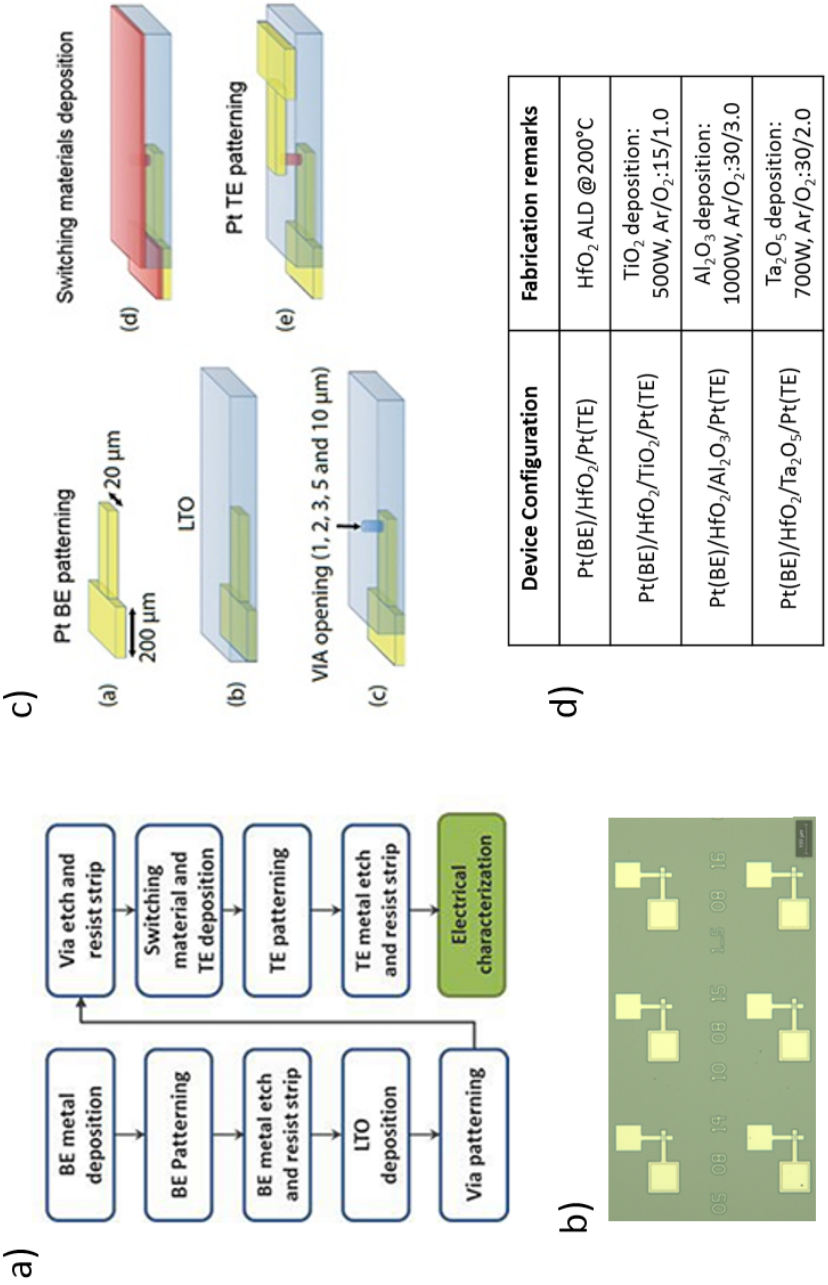
Resistive Random Access Memories (ReRAMs) have been researched intensively in the last decades as one of the next generation non-volatile memory (NVM) candidates to replace conventional charge-based memories for future computing systems. ReRAMs, with their comparatively simple structure and fabrication techniques, have been considered as one of the most promising candidates. Generally, ReRAMs consists of a metal-oxide layer sandwiched between two different metal and work based on the movement of vacancies[78]. During the set process, the oxygen vacancies are relocated and form conductive filaments (C.F.s) through the metal-oxide layer and switch ON the device (LRS), while partially/fully annihilation of the C.F.s can drift back the resistance to higher resistance states(HRS) during the so-called reset process. It is hard to control the switching mechanism of ReRAMs due to the movement of nano-scale oxygen vacancies. The variations issue in the key switching parameters has resulted from this uncontrolled formation of filaments with different geometries, which decrease the reliability of this technology and acts as a hurdle in commercializing it[53]. To solve this problem, a better understanding of the switching mechanism by having an in-depth knowledge of the interaction between layers at the interfaces is highly required[59]. In this study, several HfO_x-based memory devices(see Table 1) have been fabricated in a systematic approach, and their

D.C. electrical characteristics have been investigated. The Hafnium oxide material has been chosen considering its promising performance among all the other candidates (i.e., TaO_x, TiO_x, etc.). The fabrication process flow is shown in the Figure8.1a,b.
It has been previously reported which employing an extra metal layer has a significant effect in limiting the variation issue[54][39][6]. Therefore, the additional Ti metal buffer layer has been chosen carefully compatible with the adjacent metal-oxide as it is shown to be the best candidate in eliminating any additional side-effect originated from the mismatch with the metal-oxide beneath it[48]. This work provides detailed process flows for the fabrication steps and systematically investigates the resistive switching properties of more than 18 different devices. Different structural methods have been implemented to suppress the variation issue, such as bi-oxide layer (using Al_2O_3, Ta_2O_5 and TiO_2 as the secondary oxide together with HfO_2), and an additional metal buffer for the bi-oxide ReRAM. To have a better understanding and to find the optimized device, different parameters have been varied throughout this work, such as thickness and order of the oxide depositions.

8.2 Method and materials

8.2.1 Process Flow and Fabrication

We implemented "in-VIA" design to vertically deposit the switching materials between the top and bottom electrodes (T.E., B.E.). A thin layer (5 nm) Ti has been deposited using D.C. sputtering (1000 W, 9.0 sccm Ar) on top of a 4" Si/SiO_2 test wafers to act as the adhesion layer for the Pt. Next, 50 nm Pt metal was deposited using D.C. sputtering (1000 W, 15.0 sccm Ar), followed with a short HMDS process and a thin coat of AZ3007 positive resist. The devices were soft baked (at 115° C to improve the adhesion of P.R. to the wafer), exposed (20 mW/Cm^2), and developed (using MF CD 26) to define the B.E. Next, we used a reactive ion etching (RIE) tool with Cl_2/Ar chemistry to pattern the B.E. made of Pt. A layer of *Low-Temperature Oxide* LTO (100 nm) has been deposited on the patterned B.E. using a *LPCVD* tool at 425° C, the LTO layer acts as a passivation layer and isolate T.E. and B.E. The second step of photolithography opened the VIAs within the LTO, followed by a wet etch step in buffered hydrofluoric acid (BHF) at 20° C. To deposit HfO_2 layer, we used an *Atomic layer deposition* (ALD) tool with TEMAH and H_2O precursors for all memory devices at 200° C. The thickness of the deposited layer has been precisely controlled with the number of purges. Al_2O_3, TiO_2, and Ta_2O_5 and metallic layer of Ti were deposited using sputtering tool. Finally, without breaking the vacuum, the Pt T.E. has been deposited and patterned as explained earlier for the B.E. Figure 8.1 provides more detail on the fabrication steps, with Fig.8.1a, schematically demonstrates the fabrication steps, Fig.8.1b shows an overview of the configuration of devices, and Fig.8.1c provides more detail for the deposition of switching materials.
To eliminate the effect of different B.E. on the switching properties of fabricated devices, all devices benefited from same B.E. and patterned via, then the wafers have been diced and been used for any further fabrication steps. The design for each structure includes more than 300 different devices, providing enough samples for the analysis of device to device distribution.



Device Configuration	Fabrication remarks
Pt(BE)/HfO_2/Pt(TE)	HfO_2 ALD @200°C
Pt(BE)/HfO_2/TiO_2/Pt(TE)	TiO_2 deposition: 500W, Ar/O_2:15/1.0
Pt(BE)/HfO_2/Al_2O_3/Pt(TE)	Al_2O_3 deposition: 1000W, Ar/O_2:30/3.0
Pt(BE)/HfO_2/Ta_2O_5/Pt(TE)	Ta_2O_5 deposition: 700W, Ar/O_2:30/2.0

Figure 8.1 – a) Flow chart of fabrication steps, b) Schematic demonstration of process flow including the material deposition and the patterning steps, c)optical microscope image of a device after fabrication and d)Device configuration and fabrication details. The relatively larger pads (in yellow) are designed to provide sufficient space for the measurement steps.

8.2.2 Electrical Setup and Measurement

We utilized an Agilent B1500 parameter analyzer to study the electrical characteristics of the fabricated devices. The biases were applied to the T.E.s while the B.E.s was grounded during the measurement. A compliance current of 150μA was enforced via an external transistor during forming and positive biasing of the devices. The compliance current is required to limit the flow of current in the low resistance state (LRS) and protect the devices against hard breakdown. The devices were biased from 0 to 5 V and back to 0 V (0 → 5 → 0 V) for set and 0 to -1.5 V and back to 0 V (0 → -1.75 → 0 V) for reset. The switches of resistance from HRS to LRS (set process) in positive polarity and the LRS to HRS switch (reset process) in negative polarity exhibited the bipolar switching property regardless of the device configuration for all our fabricated devices.

8.3 Result and discussion

For the consistency of the discussion, the paper is categorized in the following order. First, we studied HfO_2-only ReRAMs (Pt(BE)/HfO_2/Pt(TE) structure) as the reference devices. Next, implementation of bi-oxide ReRAMs are studied, this section provides an overview of the effect of the choice of the secondary oxide and the thicknesses on the electrical characterization of fabricated ReRAMs. Finally, the role of the buffer layer in improving the uniformity of electrical behavior of the devices has been studied.

8.3.1 HfO_2-alone ReRAMs

For HfO_2-alone device structure, we tried different thickness of HfO_2=1, 3, 5, 7, and 10 nm. The device was biased, as mentioned earlier. We observed the device with 1 nm of HfO_2 to be leaky (in pristine low resistance state), for HfO_2=3 nm even though the device initially appeared to be resistive, but after the forming sweep, the reset bias could not switch back the resistance to HRS, and the device failed at LRS. For a device with HfO_2=5 nm, we could successfully switch the device between HRS and LRS. Figure8.2 shows the resistive switching (R.S.) behavior of the device for the first 100 cycles. The sweep plotted in red presents the first positive bias applied to our as-fabricated device (known as forming voltage), switched at 4.2 V to LRS. The initial reset could successfully bring back the device resistance state back to LRS. while the problem with the device with the HfO_2=5 nm appears to be the high variation in its switching parameters, the other devices with 7 and 10 nm also suffered from high forming voltage and unstable switching (V_f>5 V for the Pt/HfO_2(7 nm)/Pt).

8.3.2 Bi-Oxide HfO_2-based ReRAMs

The variation in the key switching parameters (V_{set}, V_{reset}, I_{HRS}, I_{HRS}) could be explained by stochasticity of the ion movements (oxygen vacancies) responsible for the set and reset opera-

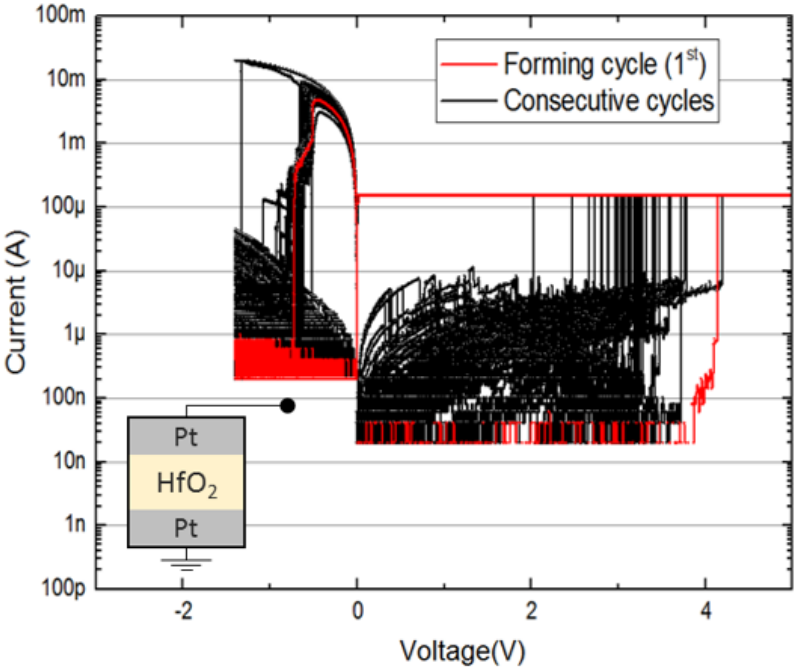


Figure 8.2 – The I-V characteristics of the Pt/HfO_2(5 nm)/Pt, the forming voltage is plotted in red while the next consecutive sweeps are plotted in black. The inset schematically demonstrates the biasing of the device.

tions. In literature, different post fabrication techniques have been introduced to suppress the undesired variability issue of the single layer ReRAMs, such as insertion of an external resistor in series with the ReRAM (to improve the LRS) or in parallel to improve the fluctuation in HRS states. However, there is not such a solution to stabilize the V_{set} and V_{reset} fluctuations, as it will not affect the stochasticity. A promising approach to overcome this issue is the implementation of bi-oxide devices. In this work we inserted different thickness of TiO_2, Ta_2O_5 and Al_2O_5 in contact with the HfO_2(5 nm)layer. Figure 8.3 shows the I-V switching properties of the bi-oxide ReRAMs with 3nm of the secondary oxide of Ta_2O_5, TiO_2, and Al_2O_3 (Pt(BE)/ HfO_2(5 nm)/Ta_2O_5, TiO_2, Al_2O_3(3 nm)/Pt(TE)) configuration. Besides the noticeable improvement in reliability of these bi-oxide layer devices comparing to the HfO_2-only device, the observed varied R.S. in the bi-oxide layer devices depending on the implemented secondary oxide is noticeable; especially for I_{HRS}, V_{set} and the shape of reset. We assume the noticeably altered R.S. behavior among bi-oxide devices is due to their different ability in the formation of oxide in competition with the Hf in the adjacent HfO_2 layer.

The conductive filaments to be formed in the bi-oxide devices is highly dependent on their standard Gibbs free energy of formation of oxide (ΔG) in competition with Hf in the layer beneath it. For instance for in bi-oxide device implementing Ta_2O_5 (with higher ΔG of oxidation in competition with Hf) the resulted R.S. is expected to be un-similar to the devices employing Al_2O_3 and TiO_2 (with lowerΔG) as their secondary oxide. For Hf5Ta3, Hf has a lower

ΔG comparing to Ta. Therefore it preferentially oxidized during the filament formation and injects some more oxygen vacancies in Ta_2O_5, especially near their interface. while in Hf5Ti3 and HfAl3 the situation is reversed, for instance in Hf5Al3, the Al reduces Hf in the HfO_2 layer and leaves behind oxygen vacancies, especially near the interface of the two oxides. Therefore, we can conclude that employing different secondary metal-oxide in contact with HfO_2 layer, will results in dissimilar R.S. as a result of different ΔG of oxidation in competition with the Hf, such as the utterly different reset observed for our bi-oxide devices (as is seen in Fig.8.3). Figure 8.4 presents a summary of Forming voltages (V_f) for the bi-oxide HfO_2-based ReRAMs with varied thickness of the secondary oxides. It is clear which the thickness of secondary oxide has a high impact on the R.S. of the devices, directly influencing V_f, V_{set} and V_{reset} and controlling the resistance values of HRS and LRS, for instance, the devices with higher thickness of the secondary oxide, require larger forming voltage. The high forming voltage is not desirable and generally leads to the degradation of performance; as an example, the device with Al_2O_3=7 nm failed after a few sweeps. Further device engineering is yet required to improve the uniformity of the resistive switching and lower the forming voltages. Next, to make a better conclusion of the bi-oxide devices, we reversed the order of deposition of the oxide layers (for HfO_2=5nm), Pt(BE)/ TiO_2(3 nm)/HfO_2(5 nm)/Pt(TE) and Pt(BE)/ TiO_2(5 nm)/HfO_2(5 nm)/Pt(TE). For devices with Pt(BE)/HfO_2/TiO_2/Pt(TE), the rupture/formation is assumed to happen in the TiO_2 layer, while for Pt(BE)/TiO_2/HfO_2/Pt(TE), the HfO_2 has this role. Considering the HfO_2 layer is deposited using ALD tool, we expect higher quality rather than sputtered TiO_2 layer. Moreover, the vacuum for Pt(B.E.)/TiO_2/HfO_2/Pt(T.E.) was unavoidably broken to transfer the samples to ALD tool, which could change the stoichiometric of the TiO_2 layer, and reduce the creation of oxygen vacancies between the oxide layers in the interface. This assumption is confirmed by observation of higher forming voltage and lower resistance variation, especially of I_{HRS} for Pt(BE)/TiO_2/HfO_2/Pt(TE) comparing to the comparable thickness but Pt(BE)/HfO_2/TiO_2/Pt(TE)

8.3.3 Role of Buffer Layer

Another proved approach in improving the reliability of ReRAMs comprise the use of an active metal layer (buffer layer) acting as an oxygen reservoir/scavenger layer. This layer not only harvest oxygen ions from the layer beneath it (creation of oxygen vacancies), but also the oxygen ions can be stored there and later inject back to the switching materials during the set and reset operations. In this work, we investigated the effect of insertion of Ti buffer layer (1, 3, 5 nm) on the performance of Pt/HfO_2(5 nm)/TiO_2(5 nm)/Pt devices (H5Ti5). The Ti=1 nm of the buffer layer resulted in relatively lower V_f (3.9V) but was not effective in improving the variation issue observed in for the switching parameters of H5T5 device. Comparing the devices with Ti=3 and Ti=5 nm, the device with 5 nm Ti showed better switching properties with uniform R.S. properties (inset of Fig.8.5c). Further increase of Ti layer thickness (Ti=7 nm), led to the noticeably larger variation (comparing to the device with 5 nm Ti as buffer layer) in R.S. which eventually resulted in degradation of performance by cycling.
Moreover, two devices with Pt/ HfO_2(5 nm)/TiO_2(3 nm)/Pt device (H5Ti3) and Pt/ HfO_2(5

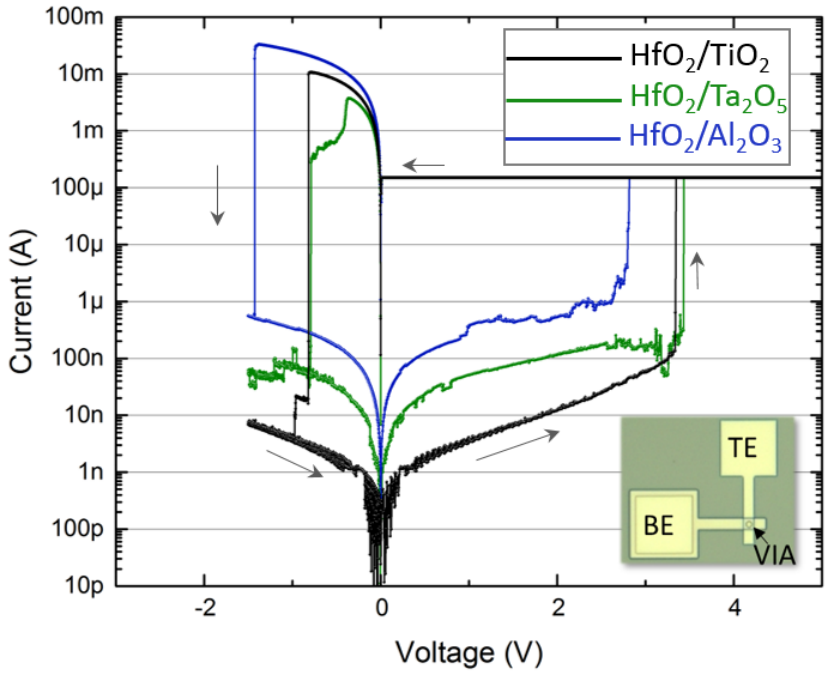


Figure 8.3 – I-V characterisation of bi-oxide devices with Pt/HfO_2(5 nm)/Al_2O_3(3 nm)/Pt (plotted in blue), Pt/HfO_2(5 nm)/Ta_2O_5(3 nm)/Pt (plotted in green), and Pt/HfO_2(5 nm)/TiO_2(3 nm)/Pt (plotted in black). The inset demonstrates a optical microscopic image of the devices, with BE and TE and the vias vertically between them.

Secondary oxide	V_F for 3nm(V)	V_F for 5nm(V)	V_F for 7nm(V)
Al_2O_3	3.4	3.9	6
TiO_2	3.9	4.1	5
Ta_2O_5	4.1	4.2	4.2

Figure 8.4 – The summary over forming voltages of bi-oxide ReRAMs HfO_2=5 nm, with secondary oxides for varied thicknesses.

nm)/TiO_2(3 nm)/Ti(5 nm)/Pt have been fabricated and their electrical characterization have been studied. We noticed a 3 nm thin layer of has significantly influenced the R.S. comparing to the H5Ti3 device. The HRS for H5Ti3 has shown more resistive properties with larger variation (52 k →2.18 MΩ) while for the device with added 3 nm the distribution appeared to be significantly less resistive with a uniform switching properties(26 K→43 KΩ). Moreover, the insertion of 3 nm Ti on Hf5Ti3 device, effectively decreased the V_{set} changing from the range of 1.8-3.9 V for HfTi3 to the range of 0.5-0.8 V for the device with extra Ti layer. This effect could be explained by the role of Ti as an active metal in creation of oxygen vacancies as the permanent defects throughout the switching materials; the more defective oxides are less resistive and required lower voltage for the formation of conductive filaments. Hence, even though the insertion of sufficiently thick buffer layer generally improves the R.S., but the stack

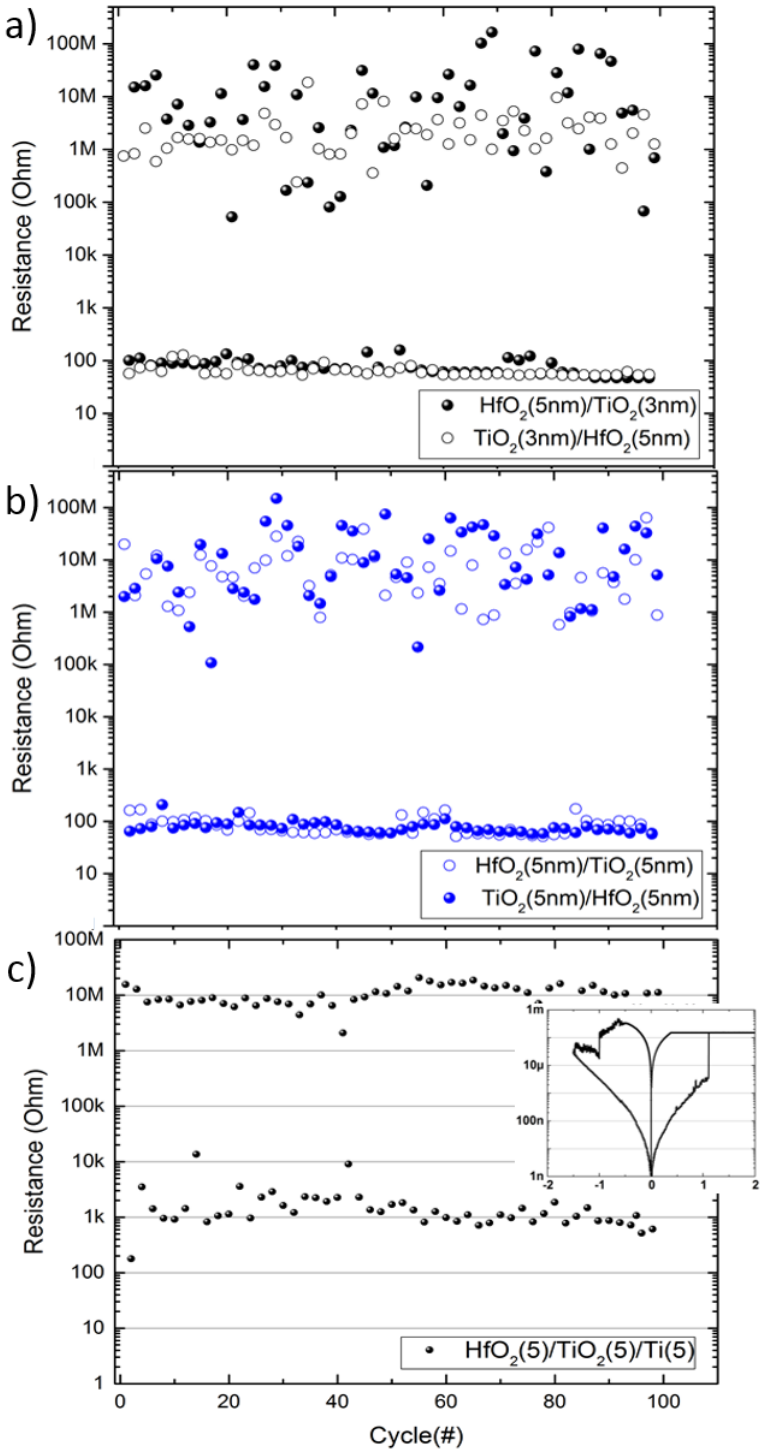


Figure 8.5 – Cycle to Cycle HRS/LRS distributions for devices with a) $TiO_2(3)/HfO_2(5)$ and $HfO_2(5)/TiO_2(3)$,and b)$TiO_2(5)/HfO_2(5)$ and $HfO_2(5)/TiO_2(5)$, and c)$HfO_2(5)/TiO_2(5)$ configurations.

structure of the ReRAMs should be precisely designed to reach a proper trade-off between required R.S. properties and cycle-to-cycle reliability, as the performance of the Hf5Ti3 and H5Ti5 with an extra Ti buffer layer appeared to be dissimilar. Among all devices with an added buffer layer, the Pt/ HfO_2(5 nm)/TiO_2(5 nm)/Ti(5 nm)/Pt showed the best switching properties with stable uniform switching among fabricated devices with uniform switching properties between HRS and LRS levels as is demonstrated in the Fig.8.5c.

8.4 Conclusion

In this work, we investigated the switching properties of HfO_2-based ReRAMs with different stack structures in pursuance of improving the reliability issue observed in the HfO_2-only ReRAMs. The HfO_2-only ReRAMs appeared to suffer significantly from variation issue, resulted in the large fluctuations of their key switching parameters and degraded R.S. behavior. Three different metal oxides (TiO_2, Ta_2O_3 and Al_2O_3) introduced to the HfO_2-only devices and the observed switching properties explained by the different Gibbs free energy of oxidation. Moreover, the role of the Ti buffer layer on the device properties has been studied. As the active metal layer of Ti introduces oxygen vacancies to the switching materials of as-fabricated devices, the thickness of switching materials together with the thickness of Ti are considered to be important in defining the R.S. behavior of the ReRAMs. We observed the ReRAM with Pt/ HfO_2(5 nm)/TiO_2(5 nm)/Ti(5 nm)/Pt demonstrated the best performance with sufficient on/off ratio and proper uniformity of switching parameters (V_{set}, V_{Reset}). Lowering the thickness of TiO_2 resulted in a significant reduction of on/off ratio.

9 Novel 3D architecture of 1S1R

Authors: ***Behnoush Attarimashalkoubeh**** *, and Yusuf Leblebici*

Microelectronic Systems Laboratory, Ecole Polytechnique Fédérale de Lausanne (EPFL, Lausanne, Switzerland

Authors contribution: B.A. conceived the research, developed the idea, fabricated the devices, and wrote the manuscripts. Y.L supervised the research and revised the manuscript.

Novel 3D architecture of 1S1R

Authors: *Behnoush Attarimashalkoubeh* , and Yusuf Leblebici*

Abstract

In this work, we present a novel 3D architecture of one-selector-one-resistor (1S1R). This design eliminates the needs of physical wiring and provides valuable information for isolated selector/resistor elements together with their 1S1R integrated configuration. This design could be used for a broad selection of materials.

Keywords: Resistive Random Access Memory (ReRAM), Bi-Oxide, Sneak path issue, the selector device, 3D integration, 1S1R architecture.

9.1 Introduction

Resistive Random Access Memories (ReRAMs) have been researched intensively in the last past decades as one of the promising alternatives of the next generation of non-volatile devices[85]. ReRAMs, with their excellent properties such as high switching speed, low power consumption, scalability together with available fabrication techniques, have raised expanding interests and encourages further studies[82].

ReRAMs in their most simple structure consisting of a thin transition metal oxide layer (TMO) sandwiched between two metal layers (top and bottom electrodes)[79]. The concept of switching mechanism is straightforward; the as-fabricated device appears to be highly resistive (HRS), upon biasing the top electrode (T.E.) when the applied voltage is sufficiently high, the device will switch to a lower resistance state (LRS) in a process called set. This process is reversible through the application of a negative voltage which brings back the resistance level to the higher values (reset process)[80]. ReRAMs due to their simple structure can be implemented to the cross-point architecture. The simple but yet effective cross-point design, allows an effective cell area of $4F^2$ in 2D, while the feasibility of achieving 3D configuration by stacking multiple 2D layers, bring down the cell area to $4F^2/n$ and lead to very high integration density. In a cross-point architecture, the parallel interconnects (word and bit lines) are considered as top and bottom electrodes (T.E., B.E.), the switching materials could be formed between them[4].

However, the undesired sneak current through unwanted cells significantly decreases the efficiency of the system, causes programming and read errors, increases the consumption of energy per bit, and limits the scaling down, as the bigger arrays present higher available paths

for the leakage[26].

The sneak path issue could be avoided by connecting a separate non-linear resistive switching device in the series with each resistive memory elements. Crystalline VO_2 and NbO_2 showing an Insulator-to-Metal Transition (IMT) have been previously reported as the passive non-linear element[69][35][13].

9.2 The 3D configuration of 1S1R

9.2.1 The Concept

In this work, we proposed a novel 3D 1S1R architecture design, which can provide exciting insights not only on the 1S1R device but also the selector and resistor individually. In the conventional 3D 1S1R design, the resistor (R) and selector (S) elements are generally deposited on two different substrates and physically wired together (shown in Figure 9.1a) Also, the resistor and selector elements can be deposited in contact between word and bit lines on two separated substrates (as is shown in Figure9.1b) and the 1S1R elements could be addressed by biasing the related word and bit lines. However, in our 3D 1S1R architecture, the selector and resistor elements are separately deposited on the same substrate between two parallel bit lines sharing a common word line, as conceptually shown in the Figure 9.1a. The shared word line acts as the top electrode: T.E. (bottom electrode: B.E.) for R(S). The critical benefit of this architecture is considered to be the elimination of wire integration of S and R. Moreover, this configuration allows the electrical characterization of all elements, separately and integrated. In other words, the design makes it possible to characterize the isolated behavior of each component (S, R) and the integrated configuration (1S1R), solely according to the setting of selected pads for the measurements as is shown in the Figure 9.2b.

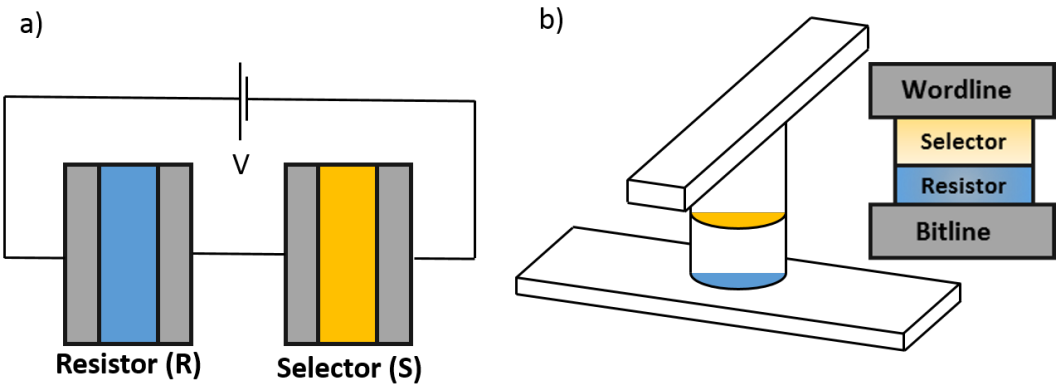
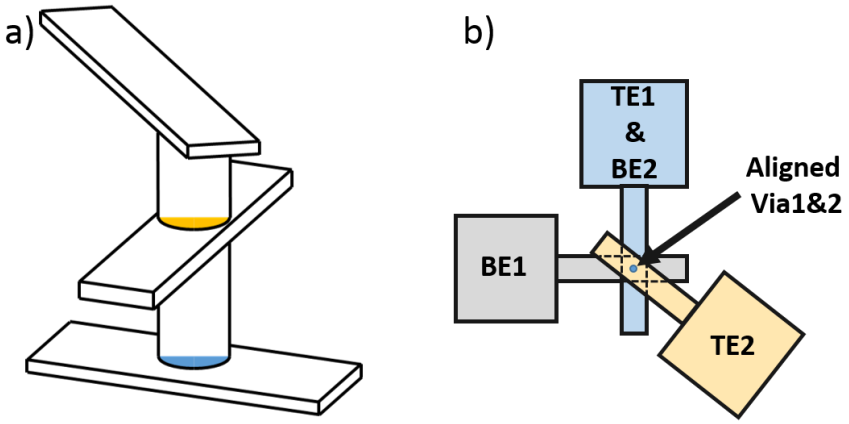


Figure 9.1 – a) Schematic demonstration of conventional 1S1R architecture a) physically wired , b) in contact together.



	BE1	TE1/BE2	TE2	Result
BE1	-	✓	-	Resistor (R)
TE1/BE2	-	-	✓	Selector (S)
TE2	✓	-	-	Resistor+Selector (1S1R)

Figure 9.2 – a) Schematic demonstration of proposed 1S1R, b) different possible configurations of device measurement (BE: bottom electrode, TE: top electrode).

9.2.2 Process Flow and Fabrication

The fabrication steps are shown in Figure9.3. To achieve a desirable performance of the 1S1R, the materials for resistor and selector should be selected carefully, and the stack of their stand-alone device must be optimized before the integration. For instance, if Tungsten is used (in oxide state as the resistor or metallic as the metal-electrodes), the resistance state of the device is determined by its degree of oxidation (WO_3 is highly resistive)[16]. Thus, the methods such as insertion of an extra oxygen barrier could be considered[66]. This configuration is not only implementable for stand-alone devices (see Figure 9.2b), but also the cross-point array (see Figure 9.4). Among the researched TMO materials, ALD deposited HfO_x has proven to present a proper performance[24]. Therefore, we have considered HfO_2-based resistor and VO_2 as the selector element. The VO_2 is deposited by reactive magnetron sputtering, using a metallic Vanadium target in an Ar plasma (17.4 sccm), while the flow of oxygen has been maintained throughout deposition by a Proportional Integral Derivative (PID) controller. The deposition followed by 1h of post-deposition annealing to ensure the crystallization of VO_2 film. To avoid the damage during the etching steps to the deposited layer of VO_2, the deposition could be done through a shadow mask with openings for the via and access pads to achieve the desired structure previously shown in Figure 9.2a. The mask must be placed and aligned precisely on the structure before deposition of the selector film followed by the T.E. deposition.

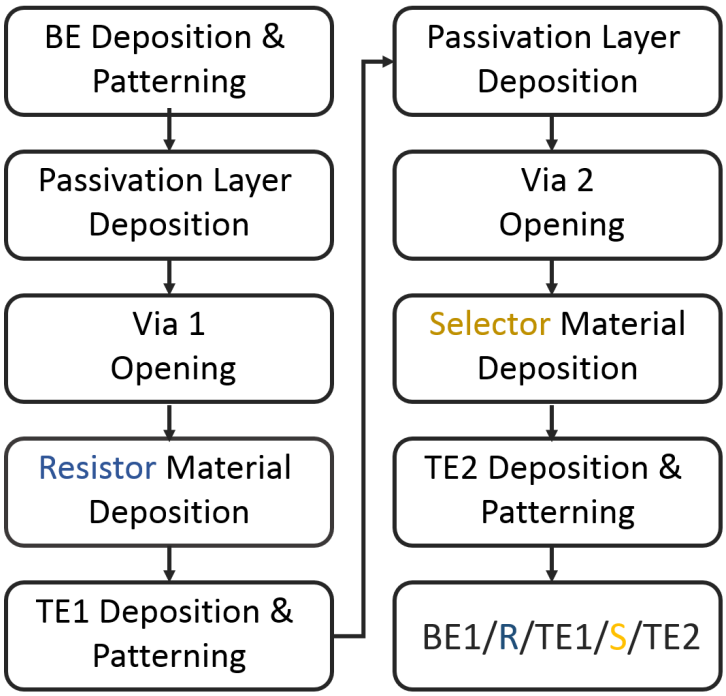


Figure 9.3 – The general process flow of fabrication of the 1S1R devices.

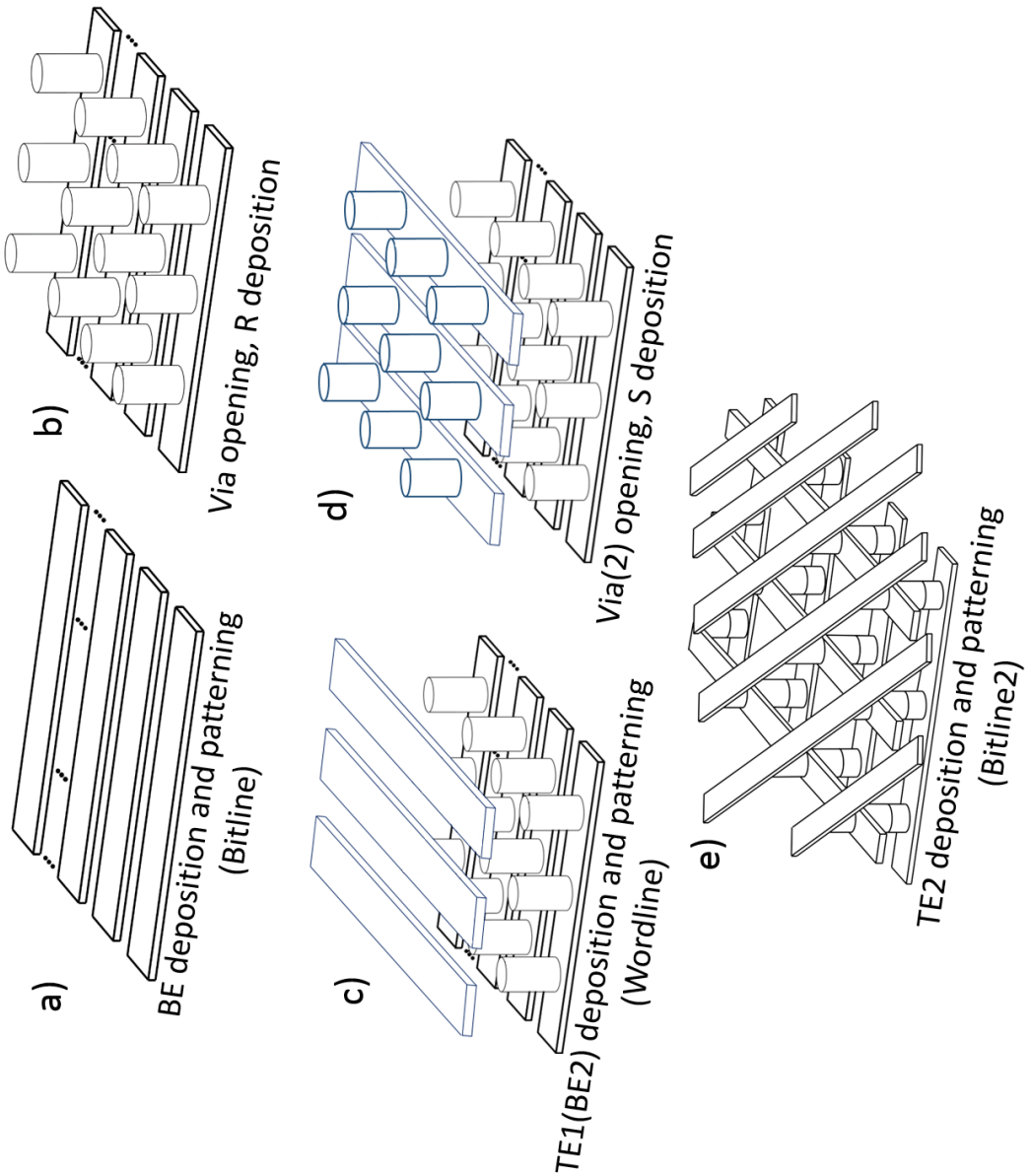


Figure 9.4 – Fabrication steps of 3D 1S1R cross-point array flow.

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10 Improving reliability issue of HfO_2-based memristors by protecting the switching materials against buffer layer deposition

Authors: ***Behnoush Attarimashalkoubeh**** *, and Yusuf Leblebici*

[a] Microelectronic Systems Laboratory, EPFL, Lausanne, Switzerland [b] Ceramics Laboratory, EPFL, Lausanne, Switzerland

Authors contribution: B.A conceived the research, developed the idea, produced the devices, performed electrical measurement and wrote the manuscripts. Y.L supervised the research and revised the manuscript.

Improving reliability issue of HfO_2-based memristors by protecting the switching materials against buffer layer deposition

Authors: *Behnoush Attarimashalkoubeh*, and Yusuf Leblebici*

Abstract

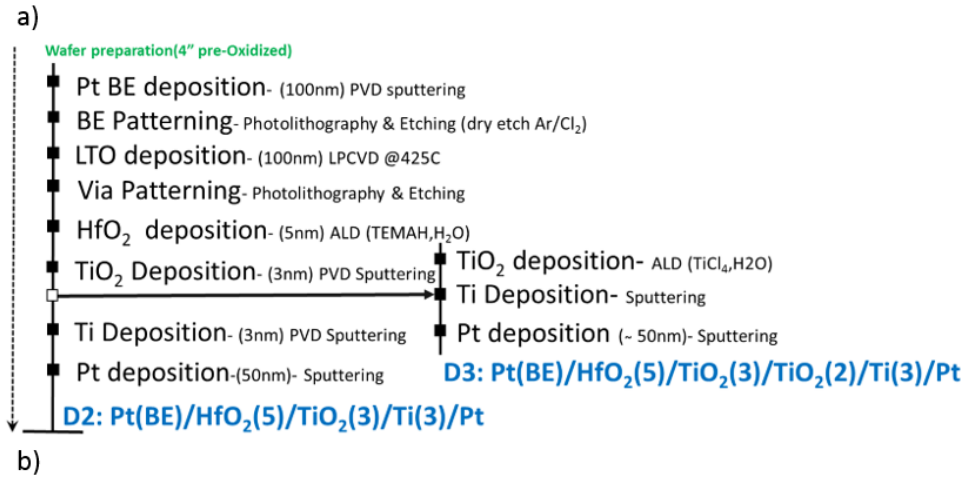
As the variability issue is considered to be the main hurdle in the commercialization of the memristor technology, further researches are encouraged to solve it. In this study, we fabricated different HfO_2-based memristors and investigated their electrical properties. We demonstrated how the insertion of a thin layer (2 nm) of TiO_2 between the Ti buffer layer and the oxide, could effectively reduce the uncontrolled formation of conductive filaments composed of oxygen vacancies and results in a better resistive switching performance. We assume the ALD deposited TiO_2 protected the oxide materials against penetration of PVD deposited Ti during the fabrication.
Keywords: ReRAMs, Memristor, Oxygen Vacancy, HfO_x-based memristors, Variation Issue, Buffer layer.

10.1 Introduction

The conventional charge-based semiconductor memories appeared to be unable to fulfill the constantly increasing needs of non-volatile memories (NVM) industries as they ceased to be scaled down due to physical limitation. The urge to replace the current NVM technologies and to present new ultra-dense storage with high speed and low-power consumption[53][79], has brought significant attention to the emerging NVM technologies such as phase change random access memory (PCRAM), magnetic random access memory (MRAM), ferroelectric random access memory (FeRAM), and resistive random access memory (ReRAM). Among all the candidates, ReRAMs (memristors) have demonstrated promising behavior due to their simple and fab-friendly structure, CMOS compatibility, and outstanding performance[79][43][82].

Memristors consist of a metal-oxide layer sandwiched between two metal electrodes, and the resistance could be tuned between different resistance levels. The switching mechanism of memristors is explained based on formation/annihilation of conductive filaments (CFs) throughout switching materials in the set/reset processes[80]. The oxygen vacancies under positive biasing rearrange and bridge between two metal electrodes, which causes the resistance switch between high resistance state (HRS) to low resistance state (LRS) through the set process. This phenomenon is reversible (LRS to HRS) through re-combination of oxygen ions and oxygen vacancies under negative polarity biases, which partially/fully dissolve the

CFs (reset process). The resistive switching (RS) has been reported for a wide range of materials including transition metal oxides -TMO- (TiO_2, ZnO, Ta_2O_3 and HfO_2) and perovskites ($BiFeO_3$)[62]. Among all TMO-based memristors, hafnium oxide (HfO_2) has been suggested as a promising material owing to its excellent performance in demonstrating a proper trade-off between key requirements of the next-generation memory technology[55]. The challenge of implementing HfO_2 in industries is considered to be high fluctuation of switching parameters such as set/reset voltage (V_{set}/V_{reset} and the current level of HRS and LRS (I_{HRS}, I_{LRS}) which is generally addressed as variability issue.



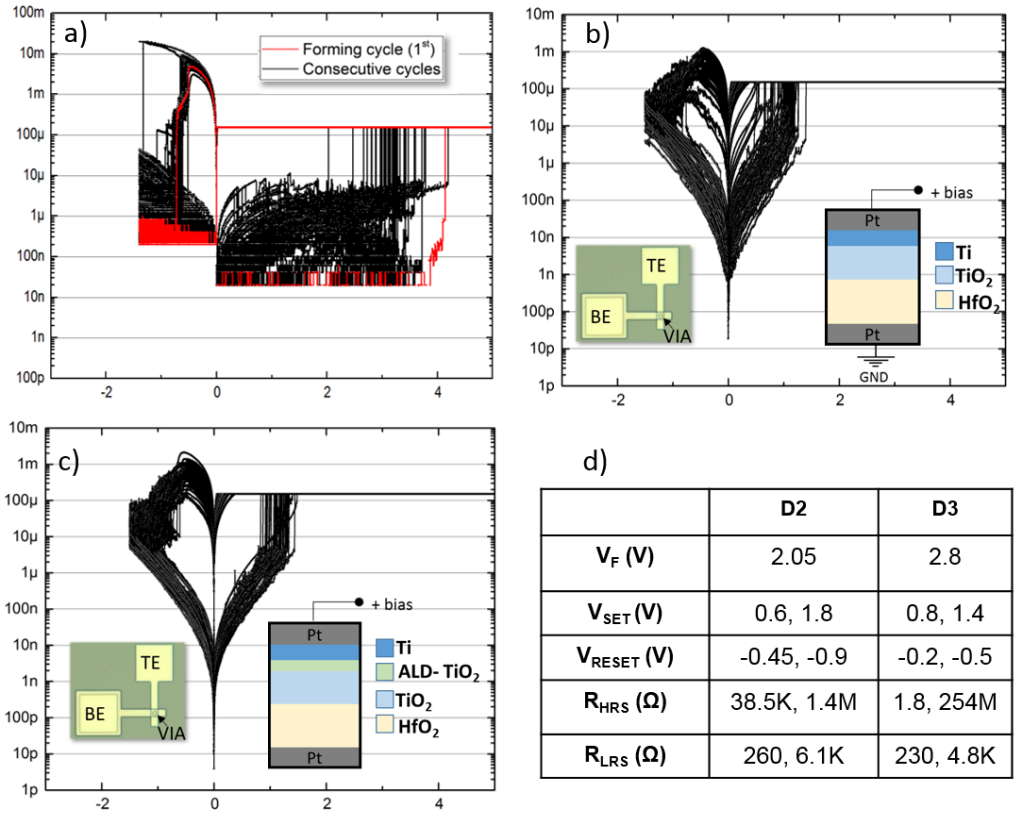
b)

ID.	Device Configuration (nm)
D1	Pt(BE)/HfO_2(5)/Pt(TE)
D2	Pt(BE)/HfO_2(5)/TiO_2(3)/Ti(3)/Pt(TE)
D3	Pt(BE)/HfO_2(5)/TiO_2(3)/TiO_2 (ALD-2)/Ti(3)/Pt(TE)

Figure 10.1 – a) Brief schematic demonstration of process flow, b) device name and configuration.

Moreover, HfO_2 is generally implemented by atomic layer deposition (ALD) tool as it provides highly uniform metal-oxide with accurate stoichiometric. However, the low density of defects such as oxygen vacancies for the as-fabricated devices necessitates the use of higher operation voltage followed by performance degradation[39][18].

Introducing oxygen vacancies to the as-fabricated memories is considered as a propitious solution effective in lowering the forming voltage (V_f), V_{set} and V_{reset}. Hence, implementation of bi-oxide memristors using relatively active reactive metal such as Ti, Ta, Hf as oxygen reservoir has been proposed as a promising solution to overcome the variability issue of memristors[76][71]. Even though structure engineering seems to be a proper solution, however, the sur-



	D2	D3
V_F (V)	2.05	2.8
V_{SET} (V)	0.6, 1.8	0.8, 1.4
V_{RESET} (V)	-0.45, -0.9	-0.2, -0.5
R_{HRS} (Ω)	38.5K, 1.4M	1.8, 254M
R_{LRS} (Ω)	260, 6.1K	230, 4.8K

Figure 10.2 – I-V characteristics for a) D_1, b) D_2. Inset shows the distribution for sets and resets, c) D_3, and d) summary of key switching parameters for D_2 and D_3. The bottom left insets in the parts b, and c shows the microscopic image of the final fabricated device with TE and BE pads and the vias formed between them. The insets in the bottom right for part b and c schematically demonstrate the biasing methods for the fabricated devices.

face/bulk properties of oxides could be affected by the PVD plasma used for later deposition of oxygen reservoir or the secondary oxides. Moreover, the probable penetration of sputtered metallic atoms which can cause performance degradation by excessive formation of oxygen vacancies[49][24].

In this work, we studied the electrical characteristics of HfO_x/TiO_y bi-oxide memristors with an additional ALD deposited TiO_2 layer in the TiO_y/Ti interface to protect the oxides. It has been shown that the addition of an ultra-thin layer of TiO_2 (2 nm) with ALD, significantly improved the cycle-to-cycle variation issue.

10.2 Materials and Methods

10.2.1 Device Fabrication

In this work, the switching materials had been deposited vertically stacked between the top and bottom electrodes (TE, BE) inside "via"s. 100 nm Pt bottom electrode (BE) was deposited using DC sputtering on 4" Si/SiO_2 test wafers with a thin layer of Ti as the adhesion layer. The BE was patterned with the conventional lithography and reactive ion etching system (Cl_2/Ar chemistry). Next, 100 nm LTO was grown using LPCVD tool at 425°C as the passivation layer to separate the top and bottom electrode. The vertical vias (1-10 μm) have been patterned through the LTO layer using lithography; followed by a wet etch step in the buffered hydrofluoric acid (BHF) at 20° C. Atomic layer deposition (ALD) has been used at 200°C with TEMAH and H_2O precursors for HfO_x, also $TiCl_4$ and H_2O for TiO_2. Next, Ti layer sputtered using DC sputtering (Ar: 9 sccm), continued with deposition of Pt as the TE without breaking the vacuum to avoid further oxidation of metallic layer of Ti. The Pt top electrode (TE) has been deposited and patterned as described earlier for the BE step. Figure10.1 shows an overview of fabrication steps, while Fig.10.1b presents the structure of the devices with their short names to address them.

10.2.2 Electrical Measurement

We used an Agilent B1500 semiconductor parameter analyzer for electrical characterization of all devices. The biases were applied to the TE while the bottom electrode was grounded throughout the measurement (see the insets of part b,c of Figure.10.2). A compliance current (IC) of 150 μA was applied to the devices to protect them against hard breakdown during the measurements.

10.3 Result and Discussion

Fig. 10.2 (a,b,c) demonstrate the electrical behaviour of D_1, D_2 and D_3 devices under 100 consecutive dc sweeps. The DC measurements started with the application of positive voltage

to the TE, which all devices appeared to be highly resistive. When the first positive bias or forming voltage (V_f) was high enough, the resistance of the devices suddenly decreased, and the current reached to the IC value (here 150 μA). The voltage swept as: (0 to 5), then (5 to 0), next (0 to -1.5) and finally (-1.5 to 0) V. It can be clearly seen in the Fig.10.1a which D1 (HfO_2-only) has shown wider distribution of key switching parameters comparing to the two bi-oxide device (Fig.10.1a vs Fig.10.1b,c).

The D_2 has already shown significant performance improvement comparing to HfO_2-only (D_1) device due to its configuration (HfO_x/TiO_y/Ti), with significantly lower operating voltage and resistance level. Even though the D_2 comparing to D_1 owned an extra oxide layer, but required lower V_f and V_{set} to operate, which is assumed to be not only because of implementing the buffer layer, but also and the side effect of plasma treatment of the oxide layers during PVD deposition of Ti which led to uncontrolled creation of oxygen vacancies. Figure10.3 exhibits the cumulative probability of resistance for $D_2$and D_3 for set and reset read at 0.25 V. We realized the D_3 demonstrated better switching performance with tightest variation comparing to D_2 and D_1. Moreover, the D_3 required higher V_f and operated with around three times larger switching window (R_{LRS}/R_{HRS} read @ 0.25V) which is expected to be due to the insertion of a thin layer of TiO_2 layer using ALD tool. The ALD deposited TiO_2 protected the switching materials against Ti metal deposition while maintaining the capability of harvesting oxygen for the buffer layer, resulted in a uniform switching distribution throughout cycling without degradation of switching window (Inset of Fig.10.2c).

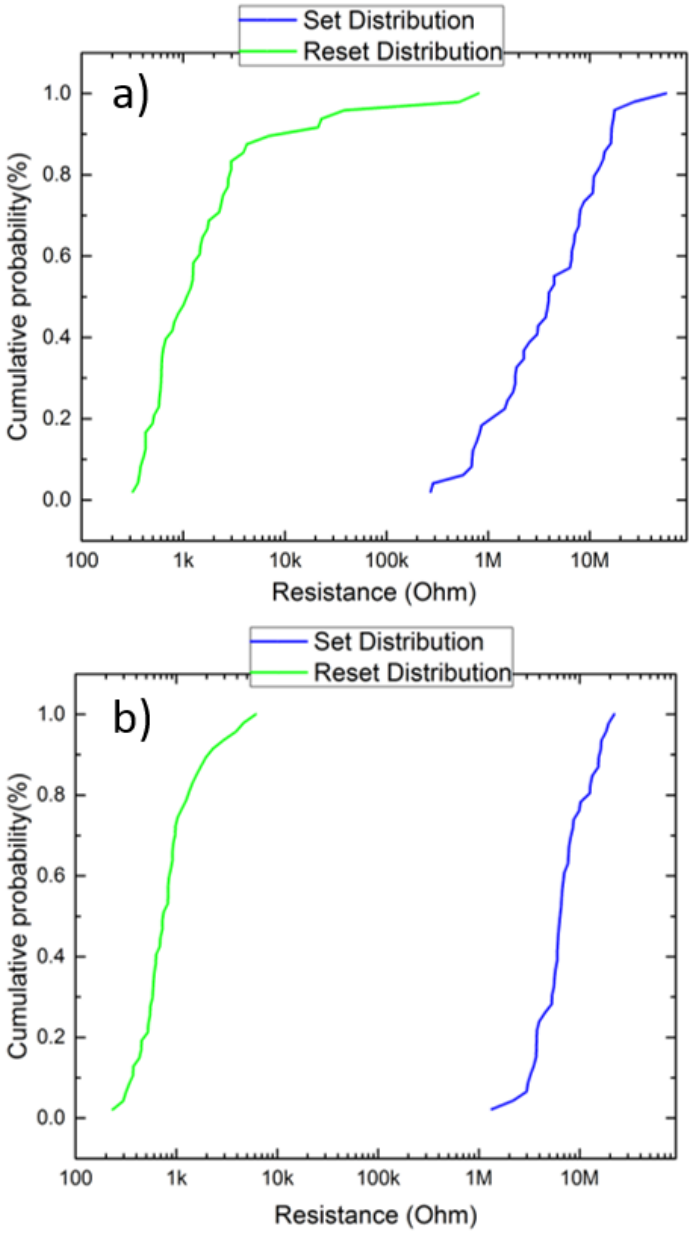


Figure 10.3 – Cumulative distributions of resistance (set and reset) for a) D_2, b) D_2.

10.4 Conclusion

In this study, we studied the effect of insertion of an extra buffer on switching properties of a HfO_2-based memristors. A novel $HfOx_x$-based memristor owing an ALD deposited TiO_2 between Ti and its oxide layer was proposed as a solution to the large variation in switching parameters. We further explained this improvement by the role of ALD deposited TiO_2 oxide layer in limiting penetration of the Ti metal during sputtering and protecting the quality of the oxide against the PVD plasma. The penetration of Ti metal and the plasma damage creates uncontrolled oxygen vacancies, which eventually degraded memristor performance and caused the reliability issue. This simple but yet effective method significantly improved the C2C uniformity of switching parameters and resulted in a more reliable resistive switching characteristics with larger switching window.

A Future Work

The reliability has been considered as the main hurdle in the commercializing of ReRAM technology, as it results in poor uniformity of cycle-to-cycle (C2C) and device-to-device (D2D) in the large scale manufacturing. The high forming voltage has been identified as a significant problem in the ReRAMs together with the wide distribution of resistance levels, set and reset voltages.

One effective approach to control the reliability issue is considered to be ion implantation, metal ions with larger electro-negativity than Hf metal are recommended. In this work, different thickness of Al-doped HfO_2 and several ratios of Al:HfO_2 have been tested and appeared to be remarkably effective in lowering the forming voltage and improving the uniformity. Further researches (including the material characterization techniques)are required to achieve a consistent understanding of the switching mechanism. It is recommended to check the effect of doping HfO_2 with elements such as Ti, Al, and Zn.

The ion penetration of secondary oxide limiting penetration of the Ti metal during sputtering and protecting the quality of the oxide against the PVD plasma.

Another factor which needs to be intensively studied is the surface/bulk properties of oxides, which can be profoundly affected by the PVD plasma used for later deposition of oxygen reservoir or the secondary oxides. Moreover, the probable penetration of sputtered metallic atoms, which can cause performance degradation by excessive formation of oxygen can enhance the variation in the switching parameters. In this work, we have implemented a thin ALD deposited layer of TiO_2 and observed a noticeable improvement in the device performance. Further researches are encouraged to study the effect of ALD deposited layer in protecting HfO_2 oxide layer and optimize the required thickness layer for this effect.

I would like to suggest the continuation of the 3D 1S1R work presented in chapter 9 of this work.

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BEHNOUSH ATTARIMASHALKOUBEH

Lgernstrasse 11, 8303 Bassersdorf, Switzerland
+41 789 54 3610 ⋄ Behnoush.attari@gmail.com

EDUCATION

Ecole Polytechnique Fdrale de Lausanne, Switzerland *September 2015-2019*
Ph.D degree
Department of Microsystems and Microelectronics
Microelectronic Systems Laboratory (LSM)
Thesis advisor: Prof. Yusuf Leblebici

Pohang University of Science and Technology, South Korea *September 2012 - 2014*
Master degree
Department of Material Science and Engineering
Semiconductor Integrated Device Process Labratory (SIDP)
Thesis advisor: Prof. Hyunsang Hwang

University of Tehran, Iran *November 2005 - 2010*
Department of Material Science and Engineering
Thesis advisor: Prof. Abbas Zarei- Hanzaki

PUBLICATIONS

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- *Effect of Hf metal layer on the switching characteristic of HfOx-based Resistive Random Access Memory*, **B. Attarimashalkoubeh**, J. Sandrini, E. Shahrabi, Y. Leblebici, Ph.D. Research in Microelectronics and Electronics (PRIME), July 2016, Lisbon, Portugal. This work awarded with a Silver leaf medal.

- *Chip-level CMOS co-integration of ReRAM-based non-volatile memories*, E. Shahrabi, J. Sandrini, **B. Attarimashalkoubeh**, Y. Leblebici, Ph.D. Research in Microelectronics and Electronics (PRIME), Jul 2016, Lisbon, Portugal.
- *"Ultrathin Two-dimensional Polymer Film for Non-Volatile Resistive Memory Application"*, I. Roy, **B. Attarimashalkoubeh**,Raghunandan Hota, Kangkyun Baek, Wooseup Hwang, Sandro Kappert, Artem Fedyay, Amit Prakash, Dimitry A. Ryndyk, Gianaurelio Cuniberti, Hyunsang Hwang, Kimoon Kim, 11th The international Symposium on Macrocyclic and Supermolecular Chemistry (ISMCE), July 2016, Seoul, Korea.
- *Toward Chip-Level ReRAMs-CMOS Co-Integration*, E. Shahrabi, J. Sandrini, **B. Attarimashalkoubeh**, Y. Leblebici, International Conference on Memristive Materials, Devices Systems (MEMRISYS 2017), Apr 2017, Athens, Greece.
- *Novel 3D Architecture of 1S1R*, **B. Attarimashalkoubeh**, Y. Leblebici, 15th IEEE/ACM International Symposium on Nanoscale architectures (NANOARCH), Qingdao, China, July 2019.
- *In-depth Structural and Electrical Characteristics Study of HfOx -based resistive Random Access Memories(ReRAMs)*, **B. Attarimashalkoubeh**, Y. Leblebici, 31st IEEE International Conference on Microelectronic(MIEL), Nis, Serbia, September 2019, Accepted.
- *Relationship between the Gibbs free energy of oxidation with the resistive switching properties of bi-oxides memristors*, **B. Attarimashalkoubeh**, I. Krawczuk, P. Muralt, Y. Leblebici, 8th International symposium on Next-Generation Electronics (ISNE), October 2019, Zhengzhou, China, Accepted.
- *Improving reliability issue of HfO2-based memristors by protecting the switching materials against buffer layer deposition*, **B. Attarimashalkoubeh**, Y. Leblebici, 14th IEEE Nanotechnology Materials and Devices Conference (NMDC), October 2019, Stockholm, Sweden, Accepted.
- *In-depth Material and Electrical study of improvement in switching performance of HfO_2-based ReRAM through material optimization*, **B. Attarimashalkoubeh**, M. Mensi, P. Muralt, Y. Leblebici,In preparation.
- *Electrical study and compact modeling of bi-layer HfO_2-based Resistive Random Access Memory (ReRAMs)*, **B. Attarimashalkoubeh**, Y. Demirag, I. Krawczuk, P. Muralt, Y. Leblebici, In preparation.

AWARD AND HONORS

- **Silver leaf for presenting in IEEE PRIME conference**, Lisbon, Portugal, 2016
- **Keynote speaker international Conference on Memristive Materials**, Devices, Systems (MEMRISYS): Athens, Greece, 2017
- **Peer reviewer of manuscripts for Electron Device Letters**, IEEE (EDL): Since 2013