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H-terminated polycrystalline diamond p-channel transistors on GaN-on-Silicon

Reza Soleimanzadeh, Mehdi Naamoun, Riyaz Abdul Khadar, Remco van Erp, Elison Matioli

***Abstract*—In many semiconductor technologies, including GaN, the lack of p-channel devices is a major obstacle for complementary operations. Here, we demonstrate high-performance polycrystalline diamond p-channel transistors on GaN-on-Si. Following the optimization of the microwave-plasma chemical-vapor-deposition of diamond on GaN, the polycrystalline layer was hydrogenated to form a 2D hole-gas at the surface, acting as p-channel. Relying on a rather simple fabrication process, these devices exhibited excellent electrical and thermal performances with on-off ratio of 10^9, breakdown voltage of 400 V, specific on-resistance of 84 mΩ·cm^2, and thermal conductivities higher than 900 W/m·K. The presented hetero-integration technology provides a promising platform for future complementary logic operations, gate drivers, complementary power switch applications such as integrated power inverters and converters, simultaneously serving as a very efficient thermal management solution in high power density applications.**

***Index Terms* – Diamond, Hydrogen terminated, P-channel, GaN, Si, CMOS, 2DHG**

I. Introduction

Diamond is a very promising material for power electronic applications due to its excellent material properties, such as large critical breakdown field, extremely high thermal conductivity and high hole mobility, resulting in a high Baliga's figure of merit (BFOM) [1]. Hydrogen-terminated diamond transistors (HTDTs) have been demonstrated on both monocrystalline and polycrystalline diamond substrates, in which a 2D hole-gas (2DHG) acts as the p-channel [2], with promising electrical characteristics for high power applications [3]–[6]. Here, we demonstrate for the first time p-channel transistors on hydrogen-terminated polycrystalline diamond deposited over AlGaN/GaN-on-Silicon by a simple and cost-effective method. After optimizing the layer quality and grain size, the fabricated devices presented excellent electrical and thermal properties with high on-off ratio, low specific on-resistance ($R_{on,sp}$), high breakdown voltage as well as low thermal resistance. This demonstration opens interesting opportunities for future integration of these p-channel devices with n-channel GaN transistors for complementary switch applications.

II. Device Structure and Fabrication

AlGaN/GaN-on-Si substrates were used as templates for the diamond depositions to demonstrate the possibility of diamond integration with GaN-based high-electron-mobility-transistors (HEMT) using AlGaN/GaN heterostructures. An extensive optimization procedure was performed for parameters such as interlayers, seeding method, microwave power, substrate temperature, operating pressure as well as the gas mixture including methane, nitrogen and argon. Prior to the deposition, a layer of SiN/Si (30 nm/5 nm) was deposited to protect the AlGaN/GaN surface during the harsh diamond deposition environment, to enhance the adhesion of diamond to the substrate, and to reduce the thermal boundary resistance (TBR) between GaN and diamond [7]. The substrates were seeded using a mixture of isopropanol and diamond nanoparticles, with an average grain size of 1 to 150 µm, in an ultrasonic bath for one hour. The SiN/Si interlayer and the seeding process were essential to obtain uniform and well-adhered seed layers, which allowed a rapid initial diamond deposition, maintaining strong adhesion during the deposition and after cooling down to room temperature.

The diamond deposition was performed in a microwave-plasma chemical-vapor-deposition (MPCVD) reactor at 800 °C, plasma power of 3.5 kW, working pressure of 140 mbar, and with 5% methane. A small amount of nitrogen and argon (few ppm) were intentionally added during the growth to keep the growth rate as high as possible (> 1 µm/h), and the highest gas purity (9N) was used to obtain high quality diamond layers.

Afterwards, the diamond surfaces were hydrogenated by a 2.8 kW hydrogen plasma at 100 mbar at a substrate temperature of 640 °C for 45 min. A 200 nm-thick gold layer was deposited to form ohmic contacts. Then, a KI+I_2 solution was used to remove gold around the devices and an 800 W oxygen plasma was used to isolate the devices. An 80 nm-thick Al_2O_3 was deposited by atomic layer deposition (ALD) at 200 °C to serve as gate oxide and surface termination. Finally, a 300 nm-thick layer of Al was deposited as the gate metal and patterned using a Cl_2/BCl_3 plasma.

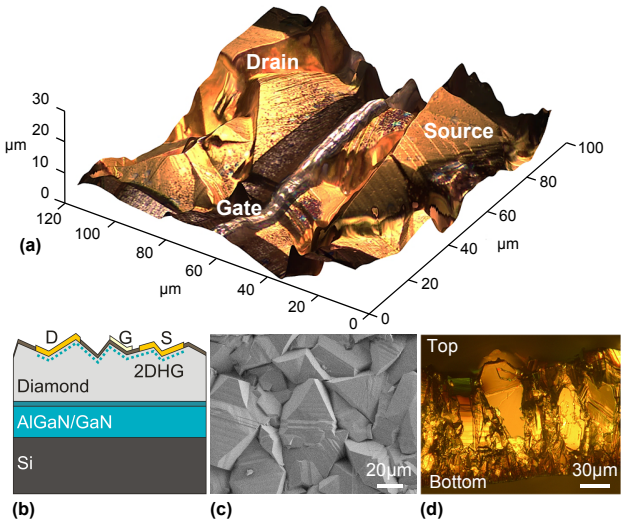

Fig. 1 (a) 3D optical microscope image of the fabricated HTDT, constructed using focus stacking method. (b) Schematic of the structure of HTDTs. (c) Top-view SEM image of the diamond surface. (d) Cross-sectional optical microscope image of the diamond layer showing larger grain sizes at the top.

This work was supported in part by the European Research Council through the European Union's H2020 Program/ERC under Grant 679425. R. Soleimanzadeh, R. A. Khadar, R. van Erp, and E. Matioli are with the Power and Wide-Band-Gap Electronics Research Laboratory (POWERlab), École Polytechnique Fédérale de Lausanne (EPFL), 1015 Lausanne, Switzerland (e-mail: reza.soleimanzadehardebili@ epfl.ch; elison.matioli@epfl.ch). M. Naamoun is with LakeDiamond SA, 1015 Lausanne, Switzerland.

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III. Results And Discussion

The 3D optical microscope image and schematic of the device structure are shown in Fig. 1 (a) and (b). The scanning electron microscope (SEM) image in Fig. 1 (c) shows pyramid-like crystallites with smooth {111} facets [8], dominating the top surface of the diamond layers with an average grain size of 34 µm, which is much smaller than that of commonly used in the literature (>100 µm). The cross-sectional image of the diamond layer in Fig. 1 (d) shows the very small grains at the bottom, where the growth initiated, and gradually enlarged across the 130 µm-thick layer towards the top side where the devices are fabricated. The hydrogenated diamond surface presented a hole-density of 10^{14} cm^{-2} and mobility of 1.3 cm^2/V.s from Hall measurements, resulting in a sheet resistance of about 50 kΩ/sq.

The existence of many pits and edges in the unpolished diamond surface, serves as activation sites, resulting in a higher carrier density compared to the commonly reported values in the literature [9]. The carrier mobility is strongly affected by the ionized impurity scattering in diamond 2DHGs due to the small distance between the hole-channel and negative charges in the oxide [1], [10]. For similar hole density of 10^{14} cm^{-2}, single-crystalline diamond presented mobilities as low as 3 cm^2/V.s [11], which in the present case were even lower due to the small diamond grains in the polycrystalline layer and the rougher surface.

The transfer characteristics of a fabricated transistor with source-to-gate length (L_{SG}) of 2µm, gate length (L_G) of 4 µm and gate-to-drain length (L_{GD}) of 8 µm revealed normally-on p-channel transistor behavior with excellent gate control with on-off ratio as high as 10^9 (Fig. 2 (a)).

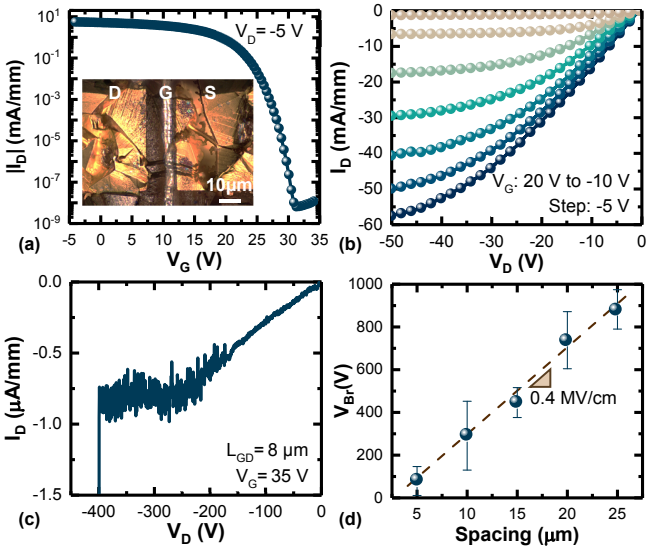

Fig. 2 (a) Transfer characteristic of a transistor with a L_G of 4 µm at a drain bias of -5 V. The inset shows the optical microscope image of the device. (b) Output characteristic of the same device at gate biases from 20 V to -10 V with voltage steps of -5 V. (c) Off-characteristic of the device at V_G of 35 V, showing a breakdown voltage of -400 V and very low leakage current. (d) Lateral breakdown characteristic of the diamond layer at different electrode spacing, showing a critical breakdown electric field of 0.4 MV/cm.

The output characteristic of the device shows current densities as high as -60 mA/mm, as well as a low $R_{on,sp}$ of 84 mΩ·cm^2 (Fig. 2 (b)). Fig. 2 (c) shows excellent off-state characteristics with very low leakage currents, below 1 µA/mm near the device breakdown.

The relatively high breakdown voltage (V_{Br}) of -400 V indicated the high quality of the CVD diamond layer. The lateral breakdown was further studied using isolated pads with different spacing (Fig. 2 (d)). Assuming a uniform electric field distribution between the pads, a critical electric field of 0.4 MV/cm was determined, which is comparable to 1 MV/cm reported for lateral breakdown field in monocrystalline diamond [12]. Besides good electrical performance, high thermal conductivity of these diamond layers is very important. As shown in Fig. 3 (a), the grain size of the polycrystalline diamond layer increases with its thickness, resulting in higher thermal conductivities. The effective in-plane thermal conductivity of the diamond layers was measured using fabricated membrane structures as shown in Fig. 3 (b), by a similar technique presented in [13], where parts of the Si substrate were removed and a resistive heater was deposited at the center of the membrane.

The thermal measurements were performed using a Quantum Focus Instruments (QFI) IR microscope with a 512 by 512 pixels array, a 20x-magnification lens and filters, providing high spatial resolution and accuracy. The IR microscope was equipped with a precise thermal stage, which enabled an accurate emissivity correction using two-temperature emissivity calculation method as well as the factory-provided calibration data. The surface of the chips was coated with black paint to avoid the errors due to the IR transparency of the layers and to increase the emissivity of the surface. Effective lateral thermal conductivity of about 900 W/m·K was measured for layers with grain sizes of 3 µm. Such excellent thermal conductivities can lead to very low thermal resistance and robust electrical performances in the high power density applications. Moreover, this shows the potential of such high-quality CVD-deposited diamond layers for efficient thermal management of high power GaN devices [14]–[18].

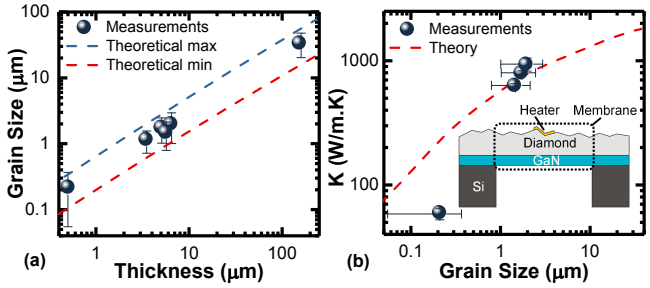

Fig. 3 (a) Grain size at the top side of diamond layers at different thicknesses. The symbols are from measurements and the dashed lines using theoretical values from [19]. (b) Lateral thermal conductivity of diamond layers with different grains size. The symbols are experimental results and the dashed line is the theoretical thermal conductivity from [20]. The inset shows a cross-sectional structure of the membranes fabricated to measure the effective in-plane thermal conductivity of diamond.

In Fig. 4, the electrical characteristics are benchmarked against other HTDTs in the literature, based on monocrystalline diamond [5], [12], [21], [22], polycrystalline diamond [4], [23], and polycrystalline diamond on SiC [6]. This work represents the first HTDT on GaN-on-Si substrates, demonstrating similar high power device figure of merit (BFOM = 2.5 MW/cm^2) compared with other HTDTs on polycrystalline and even some on monocrystalline diamond. However, there is still a gap

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between the performance of current HTDTs and their theoretical limits, which highlights the significant potential for improvement of this technology.

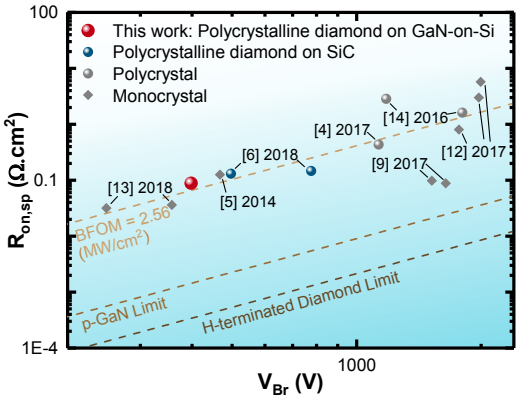

Fig. 4 Benchmark of the specific-on resistance ($R_{on,sp}$) and breakdown voltage (V_{Br}) of this work with other heteroepitaxial (on SiC), as well as polycrystalline and monocrystalline HTDTs.

Moreover, the HTDTs in this work present a much superior performance compared to state-of-the-art p-channel GaN transistors, achieving 6-times higher current density, 4-orders of magnitude higher on-off ratio and more than 6-times higher thermal conductivity [24]–[26]. The much larger theoretical BFOM of HTDTs compared to that of p-channel GaN (Fig. 4) and the ease of integration with n-channel GaN transistors open a pathway for future complementary power switch and logic applications.

IV. Conclusions

In this work, polycrystalline diamond layers were deposited on GaN-on-Si substrates to demonstrate H-terminated diamond p-channel transistors. The fabricated devices showed a high on-off ratio of 10^9, high current density of 60 mA/mm, low on-resistance of 84 mΩ·cm^2 as well as high breakdown voltage of 400 V, resulting in a BFOM similar to those on polycrystalline and monocrystalline diamond reported in the literature. High thermal conductivities measured up to 900 W/m·K in these diamond layers lead to low thermal resistances, and can be utilized for the thermal management of the GaN devices in high power density applications. The devices in this work significantly outperform the state-of-the-art p-channel GaN devices, electrically and thermally, providing new opportunities for complementary logic operation, gate drivers and complementary power switches by the integration of p-channel diamond devices with n-channel GaN devices.

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