

# A Fully Integrated State-of-the-Art Analog SiPM with on-chip Time Conversion

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**Abstract** - In this work, we present a complete design implementation and characterization of an analog silicon photomultiplier (SiPM) with integrated time-to-digital converter (TDC). The combination of a photodetector together with on-chip readout circuitry in close proximity enables system-level advantages such as internal parasitic reduction for better single-photon timing resolution (SPTR), but also overall simplicity and compactness. The system comprises a C-Series analog SiPM developed by SensL, a TDC, and a comparator. The design was implemented in  $0.35\mu\text{m}$  CMOS technology. The proposed analog SiPM features 48% photon detection efficiency (PDE) at 420nm wavelength and +6.0V excess bias. Thanks to the small size of the electronics, the overall sensor fill factor is 75% and its sensitive area is  $3\times 3\text{mm}^2$ . The SiPM fast output, which is a specialized terminal for fast timing output signals, has a parasitic capacitance of about 12pF. The TDC is a multi-path-gated ring oscillator with a 6-bit coarse counter and 9-bit phase detector. Post-layout simulation results indicate a 65ps LSB in typical corner with differential non-linearity (DNL) and integral non-linearity (INL) of  $\pm 0.55\text{LSB}$  and  $\pm 1\text{LSB}$ , respectively. The comparator is composed of two preamplifier stages followed by a complementary self-biased differential amplifier stage (CSDA), directly coupled to the fast output through a capacitor. Post-layout simulation indicates 48V/ns slew rate and a preamplifier stage bandwidth of ~1GHz. The comparator power consumption without the additional preamplifier stage is  $198\mu\text{W}$ .

**Index Terms**—Silicon photomultiplier, SiPM, TDC, time-to-digital converter, comparator, CSDA, fast output.

## I. INTRODUCTION

DURING the last decade, SiPMs have shown to be an effective replacement of photomultiplier tubes in fast timing and/or high magnetic field applications, such as time-of-flight positron emission tomography (ToF-PET), PET/MRI [1]. SiPMs are compact photon-counting detectors that operate at relatively low bias voltage, exhibit low noise and good timing resolution, while being insensitive to magnetic fields. PET is one of the applications in which SiPMs are most useful, especially with the trend towards integrating PET-MRI systems together. Several studies over the past decade proposed developments in PET systems based on SiPM detectors both for human and small animal imaging [2] [3]. Apart from medical applications, current research focuses on SiPMs as highly

sensitive photon counting detectors for LiDAR systems [4] [5].

Analog (A-SiPMs) are composed of an array of single-photon avalanche diodes (SPADs), whose output currents are summed up into one node and the output pulse is processed using off-chip circuitry. The main drawback of this approach is the large capacitance of the output path, which degrades timing performance. A capacitive decoupling at SPAD level (fast output concept) mitigates this degradation, while an even larger effect is achieved by integrating the timing circuitry (comparator and TDC) in a system on-chip. The low-capacitance connection results in minimal timing degradation with the added benefit of a purely digital output.

This work presents the implementation and characterization of a state-of-the-art system, which performs the digitization (capacitive decoupling, comparison and conversion on-chip) of the C-Series A-SiPM's fast output. Further expansion onto a high-granularity system with multiple TDCs to achieve a multi-channel digital SiPM (MD-SiPM) is envisioned.

## II. SYSTEM ARCHITECTURE

The system block diagram is depicted in Fig. 1. The fast output of the C-series SiPM is connected to the integrated comparator through AC coupling (not shown in the figure), and threshold voltage  $V_{th}$ , which is externally controlled. The comparator's output is connected to a multiplexer that selects between the comparator's output and an external electrical trigger to act as the TDC's start signal. In contrast, the STOP signal is always generated externally by an FPGA. A trigger validation signal called FLAG is generated from an SR latch. The FPGA starts a readout phase only if the FLAG signal is

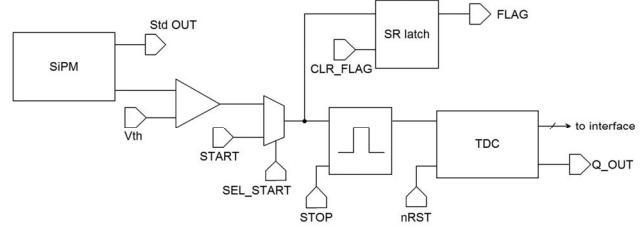


Fig. 1. System architecture block diagram – A-SiPM, integrated comparator and TDC.

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active during the measurement cycle. Also, by using the Q\_OUT signal, the TDC range can be further extended on the FPGA through the use of an additional counter, if necessary. The StdOUT signal represents the standard SiPM output, which is externally available for energy measurements. The standalone TDC design and post-layout functionality have been extensively characterized in [6].

The Asynchronous comparator is based on a near-threshold topology [7]. A preamplifier stage, as shown in Fig. 2a is added before the actual comparator, in order to increase the relative threshold sensitivity. The actual comparator comprises two stages: the first stage (Fig. 2b) is a self-biased preamplifier, which is a modified version of the CSDA that is able to operate in near threshold regions [7] [8], while the second stage (Fig. 2c) consists of a conventional CSDA followed by inverter stages. The CSDA is composed of two complementary differential amplifiers. This structure approximately doubles the gain compared to a conventional differential amplifier. The comparator's post-layout simulation results indicate 48V/ns slew rate and that the preamplifier stage has a bandwidth of  $\sim$ 1GHz. The comparator power consumption without the preamplifier stage is  $198\mu$ W. Post-layout simulation results are presented in Fig. 3 and Fig. 4.

### III. CHARACTERIZATION

The system was tested in post-layout mode using extensive mixed-signal simulations in the Virtuoso AMS environment, so as to verify that the entire SiPM-comparator-TDC chain works under the design specifications. The sample TDC will be completely characterized in terms of timing resolution, TDC nonlinearities, and power consumption. Comparator parameters such as: slew rate, bandwidth, power consumption will be measured, after which the entire system (SiPM included) will be tested in PET and LiDAR setups. The chip micrograph is shown in Fig. 5.

### IV. CONCLUSION

We implemented and are currently characterizing a fully functional system-on-chip dedicated to fast timing with SiPMs. We verify the integration of high-speed electronics into an optimized CMOS processes for A-SiPMs. We have achieved a compact photosensor with state-of-the-art PDE, in addition to fast electronics in a monolithic chip with minimal parasitic degradation for digital timestamping. The output of the circuit is backward compatible with the C-series SiPM.

### V. FUTURE RESEARCH

Future research will focus on developing higher-granularity timestamping and faster TDCs. Comparator optimization in terms of area and power consumption will be further investigated. 3D ICs represent a very attractive alternative due to the possibility of using an optimized sensor technology integrated with advanced technology nodes. This will lead to further increase in on-chip processing capability.

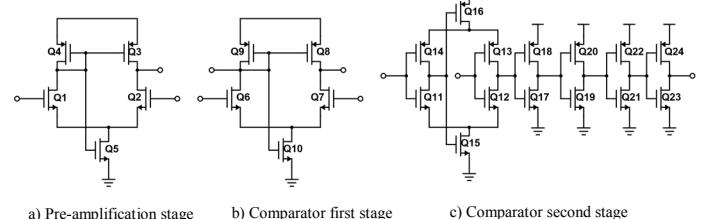


Fig. 2. Comparator architecture [7].

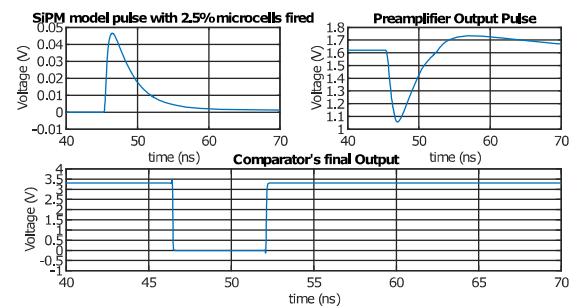


Fig. 3. Preamplifier output pulse and comparator's final output.

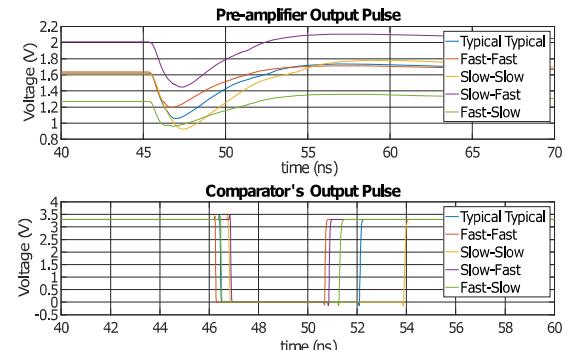


Fig. 4. Preamplifier output pulse and comparator's final output for all five corners.

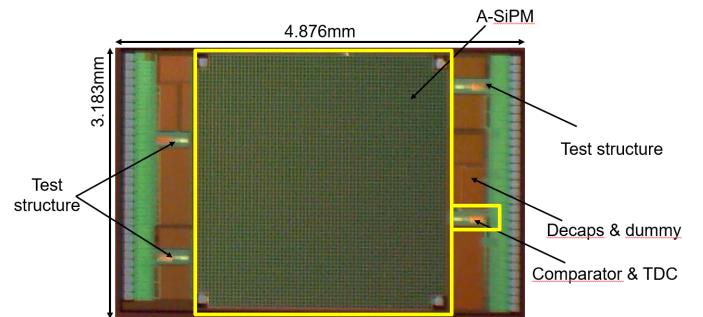


Fig. 5. Chip micrograph. The SiPM is surrounded by the TDC, additional test circuitry, and decoupling capacitors.

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