Auxiliary submodule power supply for a medium voltage modular multilevel converter

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Auxiliary Submodule Power Supply for a Medium Voltage Modular Multilevel Converter

Alexandre Christe, Marko Petkovic, Ignacio Polanco, Milan Utvic, and Drazen Dujic

Abstract—The auxiliary submodule power supply is a vital component of a modular multilevel converter submodule or any multi-submodule converter. Considering the high isolation requirements and difficulties to provide power from the ground potential, the auxiliary submodule power supply must be simple, work reliably and not compromise the submodule's reliability. A flyback supply from the submodule's dc link with multiple sets of isolated secondary windings solves at once the low-voltage generation and the required voltage isolation for semiconductor gate circuits and protection without need for an externally supplied low-voltage input to the submodule (high-isolation connection). This paper presents an isolated, flyback-based auxiliary submodule power supply with planar magnetic, printed circuit board integrated windings and multiple isolated outputs for a medium voltage modular multilevel converter as well as detailed electrical and magnetic mathematical modelling, technological integration challenges description and proper experimental test considerations.

Index Terms—Auxiliary submodule power supply (ASPS), flyback, modular multilevel converter (MMC), planar transformer.

NOMENCLATURE

V_{sm}	Submodule voltage.
L_p	Flyback transformer primary inductance.
I_p	Primary peak current.
D	Duty cycle.
f_{sw}	Switching frequency.
N	Turns number.
μ_0	Permeability in vacuum.
μ_r	Relative permeability.
$\mathcal{R}$	Magnetic reluctance.
l_{ag}	Air-gap length.
V_{DS}	Drain to source voltage.
V_L	Voltage spike due to the leakage inductance.
V_D	Rectifier diode forward voltage drop.
$R_{load,eq}$	Equivalent load resistance.
$C_{out,eq}$	Equivalent output capacitance.
R_{ESR}	Equivalent series resistance.

I. INTRODUCTION

The modular multilevel converter (MMC) is being considered as the most promising technology in the medium-voltage high-power conversion field. Desirable characteristics such as modularity, scalability, high efficiency and outstanding harmonic performance are achieved by means of the connection of a large number of low-voltage rating submodules (SMs). In recent years, at MMC system level, modulation techniques, modelling and control strategies have been the main topics for specialized researchers and industry. Less attention has been paid to the submodule (SM) level since, in most cases, it is a simple and well known topology. Nevertheless, in a real implementation, the SM is a complex and challenging integration of 1) a half or full IGBT-based power bridge, their gate drivers and dc bus capacitors, 2) a hardware-level over-voltage and over-current circuit detection and their bypass circuit, 3) critical voltage, current and temperature measurements, 4) a control unit to perform analog-to-digital conversions, control actions, monitoring and upstream communication protocols, and 5) an auxiliary submodule power supply (ASPS) to supply with a low voltage each component. In this sense, ASPS's technological selection along with designing, manufacturing and testing process must receive particular attention since high voltage isolation requirements have to be achieved among other critical characteristics as reliability, safety, practicality, efficiency and cost-effectiveness.

Solutions such as tapped-inductor buck converter with one or multiple series connected switches in the high-voltage side and a single non-isolated output are presented in [1] and [2] respectively. Additional components are needed in multi-switch topologies in order to synchronize their operation. Conversely, an isolated and centralized external power supply based on a LLC resonant converter is presented in [3] with the starting-up possibility from de-energized converter. Widely used, isolated and non-centralized internal power supply solutions based on flyback converters are popular choices. For instance, [4] presents a common flyback design to address high voltage power electronics device supply. [5] shows a two-switches flyback power supply for a 1300 V SM input voltage, where proper switches synchronization has to be addressed to avoid voltage stress and voltage oscillations across them. [6] shows a high voltage input auxiliary power supply based on a two stages cascade flyback converter. The
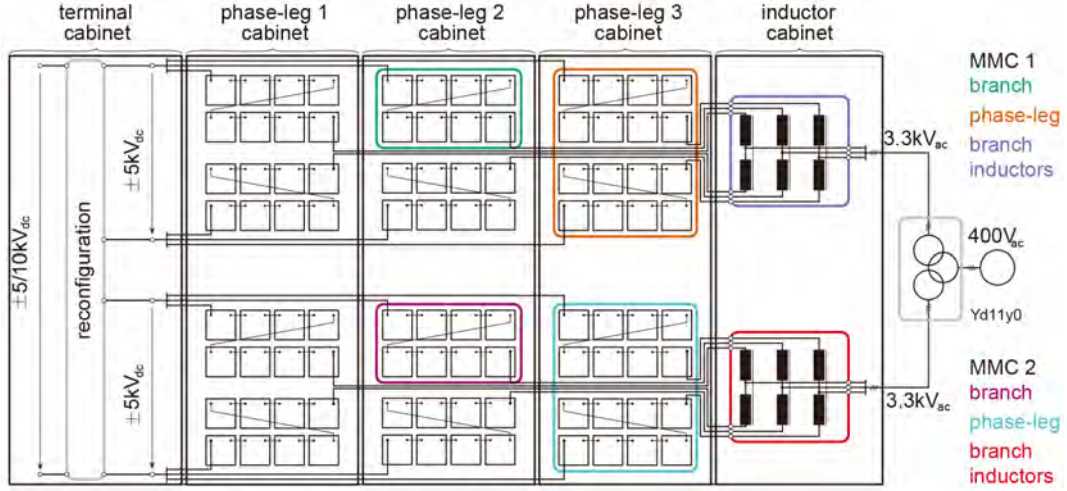
Fig. 1. 0.5 MVA rectifier composed of two MMC connected, through a conventional twelve pulse transformer, to the ac grid and their dc terminals connected in series to generate arbitrary voltage in the range of ±10 kV.

first stage is based on flyback converter and the second stage is based on a commercial power supply. In this case, a stability model between both stages must be established to achieve proper operation. Single power switch [7], [8] and two switches [9] input-series output-parallel (ISOP) power supplies have been presented as well. Even though ISOP configuration is able to meet a high-voltage input and high-power output with a simple principle, it must overcome technical challenges beyond flyback's design, such as input capacitor voltage balance, start-up synchronization and input voltage unbalance protection. It is also important to emphasize that previously presented solutions have left aside other critical design aspects as well as construction and test considerations. In fact, [1], [2], [4]–[9] do not consider partial discharge test and show only one low-voltage output, which may not be enough to supply all circuits in a SM or may require an extra (commercial) isolated power supply. Solely [6] presents stability test, [5] presents thermal test and [7] presents shut-down test, while [3], [4] do not show start-up test.

This paper proposes an isolated, flyback-based ASPS with planar magnetic, PCB integrated windings and multiple isolated outputs as a feasible and simple low-voltage components power supply solution for a SM in a medium voltage MMC application. Additionally, this paper describes extensively its design procedure, taking in account electrical and magnetic mathematical modelling, technological integration challenges as well as proper experimental test considerations. Section II presents an overview of the SM application and characteristics, giving way to ASPS's requirements. Section III describes the electrical design procedure and presents the main mathematical expressions and assumptions. Section IV presents the detailed design of a planar transformer with printed circuit board (PCB) integrated windings, which is supported by finite element method (FEM) simulations. Section V derives a small signal model and control loop design for the case of a flyback with

multiple outputs. Section VI provides the final implementation results as well as a thorough experimental verification of the ASPS operation. Section VII concludes the paper.

II. SUBMODULE APPLICATION OVERVIEW

Even though MMCs are intended to be used in a wide range of applications, by way of illustration, a 0.5 MVA rectifier, made out of two MMCs with 48 low voltage SMs in each, has been considered [10], able to generate arbitrary voltage in the range of 10 kV at its dc terminals (cf., Fig. 1). The MMC SM (cf., Fig. 2) is built with a 1.2 kV/50 A IGBT H-bridge module, which can operate either as unipolar or bipolar SM depending on the hardware reconfiguration (HR) connection. The capacitor bank is made out of 6×1.5 mF/400 V electrolytic capacitors, for a total SM capacitance of 2.25mF. The SM bypass is a twofold: a fast and non-permanent bypass is realized with a 1.2 kV/72 A anti-parallel thyristors module (THYB), while the permanent SM bypass is provided by a relay. The SM's bypass is either triggered by the local SM controller (e.g., in case a gate driver fault is detected) or as last resort with a chain of transil diodes located at the SM terminals to detect over-voltages (OVD). Additional information on the MMC design is available in [11]–[14]. Consequently, isolated voltages have to be provided to the semiconductor's gate drivers (IGBTs), SM's controller, ASPS self-supply and protection circuit (over voltage detection sub-circuitry, anti-parallel thyristors and permanent bypass relay). This can be realized at once with a transformer[1] with multiple outputs (cf., Fig. 3). The transformer described and designed must have six sets of secondary windings:

- 1×5 V, 4 W for the SM's controller supply ($V_{\text{out},+5V}$) .

[1] Even though the magnetic circuit in a flyback converter is actually a multi-winding inductor, for the sake of brevity and schematic representation, we will refer to it as a multi-winding transformer in this paper.
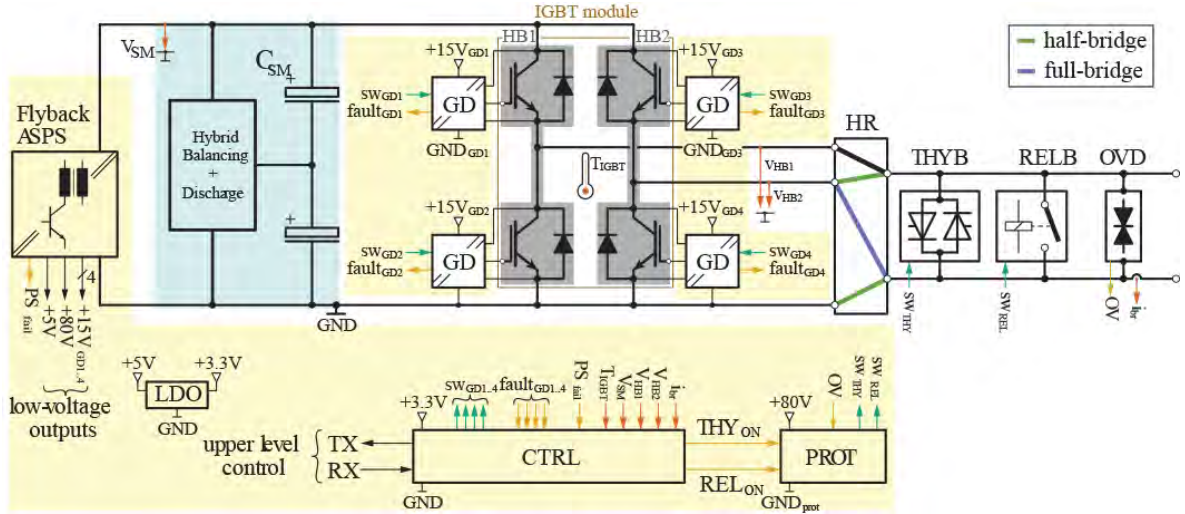
Fig. 2. MMC SM functionality: hardware reconfiguration (HR), anti-parallel thyristor bypass (THYB), relay bypass (RELB), over-voltage detection (OVD) and SM controller (CTRL). The SM's reference potential is common with the controller ground and is connected to the SM's enclosure that is on a floating potential.
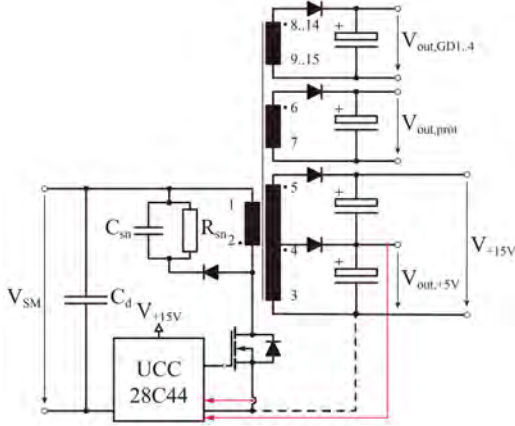

Fig. 3. Simplified flyback circuit with 7 sets of windings as a result of specific design requirements. The bias circuit and additional filtering elements have been omitted. The pin numbers are matching the ones on the planar transformer PCB. Each IGBT gate driver is supplied by a separated winding.

This output has to be tightly regulated in closed-loop. In practice, this is a tapped winding with the V_{+15V} winding used to power the PWM controller. The SM's ground potential is common with the SM controller's ground.

- 4×15 V, 1.5 W for the IGBT gate drivers ($V_{out,GD1..4}$). An additional 900 V isolation is required between the upper and lower gate driver's windings.

- 1×80 V, 15 W for 15 s operation when activated for the protection circuit ($V_{out,prot}$). The voltage is on purpose high in order to obtain a sufficiently large energy buffer with a relatively low storage capacitance value ($E \propto V^2 - E \propto C$ trade-off).

The SMs are first charged passively from outside (e.g., with an inrush current limiting resistor from the ac side). In that way, it only gets charged to the peak of the ac voltage, which

TABLE I
TECHNICAL SPECIFICATIONS PER WINDING FOR THE PLANAR TRANSFORMER

Winding	Voltage (V)			Power
	Min.	Nom.	Max.	
Primary (pri)	200	625	900	≈ 20 W
Protection (prot)		80		15 W-15 s
+5 V		5		4 W
+15V		15		1 W max.
Gate drivers (GD) (4x)		15		1.5 W each

roughly corresponds to approximately 35% of the nominal SM voltage. As a consequence, in order to enable active charging (in closed-loop), the ASPS should start its operation at a relatively low voltage. The minimum SM voltage at which the ASPS is expected to operate is set to $V_{SM,min} = 200$ V. The nominal SM voltage is $V_{SM,nom} = 625$ V (considering a connection with a 5 kV$_{dc}$ bus, with 8 SM per branch of one MMC). The maximum SM voltage, related to the threshold voltage at which the SM's bypass gets activated for preserving its components (both the IGBTs and capacitors), is set to $V_{SM,max} = 900$ V. The estimated ASPS input power is 20 W. The specification for the planar transformer is summarized in Table I.

III. ASPS ELECTRICAL DESIGN

For sake of simplicity, the following developments consider only one secondary. All the results presented in this section can be extended to the case with six (or more) outputs.

A. PWM Controller

As the input ASPS voltage and load vary over a wide range,

the IC UCC28C44 [15] performing a current mode control is chosen. The control loop is the following: a fast inner control loop acts on the switch current (feedback of the primary current with a sensing resistor) and a slower outer control loop acts on the voltage (feedback of the +5 V controlled output voltage with a resistive divider. The other outputs are cross-regulated). Since both the input and +5 V output share the same ground, there is no need for an isolated feedback of the controlled voltage.

B. Duty Cycle and Primary Inductance

The maximum duty cycle, $D_{max} = 0.5$ is set by the PWM controller, which operates in discontinuous conduction mode (DCM). This condition, combined with the minimum SM voltage, gives the turns ratio between the primary and the secondary winding. For the calculation, the protection winding was taken, but the same holds for any other winding:

$$D_{max}=\frac{V_{prot}N_p}{V_{prot}N_p + V_{SM,min}N_{s,prot}}=0.5 \rightarrow \frac{N_p}{N_{s,prot}}=\frac{5}{2} \qquad (1)$$

The condition on the turns ratio and maximum SM voltage gives the minimum duty cycle:

$$D_{min}=\frac{V_{prot}N_p}{V_{prot}N_p + V_{SM,max}N_{s,prot}}=\frac{2}{11} \simeq 0.182 \qquad (2)$$

Additionally, the nominal duty cycle is estimated to $D_{nom} = 0.242$, which is relevant for evaluating the magnetic field density norm and eventual saturation level in the transformer core. The primary inductance to be matched is defined in (3). This value is relevant for the choice of the semiconductor's current rating.

$$L_p=\frac{V_{SM,min}^2 D_{max}^2}{2P_{in}f_{sw}} \qquad (3)$$

The obtained primary inductance is $L_p = 12.5$ mH with $f_{sw} = 20$ kHz, which was found as trade-off between the efficiency and power density.

C. Semiconductor Device Sizing

The semiconductor device selected for this application is an N-chanel enhancement mode MOSFET. The drain to source voltage that the MOSFET has to withstand [16] is derived considering the worst case scenario, i.e., at $V_{SM,max}$ input voltage together with a voltage spike due to the leakage inductance, which is estimated at 30% of the input voltage, and the highest reflection voltage coming from the +5 V output:

$$V_{DS}=1.3(V_{SM,max})+\left(\frac{N_p}{N_s}\right)(V_{out,+5V}+V_D) \qquad (4)$$

From (4), the maximum voltage that the MOSFET has to withstand is 1.41 kV. The current rating of the switch is:

$$I_{DS,pk}=\frac{V_{out,+5V}(1 - D_{max}) N_p}{L_p f_{sw}}\frac{N_p}{N_s} = 0.4 \text{ A} \qquad (5)$$

The selected semiconductor device is the 1.5 kV/2 A 2SK4177 MOSFET from ON Semiconductor [17]. The 2SK4177 comes in a TO-263-2L package, which perfectly conforms to the space constraints on the SM.

D. MOSFET Gate Driver

The selected MOSFET has a gate capacitance $Q_{g(on)} = 39$ nC. The peak gate current is limited by an additional gate resistor, so that it remains below one third of the maximum current that the PWM controller can output ($I_{g,max} = 1$ A). Taking into account the 10 Ω impedance to rail of the controller, a safe choice is around 35 Ω. For the discharge, the sink to ground can take much higher current, so a small 15 Ω is put in series with a Schottky diode on the return path, all in parallel with the 35 Ω resistor.

E. Snubber Circuit

In order to protect the MOSFET from voltage spikes, a RCD snubber circuit is used, as indicated in Fig. 3. The snubber resistor R_{sn} and capacitor C_{sn} values are obtained from (6b) and (6c) according to [18]. The snubber voltage V_{sn} is taken as 2~2.5 times the reflected output voltage $V_{ro} = 240$ V (slightly higher than (N_{pri}/N_{+5V}) V_{+5V} due to the leakage inductance). The leakage inductance is considered to be 3% of the magnetizing inductance, i.e., $L_\sigma = 375$ μH. The snubber voltage ripple ΔV_{sn} should not be greater than 10%~15%.

$$\Delta V_{sn}=\frac{V_{sn}}{C_{sn}R_{sn}f_{sw}} \qquad (6a)$$

$$R_{sn}=\frac{V_{sn}^2}{\frac{1}{2}f_{sw}L_\sigma I_{DS,pk}^2 \frac{V_{sn}}{V_{sn} - V_{ro}}} \qquad (6b)$$

$$C_{sn}=\frac{V_{sn}}{R_{sn}\Delta V_{sn}f_{sw}} \qquad (6c)$$

As a result, the values of the snubber resistor and capacitor are 192 kΩ and 2.7 nF respectively. The snubber diode is BYG10Y, with $V_{RRM} = 1.6$ kV [19].

F. Start-up Circuit

A series R-C bias circuit powers the PWM controller from the dc-link until the V_{+15V} output gets activated (the turn-onthreshold for the PWM controller is $V_{DD} = 14.5$ V, while the turn-off threshold is $V_{DD} = 9.5$ V). The bias circuit is sized

considering $V_{SM}(t) = \frac{dV_{SM}}{dt} t$ (approximately, linear behavior at beginning of capacitor charge) with $\frac{dV_{SM}}{dt} = 1450$ V/s (from 0 V to 290 V in 200 ms from passive charging) and $V_{DD} = 14.5$ V past 0.5 s. The resistor and capacitor R_{in} and C_{in} are obtained with (7).

$$V_{DD}(t) = \frac{dV_{SM}}{dt}(t - R_{in}C_{in}) + \frac{dV_{SM}}{dt} R_{in}C_{in} e^{-\frac{t}{R_{in}C_{in}}} \qquad (7)$$

Choosing $R_{in} = 1.4$ MΩ and $C_{in} = 10$ μF, V_{DD} will take 533 ms to reach the desired voltage. A 18 V Zener diode prevents V_{DD} from exceeding the controller limit.

G. Output Filtering and Rectification Diodes

Since $V_{out,+5V}$ is supplying the SM controller, the voltage ripple on this output must be lower than specified by the SM controller. For this reason, a maximum of 1% $\Delta V_{pk,pk}$ is allowed, i.e., 50 mV. According to [20]:

$$C_{out,min,+5V} = \frac{I_{out,max,+5V} D_{max}}{f_{sw} \Delta V_{pk,pk}} \qquad (8)$$

This leads to $C_{out,min,+5V} = 0.4$ mF. The actual filter capacitance is increased to 3 mF for safety margin.

For the +15 V output, no large capacitance is needed, since the power consumption is low. $C_{out,+15V}$ is set to 11 μF.

The current flowing through the gate driver outputs is approximately 100 mA and the maximum ripple allowed is $\Delta V_{pk,pk} = 100$ mV. For the gate driver outputs, the minimum capacitance is $C_{out,min,GD} = 25$ μF. The actual filter capacitance is increased to 100 μF for safety margin.

The protection output is not requiring any filtering, since a larger energy buffer (required to activate the permanent bypass in case of supply loss) is present on the receiver end.

The output rectifier diodes used are MURS340 [21] for the V_{+5V} output and MURS160 [22] for all the other outputs. The reason for this choice is the current rating of MURS340 and MURS160 of 1 A and 3 A, respectively. These ratings are high enough compared to the output current flowing through them, which is in range of 67~800 mA, according to Table I.

IV. ASPS MAGNETIC DESIGN

The magnetic part of the ASPS comprises a planar transformer with seven windings in total (cf., Fig. 3). The use of PCB integrated windings allows for a very compact transformer design, which means cores with small window heights are well suited. Moreover, all units will have almost identical electrical parameters. The design presented in this paper has considered the following manufacturing constraints and minimum requirements: 1) track width of 200 μm and 2) 200 μm track spacing if the tracks belong to the same net (i.e., winding). The main impact of those constraints results in the maximum achievable number of turns per layer, or in the minimum number of layers per winding.

A. Reluctance Model

A combination of a ferrite planar E-core and its matching I-core is selected in order to obtain a design with a reasonable window height utilization. An air-gap is considered on the center limb, where the majority of the magnetic energy isstored during the power transfer from the primary to the secondaries. The PCB containing the windings is placed at the bottom of the window area (the furthest from the air-gap) in order to minimize the winding losses [23]. The core geometry and its parametrization are presented in Fig. 4(a).

The detailed expressions for each reluctance according to the partitioning in Fig. 4(b) are given in (9). The core reluctance expressions follow [24].

$$\mathcal{R}_1 = \frac{\frac{\pi}{8}(H + F/2)}{\mu_0 \mu_r (I_{p,max})C(H + F/2)/2} \qquad (9a)$$

$$\mathcal{R}_2 = \frac{M}{\mu_0 \mu_r (I_{p,max})CL} \qquad (9b)$$

$$\mathcal{R}_3 = \frac{\frac{\pi}{8}(H + L)}{\mu_0 \mu_r (I_{p,max})C(H + L)/2} \qquad (9c)$$

$$\mathcal{R}_4 = \frac{D}{\mu_0 \mu_r (I_{p,max})CL} \qquad (9d)$$

$$\mathcal{R}_5 = \frac{\frac{\pi}{8}[(B - D) + L]}{\mu_0 \mu_r (I_{p,max})C[(B - D) + L]/2} \qquad (9e)$$

$$\mathcal{R}_6 = \frac{M}{\mu_0 \mu_r (I_{p,max})C(B - D)} \qquad (9f)$$

$$\mathcal{R}_7 = \frac{\frac{8}{\pi}[(B - D) + F/2]}{\mu_0 \mu_r (I_{p,max})C[(B - D) + F/2]/2} \qquad (9g)$$

$$\mathcal{R}_8 = \frac{D - l_{ag}}{\mu_0 \mu_r (I_{p,max})C(F/2)} \qquad (9h)$$

$$2\mathcal{R}_{core} = \sum_{i=1}^{8} \mathcal{R}_i \qquad (9i)$$

The air-gap reluctance R_{ag} accounts for the fringing flux (the effective air-gap is larger than the core's cross-section at the air-gap) as presented in [25]. Details about its calculation are presented in Appendix. The total circuit reluctance is given as a function of the air-gap length:

$$\mathcal{R}_{tot}(l_{ag}) = \frac{1}{2}(2\mathcal{R}_{core} + \mathcal{R}_{ag}) \qquad (10)$$
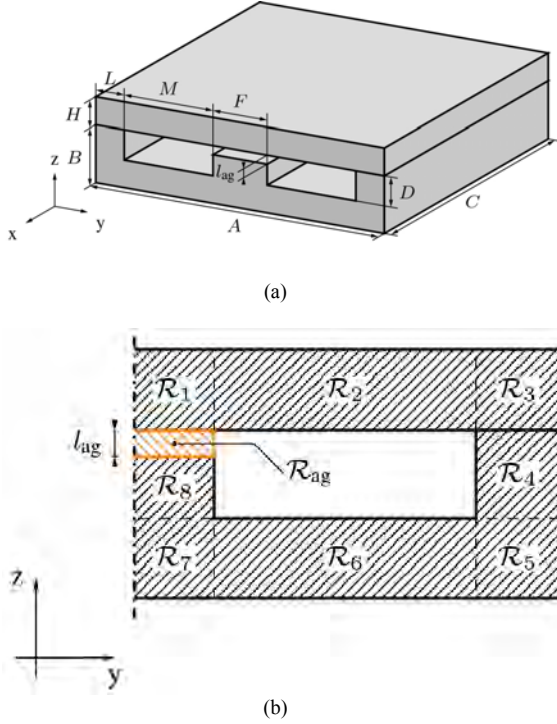
(a)

(b)

Fig. 4. Ferrite core. (a) Geometry parametrization. (b) Magnetic circuit partitioned into reluctances. For symmetry reasons, only its half is represented.

B. Design Optimization

The design specifications are summarized in Table II. The first element to be evaluated is the minimum allowable number of turns on the primary winding so that the maximum flux density in the core remains way below saturation ($B_{max} = k_{sat}B_{sat} < B_{sat}$). Note that k_{sat} can be relatively high (close to one) without affecting the performance of the converter at nominal SM voltage, since both the peak primary current and the duty cycle (close to D_{nom}) are decreasing.

$$B_{max} = \frac{\Phi_1}{2A_8} = \frac{L_p I_{p,max}}{N_p 2A_8} = \frac{V_{SM,max}D_{min}T_{sw}}{N_p 2A_8}$$

$$\rightarrow N_{p,min} = \text{ceil}\left(\frac{V_{SM,max}D_{min}T_{sw}}{2A_8 B_{max}}\right) \qquad (11)$$

where $2A_8 = FC$ is the core center limb's cross-section. L_p is matched by adjusting the air-gap length:

$$L_p = \frac{N_p^2}{\mathcal{R}_{tot}(l_{ag})} \qquad (12)$$

Notably, for costs reasons, the number of turns (i.e., indirectly the number of layers in the PCB) should be kept at a minimum. This means smaller core sizes (e.g., 1804), for which $N_{p,min}$ will be inevitably large in order to prevent the core's saturation,

TABLE II
PLANAR TRANSFORMER DESIGN INPUTS

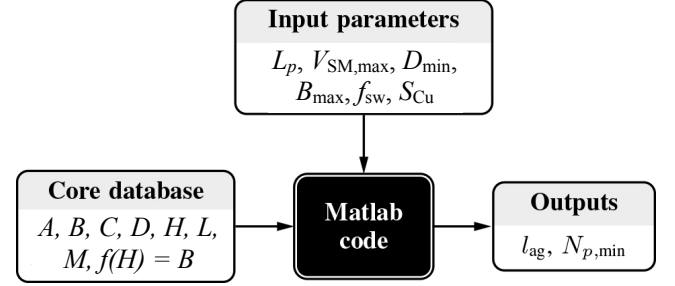| L_p	$V_{SM,max}$	D_{min}	k_{sat}	f_{sw}	$S_{Cu,min}$
12.5 mH	900 V	0.182	0.725	20 kHz	$35 \times 200\ \mu m$

Fig. 5. Planar transformer design tool.

are discarded. On the other hand, large core sizes (e.g., 6450) require low $N_{p,min}$, but are discarded due to space constraints on the SM.

A transformer design tool encompassing the above discussed design steps is built (cf., Fig. 5). The core database comprises the core's geometry parameters as well as the material's *B-H* curve, from which the relative permeability is derived. The input parameters are specific to the desired design.

C. Design Results

The core database is built with planar EI cores from Cosmo Ferrites [26]. The selected ferrite material is CF297, whose *B-H* curve is shown in Fig. 6. The choice was based on the material availability from the supplier. The fitted Jiles-Atherton [27] parameters are indicated in Table III. Its *B-H* and corresponding relative permeability curves are shown in Fig. 7. The design results are shown in Fig. 8. For the selected design, the inductance contribution from the core and the airgap are given by:
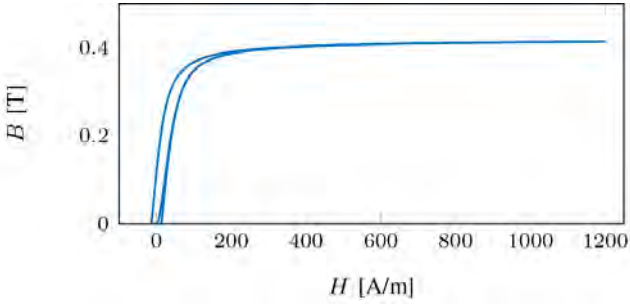
$$L_{p,core} = \frac{N_p^2 \mathcal{R}_{core}}{\mathcal{R}_{tot}^2} = 565\ \mu H$$

$$L_{p,ag} = \frac{N_p^2 \mathcal{R}_{ag}}{\mathcal{R}_{tot}^2} = 11.9\ mH$$

meaning that the influence of the peak primary current on the primary inductance value is negligible, as the magnetic energy is almost exclusively stored in the air-gap.

The turns numbers for the other windings are given by:

$$\frac{x}{N_{s,x}} = \frac{80\ V}{N_{s,80}} \qquad (13)$$

Fig. 6. *B-H* curve for the magnetic material CF297 at 25 °C.

TABLE III
JILES-ATHERTON FITTED PARAMETERS FOR CF297 FERRITE MATERIAL

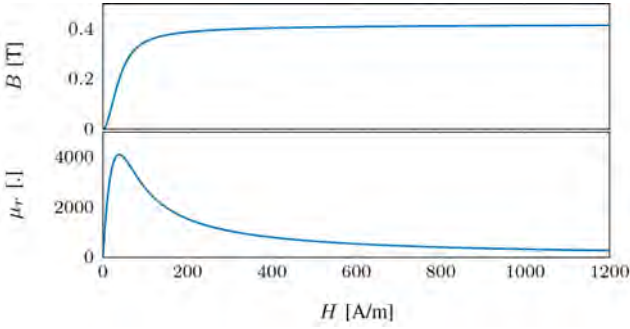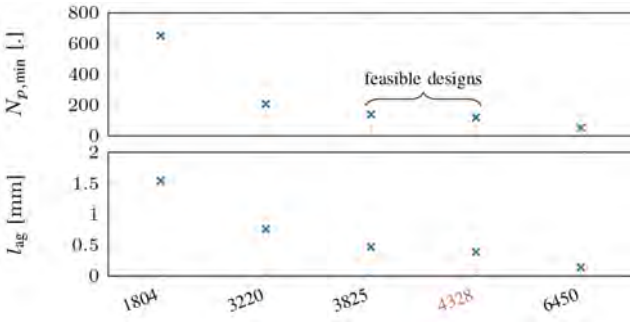| M_s	k	a	c	α
332327	14.47	13.55	$6 \cdot 10^{-6}$	$5.83 \cdot 10^{-9}$

Fig. 7. Magnetization from Jiles-Atherton coefficients for CF297 ferrite material at 25 °C and derived relative permeability curves. The first curve is used as input to define the nonlinear magnetic material in the FEM simulations.

Fig. 8. Design algorithm results for a range of planar EI cores. The selected core combination (4328) is indicated in red. $N_{p,min} = 120$ and $l_{ag} = 390 \ \mu m$.
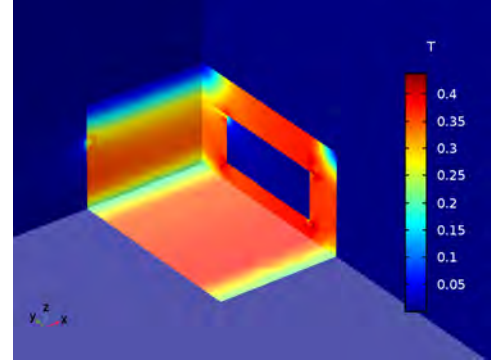
where $x = V_{+5V}$, V_{+15V}. Finally, the turns numbers are summarized in Table IV.
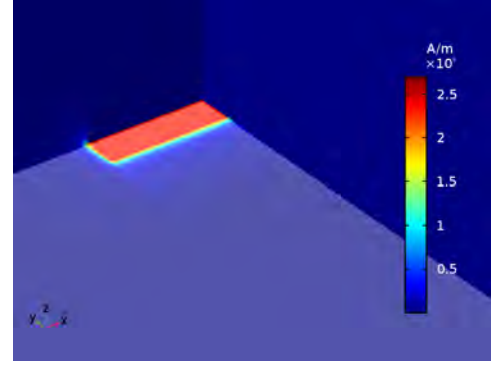
D. FEM

In order to accurately capture the fringing effect, a 3D FEM model is built in Comsol Multiphysics® in order to verify the magnetic characteristics of the design. Even though 3D simu-

TABLE IV
TURNS NUMBERS FOR THE SELECTED DESIGN

Primary	Protection	+5V	+15V	Gate Drivers
120	48	3	9	9

(a)

(b)

Fig. 9. 3D FEM fields. (a) Magnetic field density (in [T]) with three orthogonal cut planes in the middle of the ferrite core (center at coordinate (C/2, A/2, [B – D)/2]). (b)Magnetic field norm (in [A/m]) for $I_{pri} = 0.8$ A with three orthogonal cut planes in the middle of the air-gap (center at coordinate (C/2, A/2, B – l_{ag}/2)). By integration of the magnetic energy, $L_{p,core} = 750 \ \mu H$ and $L_{p,air} = 11.5$ mH, resulting in $L_p = 12.25$ mH.

lations come with a large computation overhead compared to 2D ones, they're necessary to avoid ~ 4.5% difference in the air-gap length (observed for the selected design) in case only the fringing flux in *zy* plane is accounted for. The primary windings are lumped in one single conductor whose dimensions are the ones of the PCB where the windings have been integrated. The air-gap length is set to the designed value. For the first FEM simulation, the coil excitation is set to the maximum primary peak current (during start-up with $D = 0.5$). The result is shown in Fig. 9. The obtained inductance value matches the analytical model with a relative error $\varepsilon = -2\%$. In a second FEM simulation, the air-gap length is swept from 375 to 385 μm with the maximum peak primary current (cf., Fig. 10). It is found that $l_{ag} = 377.5 \ \mu m$ reaches exactly the target L_p. For the third FEM simulation, the primary peak current is
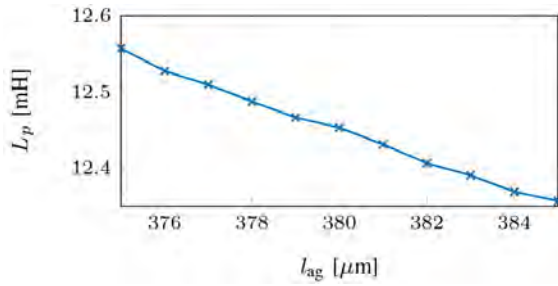
Fig. 10. 3D FEM primary inductance variation over a sweep of the air-gap length from 375 to 385 μm with a primary current of 0.8 A.
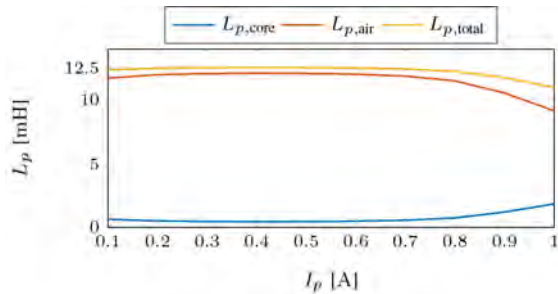

Fig. 11. 3D FEM primary inductance variation over a sweep of the peak primary current from 0.1 to 1 A with 0.1 A step.

swept from 0 to 1 A with 0.1 A step in order to observe the variation of the primary inductance with respect to the SM voltage variation. As the magnetic energy is mainly stored in the air-gap, the variation of the primary inductance value is barely existent (cf., Fig. 11).

E. Planar Transformer Layout

The planar transformer layout is designed in Altium Designer®. The windings are drawn thanks to the user script PlanarTXv0.7 tool. The tracks are spread across 12 layers.

The need for high voltage (HV) isolation between winding sets results in creepage/clearance distances that have to be met in the PCB. The standard UL840 [28] is followed, considering a pollution degree 2 and an overvoltage category II. It is allowed to interpolate the values from the standard. While BT-epoxy laminates (like G200 from Isola Group [29]) offer superior dielectric properties, they're generally not stocked by PCB manufacturers and can't be requested for low order quantities. The laminate belongs to the material group IIIa (high comparative tracking index (CTI)). The minimum creepage and clearance distances are presented in Table V and Table VI, respectively.

The final PCB dimensions are 61.6 mm × 34.1 mm × 3 mm. The layer stack is shown in Fig. 12, while the layers layout is shown in Fig. 13. The copper layers spacing is selected according to the dielectric properties of the substrate and the minimum isolation voltage required for the design. As the primary winding is spread across 5 layers in order to comply with the

TABLE V
MINIMUM CREEPAGE DISTANCES BETWEEN SETS OF WINDINGS (IN [MM]) FOR 900 V MAXIMUM OPERATION VOLTAGE

Set	pri	5/15V	prot	GD1	GD2	GD3	GD4
pri	0	9	9	9	9	9	9
5/15V		0	9	9	0	9	0
prot			0	9	9	9	9
GD1				0	9	9	9
GD2					0	9	0
GD3						0	9
GD4							0

TABLE VI
MINIMUM CLEARANCE DISTANCES BETWEEN SETS OF WINDINGS (IN [MM]) FOR 900 V MAXIMUM OPERATION VOLTAGE

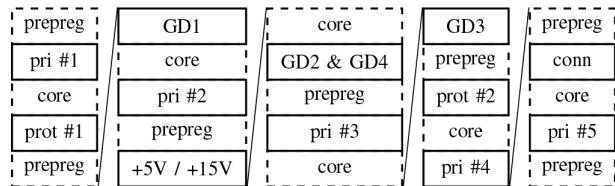| Set	pri	5/15V	prot	GD1	GD2	GD3	GD4
pri	0	2.625	2.625	2.625	2.625	2.625	2.625
5/15V		0	2.625	2.625	0	2.625	0
prot			0	2.625	2.625	2.625	2.625
GD1				0	2.625	2.625	2.625
GD2					0	2.625	0
GD3						0	2.625
GD4							0

Fig. 12. PCB layer stack with constant 200 μm fiberglass layers (either core or prepreg) between copper layers. The two prepreg layers on top and at the bottom are required to cover the vias around the center limb for layers connections, as their spacing is way too small compared to the required clearance in air.

manufacturing constraints regarding the minimum track width and track spacing, a full voltage isolation is required between each neighboring layer. Consequently, a 200 μm layer spacing is selected. A radiography to highlight one slice of the PCB in *zx* plane is shown in Fig. 14.

V. SMALL-SIGNAL MODEL AND CONTROL LOOP DESIGN

Small-signal flyback models have been presented, amongst others, in [31], [32]. They only focus on single output supplies, unlike this work. For a single output flyback operated in DCM, it is straightforward to build a small-signal model and construct an open-loop transfer function. Considering the specifications given in Table I, each output is taken into consideration and is modeled as a load resistor in parallel with an output capacitor. When dealing with multiple outputs flyback, all elements have to be taken into account and referred
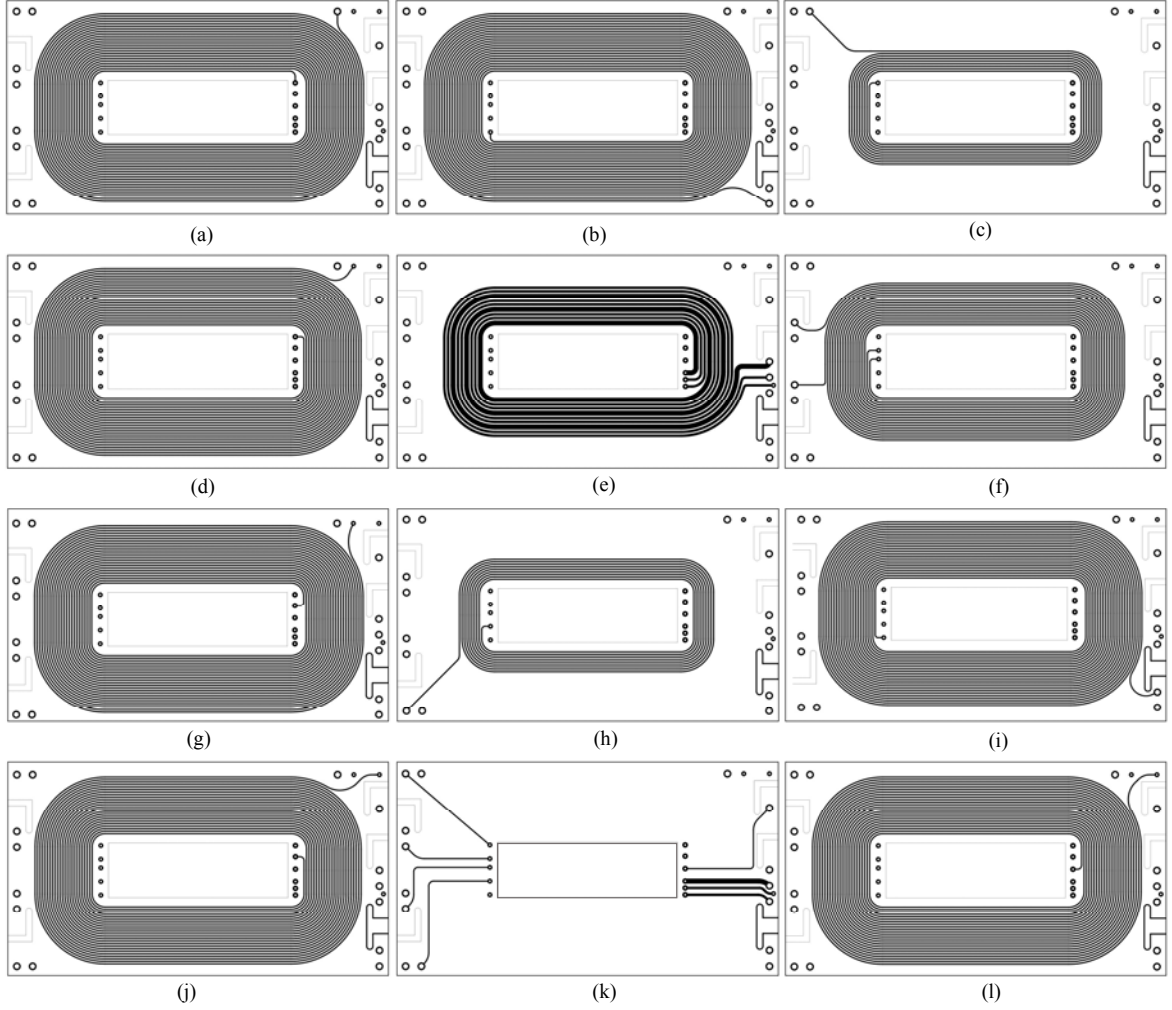
Fig. 13. Flyback trafo PCB layers. (a) Primary layer #1. (b) Protection layer #1. (c) GD3. (d) Primary layer #2. (e) +5 V/+15V. (f) GD2 & GD4 (bottom switches). (g) Primary layer #3. (h) GD1. (i) Protection layer #2. (j) Primary layer #4. (k) Connections. (l) Primary layer #5. The 15 transformer pins are numbered clockwise from 12 o'clock. All vias not used as electrical connections (pin #1 to #15) are blind vias, as clearances cannot be met around the central opening of the ferrite core.

Fig. 14. Planar transformer PCB windings cut view is in the *zy* plane, in the middle of the bottom horizontal section of Fig. 13, obtained by a micro computed tomography (CT) scanner [30]. Only 11 out of 12 layers are visible, since the connection layer (conn in Fig. 12) is not present where the cut view was made.

to the controlled output through the turns ratio according to Table IV. The relations between the referred and non-referred resistance and capacitance are given in (14), where R_x and C_x denote the output resistance and capacitance being referred and N_x the number of turns.

$$R_{x \to +5V} = \left(\frac{N_{+5V}}{N_x}\right)^2 R_x \qquad (14a)$$

$$C_{x \to +5V} = \left(\frac{N_x}{N_{+5V}}\right)^2 C_x \qquad (14b)$$

Table VII lists the transformed values of the relevant circuit elements. The equivalent output resistance and capacitance are $R_{\text{load,eq}} = 2.43\ \Omega$ and $C_{\text{out,eq}} = 6.85$ mF. It should be noted that the load resistor of the protection output is not taken into account, since in normal operation there is no load on this output (the protection circuit gets activated only in case of a fault). The parasitic elements, such as the ESR of the output capacitors, also have an impact on the overall loop(s) shape(s).

TABLE VII
OUTPUT RESISTORS AND CAPACITORS FOR DIFFERENT OUTPUTS AND
THEIR VALUES WHEN REFERRED TO THE +5V CONTROLLED OUTPUT

Circuit Element	Value	Referred to +5V output
$R_{\text{load,GD1..4}}$	170 Ω	18.9 Ω
$R_{\text{load,+15V}}$	225 Ω	25 Ω
$C_{\text{out,GD1..4}}$	101 μF	901 μF
$C_{\text{out,+15V}}$	11 μF	99 μF
$C_{\text{out,prot}}$	470 nF	120 μF

TABLE VIII
DCM CURRENT-CONTROLLED FLYBACK SMALL-SIGNAL POLES, ZEROS
AND DC GAIN. $N = N_{+5v}/N_{\text{pri}}$ IS THE TRANSFORMER TURNS RATIO

$\omega_{\text{p,1}}$	$\dfrac{1}{\pi R_{\text{load}} C_{\text{out}}}$
$\omega_{\text{p,2}}$	$\dfrac{f_{\text{sw}}}{\pi} \left[\dfrac{\frac{V_{\text{SM}}}{V_{+5V}}}{\sqrt{\frac{2L_p f_{\text{sw}}}{R_{\text{load}}}\left(1 + \frac{V_{\text{SM}}}{NV_{+5V}}\right)}} \right]^2$
ω_{lhpz}	$\dfrac{1}{2\pi R_{\text{ESR}} C_{\text{out}}}$
ω_{rhpz}	$\dfrac{R_{\text{load}}}{2\pi \frac{V_{+5V}}{NV_{\text{SM}}}\left(1 + \frac{NV_{+5V}}{V_{\text{SM}}}\right) L_p}$
dc gain	$\dfrac{V_{\text{in}}}{D_{\text{iv}}}\sqrt{\dfrac{R_{\text{load}} f_{\text{sw}}}{2L_p}\dfrac{L_p}{V_{\text{SM}} R_{\text{sense}}}}$

The output load impedance $Z_x = R_{\text{ESR},x} - jX_x$ is referred to the regulated output winding and the ESR is $R_{\text{ESR},x} = 20$ mΩ (from the device datasheet). For the DCM current-mode controlled flyback, the poles, zeros and dc gain are summarized in Table VIII [33]. The parameters R_{sense} and D_{iv} are the current sensing resistor and divider ratio between the current sense pin and the comparator inside the PWM controller. They equal 1.5 Ω and 3, respectively. The power stage transfer function is given by (15a), where ω_{lhpz}, ω_{rhpz}, $\omega_{\text{p,1}}$, $\omega_{\text{p,2}}$ correspond to the poles and zeros positions in rad/s. The selected compensator is an active single-pole filter with a flat low-frequency response. Its transfer function is given by (15b).

$$G_{\text{P}}(s) = G_{\text{o}} \frac{\left(1 + \frac{s}{\omega_{\text{lhpz}}}\right)\left(1 - \frac{s}{\omega_{\text{rhpz}}}\right)}{\left(1 + \frac{s}{\omega_{\text{p,1}}}\right)\left(1 + \frac{s}{\omega_{\text{p,2}}}\right)} \quad (15a)$$

$$G_c(s) = \frac{R_{\text{in}}}{R_c}\frac{1}{1 + \frac{s}{\omega_c}} \quad \omega_c = \frac{2\pi}{R_c C_c} \quad (15b)$$

VI. EXPERIMENTAL RESULTS

A series of tests are conducted on the designed ASPS in order to verify that the design requirements are satisfied.

A. Planar Transformer Testing

The realized transformer (cf., Fig. 16) is tested first separately in order to verify that it is compliant with the design objectives. 125 custom gapped cores (gap on the center leg of the E core, as shown in Fig. 4) were ordered from Cosmo Ferrites. Grinding and gluing of the ferrite cores was preferred over shimming and clamping for its increased flexibility and precision (no dependency on the isolated sheet's thickness).

1) Impedance measurements: The transformer is measured with an Omicron Bode 100 network analyzer. The results are shown in Fig. 17. In the low frequency region ($f < 1$ MHz), the characteristic is dominated by the core geometry and the air-gap, while in the high frequency region the characteristic is dominated by the parasitic elements in the PCB integrated windings. The transformer design experiences a main resonance at 228 kHz (which corresponds to a capacitance of 37.5 pF).

The gapping manufacturing repeatability process has been assessed by measuring the magnetizing inductance at 20 kHz for all 125 cores, as shown in Fig. 18. The mean value is 12.9 mH (σ = 0.18 mH), which is slightly higher than the target value of 12.5 mH, due the manufacturing process.

2) AC dielectric withstand test: The planar transformer's PCB is tested in a Faraday cage with a single-phase high step-up line frequency test transformer (capable of generating voltages up to 100 kV) and an Omicron MPD600 partial discharge (PD) measurement system in order to see if any breakdown occurs in the substrate. As the primary layer is spread among five layers distributed almost symmetrically inside the layer stack, it is sufficient to perform a single test where the primary winding is shorted and all secondary windings are shorted together and tied to the same potential. A trapezoidal voltage profile according to the IEC 61800-5 standard [34] is applied and the results are shown in Fig. 19.

B. ASPS Testing

The designed ASPS is inserted on the MMC SM as is shown in Fig. 15(a), therefore real loads are connected to their outputs. Fig. 15(b) presents the complete SM that matches the functionality introduced in Fig. 2: (1) a power board, which holds the IGBT module, the capacitor bank, the bypass thyristor module, the bypass relay, the hardware reconfiguration, a branch current sensor and (2) a signal board, which holds the ASPS, the SM controller, four IGBT gate drivers, the protection circuit (with three large capacitors that provide a sufficient energy storage to bypass the SM in case of loss of the ASPS) and a pair of optical fiber modules for communication with the upper layer control. Fig. 15(c) shows the SM and MMC metallic enclosure to provide mechanical protection, field shaping functions and proper airflow path through the SMs.

1) Start-up test: Fig. 20 shows the start-up of the ASPS, performed with an SM voltage stepped from 0 V to 290 V in 200 ms (controlled by voltage supply in current limit mode).
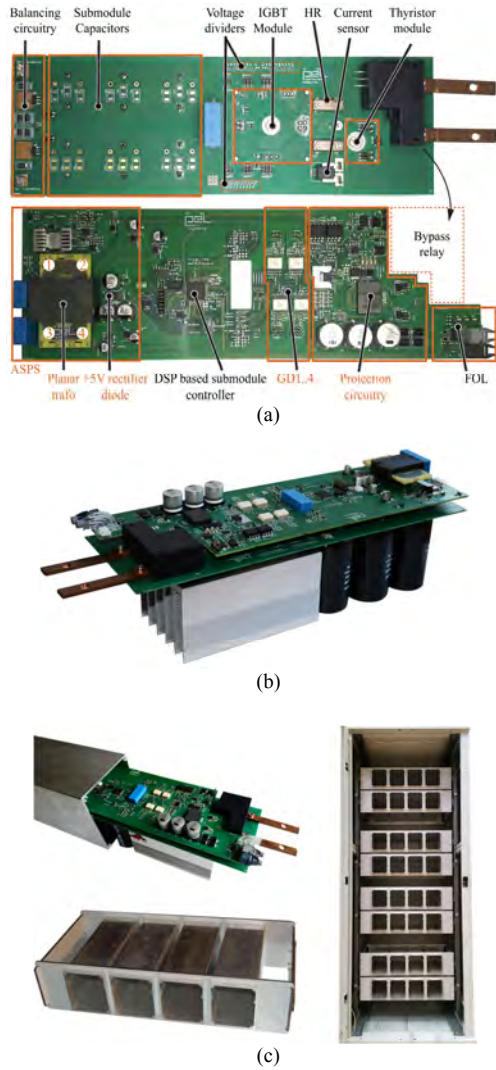
(a)

(b)

(c)

Fig. 15. (a) Detailed and annotated view of boards in the SM. The numbers 1 to 4 correspond to the measurement points where thermocouples were attached on the planar transformer for thermal test. Also, $V_{out,+5V}$ rectifier diode thermocouple position is shown. (b) Assembled MMC SM with power and signal boards. (c) MMC: SM with aluminum enclosure (top-left), SM's drawer (bottom-left), MMC cabinet (right).
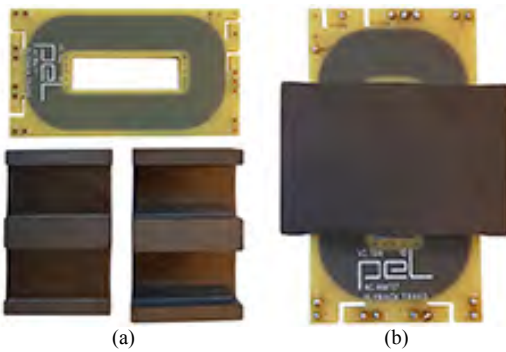

(a)   (b)

Fig. 16. Realized planar transformer. (a) Separate elements before assembly. (b) Assembled transformer. The PCB is 61.6 mm × 34.1 mm × 3 mm and the ferrite core 43.2 mm × 27.8 mm × 13.6 mm. The total planar transformer footprint is 61.6 mm × 43.2 mm.
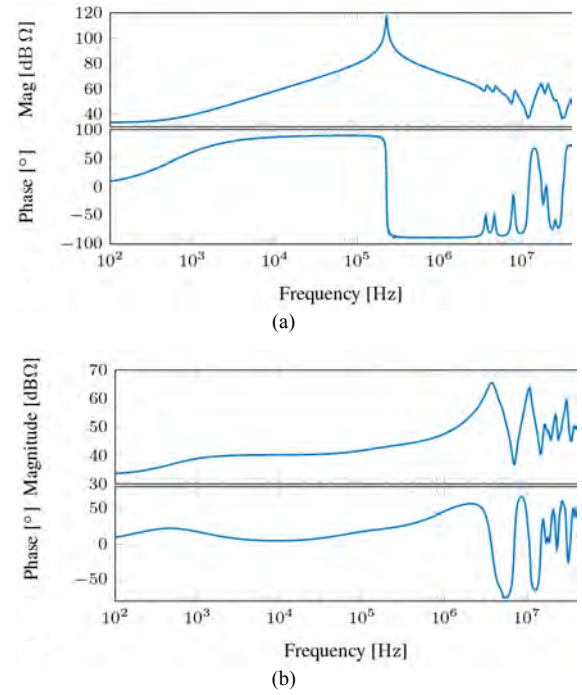

(a)

(b)

Fig. 17. Transformer impedance measurements with an Omicron Bode 100 network analyzer from 100 Hz to 40 MHz. (a) Open-circuit test (all secondaries open), giving L_p = 12.99 mH (R_s = 48.12 Ω) at 20 kHz. (b) Short-circuit test (all secondaries shorted), giving L_σ = 88.21 μH (R_σ = 102.64 Ω) at 20 kHz. The curves are obtained with 1601 logarithmically spaced frequency points.
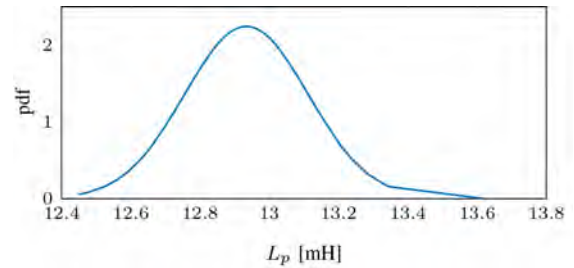

Fig. 18. Normal distribution of L_p at 20 kHz for 125 unglued cores measured with an Omicron Bode 100 network analyzer.
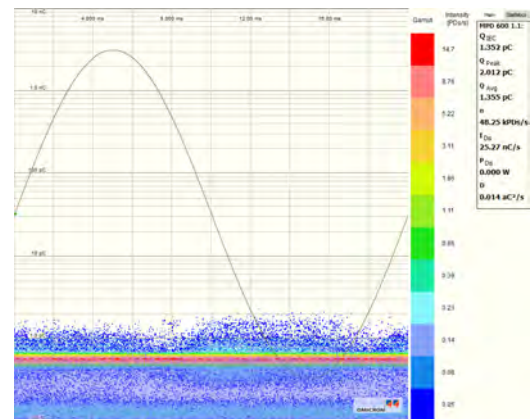

Fig. 19. AC dielectric withstand test results. A full 50 Hz period allows to potentially identify a higher level of PD at high dv/dt. Additional statistics are provided in the top right corner.
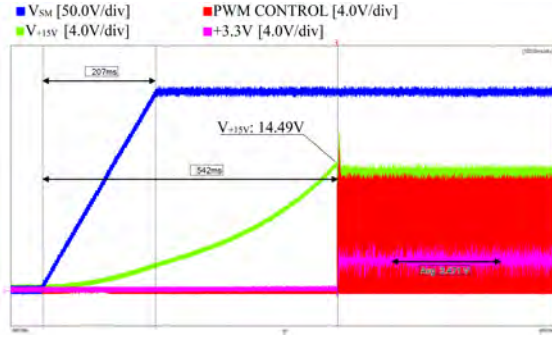
Fig. 20. Start-up of the ASPS. The PWM controller supply voltage is slowly charged through the bias circuit until its turn-on threshold is reached (14.5 V). Then the gate pulse is released. The voltage V_{DD} is recovered once the +15V output gets charged.
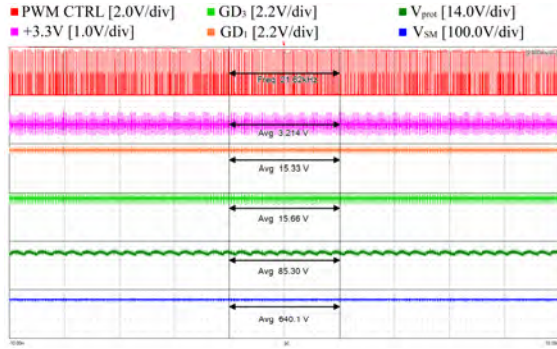

Fig. 21. Steady-state operation at 640 V SM voltage with each winding loaded as in Table I.

2) Steady-state operation and efficiency: The steady-state operation at 640 V SM voltage of the ASPS is reported in Fig. 21. The outputs are within their ripple limits and a small jitter is observed at the switching instants. Only two gate drivers outputs are shown for sake of simplicity. The efficiency was measured to 89.4% (at rated load and rated input voltage), which is higher than the usual flyback efficiency (around 80%).

3) Shutdown test: The shutdown test was performed with an SM voltage step from its nominal value to 0 V by activating bypass thyristors at the input to short circuit the power source connection. Once V_{SM} is below 140 V, the ASPS is not able to maintain the V_{+15V} with $D = 0.5$ and V_{DD} falls until it is lower than the UVLO turn-off threshold (9.5 V). The ASPS stops its operation when the SM voltage is below 90 V. The complete SM shutdown time is around 36 s. The result is shown in Fig. 22. Once the ASPS stops its operation, the balancing circuit (hybrid balancing + discharge block in Fig. 15) ensures a finite converter discharge time.

4) Stability analysis: The stability analysis of the ASPS is performed with an Omicron Bode 100 network analyzer. A perturbation signal is injected through an injection resistor R_i = 20 Ω, that is inserted in the feedback loop (cf., Fig. 23), with a wide band 1:1 isolation transformer B-WIT 100. In this way, the power stage together with the compensator are seen by the
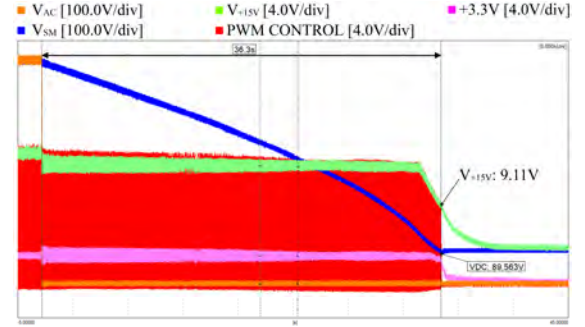
Fig. 22. Shutdown of the ASPS. The dv/dt is limited by the Delta SM 660-AR-11 used to emulate the SM voltage. When the SM voltage gets too low to regulate the V_{+5V} output (the duty cycle is clamped at 0.5, which occurred at V_{SM} = 178 V), the output voltages start decreasing. The ASPS completely shuts down when the undervoltage lockout (UVLO) turn-off threshold of 9.5 V is crossed.
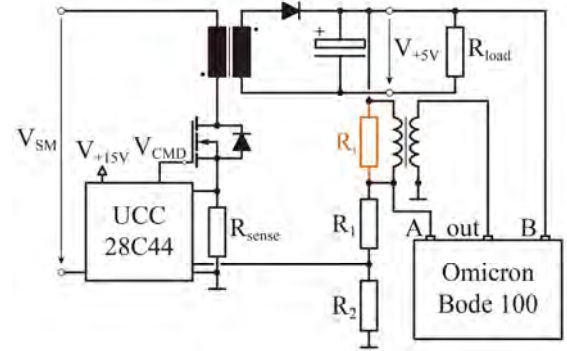

Fig. 23. Circuit connection for the stability analysis of ASPS with an Omicron Bode 100 network analyzer. The injection resistor R_i is added in series with R_1 the regular resistor for the output voltage divider. The injection transformer enables the injection of the perturbation signal generated in the Omicron Bode 100 network analyzer.

network analyzer between the points A and B. The results shown in Fig. 24 present a close match between the theoretical and experimental loops, with slight differences at certain points. The reason for these differences might be the tolerance of the output capacitors, whose values should always be taken into consideration with prudence. The gain and phase margins measured are 28.5 dB and 100.1° which provides enough stability margin according to [35]. The glitches around f_{sw} and its multiples comes from the impossibility to perform an accurate measurement at these frequencies.

5) Thermal measurements: The thermal measurements are presented as an overall view of the ASPS, where the temperature was observed with a FLIR E60 infrared camera in Fig. 25. Additionally, the temperature at five specific locations on the ASPS (as shown in Fig. 15) were recorded over the span of one hour of operation at nominal SM voltage from cold start. OMEGA wireless thermocouples were used [36]. The results are shown in Fig. 26. Certain measurements points on the transformer experience EMI and consequently differ one from another. As a consequence, it was decided to
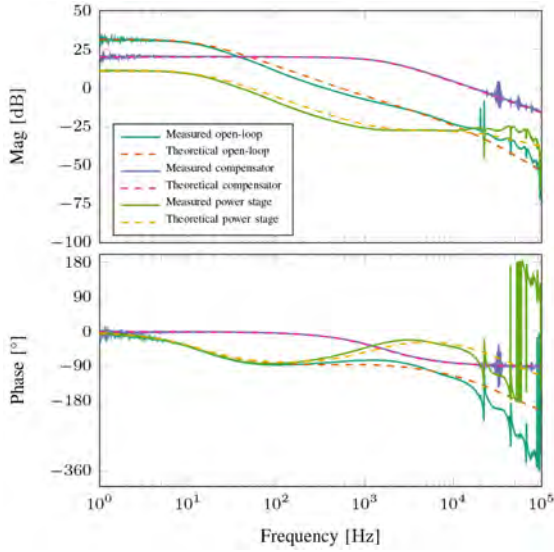
Fig. 24. ASPS open-loop, compensator and power stage impedance measurement from 1 Hz to 100 kHz with 1601 logarithmically spaced frequency points.
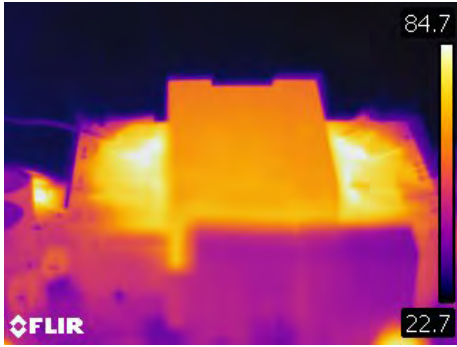

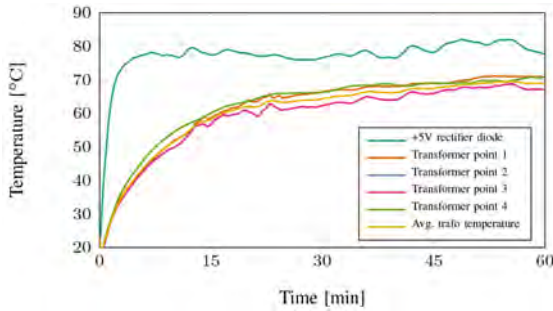Fig. 25. Thermal camera capture after one hour of operation.

Fig. 26. Thermal measurement done on four different points on the transformer PCB and on the V_{5V} rectifier diode.

include an average of the measurements, which can represent the transformer temperature in a better way.

VII. CONCLUSION

This paper has presented an isolated, flyback-based ASPS with

planar magnetic, PCB integrated windings and multiple isolated outputs for a 10 kV MMC with a maximum SM voltage of 900 V. Starting from its electrical specifications, the complete ASPS was designed. To guarantee a minimum variation of the magnetic component parameters in the ASPS of each of the 96 MMC SMs, a planar transformer has been favored over a wire-wound realization. The analytical design algorithm was supported by FEM simulations, where the design parameters were validated. The measurements of the magnetic parameters of the 125 custom gapped cores have shown an acceptable variation from the target value. AC dielectric withstand tests on the realized prototype have confirmed that the PD level is below the 10 pC threshold as designed for. Finally, a complete set of electrical tests have confirmed the proper operation of the ASPS in nominal conditions, at start-up and shutdown.

APPENDIX

The original concept for accounting for the fringing flux in gapped inductors was presented in 2D in [37]. Starting from a basic air-gap geometry illustrated in Fig. 27, its equivalent reluctance is calculated using the Schwarz-Christoffel transformation, resulting in:

$$\mathcal{R}_{\text{basic}} = \frac{1}{\mu_0 \left[\frac{\omega/2}{l} + \frac{2}{\pi}\left(1 + \ln\frac{\pi h}{4l}\right)\right]} \tag{16}$$

From there, more complex air-gap geometries can be obtained by an arrangement of basic air-gap geometries. In [25], an extension to pseudo 3D is made by combining the modified reluctances in two orthogonal planes whose intersection is parallel to the air-gap flux.

The combination of basic reluctances results into the following reluctance expressions on zy and zx planes (cf., Fig. 28):

$$\mathcal{R}'_{zy} = \frac{1}{\mu_0 \left\{ \frac{F/2}{l_{\text{ag}}} + \frac{2}{\pi}\left[1 + \ln\frac{\pi(D - l_{\text{ag}})}{4l_{\text{ag}}}\right]\right\}}$$

$$\mathcal{R}'_{\text{basic,down}} = \frac{1}{\mu_0 \left\{ \frac{C/2}{l_{\text{ag}}/2} + \frac{2}{\pi}\left[1 + \ln\frac{\pi(B - l_{\text{ag}}/2)}{2l_{\text{ag}}}\right]\right\}} \tag{17a}$$

$$\mathcal{R}'_{\text{basic,up}} = \frac{1}{\mu_0 \left[\frac{C/2}{l_{\text{ag}}/2} + \frac{2}{\pi}\left(1 + \ln\frac{\pi H}{2l_{\text{ag}}}\right)\right]}$$

$$\mathcal{R}'_{zx} = \frac{\mathcal{R}'_{\text{basic,up}} + \mathcal{R}'_{\text{basic,down}}}{2} \tag{17b}$$

Finally, the air-gap reluctance with fringing flux is given by:

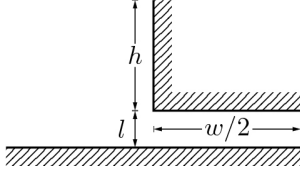$$\mathcal{R}_{\text{ag}} = \sigma_{zy}\sigma_{zx}\frac{l_{\text{ag}}}{\mu_0 C(F/2)} \tag{18}$$

Fig. 27. Basic air-gap geometry with a half-infinite plane, on which the Schwarz-Christoffel transformation is applied.

(a)   (b)
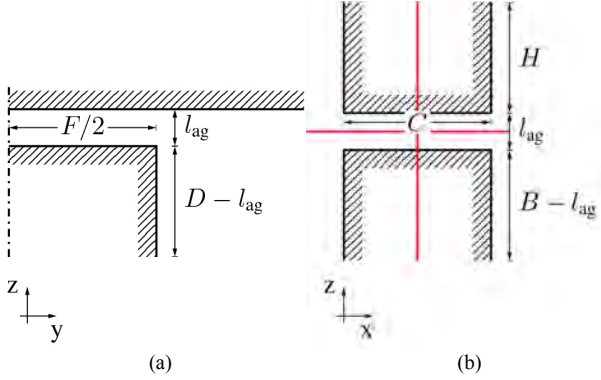
Fig. 28. Air-gap seen from: (a) The *zy* plane, which directly corresponds to $\mathcal{R}_{\text{basic}}$. (b) The *zx* plane, where four $\mathcal{R}_{\text{basic}}$ are combined according to the red separations.
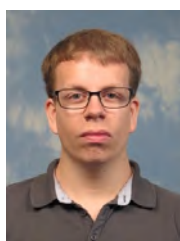
where

$$\sigma_{zy} = \frac{\mathcal{R}'_{zy}}{\dfrac{l_{\text{ag}}}{\mu_0 (F/2)}} \quad \text{and} \quad \sigma_{zx} = \frac{\mathcal{R}'_{zx}}{\dfrac{l_{\text{ag}}}{\mu_0 C}} \tag{19}$$

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