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# Comprehensive analysis and design of a quasi two-level converter leg

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# Comprehensive Analysis and Design of a Quasi Two-Level Converter Leg

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***Abstract*—Quasi two-level operation of voltage source converters, intended to operate either within high/medium voltage DC networks or low output frequency applications, has caught the attention of both academia and industry. Sequential insertion of the so-called submodules (cells) into the circuit alleviates potential problems related to high voltage slopes (d*v*/d*t*), whereas the ease of stacking them together provides the means for satisfactory performance in terms of voltage scalability. Although resembling the modular multilevel converter, quasi two-level converter operates in a different manner, leading to the completely different sizing, operating and balancing principles. So far, no publication has analyzed the transition process occurring within the quasi two-level converter leg, which can be considered crucial from the cell capacitance sizing perspective. Therefore, this paper provides thorough and generalized mathematical description of converter leg dynamics during the voltage transition process. Comprehensive method giving the possibility for cell capacitance determination is presented. With the aim of validating the conducted analysis, simulation results covering the operation of a few different topologies, with varying number of cells, are presented.**

***Index Terms*—Modular multilevel converter (MMC), quasi two-level operation, DC-DC conversion.**

## NOMENCLATURE

| | |
|---|---|
| $\Delta V_{sm}$ | Submodule voltage ripple. |
| $\gamma$ | Submodule capacitance factor of safety. |
| $\hat{i}_o$ | Leg output current peak. |
| $\varphi_{nom}$ | Nominal DAB voltage waveforms displacement. |
| $C_{req}$ | Submodule capacitance meeting a desired voltage ripple requirement. |
| $C_{sm}$ | Submodule capacitance. |
| $f_r$ | Arm current resonant frequency ($\omega_r = 2\pi f_r$). |
| $i_n$ | Lower arm current. |
| $i_o$ | Leg output current. |
| $i_p$ | Upper arm current. |
| $L_\gamma$ | Arm stray inductance. |
| $L_a$ | MMC arm inductance. |
| $L_o$ | Converter phase inductance. |
| $N$ | Number of submodules per converter arm. |
| $R_\gamma$ | Arm stray resistance. |
| $T$ | Fundamental switching period ($T = 1/f$) |
| $T_d$ | Dwell time. |
| $T_T$ | Total transition time ($T_T = NT_t$). |
| $v_{AN}$ | Leg AC voltage component. |
| $v_n$ | Lower arm instantaneous voltage. |
| $v_p$ | Upper arm instantaneous voltage. |
| $V_{in}$ | Converter input voltage. |

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## I. INTRODUCTION

IN order to operate within high voltage (HV) or medium voltage (MV) domain, two-level (2LVL) voltage source converters (VSCs) must satisfy the requirements of an application they are intended for, while withstanding substantial voltage stresses. Given the limited voltage blocking capabilities of commercially available insulated gate bipolar transistors (IGBTs), which nowadays reach as high as 6.5 kV, series connection of switching devices/converter stages appears to be inevitable for the purpose of handling HV/MV at either of the converter ports. Fig. 1(a) presents a single leg of the conventional 2LVL VSC utilizing series connection (string) of power devices with the aim of realizing the switch of a desired voltage blocking capabilities. Within such a configuration, balancing of the voltages across power devices has been considered challenging given the high likelihood of mismatch among individual power devices' parameters. On these terms, unequal voltage distribution, originating from the inevitable parameters mismatch, threatens to cause destruction of a certain device within the string. Consequently, various methods of connecting the IGBTs in series have been proposed in the literature [1]–[4]. The proposed methods rely either on the employment of balancing circuits (BCs), which are quite commonly referred to as snubbers, connected in parallel to every single device within a string or intelligent driver circuits ensuring satisfactory and safe operation of power devices or hybrid combination of the latter. Nevertheless, employment of the presented 2LVL configuration within the grid connected applications results in quite high filtering requirements, even if proper voltage balancing among the switching devices is ensured.

Multilevel topologies, such as neutral-point clamped (NPC) [5] and flying capacitor (FC) converter [6], can be perceived as an improvement compared to the conventional 2LVL VSCs within HV/MV domain owing to the better output voltage quality, reduced filtering requirements, etc. Notwithstanding the theoretical possibility of employing NPC or FC converter within this voltage range, number of bypassing diodes or flying capacitors, respectively, increases quadratically with the number of voltage levels. Hence, these multilevel topologies

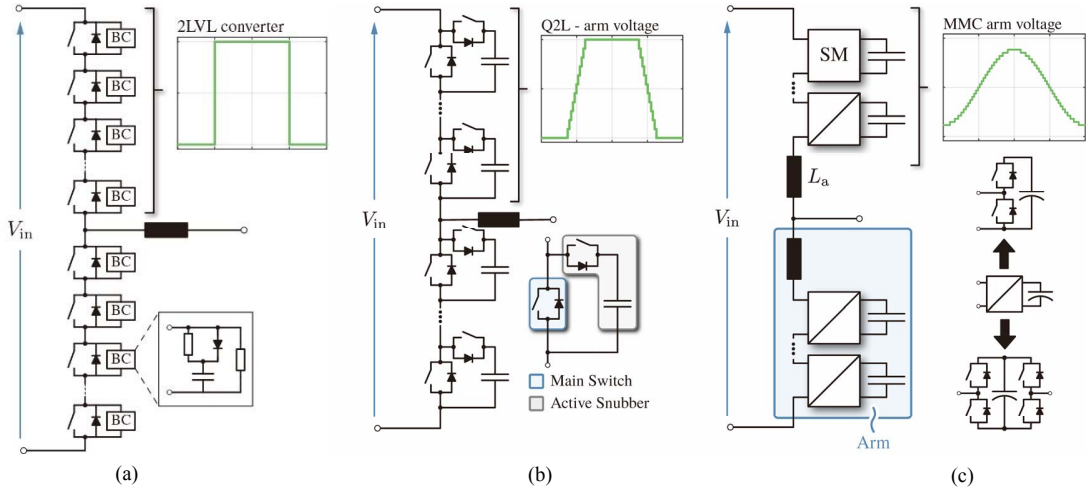
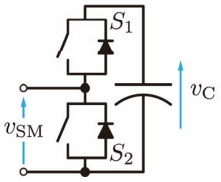



Fig. 1. (a) Series connection of power switches with the aim of handling high/medium input voltage. In order to balance voltages among the switches, RCD snubber circuits are connected in parallel to every single switching unit. (b) Quasi two-level (Q2L) converter - instead of employing passive balancing circuits in order to equalize the voltages across the employed power switches, active clamp consisting of series connection of a switch and capacitor is used. (c) Modular multilevel converter (MMC) consisting of series connection of the so-called submodules (SMs), which can be either half-bridge (HB) or full-bridge (FB). Compared to the Q2L converter, MMC utilizes intentionally installed arm inductors ($L_a$) in order to keep its relevant current components under control.

cannot be considered modular (in terms of voltage), given that new design is required for different system voltages. On the other hand, Modular Multilevel Converter (MMC) [7] presented in Fig. 1(c) enables the straightforward increase in converter's voltage handling capabilities by employing the so-called submodules (SMs), which can be either half-bridge (HB) or full-bridge (FB) depending upon the application. Namely, by stacking more of the SMs together, voltage handling capabilities of the converter increase. Further, in comparison to the standard VSCs, MMC utilizes intentionally mounted arm inductors ($L_a$) with the aim of controlling its relevant current components [8]–[10]. Normally, series connection of SMs provides the opportunity to synthesize high-quality step-wise sinusoidal voltages, therefore requiring very little or no filtering at all. Nevertheless, in order to meet requirements imposed upon the SMs voltage ripple, high capacitance is usually needed consequently increasing the size and cost of the converter. Since utilization of the HB SM can be considered sufficient for the applications falling within this paper's scope, Fig. 2 presents it along with the list of its possible states. Under normal operating conditions, two different SM states are observed. Namely, if voltage across a SM terminal equals its capacitor voltage, the SM is said to be inserted into the circuit. As opposed to insertion, a SM is said to be bypassed if voltage across its terminals equals zero.

Additional subject concerning the upcoming analysis refers to the DC systems, which have undoubtedly gained a momentum due to the advantages they have shown over their AC counterparts. With the objective of obtaining flexible and resilient DC grid, reliable connection between two of its parts operating under different voltage levels needs to be guaranteed. Consequently, DC-DC converter can be perceived as the part of the vital importance with regards to the proper operation of




List of possible HB SM states

| $S_1$ | $S_2$ | $v_{SM}$ | State |
|---|---|---|---|
| 0 | 0 | depends on $i_{arm}$ | Idle |
| 0 | 1 | 0 | Bypassed |
| 1 | 0 | $v_C$ | Inserted |
| 1 | 1 | X | Forbidden |

Fig. 2. Half-bridge submodule.

a DC system. Additionally, even though significant amount of research has been dedicated to the non-isolated DC-DC converters [11]–[16], isolation stage can still be considered mandatory within majority of applications owing to the various safety regulations. In [17] the topology based on the single-phase (1PH) dual-active bridge (DAB) [18] was presented, however it incorporated the MMC at both of its stages with the aim of obtaining the electronic tap changer. Moreover, MMC operation in the medium-frequency range was proposed, thus enabling the replacement of bulky low frequency transformer (LFT) with more compact medium frequency transformer (MFT). According to [19], increase in the MMC operating frequency results in the energy storage requirements reduction, which definitely results in the converter volume and cost cuts. However, reference [17] has not considered the adverse effects of sharp voltage transitions on the MFT insulation. Hence, quasi two-level (Q2L) operation, which was also referred to as trapezoidal operation, was proposed and analyzed in [20], [21] with the aim of realizing the three-phase (3PH) DAB. Q2L operation implies sequential insertion of SMs (or a group of SMs) into the circuit over the equidistant time intervals $T_d$ being referred to as the dwell time. Furthermore, rail-to-rail operation was proposed, meaning that all SMs within an arm are either inserted or bypassed having gone through the transition, as shown in Fig. 3. It was

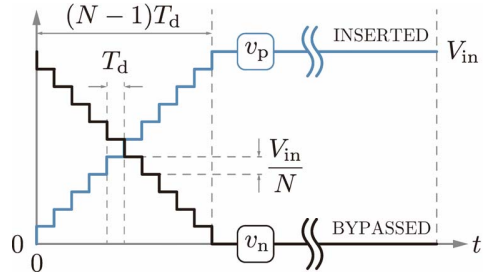



Fig. 3. Sequential insertion of SMs into the circuit. Upper and lower arm voltages were denoted by $v_p$ and $v_n$, respectively. Number of SM was denoted by $N$, whereas $T_d$ designates the dwell time.

stated that such an operation had proven to be beneficial from several points of view. Firstly, large MMC arm inductors can be removed providing proper control algorithm, which maintains SMs voltages balanced, is employed leading to the disappearance of the MMC common-mode current. In other words, either of the converter arms conducts the output current only during the half of the fundamental operating cycle, which perfectly corresponds to the conventional 2LVL VSC. Secondly, the converter SMs serve as energy buffers during, normally short, voltage transitions, meaning that once the transition is finished, current diverts to the arm being bypassed. Ultimate result of the aforementioned changes is substantial reduction in the converter SMs capacitances, which reflects positively upon spatial and cost requirements, consequently giving the Q2L converter the edge over the conventional MMC within a certain span of applications. Further, the MMC, with arm inductors being removed and operating in the Q2L mode, can also be depicted as in Fig. 1(b). Since no arm inductors are present, MMC SMs can as well be perceived as the parallel connection of the main switch and its active snubber. Apart from utilizing very small capacitors for the snubbing purposes, Q2L structure presented in Fig. 1(b) reduces the voltage slope during the converter state change compared to the conventional 2LVL counterparts. Hence, its exploitation within carrier-based modulation schemes with the aim of synthesizing low frequency output waveforms (low-speed drives as a possible application) was proposed in [22] and [23].

Despite the popularity Q2L operation mode has enjoyed lately, to the best knowledge of the authors, no publication has ever thoroughly explained converter phase current exchange between the strings of SMs, belonging to the same leg, over the voltage transition interval. Moreover, it was stated in [20] that, during the transition, a string of switches gets exposed to the converter output current which is a very strong statement given that output current actually equals the difference between upper and lower arm currents. Additionally, influence of the arm stray inductance on the transition dynamics was neglected, even though it influences the transition itself along with general converter operation, as will be seen in the upcoming sections. This paper assumes that transition period occurs according to the so-called complementary switching (CS) method despite the other methods being reported in [20]. Namely, insertion of one SM in an observed arm, implies bypassing of one SM in the adjacent arm within the same switching leg. Consequently, new resonant circuit is formed at every new dwell interval. Therefore, this paper presents thorough mathematical description of the converter leg transition process dynamics. In order to conduct the desired analysis, the circuit consisting of a single leg is used. However, all the results are presented in generalized form, hence it is possible to apply them within variety of configurations. Additionally, active snubber capacitance sizing method is presented taking into account mathematical description of the transition itself.

The outline of this paper is as follows. Section II provides piece-wise analysis of the transient process, which is afterwards followed by the derivation of analytic equations suitable for the SMs sizing purposes. Section III deals with the aforementioned sizing providing information on the algorithm employed for this matter. Finally, section IV presents simulation results obtained in PLECS. With the aim of evaluating the proposed sizing method, simulations considering the employment of various voltage class semiconductor devices within different converter configurations were conducted.

## II. Leg Transient Analysis

In order to investigate internal dynamics of the Q2L converter during its transition period, switching leg presented in Fig. 4(a) will be observed. It is assumed that voltages $v_{AN}$ and $v_s$ have the same shape and amplitude, though being shifted by a certain angle denoted by $\varphi$. During the observed transition, voltage $v_s$ remains unchanged. Converter input voltage $V_{in}$ is assumed stiff, whereas the arm stray inductance and resistance will be denoted by $L_\gamma$ and $R_\gamma$, respectively. Number of SMs within an arm of the observed converter is denoted by $N$. It is noteworthy that despite conducting the analysis in the case of single switching leg, it is easy to expand it onto all the converters utilizing Q2L operating principles. Furthermore, transition period during which the upper arm voltage $v_p$ changes from zero to full input voltage $V_{in}$, whereas the lower arm voltage $v_n$ changes in the opposite direction, according to Fig. 4(b), will be observed. Similarly to the MMC, and neglecting voltage drops across stray parameters of the converter arms, voltage $v_{AN}$ can be expressed according to (1).

$$v_{AN}=\frac{v_n - v_p}{2} \tag{1}$$

Providing there is a proper balancing algorithm employed, strings of converter SMs can be replaced by the ideal voltage sources, therefore transition analysis can be conducted observing

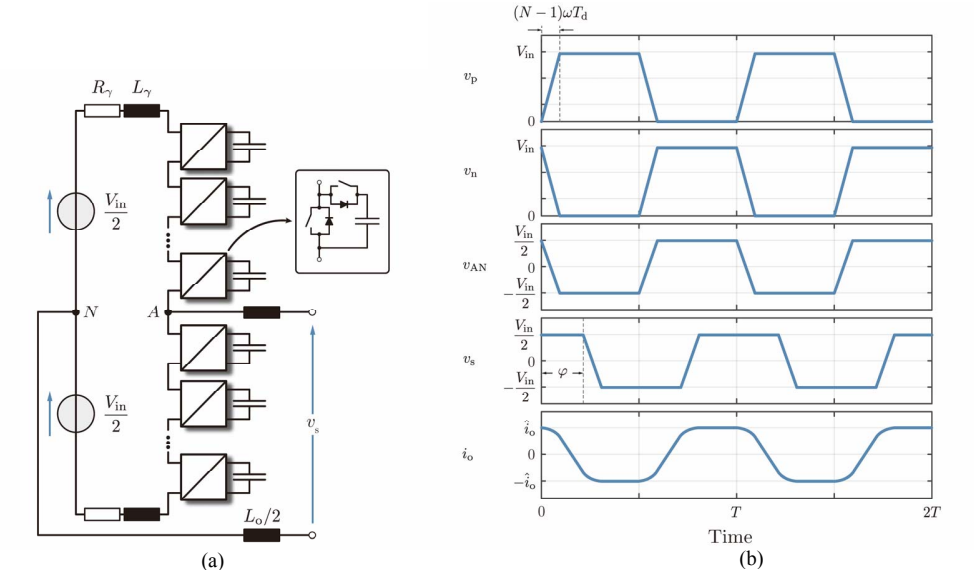



Fig. 4. (a) The circuit used to analyze Q2L converter leg transition process. Given the focus of this paper being laid on providing generalized transition analysis, all the conclusions can easily be expanded onto topologies such as single-phase DAB, three-phase DAB or Q2L VSC intended to operate within low output frequency applications. (b) Idealized converter waveforms. Voltage transitions are presented as linear for the sake of alleviating visual presentation. Upper and lower arm currents ($i_p$ and $i_n$, respectively) are not presented since they are yet to be calculated.

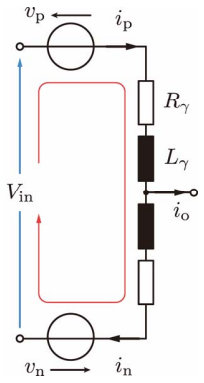



Fig. 5. Converter leg equivalent circuit. Providing proper balancing algorithm is employed, upper and lower strings of SMs can be replaced by an ideal voltage source.

the circuit presented in Fig. 5. It is noteworthy that unless balancing algorithm is employed, voltages across SMs' capacitors diverge, consequently making the converter operation unfeasible. Nevertheless, balancing algorithms differ depending upon the application the Q2L converter is used for, therefore thorough discussion covering this matter is omitted in this paper. Additionally, voltages across SMs' capacitors are not identical, however they all oscillate around the same mean value ($\overline{V_{SM}} = V_{in} / N$). Consequently, SMs' voltage ripple can be neglected, which is the common practice adopted in modelling of the MMC-alike circuits, therefore reinforcing the assumption of modeling Q2L converter arm with an ideal voltage source.

### *A. Piecewise Analysis*

Strict analysis of the Q2L converter leg transition process can be conducted observing each of the dwell intervals individually, which can be considered suitable should the calculations be performed by means of the computer. Namely, starting point of a dwell interval is considered the time axis origin ($t$ = 0), whereas an arm current/voltage initial conditions are inherited from the previously analyzed one. Finally, acquired responses are grouped together in order to obtain complete image of the transition. Considering that number of SMs within an arm equals $N$, total number of differential equations to be solved equals $N_{eq} = N$ providing voltages within the observed converter leg are expressed according to (2) and (3), where $V_0$ and $h(t)$ denote inserted SM initial voltage (which is assumed to be similar for all the SMs providing satisfactory operation of a balancing algorithm) and Heaviside step function [$\forall x \geq 0$, $h(x)$ = 1, otherwise $h(x)$ = 0], respectively.

$$v_P = \sum_{k=1}^{N} V_0 h\left[t - (k-1)T_d\right] \tag{2}$$

$$v_n = V_{in} - \sum_{k=1}^{N} V_0 h\left[t - (k-1)T_d\right] \tag{3}$$

Differential equation describing an observed converter leg can be written for every interval $(k-1)T_d < t \leq k\,T_d$, where $k \in [1, N]$. According to Fig. 5, KVL labeled by red can be formed, from which (4) follows. Both $v_p$ and $v_n$ actually represent series connection of SMs, however with different number of them being inserted into the loop.

$$V_{in} = L_\gamma \frac{d}{dt}\left(i_p + i_n\right) + R_\gamma \left(i_p + i_n\right) + v_p + v_n \tag{4}$$

Differentiating (4), while keeping basic capacitor voltage equation ($i_c = C\frac{dv_C}{dt}$) in mind, leads to

$$0 = L_\gamma \frac{d^2}{dt^2}\left(i_p + i_n\right) + R_\gamma \frac{dt}{dt}\left(i_p + i_n\right) + k\frac{i_p}{C} + (N - k)\frac{i_n}{C} \tag{5}$$

Further, by following the arm current directions defined in Fig. 5, (6) can be derived.

$$\begin{aligned} 0 = {} & 2L_\gamma \frac{d^2}{dt^2} i_p + 2R_\gamma \frac{dt}{dt} i_p + \frac{N}{C} i_p - \ldots \\ & \ldots - \left(L_\gamma \frac{d^2}{dt^2} i_o + R_\gamma \frac{d}{dt} i_o + \frac{N - k}{C} i_o\right) \end{aligned} \tag{6}$$

From (6) one can see that the converter leg output current definitely affects its inner dynamics, hence it needs to be further investigated. Fig. 4(a) and (b) depict the circuit to be analyzed along with ideal current and voltage waveforms which are to be used in the forthcoming analysis. Based on Fig. 4(a), along with (1)–(3), one can easily derive (7), where it is assumed that every SM voltage remains balanced around the value $V_{in}/N$, which is in accordance with the basic operating principles of MMC-alike circuits. Within subsection II-B, it will be shown that (7) can be generalized, therefore allowing for the analysis of various topologies by means of equations differing with respect to each other only by a single coefficient.

$$\begin{aligned} L_o \frac{di_o}{dt} &= V_{in}\frac{(N - k) - k}{2N} - \frac{V_{in}}{2} \\ &= -k\frac{V_{in}}{N} \end{aligned} \tag{7}$$

Now, (6) can be transformed utilizing (7).

$$\begin{aligned} 0 = {} & 2L_\gamma \frac{d^2}{dt^2} i_p + 2R_\gamma \frac{d}{dt} i_p + \frac{N}{C} i_p - \ldots \\ & \ldots - \Bigg(\underbrace{L_\gamma \frac{d^2}{dt^2} i_o}_{=0} + \underbrace{R_\gamma \frac{d}{dt} i_o}_{=-k\frac{R_\gamma V_{in}}{NL_o}} + \frac{N - k}{C} i_o\Bigg) \end{aligned} \tag{8}$$

Transposing (8) into the Laplace domain yields

$$\begin{aligned} 0 = {} & \underbrace{2L_\gamma\left[s^2 i_p(s) - s\cdot i_p\big|_{(k-1)T_d} - \frac{di_p}{dt}\Big|_{(k-1)T_d}\right]}_{Part\ 1} + \ldots \\ & \underbrace{\ldots + 2R_\gamma\left[s i_p(s) - i_p\big|_{(k-1)T_d}\right] + \frac{N}{C} i_p(s) - \ldots}_{Part\ 2} \\ & \underbrace{\ldots - \left\{\frac{N - k}{sC}\left[i_o\big|_{(k-1)T_d} - k\frac{V_{in}}{sNL_o}\right] - k\frac{R_\gamma V_{in}}{sNL_o}\right\}}_{Part\ 3} \end{aligned} \tag{9}$$

Analyzing (9), one can notice that Parts 1 and 2 depend upon initial condition which is subject to changes every time a new dwell interval commences. However, these two parts combined represent the differential equation with constant parameters. Part 3 is actually introducing the effect of variable capacitance into the circuit (the term $C / (N - k)$). Given that (9) represents the second order differential equation, it is clear that response of the circuit it represents implies the existence of oscillations. Nevertheless, every time new transition interval commences, natural frequency of the circuit changes. Moreover, circuit formed within a transition interval oscillates in its natural manner only during the observed dwell interval. With the observed dwell interval being finished, new circuit is formed using new parameters and new voltage/current initial conditions, as presented in Fig. 6. To get a better insight into the previous discussion, Fig. 7 presents upper arm current transition within the converter depicted in Fig. 4(a). Additionally, transition period during which the upper arm voltage changes from zero to full input voltage is observed. Converter parameters used for the purpose of conducting presented calculations can be found in Table I. Fig. 7 contains several different plots, assuming 1.7 kV, 3.3 kV and 6.5 kV IGBT modules were employed. Accordingly, dwell times were adjusted to match the approximate practical deadtimes for a given voltage class. Number of SMs within an arm was determined so that the average voltage across a SM capacitor equals around 55% of an employed semiconductor voltage class, as summarized in Table II. Plots on the right-hand side of Fig. 7 present the upper devices. Arm current behavior during the transition process assuming stray inductance and SM capacitance were increased by the factor of 100. Normalization with the maximum arm current being adopted as the base value was performed. Converter utilizing increased passive components approaches the MMC, which can be concluded given the negligible arm current changes during the transition period. Despite the fact that the line between the Q2L converter and the MMC has not been distinctively drawn, it is clear from Fig. 7 that the higher the arm inductance along with SM capacitance, the lower the resonant frequency of the converter leg, therefore the lower the changes in its current originating from any transition processes. However, this interferes with the basic principles of Q2L operation mode. Unless conventional MMC operation is to be achieved, one should carefully design the converter circuit with the aim of minimizing the arm stray inductance from which the SM capacitance can be determined. Otherwise, branch output current drift from one arm to another takes too long and Q2L operation becomes unfeasible. Please notice that the lower arm current can be easily calculated as $i_n = i_p - i_o$, hence analysis of the upper arm can be considered sufficient. For a known arm stray inductance, piece-wise calculation of arm currents can be utilized with the aim of minimizing SM capacitance which meets the requirements related to its voltage ripple under the most critical operating conditions, which implies the operation with maximal arm currents, while providing conditions to maintain the operation fulfilling Q2L principles. An alternative to piece-wise observation of the Q2L converter leg transition can be found within

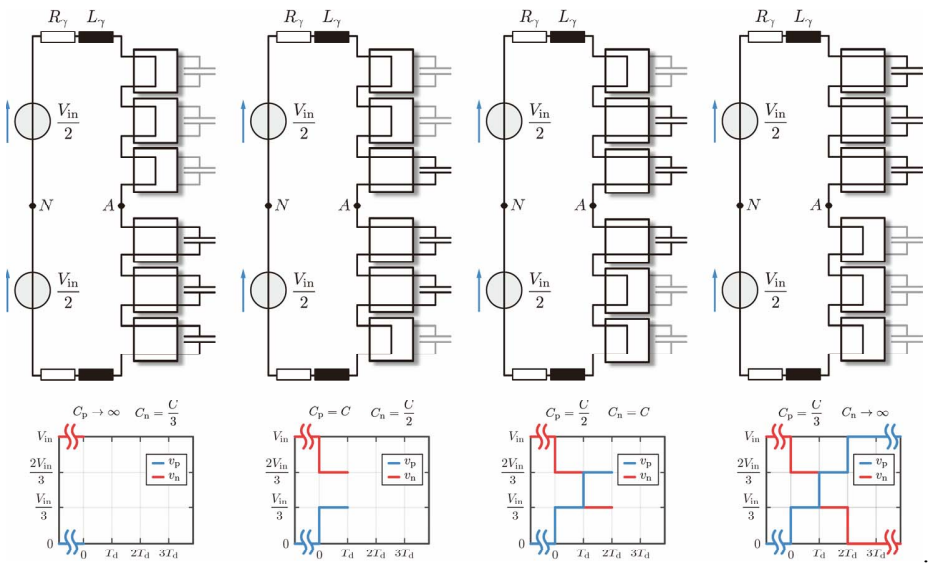



Fig. 6. Q2L converter leg transition process in case $N = 3$. It can be seen that an arm equivalent capacitance changes depending on the leg switching stage, which introduces resonances with different natural frequencies. Hence, every dwell interval can be analyzed individually with new differential equations being taken into account. Please, keep in mind that exemplary cell insertion order depicted above was used for the presentation purposes only. Generally, it depends on the balancing algorithm, which is out of this paper's scope.

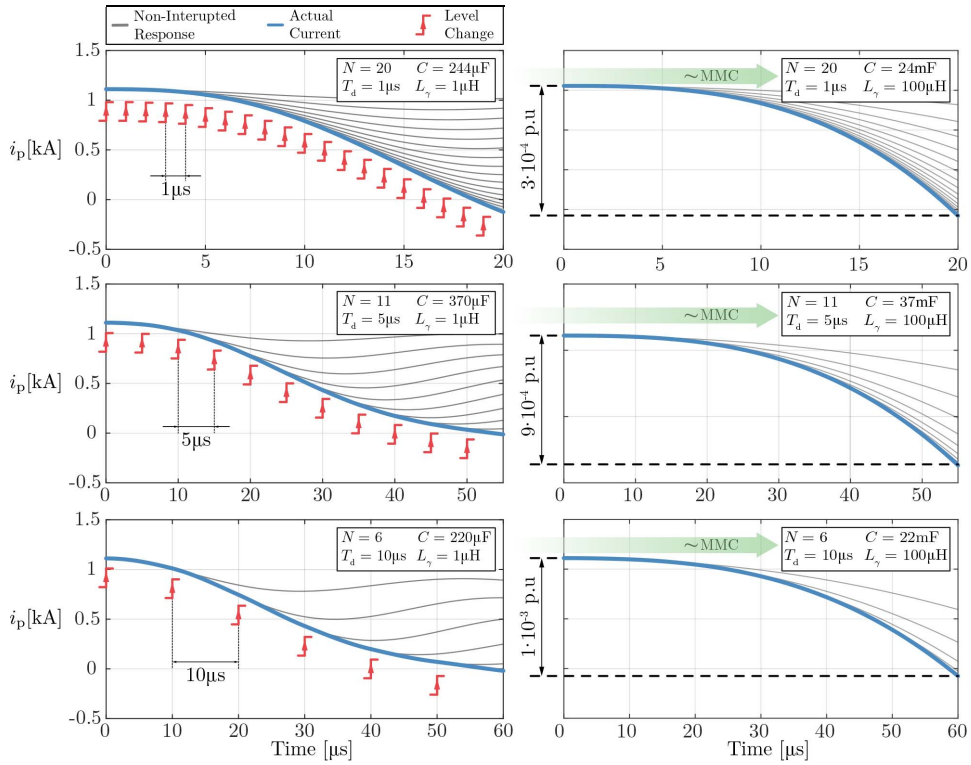



Fig. 7. Upper arm current behavior during the transition process concerning different semiconductor voltage classes being employed (left). Level changes, indicated by red, correspond to the insertion of one SM within the upper arm along with the bypassing of one SM within the lower arm. It can be seen that as long as the new level change is not triggered, the arm current oscillates along the so-called non-interrupted response curve. Insertion of a new SM into the circuit changes the arm resonant parameters, meaning that the new non-interrupted response curve is established and followed until the next insertion takes place; Upper arm current behavior during the transition process providing arm stray inductance and SM capacitance were increased by the factor of 100 (right). The arm current was normalized with respect to its maximum value. Please notice that such an increase leads to the behavior recognized within the conventional MMC (considering that the arm current exhibits negligible change during the voltage transition period), which is in contrast to the basic principles of Q2L operating mode. Therefore, if Q2L operation is to be achieved without any additional common-mode currents control, arm stray inductance should be minimized and SM capacitance sized accordingly. Dwell times and number of cells were adjusted accordingly, depending upon the voltage class of the employed switching devices.

TABLE I
PARAMETERS OF THE CONVERTER USED TO SHOWCASE THE BEHAVIOR OF ITS UPPER ARM CURRENT DURING THE VOLTAGE TRANSITION PROCESS

| Parameter | Annotation | Value |
|---|---|---|
| Input voltage | $V_{in}$ | 20 kV |
| Rated power | $P$ | 10 MW |
| Operating frequency | $f$ | 250 Hz |
| Stray inductance | $L_\gamma$ | 1 $\mu$H |
| Stray resistance | $R_\gamma$ | 40 m$\Omega$ |
| Output inductance | $L_o$ | 1.8 mH |

TABLE II
NUMBER OF SMS EMPLOYED DEPENDING UPON SEMICONDUCTORS VOLTAGE CLASS

| Voltage class (kV) | Number of SMs | Dwell time ($\mu$s) | SM capacitance ($\mu$F) |
|---|---|---|---|
| 1.7 | 20 | 1 | 244 |
| 3.3 | 11 | 5 | 370 |
| 6.5 | 6 | 10 | 220 |

the analytic calculations, as presented in the following subsection.

### *B. Analytical Solution*

It is worth restating that the assumption of balancing algorithm, which keeps SMs voltages within predefined limits, existence holds. Hence, average voltage across each SM can be assumed as $V_{sm} = V_{in}/N$. In order to conduct the analysis of the Q2L converter arm current behavior, transition at which the upper arm voltage exhibits the change from zero to full converter input voltage will be observed. Please note that, in accordance with Fig. 4(b), lower arm voltage changes in the opposite direction. With the aim of deriving upper arm current equation, knowing the shape of voltages $v_p$ and $v_n$, from Fig. 5, is necessary. Time instant at which the transition commences will be adopted as the time axis origin ($t = 0$), whereas the total transition time will henceforth be considered as $T_T = NT_d$.

*1)Upper arm voltage*: Providing SMs insertion occurs sequentially in time instants matching the dwell time $T_d$, as presented in Fig. 3, during the interval $mT_d \le t < (m + 1)T_d$, where $m \in [0, N-1]$, instantaneous value of the upper arm voltage $v_p$ can be calculated according to (10). With the aim of making the equations less cumbersome, $floor\left(\frac{t}{T_d}\right)$ will be denoted by $m$.

$$v_P = V_{c0}h(t) + \frac{1}{C}\int_0^t i_p\,dt + V_{c0}h(t - T_d) + \dots + \frac{1}{C}\int_{T_d}^t i_p\,dt + V_{c0}h(t - mT_d) + \int_{mT_d}^t i_p\,dt \qquad (10)$$

Grouping the similar terms within (10), yields

$$v_P = \underbrace{\sum_{k=0}^{m} V_{c0}h(t - kT_d)}_{v_P^{(1)}} + \underbrace{\frac{1}{C}\sum_{k=0}^{m}\left[\int_{kT_d}^t i_p(\tau)d\tau\right]}_{v_P^{(2)}} \qquad (11)$$

It can be seen from (11), that the upper arm voltage can be expressed as sum of two terms which can be further inspected.

$$v_P^{(1)} = \sum_{k=0}^{m} V_{c0}h(t - kT_d) = \frac{V_{in}}{NT_d}\sum_{k=0}^{m} h(t - kT_d)\,T_d \qquad (12)$$

Practical values of the dwell time $T_d$ fall in the range of several microseconds. Therefore, with respect to the fundamental operating period of the converter, the dwell time can, to a certain extent, be perceived as time increment ($T_d \to d\tau$), whereas the term $kT_d$ can be considered almost continuous, therefore representing time ($kT_d \to \tau$). Consequently, sum can be replaced with integral ($\Sigma \to \int$), leading to (13). It is noteworthy that the shorter the dwell time, the higher the precision of the results acquired using the above simplification. Additionally, by using the basic property of Heaviside step function, given by (14), (13) can be rearranged to (15). The above analysis can be graphically perceived according to Fig. 8.

$$v_P^{(1)} = \frac{V_{in}}{T_T}\int_{\tau=0}^t h(t - \tau)d\tau \qquad (13)$$

$$h(x) = \begin{cases} 1, & x \ge 0 \\ 0, & \text{otherwise} \end{cases} \qquad (14)$$

$$v_P^{(1)} = \frac{V_{in}}{T_T}t \cdot h(t) \qquad (15)$$

Applying the same reasoning to the second term in (11) provides

$$v_P^{(2)} = \frac{N}{CT_T}\int_0^t\left[\int_{\xi=\tau}^t i_p(\xi)d\xi\right]d\tau \qquad (16)$$

Finally, at any time instant fulfilling the condition $t < T_T$, upper arm voltage can be approximated as

$$v_P = \frac{V_{in}}{T_T}t \cdot h(t) + \frac{N}{CT_T}\int_0^t\left[\int_{\xi=\tau}^t i_p(\xi)\,d\xi\right]d\tau \qquad (17)$$

*2) Lower arm voltage*: Observing idealized voltage waveforms

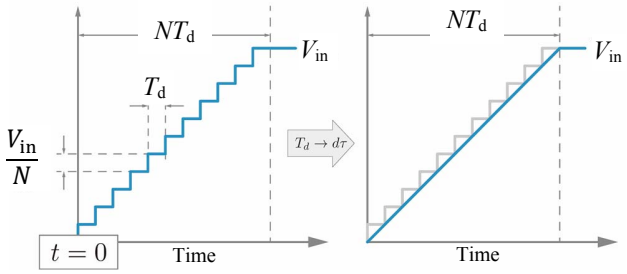



Fig. 8. Effect of linearization process.

given by Fig. 3, instantaneous value of the lower arm voltage can be expressed as

$$v_n = V_{C0}[(N-1)h(t) - h(t-T_d) - h(t-mT_d)] + \cdots + \frac{N-1}{C}\int_0^{T_d} i_n(\tau)d\tau + \frac{N-2}{C}\int_{T_d}^{2T_d} i_n(\tau)d\tau + \cdots + \frac{N-(m+1)}{C}\int_{mT_d}^{t} i_n(\tau)d\tau \quad (18)$$

Following the analysis already presented above, two terms $v_n^{(1)}$ (the first line of the above expression) and $v_n^{(2)}$ (second and third line combined) can be identified.

$$v_n^{(1)} = V_{in}h(t) - \frac{V_{in}}{T_T}\sum_0^m h(t-kT_d)\,T_d \quad (19)$$

Approximation techniques applied within the paragraph devoted to the upper arm voltage determination can be reapplied here, leading to

$$v_n^{(1)} = V_{in}\left(1 - \frac{t}{T_T}\right) \quad (20)$$

As for the other term from (18), it can be noticed from (21) that it can as well be presented with two separate terms $v_n^{(2,1)}$ and $v_n^{(2,2)}$, respectively.

$$v_n^{(2)} = \underbrace{\frac{N}{C}\left(\int_0^{T_d} i_n d\tau + \int_{T_d}^{2T_d} i_n d\tau + \ldots + \int_{mT_d}^{t} i_n d\tau\right)}_{v_n^{(2,1)}} - \cdots \underbrace{- \frac{1}{C}\left[\int_0^{T_d} i_n d\tau + 2\int_{T_d}^{2T_d} i_n d\tau + \ldots + (m+1)\int_{mT_d}^{t} i_n d\tau\right]}_{v_n^{(2,2)}} \quad (21)$$

Sum of integrals $v_n^{(2,1)}$ in the expression above represents integral of the lower arm current over time (22).

$$v_n^{(2,1)} = \frac{N}{C}\int_0^t i_n(\tau)d\tau \quad (22)$$

Upper limit of the integral within the sum in (23), should be paid attention to. It can be seen that the last term of the integral sum from (21) considers the integral with the lower limit equal to $mT_d$ and the upper one equal to the observed time instant $t$. However, if $T_d$ is considered significantly small, it can be claimed that the error committed by extending the limit of the last integral within the sum in (23) to $kT_d$ will not introduce large computational error into the calculations (the purpose of this being simplification of mathematical operations to be performed).

$$v_n^{(2,2)} = \frac{N}{CT_T}\sum_{k=1}^{m+1} k\left[\int_{(k-1)T_d}^{kT_d} i_n dt\right] T_d \quad (23)$$

Further, it can as well be claimed that the lower arm current will not significantly change during the dwell interval, providing $T_d$ being considered infinitely small ($d\tau$). Hence, the integral within the previous equation can be solved in a simplified manner (24).

$$v_n^{(2,2)} = \frac{N}{CT_T}\sum_{k=0}^{m+1} (kT_d)\, i_n T_d \quad (24)$$

Once again, $T_d$ can be translated into the time increment $d\tau$, leading to

$$v_n^{(2,2)} = \frac{N}{CT_T}\int_0^t \tau i(\tau)\,d\tau \quad (25)$$

Finally, combining (20), (22) and (25) leads to the instantaneous value of the lower arm voltage during the observed transition period.

$$v_n = V_{in}\left(1 - \frac{t}{T_T}\right) + \frac{N}{C}\int_0^t i_n(\tau)d\tau - \frac{N}{CT_T}\int_0^t \tau i(\tau)d\tau \quad (26)$$

$$\frac{d}{dt}\left[\int_{a(t)}^{b(t)} f(t,\tau)d\tau\right] = f[t, b(t)]\frac{db(t)}{dt} - f[t, a(t)]\frac{da(t)}{dt} + \int_{a(t)}^{b(t)} \frac{\partial}{\partial t} f(t,\tau)d\tau \quad (27)$$

Once the voltages across the Q2L converter arms are known, upper/lower arm currents can be evaluated as well. Motivation for expressing voltage equations by virtue of integral terms lies within the fact that Laplace transform can be applied, and all equations solved in the continuous domain even though voltage transition occurs in discretely defined time steps. In other words, no piecewise solutions are necessary once the analytical solutions defining arm currents within the time frame defined as $t \in [0, T_T]$ are derived.

*3) Arm current determination*: In order to derive arm currents during the Q2L converter transition process, derivatives of the upper and lower arm voltages ( $\frac{\mathrm{d}v_\mathrm{p}}{\mathrm{d}t}$ and $\frac{\mathrm{d}v_\mathrm{n}}{\mathrm{d}t}$, respectively) need to be calculated (28)–(29).

$$\frac{\mathrm{d}v_\mathrm{p}}{\mathrm{d}t}=\frac{\mathrm{d}}{\mathrm{d}t}\left\{\frac{V_\mathrm{in}}{T_\mathrm{T}}t\cdot h(t)+\frac{N}{CT_\mathrm{T}}\int_0^t\left[\int_{\xi=\tau}^t i_\mathrm{p}(\xi)\mathrm{d}\xi\right]\mathrm{d}\tau\right\} \tag{28}$$

$$\frac{\mathrm{d}v_\mathrm{n}}{\mathrm{d}t}=\frac{\mathrm{d}}{\mathrm{d}t}\left[V_\mathrm{in}\left(1-\frac{t}{T_\mathrm{T}}\right)+\frac{N}{C}\int_0^t i_\mathrm{n}(\tau)\mathrm{d}\tau-\ldots \right.$$
$$\left.\ldots-\frac{N}{CT_\mathrm{T}}\int_0^t\tau\, i(\tau)\mathrm{d}\tau\right] \tag{29}$$

It can be seen from (28) that calculating the derivative of its second term is not that straightforward due to the existence of double integral. However, Leibnitz integral rule defined by (27) can be used for the purpose of conducting the desired differentiation.

Another mathematical relation defined by (30) will also be recalled to calculate the derivatives of the upper and lower arm voltages.

$$\frac{\mathrm{d}}{\mathrm{d}t}\int_a^t f(\tau)\ \mathrm{d}\tau=f(t) \tag{30}$$

By combining (27)–(30), needed derivatives can be calculated as

$$\frac{\mathrm{d}v_\mathrm{p}}{\mathrm{d}t}=\frac{V_\mathrm{in}}{T_\mathrm{T}}+\frac{N}{CT_\mathrm{T}}\,t\,i_\mathrm{p} \tag{31}$$

$$\frac{\mathrm{d}v_\mathrm{n}}{\mathrm{d}t}=-\frac{V_\mathrm{in}}{T_\mathrm{T}}-\frac{N}{CT_\mathrm{T}}ti_\mathrm{p}+\frac{N}{C}i_\mathrm{p}-\frac{N}{C}i_\mathrm{o}+\frac{N}{CT_\mathrm{T}}\,t\,i_\mathrm{o} \tag{32}$$

Adding (31) and (32) yields

$$\frac{\mathrm{d}(v_\mathrm{n}+v_\mathrm{p})}{\mathrm{d}t}=\frac{N}{C}i_\mathrm{p}-\frac{N}{C}i_\mathrm{o}+\frac{N}{CT_\mathrm{T}}t\,i_\mathrm{o} \tag{33}$$

Equation (33) suggests that upper/lower arm current dynamics also depends on the branch output current dynamics. It can be shown that voltage across Q2L converter phase inductor $L_\mathrm{o}$ can be calculated according to (34). One can also notice that approximately linear change of voltage over the output inductor occurs due to the sequential change of upper and lower arm voltages within the observed converter branch.

$$v_{L_\mathrm{o}}=-\rho\frac{V_\mathrm{in}}{T_\mathrm{T}}\,t \tag{34}$$

Hence, output current dynamics during the Q2L leg voltage transition process can be described with

$$\frac{\mathrm{d}i_\mathrm{o}}{\mathrm{d}t}=-\rho\frac{V_\mathrm{in}}{L_\mathrm{o}T_\mathrm{T}}\,t \tag{35}$$

where,

$$\rho=\begin{cases}1, & \text{1PH-DAB HB config.}\\ 2, & \text{1PH-DAB FB config.}\\ \frac{2}{3}, & \text{3PH-DAB.}\end{cases}$$

In (35), coefficient $\rho$ changes depending on the analyzed circuit configuration, which can be seen in Fig. 9. In case Q2L VSC intended for low output frequency operation is observed, coefficient $\rho$, from the equation above, can be considered equal to zero, providing fundamental switching period of the converter itself is sufficiently small compared to the output current frequency (for instance, 200 Hz switching frequency employed to synthesize 1 Hz output current). In order to solve the equation obtained by differentiating (4), it comes in handy to observe all of its quantities in the Laplace domain. Therefore, output current Laplace transform can be expressed as (36) assuming converter phase current flows exclusively through the upper arm prior to entering the transition process, according to Fig. 4(b).

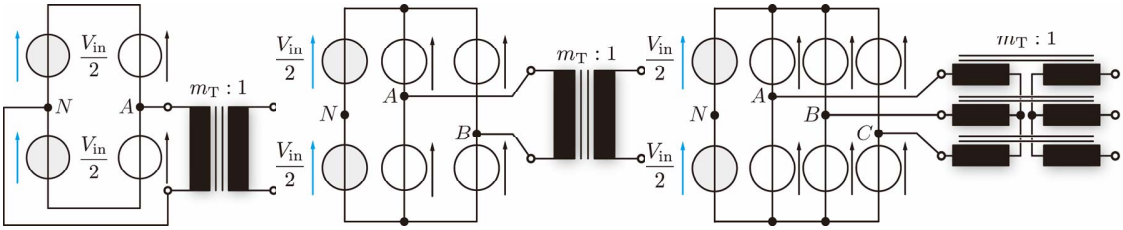
$$I_\mathrm{o}(s)=\frac{\hat{i}_\mathrm{o}}{s}-\frac{\rho V_\mathrm{in}}{s^3L_\mathrm{o}T_\mathrm{T}} \tag{36}$$

In the above equation, current flowing through the upper arm of the Q2L converter switching leg at the moment the transition interval commences was denoted by $\hat{\imath}_\mathrm{o}$. Its value also depends upon the analyzed configuration, according to (37), where $\varphi$ denotes relevant voltage waveforms phase-shift in case DAB-alike topologies are analyzed. If, however, low output frequency applications were subject to analysis, output frequency, output current amplitude and power factor, are denoted by $f_\mathrm{o}$, $I_\mathrm{max}$ and $\cos(\psi)$, respectively.

$$\hat{\imath}_\mathrm{o}=\begin{cases}\frac{1}{2}\frac{V_\mathrm{in}}{\omega L_\mathrm{o}}\varphi, & \text{1PH-DAB HB config.}\\ \frac{V_\mathrm{in}}{\omega L_\mathrm{o}}\varphi, & \text{1PH-DAB HB config.}\\ \frac{1}{3}\frac{V_\mathrm{in}}{\omega L_\mathrm{o}}\varphi, & \text{3PH-DAB}\\ I_\mathrm{max}, & \text{LF operation.}\end{cases} \tag{37}$$

Lower arm current $i_\mathrm{n}$ can be expressed as the difference between upper arm current and branch output current. Consequently, the upper arm current dynamics can be described with (38).

$$0=\underbrace{2L_\gamma\frac{\mathrm{d}^2i_\mathrm{p}}{\mathrm{d}t^2}+2R_\gamma\frac{\mathrm{d}i_\mathrm{p}}{\mathrm{d}t}+\frac{N}{C}i_\mathrm{p}}_{\textit{Part 1}}-\ldots$$
$$\ldots-\underbrace{\left(L_\gamma\frac{\mathrm{d}^2i_\mathrm{o}}{\mathrm{d}t^2}+R_\gamma\frac{\mathrm{d}i_\mathrm{o}}{\mathrm{d}t}+\frac{N}{C}i_\mathrm{o}-\frac{N}{CT_\mathrm{T}}\,t\,i_\mathrm{o}\right)}_{\textit{Part 2}} \tag{38}$$




(a) Half-Bridge configuration (b) Full-Bridge configuration (c) Three-Phase configuration

Fig. 9. Circuit configurations used to investigate Q2L converter arm current behavior. Depending upon the application, all topologies can be employed as either the DAB or with the aim of synthesizing low output frequency waveforms. String of SMs was represented with ideal voltage sources.

With the aim of transposing (38) into the s-domain, property defined by (39) is used, consequently leading to (40).

$$\mathcal{L}\left[tf(t)\right] = -\frac{\mathrm{d}F(s)}{\mathrm{d}s} \tag{39}$$

$$I_{\mathrm{p}}(s) = \frac{a_5 s^5 + a_4 s^4 + a_3 s^3 + a_2 s^2 + a_1 s + a_0}{b_6 s^6 + b_5 s^5 + b_4 s^4} \tag{40}$$

where,

$$\begin{aligned}
a_5 &= 2C\hat{i}_{\mathrm{o}} L_\gamma L_{\mathrm{o}} T_{\mathrm{T}}^2 \\
a_4 &= 2C\hat{i}_{\mathrm{o}} R_\gamma L_{\mathrm{o}} T_{\mathrm{T}}^2 \\
a_3 &= \hat{i}_{\mathrm{o}} N L_{\mathrm{o}} T_{\mathrm{T}}^2 - C L_\gamma T_{\mathrm{T}} V_{\mathrm{in}} \rho \\
a_2 &= -\hat{i}_{\mathrm{o}} N L_{\mathrm{o}} T_{\mathrm{T}} - C R_\gamma T_{\mathrm{T}} V_{\mathrm{in}} \rho \\
a_1 &= -N T_{\mathrm{T}} V_{\mathrm{in}} \rho \\
a_0 &= 3N V_{\mathrm{in}} \rho \\
b_6 &= 2C L_\gamma L_{\mathrm{o}} T_{\mathrm{T}}^2 \\
b_5 &= 2C L_{\mathrm{o}} L_\gamma T_{\mathrm{T}}^2 \\
b_4 &= L_{\mathrm{o}} N T_{\mathrm{T}}^2 .
\end{aligned}$$

Expression (40) can be split into two parts representing different time domain responses (41). First part of (41) indicates that the upper arm current response to the voltage excitation defined by (33) represents a sum of cubic, square and linear function and a constant term. Second fraction within (41) represents a sinusoidal function.

$$\begin{aligned}
i_{\mathrm{p}}(s) &= \frac{a_5 s^5 + a_4 s^4 + a_3 s^3 + a_2 s^2 + a_1 s + a_0}{b_6 s^6 + b_5 s^5 + b_4 s^4} \\
&= \underbrace{\frac{p_3 s^3 + p_2 s^2 + p_1 s + p_0}{s^4}}_{\textit{Qubic + Square + Linear + Constant Term}} + \underbrace{\frac{q_1 s + q_0}{b_6 s^2 + b_5 s + b_4}}_{\textit{Sinusoidal Term}}
\end{aligned} \tag{41}$$

Accordingly, inverse Laplace transform of (41) can be represented in the form of (42), with all the coefficients being defined by (43) and (44).

$$\begin{aligned}
\mathcal{L}^{-1}\left[i_{\mathrm{p}}(s)\right] &= Q_4\left(Q_3 t^3 + Q_2 t^2 + Q_1 t + Q_0\right) + \ldots \\
&\cdots + e^{-\frac{R_\gamma}{2L_\gamma}} S_3 \left[S_1 \sin(\omega_r t) + S_2 \cos(\omega_r t)\right]
\end{aligned} \tag{42}$$

Since (43) and (44) are quite cumbersome, it would be useful to graphically examine the effect of certain factors on the upper/lower arm current shape during the voltage transition period. For that matter, converter operating with parameters provided in Table I is observed. However, three different arm stray inductance values were used with the aim of conducting the analysis of desired response components, whereas SMs capacitance was fixed at $C_{\mathrm{sm}}$ = 370 $\mu$F (this value was set according to the sizing algorithm, which is to be presented shortly). Number of SMs per arm was set as $N$ = 11. Fig. 10 presents upper arm current during the voltage transition period for three different arm stray inductances. It can be seen that the higher the stray inductance, the more emphasized the effect of the sinusoidal component within the current response. This is, to a certain extent, logical given that for, a fixed SM capacitance, higher inductance reduces natural frequency of all the oscillations occurring within the observed circuit. With the aim of getting an insight into the effect of the afore-mentioned stray inductance upon the arm currents over the complete fundamental operating period, circuits utilizing parameters defined within Fig. 10 were simulated in PLECS. It can be seen from Fig. 11 that with an increase in the arm stray inductance (moving from left to right in Fig. 11) arm current oscillations become more emphasized, both in terms of duration and the overshoot. Additionally, the higher the stray inductance the more time the arm current needs to drift from one arm to another, therefore increasing the need for larger SM capacitance with the aim of keeping its voltage within a predefined limit. During the previously conducted analysis, it was assumed that converter input voltage was stiff. However, certain capacitive filter at converter input stage would be inevitable in practice. Last but not least, if the arm stray inductance were unreasonably high, the arm current drift would not manage to occur prior to the following voltage transition,

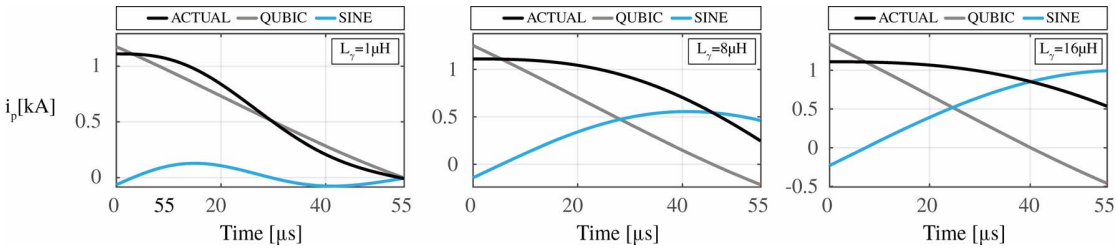



Fig. 10. Effect of the arm stray inductance on the upper arm current components. The number of converter SMs was set as $N = 11$, whereas its capacitance was set as $C = 370\ \mu$F. It can be seen that the increase in the arm stray inductance increases both period and amplitude of the sinusoidal component. Moreover, non-sinusoidal part of (42) tends to be less sensitive to stray inductance changes.

$$
\begin{aligned}
Q_0 &= \rho V_{\text{in}}\left[(2CL_\gamma N^2 - 4C^2NR_\gamma^2)T_\text{T} - 48C^3R_\gamma^3 + 48C^2L_\gamma NR_\gamma\right] + 2\hat{i}_\text{o}L_\text{o}N^3T_\text{T}^2 + 4C\hat{i}_\text{o}L_\text{o}N^2R_\gamma T_\text{T} \\
Q_1 &= \rho V_{\text{in}}\left(2CN^2R_\gamma T_\text{T} + 24C^2NR_\gamma^2 - 12CL_\gamma \text{N}^2\right) - 2\hat{i}_\text{o}L_\text{o}N^3T_\text{T} \\
Q_2 &= -\rho V_{\text{in}}\left(N^3T_\text{T} + 6CN^2R_\gamma\right) \\
Q_3 &= \rho V_{\text{in}}N^3 \\
Q_4 &= \frac{1}{2L_\text{o}N^3T_\text{T}^2}
\end{aligned}
\tag{43}
$$

$$
\begin{aligned}
S_1 &= \rho V_{\text{in}}\left[(2C^3NR_\gamma^3 - 3C^2L_\gamma N^2R_\gamma)T_\text{T} + 24C^4R_\gamma^4 - 48C^3L_\gamma NR_\gamma^2 + 12C^2L_\gamma^2N^2\right] + \cdots \\
&\quad \cdots + \left(2C\hat{i}_\text{o}L_\gamma L_\text{o}N^3 - 2C^2\hat{i}_\text{o}L_\text{o}N^2R_\gamma^2\right)T_\text{T} \\
S_2 &= \left\{\rho V_{\text{in}}\left[\left(2C^2NR_\gamma^2 - CL_\gamma N^2\right)T_\text{T} + 24C^3R_\gamma^3 - 24C^2L_\gamma NR_\gamma\right] - 2C\hat{i}_\text{o}L_\text{o}N^2R_\gamma T_\text{T}\right\}\sqrt{2CL_\gamma N - C^2R_\gamma^2} \\
S_3 &= \frac{1}{L_\text{o}N^3T_\text{T}^2\sqrt{2CL_\gamma N - C^2R_\gamma^2}} \\
\omega_\text{r} &= \frac{\sqrt{2CL_\gamma N - C^2R_\gamma^2}}{2CL_\gamma}
\end{aligned}
\tag{44}
$$

therefore basic principles of the Q2L operation mode would be violated and converter operation approaches the MMC. Hence, during the converter design phase, efforts to keep the arm stray inductance as low as possible should be made.

## III. Submodule Capacitor Sizing

Figs. 10 and 11 demonstrated the adverse effect high arm stray inductance has on the Q2L converter operation. Consequently, for known branch parameters, SM capacitance needs to be determined such that a compromise between its desired voltage ripple and Q2L operation can be made. Fig. 12 presents idealized upper arm current during the voltage transition period. In the beginning of the transition interval, one SM within the upper arm gets inserted into the circuit meaning that the whole current flowing through the upper arm during the interval defined as $0 \leq t \leq T_\text{T}$ flows through its capacitor consequently changing its voltage. It is indicated by Fig. 12 that the area under the current curve represents the charge received by a firstly inserted capacitor during the observed process. Hence, all SMs' capacitors need to be sized according to this area since balancing algorithm selects one of the SMs to the beginning of the sequence depending upon voltage distribution over an arm. Furthermore, it would be highly beneficial if the upper arm current crossed zero within the observed interval considering that the charge acquired by the first SM being inserted into the circuit would be reduced compared to the case where no zero crossing occurs. However, if this comes out as unachievable, defining a certain band around zero described by $|i| \leq \varepsilon$ can be considered for the purpose of SM capacitance sizing. In other words, handling the transitions with no zero-crossings of the arm current is alleviated. It should be emphasized that determination of $\varepsilon$ depends upon the circuit designer. However, one has to keep in mind that the higher the tolerance represented by this coefficient, the higher the possible capacitance being the output of the presented algorithm (the area denoted by $Q^+$ increases). Moreover, the longer the transition the closer the converter approaches to the MMC (even though the distinct line between

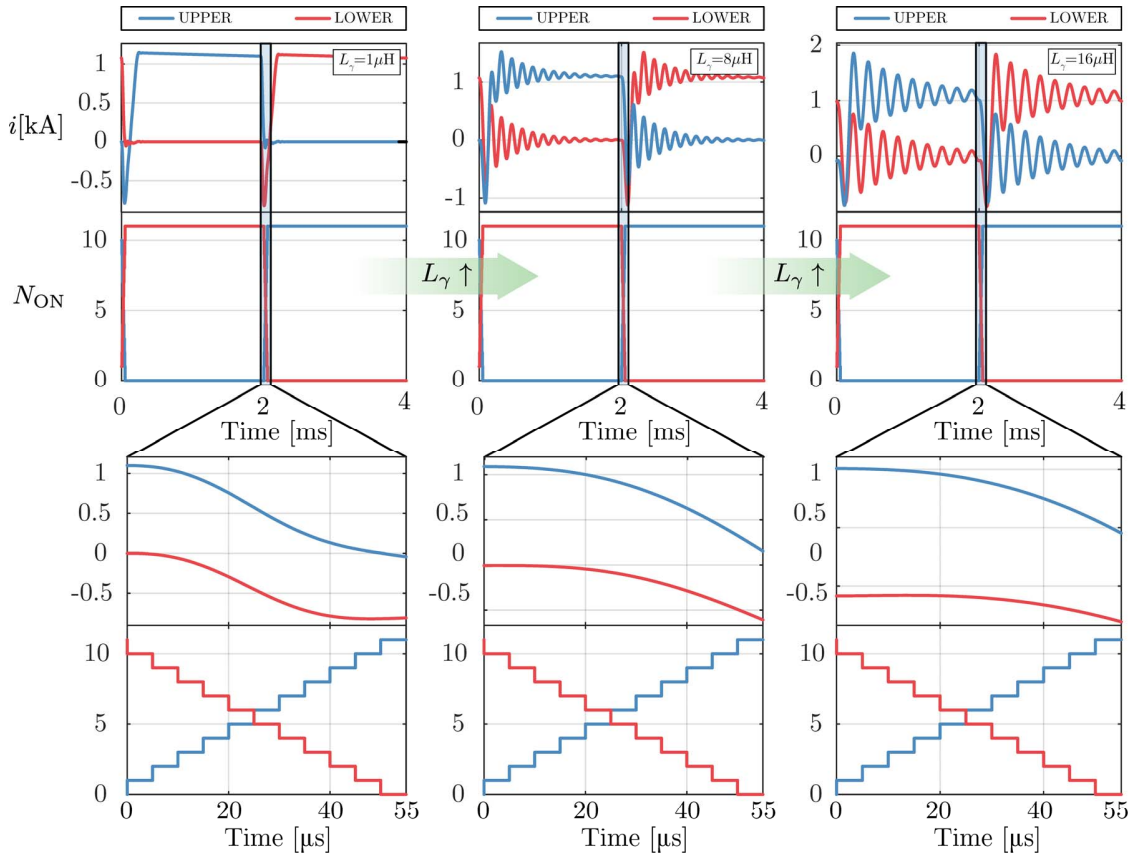



Fig. 11. Effect of the arm stray inductance on general converter behavior. Please notice that the higher the stray inductance, the higher the oscillations caused by the voltage transition period. Furthermore, current overshoot significantly increases with an increase in the stray inductance. Moreover, higher values of stray inductance prevent the arm current from quickly drifting from one arm to the other, therefore increasing the need for higher SM capacitance in order to keep its voltage between predefined limits.

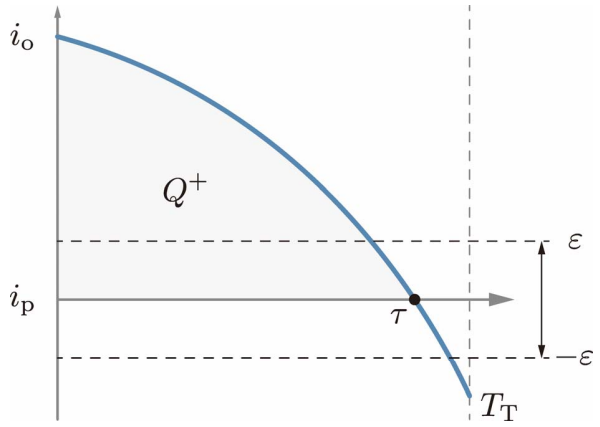



Fig. 12. Q2L converter upper arm current shape during the transition process (idealized). It is noteworthy that once the transition period commences, capacitor in an observed arm, being firstly inserted into the circuit, acquires all the charge denoted by $Q^+$. Therefore, capacitor sizing needs to be conducted according to this charge given that in the following transition interval some other cell will be assigned this gate signal depending upon the voltage distribution within an arm.

these two has never been drawn), therefore violating the basic Q2L principles.

Fig. 13 presents sizing algorithm flow chart. Firstly, all parameters related to the converter operation, such as input voltage, operating frequency, rated power, maximum arm current and passive components, apart from the SM capacitance, are defined. Additionally, certain range of possible SM capacitances, over which the algorithm is going to perform the search, needs to be defined. Maximum capacitance $C_{sm}^{max}$ to be taken into account by the algorithm can be estimated assuming the constant output current flows through the arm during the transition (45).

$$C_{sm}^{max} = \frac{\hat{i}_o T_T}{\Delta V_{sm}^*} \tag{45}$$

In (45), $\Delta V_{sm}^*$ refers to the desired SM voltage ripple under the nominal operating conditions, which implies rated current flowing to the upper arm prior to commencing the transition. With the aim of calculating this current, (37) can be used, where

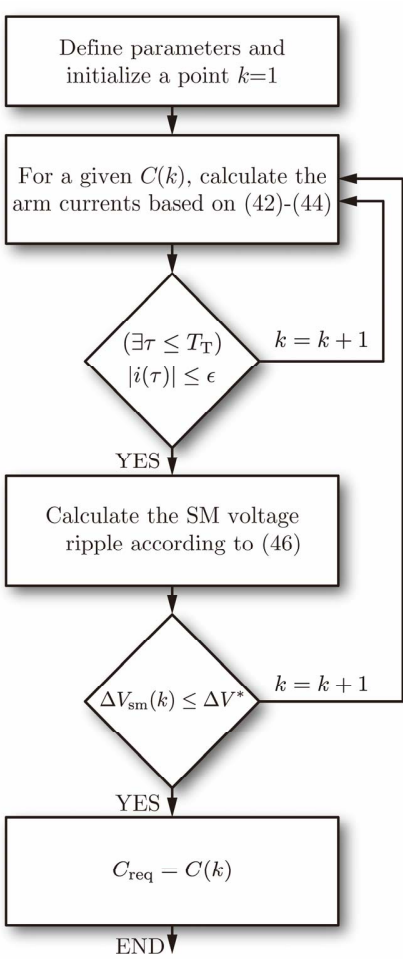



Fig. 13. Flowchart of the algorithm used to determine SM capacitance value.

the phase-angle resulting with rated power flowing through the converter $\varphi_{nom}$ should be used. Minimal capacitance $C_{min}$, to be used with the aim of starting the algorithm, can be a dopted as a fraction of the maximal one (for instance $C_{min} = C_{max}/4$). Thereafter, upper arm current can be calculated according to (42)–(44), whereas the algorithm checks if the calculated current falls within the band defined by $|i| \le \varepsilon$ for any time instant $\tau \le T_T$. If so, a SM voltage ripple $\Delta V_{sm}$ can be calculated according to (46), otherwise the algorithm runs into a new iteration.

$$\Delta V_{sm}(k) = \frac{1}{C(k)} \int_0^{\tau} i_p \, dt \tag{46}$$

If capacitance taken into account within the observed iteration fulfills the desired voltage ripple criterion ($\Delta V_{sm} < \Delta V^*$), the algorithm assigns its value to the SM required capacitance ($C_{req}$). Moreover, once the first capacitance fulfilling the above mentioned criteria is found, the algorithm terminates the search given that the subsequent iterations would provide higher SM capacitance. Of course, if needed, it is always possible to adopt a certain margin in the SM capacitance, as presented in the expression below.

$$C_{sm} = \gamma C_{req} \tag{47}$$

## IV. Simulation Results

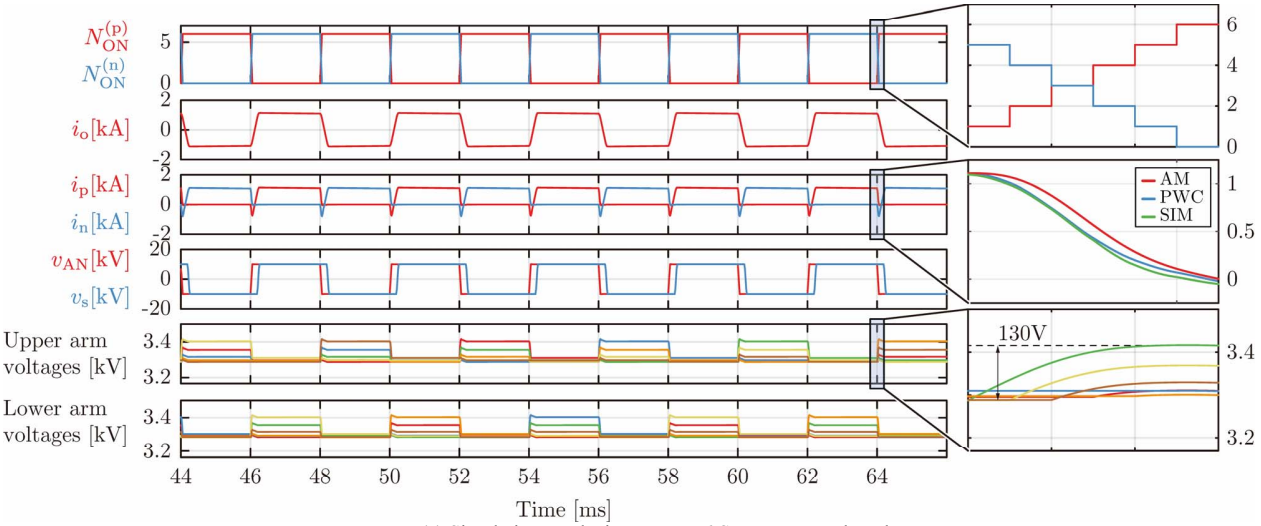
In order to validate the analysis conducted above, a set of simulations was performed using PLECS. Parameters of the simulated converter, which is presented in Fig. 4(a) can be found in Table I. Moreover, simulations were conducted utilizing various number of SMs depending upon semiconductor voltage class to be employed, as presented in Table II. Last but not least, simulation results during the transition are compared with both piece-wise calculations (9) and analytic (42)–(44). Fig. 14(a) presents converter operation over five fundamental cycles in case 6.5 kV IGBTs are employed within every SM. It can be seen that SMs voltages remain balanced during the observed interval. SM capacitance was determined such that its voltage change during the transition interval remains less than 5% of the nominal value ($V_{in}/N$).

On the right-hand side of Fig. 14(a), one can observe the waveform of the converter upper arm current along with the changes in SMs voltages. It can as well be seen that maximal voltage change of a SM equals $\Delta\widehat{V}_{SM}$ = 130 V which equals to around 4% of nominal SM voltage. Fig. 14(b) and (c) present converter operation in case 3.3 kV and 1.7 kV IGBT modules are used, respectively. Further, the plot presenting the upper arm current over all of the analyzed cases, contains its waveforms obtained by virtue of analytical model (red curve) and piece-wise calculations (blue curve). One can also notice from the Fig. 14 (a)–(c) that the lower the dwell time the higher the precision of the conducted calculation. One might find this logical given that sums within the piece-wise calculations were replaced by integrals under the assumption of infinitely small dwell time. However, for the sizing purposes a slight mismatch should not introduce significant errors which would threaten to impair converter performance.

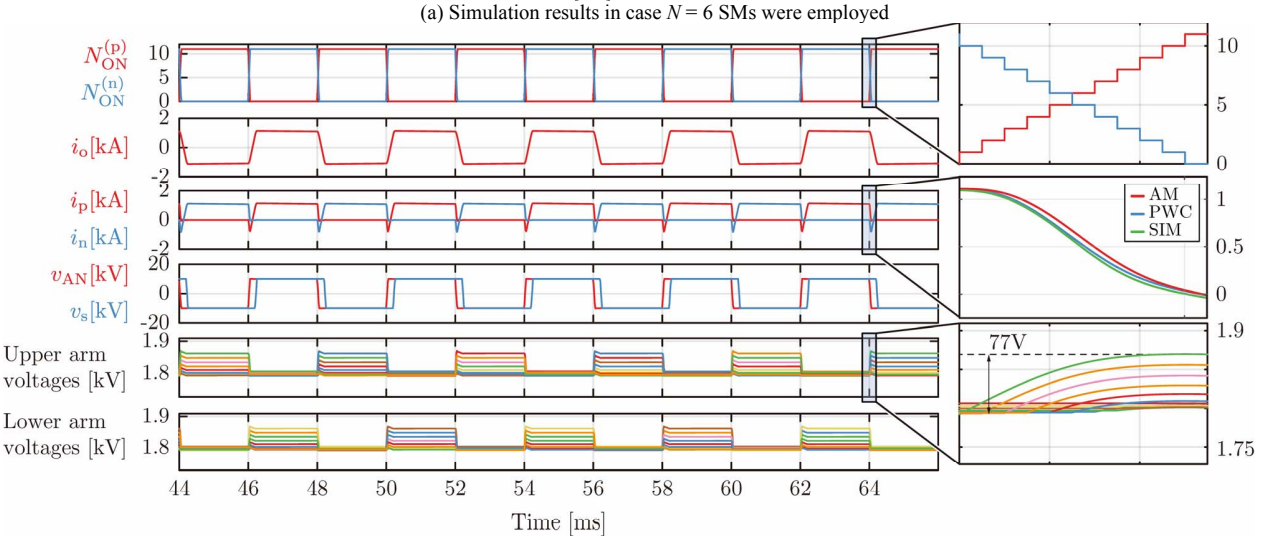
The algorithm presented above was also employed with the aim of sizing SMs capacitance for the 3PH DAB. Reference [20] provided SM capacitance sizing rule defined by

$$C_{sm} = \gamma \frac{NT_T}{3\omega L_o \Delta V_{sm}(\text{p.u.})} \left( \varphi_{nom} - \frac{\omega T_T}{3} \right) \tag{48}$$

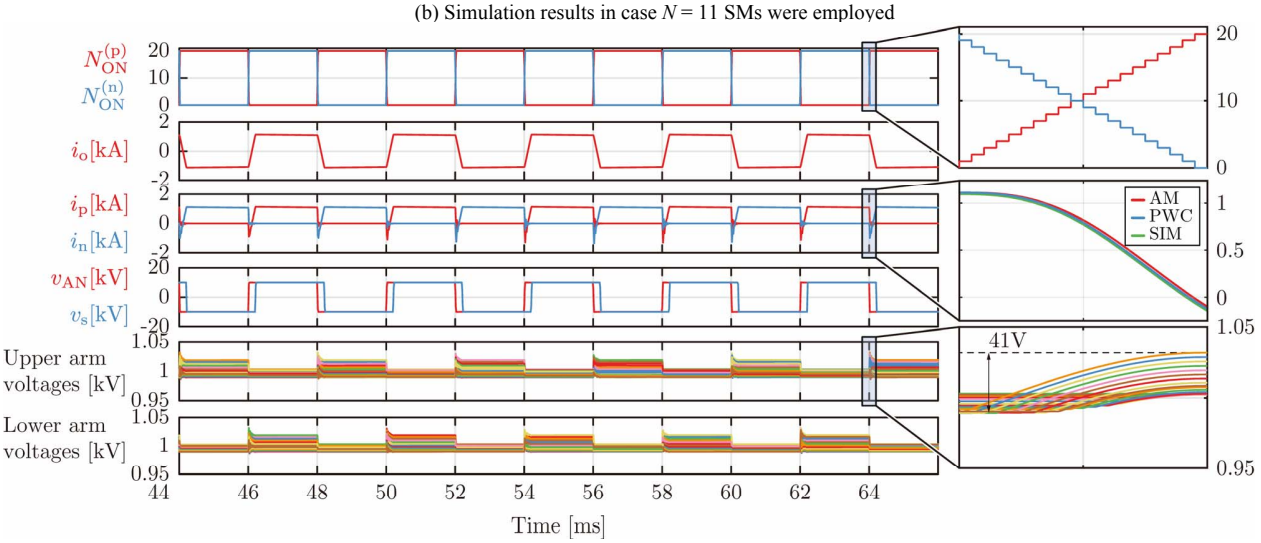
For the sake of comparison, 3PH DAB with parameters given in Table I was observed. Number of SMs was set as $N$ = 11. According to (48), SMs capacitance should be set as $C_{sm}$ = 257 $\mu$F with the aim of keeping a SM voltage ripple less than 5% of its nominal mean value [$\Delta V_{sm}$(p.u.) = 0.05]. Security factor $\gamma$ was set as unity. On the other hand, using the sizing algorithm presented in this paper, capacitance value of $C_{sm}$ = 160 $\mu$F was chosen. Fig. 15 presents voltages across Phase A upper arm converter within the 3PH DAB operating in the Q2L manner while using the capacitances determined above. It can be seen that the use of the proposed algorithm provides the possibility of reducing the SMs capacitance, while still fulfilling desired voltage ripple constraints.




(a) Simulation results in case $N = 6$ SMs were employed




(b) Simulation results in case $N = 11$ SMs were employed




(c) Simulation results in case $N = 20$ SMs were employed

Fig. 14. Simulation results in case different number of SMs was employed. On the right, one can notice the comparison among upper arm current waveforms obtained using the analytic model (AM), piece-wise calculations (PWC) and simulations (SIM).

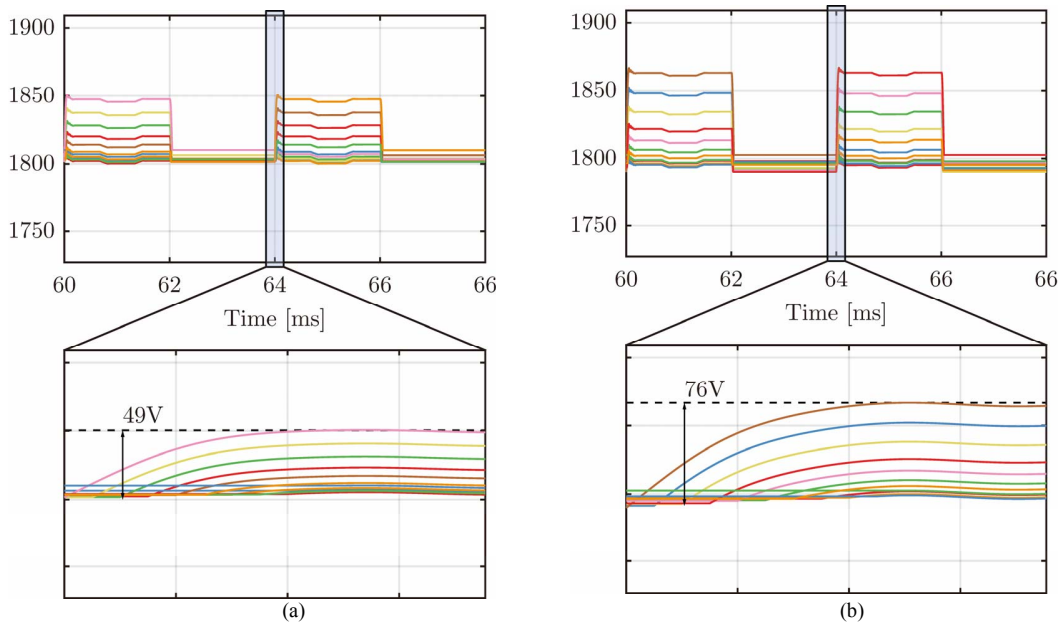



Fig. 15. Voltage across SMs capacitors in case $N = 11$ SMs are employed. On the left-hand side, one can see that peak-to-peak voltage ripple, in case (48) is used for the sizing purposes, equals approximately 2.53% of the SM rated mean voltage. SM capacitance determined in this fashion clearly satisfies voltage ripple criterion define above. However, on the right-hand side, one can notice that even with almost 40% reduction in the SM capacitance, which is the result obtained based on the employment of the presented algorithm, the same voltage ripple criterion can be fulfilled.

## V. Conclusion

This paper presented thorough mathematical analysis of the Q2L converter transition process. With the aim of alleviating mathematical determination of the SM capacitance, analytical formulas were derived. Instead of solving $N$ differential equations (piece-wise solution) with the aim of determining converter's current shape over the transition interval, the approximation comprising the combination of sinusoidal, qubic, square, linear and constant term was provided. Given that presented approximation represents the linearization of transient waveforms, the smaller the dwell intervals used to achieve desired transition the better the approximation results. By virtue of the proposed equations, capacitor sizing algorithm was designed with the aim of finding the capacitance to meet the requirements of SM voltage ripple and Q2L operation. Furthermore, on the example of the 3PH DAB, it was shown that the proposed sizing algorithm reduces the need for SM capacitance compared to the sizing method proposed in the literature. Simulation results obtained in PLECS were presented, from which it can be seen that converter manages to operate in the Q2L mode while keeping the voltage ripple across SMs within desired limits.

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