High-voltage Normally-off Recessed Tri-gate GaN Power MOSFETs with Low On-resistance

Minghua Zhu, Jun Ma, Luca Nela, Catherine Erine, and Elison Matioli, *Member, IEEE*

***Abstract*— In this letter, we present normally-off GaN-on-Si MOSFETs based on the combination of tri-gate with a short barrier recess to yield a large positive threshold voltage (V_{TH}), while maintaining a low specific on resistance ($R_{ON,SP}$) and high current density (I_D). The tri-gate structure offered excellent channel control, enhancing the V_{TH} from +0.3 V for the recessed to +1.4 V for the recessed tri-gate, along with a much reduced hysteresis in V_{TH}, and a significantly increased transconductance (g_m). Additional conduction channels at the sidewalls of the tri-gate trenches compensated the degradation in ON resistance (R_{ON}) from the gate recess, resulting in a small R_{ON} of 7.32 ± 0.26 Ω·mm for L_{GD} of 15 µm, and an increase in the maximum output current (I_D^{max}). In addition, the tri-gate inherently integrates a gate-connected field-plate (FP), which improved the breakdown voltage (V_{BR}) and reduced the degradation in dynamic R_{ON}. With proper passivation techniques, these devices could be very promising as high performance power switches for future power applications.**

***Index Terms*— E-mode, normally-off, GaN, MOS HEMT, tri-gate, high breakdown, low leakage, low on-resistance, gate recess.**

I. Introduction

GaN (MOS)HEMTs offer a huge potential for power applications thanks to their low losses and high blocking voltages [1]. Efficient power switches usually require a positive V_{TH} that is sufficiently large, along with low $R_{ON,SP}$ and high V_{BR} [2], which is however very challenging in GaN MOSHEMTs. Among several reported techniques, such as fluorine plasma treatment [3]–[5] and p-GaN gate [6]–[8], recessing the barrier under the gate region [9]–[12], either partially or fully, can lead to large V_{TH} [13], which however typically degrades R_{ON}. While reducing the gate recess length can improve R_{ON}, it also results in a negative shift of V_{TH} [14].

Recently tri-gate structures are attracting considerable attention due to their better gate control [15]–[17] and enhanced V_{BR} [18]–[20] compared to planar devices, without degrading the R_{ON} [17]. In addition, tri-gates allow a controllable positive shift of V_{TH} by changing the fin width, due to the partial relaxation of the AlGaN barrier and the enhanced electrostatic control from the tri-gate sidewalls [15]–[21].

However, reaching positive V_{TH} relying only on tri-gates, requires very small fin widths [21], [22], which demands high resolution lithography. This requirement can be significantly relieved by combining tri-gates with gate recess, as demonstrated in [19].

This work was supported in part by the Swiss National Science Foundation under Assistant Professor (AP) Energy Grant PYAPP2_166901 and in part by the European Research Council under the European Union's H2020 Program/ERC Grant Agreement 679425, and in part by the ECSEL Joint Undertaking (JU) under grant agreement No 826392.The JU receives support from the European Union's Horizon 2020 research and innovation programme and Austria, Belgium, Germany, Italy, Norway, Slovakia, Spain, Sweden, Switzerland.

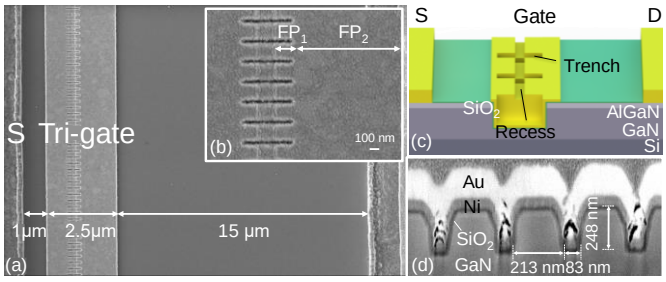

Fig. 1. (a) Top-view and (b) zoomed SEM images of the recessed tri-gate MOSFET. (c) 3D schematic of recessed tri-gate MOSFET. (d) Cross-sectional views of recessed tri-gate MOSFET.

In this letter, we demonstrate high-performance normally-off GaN-on-Si MOSFETs based on an optimized recessed tri-gate structure. This structure offered large V_{TH} and low R_{ON} concurrently, thanks to the additional conduction channels at the tri-gate sidewalls. In addition, the tri-gate inherently integrates a gate-connected FP, which improved the V_{BR} and reduced the degradation in dynamic R_{ON}, even without passivation. These results show the enormous potential of recessed tri-gate for high-voltage normally-off GaN transistors.

II. Device Design and Fabrication

The AlGaN/GaN epitaxial structure in this work consisted of 4.2 µm buffer, 420 nm un-doped GaN channel, 20 nm $Al_{0.25}Ga_{0.75}N$ barrier and 2.5 nm GaN Cap layers. The schematics and scanning electron microscopy (SEM) images of the device are shown in Fig.1 (a-d). The device fabrication started with the definition of the mesa and tri-gate regions by e-beam lithography, and followed by Cl_2-based ICP etch. The tri-gate width (w) was varied from 200 nm to 600 nm, and the spacing (s) was fixed at 100 nm. This corresponds to filling factors (FF = $w/(w+s)$) varying from 0.66 to 0.87. The tri-gate length (l) was fixed at 700 nm and the height of tri-gate trench (h) was ~250 nm. A 150 nm-long gate recess (l_r) was defined by e-beam lithography, followed by a 20 nm-deep slow-etch-rate Cl_2-based ICP etch. A metal stack composed of Ti/Al/Ti/Ni/Au was deposited in source and drain regions, followed by rapid thermal annealing. The gate dielectric was 25 nm-thick SiO_2, deposited by atomic layer deposition (ALD), without any further passivation layers. Finally, gate and contact pads were formed by Ni/Au. Devices with planar gates (planar) and recessed planar gates (recessed) were fabricated on the same

© 2019 IEEE. Personal use of this material is permitted. Permission from IEEE must be obtained for all other uses, in any current or future media, including reprinting/republishing this material for advertising or promotional purposes, creating new collective works, for resale or redistribution to servers or lists, orreuse of any copyrighted component of this work in other works."

batch with same process conditions for comparison. All current values were normalized by the device width of 80 µm, and the standard deviation was determined from about 8 separate devices of the same kind.

III. Results and Discussion

The transfer characteristics of the Planar, Recessed Planar and Recessed tri-gate devices are shown in Fig. 2(a). A significant positive shift of V_{TH} was observed from –3.6 V (at 1 µA/mm) for the planar, to +0.3 V for the recessed and +1.4 V for the recessed tri-gate (Fig. 2(a)). The large V_{TH} in the recessed tri-gate is mainly due to the strain relaxation of the AlGaN barrier and the sidewall gate modulation [16], [17], [23], [24]. The recessed tri-gate exhibited a larger g_m of 275 ± 12 mS/mm, with an ON/OFF ratio beyond 10^9, an improved *SS* of 95 ± 3 mV/dec and I_{OFF} at V_G = 0 V as small as 300 pA/mm, as compared with planar and recessed devices, revealing an improved tri-gate control over electrons in the channel. The small hysteresis below 0.5 V for all devices, under different V_G up to 8 V (Fig. 2(b)) indicates a good oxide quality. The recessed tri-gate devices showed the smallest hysteresis of 0.18 ± 0.05 V (at V_G^{max} of 8 V) compared to 0.47 ± 0.09 V of recessed planar and 0.53 ± 0.06 V. Moreover, the recessed tri-gate presented a much narrower V_{TH} distribution among all measured devices, with an average V_{TH} of +1.41 ± 0.12 V, confirming the excellent gate uniformity of our process.

The output characteristics of these devices are shown in Fig. 2 (c). The recessed tri-gate presented a larger I_D^{max} of 622 ± 16 mA/mm at V_G = 7 V compared to 581 ± 34 mA/mm for the recessed planar, which was only slightly smaller than that of the planar D-mode device (672 ± 19 mA/mm) (Fig. 2(c)). The degraded output characteristic of recessed planar devices shown in Fig. 2(c) is likely due to the short recess length of 150 nm, since the recessed planar with 500 nm-long recessed region presented good output characteristics. The recessed tri-gate presented much better performance with the same recess length of 150 nm, revealing a better channel control of the tri-gate combined with a narrow gate recess. The negative output resistance of these devices is mostly due to the self-heating. The R_{ON} of planar, recessed and recessed tri-gate, extracted from I_D - V_D sweeps in linear region, were 6.82 ± 0.29 Ω·mm, 7.37 ± 0.45 Ω·mm, and 7.32 ± 0.26 Ω·mm at V_G = 7 V, respectively (Fig. 2(d)). The recessed tri-gate required a much smaller gate driving voltage to reach low R_{ON} (Fig. 2(d)), as compared to the recessed planar devices, which is due to the superior control of the tri-gate recessed over electrons in the channel that results in a larger g_m compared to the planar recessed device.

The low R_{ON} and large I_D^{max} of the recessed tri-gate are a consequence of the trench conduction in the tri-gate geometry. To illustrate this, we fabricated recessed tri-gate devices with *w* of 200, 400, 500, and 600 nm and fixed *s* of 100 nm, corresponding to a number of tri-gate wires per mm (N_{NW}) of 3333, 2000, 1666, and 1333, respectively. The R_{ON} was extracted at V_G = 7 V for all recessed tri-gate device, since the small difference in V_{TH} is negligible compared to the driving voltage, and the R_{ON} is already saturated at this V_G.

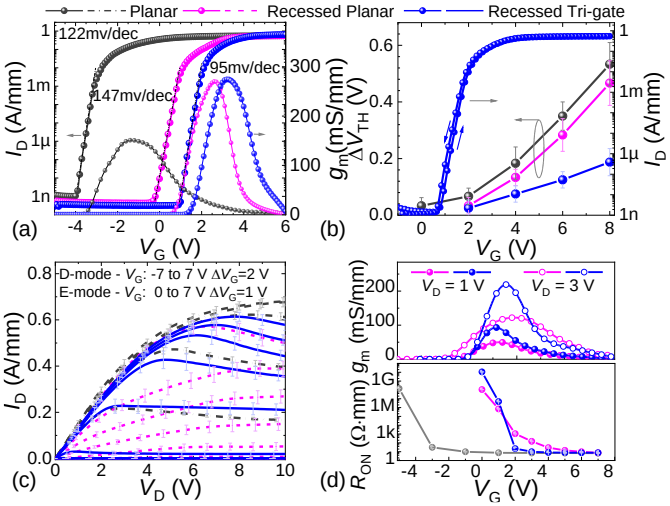

Fig. 2. Comparison of the normally-off recessed tri-gate with planar and recessed devices. (a) Transfer at V_{DS} = 5 V and (b) Measured V_G^{max} - ΔV_{TH} dependence of planar, recessed and recessed tri-gate devices and gate hysteresis up to 8 V of recessed tri-gate transistor. (c) Output characteristics of the three devices with V_G up to 7 V. (d) g_m of recessed planar and recessed tri-gate MOSFET under V_D of 1 V and 3 V and extracted V_G – R_{ON} dependence of planar, recessed and recessed tri-gate transistors. The L_{GS}, L_G and L_{GD} were 1, 2.5 and 15 µm, respectively, and *FF* was 0.66. Standard deviation bars were determined from the measurement of 8 devices of each type, revealing their consistent performance.

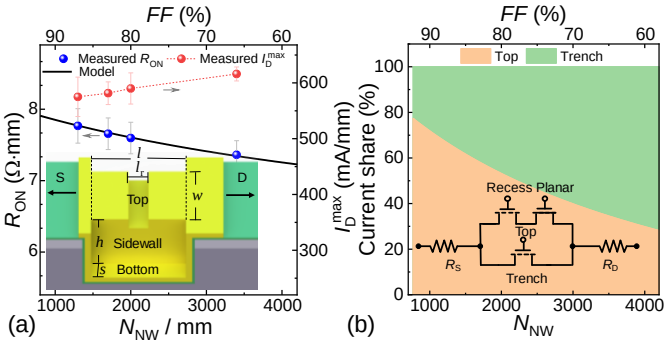

Fig. 3. (a) R_{ON} and I_D^{max} of the recessed tri-gate versus the number of nanowires (N_{NW}) and fill factor (*FF*) in the tri-gate region. (b) Current share in the recessed tri-gate region. Insets: Schematic and equivalent circuit of the recessed tri-gate.

An increase in I_D^{max} and a reduction of R_{ON} were observed when increasing N_{NW} (Fig. 3(a)). This can be understood with an equivalent model of the recessed tri-gate MOSFET (inset of Fig. 3(a)) consisting of 2 parallel parts of the top (recessed + planar) and trench portions of the tri-gate (sidewall and bottom portions), plus the source (R_S) and drain (R_D) contact and access resistances (inset of Fig. 3(b)). Thus the total R_{ON} can be written as:

$$R_{ON} = \left\{ \left[\left(\frac{R_{sh}^{r} \cdot l_r + R_{sh}^{p} \cdot (l - l_r)}{w} \right)^{-1} + \left(\frac{R_{sh}^{trench} \cdot l}{2h} \right)^{-1} \right] N_{NW} \right\}^{-1} + R_S + R_D$$

Where, R_{sh}^{r} and R_{sh}^{p} are the equivalent sheet resistances of the recessed and top planar regions, respectively. We assumed an equivalent sheet resistance for the sidewall and bottom parts (R_{sh}^{trench}) to simplify the model [25]–[27]. The R_{sh}^{r} and R_{sh}^{p} were obtained by averaging 7 separate planar and recessed gated halls, respectively, resulting in R_{sh}^{p} and R_{sh}^{r} of 269 ± 7 Ω/sq and 1713 ± 92 Ω/sq (at V_G = 7 V). The R_S and R_D were calculated

© 2019 IEEE. Personal use of this material is permitted. Permission from IEEE must be obtained for all other uses, in any current or future media, including reprinting/republishing this material for advertising or promotional purposes, creating new collective works, for resale or redistribution to servers or lists, orreuse of any copyrighted component of this work in other works."

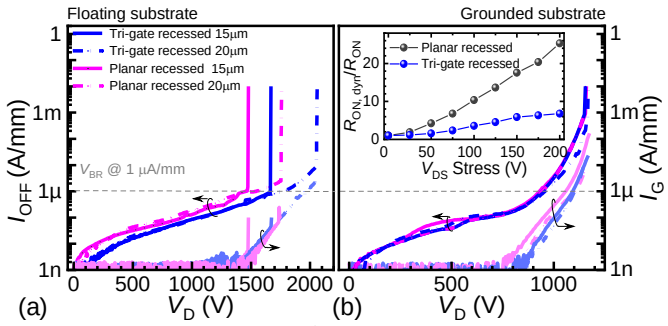

Fig. 4. Breakdown characteristics of the recessed (V_G = -1 V) and recessed tri-gate (V_G = 0 V) MOSFETs with L_{GD} = 15 μm and 20 μm, for (a) grounded and (b) floating substrate. Inset: Dynamic R_{ON} of unpassivated recessed planar and recessed tri-gate transistors measured up to a quiescent bias stress of 200V with a pulse width of 50 μs and a period of 5ms.

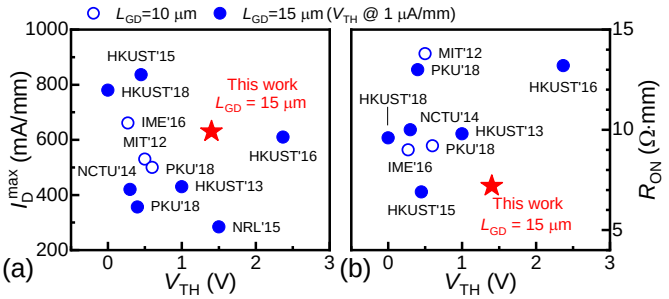

Fig. 5. Benchmarking of (a) I_D^{max} and (b) R_{ON} versus V_{TH} (defined at 1 μA/mm) of the recessed tri-gate against E-mode GaN-on-Si transistors. For fair comparison, L_{GD} smaller than 10 μm were not included.

based on the planar sheet resistance and contact resistance from separate TLM on the same wafer. To determine the missing variable R_{sh}^{trench}, the measured R_{ON} versus N_{NW} was fitted using this model (black curve in Fig. 3(a)), resulting in R_{sh}^{trench} of 3355 ± 138 Ω/sq. Based on these values, we calculated the share of current flowing at the top and sidewall regions (Fig. 3(b)). For large *FF*, the main contribution to conduction is from the top region, whereas by reducing *FF*, N_{NW} is increased and the contribution from the sidewalls becomes dominant.

The breakdown voltage of the devices was measured with floating (Fig. 4(a)) and grounded substrates (Fig. 4(b)), with V_G = 0 V. The observed breakdown mainly happened at the edge of gate. With floating substrate, the soft V_{BR} at I_{OFF} of 1 μA/mm of the recessed tri-gate with L_{GD} of 15 μm and 20 μm were 1650 V and 1800 V, respectively. A large hard V_{BR} of 2050 V was measured for the recessed tri-gate with L_{GD} of 20 μm (at I_{OFF} = 9 μA/mm). The gate leakage was ~1 nA/mm until 1400 V. A V_{BR} of 960 V at 1 μA/mm was observed with grounded substrate, for both recessed and recessed tri-gate, with a high hard breakdown of 1100 V, which was mainly limited by the buffer thickness and quality. The observed improvement in V_{BR} compared with the recessed devices is mainly due to the integrated field plates (FP) in the recessed tri-gate. The gate region in the recessed tri-gate device contains two FPs: tri-gate FP (FP_1) from the recess edge to tri-gate drain-side edge, and planar FP (FP_2) from the tri-gate drain-side edge to gate drain-side edge (Fig.1(b)). These regions function as two gate-connected FPs, due to their more negative pinch-off voltages compared to the recessed region, of -2 V in the tri-gate FP and -4 V in the planar FP [17]–[20]. With increasing V_D, the 2DEG under FP_1 and FP_2 are sequentially depleted, reducing the electric field in the recessed gate region and leading to a much enhanced V_{BR} [28], [29]. In addition, despite the lack of passivation in both devices, this additional FP also improved the dynamic R_{ON} of the recessed tri-gate devices by better distributing the electric field under the gate, as supported by [30], [31] (inset of Fig.4 (b)). The measured floating breakdown voltage could be affected by virtual gating, which can be resolved by a proper passivation process without sacrificing the breakdown voltage [32]–[34].

The I_D^{max} and R_{ON} versus V_{TH} of the recessed tri-gate devices in this work were benchmarked against E-mode GaN transistors in the literature, demonstrating concurrently high I_D^{max}, low R_{ON} and large V_{TH} of 1.4 V (Fig. 5(a,b)), with $R_{ON,SP}$ of 1.76 and 2.42 mΩ·cm^2 for L_{GD} of 15 μm and 20 μm, respectively. These results highlight the benefits of combining tri-gate structures and narrow gate recess for high-performance normally-off devices.

IV. Conclusions

In this work we have demonstrated state-of-the-art normally-off recessed tri-gate GaN-on-Si MOSFETs by combining tri-gates with a short barrier recess. Due to trench conduction in the tri-gate region, the devices presented concurrently large positive V_{TH} of 1.4 V at 1 μA/mm, along with high I_D^{max} of 622 ± 16 mA/mm at V_G = 7 V and low R_{ON} of 7.32 ± 0.26 Ω· mm. The excellent channel control from the tri-gate structure enhanced the V_{TH} stability, reduced gate driving voltage and increased the transconductance. These results unveil the excellent prospect of recessed tri-gate for power applications.

Acknowledgement

The authors would like to acknowledge the staff of CMI and ICMP cleanrooms at EPFL for their technical support.

References

[1] C. Lee, W. Lin, Y. Lee, and J. Huang, "Characterizations of Enhancement-Mode Double Heterostructure GaN HEMTs With Gate Field Plates," *IEEE Trans. Electron Devices*, vol. 65, no. 2, pp. 488–492, Feb. 2018, doi: 10.1109/TED.2017.2786479.

[2] M. Ishida, T. Ueda, T. Tanaka, and D. Ueda, "GaN on Si Technologies for Power Switching Devices," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3053–3059, Oct. 2013, doi: 10.1109/TED.2013.2268577.

[3] Y. Zhang, M. Sun, S. J. Joglekar, and T. Palacios, "High threshold voltage in GaN MOS-HEMTs modulated by fluorine plasma and gate oxide," in *71st Device Res. Conf.*, Jun. 2013, pp. 141–142, doi: 10.1109/DRC.2013.6633833.

[4] Y. He, M. Mi, C. Wang, X. Zheng, M. Zhang, H. Zhang, J. Wu, L. Yang, P. Zhang, X. Ma, and Y. Hao, "Enhancement-mode AlGaN/GaN nanowire channel high electron mobility transistor with fluorine plasma treatment by ICP," *IEEE Electron Device Lett.*, vol. PP, no. 99, pp. 1–1, 2017, doi: 10.1109/LED.2017.2736780.

[5] L. Yang, B. Hou, M. Mi, Q. Zhu, M. Wu, J. Zhu, Y. Lu, M. Zhang, L. Chen, X. Zhou, L. Lv, X. Ma, and Y. Hao, "High-Performance Enhancement-mode AlGaN/GaN high electron mobility transistors combined with TiN-based Source Contact Ledge and Two-Step Fluorine Treatment," *IEEE Electron Device Lett.*, pp. 1–1, 2018, doi: 10.1109/LED.2018.2864135.

[6] Y. Zhou, Y. Zhong, H. Gao, S. Dai, J. He, M. Feng, Y. Zhao, Q. Sun, A. Dingsun, and H. Yang, "p-GaN Gate Enhancement-Mode HEMT Through a High Tolerance Self-Terminated Etching Process," *IEEE J. Electron Devices Soc.*, vol. 5, no. 5, pp. 340–346, Sep. 2017, doi: 10.1109/JEDS.2017.2725320.

© 2019 IEEE. Personal use of this material is permitted. Permission from IEEE must be obtained for all other uses, in any current or future media, including reprinting/republishing this material for advertising or promotional purposes, creating new collective works, for resale or redistribution to servers or lists, orreuse of any copyrighted component of this work in other works."

[7] X. Tang, B. Li, H. A. Moghadam, P. Tanner, J. Han, and S. Dimitrijev, "Effect of hole-injection on leakage degradation in a p-GaN gate AlGaN/GaN power transistor," *IEEE Electron Device Lett.*, pp. 1–1, 2018, doi: 10.1109/LED.2018.2849398.

[8] G. Tang, M. H. Kwan, R. Y. Su, F. W. Yao, Y. M. Lin, J. L. Yu, T. Yang, C. H. Chern, T. Tsai, H. C. Tuan, A. Kalnitsky, and K. J. Chen, "High-Capacitance-Density p-GaN Gate Capacitors for High-Frequency Power Integration," *IEEE Electron Device Lett.*, pp. 1–1, 2018, doi: 10.1109/LED.2018.2854407.

[9] Z. Xu, J. Wang, Y. Liu, J. Cai, J. Liu, M. Wang, M. Yu, B. Xie, W. Wu, X. Ma, and J. Zhang, "Fabrication of Normally Off AlGaN/GaN MOSFET Using a Self-Terminating Gate Recess Etching Technique," *IEEE Electron Device Lett.*, vol. 34, no. 7, pp. 855–857, Jul. 2013, doi: 10.1109/LED.2013.2264494.

[10] M. Hua, Z. Zhang, J. Wei, J. Lei, G. Tang, K. Fu, Y. Cai, B. Zhang, and K. J. Chen, "Integration of LPCVD-SiNx gate dielectric with recessed-gate E-mode GaN MIS-FETs: Toward high performance, high stability and long TDDB lifetime," in *2016 IEEE Int. Electron Devices Meet. IEDM*, Dec. 2016, pp. 10.4.1-10.4.4, doi: 10.1109/IEDM.2016.7838388.

[11] W. B. Lanford, T. Tanaka, Y. Otoki, and I. Adesida, "Recessed-gate enhancement-mode GaN HEMT with high threshold voltage," *Electron. Lett.*, vol. 41, no. 7, pp. 449–450, Mar. 2005, doi: 10.1049/el:20050161.

[12] J. He, M. Hua, Z. Zhang, and K. J. Chen, "Performance andVTHStability in E-Mode GaN Fully Recessed MIS-FETs and Partially Recessed MIS-HEMTs With LPCVD-SiNx/PECVD-SiNxGate Dielectric Stack," *IEEE Trans. Electron Devices*, vol. 65, no. 8, pp. 3185–3191, Aug. 2018, doi: 10.1109/TED.2018.2850042.

[13] Q. Zhou, L. Liu, A. Zhang, B. Chen, Y. Jin, Y. Shi, Z. Wang, W. Chen, and B. Zhang, "7.6 V Threshold Voltage High-Performance Normally-Off Al2O3/GaN MOSFET Achieved by Interface Charge Engineering," *IEEE Electron Device Lett.*, vol. 37, no. 2, pp. 165–168, Feb. 2016, doi: 10.1109/LED.2015.2511026.

[14] B. Lu, O. I. Saadat, and T. Palacios, "High-Performance Integrated Dual-Gate AlGaN/GaN Enhancement-Mode Transistor," *IEEE Electron Device Lett.*, vol. 31, no. 9, pp. 990–992, Sep. 2010, doi: 10.1109/LED.2010.2055825.

[15] B. Lu, E. Matioli, and T. Palacios, "Tri-Gate Normally-Off GaN Power MISFET," *IEEE Electron Device Lett.*, vol. 33, no. 3, pp. 360–362, Mar. 2012, doi: 10.1109/LED.2011.2179971.

[16] S. Liu, Y. Cai, G. Gu, J. Wang, C. Zeng, W. Shi, Z. Feng, H. Qin, Z. Cheng, K. J. Chen, and B. Zhang, "Enhancement-Mode Operation of Nanochannel Array (NCA) AlGaN/GaN HEMTs," *IEEE Electron Device Lett.*, vol. 33, no. 3, pp. 354–356, Mar. 2012, doi: 10.1109/LED.2011.2179003.

[17] J. Ma and E. Matioli, "High Performance Tri-Gate GaN Power MOSHEMTs on Silicon Substrate," *IEEE Electron Device Lett.*, vol. 38, no. 3, pp. 367–370, Mar. 2017, doi: 10.1109/LED.2017.2661755.

[18] J. Ma and E. Matioli, "Slanted Tri-Gates for High-Voltage GaN Power Devices," *IEEE Electron Device Lett.*, vol. 38, no. 9, pp. 1305–1308, Sep. 2017, doi: 10.1109/LED.2017.2731799.

[19] J. Ma, M. Zhu, and E. Matioli, "900 V Reverse-Blocking GaN-on-Si MOSHEMTs With a Hybrid Tri-Anode Schottky Drain," *IEEE Electron Device Lett.*, vol. 38, no. 12, pp. 1704–1707, Dec. 2017, doi: 10.1109/LED.2017.2761911.

[20] J. Ma and E. Matioli, "2 kV slanted tri-gate GaN-on-Si Schottky barrier diodes with ultra-low leakage current," *Appl. Phys. Lett.*, vol. 112, no. 5, p. 052101, Jan. 2018, doi: 10.1063/1.5012866.

[21] L. Nela, M. Zhu, J. Ma, and E. Matioli, "High-Performance Nanowire-Based E-Mode Power GaN MOSHEMTs With Large Work-Function Gate Metal," *IEEE Electron Device Lett.*, vol. 40, no. 3, pp. 439–442, Mar. 2019, doi: 10.1109/LED.2019.2896359.

[22] J. Ma, C. Erine, P. Xiang, K. Cheng, and E. Matioli, "Multi-channel tri-gate normally-on/off AlGaN/GaN MOSHEMTs on Si substrate with high breakdown voltage and low ON-resistance," *Appl. Phys. Lett.*, vol. 113, no. 24, p. 242102, Dec. 2018, doi: 10.1063/1.5064407.

[23] M. Azize and T. Palacios, "Top-down fabrication of AlGaN/GaN nanoribbons," *Appl. Phys. Lett.*, vol. 98, no. 4, p. 042103, Jan. 2011, doi: 10.1063/1.3544048.

[24] O. Landré, D. Camacho, C. Bougerol, Y. M. Niquet, V. Favre-Nicolin, G. Renaud, H. Renevier, and B. Daudin, "Elastic strain relaxation in GaN/AlN nanowire superlattice," *Phys. Rev. B*, vol. 81, no. 15, p. 153306, Apr. 2010, doi: 10.1103/PhysRevB.81.153306.

[25] K. Im, C. Won, Y. Jo, J. Lee, M. Bawedin, S. Cristoloveanu, and J. Lee, "High-Performance GaN-Based Nanochannel FinFETs With/Without AlGaN/GaN Heterostructure," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3012–3018, Oct. 2013, doi: 10.1109/TED.2013.2274660.

[26] S. Takashima, Z. Li, and T. P. Chow, "Sidewall Dominated Characteristics on Fin-Gate AlGaN/GaN MOS-Channel-HEMTs," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3025–3031, Oct. 2013, doi: 10.1109/TED.2013.2278185.

[27] C. Yadav, P. Kushwaha, S. Khandelwal, J. P. Duarte, Y. S. Chauhan, and C. Hu, "Modeling of GaN-Based Normally-Off FinFET," *IEEE Electron Device Lett.*, vol. 35, no. 6, pp. 612–614, Jun. 2014, doi: 10.1109/LED.2014.2314700.

[28] Y. Dora, A. Chakraborty, L. Mccarthy, S. Keller, S. P. Denbaars, and U. K. Mishra, "High Breakdown Voltage Achieved on AlGaN/GaN HEMTs With Integrated Slant Field Plates," *IEEE Electron Device Lett.*, vol. 27, no. 9, pp. 713–715, Sep. 2006, doi: 10.1109/LED.2006.881020.

[29] R. Coffie, "Slant Field Plate Model for Field-Effect Transistors," *IEEE Trans. Electron Devices*, vol. 61, no. 8, pp. 2867–2872, Aug. 2014, doi: 10.1109/TED.2014.2329475.

[30] W. Saito, T. Nitta, Y. Kakiuchi, Y. Saito, K. Tsuda, I. Omura, and M. Yamaguchi, "Suppression of Dynamic On-Resistance Increase and Gate Charge Measurements in High-Voltage GaN-HEMTs With Optimized Field-Plate Structure," *IEEE Trans. Electron Devices*, vol. 54, no. 8, pp. 1825–1830, Aug. 2007, doi: 10.1109/TED.2007.901150.

[31] M. T. Hasan, T. Asano, H. Tokuda, and M. Kuzuhara, "Current Collapse Suppression by Gate Field-Plate in AlGaN/GaN HEMTs," *IEEE Electron Device Lett.*, vol. 34, no. 11, pp. 1379–1381, Nov. 2013, doi: 10.1109/LED.2013.2280712.

[32] C. Tang and J. Shi, "Effects of passivation on breakdown voltage and leakage current of normally-off InAlN/GaN MISHFETs—a simulation study," *Semicond. Sci. Technol.*, vol. 29, no. 12, p. 125004, Oct. 2014, doi: 10.1088/0268-1242/29/12/125004.

[33] H. Hanawa, H. Onodera, A. Nakajima, and K. Horio, "Numerical Analysis of Breakdown Voltage Enhancement in AlGaN/GaN HEMTs With a High-k Passivation Layer," *IEEE Trans. Electron Devices*, vol. 61, no. 3, pp. 769–775, Mar. 2014, doi: 10.1109/TED.2014.2298194.

[34] T. Kabemura, S. Ueda, Y. Kawada, and K. Horio, "Enhancement of Breakdown Voltage in AlGaN/GaN HEMTs: Field Plate Plus High-k Passivation Layer and High Acceptor Density in Buffer Layer," *IEEE Trans. Electron Devices*, vol. 65, no. 9, pp. 3848–3854, Sep. 2018, doi: 10.1109/TED.2018.2857774.

© 2019 IEEE. Personal use of this material is permitted. Permission from IEEE must be obtained for all other uses, in any current or future media, including reprinting/republishing this material for advertising or promotional purposes, creating new collective works, for resale or redistribution to servers or lists, orreuse of any copyrighted component of this work in other works."