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Near-junction heat spreaders for hot spot thermal management of high power density electronic devices

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Abstract

Many high power (opto-) electronic devices such as transistors, diodes and lasers suffer from significant hot spot temperature rises due to the high heat fluxes generated in their active area, which limits their performance, reliability and lifetime. Employing high thermal conductivity materials near the heat source, known as near-junction heat spreaders, offers a low-cost and effective thermal management approach. Here, we present an analytical model of heat spreaders and a methodology to evaluate their performance. Experimental demonstration of near-junction diamond heat spreaders on vertical GaN PiN diodes revealed significantly reduced spreading resistances, along with very low temperature gradients across the device. The findings in this work provide design guidelines and demonstrate excellent prospects, especially for the devices on low thermal conductivity substrates. The theoretical analysis of optimized diamond heat spreaders shows 86% reduction of spreading resistance for GaN devices, and 98% for Ga_2O_3 devices. In addition, our results show that a 3 μm-thick layer of high-quality CVD-deposited diamond heat spreaders on GaN-on-Si devices can provide better heat spreading than GaN-on-SiC devices and perform similarly to GaN-on-diamond devices, highlighting the significant potential of heat spreaders as an effective and low-cost thermal management approach.

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Introduction

The increasing power density of high power electronic and optoelectronic devices, radio frequency (RF) devices and power ICs leads to large heat fluxes in the active region of the devices. The hot spot heat flux has to be conducted through several thermal resistances such as the bulk substrate material, thermal boundary resistances (TBRs), packaging and thermal interfacial materials (TIMs), before being extracted from the chip.[1] High power devices can reach power densities, as high as 50 W/mm in GaN devices,[2,3] that can result in extremely large heat fluxes, as high as 300 kW/cm^2.[4] The generated heat can be very confined in some cases (e.g. at drain side of the gate in GaN HEMTs),[5] thus the heat flux faces thermal spreading resistances before being extracted from the chip, which limits the cooling of the device.[6] In the case of GaN, as the device power density increases, its thermal conductivity[7] is becoming insufficient to handle the hot spots and provide enough heat spreading, leading to large peak temperature rises. This problem is more troublesome for emerging oxide electronic devices. Ga_2O_3 has a large Baliga's Figure of Merit (almost four-times that of GaN), therefore being very promising for future high power density devices.[8] However, its extremely poor thermal conductivity (ten-times lower than GaN) results in a limited thermal conduction and heat spreading.[9] As a result, the large thermal resistances of Ga_2O_3 devices[10,11] impose a severe limit on the device power density, and without a proper thermal management, would strongly affect their performance, reliability and lifetime.

To address the localized heat fluxes and limited heat spreading, it is common to use high thermal conductivity substrates, such as SiC and diamond, which results in enhanced thermal and electrical performances.[12–14] Nonetheless, the potential advantages of such technologies should be considered together with the issues of the limited available size of these substrate, CTE mismatch for heteroepitaxy and high system-level cost.[15,16]

In addition, a larger impact on heat spreading requires the use of high thermal conductivity materials as close as possible to the hot spots to spread the heat away from the heat source to larger areas on the chip,[17] which is the basis for the concept of near-junction heat spreaders.

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Heteroepitaxial chemical vapor-phase deposited (CVD) diamond layers are very promising for thermal management applications. The effective lateral thermal conductivity of polycrystalline diamond is strongly affected by the grain size,[18] which is determined by the thickness of the layer, as well as the quality of the deposited layer.[19] In addition, the interface between the diamond layers and the substrate plays an important role on its adhesion and TBRs.[20] Therefore, to enhance the effect of diamond heat spreaders, the lateral thermal conductivity and thickness of the diamond, as well as its interface with the substrate has to be optimized.[21]

Finding a method to assess the effect of near junction heat spreaders is of a great importance for comparing their performance and providing design guidelines for device engineers. However, this is not a simple task, since different heat spreaders cannot be compared by reporting the device temperature as a function of dissipated power normalized by the device size, because the thermal resistance does not scale linearly with the device size. This is in contrast to electrical characteristics, where such normalizations can provide useful and comparable information. Moreover, the total thermal resistance of a device is not a general characteristic to be solely used to compare the effectiveness of different heat spreaders, because it depends on many parameters such as the size and the thermal conductivity of the heat spreader and substrate, cooling of the chip, and the shape and size of the heat source.

In this paper, we present an analytical model to evaluate and compare the thermal performance of heat spreaders, which reveals the theoretical limits of the reduction of thermal spreading resistances, and provides general guidelines for the design of effective heat spreaders. We experimentally evaluated the performance of two sets of near junction heat spreaders, based on diamond and Cu, on GaN-on-Si vertical PiN diodes. The diamond near junction heat spreaders were deposited on the GaN devices with optimized interlayers, which resulted in high-quality micro-crystalline diamond layers with high lateral thermal conductivities. The heat spreader geometry was evaluated for different devices and their heat spreading performance was compared to that of high thermal conductivity substrates, demonstrating an excellent heat spreading especially on low thermal conductivity substrates.

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Theoretical analysis

To evaluate the effect of the near junction heat spreaders, we have developed an analytical model using the thermal spreading resistances in a cylindrical geometry as shown see Fig. 1(a). In this model, the device structure consisted of a heat spreader with a thickness t_{HS} and thermal conductivity k_{HS} on top of a substrate with a thickness t_{Sub}, and thermal conductivity k_{Sub}. The heat source (q_{in}) was considered as an iso-flux boundary condition at the interface with a radius of a, and the structure is cooled with a heat transfer coefficient of h_{Sub} to a reference temperature T_{Ref} at the backside of the substrate. All of the thermal resistances are determined based on the hotspot temperature, which is located at the center of the heat source and marked as T_J in Fig. 1(b). This model could be expanded to represent the case of the scaled up devices with multiple unit cells in parallel and each cell having a thermal circuit shown in Fig. 1(b). Although we have studied the unit cells with a cylindrical geometry, the results can be used for unit cells with some other configurations and geometries without introducing a large discrepancy.[22]

Interfacial thermal resistances can degrade the heat transport at the interfaces and can have a negative effect on the heat spreaders.[23] However, since the analytical model presented here has the purpose to give a general view of heat spreaders and to show its theoretical limits, it was simplified by assuming no TBRs, to obtain a closed-form expression. Therefore, the analytical model provides a big picture on the other aspects of the heat spreaders that have very significant effect such as the relative size and relative thermal conductivity. In addition, recent studies demonstrated significant reductions of the TBRs using SiN interlayers between GaN and diamond, reaching to TBRs below 10 m^2.K/GW [21,24], in which case, the TBRs would have a minor effect on the performance of heat spreaders and could be ignored without introducing major errors in the analytical model.

The total thermal transport in a device is represented by a network of thermal resistances considering 3D and 1D thermal conductions, as well as the thermal resistance due to the cooling. The conductive thermal resistance can be separated into two thermal resistances: the spreading thermal resistance, which considers the 3D thermal transport from the heat source to the chip edge and the 1D thermal resistance, which considers the 1D conduction of heat through the thickness of the chip to the cooling side.[22]

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Therefore, the total thermal resistance (R_θ) consists of three thermal resistances in series

$$R_\Theta = R_{\mathrm{Sp}} + R_{\mathrm{1D}} + R_{\mathrm{Conv}}, \quad (1)$$

where R_{Sp} is the spreading resistance, R_{1D} is the 1D thermal resistance and R_{Conv} is the convective thermal resistance at the backside of the chip. The 1D thermal resistance of the device can be calculated as

$$R_{\mathrm{1D}} = \frac{t_{\mathrm{Sub}}}{k_{\mathrm{Sub}}\pi b^2}, \quad (2)$$

where b is the radius of the substrate, resulting in the following convective thermal resistance

$$R_{\mathrm{Conv}} = \frac{1}{h_{\mathrm{Sub}}\pi b^2}. \quad (3)$$

The spreading resistance of the device according to the model shown in Fig. 1(b) is calculated as

$$R_{\mathrm{Sp}} = \frac{R_{\mathrm{HS}}\, R_{\mathrm{Sp,sub}}}{R_{\mathrm{HS}} + R_{\mathrm{Sp,sub}}}, \quad (4)$$

where R_{HS} is the spreading resistance of the heat spreader and $R_{\mathrm{Sp,sub}}$ is the spreading resistance of the substrate, which was calculated using analytical solutions to Laplace's equation provided in [25–27] and adapted to our boundary conditions:

$$R_{\mathrm{Sp,sub}} = \sum_n \frac{2a\, J_1(\lambda_n a)}{\phi_n k_{\mathrm{Sub}} \delta_n^2 J_0^2(\lambda_n b)} - (R_{\mathrm{1D}} + R_{\mathrm{Conv}}), \quad (5)$$

where J_ν are Bessel functions of the first kind and ν^{th} order, δ_n the eigenvalues of J_1. ϕ_n and λ_n are

$$\phi_n = \frac{Bi_{\mathrm{Sub}} + \delta_n\, tanh(\delta_n \tau_{\mathrm{Sub}})}{\delta_n + Bi_{\mathrm{Sub}}\, tanh(\delta_n \tau_{\mathrm{Sub}})}, \quad (6)$$

$$\lambda_n = \frac{\delta_n}{b}, \quad (7)$$

where the Biot number of the substrate (Bi_{Sub}) and the relative substrate thickness (τ_{Sub}) are

$$Bi_{\mathrm{Sub}} = \frac{h_{\mathrm{Sub}} b}{k_{\mathrm{Sub}}}, \quad (8)$$

$$\tau_{\mathrm{Sub}} = \frac{t_{\mathrm{Sub}}}{b}. \quad (9)$$

The heat spreader's boundary conditions can be approximated as shown in Fig. 1(c), where the h_{HS} is

$$h_{\mathrm{HS}} = \frac{1}{(R_{\mathrm{1D}} + R_{\mathrm{Conv}})\pi b^2} = \frac{h_{\mathrm{Sub}} k_{\mathrm{Sub}}}{k_{\mathrm{Sub}} + h_{\mathrm{Sub}} t_{\mathrm{Sub}}}. \quad (10)$$

The Biot number for the heat spreader (Bi_{HS}) is defined as

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$$Bi_{\mathrm{HS}} = \frac{h_{\mathrm{HS}} b}{k_{\mathrm{HS}}}. \tag{11}$$

Assuming that the thermal conductivity of the heat spreader is higher than the substrate and h_{HS} is generally smaller than h_{Sub}, thus the Biot number of the heat spreader would be small, in which case, all of the heat spreader volume contributes to the heat spreading. Therefore, the spreading term of the heat spreader thermal resistance can be determined using an alternative boundary condition shown in Fig. 1(d). This enables the use of a similar formulation as for the spreading resistance of the substrate. By doing so and adapting it for the heat spreader, R_{HS} can be obtained:

$$R_{\mathrm{HS}} = \sum_n \frac{2a\, J_1(\lambda_n a)}{\phi_{\mathrm{n,HS}} k_{\mathrm{HS}} \delta_n^2 J_0^2(\lambda_n b)} - \left(R_{\mathrm{1D,HS}} + R_{\mathrm{Conv,HS}}\right), \tag{12}$$

where $\phi_{\mathrm{n,HS}}$ and the relative thickness of the heat spreader (τ_{HS}) are

$$\phi_{\mathrm{n,HS}} = \frac{Bi_{\mathrm{HS}} + \delta_n \tanh(\delta_n \tau_{\mathrm{HS}})}{\delta_n + Bi_{\mathrm{HS}} \tanh(\delta_n \tau_{\mathrm{HS}})}, \tag{13}$$

$$\tau_{\mathrm{HS}} = \frac{t_{\mathrm{HS}}}{b}. \tag{14}$$

The one-dimensional heat spreader thermal resistance ($R_{\mathrm{1D,HS}}$) and its convective thermal resistance ($R_{\mathrm{Conv,HS}}$) are

$$R_{\mathrm{1D,HS}} = \frac{t_{\mathrm{HS}}}{k_{\mathrm{HS}} \pi b^2}, \tag{15}$$

$$R_{\mathrm{Conv,HS}} = \frac{1}{h_{\mathrm{HS}} \pi b^2}. \tag{16}$$

The other parameters used in this study are the relative heat source size (ε) and relative thermal conductivity (κ), which are defined as

$$\varepsilon = \frac{a}{b}, \tag{17}$$

$$\kappa = \frac{k_{\mathrm{HS}}}{k_{\mathrm{Sub}}}. \tag{18}$$

This validity of the model was verified with finite element simulations using COMSOL, as shown in Fig. 2 (a), in which the thermal resistances of GaN devices with and without Cu heat spreader are plotted for ε = 0.1 and cooling h_{Sub} of 10^5 W/m^2.K w, showing an excellent agreement between the model (dashed lines) and the COMSOL simulations (symbols). In Fig. 2 (b), the different components contributing to the total thermal resistance are plotted, which shows that the only thermal resistance

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affected by the heat spreader is the R_{Sp}, while the convective term (R_{Conv}), which is constant, depends on the cooling of the chip, and R_{1D} on the substrate thickness. A thinner substrate reduces R_{1D} but limits heat spreading in the substrate, causing a large R_{Sp} as can be seen in Fig. 2 (b). At a relative substrate thickness τ_{Sub} of 0.03, by adding a heat spreader with thickness τ_{HS} of 0.001, the thermal resistance can be reduced by 40% while τ_{HS} = 0.1 can reduce the spreading resistance by 83%, leading to a 2.4-time smaller total thermal resistance. By increasing the substrate thickness, the substrate spreading resistance is reduced, and reaches a minimum for relative substrate thicknesses $\tau_{Sub} > 0.3$. This implies that a limited heat spreading in very thin substrates, can be significantly compensated by the heat spreading provided by the near junction heat spreaders. However, to show the additional value and the real contribution of the heat spreaders to the total heat spreading, it is more reasonable to consider thick enough substrates that can provide most of their heat spreading. Therefore, the next simulations consider thick substrates, to ensure that the heat spreading in the substrate is not limited by its thickness, so the impact of heat spreaders on the spreading resistance can be more realistically studied.

In addition, to investigate the heat spreading in a more generalized way and to be independent of the absolute values of the sizes and thermal conductivities, dimensionless spreading resistances (ψ_s) were defined as

$$\psi_s = R_{Sp}\, a\, k_{Sub}\,. \qquad (19)$$

The dimensionless spreading resistance is plotted as a function of the relative heat spreader thickness in Fig. 3(a) for a relative heat source size of $\varepsilon = 0.1$, for diamond and Cu heat spreaders on SiC, GaN and Ga_2O_3 substrates, whose absolute and relative thermal conductivities are listed in Table 1.

Table 1. The absolute and relative thermal conductivity of selected materials

Material	k @ room temp. (W/m.K)	κ (Cu spreader)	κ (Diamond spreader)
Ga_2O_3	15 [9]	26	66.7
Si	130 [28]	3	7.7
GaN	160 [7]	2.4	6.3
SiC	490 [28]	0.8	2
Cu	390 [29]	-	-
Diamond (Polycrystalline)	1000 [18]	-	-

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The overall reduction of spreading resistance observed in Fig. 3(a) shows that with higher thermal conductivity, thinner heat spreaders are required. At higher relative thermal conductivities, by increasing the relative heat spreader thickness, ψ_s reduces significantly even at small τ_{HS}, and levels off at thicknesses larger than about $\tau_{HS} > 0.3$, achieving the lowest spreading resistances. The Cu spreaders can lead to a 1.8x reduction of spreading resistance for SiC, 3.4x for GaN and 26x for Ga_2O_3 devices. Using diamond heat spreaders the spreading resistance can be further reduced by 3x for SiC, 7x for GaN and 60x for Ga_2O_3 devices. These results show that by using relative heat spreader thicknesses above 0.3, the effect of heat spreaders can be maximized, and the extent of their impact can be determined by their relative thermal conductivity. As it can be seen, diamond heat spreaders on SiC substrate have a relative thermal conductivity (κ) of 2, leading to a 3x-reduction in spreading resistance, while the same diamond heat spreaders on Ga_2O_3 substrates have a relative thermal conductivity of 66.7, leading to a 60x-lower spreading resistance. Therefore, generally speaking, near junction heat spreaders have significantly more pronounced impact for lower thermal conductivity substrates.

The relative size of the heat source (ε) has a strong influence on the spreading resistance. Fig. 3(b) shows the dimensionless spreading resistance of GaN devices with Cu heat spreaders ($\kappa = 2.4$) as a function of relative heat source size. Because of the high heat constrictions in small heat sources without heat spreaders, a high spreading resistance is observed at small ε. By increasing the size of the heat source, the generated heat becomes less concentrated and the spreading resistance gradually reduces until it reaches zero at $\varepsilon = 1$. A relatively thin heat spreader with τ_{HS} of 0.01 leads to an overall reduction of the dimensionless spreading resistance with more pronounced effects at smaller relative heat sources.

Interestingly, for a fixed relative thickness τ_{HS} of 0.01, a positive slope was observed until $\varepsilon = 0.1$, showing that by increasing the heat source size, the heat spreader becomes less effective, which leads to higher spreading resistances. This means that such near junction heat spreaders are efficient for thermal management of smaller heat sources, or in other words, high heat fluxes in high power density devices. Increasing the thickness of the heat spreader to τ_{HS} of 0.1 leads to smaller spreading resistances as well as smaller positive slopes, which means that the heat spreader becomes more effective for a wider range of heat source sizes.

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Further increasing the τ_{HS} to 0.3, results in about a 3.4-time lower ψ_s for the entire range of source sizes, which is the minimum spreading resistance for such heat spreader/substrate combination (as shown in Fig. 3 (a) by the flat spreading resistance for $\tau_{HS} > 0.3$). Therefore, to maximize the effect of heat spreaders a relative thickness of 0.3 can be used as a rule of thumb for their design.

These results have also implications for a new class of materials with very high thermal conductivity, such as graphene sheets and individual carbon nanotubes (CNTs).[30,31] Despite their high thermal conductivities, an effective heat spreading would require thicknesses much larger than just a monolayer of carbon ($\tau_{HS} \sim 10^{-6}$), as shown in Fig. 3 (a), however stacking graphene layers to increase the thickness significantly reduces the effective lateral thermal conductivity, down to that of regular bulk graphite (about 700 W/m.K) after only 4 monolayers.[32]

The same applies for very thin layers of nanocrystalline diamond films[33–36], for which, the small thickness not only result in limited heat comduction, but also the thermal conductivity of the nanocrystalline diamond films[18] is usually much lower than that of microcrystalline diamond (as experimentally shown later in this paper). Therefore, the effect of diamond heat spreaders can be maximized by optimizing the thickness and the size of the diamond grains, which affects the thermal conductivity and the heat spreading capability.

Device Fabrication

Two sets of heat spreaders, based on diamond and Cu, were experimentally demonstrated on vertical PiN diodes on GaN-on-Silicon substrates. The fabrication and electrical characterization of the diodes can be found in a previous work.[37] The PiN diodes used in this study has an anode radius (r_A) of 10 µm, and presented a large breakdown voltage of 820 V and low specific on-resistance of 0.25 mΩ.cm^2, along with a large current density of 15 kA/cm^2. To provide electrical isolation between the device and the Cu heat spreaders, a 2 µm-thick SiO_2 layer was deposited at 300 °C using plasma-enhanced chemical vapor deposition (PECVD), and then patterned by dry etching to access the anode and cathode electrodes. Finally, a 6.5 µm-thick layer of Cu was electroplated and patterned on top of the devices.

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To fabricate diamond heat spreaders (Fig. 4), high-quality diamond layers were deposited on GaN vertical PIN diodes using microwave plasma assisted chemical-vapor-deposition (MPCVD). A 30 nm-thick SiN interlayer was deposited by PECVD to protect the GaN surface from decomposition during the diamond deposition, as well as to improve the adhesion of diamond and to reduce the TBR.[21,24] Prior to the MPCVD, devices were seeded inside an ultrasonic bath of isopropanol with nano-diamond particles. A 3 µm-thick layer of diamond was deposited at 820 °C using hydrogen and methane gas mixtures with the highest level of gas purity (N6.0) to avoid any impurity incorporation during the process. The temperature and pressure of deposition were optimized to obtain high quality diamond layers with large grain size and high thermal conductivity. The diamond layer was patterned using oxygen plasma with a SiO_2 mask to access the GaN surface to form the metal electrodes to the p- and n-type layers, followed by electroplated Cu pads.

Experimental results on Cu heat spreaders

The Scanning Electron Microscope (SEM) top and cross-sectional view images of a PiN diode with Cu heat spreader are shown in Fig. 5(a) and (b). Thermal measurements were performed using a Quantum Focus Instrument (QFI) IR microscope with a 512-by-512-pixels array of cooled IR detectors, which with a 20x magnification lens and filters, provided a high special resolution and accuracy. The IR microscope was equipped with a precise thermal stage, which enabled an accurate emissivity correction using the two-temperature emissivity calculation method as well as the factory-provided calibration data. In addition, to increase the emissivity of the chips and to avoid errors due to the IR transparency of the layers, a black paint was used on top of the chips. For all of the measurement points in this work accurate pixel-by-pixel emissivity calibrations was performed to ensure valid measurements.

The temperature at the top surface of the devices was measured at different biases. Since the heat source in the PiN diode is located below the heat spreader, the maximum temperature measured at the top surface of the heat spreader is not representative of the maximum device temperature because of a temperature drop in the thickness of the heat spreader. To estimate the maximum device temperature in the fabricated devices, the temperature profile was simulated using COMSOL and the surface temperature in the model was matched with the experimental measurements. The thermal model of the

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devices is depicted in Fig. 5(c), in which a volumetric heat source is located at the i-GaN layer in the structure to represent the joule heating in the device, and the device is cooled at the bottom by convective cooling. TBRs of 70 m^2K/GW was set between GaN and Si,[38] and 20 m^2K/GW between diamond and GaN.[21] The natural convection of air at the surface was neglected due to small surface area of the device, therefore all other boundary conditions were considered as adiabatic.

The SEM and thermal microscope images of two diodes with anode radius of 10 µm and heat spreaders of 15 µm and 60 µm are shown in Fig. 6 (a) and (b) respectively, which were measured at a dissipation power of 0.9 W, corresponding to a very large heat flux of 102 kW/cm^2 (normalized by the surface area of the i-GaN layer under the anode).

Such large heat flux caused a high hot spot temperature rise of about 180 °C and high temperature gradients near the edge of the heat source for the device with a small heat spreader, as shown in Fig. 6 (a). The use of a 60 µm heat spreader resulted in a reduction of 73 °C in the maximum temperature, and much smaller thermal gradients in the device footprint, as shown in Fig. 6 (b). Fig. 6 (c) shows an excellent agreement between the thermal resistances measured from the maximum surface temperatures on the fabricated devices (symbols) and the COMSOL simulations (dashed lines). However, the device thermal resistance (solid lines), calculated from the maximum device temperatures in the i-GaN layer, are slightly higher due to a temperature drop in the heat spreader along its thickness. By using 60 µm-radius Cu heat spreaders, a significant drop of the thermal resistance was observed (Fig. 6 (c)), which resulted in a reduction of 2.3x, 1.7x, 1.4x and 1.37x on the total thermal resistance for the devices with anode radius of 5, 10, 20 and 30 µm, respectively.

Experimental results on Diamond heat spreaders

The characteristics of MPCVD-deposited diamond layers on GaN-on-Si substrate are shown in Fig. 7(a) and (b). The effective in-plane thermal conductivity of a 3µm-thick diamond layers with an average grain size of 1µm were as high as 900 W/m.K. The superb effective lateral thermal conductivity and

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electrical insulation of such films deposited heterogeneously on GaN makes them extremely promising for near junction heat spreading applications.

It must be noted that the thermal conductivity of the heterogeneously deposited diamond layers are not uniform and can vary though their thickness, with higher values at the top surface and smaller values near the seeding layer, due to their different grain size.[39] However, it has been shown that to accurately determine the steady-state thermal performance of the devices, an average thermal conductivity can be used instead of a gradient of thermal conductivities.[23] In this study, the effective lateral thermal conductivity of the diamond was measured using devices with structures as shown in the inset of Fig. 7(b), by a similar technique explained in [40,41]. In these devices, parts of the Si substrate was removed to fabricate diamond/GaN membranes and a resistive heater was deposited at the center of the membrane. Accurate measurements were done using an IR microscope to determine the lateral temperature gradient on the membrane. Using the thermal conductivity of GaN as well as the thickness of GaN and diamond, the effective thermal conductivity of diamond was determined using the measured temperature gradient and normalized by the total thickness of diamond.

The SEM and cross sectional images of a fabricated device with a 3 µm-thick diamond heat spreader are shown in Fig. 7(c) and (d). The undoped diamond layer serves as high thermal conductivity heat spreader, and also provides electrical isolation to the Cu pads. Therefore, the use of diamond spreaders eliminate the need for SiO_2 insulating layer, which has a very poor thermal conductivity (about 1 W/m.K [42]). In addition, as it can be seen in Fig. 7 (d), the Cu pads not only provide extra heat spreading, it also connects the heat source (diode) to the top side of the diamond layer, which has the highest thermal conductivity, thus bypasses the lower thermal conductivity diamond layer near the device.

Fig. 8(a) and (b) show the IR microscope images of two devices with r_A=10 µm at a power dissipation of 0.9 W and diamond heat spreaders of 15 µm and 60 µm, respectively. A 64% lower temperature is observed in the device with larger heat spreader in Fig. 8(b) compared without heat spreaders, which shows the excellent heat spreading of diamond heat spreaders. In Fig. 8(c), the spreading resistance of the GaN-on-Si devices with Cu and Diamond heat spreaders (symbols), are compared with simulated spreading resistance of devices without heat spreaders on GaN-on-Si, GaN-on-SiC and GaN-on-

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Diamond substrates (dashed lines), with TBRs of 70, 60 and 10 m^2.K/GW as typical values for such substrate, respectively.[20,38,43] By using Cu heat spreaders on GaN-on-Silicon devices, the thermal spreading resistance of the diodes with r_A of 10 µm can be similar to that of GaN-on-SiC devices, and for a radius of 5 µm, it can be as low as that of GaN-on-Diamond devices. On the other hand, by using 3µm-thick diamond spreaders with a radius of 60 µm for the devices with r_A of 10 µm, leads to a 2.8x reduction of the spreading resistance, showing excellent spreading resistances similar to the devices on GaN-on-diamond substrates. These results show that the near junction thermal managements achieved with relatively thin layers of heat spreaders can provide heat spreading properties as good as those of high-cost high thermal conductivity substrates, such as SiC and diamond, offering a cost-effective thermal management technology for low thermal conductivity substrates.

Conclusions

In this work, near-junction heat spreaders were demonstrated for thermal management of high heat flux hot spots generated in high power density devices. The analytical thermal model and analysis presented in this study, based on dimensionless spreading resistances and relative geometrical and material parameters, provide a comprehensive method to assess the effect of any heat spreaders/substrates combinations. The model also provides design guidelines for efficient near junction heat spreaders and shows the broad view of their impact on the thermal performance of devices.

Diamond and Cu heat spreaders were fabricated on vertical GaN PIN diodes and characterized, together with accurate simulations. The experimental results showed a large reduction of device temperature and a more uniform temperature profile in the device footprint due to the significant enhancement of heat spreading. Using near junction diamond heat spreaders on GaN-on-Si substrates, with a thickness of only 3 µm, demonstrated heat spreading resistances similar to those of GaN-on-Diamond substrates. This work shows that the near junction heat spreaders can offer effective low-cost thermal management solutions for power devices, especially those on low thermal conductivity substrates, such as Ga_2O_3, GaN-on-Silicon, GaN-on-Sapphire or even bulk GaN substrates. This thermal management technology could be leveraged to achieve high power densities in power electronic devices, such as transistors and diodes, as well as in power optoelectronic devices, such as laser diodes.

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References

[1] Y. Won, J. Cho, D. Agonafer, M. Asheghi, and K.E. Goodson, Tech. Dig. - IEEE Compd. Semicond. Integr. Circuit Symp. CSIC 1 (2013).

[2] Y. -f. Wu, M. Moore, A. Saxler, T. Wisleder, and P. Parikh, IEEE Device Res. Conf. 151 (2007).

[3] R. Leoni, N. Kolias, P. Jablonski, F. Altunkilic, E. Johnson, and W. Bourcy, 2017 IEEE Compd. Semicond. Integr. Circuit Symp. CSICS 2017 1 (2017).

[4] Y. Won, J. Cho, D. Agonafer, M. Asheghi, and K.E. Goodson, IEEE Trans. Components, Packag. Manuf. Technol. **5**, 737 (2015).

[5] E. Heller, S. Choi, D. Dorsey, R. Vetury, and S. Graham, Microelectron. Reliab. **53**, 872 (2013).

[6] Y.S. Muzychka, K.R. Bagnall, and E.N. Wang, IEEE Trans. Components, Packag. Manuf. Technol. **3**, 1826 (2013).

[7] J. Zou, D. Kotchetkov, A.A. Balandin, D.I. Florescu, and F.H. Pollak, J. Appl. Phys. **92**, 2534 (2002).

[8] H.W. Xue, Q.M. He, G.Z. Jian, S.B. Long, T. Pang, and M. Liu, Nanoscale Res. Lett. **13**, (2018).

[9] Z. Guo, A. Verma, X. Wu, F. Sun, A. Hickman, T. Masui, A. Kuramata, M. Higashiwaki, D. Jena, and T. Luo, Appl. Phys. Lett. **106**, 111909 (2015).

[10] B. Chatterjee, A. Jayawardena, E. Heller, D.W. Snyder, S. Dhar, and S. Choi, Rev. Sci. Instrum. **89**, 114903 (2018).

[11] M.H. Wong, Y. Morikawa, K. Sasaki, A. Kuramata, S. Yamakoshi, and M. Higashiwaki, Appl. Phys. Lett. **109**, 193503 (2016).

[12] T. Ohki, A. Yamada, Y. Minoura, K. Makiyama, J. Kotani, S. Ozaki, M. Sato, N. Okamoto, K. Joshin, and N. Nakamura, IEEE Electron Device Lett. **40**, 287 (2019).

[13] J.G. Felbinger, M.V.S. Chandra, Y. Sun, L.F. Eastman, J. Wasserbauer, F. Faili, D. Babic, D. Francis, and F. Ejeckam, IEEE Electron Device Lett. **28**, 948 (2007).

[14] G.D. Via, J.G. Felbinger, J. Blevins, K. Chabak, G. Jessen, J. Gillespie, R. Fitch, A. Crespo, K. Sutherlin, B. Poling, S. Tetlak, R. Gilbert, T. Cooper, R. Baranyai, J.W. Pomeroy, M. Kuball, J.J. Maurer, and A. Bar-Cohen, Phys. Status Solidi Curr. Top. Solid State Phys. **11**, 871 (2014).

[15] D. Francis, F. Faili, D. Babić, F. Ejeckam, A. Nurmikko, and H. Maris, Diam. Relat. Mater. **19**, 229 (2010).

[16] H. Amano, Y. Baines, E. Beam, M. Borga, T. Bouchet, P.R. Chalker, M. Charles, K.J. Chen, N. Chowdhury, R. Chu, C. De Santi, M.M. De Souza, S. Decoutere, L. Di Cioccio, B. Eckardt, T. Egawa, P. Fay, J.J. Freedsman, L. Guido, O. Häberlen, G. Haynes, T. Heckel, D. Hemakumara, P. Houston, J. Hu, M. Hua, Q. Huang, A. Huang, S. Jiang, H. Kawai, D. Kinzer, M. Kuball, A. Kumar, K.B. Lee, X. Li, D. Marcon, M. März, R. McCarthy, G. Meneghesso, M. Meneghini, E. Morvan, A. Nakajima, E.M.S. Narayanan, S. Oliver, T. Palacios, D. Piedra, M. Plissonnier, R. Reddy, M. Sun, I. Thayne, A. Torres, N. Trivellin, V. Unni, M.J. Uren, M. Van Hove, D.J. Wallis, J. Wang, J. Xie, S. Yagi, S. Yang, C. Youtsey, R. Yu, E. Zanoni, S. Zeltner, and Y. Zhang, J. Phys. D. Appl. Phys. **51**, 163001 (2018).

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PLEASE CITE THIS ARTICLE AS DOI: 10.1063/1.5123615

[17] P.K. Schelling, L. Shi, and K.E. Goodson, Mater. Today **8**, 30 (2005).

[18] H. Dong, B. Wen, and R. Melnik, Sci. Rep. **4**, 7037 (2014).

[19] R.B. Simon, J. Anaya, F. Faili, R. Balmer, G.T. Williams, D.J. Twitchen, and D.M. Kuball, Appl. Phys. Express **9**, (2016).

[20] L. Yates, J. Anderson, X. Gu, C. Lee, T. Bai, M. Mecklenburg, T. Aoki, M.S. Goorsky, M. Kuball, E.L. Piner, and S. Graham, ACS Appl. Mater. Interfaces **10**, 24302 (2018).

[21] Y. Zhou, J. Anaya, J. Pomeroy, H. Sun, X. Gu, A. Xie, E. Beam, M. Becker, T.A. Grotjohn, C. Lee, and M. Kuball, ACS Appl. Mater. Interfaces **9**, 34416 (2017).

[22] S. Lee, S. Song, V. Au, and K.P. Moran, in *Proc. 4th ASME/JSME Therm. Eng. Jt. Conf.* (1995), pp. 199–206.

[23] Y. Zhou, R. Ramaneti, J. Anaya, S. Korneychuk, J. Derluyn, H. Sun, J. Pomeroy, J. Verbeeck, K. Haenen, and M. Kuball, Appl. Phys. Lett. **111**, 41901 (2017).

[24] L. Yates, J. Anderson, X. Gu, C. Lee, T. Bai, M. Mecklenburg, T. Aoki, M.S. Goorsky, M. Kuball, E.L. Piner, and S. Graham, ACS Appl. Mater. Interfaces **10**, 24302 (2018).

[25] Y.S. Muzychka, M.M. Yovanovich, and J.R. Culham, *Influence of Geometry and Edge Cooling on Thermal Spreading Resistance* (2008).

[26] K.R. Bagnall, Y.S. Muzychka, and E.N. Wang, IEEE Trans. Components, Packag. Manuf. Technol. **4**, 817 (2014).

[27] W.B. Joyce and R.W. Dixon, J. Appl. Phys. **46**, 855 (1975).

[28] G.A. Slack, J. Appl. Phys. **35**, 3460 (1964).

[29] P. Nath and K.L. Chopra, *Thermal Conductivity of Copper Films* (1974).

[30] A.A. Balandin, S. Ghosh, W. Bao, I. Calizo, D. Teweldebrhan, F. Miao, and C.N. Lau, Nano Lett. **8**, 902 (2008).

[31] A.A. Balandin, Nat. Mater. **10**, 569 (2011).

[32] S. Ghosh, W. Bao, D.L. Nika, S. Subrina, E.P. Pokatilov, C.N. Lau, and A.A. Balandin, Nat. Mater. **9**, (2010).

[33] M. Seelmann-Eggebert, P. Meisen, F. Schaudel, P. Koidl, A. Vescan, and H. Leier, *Heat-Spreading Diamond Films for GaN-Based High-Power Transistor Devices* (2001).

[34] T.J. Anderson, K.D. Hobart, M.J. Tadjer, A.D. Koehler, T.I. Feygelson, J.K. Hite, B.B. Pate, F.J. Kub, and C.R. Eddy, Tech. Dig. - IEEE Compd. Semicond. Integr. Circuit Symp. CSIC 1 (2013).

[35] M. Alomari, M. Dipalo, S. Rossi, M.A. Diforte-Poisson, S. Delage, J.F. Carlin, N. Grandjean, C. Gaquiere, L. Toth, B. Pecz, and E. Kohn, Diam. Relat. Mater. **20**, 604 (2011).

[36] T.J. Anderson, K.D. Hobart, M.J. Tadjer, A.D. Koehler, E.A. Imhoff, J.K. Hite, T.I. Feygelson, B.B. Pate, C.R. Eddy, and F.J. Kub, ECS J. Solid State Sci. Technol. **6**, Q3036 (2016).

[37] R.A. Khadar, C. Liu, L. Zhang, P. Xiang, K. Cheng, and E. Matioli, IEEE Electron Device Lett. **39**, 401 (2018).

[38] J. Kuzmík, S. Bychikhin, D. Pogany, C. Gaquìre, E. Pichonat, and E. Morvan, J. Appl. Phys. **101**, 54508 (2007).

[39] J. Anaya, S. Rossi, M. Alomari, E. Kohn, L. Tóth, B. Pécz, K.D. Hobart, T.J. Anderson, T.I. Feygelson, B.B. Pate, and M. Kuball, Acta Mater. **103**, 141 (2016).

[40] J. Anaya, S. Rossi, M. Alomari, E. Kohn, L. Tóth, B. Pécz, and M. Kuball, Appl. Phys. Lett. **106**, 223101 (2015).

[41] V. Linseis, F. Völklein, H. Reith, P. Woias, and K. Nielsch, J. Electron. Mater. **47**, 3203 (2018).

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[42] T. Yamane, N. Nagai, S.I. Katayama, and M. Todoki, J. Appl. Phys. **91**, 9772 (2002).
[43] A. Manoi, J.W. Pomeroy, N. Killat, and M. Kuball, IEEE Electron Device Lett. **31**, 1395 (2010).

Figure Captions

Fig. 1 (a) Geometry and boundary conditions of the model. (b) Thermal circuit model and the unit-cell concept in scaled up devices. (c) Heat spreader's approximate and (d) alternative boundary conditions.

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Fig. 2 (a) Total thermal resistance (R_θ) as a function of the relative GaN substrate thickness, with and without Cu heat spreader compared at two relative heat spreader thicknesses. The excellent agreement between the analytical model (dashed lines) and COMSOL simulations (symbols) shows the accuracy of the proposed analytical model. (b) (left y-axis) Spreading resistance (R_{Sp}) and (right y-axis) sum of one-dimensional conduction (R_{1D}) and convective (R_{Conv}) thermal resistances versus relative substrate thickness, showing the contribution of each thermal resistance to the total thermal resistance of the device and the fact that heat spreaders strongly reduce the spreading resistances. The dashed lines are from the analytical model and the symbols from COMSOL simulations.

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Fig. 3 (a) Dimensionless spreading resistance (ψ_s) as a function of the relative thickness of Cu or diamond heat spreaders (τ_{HS}) for Ga_2O_3, GaN and SiC substrates with relative heat source size (ε) of 0.1. (b) Dimensionless spreading resistance of GaN devices with Cu heat spreaders as a function of heat source size (ε) at different heat spreader thicknesses.

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Fig. 4 Fabrication process of GaN PiN diodes with diamond heat spreaders: (a) SiO_2 deposition and pattering using photoresist and dry etching of SiO_2. (b) Deep etching of GaN for mesa isolation, deposition of SiN interlayer and diamond seeding step (c) CVD deposition of micro crystalline diamond. (d) SiO_2 deposition as a masking layer for diamond etching. (e) SiO_2 mask patterning. (f) Diamond etching with oxygen plasma. (g) SiO2 and SiN interlayer removal. (g) Ohmic contacts to the n and p type semiconductors. (h) Cu electroplating.

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Fig. 5(a) SEM picture of a GaN vertical PiN diode with a Cu heat spreader. (b) Cross sectional image of the device across *AB* indicated in (a). (c) Schematic of the device structure simulated in COMSOL.

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Fig. 6 (a) SEM and IR microscope image of the device with anode of 10 µm and heat spreader radius of 15 µm and (b) 60 µm, both operated at 0.9 W, respectively. (c) Total thermal resistance (R_θ) as function of Cu heat spreader radius (r_{Cu}) at different anode radius (r_A). Dashed lines are from COMSOL simulations matching the experimental points (symbols), based on the hot spot temperature at the top surface, and solid lines are the device thermal resistance calculated from the maximum device temperature from COMSOL simulations.

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Fig. 7 (a) Average grain size as a function of the diamond layer thickness. The symbols are from the experiments and the dashed lines show the theoretical spread of grain sizes.[19] (b) Effective in-plane thermal conductivity of the diamond layers. The symbols are the measured values and the dashed line is the theoretical effective thermal conductivity of the polycrystalline diamond.[18] The inset shows the cross-sectional schematic of the suspended membranes with heaters at the center, which were fabricated to measure the effective lateral thermal conductivity of diamond. (c) SEM picture of a vertical GaN PiN diode with diamond heat spreaders. (d) The cross sectional image of the device across the *AB* line shown in (b).

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Fig. 8(a) IR microscope image of the device with anode of 10 μm and diamond heat spreader of 15μm and (b) 60 μm both operated at 0.9W, showing maximum temperatures of 137 °C and 86 °C, respectively. (c) Experimental spreading resistance of diodes with Cu (blue symbols) and Diamond (red symbols) heat spreaders compared with the spreading resistance in GaN-on-Si, GaN-on-SiC and GaN-on-diamond substrates (dashed lines). Symbols with the lightest colors correspond to heat spreaders with a radius 60 μm.

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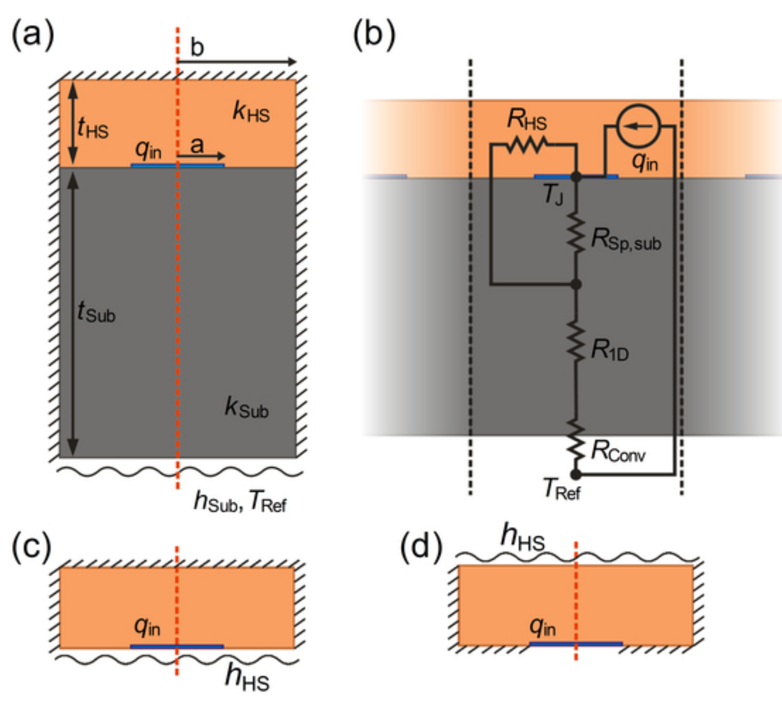

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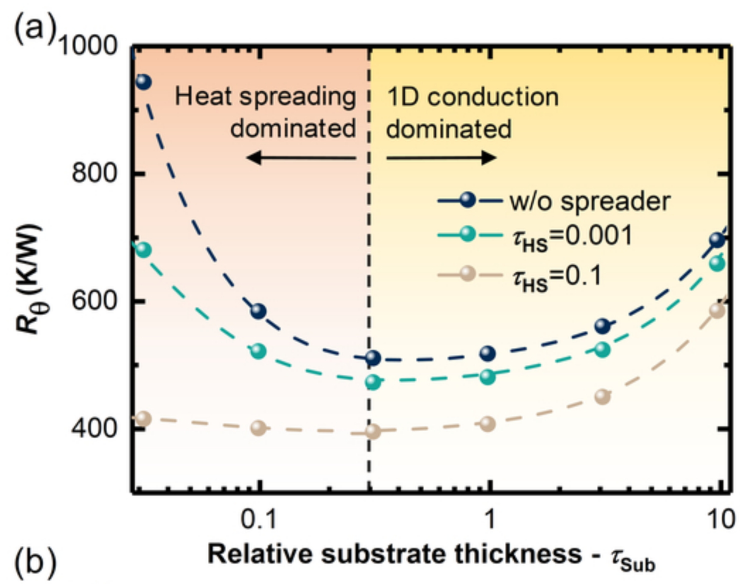

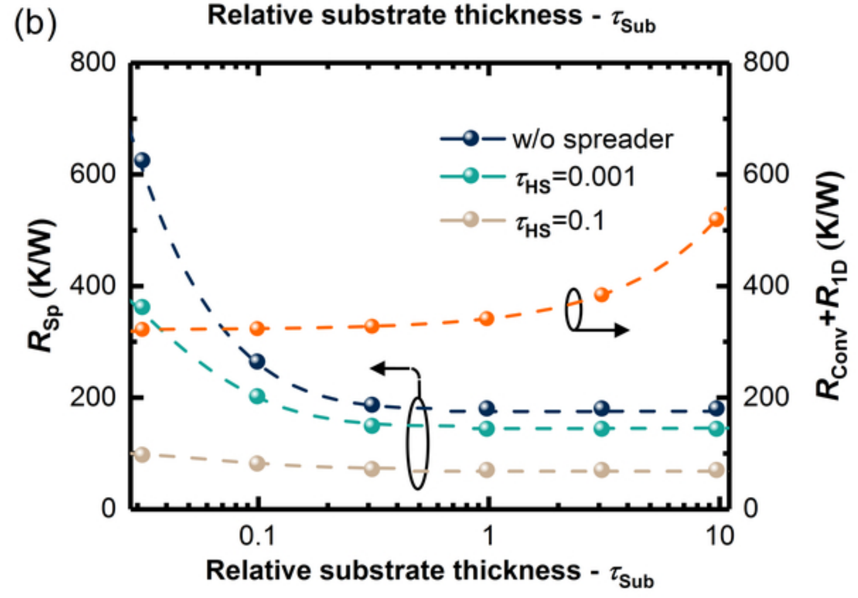

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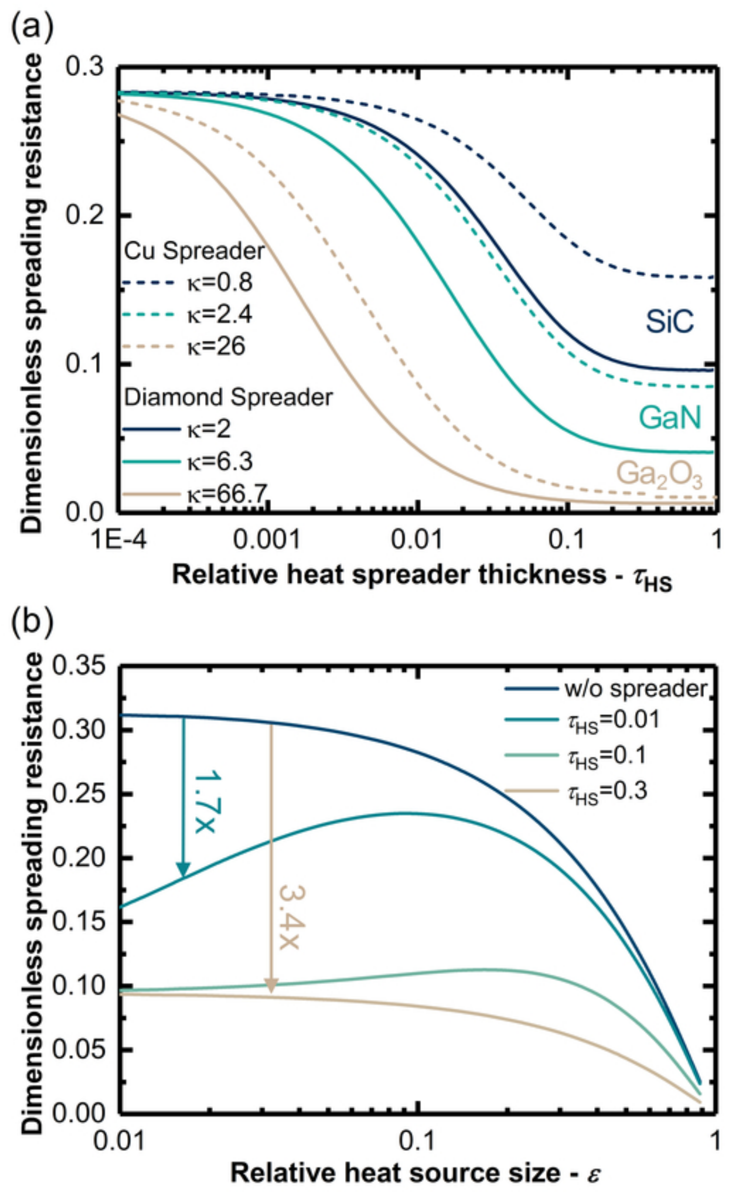

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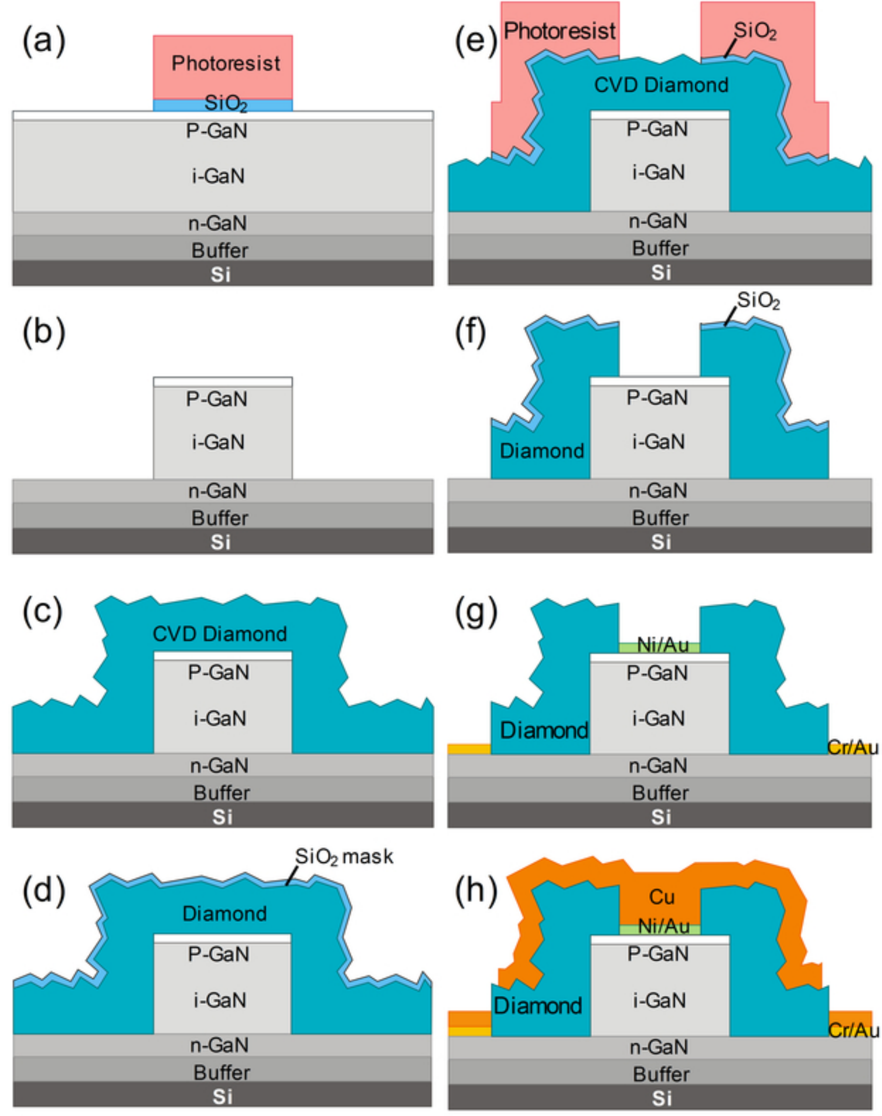

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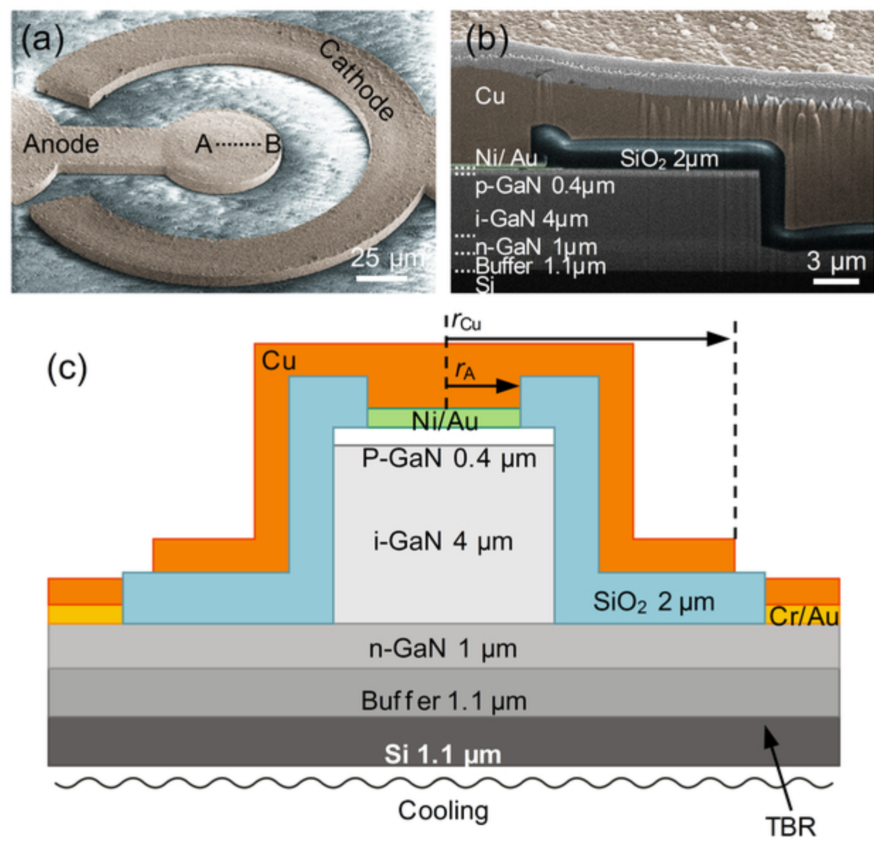

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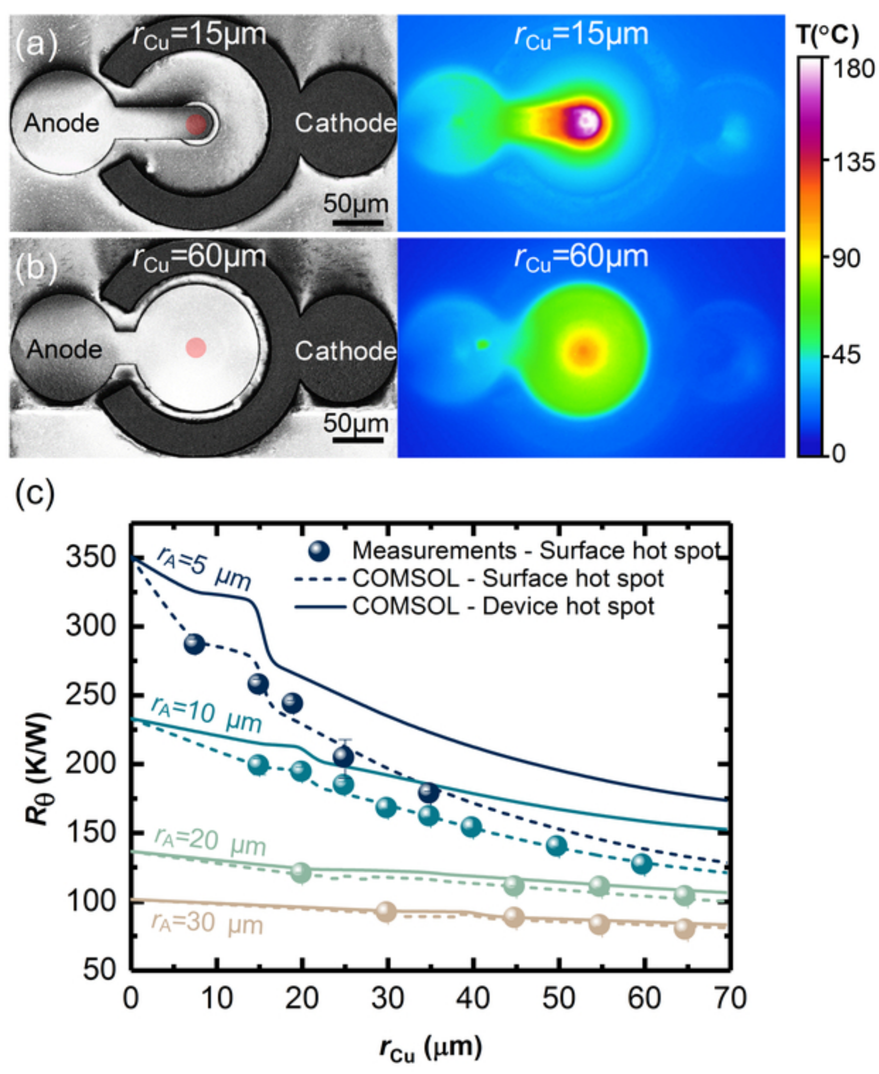

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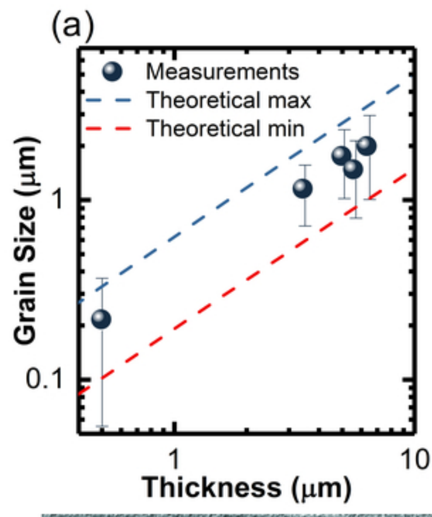

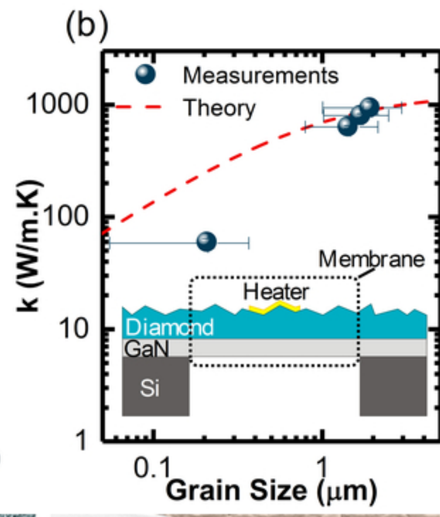

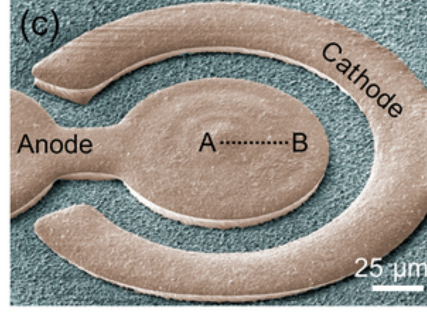

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