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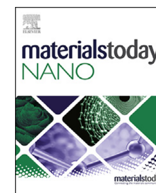

Semiconductor nanowires: to grow or not to grow?

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ABSTRACT

Semiconductor nanowires have demonstrated exciting properties for nanophotonics, sensors, energy technologies, and end-of-roadmap and beyond-roadmap electronic devices. Fabrication schemes for nanowires are varied, but they fall into three general categories: (1) top-down lithographic patterning and etching of bulk crystals and epitaxial films; (2) bottom-up, locally catalyzed crystal growth of nanowires; and (3) hybrid methods that combine aspects of categories (1) and (2). In this article, we examine the relative merits and unique attributes of each of these paradigms for nanowire synthesis. We review literature relevant to nanowire fabrication methods, faceting and dimensional control (diameter and length), positioning and alignment, doping, bulk and surface defects, and formation of unique nanowire heterostructures and metastable phases. Finally, we describe the factors governing selection among top-down, bottom-up, and hybrid methods to fabricate nanowire structures depending on their desired structural features and applications.

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We are living today in the era of nanotechnology. Nanostructures are part of many products, ranging from sunscreens to catalysts to computers. These nanostructures are obtained by very different fabrication methods having aspects of growth from atomic constituents (bottom-up) and/or sculpturing of larger-scale solids down to nanoscale dimensions (top-down). Both top-down and bottom-up approaches have their specific advantages and disadvantages, especially when it comes to semiconductor nanostructures.

This situation naturally leads to a question regarding semiconductor nanowires: to grow or not to grow? This review outlines some of the main characteristics of the bottom-up and top-down approaches for nanowire fabrication and of their combination in hybrid methods. Its purpose is to introduce these issues to newcomers to the field and to provide a perspective for deciding on research and development priorities among scientists and engineers investigating semiconductor nanowires and their applications.

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1. NW growth

1.1. Growth modes

Universal to all nanowire growth is crystal growth anisotropy: a particular physical aspect constrains growth so that it takes place along one crystallographic direction at a much higher rate than others. This anisotropy results in the formation of one-dimensional needle-like structures such as nanowires. Images of these needle-like structures remind one of macroscopic crystals in a geology museum, the underlying processes governing anisotropic growth being extremely similar. The most common way to obtain anisotropic growth at the nanoscale is the use of metal nanoparticle catalysts, which can be in either the solid or liquid phase under nanowire growth conditions [see Fig. 1(a)]. Gaseous precursors supplied in either molecular or atomic form are preferentially gathered and (for molecules) decomposed by these metal nanoparticles. Upon supersaturation of the nanoparticles, the precursor component(s) precipitate beneath them. Continuous transport of precursor components from the gas phase via the catalysts to the growing solid crystals beneath results in the formation of nanowires with diameters determined by the catalyst size. Whether the nanoparticle catalyst is in a liquid or solid state defines whether growth occurs via the so-called vapor-liquid-solid (VLS) or vapor-

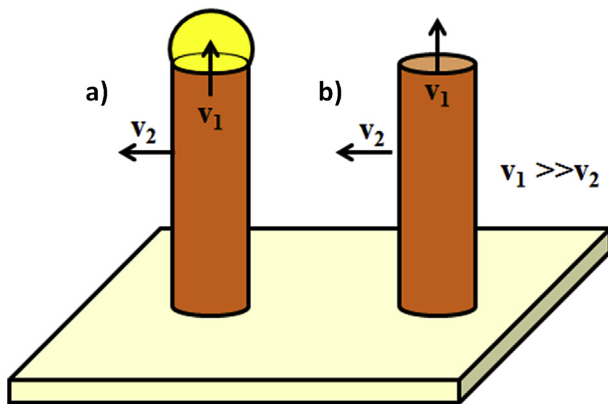

Fig. 1. Schematic depicting anisotropy of axial and radial nanowire growth rates: (a) a liquid or solid metal droplet (VLS/VSS) serves as a catalyst for the preferential decomposition and gathering of growth precursors and provides the driving force for a much higher growth rate in the axial direction; (b) the vapor-solid method (VS) uses differentiated growth rates for different facets planes to create an anisotropic nano-scale crystal. VLS, vapor-liquid-solid; VSS, vapor-solid-solid.

solid-solid (VSS) mechanisms. Pioneers who identified and brought understanding of these new methods of crystal growth in the 1960s and 70s were Wagner and Ellis [1] at Bell Laboratories and Givargizov at the Academy of Sciences in Moscow [2].

It was not until the 1990s that VLS and VSS were widely recognized as bottom-up approaches for obtaining semiconductors with tailored dimensions on the nanoscale. One of the first semiconductors synthesized by VLS in the form of nanowires was silicon [3–6]. In the search for more sophisticated physics and a wider range of application in devices, arsenide and phosphide [7–15] and nitride [16–18] III-V semiconductors brought new possibilities. Changing the composition of III-V nanowires during growth allows for new forms of band gap engineering at the nanoscale. The reduced diameter of nanowires permits combining materials with a high lattice mismatch, and local changes in crystal phase provide novel ways to vary materials properties. These new forms and examples of band gap engineering provide new opportunities for both fundamental science and applications. Motivated by the important milestones achieved with nanowires in the last decade, fundamental understanding on the crystal growth by VLS and VSS has improved, and at the same time, it has provoked new questions. As an example, the role of the triple-phase line and contact angle in the nucleation of layers in nanowire growth and in the appearance of polytypism have been outlined, but the details of their contribution to specific growth outcomes is not yet understood in a completely satisfactory manner. Detailed reviews on this topic have been published recently [19–26].

The success of VLS and VSS may reside in their versatility both for achieving quasi-1D growth of many different materials and for accommodating different precursors and delivery methods. In chemical vapor deposition (CVD), including metal-organic CVD (MOCVD) molecular precursors such as SiH_4, PH_3, or $(CH_3)_3Ga$ are preferentially decomposed on the metal nanoparticle surface. This is the reason why this metal is often called a ‘catalyst’ in VLS and VSS. Upon decomposition, precursors are incorporated and diffused through the catalyst nanoparticle. In non-CVD techniques such as electron-beam evaporation, pulsed-laser deposition, or molecular beam epitaxy (MBE), a flux of atomic species is produced by evaporation or sublimation. Here, the nanoparticle acts as a site where adatoms preferentially stick [27,28]. A deposition technique that combines both aspects is plasma-enhanced CVD. For a comprehensive review on the different deposition techniques, see for example Refs. [29,30].

VLS and VSS can even be generalized to growth from a liquid solution. Typically, supercritical organic solutions at high pressure enriched in precursor species are used. In this case, the growth mechanism is referred to as SLS: solution-liquid-solid growth. It has been applied to a variety of semiconductors including Si [31,32], Ge [33], ZnO [34], and CdSe [35].

Finally, in the vapor-solid (VS) approach [Fig. 1(b)], crystal growth anisotropy is fostered by the accentuated growth rate along one crystal direction with respect to more depressed rates of deposition onto facets bounding this preferred growth axis, see Fig. 1b [36–40]. The dynamics of the system determine in this case the final shape of the crystal [41] rather than purely energetic (Wulff) considerations [42].

1.2. Faceting during crystal growth

Faceting during nanowire growth is driven, in a thermodynamic picture, by the anisotropy of surface energy and, from a kinetic viewpoint, by the anisotropy of surface reaction (in this case, atom attachment) rate. The full picture for understanding of the final shape has to consider these two elements [43]. Surfactants can play a role in such processes by segregating strongly to surfaces and encouraging the preferential development of certain facet planes. There are numerous examples of surfactant-mediated shape control of solution-grown semiconductor nanostructures [44]. Vapor phase crystal growth can also be strongly influenced by surfactants [45], such as dopant species that can eventually be incorporated into semiconductor nanowires during CVD or MBE.

Surface facet development during growth can dictate and modify the axial crystallographic alignment and polarity of the wires [47–53]. This occurs because the chemical potential reduction of the components incorporated into a nanowire from the growth environment that occurs with each increment of wire axial growth is dependent upon the sidewall facet planes and their surface energies [40,47]. Especially for small nanowire diameters, where sidewall energies make an increasing contribution, this effect will bias wires into a particular orientation [6]. For example, for synthesis of Si or Ge nanowires via Au-mediated VLS growth, a transition diameter of ~20 nm is observed below which the typical <111> axial direction switches to <110>. [47,51]. The <110> direction produces lower-energy {111} and {100} sidewall facets than the pseudo {112} facets reported for the sidewall surface planes of the <111>-oriented nanowires [40]. Closer inspection of the sidewalls of Si and Ge <111>-oriented wires often indicates that the nominal {112} sidewall facets for this axial orientation break up into a saw-tooth facet structure (Fig. 2) composed of small inclined {111} and {113} facet segments [46].

1.3. Contact angle

One of the key aspects for VLS and VSS growth is the capillary stability of the metal catalyst at the nanowire tip. The stability and shape of the metal catalyst determines where the new layers start, the crystal phase, growth direction, and even the possibility of tilting.

Typically, the metal catalyst is characterized by the contact angle it forms with the nanowire growth facet. The equilibrium contact angle can be calculated if the surface and interface energies and geometries are known [54]. Fig. 3(a) depicts three different scenarios of a liquid catalyst droplet on top of a nanowire: a droplet wetting on top of a cylindrical nanowire, a tapered nanowire, and a nanowire with an external edge. For the first two cases, we also plot the possibility that the droplet wets the nanowire side facets [18,59] (dark yellow). The metal droplet exhibits a surface energy $\gamma_{LV}$and radius R, generally different from

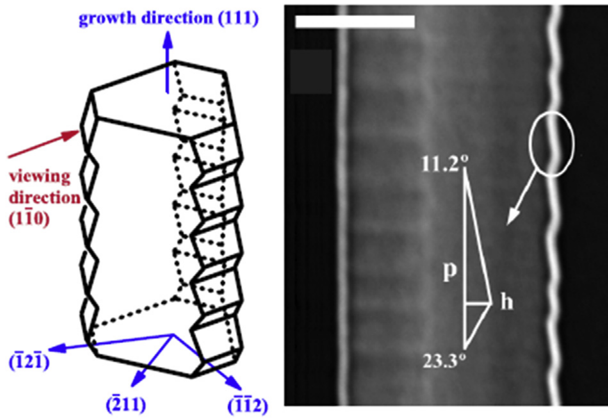

Fig. 2. Sidewall facet structure of <111>-oriented VLS-grown Si nanowire (600 °C disilane ultra high vacuum CVD). Scale bar is 50 nm [46]. VLS, vapor-liquid-solid; CVD, chemical vapor deposition.

the nanowire radius r. $\gamma_{LS}$and γ_{SV}correspond to the solid-liquid interface and facet surface energies, respectively. β corresponds to the contact angle of the metal-containing droplet with the projected nanowire-liquid interface. θ is the tapering angle of the slightly tapered nanowires. We consider also the case in which the interface between the solid nanowire and the liquid droplet is not flat, but with an external edge as it has been observed by Schwartz et al. [55]. One should note that β can be quantified in, for example, cross-section scanning electron microscope (SEM) measurements when the liquid-solid interface is flat and the metal does not wet the facets.

For the system to be in equilibrium, the Gibbs free energy of system G should remain constant and at a minimum value (dG = 0). Traditionally, the solution is found by minimizing the Gibbs energy as a function of R in the form:$G_o = \frac{\gamma_{LV} 2\pi R^2}{(1+\cos\beta)} + \gamma_{SL}\pi R^2$. The result is equivalent to assuming that the droplet is in equilibrium when the horizontal forces acting on the droplet are equal [56,57]:

This derivation of what is known as the Nebol'sin-Shchetinin criterion has been very often used to explain and calculate the equilibrium contact angle of catalyst droplets on top of the nanowires. Recently, the limitations of using this expression have been elucidated [58].

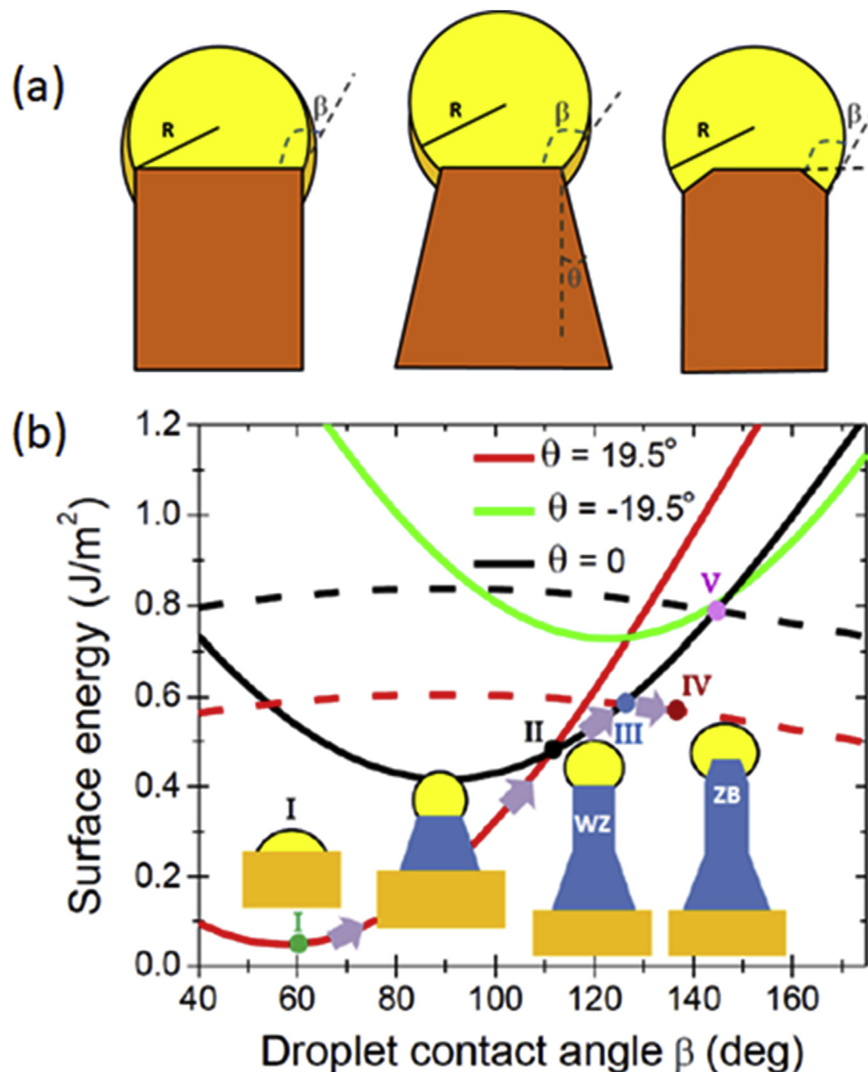

Fig. 3. (a) Drawings of the three main types of configurations that the liquid metal droplet can adopt on top of a compound semiconductor nanowire, one should note that the value of β also depends on the catalyst-solid interface morphology. (b) Extended Nebol'sin criterion (from Ref.59 ©).

In the Nebol'sin-Shchetinin criterion, G_o is minimized by varying R, which at the same time has an impact on the liquid-solid interface energy, and it is obviously not a free parameter. A more sophisticated version of this calculation should include a fixed volume of the droplet by fixing at least the radius of the nanowire [59]. The model developed recently by V.G. Dubrovskii predicts the evolution of the contact angle during growth by considering the variation in surface energy when a new monolayer is formed as a function of the contact angle and for the three geometries of Fig. 3(a). The results of the model applied to the Au-GaAs system are shown in Fig. 3(b). Dashed and continuous lines correspond respectively to the droplet wetting or not wetting the nanowire side facets, respectively. Fig. 3(b) also shows possible evolution of the droplet contact angle as follows, which can explain the variety of contact angles observed in the literature. At the beginning of growth, the catalyst nanoparticle is located on the substrate, with a relatively small contact angle. As the nanowire is formed, the contact angle will increase, resulting in an inward tapering geometry. As the nanowire increases in length, the radius is reduced at the same time that β increases. Steady state can be achieved in these conditions. The equilibrium contact angle is slightly larger than 90° and smaller than what would be obtained by the Nebol'sin-Shchetinin relation. In the case the droplet increases in size, the contact angle will also increase at the expense of its stability on top. At a critical angle the droplet would slide on to the nanowire sidewall facets. Sliding of the droplet as a result of increasing volume was recently observed by Potts et al. [60].

The effect of the contact angle on the shape of the liquid-solid interface has profound consequences, such as the existence of polytypism in nanowires of compound semiconductors such as GaAs. A flat interface provides the triple-phase line as a preferred nucleation site of each new monolayer of the solid. Energetic considerations and experiments in arsenide and phosphides show that this nucleation fosters the formation of wurtzite phase, for a range of wetting angles [61–64]. Nucleation on the liquid-solid interface, and not at the triple-phase line, is predicted to result in the formation of the zinc blende phase.

Controlling the contact angle can also modify the crystal growth direction and polarity [65–68]. A satisfactory microscopic picture explaining the mechanism is, to the best of our knowledge, still missing. Complete mastery of nanowire growth direction is key not only for the fabrication of nanowire-based complex structures such as crosses [69] but also for the integration of nanowires in electronic, photovoltaic, and optoelectronic device platforms based on bulk single crystal substrates.

2. Catalyst selection

The nature of the catalyst chosen for either VLS or VSS often determines the overall kinetics of nanowire deposition. The nature of the catalyst also determines the compatibility with other materials and device fabrication methods because of its effects on the parameter space for growth and because of potential contamination issues. A catalyst nanoparticle should favor the selective gathering and decomposition of the growth precursors. The precursor elements should, in principle, be soluble in the catalyst metal or compound or diffuse readily via surface sites around its periphery to reach the interface with either the substrate (during wire nucleation) or with the growing solid (during wire growth). Whether nanowire growth occurs by VLS or VSS mechanisms is determined by the appropriate temperature-composition phase diagram of the multicomponent catalyst-precursor system and by the growth conditions. The conditions for solidification from nanoscopic liquid droplets, for example, are also influenced by surface and interface energy terms. Such effects cause phase stability at the nanoscale to deviate from predictions made using bulk phase diagrams [70–73]. Among the advantages of choosing VSS conditions over VLS is that interfaces between regions of differing composition in the grown nanowires are sharper: precursor components are generally less soluble in a solid catalyst than in a liquid, a phenomenon known as a reduced reservoir effect [74,75].

The nature of the catalyst is not only key for the growth of nanowires but also for the functional properties of the grown structures. An incorporation ratio $\geq 10^{-7}$ for catalyst atoms in the nanowire can modify its semiconducting properties by introducing states within the band gap. When the energy of the introduced states is within a few meV of the valence or conduction band, the catalyst atoms act as parasitic dopants. As an example, Al, In, and Ga are incorporated in Si during VLS growth at levels often exceeding their equilibrium solubility [76–78]. Ga and Al are p-type dopants for silicon. This means that catalyzing nanowire growth of silicon using of these metals results in intrinsic p-doping. If the incorporation of the catalyst atoms is controlled by the growth conditions, this effect can also be used to modulate the local conductivity as has been done, for example, in the fabrication of nanowire-based radial p-n junctions for solar cell applications [79].

In most cases, impurities introduce defect levels deep in the semiconductor band gap, often near the middle of the band gap. This is the case for Au and Cu in silicon, well-known deep-level impurities [80]. Their impact depends on the solubility of the impurities at the growth temperature. It has been shown that Au can incorporate at concentrations up to $1.6 \times 10^{16}\ cm^{-3}$ in silicon, while Cu concentrations are much lower [81,82]. It has been argued that deep-level impurities may not dominate non-radiative recombination processes in very small-radius nanowires, in which surface states are likely to be dominant [83]. However, there are applications for semiconducting wires, such as in photovoltaics, in which diameters of 100's of nm to microns may be preferred [84]. In such cases, the tendency of deep-level impurities to promote non-radiative carrier recombination and pn junction leakage prompt interest in catalysts that do not contaminate the wires [85,86].

Contrary to Si and Ge, the potential contamination of III-V nanowires with Au has been much more controversial. While some studies have demonstrated the incorporation of Au atoms during VLS growth in the nanowire stacking faults [87], the real impact on the optical properties is to date still not completely clear. In fact, reports on short and long recombination rates in Au-catalyzed III-V nanowires have been reported, suggesting that growth conditions play an important role [88,89]. While incorporation of Au during VLS growth of III-V nanowires may be too small to be significant, one should consider also possible incorporation during subsequent semiconductor shell growth in radial heterostructures. While MBE tends to use lower temperatures for the shell growth than axial nanowire growth [90], MOCVD typically employs much higher temperatures to enhance the uncatalyzed decomposition rate of the precursors [91]. The use of a higher temperature for shell growth results in the diffusion of Au in the nanowire [92]. Temperature and/or duration should be optimized to avoid such parasitic contamination.

If one considers solely growth aspects, Au is an ideal catalyst; it does not easily oxidize when exposed to air, and it works as a VLS/VSS-catalyst for a broad range of materials systems [93]. The excellent properties of Au for nanowire growth justifies its widespread use. As described above, Au introduces deep-level traps in silicon and germanium, rendering Au-decorated substrates incompatible with complementary metal oxide semiconductor (CMOS) fabrication lines even if Au catalysts do not produce detrimental effects on the nanowires themselves during low-temperature wire growth. For this reason, scientists have looked

for alternative catalysts both for group IV and III-Vs. Avoidance of Au in VLS and VSS growth is a challenging task, both in group IV and III-V semiconductors, although there are selective chemical etches for postgrowth Au tip removal from some nanowire materials [94,95].

The Nebol'sin-Shchetinin criterion has also been extensively used for the selection of metals as catalysts as the surface energy of the metal determines if there is a contact angle at which the droplet is stable on the nanowire top. This relation predicts that Au and Ni should work very well for VLS growth, while metals with low surface energies such as Sn, In, and Bi should not work for VLS growth. Now, while it is correct that VLS growth is more challenging for low surface energy metals, experimental results show that it is possible (see references below). Schmidt et al. classified the catalysts for Si nanowire growth according to their phase diagrams, which relate directly to the conditions needed for nanowire growth [29]. Depending on whether the catalyst-Si phase diagram presents a single eutectic point at high or low Si concentration, catalysts were named type A or B, respectively. Type C catalysts are those presenting metal silicide compound phases. This classification works less well for III-Vs as at least two elements of which the semiconductor wire is composed should be considered. Among the catalyst metals other than Au investigated for either VSS or VLS growth of group IV nanowires are Al [28,96], Pd [97], Cu [98–101], Ti [102,103], Mn [104,105], Ni [106,107] In Refs. [108,109], Ga [110], Sn [111], and Bi [112].

In III-V nanowires, the most common strategy for avoiding Au during nanowire growth has been the use of self-assisted or catalyst-free methods. Catalyst-free methods employ crystal growth rate anisotropy to drive preferential one-dimensional growth. Critical to this method is the nucleation of nanoscale islands the initiate the growth. This can be achieved by employing lattice mismatched substrates and is known as VS growth [113,114]. Alternatively, it can be obtained by covering the substrate with a mask containing nanoscale apertures, a method known as selective-area-epitaxy (SAE) [115]. Both VS and SAE have been successfully applied to III-V compounds InAs [116,117], InP [118], InGaAs [119,120], GaAs [121,122], InGaN, and GaN [123,124]. Self-assisted nanowire growth corresponds to the VLS mechanism in which the primary constituent of the liquid droplet is itself a component of the semiconductor nanowire. The best known example is gallium used to catalyze GaAs nanowire growth, also known as Ga-assisted growth [125], although it has also been applied to In-assisted growth of InAs [126] and InP [127]. One should note that both SAE and self-assisted growth present challenges for achieving sharp variations in the composition along the nanowire axis (see Section 5).

In the quest to achieve VLS in a non-self-catalyzed manner, Hallberg et al. and Sun et al. have performed pioneering work on alternative metals for the growth of III-arsenide and III-phosphide nanowires. For example, Pd- and Sn-catalyzed GaAs [128,129] and Cu-catalyzed InP [130,131] nanowire growth has recently been demonstrated. This area of research is still in its relatively early stages; high quality nanowires are still challenging to grow with catalyst metals other than Au.

3. Wire dimensional control and roughness

The growth and etching paradigms for nanowire synthesis both suffer from challenges associated with wire diameter control. Current technology allows for the definition of catalyst seeds and etching masks of few nanometers' diameter. In principle, these features should be translated to a similar nanowire size. In practice, however, both systematic changes in diameter with length (taper) and local diameter fluctuations (random or non-random) are often observed. A mechanistic understanding of the growth or etching processes used to define the wire shape can be invaluable in finding conditions that avoid such diameter variations.

3.1. *Minimum nanowire diameter*

The minimum feature size that can be patterned and etched in either a catalyst particle (for grown wires) or in the nanowire material itself (etched wires) may be considered a practical lower limit for the diameter of nanowires and their pitch fabricated in an ordered array. For optical or e-beam lithography, this will depend on the exposure tool and the resist chemistry used in patterning, but minimum feature sizes can be less than 10 nm for dense patterns [132]. However, there are complicating factors for grown nanowires. In VLS growth, an initial catalyst nanoparticle will melt and often expand as it becomes saturated with the nanowire component(s) before wire nucleation and growth. This can cause the grown nanowire diameter to exceed the initial catalyst particle size [133,134]. Moreover, the Gibbs-Thomson effect [135,136] raises the free energy of nanoscale structures relative to bulk crystals of the same material. To nucleate a wire or to achieve a satisfactory growth rate, decreasing the wire diameter (and thus increasing the relative effect of sidewall surface energy [137–140]) may require an increase in the chemical potential (e.g. precursor partial pressure) of the nanowire components in the vapor phase [141,142]. For the smallest diameter nanowires ($<<$ 10 nm), such high precursor activities may not be practical for some deposition systems, or they may lead to a loss in selectivity of deposition at the catalysts versus on the wire sidewalls and on surrounding regions of the substrate. The smallest diameter obtained for self-catalyzed growth is also around 10 nm and can only be obtained for a contact angle around 90° which does not foster diameter increase [143]. For both etched and grown nanowires, however, further reduction in diameter is possible by subsequent radial trimming [144]. For example, silicon wires can have their diameters reduced by cyclic oxidation and oxide etching after growth [145]. In an alternative manner, ultrathin GaAs nanowires were demonstrated by congruent evaporation from the side facets [146].

3.2. *Tapering during nanowire growth and etching*

The diameter of a nanowire can vary during growth, resulting in inclined side walls. Tapering can be the consequence of the value of the contact-angle favoring inclined facets [59,125] or of the variation of the volume of the metal catalyst during growth [143]. Tapering of a nanowire is represented by the angle θ in Fig. 3(a), which is related to the change in wire diameter as a function of position along the wire axis from the catalyst tip. For example, in silicon nanowire growth, the diameter can be varied by appropriate choice of wire growth conditions. In a binary eutectic VLS system such as Au–Si, increasing the growth temperature will increase the liquidus composition associated with the semiconductor component and thus increase the supersaturated liquid droplet size for a given initial quantity of catalyst metal [73]. Alternatively and in other material systems, changing the precursor partial pressures in the growth chamber can alter the supersaturation of the semiconductor components in the liquid droplet and thus transiently change the droplet contact angle and nanowire diameter [64].

Another common source of sidewall tapering in grown nanowires is uncatalyzed deposition of vapor-phase components onto the wire sidewalls at a rate that is not insignificant compared with the rate of catalyzed deposition at the tip [147]. The tapering angle can be related to the ratio of the sidewall and axial growth velocities of the nanowire,

$$\tan(\theta) = \left(\frac{v_r}{v_z}\right) \quad \text{(P2)}$$

where v_r is the effective radial growth velocity due to sidewall deposition, normal to the nanowire long axis, and v_z is the axial growth velocity. Because the catalyst in either VSS or VLS growth reduces the activation enthalpy for deposition from the vapor phase compared with uncatalyzed film growth, decreasing the temperature increases the ratio of v_z to v_r, thus suppressing nanowire taper [148]. Another interesting example of the effect of the deposition temperature on wire taper is provided by the Au—Ge VLS growth process, in which steady-state germanium VLS growth at subeutectic temperatures is possible [70,149]. After nucleating and initiating VLS growth of Ge nanowires at temperatures slightly above the bulk Au—Ge eutectic, subsequent cooling to subeutectic temperatures can be used to produce single crystal wires with nearly parallel sidewalls having taper angle $\vartheta \cong 0$. This occurs because (1) sidewall deposition is kinetically inhibited at such low temperatures compared with Ge deposition onto the nanowire tip through the catalyst and (2) the catalyst diameter remains stable.

The deposition condition-dependent taper of silicon nanowires grown in a gold-mediated VLS process using a $SiCl_4/H_2/N_2$ gas mixture has also been reported [150]. In this case, the authors detected a pronounced effect of the $SiCl_4$:H_2 partial pressure ratio in their CVD reactor on silicon sidewall deposition at 850°C, a temperature far above the Au-Si eutectic (Fig. 4). Tapered Si NW growth by sidewall reaction of SiH_4(g) precursors has also been discussed in several prior reports e.g. Refs. [151,152, 153].

In addition, tapering may result from progressive loss of the catalyst material, either from surface diffusion along the nanowire sidewalls, gradual dissolution in the nanowire bulk, or, possibly, evaporation at the growth temperature and pressure [154,155].

Etching of semiconductor nanowires can be performed in either horizontal or vertical wire geometries. For example, horizontal silicon NWs have been fabricated in either silicon-on-insulator or bulk silicon substrates using process flows that include fin patterning, etching, and lateral size reduction (e.g. by oxidation and oxide wet etching) [156—158]. Vertical nanowire arrays (nanopillars) can be produced by deep reactive ion etching through photoresist (PR) masks or patterned hard masks [159,160] or by nanoimprint lithography [161]. For the vertical geometry, taper can be a significant problem because of etching of already-exposed sidewalls during the deep etching of the substrate. This effect can be reduced by simultaneous deposition of a protective layer on the sidewalls during etching, as occurs in the Bosch process [162] for silicon [163].

In addition to taper, a more general issue in nanostructure etching is line edge roughness (LER), which results from the compounding effects of variations in local resist exposure and local etch rates on pattern definition. Fig. 5(a) is a representative plan view SEM image of LER for an etched horizontal silicon nanowire of 40 nm nominal diameter fabricated by e-beam lithography and self-limiting oxidation for shape control [164]. Fig. 5(b) shows the nanowire edge as defined by threshold grey scale analysis of the image. The plot in Fig. 5(c) compares the autocorrelation of the left edge in Fig. 5(b) with the Gaussian function shown in the inset legend of Fig. 5(c), where L is the roughness correlation length. The extracted correlation length and root mean square roughness amplitude, D, for this nanowire are listed in the legend of Fig. 5(c). Increasing D is expected to increase the variation of threshold voltage and decrease the ratio of on-state to off-state current of transistors fabricated on nanowires. In contrast, 3D simulations indicate that transistor performance is largely unaffected by L until the correlation length decreases to values less than the gate length of the device [164].

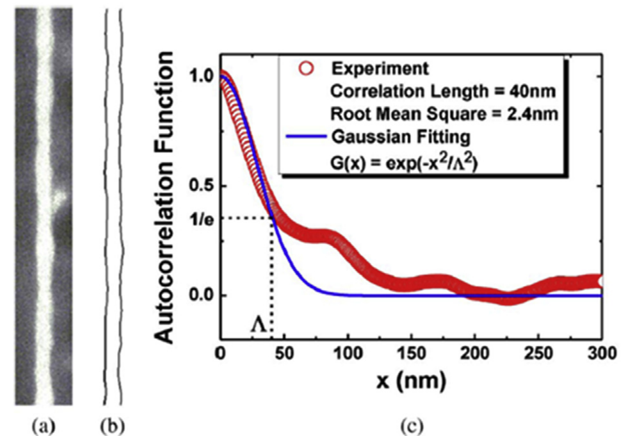

Fig. 5. (a) Top-view SEM image of 40 nm nanowire with (b) edges detected; (c) autocorrelation function of the left edge fits well with Gaussian function [164].

3.3. Sidewall roughness

With their high surface-to-volume ratio, the nature of the sidewalls plays a significant role in the functional properties of nanowires. Compared with the characteristic facet structures of grown nanowires [Section 1.2], sidewalls produced by semiconductor dry-etching processes generally exhibit less ordered and periodic roughness because the higher pressures and lower temperatures typical of these etch processes tend to inhibit atom surface mobility.

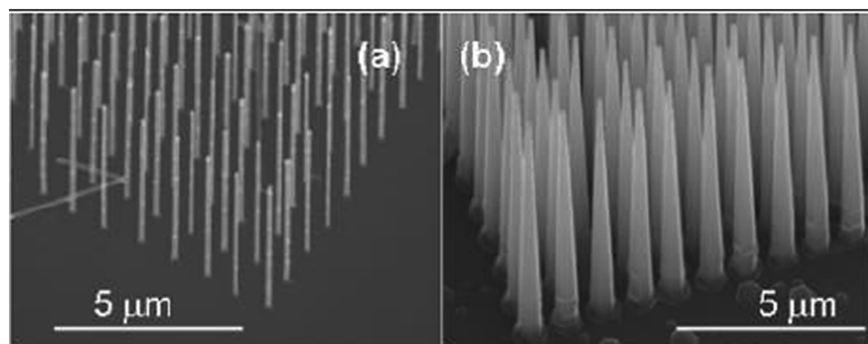

Fig. 4. Silicon nanowires produced using gas phase compositions. (a) X ($SiCl_4$)/X (H_2) = 0.03/0.2 at 600 Torr total pressure for 5 min and (b) X ($SiCl_4$)/X (H_2) = 0.01/0.1 at 300 Torr for 15 min. Array of Au catalyst dots (100 nm diameter, 75 nm thick) patterned by e-beam lithography. T = 850°C, from ref. [150].

As in the case of crystal growth, however, anisotropic etching processes can promote the reduction of surface free energy during etching by causing the surfaces of crystalline nanostructures to become delimited by facet planes. Crystallographic planes with low surface energy tend to exhibit relatively slow etch rates that leave them as the bounding surfaces of nanocrystals. From the point of view of applications, achieving a well-defined surface facet structure is often an important goal. The density of semiconductor interface states depends on crystallographic orientation [165], so preparing structures with facets that have low densities of dangling bonds is desirable. In addition, the functional properties of semiconductors are orientation dependent. For example, the sub-band structure of electron energy bands of semiconductors is anisotropic. This causes the effective masses of electrons and holes in a surface channel device to depend on the channel's crystallographic orientation. Finally, surface roughness is an important source of carrier scattering; achieving flat sidewall facets is key in many applications [166–169]. For all of these reasons, the surface facet structure can determine device performance.

In the case of anisotropic etching, the etch chemistry often contains species that can either react with the solid or, by adsorbing on its surface, protect it from further etching. The relative etch rates of different crystalline planes will depend on the rates of the etching reaction versus protective species adsorption. One such example is shown in Fig. 6 [170], in which a sulfur-oleylamine (S-OA) liquid solution is used in anisotropic etching of an InP single crystal substrate. Oleylamine ($C_{18}H_{37}N$) is a surfactant. It can react with S to form H_2S, which will etch InP. By controlling the S-OA composition and temperature, relatively slow, layer-by-layer, etching of InP is achieved [171]. A circular hole initially patterned into the InP (100) crystal by e-beam lithography develops preferred {011} sidewall facets Fig. 6(a and b). Alternatively, a circular InP island with sloped sidewalls develops a faceted appearance after S–O etching Fig. 6(c and d). As reported by Walavalkar et al. [159], this wet etch chemistry does not significantly reduce the photoluminescence (PL) yield measured from patterned and etched InP nanopillars, whereas a Cl_2 and CH_4-based dry etch process greatly suppresses PL, indicating increased non-radiative recombination because of surface defects. Additionally, the presence of sulphur in the S-OA etch was found to have a passivating effect on surface dangling bonds for etched GaAs nanopillars. More recently, metal-assisted chemical (wet) etching of InP nanopillars has also been reported to achieve well-controlled anisotropic etching without a measured increase in the density of surface electronic carrier traps [172].

Atomic layer etching (ALEt) has attracted attention as a method for top-down nanostructure formation that is compatible with semiconductor nanowire device fabrication [173]. One class of ALEt processes is illustrated schematically in Fig. 7, in which a self-limiting surface reaction modifies the surface monolayer of a substrate, and this modified layer is then removed chemically by reaction with ligands that produce volatile molecular species. Removal of the modified surface layer by ion or neutral species bombardment is also possible, although this may induce significant damage of the underlying semiconductor. The self-limiting and surface-saturating nature of the initial surface modification step in each cycle makes ALEt amenable to etching of complex, high aspect ratios features while minimizing LER.

3.4. Catalyst coarsening

The nanowire growth catalyst selection criteria summarized in Section 1 include very low bulk solubility of catalyst components in the semiconductor crystal. However, even when this criterion is satisfied, adsorption of the catalyst onto the surface of either the nanowires or their substrate can have a profound impact on the fidelity of nanowire diameter and orientation control during growth. In the case of silicon, surface diffusion of the Au catalysts most commonly used in VLS growth occurs readily, in some cases, forming specific surface reconstructions that depend on the extent of Au surface coverage. Slezak et al. [174] measured a surface diffusivity of Au on the initially clean (111) Si surface of ~1×10^{-7} cm [2]/s at a temperature of 985 K in ultrahigh vacuum. The Au surface diffusivity is suppressed relative to this value by

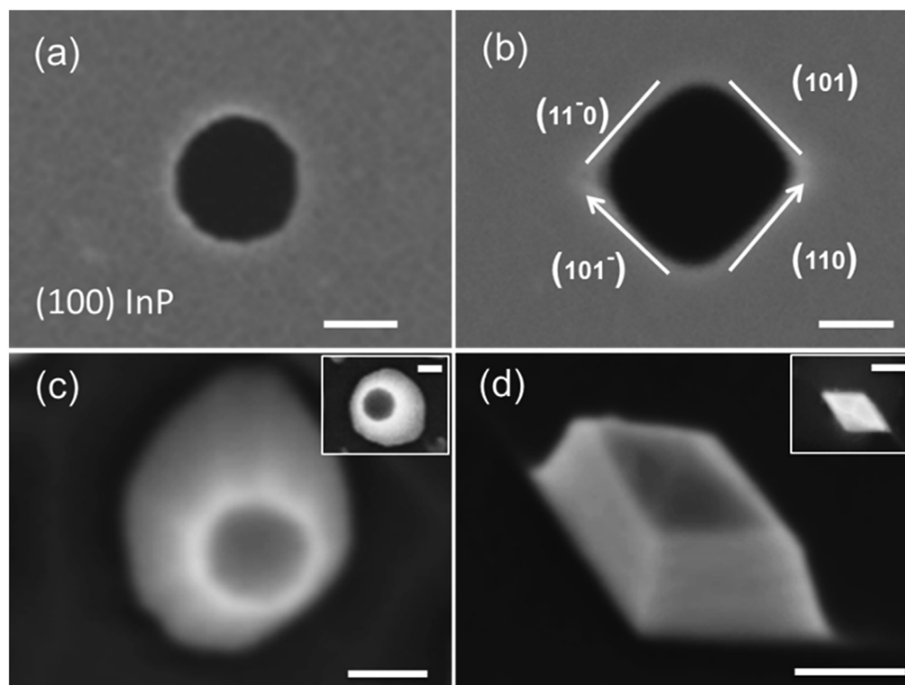

Fig. 6. Sulfur-oleylamine anisotropic wet etching of an InP film to produce (a) and (b) faceted holes and (c) and (d) tapered mesas [170].

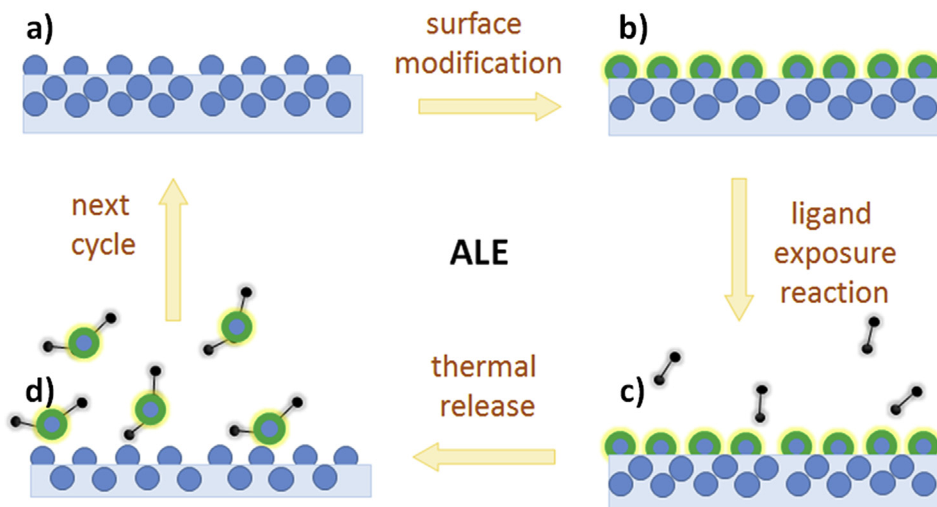

Fig. 7. Cyclic atomic layer etching (ALE) processing including (a) and (b) self-limiting surface reaction to form a modified surface monolayer, and (c) and (d) removal of the modified surface layer by exposure to ligands that form volatile product molecules. Adapted from Ref. [173].

lowering the temperature and by increasing the pressure to the mTorr – Torr pressure range typical of LPCVD growth [175,176].

Catalyst diffusion on the surface of the substrate before nucleation of nanowires during the early stages of either VLS or VSS growth will promote coarsening of the catalyst particles, thus broadening the distribution of the final wire diameter compared with the initial distribution of catalyst size. This effect was illustrated clearly by Koto et al. [177] who used nanoporous Si (111) substrates to effectively increase the diffusional path length between colloidal Au nanoparticle catalysts deposited on the surface of the wafer, thus reducing the extent of coarsening. Postgrowth cross-sectional transmission electron microscopy (TEM) (Fig. 8) and secondary ion mass spectrometry (SIMS) analysis revealed diffusion of Au into the H-terminated pore channels of the Si substrate to depths far greater than the average lateral catalyst separation on the substrate surface.

Inhibition of catalyst atom surface diffusion is a more easily generalized approach to achieve high areal densities of grown semiconductor nanowires on a substrate while avoiding catalyst coarsening. In addition to adjusting growth conditions to encourage diffusion-suppressing surface adsorption of species from the vapor phase, coating the substrate surface in between catalyst nanoparticles with a layer that inhibits surface diffusion can be effective. For the Au–Si system, Au adsorbs in a highly selective fashion on Si surfaces compared with SiO_2 [178]. This indicates the potential for oxide and other surface mask layers between catalysts to suppress the coarsening phenomenon and thus promote diameter control of grown Si nanowires.

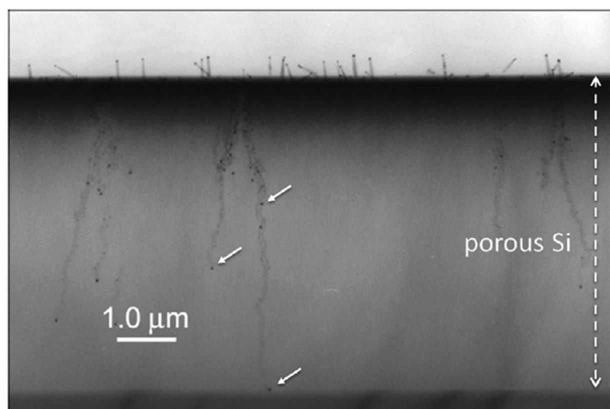

Fig. 8. Cross-sectional TEM image showing details of pore channels in porous Si(111) substrate after Ge nanowire nucleation and growth. Local Au decoration (dark-contrast particles, several marked by arrows) and pore channel surface coating by germanium [177].

Catalyst atomic diffusion along sidewall surfaces during nanowire growth has also been noted [179]. In the case of the Au–Si VLS system, Au atomic clusters are frequently observed on the sidewalls of growing Si nanowires [175,179]. Under conditions, such as low pressures, that promote fast Au surface diffusion on Si, coarsening of the Au–Si liquid droplets during nanowire growth is reported [176]. This leads to tapering of wires with smaller droplets at their tips because these droplets continue to shrink as growth proceeds. Simultaneously, a number of wires will exhibit inverse tapering (increasing wire diameter as they grown longer) because their, larger, catalyst droplets continuously grow via coarsening.

3.5. Length limits

The minimum length of a VLS- or VSS-grown nanowire is similar to the catalyst diameter; although, in initial growth orthogonal to a substrate surface, the wire cross-section is generally tapered as a result of the change in wetting conditions as the catalyst (either solid or liquid) lifts away from the substrate [28,61]. Growth of several catalyst diameter's length is typically necessary to achieve a constant wire diameter. For top-down fabricated nanowires, the minimum length will be set by the minimum feature size for the patterning method used (horizontal wires), or the wire length may be determined by thickness of the film from which the nanowires are etched (vertical wires).

Sidewall taper (Fig. 4) and pattern collapse during postetch cleaning can result in a practical upper limit to the length of patterned and etched nanowires, although wires 10's of µm in length have been reported [180] for metal assisted etching of silicon nanowires. A maximum length limit for grown nanowires may occur if catalyst is lost, for example via sidewall diffusion or dissolution into the wire, during growth. Once the catalyst is completely lost or is too small to sustain growth under the chosen deposition conditions, wire elongation will cease. Similarly, gradual poisoning of the catalyst surface by adsorption of impurities in the

vapor phase may cause a cessation of growth. Alternatively, for a growth mechanism that requires reactant species surface diffusion to the wire tip [181,182], the growth may slow significantly after sufficiently long wires are grown. The longest bottom-up III-V nanowires have been obtained by hydride-vapor phase deposition, reaching lengths of 100's of microns [183,184].

4. Nanowire placement and axial alignment

4.1. Bottom-up placement and alignment methods

Techniques for placement and alignment of nanowires on substrate surfaces can be categorized as 'bottom-up', 'top-down', or hybrid. Bottom-up approaches do not use lithographic patterning to define the location and orientation of nanowires on a surface but instead make use of templating or various physical forces that can act on nanowires to control their morphology.

The simplest templating approach, which does not result in control of wire location on a surface but does control the growth alignment relative to that surface, is epitaxy. Deposition of catalyst nanoparticles on a single crystal substrate or their formation by thermal dewetting of a thin film of a catalyst metal before nanowire growth will, in general, result in a random areal distribution of seeds for nanowire growth. If the single crystal substrate shares an orientation relationship (lattice matching) with the crystal structure of the growing nanowires, one or more preferred orientation relationships will exist between the nanowires and substrate. An example is the growth of diamond cubic semiconductor nanowires on (111) Si substrates, which occurs vertically, with a [111] nanowire axis parallel to the [111] surface normal of the substrate. If kinking occurs during [111] wire growth [185–188], the growth axis may switch to become coincident with one of three directions parallel to the substrate's <111> axes which are inclined to the surface normal [189].

In addition, templated nanowire growth can occur through holes formed in an inert mask layer on a substrate. An example of this method for bottom-up wire placement and alignment is growth of single crystal nanowires in the pore channels that form in anodized aluminum oxide (AAO) [190,191]. This templating process achieves a degree of positional and alignment control of the wires, as the vertical pores can assemble into a hexagonal array during anodization of aluminum [191]. If the AAO template layer is formed on a single crystal substrate, epitaxy can dictate the crystallographic orientation of the resulting vertical nanowires as well. The combination of epitaxy and an alternative mechanism for defining wire axial alignment relative to the substrate surface permits formation of vertical nanowires with orientations that cannot usually be achieved by epitaxial growth of free-standing wires, such as vertical [001] Si nanowires grown on a Si (001) substrate [190]. Arrays of reasonably well-ordered vertical nanowires can also be fabricated using polystyrene sphere templates. A two dimensional array of polystyrene spheres are used as a shadow mask to pattern an underlying catalyst layer for subsequent nanowire growth [192]. Gold-catalyzed VLS growth of vertical Si nanowire arrays is shown in Fig. 9.

Bottom-up assembly of horizontal nanowires into axially aligned assemblies suitable for device applications can be achieved using the Langmuir-Blodgett (LB) technique [193] to uniaxially compress a monolayer of nanowires and surfactant in a layer of non-polar solvent present on a film of water. This layer can then be transferred to a substrate of interest [194,195]. By controlling the compression process in the LB trough, the average lateral spacing of the wires can be controlled for spacings greater than a critical value (typically, 100's of nm) at which strong attractive forces cause nanowire aggregation. The alignment and transfer steps can be repeated with controlled orientation to produce crossed and more complex NW structures [194]. In addition to the LB approach, bottom-up placement of nanowires using methods such as controlled solvent evaporation [196,197] and contact printing [198,199] has been reported. Although these methods can control the local areal density of nanowires on a surface and, in some cases, achieve reasonably parallel axial alignment, they do not allow for the precise positional control required to make individually addressable nanowire devices at high densities.

4.2. Orientation control and substrate effects for grown nanowires

A significant advantage of semiconductor nanowire growth compared with etching-based methods is substrate flexibility. Reproducible preparation of single crystal nanowires by patterning and etching requires a single crystal substrate, from which the wires are etched. Locally catalyzed growth of nanowires can occur even on amorphous substrates [200,201], as a wire's crystallinity is typically defined by a single nucleation event that occurs at the catalyst/substrate interface. Different substrates will exhibit different wetting characteristics of the nanoscale catalyst. Compared with a crystalline substrate, an amorphous surface affects the initial wire shape during catalyzed growth, and it also changes the energy barrier for nucleation of the nanowire crystal, but it generally will not produce a polycrystalline wire. Moreover, the crystallographic orientation and the axial alignment of etched nanowires are necessarily related, whereas they can be decoupled for grown nanowires. A single crystal nanowire prepared by locally catalyzed growth will have a crystallographic orientation that is typically determined by the balance of sidewall facet surface energies and the catalyst/nanowire interface energy, independent of the substrate. Growth on amorphous or non-lattice matched substrates does not usually produce nanowire arrays with significant axial alignment, but this may not be a requirement for many applications.

In metal-catalyzed III-V nanowire growth, the substrate surface polarity also plays an important role in controlling crystallographic orientation. In homoepitaxial wire growth on the polar GaAs (111) plane, vertical epitaxial growth of [111]B-oriented GaAs nanowires is strongly preferred on (111)B (As-terminated) substrates, whereas both vertical [111]A-oriented and inclined [111]B-oriented wires have been observed on Ga-terminated, (111)A substrates [202,203]. For Au-catalyzed VLS growth of GaAs nanowires, inclined wire nucleation on (111)A substrates can be suppressed by addition of Sb to the sample surface immediately before nucleation [68]. This may be correlated with an increase of the wetting angle of the catalyst droplet on the (111)A surface. A wider range of off-vertical orientations are possible for self-catalyzed growth of polar III-V nanowires (e.g. Ga-catalyzed growth of GaAs wires) on non-polar (e.g. Si or Ge) substrates. Multiple rotational twinning (Fig. 10) of the individual nuclei from which nanowires grow can occur. [204,205] These twinned nuclei produce a wide variety of angles of inclination with respect to the substrate surface normal. Also in this case, it has been shown that the wetting properties of the metal droplets on the substrate can influence the degree of 3D twinning [206,207].

An interesting example of substrate crystallography influencing nanowire growth orientation is provided by guided VLS growth of nanowires along surface ledges on vicinally cut single crystal surfaces. [208,209]· This growth process is related to graphoepitaxy [210], in which substrate features, and not necessarily atomic-scale epitaxial templating, guides the orientation selection of deposited crystals. In the case of guided VLS growth, substrate surface features direct the 'crawling' motion [211] of the liquid catalyst droplet by processes such as local capillary pinning. Tsivion et al. [208,209] demonstrated growth of well-aligned GaN nanowires over

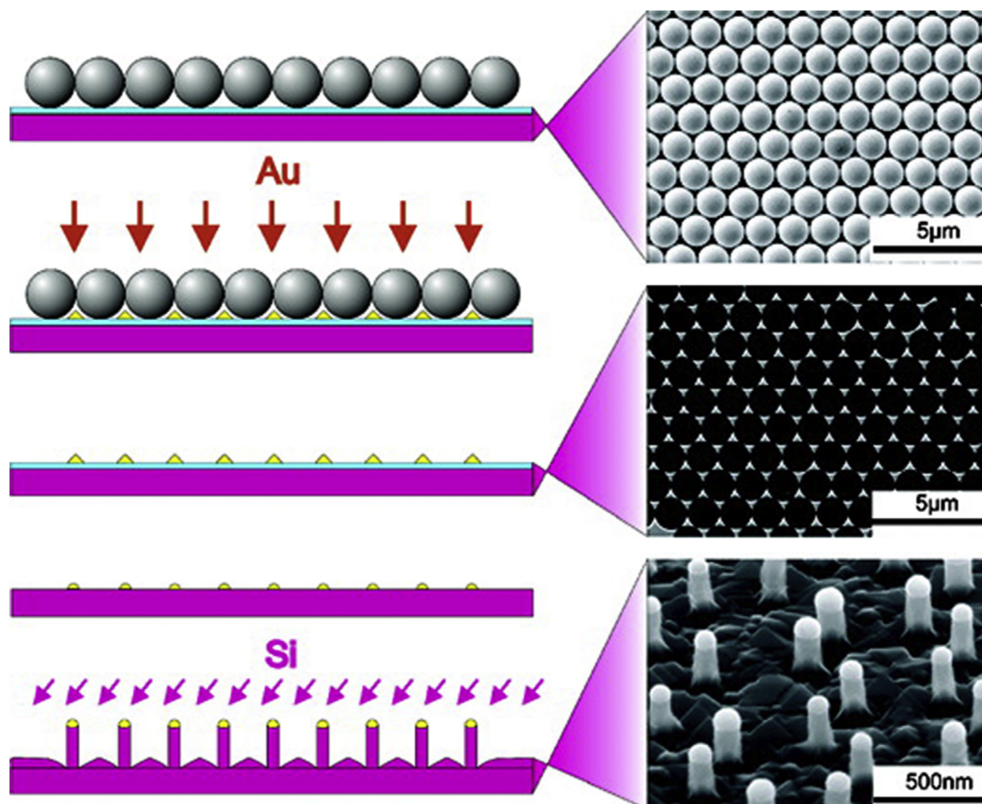

Fig. 9. Nanosphere lithography to prepare ordered vertical Si <111> nanowires using Au-catalyzed VLS growth [192]. VLS, vapor-liquid-solid.

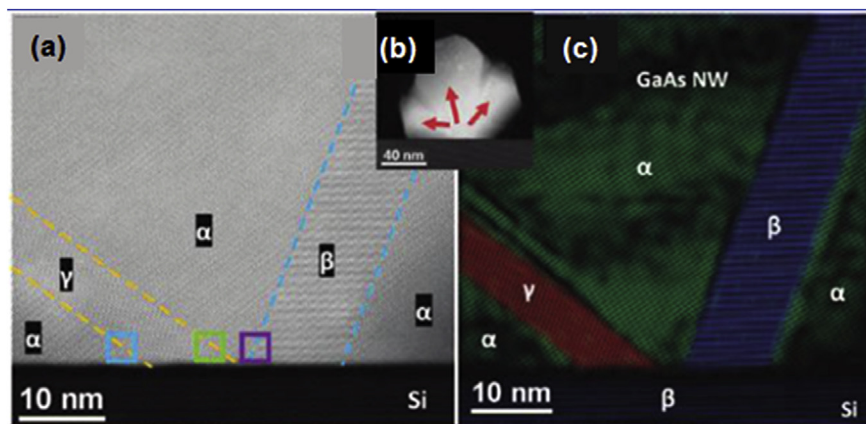

Fig. 10. (a) Atomic high-angle annular dark field scanning transmission electron micrograph of the initial stages of GaAs nanowire growth exhibiting a multiple crystalline seed structure. (b) Low magnification TEM image of the sample, showing the three nanowire growth directions. (c) Visualization of the different crystal orientations [204].

millimeters of length when they were aligned parallel to surface steps produced by intentional vicinal miscutting of sapphire substrates. This approach was later extended to fabrication of 2-D nanowire ZnO transistor arrays and simple circuits [212]. Fortuna et al. reported aligned <110> GaAs surface nanowire VLS growth on GaAs (111) substrates [209]. Although the reason for the parallel alignment of the nanowires was not explained in a study published by Fortuna et al. [209], a subsequent report from the same group suggested that miscut of the GaAs wafer may play a role in the observed surface nanowire growth [213].

Kinking of nanowires (Fig. 11), a sudden change in their crystallographic orientation during growth, can be caused by intentional rapid changes of growth conditions [186,214,215] or composition [187], or by stochastic processes that influence the balance between the surface energies of the sidewalls and the interface energy of the catalyst/nanowire growth facet [187,216]. In many cases, kinking involves dropping of the metal catalyst [217], formation of a crystallographic defect, often a twin boundary, such as in cases where kinking of a silicon nanowire involves segments with <112> axial orientation [214,217], or in kinking of a non-centrosymmetric crystal nanowire during growth along a polar axis [218]. However, coherent kinking, in which no defect is present in the kink vicinity of a nanowire, also occurs [187]. Coherent kinking is observed in Ge nanowires of a diameter close to the value at which <111>−oriented and <110>-oriented VLS growth are almost equally favored by the balance of surface/interface energies

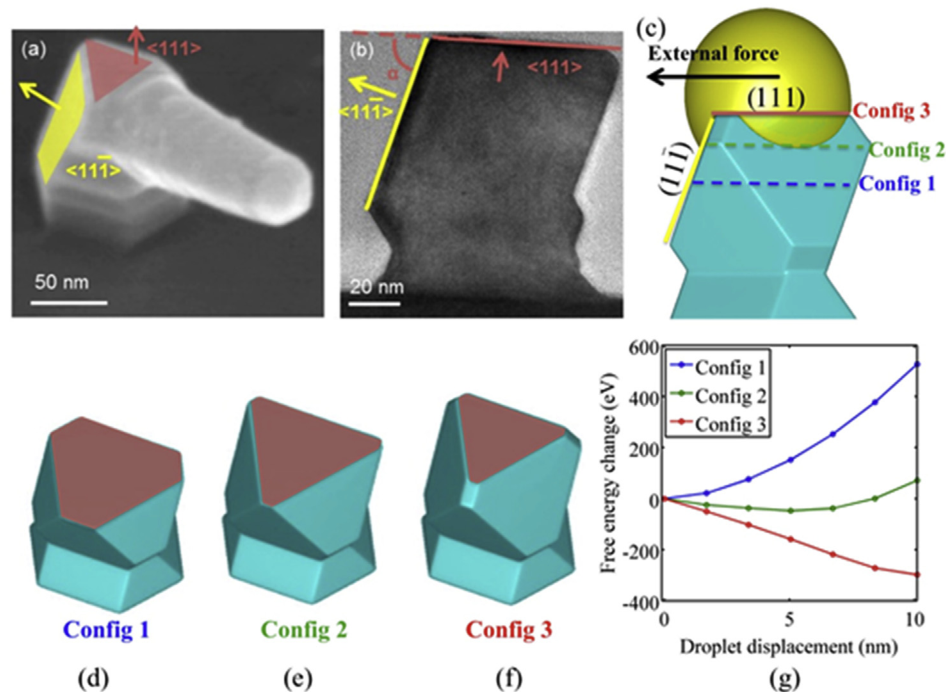

Fig. 11. Vertical [111] to inclined <111> Ge nanowire kinking. (a) Kinked NW with triangular top surface and large (111) sidewall facets; (b) TEM image showing top and sidewall (111) facets and taper angle α. (c) A side view of the nanowire pedestal created by a 3D phase field model based on the experimental image. (d), (e), and (f) show 3D views of the base structures at different NW height. (g) Predicted free energy change as a function of the droplet horizontal displacement [188].

[35,218,219]. In contrast, coherent kinking from an initially vertical [111] orientation to an inclined <111> axis occurs in the very early growth stage because of an error in sidewall facet development (Fig. 11) as the wire cross-section area is rapidly reduced, while the catalyst droplet 'lifts off' the substrate surface. [58,219], Surface adsorbates, which alter nanowire sidewall energies, can promote kinking, as observed for the case of Au sidewall wetting during VLS growth of Si nanowires [179]. Filler et al. have shown that intentional kinking of Si nanowires [215] and subeutectic VLS growth of Ge nanowires [220], in both cases using Au catalysts, are strongly influenced by hydrogen adsorption on the wire sidewalls.

A very low probability of kinking is required to achieve high fidelity nanowire device fabrication via local crystal growth. The kinking probability can be reduced by controlling growth temperature [188,218], adsorption of surfactant species on the nanowire sidewalls [215], and addition of alloying components to the catalyst [218] to adjust sidewall surface energies, the catalyst/nanowire interface energy, and the effective mobility of the catalyst on the wire surface. These approaches inhibit unpinning of the catalyst from the nanowire growth facet by either thermodynamic or kinetic means.

4.3. Top-down patterning of nanowires

Lithographic patterning combined with etching is a widely used approach for top-down fabrication of semiconductor devices and has been adapted to the preparation of nanowires. State-of-the-art optical lithography uses 193 nm deep ultraviolet illumination passing through a patterned metal mask layer to expose PR, thus controlling the resist's local solubility in a developer solution. Resist removal in the developer produces a pattern that can be transferred to the underlying substrate by etching. The smallest critical dimension (CD) of features that can be written in PR depends linearly on the wavelength of the incident light and inversely on the refractive index of the medium separating the PR surface from the final projection lens of the lithography system. Therefore, to make truly nanoscale devices, there has been a general trend over time of decreasing emission wavelength of the light sources used in optical lithography and the adoption of immersion lithography in which a liquid medium with refractive index > 1 is placed between the lens and PR-coated substrate [221]. Further advances have included the lateral trimming of features written in the PR layer [222], double patterning [223], and use of phase shift masks [224]. Combining these methods permits fabrication of nanostructures with CD approaching 10 nm using a deep UV light source (Fig. 12) [158].

Other routes to achieve definition of such small-diameter features include [225–227] extreme UV (EUV, 13.5 nm wavelength) and X-ray (<1 nm wavelength) lithography and electron beam lithography.

All such alternative exposure sources suffer from various technical and economic challenges which have, to date, limited their deployment in manufacturing, although electron beam lithography has been widely used in laboratory-scale studies involving nanowire device fabrication, primarily for defining metal contacts on arbitrarily positioned grown wires that have been transferred to a substrate surface. State-of-the-art semiconductor device fabrication facilities are now being equipped with EUV lithography to continue downward scaling of the most critical device dimensions beyond the minimum sizes that can be patterned with a deep UV light source.

Nanoimprint lithography, in which an imprint mold having nanoscale features patterns a curable polymer layer on a substrate, can be used for direct patterning of both horizontal [228] and vertical [229] nanowire arrays. The imprint mold is itself patterned by methods that produce well-defined, typically ordered, topographical features at very small dimensions. These may include superlattice nanowire pattern transfer [230] or UV interference lithography [231]. Reactive ion etching of the substrate surface masked by the imprinted polymer layer transfers the pattern into the substrate surface. If a high quality imprint mask is used, this

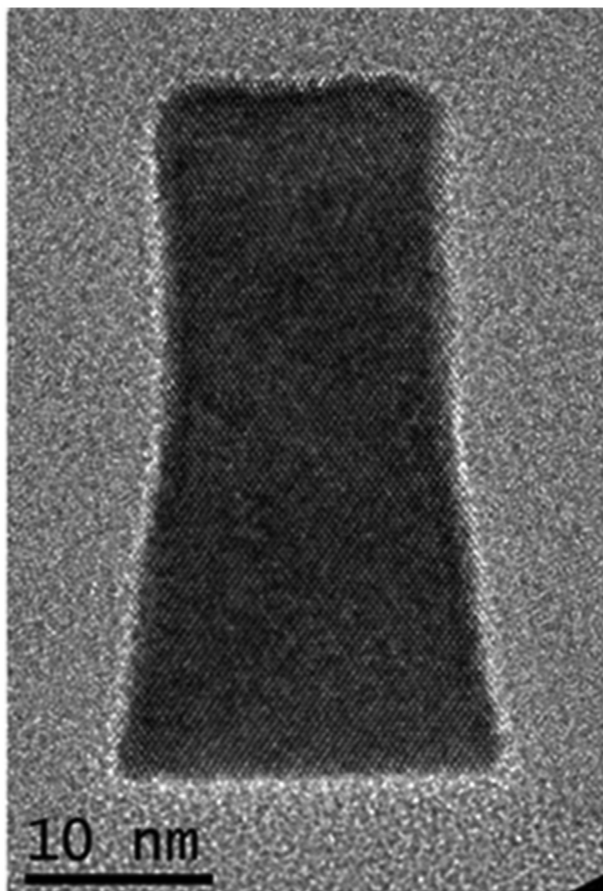

Fig. 12. TEM cross-section of dry etched silicon fin patterned by 193 nm deep UV immersion lithography [158].

method can achieve excellent pattern transfer for horizontal wires with half-pitch < 20 nm and feature size <40 nm, although the LER and defectivity of the resulting wires will be dictated by the quality of the reactive ion etching (RIE) process and subsequent surface treatment steps.

The complexity of top-down semiconductor nanowire fabrication increases significantly when the semiconductor of interest has a substantial lattice mismatch with silicon, the most common single crystal substrate material for integrated electronics applications and for microelectromechanical systems. Non-silicon (e.g. alloy or compound) semiconductor layers must first be deposited on the Si substrate up to the thickness required for either the intended length of vertical nanowires or the intended diameter of horizontal nanowires. For epilayers deposited directly on silicon, the misfit strain stored in these films will promote the formation of misfit dislocations when the lattice mismatch and thickness are such that it is energetically favorable to form such dislocations rather than to store the strain elastically [232]. Furthermore, misfit dislocations grow along the epilayer/substrate interface by propagation of threading dislocations through the bulk of the epilayer. Both interfacial misfit dislocations and bulk threading dislocation segments in partially relaxed epilayers may persist in the patterned and etched nanowires, acting as carrier recombination centers [233].

Residual strains present as a result of incomplete misfit strain relaxation of the epilayers will produce complex states of strain in top-down fabricated nanowires. For vertical nanowires, the misfit strain will be confined to a region a few nanowire diameters in height above the nanowire/substrate interface, as the remainder of the wire length is unconstrained by the substrate and can relax through radial and axial dilatation [234]. A similar situation will apply at the attached ends of free-standing horizontal nanowires; however, misfitting horizontal nanowires in contact with the substrate over their entire length will exhibit a graded strain profile in the orthogonal directions. Because strain can strongly influence the energies of conduction and valence band states and the effective masses of electrons and holes [235], such complex strain states in misfitting semiconductor nanowires must be controlled and quantified to determine their influence on device characteristics.

Dislocations and complex residual strains in top-down fabricated nanowires can be minimized by reducing the misfit strain of the semiconductor layer from which the nanowires are etched. Approaches for misfit strain reduction include epilayer growth on a buffer layer, such as a composition-graded Si–Ge alloy buffer layer [236], lateral overgrowth of the misfitting semiconductor film [237], or transfer (rather than epitaxial growth) of the semiconductor layer to another substrate [238,239].

4.4. Hybrid methods

Hybrid nanowire assembly combines top-down and bottom-up approaches in a complementary manner. Dielectrophoresis is one such hybrid method. Compared with microfluidic alignment or compression in a Langmuir Blodgett trough, greater alignment and spatial positioning control can be achieved using dielectrophoresis to move individual nanowires suspended in a liquid solvent layer onto electrode structures already fabricated on a substrate surface. This is, therefore, a hybrid approach in that it combines top-down patterning of the surface electrodes and field-driven placement of the wires. The dielectrophoretic forces that cause motion of nanowires result from their shape anisotropy and the fact that their dielectric constant is larger than that of the surrounding solvent [240]. Hybrid assembly of silicon nanowire arrays with high spatial fidelity has been demonstrated [241] on electrodes fabricated in a silicon microfluidic channel, which allows continuous flow of the nanowire suspension in an isopropyl alcohol/water solution. A critical voltage across adjacent electrodes is needed to pin a single nanowire across the electrode-electrode gap (Fig. 13), and a significantly larger pinning voltage is needed for a second wire to attach to the electrodes, thus achieving self-limiting assembly.

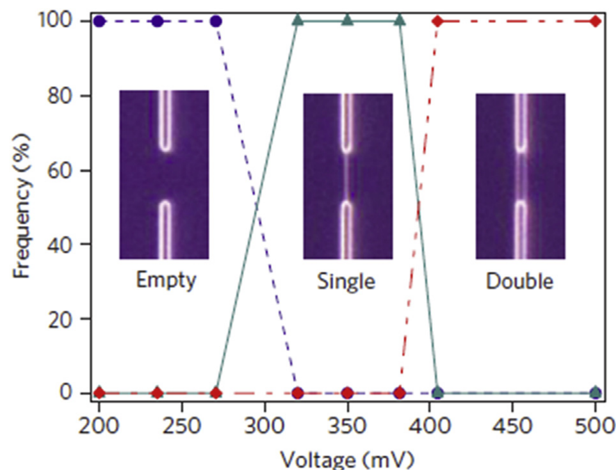

Fig. 13. Critical voltages for silicon nanowire dielectrophoretic assembly across an electrode gap [241]. Electrode dimensions: 12 μm gap and 2 μm width.

Hybrid fabrication of vertical nanowire arrays can also be achieved by combining LB assembly of a shadow mask such as polystyrene spheres to define deposited metal catalyst particles that are used in subsequent electroless etching of silicon [242]. Alternatively, self-assembled silica spheres can be used as an RIE etch mask [243].

Directed self-assembly or block copolymer lithographic patterning [244,245] is another hybrid method suitable for nanowire fabrication in which standard lithography and etching processes are used to produce substrate surface features that guide subsequent phase separation in an overlying block copolymer film. Phase separation of diblock copolymers (DBC's) produces various ordered structures (e.g. lamellae, cylinders, spheres) with the specific structure dictated by the relative fraction of the two blocks in the polymer and the geometric confinement or chemical environment of the polymer film [246,247]. A DBC film deposited in a patterned substrate channel of small dimensions can phase separate into a striped lamellar pattern of nanoscale periodicity. Selective chemical removal of one set of lamellae, those rich in a particular block, produces a very fine mask for subsequent etching of horizontal [248] or vertical [249] nanowires into the substrate surface. Because the mask period is set by phase separation rather than photon or electron stimulated chemical reactions in a resist, directed self-assembly has the potential to achieve smaller diameter nanowires than can single-step top-down methods. Block copolymer lithography has been used to prepare parallel horizontal silicon nanowire arrays with CD less than 20 nm and ~40 nm pitch on a silicon-on-insulator wafer [250]. In addition to local variations in etching rate, which is an issue for all etch-based wire fabrication methods, the quality of nanowire dimensional control in this approach depends on the uniformity of the nanoscale phase separation of the DBC layer and the presence of defects in that layer or on the guiding surface features that are defined by lithography.

A widely studied hybrid method for fabrication of nanowires with controlled position and crystallographic orientation is top-down patterning of metal catalyst seed particles used for subsequent bottom-up growth of nanowires from these seeds. Typically, electron beam exposure of a polymer resist layer, exposure to a developer solution, blanket metal catalyst deposition, and lift-off are used to produce a pattern of metal catalyst dots on the substrate surface [11,140,251], although imprint nanolithography of catalyst seeds has also been demonstrated [252,253]. Vapor-liquid-solid growth on a single crystal substrate which shares an epitaxial relationship with the wires determines their orientation. This is a relatively simple approach for achieving well-ordered arrays of vertical nanowires (Fig. 14). An alternative—patterning of holes and lift-off using both an e-beam resist and a deposited oxide mask to prepare oxide-isolated metal catalyst islands on a semiconductor surface for subsequent VLS nanowire growth—has also been studied [254]. Diameter control of the nanowires is limited both by factors typical of the top-down processing—the quality of the lithography step and the uniformity of the etching and lift-off steps, for example—and by those arising from nanowire nucleation and growth. These include coarsening of the catalyst seed particles before and during wire growth, tapering, and kinking. A variant of VLS catalyst lithographic patterning has been demonstrated for Si nanowire fabrication on amorphous SiO_2 substrates [255] and shows surprisingly good wire diameter uniformity at approximately 100 nm nominal diameter and a high yield of wires from patterned catalyst islands. In the absence of epitaxy with the substrate, however, there is some dispersion of the nanowire axial alignment.

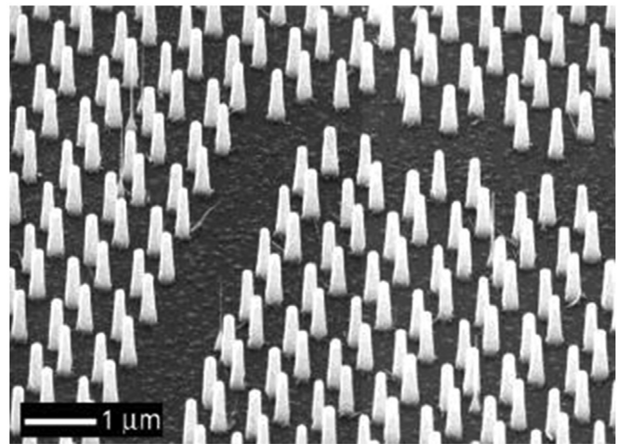

Fig. 14. Patterned InP nanowire array fabricated using e-beam lithography to define Au nanoparticles for VLS growth, from ref [11]. VLS, vapor-liquid-solid.

5. Nanowire heterostructure formation: growth vs. etching

Heterostructures respond to the change in material composition across an interface, known as a heterointerface. Thanks to their anisotropic shape, nanowires can incorporate heterostructures in different spatial orientations. An illustration of the degree of liberty that is in principle possible with this geometry is shown in Fig. 15(a). Change in material composition can occur along or perpendicular to the nanowire axis, be localized in some regions of the outer facets or even in the form of branches [256–258].

Axial nanowire heterostructures prepared in the top-down fashion are limited by the compositions achievable in thin film heterostructure growth. Atomically sharp heterostructures can be obtained, but on the other hand, materials combinations are constrained to a minimal lattice mismatch to avoid dislocations and strain-driven roughening. Lattice mismatch is much less of a constraint in VLS or VSS grown axial heterostructures. Reduced lateral dimensions of nanowires allow for an enhanced strain relaxation at misfitting interfaces, thus allowing materials combinations otherwise unviable in the thin film form [259]. Such axial heterostructures are obtained upon switching the growth precursors during the elongation of the nanowire. The switching of materials in VLS or VSS involves switching precursors which is reflected in changes in the composition of the liquid or solid catalyst. This switching is rarely atomically sharp and results in graded interfaces [see Fig. 15 (b)], a phenomenon known as the reservoir effect [260,261]. Typically, the reservoir effect is less pronounced for VSS compared with VLS and for nanowire-catalyst systems exhibiting limited solubility of the nanowire components. In III-V nanowires, it has been shown that switching of the group V element results in much sharper heterostructures with respect to varying the group III composition. Variation of group III is much more challenging both because of the reservoir effect and the complex phase diagrams of the corresponding ternary or quaternary alloys with catalyst metals [262–264].

For cases in which heterostructures are sharp at the atomic level, one would assume that this requires monolayer precision in the switching of material composition and crystal structure. This kind of accuracy is standard for MBE-based heterostructures, and it has been exploited in many applications including quantum-well and quantum-cascade lasers [265]. In the case of MBE, thickness control down to the monolayer level is possible thanks to the extremely well controlled flux and is aided by monitoring of the completion of each monolayer by reflection high-energy electron

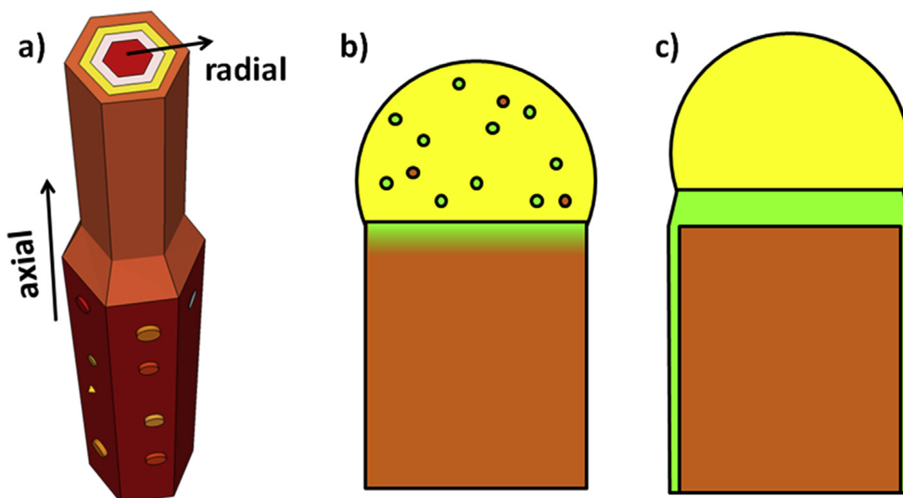

Fig. 15. Schematic illustration of various kinds of nanowire heterostructures emphasizing the design freedom given by the nanowire morphology.

diffraction. In nanowires, however, extremely accurate flux control does not guarantee monolayer precision. This is mainly because of the incorporation of chemical components through the catalyst [266,267]. Indeed, the creation of every new layer in a nanowire follows certain nucleation statistics, implying a time variation in the formation of each new monolayer [268]. Equally important, these nucleation statistics produce a distribution of interface thicknesses between segments of different composition and/or structure within nanowires growing in a parallel array on the same substrate. Thanks to the reservoir effect, this distribution is limited and follows a sub-Poissonian law [269].

Let us now discuss the case of heterostructures formed by growth on the side facets of nanowires. Radial heterostructures in VLS-VSS nanowires are obtained by enhancing the relative rate of precursor decomposition on the nanowire sidewall facets [(Fig. 15 (c)], in some cases by removing the metal catalyst. Radial growth is in principle also possible for top-down structures. After a top-down etch, the structures can be loaded in an epitaxial growth reactor, and growth can proceed on the side and top facets. In this case, the electronic quality of such heterostructures can be high, if the facets of the nanowires can be recovered and the native oxide and any etch residues are removed. As for axial heterostructures, radial heterostructures add functionality to nanowires, including quantum wells, dots, and variations in doping [270]. In addition, covering the side facets of nanowires is employed to passivate surface states and to reduce surface recombination [271]. Such approaches are used for both lattice matched and mismatched shells [272]. Extensive reviews of various radial nanowire heterostructures can be found in Refs. [273,274].

Finally, one should note that both the bottom-up and top-down approaches can be combined for the creation of heterostructures. As an example, after a nanowire has been etched down from a layer stack or a wafer, the structure can be covered by a further heterostructure in a bottom-up approach. To give an example, silicon nanowires could be first etched on a substrate. These could be used as templates to initiate growth of III-V nanowires on their tips and create an axial heterostructure [52,275,276]. Likewise, etched III-V nanowire structures could benefit from passivation with a subsequent radial growth of a higher bandgap material.

6. Doped semiconductor nanowires: growth vs. etching

Doping of a host crystal with electron donating (n-type) or accepting (p-type) impurities is typically required to fabricate semiconductor devices. Dopants often exhibit maximum bulk solubilities of ~1 at%, but they determine the majority and minority carrier types of the semiconducting crystal at much lower concentrations. Important attributes of introduced dopant concentration profiles are uniformity and control of the concentration in the field regions of a device and well-controlled spatial abruptness of the dopant profile in junction regions where one type of doping transitions to another. Difficulties arise in achieving desired doping profiles in the process of growing semiconductor nanowires. The challenges here in abruptness and incorporation are similar to the ones in heterostructure formation [277], including the reservoir effect resulting from the need to empty a liquid catalyst droplet of one dopant type and fill it with the other. In certain cases, impurities can be incorporated in a non-homogeneous manner in crystal defects such as stacking faults and twins [278].

Uniform dopant incorporation occurs in bulk and planar semiconductor devices by substrate crystal growth with dopant added to the melt from which the crystals grow. Often, these substrates are coated with a thin film of the same semiconductor grown from the vapor, also with controlled dopant concentration, but with lower concentrations of unintentional impurities (e.g. incorporated components of crucible materials used to contain the melt). Uniform doping of etched nanowires can generally be achieved simply by patterning and etching a bulk or thin film semiconductor that itself has a uniform and well-controlled dopant concentration. During catalyzed growth of nanowires, uniform dopant incorporation is often complicated by the varying kinetics of incorporation of different species in the nanowire crystal [279,280]. This may be a consequence of differences in decomposition kinetics of the respective precursor species on the catalyst or of atom attachment kinetics from the catalyst onto the wire tip. A typical result is incorporation of a significantly lower dopant concentration than is reflected in the gas phase composition from which the wires grow. In addition, the large dopant concentration in the vapor phase can produce uncatalyzed growth of more highly doped shells around the wires [281,282]. The resulting radial gradient in dopant concentration (Fig. 16) can be reduced by solid-state diffusion during postgrowth annealing [283] or by optimizing the growth process. For example, it was reported that the tapered P-rich Ge shell growth depicted in Fig. 16 could be eliminated by ceasing the flow of PH_3 at the end of steady-state nanowire CVD growth [284]. This change revealed the existence of a less severe radial dopant segregation in wires of constant diameter, consistent with the accumulation of dopant atoms in the liquid droplet adjacent to side

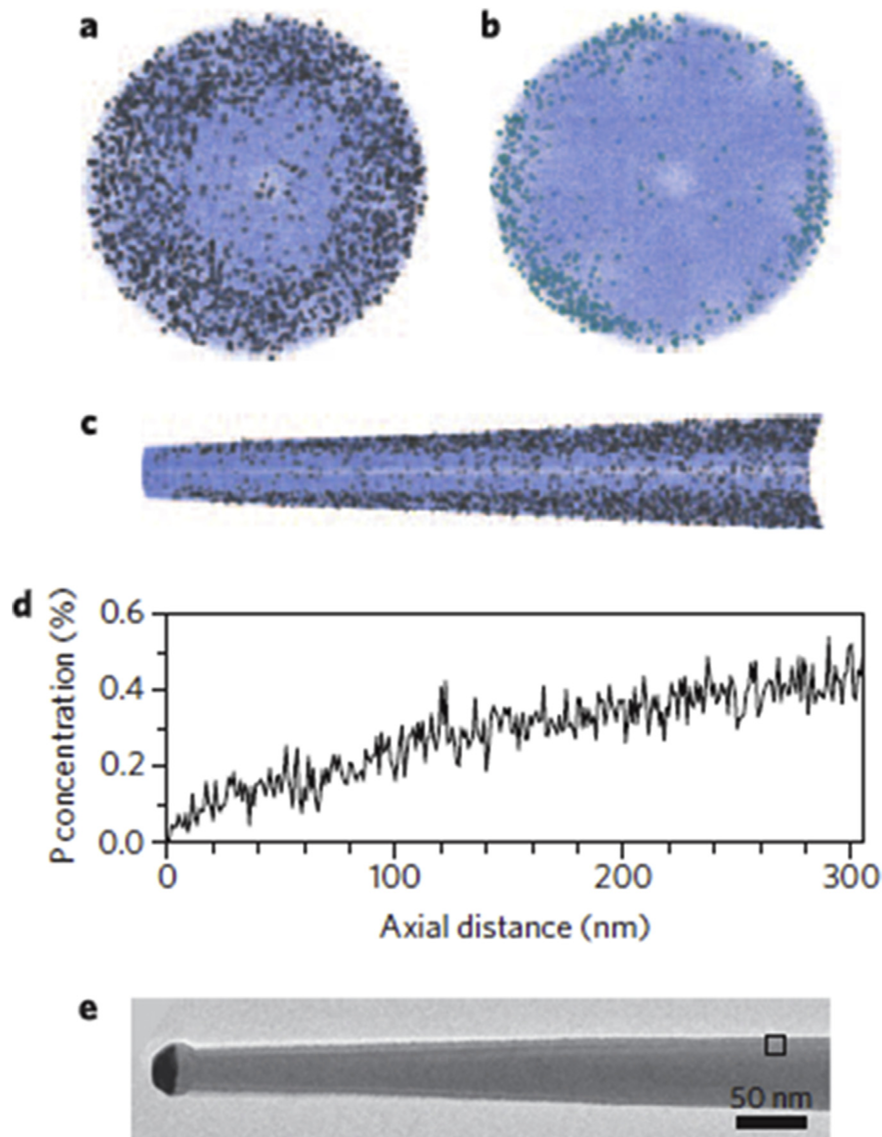

Fig. 16. Distribution of dopant atoms. (**a,b**) End-on view of nanowire highlighting the distribution of phosphorus (a, grey spheres) and oxygen (**b**, light blue spheres) in germanium (blue dots). (**c**) Side view of nanowire cross-section (2 nm thick) aligned with d. **(d)** Average phosphorus concentration along the growth axis. (**e**) Bright-field TEM image of phosphorus-doped germanium nanowire. After **ref 281.**

facets that are inclined relative to the (111) Ge nanowire growth facet [284]. The local phosphorus excess in the liquid freezes into the nanowire during steady-state growth. Abrupt doped junctions can be formed in bulk or planar devices by rapid switching of dopant sources during crystal growth. This technique is widely employed to prepare semiconductor quantum wells by MBE [285]. In elemental semiconductors, ion implantation followed by annealing is used to independently control the junction depth and dopant dose [286], while the abruptness of the concentration profiles across the junction are dictated by annealing conditions. In addition to electrically activating most of the ion-implanted dopant dose by promoting placement of dopants on appropriate lattice sites, the post-implant anneal annihilates point defects and removes extended imperfections from the ion implanted region [287].

Annealing to remove damage and activate dopants after ion implantation is complicated for compound semiconductors by their varied point defect chemistry and propensity to form complex extended defect structures. Annealing temperatures greater than those needed for As vaporization are typically used for implanted III-As crystals, requiring inert capping layers and adding process complexity [288].

Abrupt axial p-n junctions are readily transferred from bulk crystals to top-down nanowires by etching [289], with radial junctions formed by postetch deposition and/or annealing steps [290,291]. As already described, radial junctions are often formed unintentionally during catalyzed nanowire growth, and these can be further engineered by intentional shell growth or exposure to a dopant vapor without breaking vacuum [292]. Axial junctions have been formed in grown elemental semiconductor wires by local masking, ion implantation, and postimplantation annealing [293,294]. Axial junction formation in grown nanowires can also be achieved by switching the dopant concentration in the growth environment [295], but the abruptness of the resulting junctions depends on the capacity of the catalyst to store dopant atoms. Relatively insoluble dopants (e.g. As in gold-containing liquids) will

produce abrupt junctions [296] because the reservoir effect of the catalyst droplet is limited. Solubilities of impurities in solids are lower than in liquids; therefore, axial junctions formed by VSS growth should, in general, be more abrupt than those formed by VLS. In the latter case, the junction width can be similar to liquid catalyst diameter or the nanowire diameter for highly soluble dopants.

7. 'Growth-only' nanowire materials

There are certain semiconductor phases and/or alloy compositions that cannot be etched from thin film or bulk crystals because they are not, in general, stable as bulk-like materials. Instead, they can be formed as metastable phases or compositions during nanowire growth. This is made possible by, for example, the greater influence of surface/interface energies in nanoscale phase selection [61,62] and/or by kinetic trapping at the relatively low temperatures characteristic of nanowire growth [297].

7.1. Axial III-V/Si heterostructures

Monolithic integration of compound semiconductors on silicon has been a key goal of optoelectronics technology in the last decades. Elastic dilatation resulting from the reduced diameter of nanowires allows for defect-free growth of misfitting compound semiconductors on Si and Ge. Inversely, the nanowire morphology also allows for the integration of group IV semiconductors with III-V compound semiconductor segments along the nanowire axis [298–300]. This possibility opens up new avenues for heterostructure formation. Given the particular band alignment between the two families of semiconductors, such heterostructures also provide new opportunities for device design.

One should note, however, that to provide the basis for integrating nanowire optoelectronics in CMOS technology, one should obtain scalable growth of nanowires of controlled orientation and geometry on (100) oriented Si substrates [52,301].

7.2. Incorporation of insoluble impurities: the case of Mn-doped GaAs

Precipitation of a solid phase from a liquid in the VLS process also provides new possibilities in terms of incorporation of magnetic impurities such as Mn in GaAs. Incorporation of Mn at technologically useful concentrations in a GaAs matrix is a well-known challenge [302]. This was first achieved in GaAs nanowires by using Mn to assist the wire growth [303]. Recently, via Ga-seeded GaAs nanowire growth, it has been shown that Mn can be incorporated locally into the structure of GaAs nanowires, even forming MnAs segments [304]. Interestingly, these segments show ferromagnetic behavior at room temperature and thus provide a new avenue for synthesis of spintronic nanostructures.

7.3. Metastable crystalline phases

As detailed in previous sections, polytypism is an intrinsic phenomenon of bottom-up nanostructure formation. It is related to both the high surface-to-volume ratio of nanowires and also can be promoted by the particular nucleation of each new compound semiconductor bi-layer formed via the VLS growth mode. Achieving metastable phases in VLS- grown semiconductor nanowires opens up many new possibilities for engineering their functional and structural properties [305].

7.3.1. Hexagonal group IV semiconductors

Alternative phases, other than the diamond cubic phase, of group IV semiconductors are interesting for their potentially novel properties. For example, the lonsdaleite (LD) phase, a hexagonal wűrtzite form of silicon and germanium, can be synthesized at very high pressures [306]. The LD Ge phase is theoretically predicted to be a direct-gap semiconductor [307]; however, thorough optical characterization of LD, silicon and germanium have not been reported previously because of the limited availability of single crystals of these materials, which are typically synthesized in diamond anvil cells. Recently, Hauge et al. have reported the first synthesis of hexagonal silicon and $Si_{1-x}Ge_x$ single crystal layers deposited as shells around lattice-matched wűrtzite GaP core nanowires [308,309]. The GaP wires are themselves in a non-equilibrium phase as a result of contact-angle kinetic trapping in the wűrtzite phase rather than growth of stable zinc blende GaP [310]. Selective removal of the GaP cores to create single crystal nanotubes [311] may permit more wide-ranging characterization and application of LD Si and LD $Si_{1-x}Ge_x$ alloys.

7.3.2. Metastable germanium-tin alloys

Germanium-tin alloys are of great interest for their high carrier mobilities [312] and the possibility of achieving a direct band gap for efficient mid-infrared light emission [313] in a materials system that is chemically compatible with silicon substrates. Tin alloying to the predicted >10 at.% composition required to achieve a direct gap in an unstrained crystal is difficult. This composition greatly exceeds the maximum equilibrium solubility of Sn in bulk Ge, ~1 at.% [314]. Tin can precipitate from GeSn alloys at high concentrations [315,316]. Moreover, the lattice mismatch of Sn to Ge and Si induces compressive biaxial strain in thin films, shifting the energies of conduction band states in opposition to the effect of Sn alloying, thus requiring even greater Sn content. Wirths et al. reported growth of direct-gap GeSn alloy films with >12 at.% Sn by CVD [317] using a Ge buffer layer coated silicon substrate. Optically pumped laser operation was achieved at $T < 90$ K, but with threshold degradation and low external quantum efficiency because of extrinsic recombination centers.

These results point out the importance of preparing free-standing, single-crystal Ge-Sn nanowires with large Sn concentrations and without the compressive misfit strains and dislocations present in two-dimensional films. A first report of single crystal $Ge_{1-x}Sn_x$ VLS nanowire growth suggested Sn compositions up to $x = 0.092$ were achieved directly by VLS growth, using metal-organic Ge and Sn precursors in a liquid injection CVD system [297]. In contrast, axial growth of GeSn nanowires by Au-catalyzed CVD using more standard GeH_4 and $SnCl_4$ precursors with HCl(g) added to the growth environment has been found to produce a very low Sn incorporation in the wires [318]. More recently, deposition of Ge core/$Ge_{1-x}Sn_x$ shell nanowires using GeH_4 and $SnCl_4$ precursors in low pressure CVD has been reported independently by two groups. Strong room temperature PL was measured from both the tensile strained Ge cores and the nearly strain-free GeSn shells [319]. Core and shell strain measurements [320] were consistent with coherent core/shell interfaces. Maximum Sn compositions incorporated in the diamond cubic shell crystal were reported to range from $x = 0.04$[319] to $x = 0.13$[320].

The Sn composition in the shell is not uniform, however. Cross-sectional images and composition mapping of the core/shell nanowires show the presence of a characteristic 'spoke and hub' distribution of components with Ge-rich spokes aligned along the <110> radial axes of NWs (Fig. 17) [321,322]. Once formed, there can be a significant elastic energy penalty for terminating the Ge-rich spokes by overgrowth of the $Ge_{1-x}Sn_x$ shell [321].

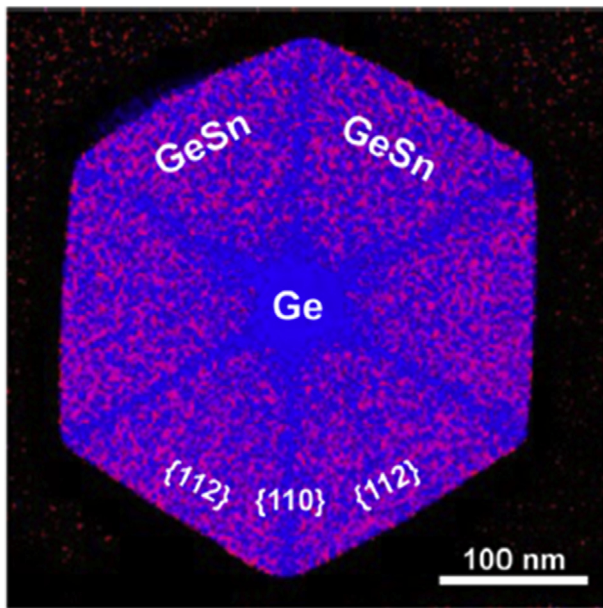

Fig. 17. Cross-sectional energy dispersive spectrometry composition map of a Ge core/ $Ge_{1-x}Sn_x$ shell nanowire. After ref [320].

8. Future outlook: comparison of growth vs. etching in nanowire synthesis

Table 1 illustrates the advantages anticipated for etched nanowires, fabricated using the top-down paradigm involving lithographic patterning. Chief among them are precise positioning control, dimensional reproducibility, and compatibility with standard silicon-based device fabrication. Incorporation of dopants is also generally favorable in top-down patterned and etched semiconductor nanowires compared with bottom-up synthesized wires because of the complexities noted in Section 6 with respect to dopant incorporation through the catalyst particle during locally catalyzed growth of the wire. These attributes are critically important in the practical fabrication of semiconductor devices for complex circuits and systems. The superior reproducibility of top-down fabrication of nanowires is also a compelling argument for using the approach in manufacturing.

The limits of 1D semiconductor dimensional control are also more easily approached using etched nanowires than grown. Even in the case of homoepitaxy, VLS growth always requires a nucleation step: nucleation of the liquid droplet. This step exhibits an energy barrier that increases as the catalyst (and wire) diameter decreases and which is not present in etching. Therefore, it is likely the case that the fabrication paradigms (top-down and, in some cases, hybrid) that rely on etching will ultimately achieve smaller nanowire diameters than growth.

Developments in top-down nanostructure fabrication methods have been driven by the needs of the semiconductor industry to scale device dimensions according to Moore's Law. As conventional device scaling comes to an end, the rate of future innovation in top-down patterning and etching may slow, prompting greater opportunities for bottom-up and hybrid fabrication approaches. One of the shortcomings of top-down patterning remains the uniformity of diameter and length control over 1D geometries. Here, the bottom-up paradigm may provide more precise control. This will become even more relevant in the future as semiconductor manufacturers consider the possible adoption of new transistor channel materials [323]. In this case, selective-area epitaxy (VS growth) approaches have demonstrated excellent control over nanostructure, geometry, connection, and scalability [324–328].

Growth, either in bottom-up or hybrid nanowire fabrication, offers some important advantages over etching processes in the formation of epitaxial nanowire heterostructures. For axial heterostructures, strains arising from lattice mismatch can be readily accommodated by elastic dilatation, particularly at small wire diameters. In comparison, 2D thin film heterostructures frequently suffer from misfit and threading dislocation formation because of lattice mismatch. Threading dislocation segments can be incorporated in wires etched from such thin films, with limited ability to detect such defects by typical postetch metrology. However, growth processes also introduce significant challenges in axial heterostructure formation. The reservoir effect often limits the compositional abruptness of grown axial nanowire heterostructures, and the complex interplay of gas phase composition and liquid catalyst

Table 1
Etched versus grown semiconductor nanowires structural features.

Characteristic	Etched	Grown	Comment	References
Shape				
Minimum diameter	2 nm	10 nm		[143,159,332,333]
Pitch	5 nm	25 nm		[230,332]
Diameter reproducibility	++	+		[230,334]
Diameter control along axis	+	++		[230,334–336]
Positioning accuracy	++	+		[230,334,337]
Axial alignment	+	−		
Bulk defects	+(1)	−	(1)Elemental (+) vs. compound (-) semiconductors	
Functionality				
Sidewall surface roughness	3 nm	0.3 nm		[170,171,230]
Surface defects/contamination	-	+/-		[170,171,230,338]
Misfitting substrates	−	++		
Non-equilibrium phases	−	++		
Design				
Axial heterostructures	+(2)	0(3)	(2) Small (+) vs. large (-) lattice mismatch systems (3) VSS (0) vs. VLS (-) growth; reservoir effect	
Radial heterostructures	-	+		
Doping design	+/0	+		
Technology				
Compatibility with large areas	+	+/0		
CMOS compatibility	++	0/-(4)	(4) Gold (-) versus self-catalyzed/electronically benign (0) catalysts	
Innovation potential	+	++		

VLS, vapor-liquid-solid; VSS, vapor-solid-solid.

wetting complicates the reproducible nucleation of one phase on another.

The advantages of nanowire growth are more clearly evident in radial heterostructure formation. An all-growth process (two deposition steps, one axial and one radial) to form a radial heterostructure avoids vacuum breaks, air exposure, and surface cleaning steps inherent in epitaxial overcoating of etched semiconductor nanowires. As long as contamination of the sidewall surface by catalyst atoms is avoided, the surface cleanliness and structure of the core wire will be superior in the all-growth methodology, and this is likely to promote formation of a more perfect crystalline shell. In the case of compound semiconductors, it may not be possible to etch nanostructures by typical semiconductor industry methods without introducing unacceptable damage to the crystal and its surface [329].

Beyond the issue of lattice mismatch, substrate flexibility in general is an important positive feature for nanowire growth. For future applications in which geometrical and crystallographic alignment of semiconductors is not especially important (e.g. nanowire sensor arrays), growth is a logical option. Indeed, the low temperatures used in many VLS and VSS growth processes make it amenable to deposition on a variety of non—single-crystal substrates, including polymers [330,331].

Perhaps the most compelling case to be made for nanowire growth is its ability to fabricate metastable phases that are either not accessible or not useful when deposited as thin films or bulk crystals from which wires can be etched. The synthesis of würtzite-structure GaAs nanowires, a phase that is not observed in the bulk, in a controlled manner is an indication of the potential that VLS growth offers to form metastable phases. Further, the use of lattice-matched würtzite GaP core nanowires as a template for forming hexagonal silicon and germanium suggests an entirely new approach to metastable semiconductor phase engineering, enabled by nanowire growth. Future developments in this field will likely include the application of these and other novel nanowire growth approaches to synthesize new, metastable semiconductor phases with unique properties. This emerging field of 'growth-only' nanowire materials synthesis shows that catalyzed growth of 1D crystals remains an important tool for materials innovation, more than five decades after the first reports of the VLS mechanism.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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