2019 IEEE Energy Conversion Congress and Exposition (ECCE)

On Facilitating the Modular Multilevel Converter Power Scalability Through Branch Paralleling

S. Milovanovic and D. Dujic

On Facilitating the Modular Multilevel Converter Power Scalability Through Branch Paralleling

Stefan Milovanović and Dražen Dujić
Power Electronics Laboratory - PEL
École Polytechnique Fédérale de Lausanne - EPFL
Station 11, CH-1015 Lausanne
stefan.milovanovic@epfl.ch, drazen.dujic@epfl.ch

***Abstract*—Modular multilevel converter current scalability challenge can be significantly alleviated by connecting its branches in parallel. In case a predefined submodule design is to be used with the aim of serving a certain span of applications, methods of achieving desired current scalability of the modular multilevel converter rely upon numerous hardware adaptations. Contrary to that, for the same goal to be achieved, paralleling of the branches eliminates the need for a major redesign of the existing converter parts. Consequently, superior operational flexibility can be achieved with most of the effort being concentrated in the control domain, allowing for less costly solutions to be realized. This paper provides a thorough control analysis of the modular multilevel converter operating with an arbitrary number of parallel connected branches.**

***Index Terms*—MMC power capacity extension, branch paralleling, medium voltage high power conversion**

I. Introduction

Modular Multilevel Converter (MMC), presented in Fig. 1, found its place within High Voltage (HV) and Medium Voltage (MV) applications owing to the possibility of effortlessly meeting the imposed voltage requirements by stacking the so-called submodules (SMs), also being referred to as cells, in series [1], [2]. Depending upon the application, SMs are mainly Half-Bridge (HB) or Full-Bridge (FB), notwithstanding the other combinations also being an option [3]. Therefore, high quality voltage waveform can be synthesized across the MMC AC terminals, while using the power devices of a lower voltage rating, resulting in very modest or even no filtering requirements on the grid side. Additionally, if any of the SMs happens to fail, operation of the converter can be maintained owing to the likely exploited redundancy principles [4]. According to Fig. 1, a cluster of SMs in series connection with an inductor L_{br} can be referred to as branch, whereas two branches comprise a leg.

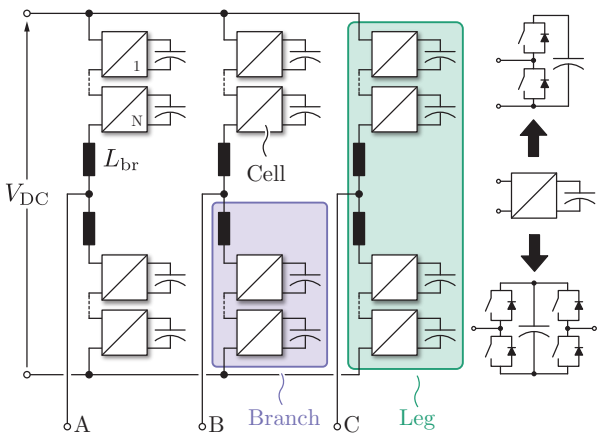


Figure 1: Modular Multilevel Converter (MMC)

Any MMC design implies clearly defined voltage and current ratings of the SMs. This means that stacking more SMs in series, in order to increase the MMC voltage rating, directly implies the MMC power rating increase, given the fixed current rating of the SMs. Nevertheless, power increase of a MMC intended to operate at a predefined voltage rating, implies the need for the boost of its current handling capabilities (an example of such a scenario can be found in hydro applications [5], where generators' insulation constraints do not allow for an arbitrary increase in the operating voltages above a certain level). In other words, rated current of the SM must be increased on these terms. On one hand, a new SM design can be carried out to support the application needs, however this is likely to introduce additional R&D costs. On the other hand, the existing SM design can be reused to increase the MMC current rating if paralleling of Power Modules (PMs) within the SM or paralleling of the SMs themselves had been foreseen in the manufacturing process.

Parallel connection of PMs, as presented in Fig. 2a, introduces the need for special considerations to be included into the SM design due to different static and dynamic characteristics of the employed semiconductors [6], [7]. Furthermore, it is likely that a SM manufacturing process might restrict the choice of PMs to be employed. To provide the flexibility in terms of the SM current rating, without the need for carrying out a new design process for each of the ratings individually, cooling system as well as the SM frame size are determined for the highest of desired currents. Additionally, paralleling of the PMs implies higher SM capacitance demands. Consequently, during the design phase, a certain amount of volume must be allocated within a SM in order to host all the necessary capacitors should PMs paralleling be the case.

Fig. 2b illustrates the extension of the MMC current capacity through paralleling of the HB SMs [8], [9]. It is noteworthy that positive terminals of the SM capacitors should also be connected, with the aim of equalizing the voltage across all of the SMs. Therefore, even though SMs paralleling

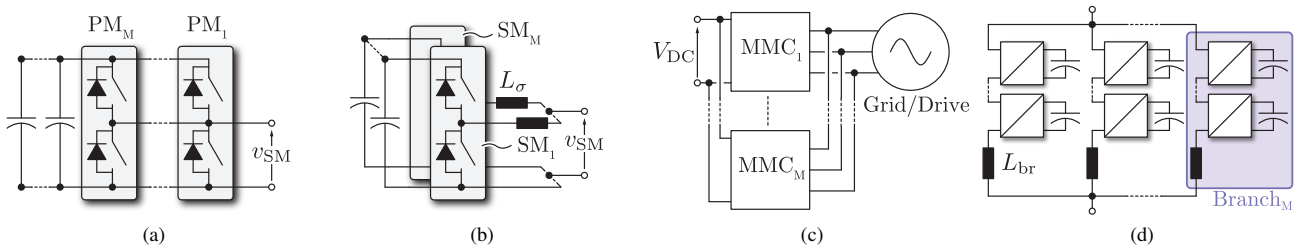


Figure 2: (a) Parallel connection of PMs within a SM; (b) Parallel connection of SMs; (c) Parallel operation of an arbitrary number of MMCs; (d) Parallel connection of MMC branches;

might not be needed, additional terminals, allowing for the connection of capacitors' positive terminals, must be foreseen in the SM design phase. It is worth mentioning that this additional terminal does not represent a part of the regular MMC SM. Furthermore, although small, additional inductance L_σ has to be installed in series with every SM in order to ensure equal current split among them in case of paralleling. One can easily conclude that additional inductance mentioned above represents unnecessary part of the SM should paralleling not be required. Moreover, due to the fact that paralleled SMs are normally switched simultaneously, synchronization among gate signals, or specially designed driver master/slave structure, must also be provided.

Fig. 2c presents an arbitrary number of converters operating in parallel, which is a well known and widely used method in case of a single MMC being incapable of delivering power demanded by the application [10], [11]. In [11] paralleling of the MMC legs, derived following the idea presented in [12], was discussed, however from the circuit configuration standpoint, it corresponds to the parallel connected MMCs.

Paralleling of the MMC branches represents an alternative to the above mentioned possibilities. Providing equal power split among the branches is ensured in a robust manner, no major redesign of the existing converter parts is needed. Consequently, problem of increasing the MMC current rating migrates to the control domain, meaning that cheaper solutions requiring less engineering effort can be obtained. In other words, the existing SMs can be reused without the need of undergoing any major redesign process. Power scaling of the MMC gets substantially facilitated, yet with constraints being imposed solely by the employed control platform. Fig. 3 presents the MMC operating in this configuration. To retain the naming consistency, what has been referred to as branch so far, will henceforth be referred to as Sub-Branch (SBR). Employment of the HB SMs will be assumed, although all the principles derived can simply be expanded onto any type of the employed SM. Number of series connected SMs within a SBR is denoted by N, whereas number of parallel SBRs within a branch is denoted by M. Moreover, Fig. 3 shows that an additional inductor L_a can be connected in series with the set of parallel SBRs. Consequently, higher level of flexibility is ensured in terms of the converter inductances optimization with respect to the simple paralleling of the MMCs. However, such an analysis falls beyond this paper's scope. In the forthcoming analysis, presence of the inductor L_a will be neglected, however it does not affect generality of presented results.

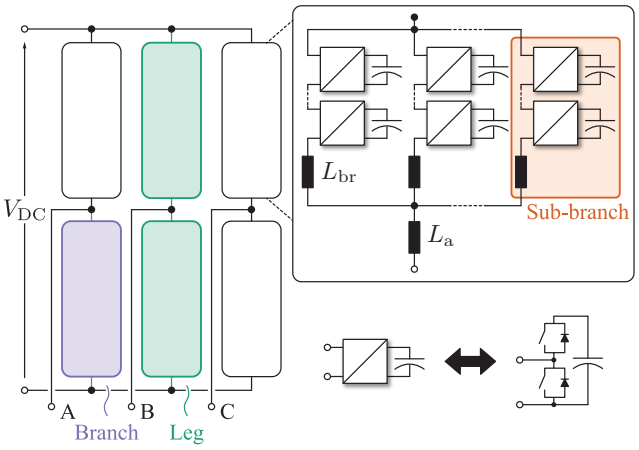


Figure 3: MMC operating with parallel SBRs

II. Preliminary Considerations

Fig. 4 depicts an arbitrary number of parallel connected SBRs assuming that clusters of MMC SMs can be replaced by the ideal voltage sources. In accordance to the Thevenin's theorem, a branch can be replaced by the series connection of equivalent voltage source, inductor and resistor. Additionally, all parameters of the branch equivalent circuit represent the averages of individual SBR parameters. Therefore, equivalent circuit of the analyzed converter does not differ from the conventional MMC [13], as depicted in Fig. 5. Consequently, control of the all the relevant quantities can be established by means of two voltages being defined for each leg as

$$v_\mathrm{si} = \frac{\overline{v_\mathrm{ni\Sigma}} - \overline{v_\mathrm{pi\Sigma}}}{2} \qquad v_\mathrm{ci} = \frac{\overline{v_\mathrm{ni\Sigma}} + \overline{v_\mathrm{pi\Sigma}}}{2} \tag{1}$$

Likewise, two current components, namely the leg output current (i_i) as well as the leg common-mode current (i_ci), are

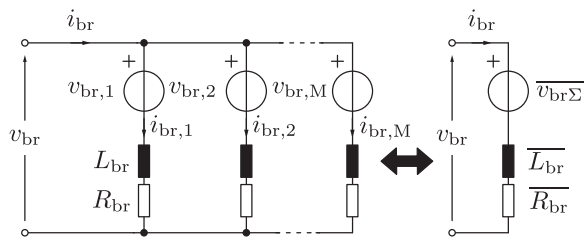


Figure 4: An arbitrary number of parallel connected SBRs (left) along with the Thevenin's equivalent of such a connection (right)

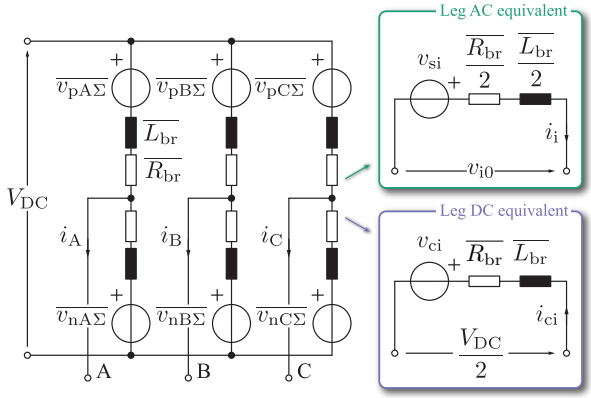


Figure 5: Equivalent circuit of the MMC operating with parallel SBRs

defined for each leg, according to (2). Subscripts "p" and "n" denote upper and lower branch quantities, respectively.

$$i_{\mathrm{i}} = i_{\mathrm{pi}} - i_{\mathrm{ni}} \qquad i_{\mathrm{ci}} = \frac{i_{\mathrm{pi}} + i_{\mathrm{ni}}}{2} \tag{2}$$

Voltages defined by (1) control the converter output and common-mode currents, respectively. Since a set of parallel SBRs can be perceived as a floating energy source, similarly to the conventional MMC, all of the control methods presented in the literature can be utilized [13]–[16]. However, these control methods aim to control the total amount of energy stored within a branch, without concerning the energy distribution among its SBRs. To track the output current reference, while maintaining the energy balance among the branches, conventional MMC control layers provide every branch with the reference voltage ($\overline{v^*_{\mathrm{br}\Sigma}}$) being obtained in the manner corresponding to the regular MMC (3). Henceforth, these control layers will be referred to as higher control layers.

$$\overline{v^*_{\mathrm{pi}\Sigma}} = \frac{v^*_{\mathrm{ci}} - v^*_{\mathrm{si}}}{2} \qquad \overline{v^*_{\mathrm{ni}\Sigma}} = \frac{v^*_{\mathrm{ci}} + v^*_{\mathrm{si}}}{2} \tag{3}$$

It is easy to understand that large discrepancies among SBR energies, which are not taken into account by the higher control layers, lead to inevitable fault or even damage of the converter. Hence, additional control measures must be taken. Perceiving the branch voltage references as the common-mode components of individual SBR voltages, voltage generated by an arbitrary SBR can be expressed as (4), where $\Delta v_{\mathrm{br,i}}$ represents the deviation of voltage generated by an individual SBR with respect to the references provided by the higher control layers.

$$v_{\mathrm{br,i}} = \overline{v^*_{\mathrm{br}\Sigma}} + \Delta v_{\mathrm{br,i}} \tag{4}$$

According to (4), there is a certain degree of freedom in the choice of a SBR voltage. However, control of the current components defined by the higher control layers, and the application where the MMC is used, must not be hindered. Consequently, all the deviations $\Delta v_{\mathrm{br,i}}$ must sum up to zero, as defined by (5).

$$\sum_{i=1}^{M} \Delta v_{\mathrm{br,i}} = 0 \tag{5}$$

III. Balancing of the sub-branch energies

Prior to commencing any SBR energy balancing discussions, balancing of the currents within a branch should be clarified. According to Fig. 4, one can easily derive

$$L_{\mathrm{br}} \frac{d}{dt} \underbrace{\left(i_{\mathrm{br,i}} - \frac{i_{\mathrm{br}}}{M} \right)}_{\Delta i_{\mathrm{br,i}}} + R_{\mathrm{br}} \left(i_{\mathrm{br,i}} - \frac{i_{\mathrm{br}}}{M} \right) = \overline{v_{\mathrm{br}\Sigma}} - v_{\mathrm{br,i}} \tag{6}$$

Replacing $v_{\mathrm{br,i}}$ from (6) with (4), leads to the conclusion that distribution of currents within a branch, can be affected by means of disturbances $\Delta v_{\mathrm{br,i}}$ (7). As will be shortly demonstrated, if properly generated, these deviations can be effectively used to perform energy balancing of the SBRs.

$$L_{\mathrm{br}} \frac{d}{dt} \Delta i_{\mathrm{br,i}} + R_{\mathrm{br}} \Delta i_{\mathrm{br,i}} = -\Delta v_{\mathrm{br,i}} \tag{7}$$

However, balancing of the SBR currents should not affect the control of other variables within the converter, therefore (5) must be respected at all times. This criteria can be met in case controller presented in Fig. 6 is employed. According to (8), sum of voltage disturbances generated by the SBR currents balancing equals zero, meaning that the other control layers of the converter are indeed not affected. Further, adopting the nomenclature from the conventional MMC, currents $\Delta i_{\mathrm{br,i}}$ can be perceived as the branch circulating currents. Branch circulating currents sum up to zero at its terminals, therefore not interfering with the currents controlled by the higher control layers. In (8) $H_{\Delta \mathrm{i}}$ denotes Δi_{br} controller, with the structure being determined by the nature of currents to be controlled. Namely, if DC currents are to be balanced among the SBRs, PI controller can be used. However, in case of an AC component existence, the resonant part must also be included.

$$\sum_{i=1}^{M} \Delta v_{\mathrm{br,i}} = H_{\Delta \mathrm{i}} \sum_{i=1}^{M} \left(\overline{i_{\mathrm{br}}} - i_{\mathrm{br,i}} \right) = 0 \tag{8}$$

Equal SBR currents distribution is desirable from the installed semiconductor devices current rating standpoint. However, from the energy sharing viewpoint, equal SBR currents distribution is not always desirable, especially if the SBR inductances differ. In case of the MMC, ensuring equal energy distribution between its (sub)branches is crucial. Please notice that in the circuit presented in Fig. 4 SBR current balancing does not necessarily imply that the SBR energy equilibrium is to be reached. To support this statement, the following analysis can be conducted.

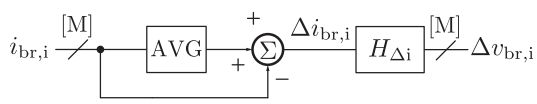


Figure 6: SBR currents balancing controller

Deviations of SBR inductances with respect to the rated value (for instance, $\pm 20\%$) is to be expected in practice. If all the SBRs generate the same voltage, while operating under the condition defined by $L_{\text{br,1}} \neq L_{\text{br,2}} \neq ... \neq L_{\text{br,M}}$, branch current does not split equally among the SBRs ($i_{\text{br,1}} \neq i_{\text{br,2}} \neq ... \neq i_{\text{br,M}}$). If, however, SBR currents were to be balanced, meaning that $i_{\text{br,1}} = i_{\text{br,2}} = ... = i_{\text{br,M}}$, SBR voltages satisfying $v_{\text{br,1}} \neq v_{\text{br,2}} \neq ... \neq v_{\text{br,M}}$ would be required. One can notice that, in both cases, SBR powers are not equal, which inevitably causes the SBR energies to diverge. Consequently, additional energy controller must be superimposed to the controller presented in Fig. 6. Also, newly introduced SBR energy balancing controller must not hinder the performance of the other control loops, as defined by (5).

To determine the correct operation of the SBR energy balancing controller, mean power equation of an arbitrary SBR can be analyzed. Given that SBRs conduct the current consisting of the DC and AC components according to (2), a SBR power equation can be expressed as

$$P_{\text{br,i}} = \overline{v_{\text{br,i}} i_{\text{br,i}}} = \pm \underbrace{V_{\text{br,i}} I_{\text{br,i}}}_{\text{DC terms}} \mp \underbrace{\overline{\tilde{v}_{\text{br,i}} \tilde{i}_{\text{br,i}}}}_{\text{AC terms}} \tag{9}$$

Generally, a SBR power equation can be expanded into the Taylor series, leading to

$$P_{\text{br}} = \underbrace{P_{\text{br}}^{\text{nom}}}_{=0} + \underbrace{\Delta P_{\text{br}}^{\text{DC}}}_{\approx \frac{1}{2} V_{\text{DC}}^{*} \Delta i_{\text{br,i}}^{\text{DC}}} + \underbrace{\Delta P_{\text{br}}^{\text{AC}}}_{\text{depends on } \Delta L_{\text{br}}} \tag{10}$$

With the current balancing controller from Fig. 6 being enabled, it can be concluded that AC components of the SBR powers depend on the SBR inductances mismatches. However, steady state value of DC voltages generated by all the branches can be approximated to half of the converter input voltage $V_{\text{DC}}^{*}/2$. Hence, all the mismatches in SBR powers can be compensated by adjusting the SBR currents mismatches $\Delta i_{\text{br,i}}^{\text{DC}}$ (DC components of branch circulating currents), making control problem of the SBR energy balancing linear.

Fig. 7 presents the structure of the SBR energy balancing controller (part labeled with green). Individual SBR energies are measured, filtered and passed to the averaging block (AVG). This way, energy reference of every individual SBR is set to the average energy of the branch as a whole. Thereupon, SBR energies are subtracted from the branch averaged energy and finally passed to the controller ($H_{\Delta \text{W}}$). Output of the SBR energy balancing controller represent its circulating current DC component $\Delta i_{\text{br,i}}^{\text{DC}*}$, which is obtained in two steps. Initially, a

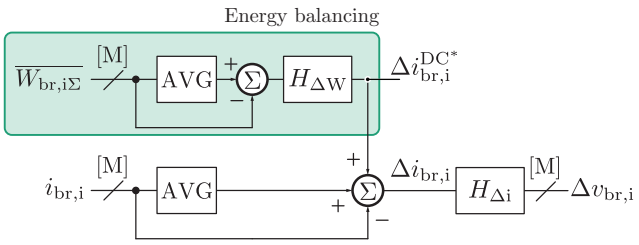


Figure 7: Structure of the SBR energies balancing controller

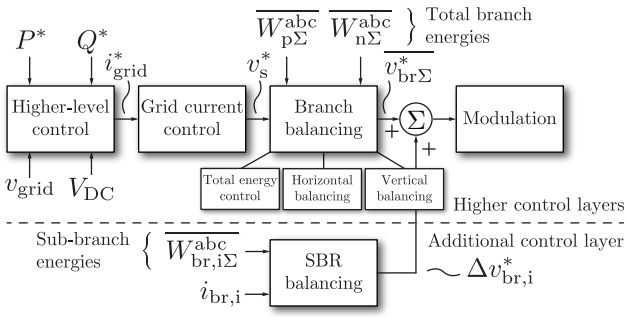


Figure 8: Control layers of the MMC operating with parallel SBRs. Please notice that conventional MMC control still represent the major part of the schematic.

SBR energy deviation (ΔW) gets passed to the PI controller in order to obtain the power component $\Delta P_{\text{br}}^{\text{DC}}$. In the following step, division with half the converter input voltage $V_{\text{DC}}^{*}/2$ is performed, which, according to (10), provides $\Delta i_{\text{br,i}}^{\text{DC}*}$. Given that the analyzed converter operates with the DC voltage ranging from several kV to a few hundred kV, contribution of the SBR energy balancing controller to a SBR current should be very modest. Notwithstanding, one should keep in mind that the SBR energy balancing controller does not take care of the total energy stored within a branch. This task is assigned to the controllers belonging to the higher control layers. Similarly to (8), and according to Fig. 7, it can be easily shown that this way of performing the SBR energies balancing does not affect the outer control layers. Once calculated, voltage components $\Delta v_{\text{br,i}}$ are summed with the branch common-mode references ($\overline{v_{\text{br}\Sigma}^*}$) obtained from the higher control layers including the grid current control, horizontal balancing, vertical balancing and total converter energy control, as presented in Fig. 8. It should be emphasized that this method of balancing the SBR energies does not depend on the number of parallel connected SBRs. Practically speaking, for a given voltage rating, a MMC power rating can be easily extended by paralleling an arbitrary number of SBRs within the branch.

IV. Modulation Considerations

As the equivalent voltage seen from the terminals of a branch corresponds to the scaled sum of the SBR voltages according to Fig. 4, by employing a suitable modulation scheme, number of voltage levels seen the from the converter's terminals (both AC and DC) can be varied. Henceforth, the use of Phase Shifted Carrier (PSC) modulation will be assumed, although the other modulation methods can also be considered.

Operation of the conventional three-phase MMC employing PSC modulation to synthesize multilevel voltage waveforms was thoroughly analyzed in [17]. Nevertheless, to support the upcoming discussion, an example of a MMC leg containing two parallel SBRs per branch, presented in Fig. 9, will be observed. Since the use of HB SMs is assumed throughout this paper, angular displacement among the carriers modulating an observed branch equals $\Delta\theta_{\text{carr}} = 2\pi/N$. In [17] the MMC operating with no parallel branches was analyzed, stating that an increase in the number of voltage levels seen from the AC terminals can be achieved by introducing an angular offset

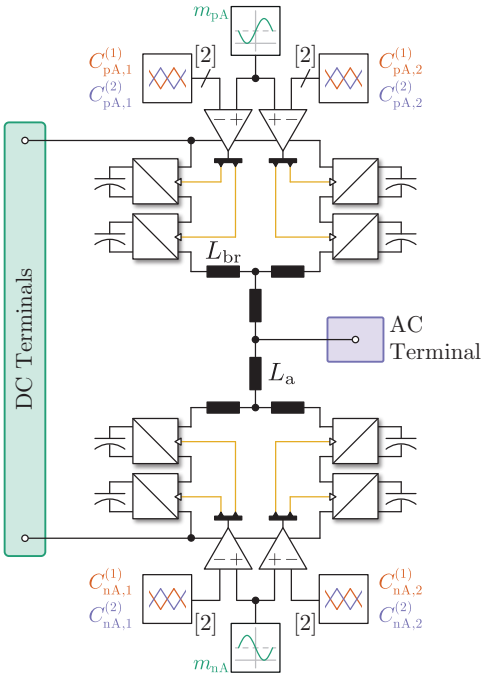


Figure 9: An exemplary case used to present the possibility of varying the number of voltage levels seen from the converter's terminals

δ into the displacement of upper and lower branch carriers. Therefore, one can easily derive (11) and (12), where i denotes the index of a SM in an observed string.

$$\theta_{\mathrm{n}}^{(\mathrm{i})} = (i-1)\Delta\theta_{\mathrm{carr}} \tag{11}$$

$$\theta_{\mathrm{p}}^{(\mathrm{i})} = (i-1)\Delta\theta_{\mathrm{carr}} + \delta \tag{12}$$

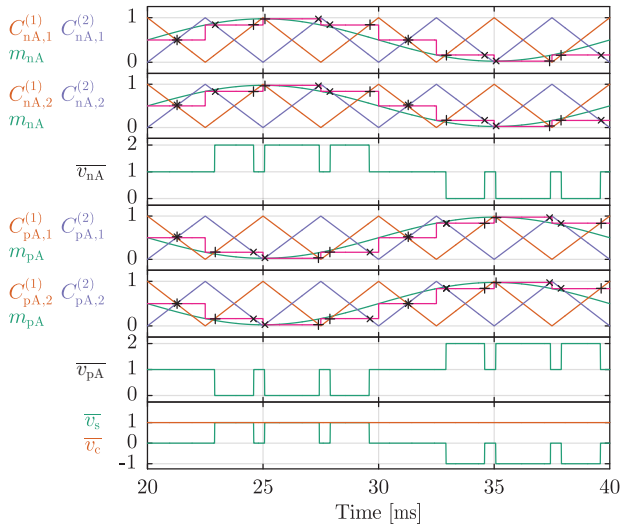
However, paralleling the SBRs provides additional degree of freedom in terms of possible displacement among the sets of carriers modulating the SBRs. Namely, an offset β can be introduced to the carriers modulating the SBRs belonging to the same branch, thus providing

$$\theta_{\mathrm{n,j}}^{(\mathrm{i})} = (i-1)\Delta\theta_{\mathrm{carr}} + (j-1)\beta \tag{13}$$

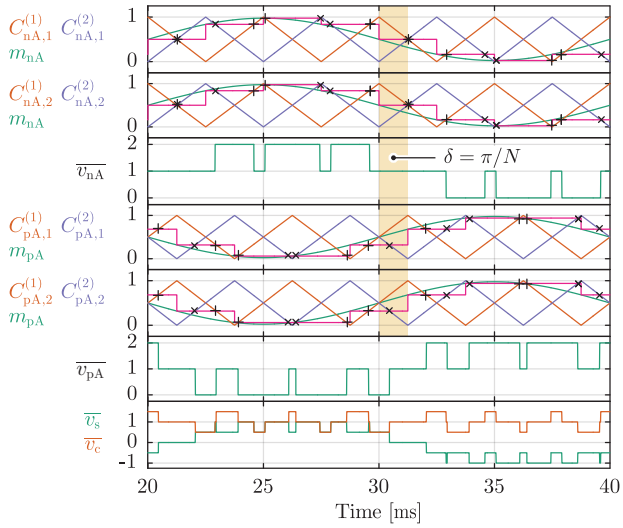
$$\theta_{\mathrm{p,j}}^{(\mathrm{i})} = (i-1)\Delta\theta_{\mathrm{carr}} + (j-1)\beta + \delta \tag{14}$$

where i denotes the index of a SM belonging to an observed SBR, whereas j denotes the index of a SBR itself.

To showcase different modulation possibilities, one can firstly start with no carrier offsets being introduced to the circuit presented in Fig. 9, meaning that $\beta = \delta = 0$. On these terms, it is straightforward to conclude that two branches, belonging to the same leg, change their state at the same time. Consequently, from the AC voltage generation standpoint, the MMC operating with parallel SBRs does not differ from the conventional MMC, therefore already established principles of PSC modulation applied to the standard MMC can be used. Seen from the converter's AC terminals, $N+1$ voltage levels are generated, thus the name $(N+1)-$level modulation, as presented in Fig. 10a. Further, introducing the offset between the groups of carriers modulating the lower and upper branch,



(a) $(N+1)-$level modulation

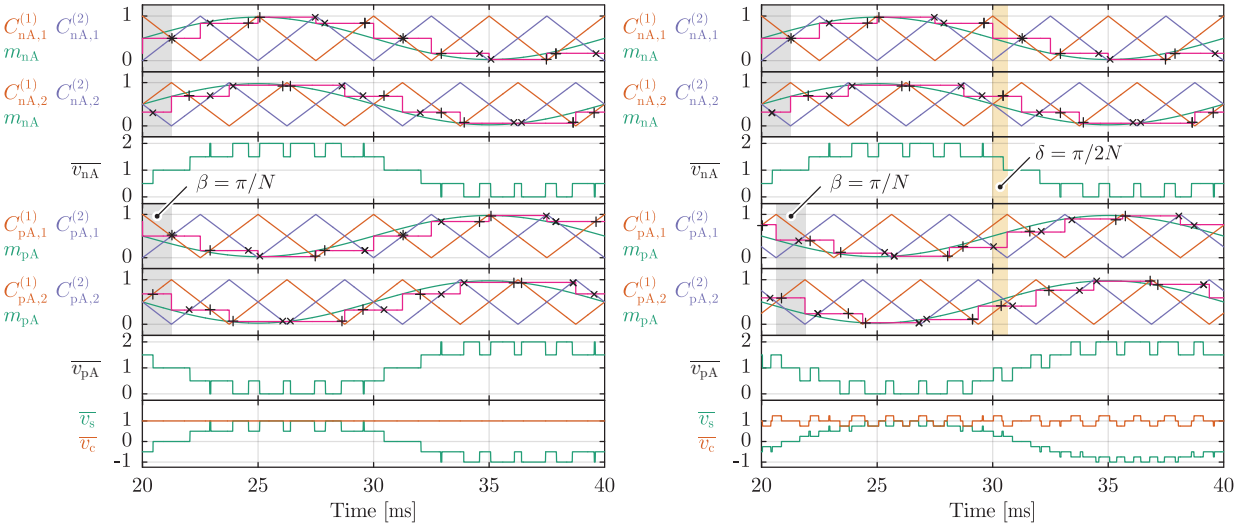


(b) $(2N+1)-$level modulation

Figure 10: Combination of carriers' displacement used in the conventional MMC, and applied to the exemplary circuit from Fig. 9, in order to obtain $N+1$ and $2N+1$ voltage levels seen from a leg AC terminals.

as $\delta = \pi/N$, which was derived in [17] for the case number of series connected SMs within a string is even, the number of voltage levels seen from the AC terminal of a leg can be increased, providing the so-called $(2N+1)-$level modulation depicted in Fig. 10b.

Degree of freedom provided by paralleling the SBRs can be exploited in order to improve the quality of a leg AC voltage even further. As presented in Fig. 11a, a leg AC voltage containing $MN+1$ levels can be obtained by setting the aforementioned offsets as $\delta = 0$ and $\beta = \pi/N$. In the exemplary case, number of parallel SBRs per branch was chosen as $M = 2$, therefore $(MN+1)-$level and $(2N+1)-$level modulations result in the same number of AC voltage levels. Nevertheless, from the bottom most plots of Figs. 10b and 11a, one can conclude that $(MN+1)-$level modulation can be considered favorable from the DC terminal



(a) $(N+1)-$ level modulation

(b) $(2N+1)-$ level modulation

Figure 11: Methods of improving the AC voltage quality provided by paralleling the SBRs. Namely, if a proper carrier angular offsets β and δ are chosen, AC voltages containing $MN+1$ and $2MN+1$ levels can be obtained. Please notice that the presented scenario refers to M and N both being even, whereas the other combinations can also be analyzed possibly requiring different setting of β and δ.

voltage standpoint. In other words, voltage component $\overline{v_c}$ realized by means of $(MN+1)-$ level modulation contains less harmonic pollution when compared to $(2N+1)-$ level modulation. Last but not least, a leg AC voltage containing $2MN+1$ levels can be synthesized by setting δ and β according to Fig. 11b. It is important to notice that some of the attempts (in the exemplary case, $(2N+1)-$ level and $(2MN+1)-$ level modulations) to increase the number of a leg AC voltage levels cause additional oscillations in the leg common-mode current and consequently converter DC link current (please, recall from section II that voltage components $\overline{v_c}$ affect the converter common-mode currents $i_{\mathrm{c,i}}$). Also, the cases presented above relate to the number of parallel SBRs and series connected SMs within a SBR being even. Parity of M and N has an impact upon the desired number of AC voltage levels to be realized, possibly requiring different setting of δ and β. However, strict mathematical proof of this statement falls out of this paper's scope due to lack of space.

V. Simulation results

Firstly, availability of a SM intended to serve the converter with the rated power of 0.5MW, being connected to the 3kV AC grid on one side and 5kV DC grid on the other side, is assumed. If 1.7kV IGBTs are selected for the observed application, number of SMs, operating with rated voltage of around 1kV, can be set as $N=5$.

Table I: Simulated converter parameters

Rated power (P)	1MW
Input voltage (V_{DC})	5kV
Number of SMs per SBR (N)	5
SM rated voltage (V_{SM})	1kV
SMs capacitance (C_{SM})	0.83mF
Number of parallel SBRs per branch (M)	2
SBR inductance (L_{br})	5mH
SBR resistance (R_{br})	60m
PWM carrier frequency (f_{c})	999Hz

In order to double the converter power, while using the same SMs, two SBRs have to be connected in parallel to form what has been referred to as branch so far. SM capacitance, ensuring the voltage ripple of $\pm 10\%$ around the nominal value, was set as $C_{\mathrm{SM}} = 0.83$mF [18]. Simulation parameters can be found in Table I. Since SBR inductances can easily be changed depending upon the converter configuration, to obtain the equivalent branch inductance of $\overline{L_{\mathrm{br}}} = 2.5$mH, SBR inductance was set as $L_{\mathrm{br}} = M\overline{L_{\mathrm{br}}} = 5$mH. In order to validate the ability of the proposed energy balancing control methods, $\pm 20\%$ mismatches were randomly included in the SBR inductances, as well as SM capacitances. $(2MN+1)-$ level modulation analyzed above was used to generate multilevel voltage waveform across the AC terminals of the converter. To test the converter dynamic performance, reference power profiles, defined in Fig. 12 were followed. Power references provided below were normalized with respect to the maximum converter power rating provided in Table I. To demonstrate the importance of the SBR energy balancing controller, its actions were disabled during the time interval $T^{\mathrm{OFF}}_{\mathrm{Wbal}} \in [1.5\mathrm{s}, 2.5\mathrm{s})$.

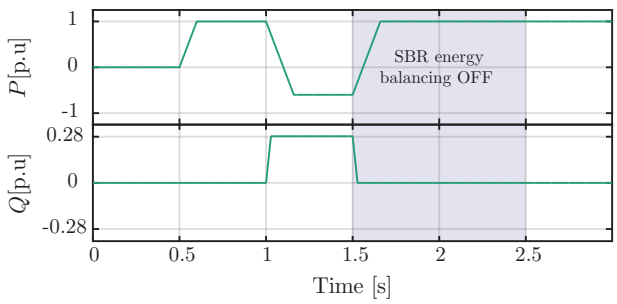


Figure 12: Power profile used to test dynamic operation of both converters

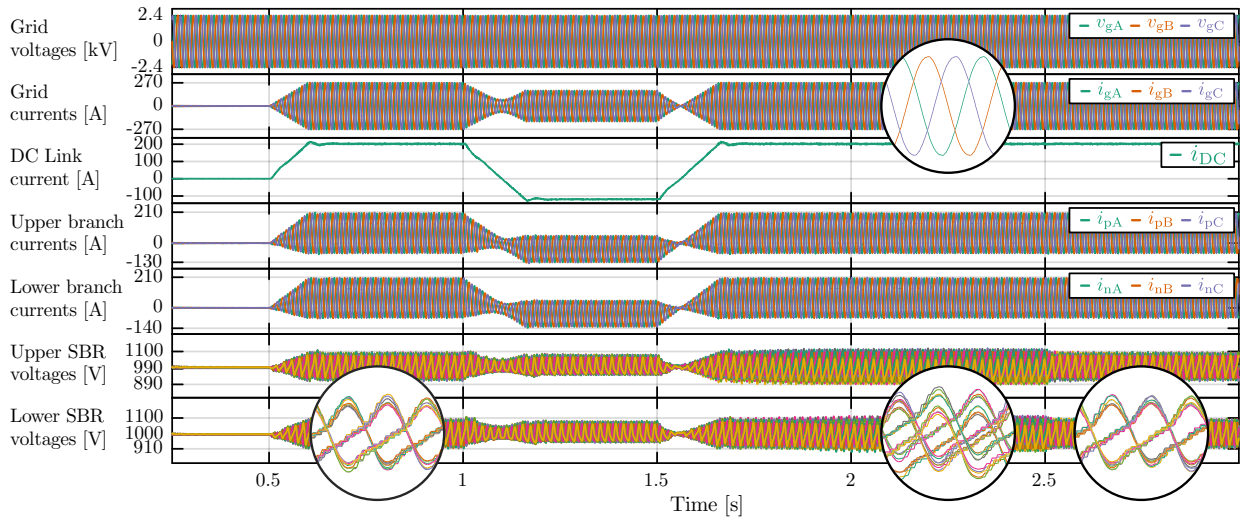


Figure 13: Operation of the converter utilizing two parallel SBRs within a branch

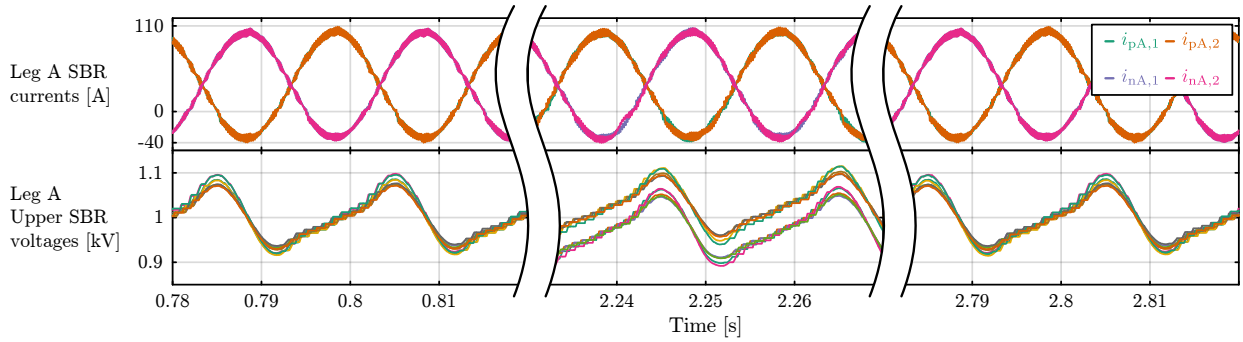


Figure 14: Leg A upper and lower SBR currents (top); Leg A upper branch voltages (bottom); In spite of the SBR currents being balanced, SBR voltages tend to diverge in case SBR energies balancing controller gets deactivated (middle part of the plot). Upon the reactivation of this controller, SBR voltages converge back to nominal values (right-most part of the plot).

Fig. 13 presents operation of the converter, utilizing two SBRs per branch, over the time span of $T_{\text{SIM}} = 3\text{s}$. The converter successfully tracks the desired active power profile, which can be concluded based on the presented DC link current i_{DC}. The lowermost plot presents voltages of the lower SBRs, whereas zoomed parts tend to showcase the contributions of the additional SBR energy balancing controller. It can be observed that, before this controller was disabled, SBR voltages remained perfectly balanced (the leftmost zoom). However, upon its deactivation at the time instant $t = 1.5\text{s}$, SM voltages of all the SBRs start to diverge (middle zoom). Please keep in mind that even though the SBR voltages show the tendency of diverging on these control terms, the total energy of every branch is still maintained at its reference level by the higher control layers. If the SBR energy balancing controller had been kept deactivated for longer, divergence would have become more emphasized, hindering the operation of higher control layers. At the time instant $t = 2.5\text{s}$, SBR energy balancing controller was reactivated, resulting in the balanced SBR voltages (rightmost zoom). Moreover, due to the closed loop control of the converter as a whole, currents injected into the grid do not get deteriorated even in the case of a slight SBR voltages divergence.

To provide a better illustration of the converter's internal quantities, Fig. 14 presents the leg A lower and upper branch currents, along with the upper branch voltages, during the subintervals being zoomed in Fig. 13. SBR currents remain balanced, owing to the actions of the SBR currents balancing controller, presented in Fig. 6. However, in spite of the SBR currents balance, SBR voltages divergence can be observed in the middle plot, which corresponds to the period at which the SBR energy balancing controller was still deactivated. It can also be seen from the right hand side plots that voltage ripple across the SM capacitors remains within the predefined boundaries of $\pm 10\%$ of the rated value if all the necessary controllers are enabled.

VI. Conclusion

This paper presented the method of extending power capacity of the MMC by paralleling its SBRs. Proposed control methods enable balancing of energies within the converter SBRs while keeping their currents balanced at all times. For an available SM design, rated power of the converter can be effortlessly multiplied without the need for a major redesign of the existing converter parts. Also, proposed SBR energy balancing method does not depend upon the number of parallel

SBRs. Consequently, scalability of the MMC depends exclusively upon the employed control platform, removing the SM hardware design constraints from the list of possible factors limiting the amount of power reached with an existing SM design. Simulation results have shown that proposed control methods guarantee stable operation of the converter, even in the case of SBR and SM parameters deviating from the rated values in the realistic range of $\pm 20\%$. Therefore, outstanding control robustness is provided. Compared to the other methods of increasing power capacity of the MMC, which are covered within the paper, paralleling of the converter SBRs avoids the need for complex SM design considerations as well as the additional parts, which can be redundant shall power extension of the original design not be the case. Thus, the problem of extending the power of the MMC, whilst utilizing the same SM design, gets shifted to the control domain allowing for more flexible, less engineering effort demanding and cheaper solutions.

Acknowledgment

This work has been funded by the Swiss Competence Center for Energy Research (SCCER FURIES) of the Swiss Innovation Agency Innosuisse.

References

[1] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in *2003 IEEE Bologna Power Tech Conference Proceedings,*, vol. 3, Jun. 2003, 6 pp. Vol.3-.

[2] R. Marquardt, "Modular multilevel converter: An universal concept for hvdc-networks and extended dc-bus-applications," in *The 2010 International Power Electronics Conference - ECCE ASIA -*, Jun. 2010, pp. 502–507.

[3] A. Nami, J. Liang, F. Dijkhuizen, and G. D. Demetriades, "Modular multilevel converters for hvdc applications: Review on converter cells and functionalities," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 18–36, Jan. 2015.

[4] J. V. M. Farias, A. F. Cupertino, H. A. Pereira, S. I. S. Junior, and R. Teodorescu, "On the redundancy strategies of modular multilevel converters," *IEEE Transactions on Power Delivery*, vol. 33, no. 2, pp. 851–860, Apr. 2018.

[5] M. Basic, P. C. Silva, and D. Dujic, "High power electronics innovation perspectives for pumped storage power plants," 2018.

[6] A. Volke, J. Wendt, and M. Hornkamp, *IGBT modules: technologies, driver and application*. Infineon, 2012.

[7] R. Hermann, S. Bernet, Y. Suh, and P. K. Steimer, "Parallel connection of integrated gate commutated thyristors (igcts) and diodes," *IEEE Transactions on Power Electronics*, vol. 24, no. 9, pp. 2159–2170, Sep. 2009.

[8] R. Grinberg, E. Bjornstad, P. Steimer, A. Korn, M. Winkelnkemper, D. Gerardi, O. Senturk, O. Apeldoorn, and J. Li, "Study of overcurrent protection for modular multilevel converter," in *2014 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sep. 2014, pp. 3401–3407.

[9] M. M. Steurer, K. Schoder, O. Faruque, D. Soto, M. Bosworth, M. Sloderbeck, F. Bogdan, J. Hauer, M. Winkelnkemper, L. Schwager, and P. Blaszczyk, "Multifunctional megawatt-scale medium voltage dc test bed based on modular multilevel converter technology," *IEEE Transactions on Transportation Electrification*, vol. 2, no. 4, pp. 597–606, Dec. 2016.

[10] F. Gao, D. Niu, H. Tian, C. Jia, N. Li, and Y. Zhao, "Control of parallel-connected modular multilevel converters," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 372–386, Jan. 2015.

[11] J. Pou, S. Ceballos, G. Konstantinou, G. J. Capella, and V. G. Agelidis, "Control strategy to balance operation of parallel connected legs of modular multilevel converters," in *2013 IEEE International Symposium on Industrial Electronics*, May 2013, pp. 1–7.

[12] J. Pou, J. Zaragoza, G. Capella, I. Gabiola, S. Ceballos, and E. Robles, "Current balancing strategy for interleaved voltage source inverters," *EPE Journal*, vol. 21, no. 1, pp. 29–34, 2011.

[13] A. Antonopoulos, L. Angquist, and H.-P. Nee, "On dynamics and voltage control of the modular multilevel converter," in *Power Electronics and Applications, 2009. EPE'09. 13th European Conference on*, IEEE, 2009, pp. 1–10.

[14] P. Münch, D. Görges, M. Izák, and S. Liu, "Integrated current control, energy control and energy balancing of modular multilevel converters," in *IECON 2010 - 36th Annual Conference on IEEE Industrial Electronics Society*, Nov. 2010, pp. 150–155.

[15] F. Kammerer, J. Kolb, and M. Braun, "Fully decoupled current control and energy balancing of the modular multilevel matrix converter," in *2012 15th International Power Electronics and Motion Control Conference (EPE/PEMC)*, Sep. 2012, LS2a.3-1-LS2a.3-8.

[16] A. J. Korn, M. Winkelnkemper, P. Steimer, and J. W. Kolar, "Capacitor voltage balancing in modular multilevel converters," in *6th IET International Conference on Power Electronics, Machines and Drives (PEMD 2012)*, Mar. 2012, pp. 1–5.

[17] K. Ilves, L. Harnefors, S. Norrga, and H. Nee, "Analysis and operation of modular multilevel converters with phase-shifted carrier pwm," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 268–283, Jan. 2015.

[18] K. Ilves, S. Norrga, L. Harnefors, and H. Nee, "On energy storage requirements in modular multilevel converters," *IEEE Transactions on Power Electronics*, vol. 29, no. 1, pp. 77–88, Jan. 2014.