Research and development of an intelligent particle tracker detector electronic system

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Abstract

In high energy physics, silicon particles detectors are widely used in tracking applications. They feature high-resolution measurements of the traversing particle positioning and frequently its energy. With the new possibilities introduced by technology scaling, the next generation of silicon detectors will be capable of real-time computing higher level information.
Within the scope of this thesis is discussed a novel silicon particle detection system, for the CMS experiment, capable of providing information regarding the particle direction and transverse momentum, in addition to simple geometrical positioning and energy measurements. This feature allows the event reconstruction and even the offline physics analysis to handle more advanced measurements. Introducing in the sensor readout ASICs the ability to perform a simple real-time analysis of the particle signatures, allows to locally reject information unnecessary for the event reconstruction, with a significant gain in terms of bandwidth and power consumption.
Studies have been carried out to identify the optimal architecture. At system-level, a simulation framework was developed to study and optimize the data processing algorithm and evaluate the more appropriate solution. A silicon prototype of the micro-strip readout ASIC incorporating all required functionalities for operating in the CMS experiment has been designed in a 65 nm technology. One of the major challenges of the design is introduced by the very harsh environment, characterized by a high ionizing radiation dose up to 100 Mrad and a low temperature around -40°C. Low-power and radiation tolerance design techniques have been employed to fulfill the very tight power requirement and to mitigate total ionizing dose and single-event effects. The ASIC performance has been characterized by different working temperatures, operating conditions, and radiation levels. For this purpose, a custom test bench and software was developed. The ASIC measurements show results in agreement with the simulations, proving to fulfill the requirements.

Résumé

En physique des hautes énergies, les détecteurs de particules de silicium sont largement utilisés dans les applications de tracking. Ils offrent des mesures à haute résolution du positionnement de la particule en traversée et souvent de son énergie. Grâce aux nouvelles possibilités offertes par la mise à l'échelle technologique, la prochaine génération de détecteurs au silicium sera capable de calculer en temps réel des informations de niveau supérieur.

Dans le cadre de cette thèse sera discuté un nouveau système de détection de particules de silicium, pour l'expérience CMS, capable de fournir des informations sur la direction des particules et la dynamique transversale, en plus de simples mesures géométriques de positionnement et d'énergie. Cette fonctionnalité permettra la reconstruction d'événements et même l'analyse physique hors ligne pour traiter des mesures plus avancées. L'introduction dans les ASICs de lecture des capteurs de la possibilité d'effectuer une simple analyse en temps réel de la signature des particules, permet de rejeter localement les informations inutiles à la reconstruction de l'événement, avec un gain significatif en termes de bande passante et de consommation électrique. Des études ont été menées pour identifier l'architecture optimale. Au niveau du système, un cadre de simulation a été développé pour étudier et optimiser l'algorithme de traitement des données et évaluer la solution la plus appropriée. Un prototype en silicium de l'ASIC de lecture des micro-stripes intégrant toutes les fonctionnalités nécessaires au fonctionnement de l'expérience CMS a été conçu dans une technologie 65 nm. L'un des principaux défis de la conception est introduit par l'environnement très dur, caractérisé par une forte dose de rayonnement ionisant jusqu'à 100 Mrad et une température basse autour de $-40°C$. Des techniques de design à faible puissance et à tolérance aux rayonnements ont été employées pour répondre aux exigences très strictes en matière de puissance et pour atténuer les effets de la dose ionisante totale et des événements uniques. Les performances de l'ASIC ont

été caractérisées par des températures de travail, des conditions de fonctionnement et des niveaux de rayonnement différents. Pour ce faire, un banc d'essai et un logiciel sur mesure ont été développés. Les résultats des mesures effectuées à l'aide de l'ASIC concordent avec les simulations, ce qui prouve que les exigences sont satisfaites.

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ADC Analog to Digital Converter , 4.5, 5.1–5.2

ASIC Application Specific Integrated Circuit , 2.0, 2.2–2.4, 3.0–3.9, 4.0–4.6, 5.0–5.3, 5.5–5.6, 6.0

barrel Concentric cylindrical layers centered in the in the nominal interaction point and located in the CMS tracker at $20\,\text{cm} < r < 120\,\text{cm}$, 2.2, 3.4, 3.8, 4.4

BX The instant at which the particles bunch are brought into collision. In the LHC, the BX rate is 40 MHz. , 1.0, 2.1, 2.3, 3.2, 3.8

BX-ID Bunch Crossing Identification Data

C4 Controlled Collapse Chip Connection, also known as Flip-Chip technology, is a method for interconnecting semiconductor devices with solder bumps deposited in the die area , 2.3, 3.5, 4.5–4.6

CAD Computer-aided design. It represents software that aim to aid in the creation, modification, analysis, or optimization of a design

CBC CMS Binary Chip (CIC). Is the strip sensor readout ASIC of the CMS outer tracker 2S-module

CIC Concentrator Integrated Circuit. It is the data concentrator ASIC of the CMS Outer Tracker PS and 2S modules for the phase-2 upgrade , 3.5–3.6, 3.8–3.9, 4.2, 4.5, 5.6

CML Current Mode Logic

CMOS Complementary Metal Oxide Semiconductor , 1.0, 2.3, 4.6

CMS Compact Muon Solenoid detector. It is a general-purpose detector at the Large Hadron Collider (LHC) 0.0, 1.0, 2.1–2.2, 3.2, 3.6, 4.2–4.3, 4.6, 5.0–5.1, 5.5–5.6

CMSSW CMS Software components , 3.7

cross-section The section normal to the beam direction outside of that the particle is not deflected. It can be considered as a measure of the interaction probability , 5.6

CSA Charge Sensitive Amplifier

CTS Clock Tree Synthesis, it is a step of the physical implementation flow , 4.6

D19C Firmware project that aimed to provide DAQ system for the CMS Phase 2 tracker upgrade , 5.1

DAC Digital to Analog Converter , 4.1–4.2,

4.5, 5.1–5.2, 5.5

DAQ Data AcQuisition system , 2.2–2.3, 4.2

DD Displacement Damage , 2.4

DL Delay Line , 4.2

DLL Delay-Locked Loop. Similar to a PLL where the internal voltage-controlled oscillator is replaced by a delay line , 4.2

DRV Design Rule Violation , 4.6

DTC Data Trigger and Control system of the CMS detector , 5.1

DUT Device under Test

DUV Design Under Verification , 3.6

ECAL Electromagnetic Calorimeter of the CMS experiment , 2.1

ECC Error Correction Code

EDA Electronic Design Automation, also referred to as electronic computer-aided design (ECAD) , 3.6

E_{DEP} Deposited ionizing energy

ELT Enclosed Layout Transistor. It is a layout technique to reduce the leakage current increase due to the charge trapped in the STIs for devices exposed to ionizing radiation , 4.6, 5.5

ENC Equivalent Noise Charge , 5.2, 5.5

end-cap Parallel disks centered in the in the z located in the CMS tracker at $z >$ 130 cm , 2.2, 3.4, 3.8, 4.4

ESD Electro-Static Discharge

FC7 flexible, µTCA compatible Advanced Mezzanine Card (AMC) for generic data acquisition/control applications , 5.1

FE Front-End , 3.5–3.6, 3.9, 5.2

FEA Finite Element Analysis

FIFO First In First Out circuit element

FPGA Field Programmable Gate Array , 3.2, 4.2, 5.1

HCAL Hadron Calorimeter of the CMS experiment , 2.1

HEP High Energy Physics , 1.0, 2.3–2.4, 3.6, 4.6

high-p_T high transverse momentum (p_T) particle. In this context it refers to particles with p_T>2 GeV/c , 3.2, 3.5–3.6, 3.8–3.9, 4.3

HIP High Ionizing Particle. In this context it refers to particles with an energy deposition in silicon greater than 1.4 times the average energy deposited by a MIP , 3.6–3.7, 3.9, 4.2, 4.4

HL-LHC High Luminosity Large Hadron Collider , 1.0, 2.1–2.2, 3.3, 3.6, 4.2, 5.0

HLT High Level Trigger system

HPD Hybrid Pixel Detector , 2.3

HV High Voltage biasing

Infinite loop i.e. link to page xvi.

INL Integral Non-Linearity , 4.2, 5.2

integrated luminosity The integrated luminosity over the operation time $\mathscr{L}$ defines the total amount of data recorded by an experiment , 1.0

IP Interaction Point or Intellectual propriety (according to the context)

IPbus A flexible Ethernet-based control system for xTCA hardware , 5.1

L1 Level-1 trigger system (hardware trigger) of the CMS detector , 2.2, 3.1–3.2, 3.5–3.6, 3.9

L1 data Raw sensor image transmitted

only when required by a L1 trigger

L1 latency latency between the transmission of a trigger request and the corresponding event occurrence. It corresponds to the time available for the L1 data processing , 2.2, 3.7

L1 rate Average occurrence frequency of the CMS Level-1 trigger request

LDD Light Doped Drain

LET Linear Energy Transfer. The amount of energy that an ionizing particle transfers to the material traversed per unit distance , 4.4, 4.6, 5.6, 6.0

Level-1 Level-1 trigger system (hardware trigger) of the CMS detector , 4.4, 4.6

LHC Large Hadron Collider , 1.0, 2.2, 3.5–3.6, 4.5, 5.6, 6.0

low-p_T Low transverse momentum (p_T) particle. In this context it refers to particles with p_T<2 GeV/c , 3.2, 3.5–3.6, 3.8–3.9, 4.3

LS3 Third long shutdown of the CMS detector to allow the upgrade operations

LSB Least Significant Bit

luminosity The events rate occurrence in a particle interaction is defined as $\frac{dN}{dt} = \sigma\ell$, where ℓ represents the instantaneous number of interactions per second, called luminosity while σ represents the cross-section of the interaction , 1.0

LV Low Voltage powering

macro-pixel pixel with high aspect ratio (i.e in the PS module is 100 × 1467 µm) , 3.4

MaPSA Macro Pixel Sub-Assembly, it represents the C4 assembly of 16 MPA ASICs over a single pixel sensor , 3.5

material budget the quantity of material in the tracker volume, that introduces a limiting factor for the detection ratios of particles that may interact with it and compromise what the detector is expected to recognize , 2.2

MIP Minimum Ionizing Particle , 2.3, 4.2, 4.4

MMMC Multi-Mode Multi-Corner analysis , 4.6

Monte Carlo A broad class of computational algorithms that rely on repeated random sampling to obtain numerical results , 3.6–3.8, 4.3–4.4

MOS Metal Oxide Semiconductor , 2.4

MPA Macro Pixel ASIC (MPA. Is the pixel-sensor readout ASIC of the CMS outer tracker PS-module 0.0, 3.0, 3.5–3.9, 4.0–4.6, 5.1, 5.3, 5.5–5.6, 6.0

MPA-Light Small scale, limited functionality prototype of the MPA ASIC , 5.5

MPW Multi Project Wafer , 4.6

nMOS n-channel Metal Oxide Semiconductor (MOS) device , 4.1, 4.4, 4.6

outer-tracker CMS tracker barrel layers and end-cap disk located at $r > 200$ mm , 2.0, 2.2, 2.4, 3.2–3.6, 4.0, 4.2–4.4, 4.6, 5.1, 5.5–5.6, 6.0

PCB Printed Circuit Board , 3.5, 4.6, 5.1, 5.3

Phase-2 Upgrade CMS detector upgrade during HL-LHC LS3 , 2.1

pileup in HEP experiments it represents the average amount of overlapped signals

in the event reconstruction 0.0, 2.1–2.2, 3.0–3.1, 3.6–3.8, 4.2

PLL Phase-Locked Loop. It is a control system that generates an output signal whose phase is related to the phase of an input signal , 5.1

pMOS p-channel Metal Oxide Semiconductor (MOS) device , 4.1, 4.4, 4.6

p-p Proton-proton collision , 5.6

pseudorapidity Kinematical variable of a relativistic particle defined as $\eta = -\ln\tan\frac{\theta}{2}$, where θ is the particle zenith angle referenced to the direction of the crossing beams , 2.1

PS module p_T-module that combines a silicon micro-strip sensor with a silicon-pixel sensor , 3.4–3.9, 4.0, 4.3, 4.6, 5.1, 5.5–5.6

PSP Power Skew Product

p_T Particle transverse momentum 0.0, 2.1, 3.2, 3.4–3.6, 3.8, 4.2–4.3

p_T-module Silicon detectors modules capable to provide transverse momentum measurements , 3.2, 3.4–3.5

Python An interpreted, high-level, general-purpose programming language

RDL Re-Distribution Layer , 4.6

RTL Register Transfer Level. It is a design abstraction which models a synchronous digital circuit in terms of the flow of digital signals (data) between hardware registers, and the logical operations performed on those signals , 3.6, 4.6

SDF Standard Delay Format (SDF) is an IEEE standard for the representation and interpretation of timing data for use at any stage of an electronic design process , 4.6

SEE Single Event Effect. Effects caused by one single ionizing particle striking a sensitive node in a micro-electronic device , 2.4

SET Single Event Transient. Time limited change of logical state caused by one single ionizing particle striking a sensitive node in a micro-electronic device , 4.6

SEU Single Event Upset. Change of logical state caused by one single ionizing particle striking a sensitive node in a micro-electronic device , 2.4, 4.4–4.6, 5.6, 6.0

SLVS Scalable Low Voltage Signaling. It is a differential signal transmission standard , 3.7–3.9, 4.6, 5.1, 5.3

SM Standard Model in particle physics is the theory describing three of the four known fundamental forces (electromagnetic, weak, and strong interactions, and not including the gravitational force) and classifying the known elementary particles , 1.0

SNM Signal to Noise Margin , 4.6

SOI Silicon On Insulator technology , 4.6

SSA Short Strip ASIC (SSA). Is the micro-strip-sensor readout ASIC of the CMS outer tracker PS-module , 1.0, 3.0, 3.5–3.9, 4.0–4.6, 5.0–5.3, 5.5–5.6, 6.0

SST Silicon Strip Tracker

STI Shallow Trench Isolation. Isolation which prevents electric current leakage between adjacent semiconductor devices , 2.4, 4.6

strip Detectors obtained by segmenting the doped side into strips over the full length of the detector , 1.0, 3.4

stub High-p_T particles primitives transmitted by p_T-modules , 3.2, 3.4–3.6, 3.8–3.9, 4.3, 5.3, 5.6

SystemVerilog IEEE 1800 standard hardware description and verification language used to model, design and simulate electronic systems , 3.6

TCL Tool Command Language. It is a high-level, general-purpose, interpreted, dynamic programming language , 4.6

TID Total Ionizing Dose, The cumulative damage of the semiconductor lattice caused by ionizing radiation over the exposition time , 2.2, 4.4, 4.6, 5.5

timewalk The difference in time between charge injection at a FE input and its detection , 3.6, 4.2

time-walk Time dispersion of a discriminated pulse due to the combined effect of the pulse heights spread and the single threshold discrimination

TLM Transaction Level Modeling abstraction , 3.6

TMR Triple Modular Redundancy. Circuit technique to increase tolerance to radiation related single-event effects , 4.6

ToA Time of Arrival of a particle , 2.3, 3.6, 4.2

ToF Time of Flight, in this context it refers to the particles time required to reach the silicon detector , 4.2

ToT Time over Threshold method to determine the amplitude of an analog signal. The signal is compared to a threshold and the duration of the output pulse is measured , 2.3, 4.2

tracker CMS sub-detector that allows reconstructing the particle trajectory and transverse momentum p_T in the 3.8 T magnetic field provided by the superconducting solenoid , 2.1–2.3, 3.0–3.6, 3.8–3.9, 4.2–4.4, 4.6, 5.0–5.1, 5.5–5.6

UBM Under Bump Metalization

UVC Universal Verification Methodology Verification Component , 3.6

UVM The Universal Verification Methodology is a standardized methodology for verifying integrated circuit designs , 3.6

VCD Value Change Dump

Verilog IEEE 1364 standard hardware description language (HDL) used to model electronic systems

Verilog-AMS It is a derivative of Verilog HDL language that includes analog and mixed-signal extensions (AMS) , 3.6

V_T Threshold voltage , 4.4, 4.6

1 Introduction

High energy physics (HEP) explores the nature of the particles that constitute matter and their mutual interactions. Particles, or related decay products, can be observed by their interactions with detectors capable of producing measurable signals. The history of particle detectors started more than a century ago. In the early days of particle physics, scintillation screens and photographic films allowed for the study of radioactivity. The "detection system" was the physicist eye [23]. Since that time, different technologies have been leading to essential steps in the particle physics field. The advent of the cloud chambers, invented by C. T. Wilson in the 1911 [24], made particle tracks directly visible and led to the discovery of the positron in 1932 [25] and of the K meson in the 1947 [26]. In the cloud chamber, when an energetic charged particle interacts with the supersaturated vapor, it results in a trail of ionized-gas particles that acts as a condensation center. The droplets are visible as "clouds" for several seconds.

A modified version of the cloud chamber, the bubble chamber, was developed by Donald A. Glaser in the 1952 [27]. As particles enter the chamber, a piston suddenly decreases its pressure, and the liquid enters into a superheated, metastable phase. At the passage of charged particles, the liquid vaporizes along with the ionizing track generating visible bubbles which density is proportional to the energy loss. The applied magnetic field imposes charged particles to travel along helical paths allowing for momentum measurements. A set of cameras allows capturing the particle trajectories. While some of the early prototypes were filled with beer [28], the CERN bubble chamber detector Gargamelle (1970-1979), filled with heavy-liquid and operating initially with a muon-neutrino beam produced by the Proton-Synchrotron and lately by the

Super Proton Synchrotron (SPS), leaded to the discovery of weak neutral currents in the 1973 [29]. The largest and last bubble chamber build (the BEBC), with its 3000km of developed and analyzed photo-film [30], enabled the discovery of D-mesons [31].

The first electronic detectors appeared much earlier with the Geiger-Müller tube [32] that uses the Townsend avalanche phenomenon to produce a readily detectable electric pulse triggered by a charge particle ionization. Only later, the scintillation counters started to be used together with photo-multiplier tubes (PMT), providing higher sensitivity [33]. After the introduction of Multi-Wire Proportional chambers (MWPC) in the 1968 [34] (proportional counter capable of providing positional information on particle trajectory) and successively of the Drift Chambers in the 1971 [35], electronic detectors started to feature increased *resolution*, finer *granularity*, and faster data read-out [36]. The possibility of reading out *electric signals* from particle detection that allows the usage of *computerized analysis* systems, defined the end of the bubble chamber era.

During the seventies appeared the Time Projection Chamber (TPC), a type of particle detector that utilizes a sensitive volume of gas or liquid to perform a three-dimensional reconstruction of particle trajectories. It found the primary application in the PEP-4 detector at SLAC [37]. More recent developments led to the micro-pattern gas detectors as MicroMegas [38] that utilizes metallic micro-meshes and GEMs (Gas Electron Multipliers) [39]. The latter has been used in many types of particle physics experiments starting from the Compass [40] experiment at CERN, in sub-detectors of today experiments and even in hadron therapy and radiotherapy [41].

Towards the end of the seventies, the possibility of using *semiconductor devices* as high precision tracking detectors started to emerge, representing a third major detector typology [36]. The first *micro-strip* silicon detector was published by the Pisa group [42] involved in charm quark production studies at CERN's SPS [43] accelerator. NA11/NA32 experiment at CERN build the first operational silicon-strip detector in 1983 [44] for tracking and vertex measurements.

The spatial resolution in the μm-range, the introduction of planar technology and the readout speed that allow measuring short-living particles, gave a strong impulse to the research on silicon strip detectors. The final boost to this technology arrived with the possibility to integrate electronic readout circuits and even dedicated readout ASICs

within the detector [45]. Micro-strip and pixel detectors represent today the leading technology for particles tracking. Particle detectors designed for modern accelerators often combine several technologies and complex readout and analysis systems.

The European Organization for Nuclear Research (CERN) was created in 1954 as a unified effort of European countries to provide a scientific facility for advanced research on particle physics [46]. It is today one of the world's largest and most successful scientific laboratories, as well as an outstanding example of international collaboration between its 22 member states and 8 associated members [47].

During the first operational runs, the Large Hadron Collider (LHC) [48] was successful in terms of discoveries. Among of all the achievements, the probably most notorious one was the discovery of a particle at about 125 GeV [49] consistent with the boson theorized by P. Higgs, R. Brout and F. Englert [50], [51], announced by the two general-purpose experiments: Compact Muon Solenoid (CMS) [52] and ATLAS (A Toroidal LHC ApparatuS) [53]. At the time of the LHC commissioning, the Higgs boson was representing the missing particle to be observed for concluding the standard model [54].

In the LHC, superconducting magnets accelerate protons up to a peak value of 7.0 TeV in the 27 km counter-rotating accelerator facility. In four crossing points, the beams are brought into collision with a center of mass energy of more than 14 TeV. A complex of several accelerators (Figure 1.1) allows reaching the target energies. At the four collision point are located the ATLAS, CMS, LHCb [55] and ALICE [56] detectors. More details about CERN and the LHC can be found in article [57].

The **events rate** occurrence in a particle interaction is defined as $\frac{dN}{dt} = \sigma \ell$, where ℓ represents the instantaneous number of interactions per second, called **luminosity**, while σ represents the cross-section of the interaction. The luminosity for a Gaussian beam distribution can be expressed in a form of:

$$\ell = F \frac{N_b^2 \gamma n_b f}{4\pi\epsilon\beta^*},$$

where N_b is the number of particles per bunch in the beam while n_b the number of bunches per beam and γ is the relativistic gamma factor. β^* represents the focal length at the collision point, ϵ_n is the transverse beam emittance and f is the frequency of

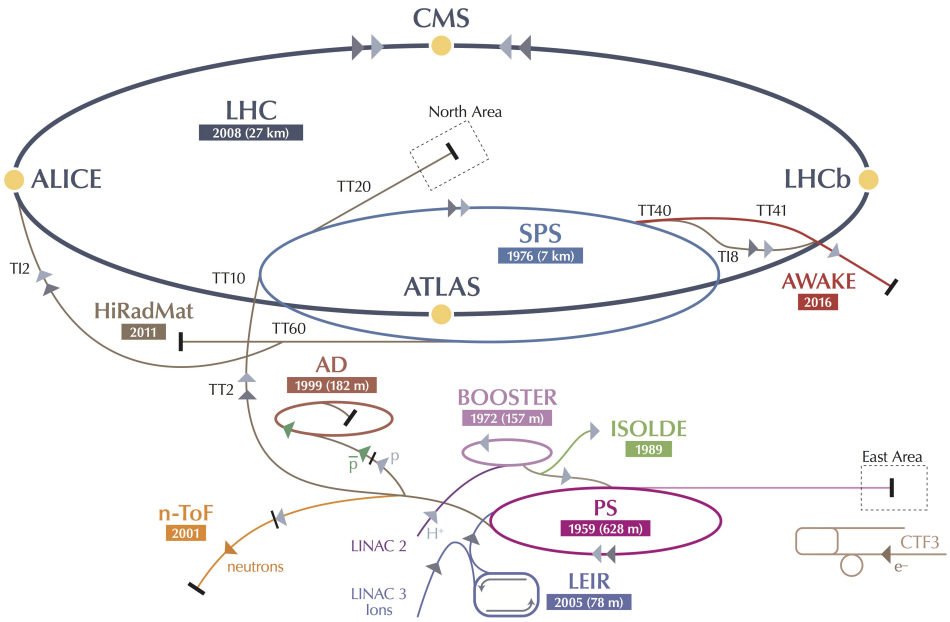


Figure 1.1. The complex of the LHC accelerators [60].

the revolution. F is a correction factor to represent the luminosity reduction due to the crossing angle at the interaction point [58]. The **integrated luminosity** over the operation time $\mathscr{L}$ defines the total amount of data recorded by an experiment. Clearly the luminosity is not constant within a run, it decays due the collisions themselves and due to inelastic interactions. The integrated luminosity is defined as:

$$\mathscr{L} = \int_0^T \frac{\ell_0}{(1 + t/\tau)}.$$

The instantaneous luminosity of the LHC reached the $2.1 \cdot 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ during the 2018 [59]. The expected integrated luminosity collected by the CMS experiment in its most recent run is $\sim 300\,\mathrm{fb}^{-1}$. The rate at which the particles bunch are brought into collision is 40 MHz and is called **bunch-crossing (BX) rate**.

Several others phenomena beyond the Standard Model (SM) need to be studied. For instance, the observation of neutrino oscillation does not conciliate with the standard model that assumes neutrino as massless. No particle was observed that can be responsible for dark matter cosmological observations. In the same time the matter-antimatter asymmetry needs to be explained. Some theories, for instance, the super-symmetry theory proposes extensions to the SM which might resolve some of these outstanding issues, and predict new particles with masses accessible at the

LHC [61].

For these motivations, a substantial upgrade of the LHC will extend its discovery potential by increasing the peak luminosity up to $5 \cdot 10^3 4\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$, and potentially to $7.5 \cdot 10^3 4\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ in the ultimate luminosity scenario [62]. The integrated luminosity expected for the High-Luminosity LHC (HL-LHC or HiLumi) operational time is $4000\,\mathrm{fb}^{-1}$. It will enable the experiments to enlarge their data sample by one order of magnitude comparing to the LHC baseline program [63]. The couplings of the Higgs boson to Standard Model fermions are currently measured with around 20% uncertainty. The large data set provided by the $4000\,\mathrm{fb}^{-1}$ integrated luminosity will allow reducing this uncertainty below 1% [61].

The CMS and ATLAS experiments will be able to provide extended studies of Higgs bosons and eventually to perform direct search for new particles that could solve open questions in HEP as the nature of dark matter, the stabilization of the Higgs mass, and the nature of the electroweak symmetry breaking [64]. It will enable the search for exotic processes as states with large missing transverse energy which could indicate the production of weakly interacting massive particles and as the signature of the lightest supersymmetric particles [65]. The LHCb experiment will pursue the observation of rare decays and CP violation in charm and beauty hadrons. Further studies on the quark-gluon plasma will be allowed by high luminosity Pb-Pb collisions in the ALICE experiment. The HL-LHC upgrade was approved in June 2016 and defined as one of the highest strategic priority by the European Strategy for Particle Physics (ESPP) [66].

For these reasons, the CMS detector will face a major upgrade towards the end of 2020 [67] which comprises the complete substitution of the CMS tracking system. The concept of intelligent particle tracking will be introduced in CMS. The front-end ASICs will be required to locally pre-select interesting physics events before the transmission to the back-end system, making possible the event-reconstruction in the high luminosity environment.

This thesis focuses on the studies and design of a micro-strip detector readout system and the ASICs that implement this concept.

This thesis is organized as follow:

- Chapter 1 (this chapter) gives a short historical introduction to particle detection systems, up to the now-days silicon pixel and strip detectors.
- Chapter 2 provides a theoretical background on the silicon detectors for HEP applications and introduces the requirements for the high luminosity upgrade of the CMS silicon tracker at CERN. State of the art is presented with emphasis on the main challenges. Finally, a short overview of the radiation effects on CMOS electronics is provided.
- Chapter 3 introduces the main goal of this thesis to combine for the first time in a high energy physics detector, particle trajectory and transverse momentum estimation, in addition to geometrical information and energy measurements and to locally pre-select interesting physics event before the transmission to the back-end system, making possible the event reconstruction in the high-luminosity environment. In the first part of the chapter, the advantages and the limitations of this approach are discussed. The second part of the chapter describes in details the studies and the design choices at the system level that lead to the implemented architecture. Besides, a simulation framework was developed to assist the studies and the design process of the whole readout system.
- Chapter 4 illustrates the design and implementation of the SSA, a readout ASIC of the silicon strip detector of the CMS Outer Tracker Pixel-strip (PS) module. The ASIC incorporates all the functionality and performance characteristics for operation in the final readout system.
- Chapter 5 describes the results of the silicon prototype characterization under different operating conditions. It presents the irradiation results and the estimation of the error rates expected by the operation in the target environment.
- In Chapter 6 the conclusions are drown and the possible improvements are discussed.

The definitions and the terminology necessary for the comprehension of the thesis are summarized in the glossary.

2 HEP detector electronics, challenges and state of the art

The Compact Muon Solenoid (CMS) experiment at CERN is foreseen to receive a substantial upgrade of the outer-tracker detector and its front-end readout electronics, requiring higher granularity and readout bandwidth to handle the large number of pileup events in the High-Luminosity LHC. For this reason, the entire tracking system will be replaced with new detectors featuring higher radiation tolerance and ability to handle higher data rates and readout bandwidths. The main challenges introduced by the upgrade are presented in this chapter.

Section 2.3 introduces the principles of silicon detector and the related readout electronics. Examples of state of the art tracking systems and their application in energy physics experiments are presented.

Radiation effects on electronics together with the power requirements represents one of the major challenge for the design of the ASICs operating in the innermost regions of the LHC experiments. Section 2.4 provides a short overview of the radiation effects on CMOS electronics.

2.1 The CMS experiment and the high luminosity upgrade

The CMS experiment is one of four CERN detectors situated on the LHC beam crossing points. Figure 2.1 shows a visualization of the detector. The particles generated in the collisions propagate radially, traversing the silicon tracker. The latter allows reconstructing the particle trajectory and transverse momentum p_T in the 3.8 T magnetic field provided by the superconducting solenoid surrounding the tracking system. Both the electromagnetic calorimeter (ECAL) composed by scintillating crystals, and the surrounding hadronic calorimeter (HCAL) located within the solenoid volume, allow evaluating the particle energy. The return yoke of the magnet is interleaved with the muon chambers. The detector is 21.6 m and features a diameter of 15 m. The overall weight is approximately $14 \cdot 10^6$ kg. A detailed description of the detector is reported in the CMS collaboration report [52].

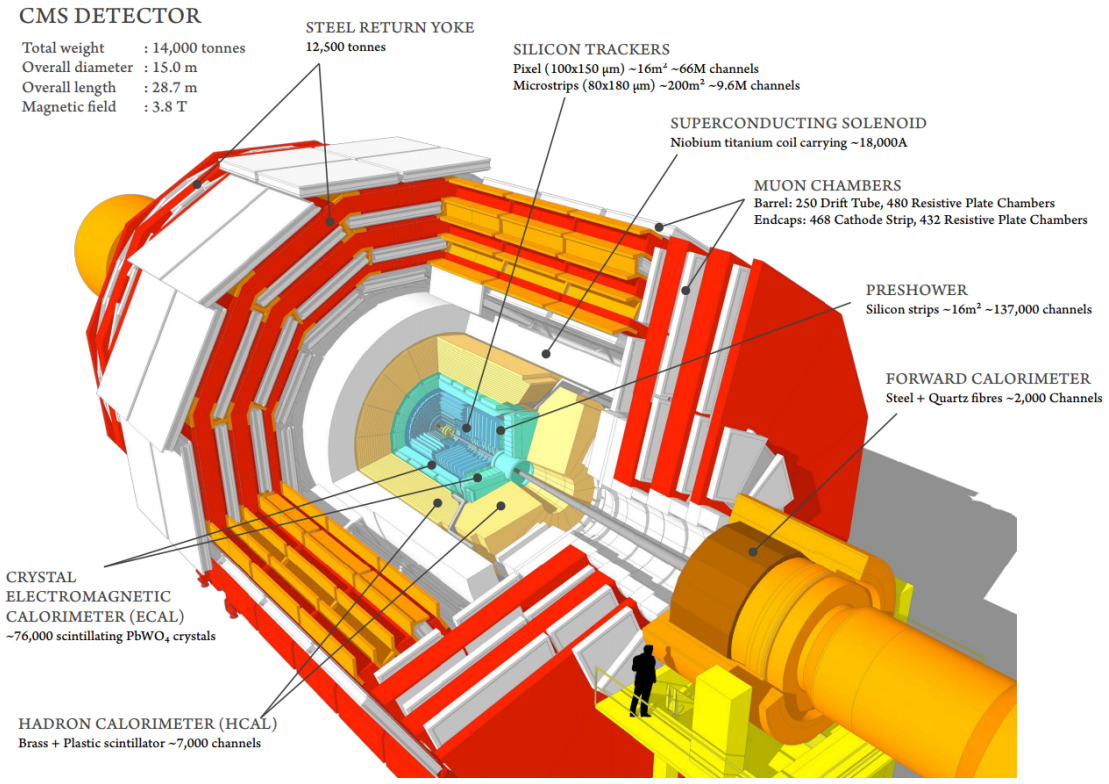


Figure 2.1. CMS detector visualization [68].

A coordinate system with origin in the nominal interaction point is defined as: $\hat{x}$ points towards the center of the LHC circle, $\hat{z}$ is tangent to the rotating beam pointing in the anticlockwise direction (longitudinal direction), $\hat{y}$ points vertical to form a right handed cartesian coordinate system. The $\hat{x}\hat{y}$ plane is called transverse plane. $\mathbf{p_T}$ and $\mathbf{E_T}$ refers respectively to the particles **transverse momentum** and **transverse energy** in the $\hat{x}\hat{y}$ plane. Due to the CMS detector structure, often a cylindrical coordinate system is adopted. r is defined as the radial distance from the nominal beam line ($\hat{z}$ axis), φ is azimuthal angle measured in the $\hat{x}\hat{y}$ plane from the x axis, θ is the angle measured in the $\hat{r}\hat{z}$ plane from the z axis. Additional derived coordinates are defined due to the direct dependency of physical properties: the **pseudorapidity** $\eta = -\ln(\tan(\theta/2))$ represents the particle angle relative to the beam axis and the **dip angle** is defined as $\lambda = \pi - \theta$.

The CMS detector requires a substantial upgrade in order to exploit the increase in luminosity provided by the HL-LHC [67]. This upgrade is usually referred as the Phase-2 Upgrade. A major update of the CMS detector is foreseen to cope with the $5 \cdot 10^3 4\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ luminosity of the HL-LHC and the cumulative radiation damages to the electronics.

At the same time, we can observe a significant overlap in space and time of signals due to different proton-proton collisions happening in the same BX. Most of this collisions are in the low energy range and not interesting for the physics analysis. They produce detectable signals that can affect the event reconstruction efficiency. In addition, the strong magnetic field, combined with the multitude of primary and secondary low energy particles, creates so-called "loopers". These particles may have a life time of more than one BX. The average amount of overlapped signals is called **pileup**.

Most of sub-detectors will feature increased granularity and resolution to mitigate the higher pileup in the event reconstruction. It makes more complex to associate particle traces to the primary vertex. The particle reconstruction in CMS is based on the particle-flow technique [69] and relies on the capability of correctly separating the charged-particle traces in the tracker, the energy deposition in the calorimeter and the measurements of the momentum in the muon system [70]. An increased granularity and resolution in energy measurement are necessary to maintain the same level of the detector performance in the extreme pileup conditions.

The rates of production data for the HL-LHC CMS detector is more than an order of magnitude higher compared to the current detector. The trigger and the readout system need to be upgraded as well to allow the analysis to make use of it.

2.2 The CMS silicon tracker

The detector located in the innermost region of the CMS detector is the silicon tracker [71]. It is composed of the multiple layers of the thin silicon sensors capable of evaluating the position of a traversing particle. The particle momentum can be evaluated at the back-end by computing the crossing coordinate in the different layers and measuring the curvature of the particle trajectory in the 3.8 T magnetic field provided by the superconducting solenoid. The inner part of the tracker allows for a precise reconstruction of the vertex due to its high spatial resolution.

The current CMS tracker is entirely composed by silicon strip particle detectors [72]. Micro-strips detectors are obtained by segmenting the silicon sensor over the full detector length to achieve spacial resolution along the φ direction. More than twenty different module geometries are currently implemented, with strip length between 80 mm and 200 mm and width ranging between 80 µm to 205 µm [73]. The total silicon detection area is $\sim 200\,\mathrm{m}^2$, divided into the 10 **barrel layers** (concentric cylindrical layers centered in the in the nominal interaction point and located at $20\,\mathrm{cm} < r < 120\,\mathrm{cm}$) and 12 **end-cap disks** per side [74].

The strip readout ASICs, called APV25 and implemented in a commercial 250 nm technology, operates in a triggered readout mode to drastically reduce the data rates [75]. In other words, the ASICs locally store the information during the time required for the Level-1 trigger computation. If no trigger signal is received within the latency time, the information is discarded. In the other case, the event is transmitted. The trigger decision is computed upon the information from the muon detectors and the calorimeter to select the most interesting events exclusively for the physics analysis, accordingly to the available bandwidth. The maximum average trigger rate is currently 100 kHz and the latency is 3.2 µs [71].

2.2.1 Requirements for the silicon tracker upgrade

In order to maintain or improve the physics performance of the CMS detector in the high pileup conditions of the HL-LHC, the entire tracking system must be replaced with new detectors featuring higher radiation tolerance and enhanced functionality allowing the front-end electronics or even the offline analysis in experiments to handle more complex features and measurements immediately [15].

The previous generation of the CMS tracker detector will be able to cope with the first few years of operation of the High Luminosity LHC. Accumulated radiation damage in the pixel sensors reduces the charge collection efficiency as well as the Lorentz angle, leading initially to decreased charge sharing among neighbouring pixels and hence to deteriorated spatial resolution, and eventually to reduced hit efficiency. Its intrinsic limitations bound the CMS Data Acquisition (DAQ) to a maximum Level-1 (L1) acceptance rate of about 100 kHz, with an available latency of 4 µ for the trigger decision.

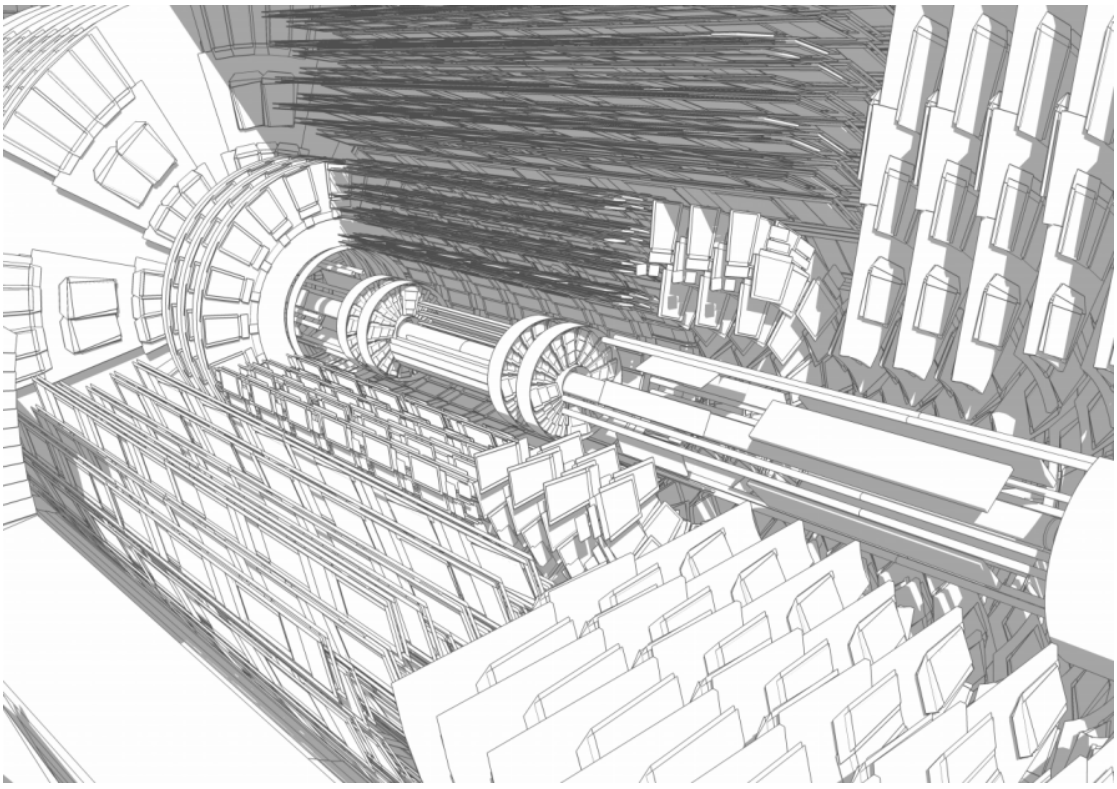


Figure 2.2. Visualization of the CMS silicon tracker for the high luminosity upgrade [68].

Higher trigger rates will allow transmitting to the experiment back-end a significantly higher amount of event data. A longer L1 latency (up to 12.5 µs) between the transmission of the trigger request and the corresponding event occurrence, will increase the time available for data processing. With the increased computation power and longer available time, the trigger system can handle more complex real-time calculations for the trigger decision.

In the previous generation of the CMS tracker detector, the highest instantaneous luminosity reached the record of 53 pileup events in a special 2017 high pileup run. In the upgraded CMS detector, an average of about 140 pileup events is expected for an instantaneous luminosity of $5.0 \cdot 10^{34}$ $cm^{-1}s^{-1}$. This value will rise to 200 pileup events in the ultimate luminosity scenario.

The larger pileup and the increase in particle density requires the tracker front-end ASICs to provide:

- Higher granularity – higher channel (either pixel or strip) density, will allow keeping the occupancy level at a few percents (< 3%) as in the current detector.
- Reduced material budget – the quantity of material in the tracker volume, that introduces a limiting factor for the detection ratios of particles that may interact with it and compromise what the detector is expected to recognize (see Section 2.2.2).
- Improved trigger capability – the ability to cope with the higher average number of collisions of the HL-LHC. In this case, the trigger rate should be increased from the current 100 kHz. The event reconstruction mostly identifies particles through its decay products. Searching for a specific decay pair has a significant probability of finding a random combination of other products with similar properties. It is generally referred as combinatorial background.
  A possible technique to overcome these limitations in the event reconstruction, enhance the rejection of the combinatorial background and improve the transverse momentum resolution, consists in utilizing information from the tracker itself in the trigger event reconstruction (see Section 3.4).
- Improved two-track separation – the present tracker is limited to highly energetic jets track finding performance due to the merging of particle hits in the pixel detector. The ability to identify and distinguish especially close particle tracks is necessary to exploit the large amounts of collision data.

- Resolution in the $\hat{z}$ direction – the higher granularity together with the requirement of having a good estimation of the z-coordinate of the hit, impose the use of pixelated sensors.
- Increased bandwidth – a drastically increased bandwidth and the introduction of a data compression procedures to accommodate the higher data rates allows the offline analysis of taking advantage of the $5 \cdot 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ luminosity.
- Improved radiation tolerance – due to the high increase in radiation levels, the electronics needs to guarantee the correct operation for the experiment within its expected lifetime (see Section 2.2.3).

2.2.2 Material budget and power constraints for the outer tracker

The quantity of material gives a limiting factor for the detection efficiency in the tracker fiducial volume (material budget) that may interact with the particles and compromise what the detector is expected to see. A quantification of the interactions can be expressed in units of radiation length, defined as the characteristic length that describes the energy decay of a beam of electrons. Figure 2.3 shows the material budget as a function of the pseudorapidity η for the current CMS detector and the expected value in the same units for the HL-LHC upgraded detector [9].

The material budget in the current detector reaches the 180% of the radiation length at η=1.5, mostly due to the stacked barrel layers of the outer tracker. It represents a significant limitation to the resolution of the electromagnetic calorimeter due to the energy loss in the layers traversed before to reach it. In addition, the particles scattering in this layers affects their trajectories and the tracking resolution.

Reducing the material budget does not come for free. It introduces a strong limitation in the material allowed for the the power distribution and in particular for the cooling system. The silicon sensors are designed to operate with a temperature below $-20°$C to avoid breakdown or thermal runaway of the sensor [76], and to limit the degradation due to radiation effects. The material budget requirements implies a strong constraint on the outer tracker modules power consumption and power density. The cooling system will be based on a CO_2 two-phase cooling to reduce the amount of passive material in the tracking volume [77].

As it will be highlighted in Section 3.4, the maximum power consumption and power

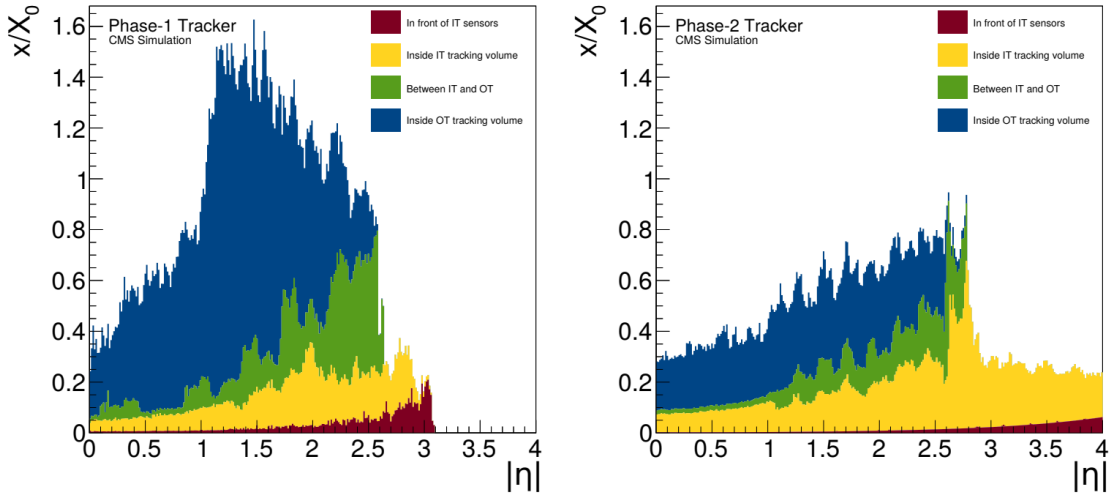


Figure 2.3. On the left the material budget in the current CMS detector volume expressed in units of radiation length as a function of the pseudorapidty η. On the right the expected material budget for the upgraded detector [9].

density for the ASICs discussed in Chapter 4 are respectively 250 mW and 90 mW/cm^2. An excess in power consumption would overload the power converters and the cooling structure, increasing the temperature of the module.

2.2.3 Radiation levels

Up to 200 pileup events is expected for an instantaneous luminosity of $5.0{\cdot}10^{34}\,\mathrm{cm^{-1}s^{-1}}$ for the upgraded CMS detector. The upgraded tracker is required to be fully efficient up to a target integrated luminosity of 3000 fb^{-1} [15], without any maintenance intervention for the outer-tracker. At such integrated luminosity, reached after 10 years of operation, the 1 MeV-neutron-equivalent fluence at the centre of the detector will be $2.3{\cdot}10^{16}\,\mathrm{n_{EQ}/cm^2}$. The Total Ionizing Dose (TID) will reach 12 MGy (1200 Mrad) [9], an unprecedented radiation level for advanced electronics, which is orders of magnitude higher of what expected in space applications.

Figure 2.4 and Figure 2.5 show the simulation results respectively of the expected fluence and the consequent collected dose in 10 years of operation and obtained using the Fluka simulation package [78], [79]. The results are expressed as function of the distance from the nominal interaction point in cylindrical coordinates.

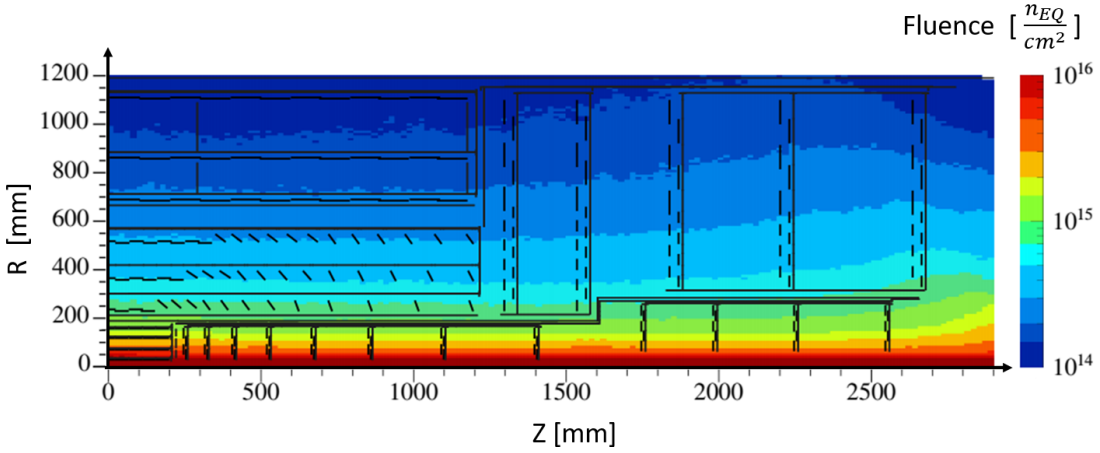


Figure 2.4. Integrated 1 MeV neutron equivalent particle fluence per cm^2 in the upgraded tracker detector [9].

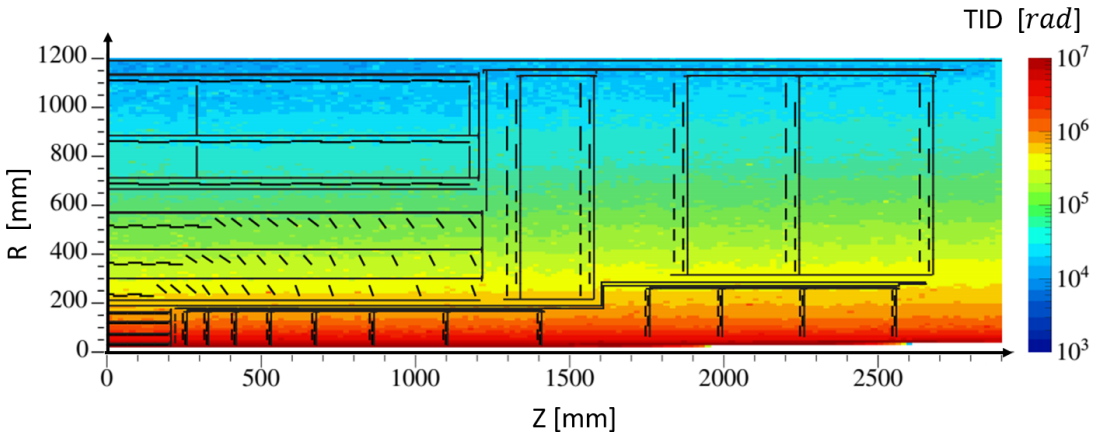


Figure 2.5. Total ionizing dose expected in the upgraded CMS tracker detector for an integrated luminosity of 3000 fb^{-1} [9].

It is evident that the particle fluence is strongly depends on the radius. The expected TID in the locations where the outer-tracker electronics will be installed, is in the order of 100 Mrad. Only custom electronics implementing high-radiation hardening techniques can operate in this environment. An additional 50% margin needs to be taken into account due to the the Fluka simulations results uncertainties on the radiation exposure [9].

2.3 Silicon particle detectors and technologies

Particle tracking detectors are based on the detection of a signal given by the free charge carriers generated by the passage of a charged particle through a medium as a semiconductor. Silicon detectors, compared to other particle detector types, combine a high precision and resolution, with a readout speed order of magnitude higher than many other systems. Signals generated by the energy deposition are directly available in electric form allowing for local analog and digital processing.

2.3.1 Silicon detector principles

The average energy loss of a charged particle traversing a material (silicon) is described by the Bethe-Bloch formula:

$$-\frac{dE}{dx} = 4\pi N_a r_e^2 m_e c^2 z^2 \frac{Z}{A}\frac{1}{\beta^2}\left[\frac{1}{2}\ln\frac{2m_e c^2\beta^2\gamma^2 T_{max}}{I^2} - \beta^2 - \frac{\delta(\gamma)}{2}\right],$$

where z represents the the incident particle charge, I - the mean excitation energy, T_{max} - the maximum kinetic energy, m_e - the electron mass, r_e - the classical electron radius, δ - the density effect correction, $\beta = v/c$, $\gamma = 1/\sqrt{1-\beta^2}$. The interesting particles for the standard physics present a momentum (GeV/c $\propto$ $\beta\gamma$) in the intermediate and higher regions, where the Bethe-Bloch formula well approximates the mean rate of ionization energy loss for charged particles (stopping power) [80]. The $1/\beta^2$ term is dominant at low energies, leading to a reduction of the stopping power for higher energies. At higher energies, a slow rise is given by the logarithmic term. The minimum of the deposited energy is located at $\beta\gamma \approx 3$. A particle detector in the target applications of the CMS tracker needs to be able to detect the minimum ionizing particle (MIP), or in other words to keep an equivalent noise level below this value. The Bethe-Bloch does not describe the low energy range where the particles have velocity on the same order of the orbital electrons leading to a drop of the stopping power.

Besides, the statistical fluctuation of the energy transfer per scattering needs to be considered. The energy loss probability distribution $f(\Delta;\beta\gamma,x)$ is described by the Landau distribution 2.7. Only a part of the absorbed energy leads to electron-hole pairs generation. The average number of $e^- h^+$ pairs (J) is related to the deposited energy $\Delta$by $J = \Delta/P$, where P represents the mean value of the energy needed for

ionization, equal to ~ 3.68 eV for the silicon [81]. The probability function f(Δ) are usually called energy loss distribution or straggling function. The most probable number of $e^- h^+$ pairs generated for a MIP in silicon is 76 per 1 µm. As a result of the high density of the silicon (2.33 g/cm^3), the average energy loss for a MIP is about 390 eV/µm resulting in 108 $e^- h^+$ pairs per 1 µm [82]. When designing a silicon detector, it is important to take in account the landau fluctuation to maximize the detection probability.

The basic principle of a silicon sensor (microstrip or pixel) is based on a highly doped silicon slice on a resistive substrate of the opposite polarity to form a diode structure. When an ionizing particle traverses the sensitive volume, it generates electron-hole pairs along its path. Due to the bias voltage applied to the sensor, for a p-sensor the holes drift to the p^+ doped strips while the electrons drift to the n^{++} backplane, or vice versa for an n-type sensor [83].

Free charge carriers are also thermally generated leading to unwanted leakage currents. The thermal generation is independent of the concentration. The rate of the recombination is proportional to the np concentration product and limited by the minority carriers. When an excess is induced by a particle passing through or by radiation, if no bias is applied, the thermal equilibrium is reached with an exponential decay which time constant depends on the concentration of the carriers in excess. For a reversely biased structure, the carriers are removed keeping the concentration below n^2 and leading to a current pulse at the contacts. The induced current can

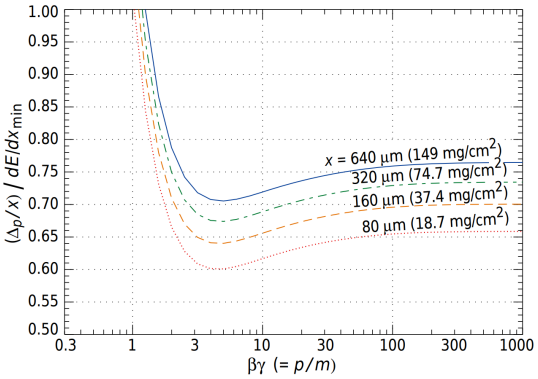


Figure 2.6. Most probable energy loss in silicon, normalized to the mean loss of a MIP [80].

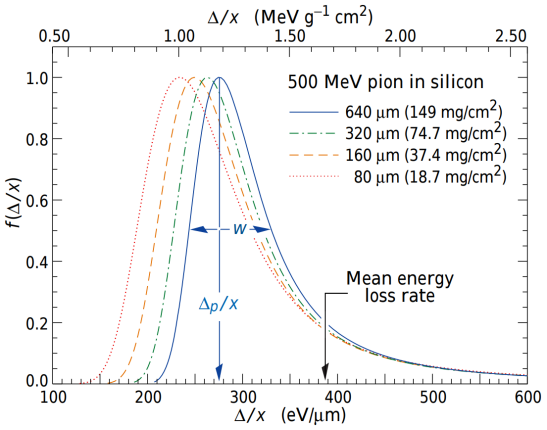


Figure 2.7. Straggling functions in silicon for 500 MeV pions, normalized respect to the most probable $\Delta p/x$ [80].

be read out by a charge-sensitive amplifier, to provide a signal proportional to the collected charge. As a result of the small energy band gap of the silicon (1.2 eV) and its material density, the ratio between the number of charge carriers produced and the traversing particle energy loss, is sufficiently high to be able to generate signals with a detectable amplitude.

The applied bias voltage is usually above the value required for full depletion to be able to utilize the whole available volume [84]. Considering the electrons and holes mobility at high temperature, the charge collection time is usually in the order of the ns, allowing adopting this kind of sensor in high event rate applications as the HEP experiments.

2.3.2 Micro-strip and pixel detectors

Microstrip detectors are obtained by segmenting the doped side into strips over the full length of the detector and with a pitch usually between few tens to few hundreds of µm. The segmented side is usually covered by a few µm layers of SiO_2 or Si_3N_4, which protect the wafer during fabrication but the detector itself as well. The aluminium contacts can be placed directly on the doped strips (DC coupled detectors) or on a thin oxide or nitride layer, in which case the doped strips are capacitively connected to the readout electronics (AC coupled detectors). The latter solution is more expensive, due to the additional steps needed in the production, however capacitive coupling prevents leakage currents to flow through the electronics. The electrical connection between the strips and the readout electronics is usually realized via thin wires (wire-bonding).

The planar process allows also the segmentation of one of the detector sides into a two-dimensional array of pixels. In this case an unambiguous 2-dimensional information about the position of the hit is achieved. The lateral size of pixels usually ranges between a few tens of µm and a few mm. The number of pixels and by that the number of readout channels increases linearly with the active area of the detector, while for silicon strip detectors, the number of readout channels increases with the square root of the active detector area. A higher cost of pixel detectors results from the complexity of the readout electronics and of the mounting techniques, especially when the pixel dimensions are small. The use of pixel detectors is nevertheless inevitable in

environments in which the detector occupancy is high, i.e. the sensor is traversed by many close-by particles. The use of strip detectors is in this case impossible due to ambiguities in the determination of the hit positions. Several categories of pixel detector are available and they can be divided according to the technology used for charge collection. Hybrid Pixel Detector (HPD) is the most used technology for HEP application [85]. It uses high resistivity silicon substrates like in the case of microstrip detectors. The sensor is divided in pixels with the same pitch as the readout chip and both are connected using a flipchip technology. This technique, also known as controlled collapse chip connection or its acronym, C4, is a method for interconnecting chips to external circuitry with solder bumps that have been deposited onto the chip pads.

In HPD, since the two parts are produced separately, they can be optimized and designed independently from each other. Also, any standard CMOS (complementary metal-oxide-semiconductor) technology can be used to design the readout electronics, so the scaling in the lithographic process can be exploited to build more advanced systems. The main disadvantage of this architecture is the cost of the flip-chip process, especially for detectors with very small pixels.

2.3.3 Front-end electronics

In the majority of the particle trackers, it is not required a direct measurement of the deposited charge. Such readout systems are comparing the front-end output signal with a single threshold, to identify the particle passage through the pixel sensitive area. In some applications, a amplitude measurements are required in addition to the spacial information. A possible approach consists of using a low-resolution flash ADC to convert the shaper pulse height. The result is directly proportional to the integrated charge deposited on the sensor.

A common solution that allows avoiding additional analog signal processing, consists of the measurements of the width of the digital pulse obtained by comparing the shaper output signal with the threshold. The particle charge information is obtained by measuring the time over threshold (ToT). Utilizing a constant current feedback leads to a linear relation between the charge and the ToT. An example of a readout ASICs that implement this techniques is the RD53A [86].

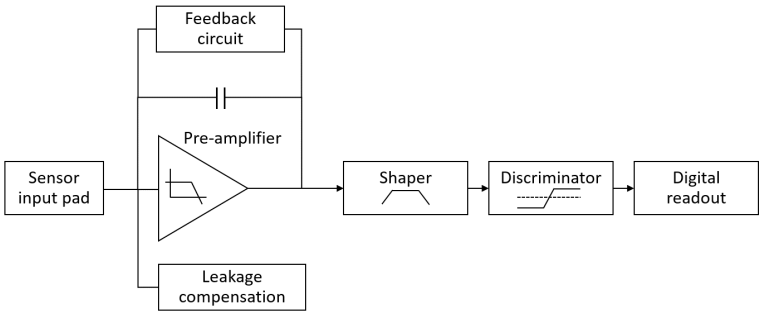


Figure 2.8. Block diagram of a typical front-end circuit implementation.

If it is not required a high resolution, the ToT can be measured by detecting rising and falling edge of the pulse with the available clock resolution. The limitation of such approach is the dead-time due to long signals and the clock jitter. Sometimes, to decorrelate the primary vertex information, could be convenient to add the time of arrival (ToA) evaluation aside to the ToT measurement, as it is implemented in the work of [87]. Applications like the CMS HGC readout ASIC combines ToT and ToA measurements together with amplitude measurements based on utilizing an ADC per channel.

A typical implementation of the front-end electronics is presented in Figure 2.8. The signal provided by silicon sensor with a thickness around $100-500\,\mu m$ is usually in the range of $\sim 10^4\,e^-$, with a collection time in the order of nanoseconds. A charge-sensitive amplifier in the front-end (FE) electronics reads out the charge signal and convert it into a voltage. The amplifier provide high open-loop gain and is enclosed with a capacitive feedback. Ideally it acts as an integrator where the closed loop gain is set by the feedback capacitor. A feedback circuit fixes the pre-amplifier DC operating point and removes the signal charges from the feedback capacitor after the amplifier response, allowing for the voltage pulse return-to-zero. In architectures where the pre-amplifier is DC coupled to the sensor, the sensor leakage current needs to be sourced by the electronics. A leakage compensation circuit, capable to sink the sensor leakage is connected to the pre-amplifier input (Figure 2.8).

To define the output pulse bandwidth, usually a shaper circuit and a filtering stage is introduced before discrimination. The purpose of the shaper is to improve the signal-to-noise ratio by filtering out high and low frequency components of the noise. Finally a discriminator allows comparing shaper output voltage pulse with a defined

threshold, usually set above the noise pedestal. The generated pulse width is directly proportional to the collected charge and can be used for ToT measurements.

2.3.4 Readout systems

The signals in the output of the front-end are digitalized, and the information is usually further processed on-chip before to be transmitted. According to the application, information on the particle charge may be required.

Another important parameter to take into consideration is the **occupancy** [s^{-1}]. It represents the fraction of channels (pixels or micro-strips) that contain hit information within a defined period. The instant occupancy defines the processing resources that need to be available to elaborate and transmit the information. On the other hand, its average will define the bandwidth requirements. The occupancy is directly proportional to the **hit-rate** [$s^{-1}cm^{-2}$], defined as the number of particle hits over the total sensitive area, within a defined period. The reference period can variate from tens of milliseconds for imaging and medical applications where the readout rates are in the order of $10-100$ frames per second, to nanoseconds in the case of the HL-LHC experiments, where $40 \cdot 10^6$ events per second are recorded (bunch-crossing rate).

In addition, another parameter to take into consideration is the information about the system efficiency. Due to front-end input noise, bandwidth limitations, or other non-idealities, a certain fraction of the particle information may be lost. The detector design keeps the efficiency over the minimum value required for the application.

Medical or X-ray imaging applications often implement a readout system based on the counting of the number of particle hits within the shutter opening interval [88], [89]. Synchronous or asynchronous counters per pixel allow collecting the cumulative statistics about the average number of particles hitting the sensitive area. The counters values are transferred to the ASIC periphery for further processing and transmission. Most of readout chips based on this approach implements a dynamic flip-flop system to form optimized shift register counters [90]. Lockup tables are used to decode the number of occurrences [91]. The overflow handling is often performed within off-pixel circuitry that periodically scans the array and increments peripheral counters [92].

Physics experiments where the input rates are sufficiently low can afford to implement

a full detector readout system transmitting either encoded or unsparsified information at the event rate. For instance, the LHCb [55] experiment will be upgraded to deal with a ten times higher luminosity while allowing for a full detector readout at BX rate [93]. This type of architecture is usually referred to as "trigger-less". Often it implements some real-time processing and encoding to compress the frame before transmission [94], [95].

A common technique to reduce bandwidth requirements and processing power consists of applying a zero-suppression. In other words it only processes the information coming from pixels where the signal amplitude is higher than a certain threshold. Some examples of recent trigger-less silicon detector readout ASICS are: CLICpix [96], Timepix [97], Velopix [98] and ToPix [99].

When detectors need to face higher event rates, it is not affordable to transmit the full meta-data. In this case, the procedure of on-detector data reduction needs to be applied. For this reason, the current CMS [52] and ATLAS [53] tracker detectors relies on a triggering system to select a fraction of the events to be transmitted and to achieve a feasible data rate towards the data acquisition system (DAQ). The approach is based on the fact that most of events do not contain information relevant for the physics and can be filtered out.

The trigger signal generation occurs in the experiment back-end. It is based on the online correlation of the information from other sub-detectors where the occupancy is significantly lower. In the current configuration of CMS experiment, for instance, the Level-1 trigger for the tracker detector is generated upon the information from the calorimeter [100]. Triggered readout architectures are required to locally store the information during trigger computation time (trigger latency), usually in the order of microseconds. To uniquely determine the required event, a fixed latency approach is adopted. If no trigger is received within the latency time, the information is discarded. In other case, the event is transmitted.

In some cases the hit information storage is implemented with a delay-line approach. All the particle hits from the front-end are delayed by the latency time with a chains of current-starved inverters [101] or a shift register (conveyor belt) [102], allowing multiple information along the delay element. When a trigger-request occurs, the delayed element is transmitted, otherwise it is discarded. Other architectures utilize

a memory element as a static or dynamic RAM to store a time-stamp of the events occurrence to associate the trigger to the event [103]. The time-stamp can be stored directly into the pixel logic or in the ASIC periphery.

Some architectures adopt a column drain topology [104] where the pixel data are transmitted as fast as possible to the end-of-column and the latency buffering is performed in the periphery. The possibility of distributing the processing unit within the pixels (or in cluster of pixel) was explored in several projects [105]. This approach results convenient in high occupancy scenarios allowing reducing the transmission rates between the pixel array and the periphery. The information is locally stored in the pixel array and transmitted only when required by the trigger system. Local domain isolation needs to be implemented to avoid digital noise injection in the analog front-ends due to the clock distribution and local digital processing [106].

2.4 Radiation effects on CMOS electronics

Radiation effects on electronics include any alteration of the expected behavior of an electronic device or circuit as a consequence of the interaction of a particle with the device. Different interaction phenomena and resulting effects are accounted within this statement. Particle interactions, or in general high energy electromagnetic radiation, represents one of the main threat for electronics design in the fields of aerospace, biomedical, and HEP [107].

In LHC experiments, the primary and secondary particles generated by hadron collisions together with the primary beam losses represents the leading cause of radiation effects. Besides, when the structures of the detectors are exposed to stray radiation, they become radioactive decaying in gamma-rays, beta particles and rarely neutrons. This radioactivity induced by the radiation process, is produced during the operation of the accelerator and it remains for a longer period. Although the overall amount of radioactivity induced in an accelerator will depend on the primary particles loss, the probability of producing a particular isotope will depend on the composition of the material struck, the spectrum of secondaries produced and the production cross section of the isotope concerned [108]. Roughly 30% of these inelastic hadronic interactions create long-lived radionuclides which contribute to the dose rate from induced activity in the experimental area [11].

It is essential implementing hardening techniques to cope with those effects, when designing an electronic circuit that operates in the proximity of the interaction point. Radiation dose-rates can reach values up to $\sim 10^6\,\mu Gy/day$ and 1 MeV-neutron equivalent fluence of up to $\sim 10^{15}\,n_{eq}/cm^2$ [9] (for the CMS outer-tracker; Section 2.2.3). As a comparison, the average dose rate in satellite orbital application and space missions ranges between $10^2 - 10^4\,\mu Gy/day$ [109].

Radiation effects on silicon circuits depend on multiple factors such as the type of interaction (dependent from the particle charge, energy, and mass) and on the properties of the circuit itself. Charged particles such as electrons or protons exhibit a Coulomb interaction with the silicon reticle atoms inducing ionization and atomic excitation. Massive particles such as protons or neutrons may cause displacement of atoms from their position in the lattice, an effect known as displacement damage (DD). DD is generally less dominant for MOS transistors [110]. Photons, depending on their energy, may interact by photoelectric effect, by Compton effect where an electron of the target atom is set free and a residual photon is emitted, or by electron-positron pair creation if the energy is above 1.024 MeV [111].

It is necessary to classify the radiation effects accordingly to their final effect on the functionality of the device. Radiation effects can be classified as cumulative and non-cumulative. In the first case the consequence of a single particle interaction can be negligible. They may accumulate over time leading to the variation of the device characteristic parameters and potentially to its failure. This category includes Total Ionizing Dose (TID) and displacement damage. On the other hand, in non-cumulative effects, the energy deposition due to a single particle traversing a device sensitive area may lead to a functional failure localized in time, for instance by modifying the logic state of a memory element or by triggering a latch-up. This type of effects, usually called Single Event Effects (SEE), are not predictable by modeling the device parameters degradation but only in statistical terms.

2.4.1 Cumulative effects: total ionizing dose and displacement damage

Cumulative effects can be divided in non-ionizing and ionizing. In the case of non-ionizing processes, the main outcome that can disrupt the performance of the elec-

tronic component is the displacement of atoms from their position in the lattice of a crystalline structure of the device by (DD) effect [112]–[116]. DD can be caused by electrons, hadrons (neutrons, protons, pions, etc.), heavy ions and γ-rays [117]–[119] and is a relevant phenomenon in several applications, e.g. space [120]–[122] and HEP [118], [123], [124], and for different semiconductor-based devices, e.g. solar cells [125]–[127] and image sensors [128]–[130]. However, MOS transistors are known to be less sensitive to DD effects (with a few exception for power MOSFETs in HEP applications [131]) and will not be described in the scope of this thesis. A comprehensive review of displacement damage effects can be found in [110] and [116].

While CMOS technology is substantially immune to DD, it can be extremely sensitive to cumulative-ionizing effects, i.e. total ionizing dose effects. MOS transistors exposed to ionizing dose can undergo a severe performance degradation due to the accumulation of radiation-induced charge in the oxides present in a CMOS structures [132]–[139]. It has been shown that the radiation-hardness of oxides increases sharply with decreasing thickness [140]–[143]. Therefore, while the radiation response of old CMOS technologies was dominated by the charge trapped in the gate oxides, more recent devices, with gate oxides a few nanometres thick, are mainly influenced by effects related to the presence of auxiliary oxides like shallow trench isolation (STI) oxides and spacers [137], [144].

The accumulation of charge in these oxides can provoke a substantial increase in the leakage current [145], [146], threshold voltage shift and variation in the transconductance [147], [148]. A comprehensive description of the TID-related effects in modern CMOS technologies can be found in [107].

2.4.2 Single event effects

Single event effects (SEE) are phenomena generated by a localized event induced by a single highly energetic particle (as an heavy ion) traversing the die. As a consequence, an immediate malfunctioning of one or more devices can be observed, eventually influencing the entire circuit, if it is not properly protected against. SEE effects are usually visible due to the energy loss of a particle traversing a sensitive area leading to Rutherford scattering (Coulomb interaction) with the lattice structure. The energy is transferred to the lattice as an ionization tail of free electron-hole pairs [76].

In the scope of the research work for the design of the GBT-SCA ASIC [11] and described in [10], was presented an overview of single event effects on CMOS electronics, as described in the following paragraphs.

Permanent single event effects

In CMOS technology, there are a number of intrinsic bipolar junction. These transistors can create problems when the combination of n-well/n-well and substrate results in the formation of parasitic p-n-p-n structures. Triggering these thyristor-like devices leads to a shorting of the VDD and GND lines, usually resulting in destruction of the chip, or a system failure that may only be resolved by power-down operation. This phenomena is usually can be avoided through layout techniques, nevertheless the onset of the parasitic p-n-p-n thyristor can be triggered by the ionizing energy deposition of an incident particle in a sensitive point of the circuit. This leads to an almost short-circuit current on the power lines, which can permanently damage the device. Sometimes, this condition can be local and the current limited (micro-latch), but the effect can still be destructive. The importance of this phenomenon in deep submicron technologies is limited according to the highly doped substrates and the trench isolation between wells [10].

Single event upsets and transients

Single Event Upsets (SEU), also called soft radiation errors, are not destructive, and happens whenever one or more bits of information stored by a logic circuit are overwritten by the charge collection following the ionization event. It is an instantaneous reversible modification of the logic state of a circuit sensitive node or elementary memory cell induced by the charge generated along the track of an incoming particle. SEUs become possible when the collected fraction of the charge liberated by the ionizing particle is larger than the electric charge stored on a sensitive node (a node whose electrical potential can be modified by internal injection or collection of electrical charges) [10]. The critical charge resulting in upset is approximately the noise margin of the charge stored on a capacitive information node. This charge scales directly with the gate area of the design at a given node bias voltage [149]. As the scale of integration increases, the amount of stored charge representing a logical value of information decreases, and information losses due to cell interactions with single

ionizing particles increase.

In addition, the charge deposition process changes the shape of the electric field in such a way that the amount of collected charge is greater than the amount, which would be collected in the equilibrium depletion region only: this phenomenon is called funneling and the length of the region involved in the charge collection is called funnel length.

Taking as an example an elementary cell of static memory in CMOS logic that consists of two inverting circuits where the output of each of them is connected to the input of the other circuit, the sensitive nodes are the transistor drains. An accumulation of positive or negative charge in such points may in fact lead to a reversing of the state of the logic cell, therefore the loss of the stored information [10].

A high-impedance node is much more sensitive to SEUs because an active circuit that provides current and restores the correct value does not always drive it. This is the reason why dynamic logic, where information is stored in high-impedance nodes, is much more sensitive to single event upsets than static logic [150].

SEU do not introduce a destructive effect and can be eliminated by rewriting the information lost in the memory cell, or for example repeating the algorithm executed in the case of CPUs. In complex circuits, an error induced on a logical value of information controlling a special function of the circuit can lead to wrong operations or the functional interruption of the whole system. Generally it is referred to this situation as Single Event Functional Interrupt. SEU is by far the main reason for failure of digital systems exposed to radiation environments [11].

SEU sensitivity increases with the scaling down of VLSI technologies: the critical charge is proportional to the node capacitance and to the supply voltage and both are scaled down with feature size. The sensitivity of a device within SEU can be evaluated through the critical charge, which is the minimum charge collected at a given node, required to upset the function of the cell [10].

3 Front-End electronics for a novel particle tracker architecture

Particle tracking detector for high energy physics needs a new readout technique to cope with the increase of the event rate foreseen for the High Luminosity LHC upgrade. In particular, the selection of interesting physics events at the first trigger stage becomes extremely challenging at high luminosity, not only because of the rate increase, but also because the selection algorithms become inefficient in high pileup conditions. A substantial increase of latency and trigger rate provides an improvement that is not sufficient to preserve the tracking performance of the current system. A possible solution consists of using tracking information for the event selection. This technique will allow to provide more accurate measurements of new particles and enable the observation of rare processes that occur below the current sensitivity level.

Given a limited bandwidth, the use of tracking information for the event selection requires the tracker detectors readout ASIC to perform a local data reduction by analyzing and transmitting self-selected information for every event. The front-end ASIC will include the intelligence for performing on-chip a continuous particle discrimination based on the transverse momentum and a local rejection of signals related to particles which are unnecessary for the event reconstruction. This novel concept, introduced for the first time in an HEP readout system, allows to drastically reduce the readout bandwidth, increase the tracker event reconstruction efficiency in the high luminosity, while enabling additional physics analysis possibilities.

The PS module, the detector unit that implement this concept, is composed of two closely spaced silicon sensors. The 6.8 T magnetic field, provided by the superconducting solenoid that surrounds the tracker system, provides a sufficient sensitivity

to measure particles transverse momentum over the small sensor separation. Such a module can be constructed using a pixel layer and a micro-strip layer sensor. This solution combines the resolution of the pixels with the lower power density of the strips. Two different readout ASICs, the SSA and the MPA, will allow reading out the sensors and performing the on-detector particle discrimination. High speed real time interconnects between readout ASICs are necessary.

Several architectures for the PS module electronic system have been studied and evaluated with physics events from Monte-Carlo simulations, to identify the implementation that minimize power consumption and bandwidth requirements while maximizing the particle recognition efficiency and reducing the information losses. For this purpose, a system-level simulation framework was developed to study and optimize the system architecture and to assist and verify the design of the multiple ASICs composing it. Featuring statistical stimuli generation and allowing linking physics Monte Carlo simulations platforms with industry standard EDA simulation tools, the framework represents an essential instrument for multi-chip verification with performance evaluation.

The module architecture proposed in this chapter as a conclusion of the studies presented, reaches an efficiency of > 98% in particle selection and a data reduction from $\sim 30\,\mathrm{Gb\,s^{-1}cm^{-2}}$ to $0.7\,\mathrm{Gb\,s^{-1}cm^{-2}}$ while limiting the total power density to $100\,\mathrm{mW\,cm^{-2}}$. Stub losses are evaluated as a function of the module location in the CMS detector, showing a maximum inefficiency of < 2% in the inner end-cap disk. The triggered data readout architecture is sized to guarantee no functionality losses (in the worst case scenario).

Publications related to this chapter: [6], [5], [12]

3.1 Particle tracking based on an intelligent pixel detector

The CMS experiment is a multipurpose detector designed for the precision measurement of leptons, photons, and jets, among other physics objects. At the target luminosity, the pp interaction rate exceeds 1 GHz. Only a small fraction of these collisions contain events that are actually interesting for the physics analysis and only a small percent of the huge amount of data produced for every event can be transmitted to the off-line storage system and further analyzed [100]. The "trigger system" is the component required to select events of potential physics interest [151].

To achieve a 10^4 data reduction from the 40 MHz collision rate to the 10^3 event per second limit of the storage capability, CMS implements a dual-layer trigger system. The level-1 (L1) trigger is implemented in hardware and allows for a $\sim 4 \cdot 10^2$ reduction factor based only on the information from the calorimeter and the muon chambers. The remaining $\sim 4 \cdot 10^2$ reduction is obtained as a result of contribution of the High-Level-Trigger (HLT) software that perform a reconstruction of the full event.

The event reconstruction that take place at the back-end, often looks for a particle not directly but through its decay products. Clearly looking for a specific decay pair have a certain probability of finding a random combination of other products which may appear similar to the analysis. This combinatorial background poses problems to the L1 trigger to the point where it is not possible to reconstruct the event only with the information from the calorimeter [76]. Most of the collision happening in a bunch crossing are in fact low-energy collisions, and are not interesting for the analysis. A fractions of the collisions produces high transverse momentum hadrons or decay products originating from high-mass primary particles. Future particle detectors, as the system presented in this thesis, could include already in the silicon detector readout ASICs the intelligence to real-time coarsely evaluate and filter the interesting information.

At the same time, the high pileup environment make this task even more challenging and increases the complexity of the selection algorithms. Different causes of pileup have undesired effect on the event reconstruction. The spacial pileup is due to the multiple collisions happening for each bunch crossing. Already in the current imple-

mentation of the CMS tracker, it represents the main source of particle hits on the silicon detector. In addition, due to the 4 T magnetic field and the high concentration of low energy primary or secondary particles, the loopers phenomena appears. This particles may generate multiple hits by looping within the tracker volume for multiple bunch crossing cycles without reaching the calorimeter.

A technique to overcome the consequent limitations and to keep the trigger rate at an acceptable level for the data acquisition electronics (< 1 MHz [15]) while not compromising physics potential, can consist in utilizing information from the tracker itself in the trigger event reconstruction.

The Particle Flow reconstruction algorithm implemented at the moment in the high level software trigger already successfully combines data from the muon chambers and from the calorimeter with transverse momentum measurements from the tracker to identify decay products. This implementation allows for a significant trigger rate reduction factor [152]. One of the most ambitious improvement of the CMS tracker anywais is to introduce the high resolution position and transverse momentum measurement from the tracker already at the level of the real-time hardware L1 trigger system. This will allow to apply more complex and powerful algorithms directly at this stage. Several studies [153]–[155] proved that including tracker information in the L1 trigger decision will allow for a significant rejection of the combinatorial background, will improve the transverse momentum resolution (i.e of jets), and will contribute to the mitigation of the pileup.

A further improvement can come from the possibility of having available information about the particle direction, making significantly easier the particle tracks reconstruction.

3.2 A new approach: The p_T module concept

To perform this operation, the tracker readout ASICs will no longer transmit the particle traces information only when required by the trigger system, but will need to provide constantly, for every collision, enough data to actively participate in the trigger decision that will take place in the remote FPGA farm.

The requirement of sending tracking information at each Bunch Crossing (BX) to-

gether with the higher granularity, leads to an significant increase of the bandwidth towards the experiment back-end. This limitation excludes the possibility to provide the particle charge measurements, and drives the system choice on a binary readout system (1-bit information per channel per BX which indicates if the charge deposited by the particle passing through the silicon sensor is above the threshold or not).

Even in this case, the full amount of raw data produced for every event only for the silicon outer-tracker (assuming 6 layer, the granularity requirement and no compression) would require a total bandwidth of $30 \cdot$ Pb/s to transmit the full raw event information. This is clearly not affordable, in particular considering the the computing power that would be required and due to the strict material budget (section 2.2.2) that introduce limits on the material allowed for power distribution, cooling and transmission lines.

The development of "intelligent" pixel sensors become necessary to real-time evaluate and select only the information that could be significant for the particle event reconstruction and for the L1 trigger decision. Not interesting information can be rejected already at the level of the readout ASICs, together with data compression capabilities.

Several techniques can be adopted for the discrimination. Among all, the more efficient approach between the ones evaluated may consist in measuring the transverse momentum p_T of the particle trajectory taking advantage of the 4 T magnetic field provided by the superconducting solenoid surrounding the tracking system. The curvature of the charged particle is directly proportional to its p_T.

Particles with a transverse momentum lower than a certain threshold can be locally rejected at the source without requiring to directly measure their charge with an ADC per each channel.

The p_T threshold should be chosen to provide a good rejection of the background and therefore a significant data reducing factor, but not too high to filter the interesting decay products with consequent impact in the analysis performances. Figure 3.1 shows the expected spectrum of the average number of tracks per event reaching a layer located at $r = 25$ cm from the beam line in simulated minimum-bias events [156], [157]. From the simulation carried out in [156] and in [158], results that, for minimum bias events, less than 10% of the particle tracks have a p_T greater than 1 GeV/c. Less than 3% feature a p_T above 1 GeV/c.

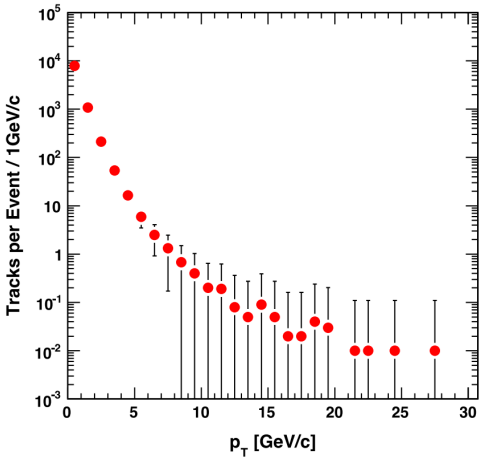


Figure 3.1. p_T spectrum of the average number of tracks per event reaching a layer located at $r = 25$ cm from the beam line, in simulated minimum-bias events [156].

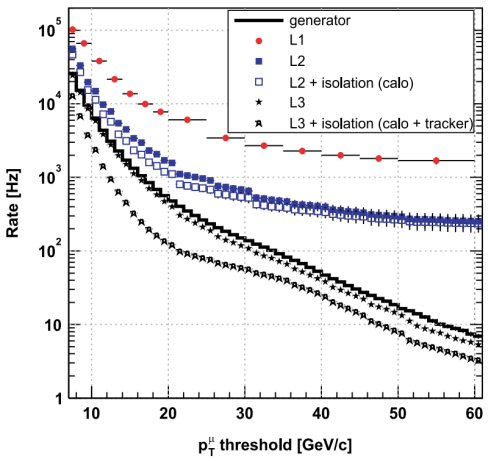


Figure 3.2. Estimated effect on the minimum trigger rate due to different p_T resolutions in the L1 and in the high-level muon trigger systems, as a function of the threshold applied [157].

Setting the p_T rejection threshold for instance at 2 GeV/c, together with a reasonable increase of the L1 trigger rate from 100 kHz to 750 kHz will allow to reduce by a factor 10 the data rate to be processed by the L1 trigger (and the bandwidth requirements), while still allowing the particle event construction in the High Luminosity scenario.

The front-end electronics thus must be able to recognize the particles with low-p_T and of applying a filtering. This feature can be achieved by measuring, not simply the position of the particle as in all silicon particle detectors, but also its direction. A possible solution to estimate the particle curvature and therefore their transverse momentum consists in detecting the particle charge deposition in two closely spaced planar silicon sensors as proposed the first time by S. Marchioro in [159], [160].

The 4 T magnetic field of CMS provides sufficient sensitivity to measure the p_T over a small sensor separation of few mm, enabling the use of this approach in the entire radial range above 20 cm from the interaction point. The high-p_T particles primitives transmitted will be named as **stubs** in the following paragraphs, while the hardware unit implementing this concept will referred as p_T-module.

The L1 track finding happens at the back-end. A track is generated combining the stubs received by the front-end modules of the different layers. The tracking-trigger computes track primitives with a dedicated timing window of ~ 5 µs. The information

can than be merged with the energy information provided by the other sub-detectors. The whole L1 latency will be required to be <12.8 µs [15].

3.3 Requirements and choice of the silicon sensor

The currently installed silicon-strip tracker sensors were designed to guarantee 10 years operation and to resist to a peak instantaneous luminosity of $10^{34}\,\mathrm{cm}^{-1}\mathrm{s}^{-1}$. The upgrade to the HL-LHC will not only increase the instantaneous luminosity by a factor five but also create an even harsher radiation environment [161]. The sensor will be exposed to a fluence up to $15\cdot10^{15}\,n_{\mathrm{eq}}\mathrm{cm}^{-2}$, a factor ten larger than the design requirement of the present tracker. The performance of p-in-n float zone sensors degrades too much in such conditions. Sensors with electron read-out are more robust in terms of high field effect after irradiation and provides higher charge collection than p-in-n sensors. According to the studies described in [161] and in [162], test structures were implemented on multiple materials in order to study and identify the more suitable material and technology for particle detection in the outer-tracker environmental conditions.

A critical point in the choice of the sensor technology is the charge collection, the noise behavior and the isolation between adjacent pixels/strips. This last point needs to be taken into account with relation to the cumulated dose due to the increase in the charge sharing effect. In addition, the bias voltage requirement needed to reach full depletion and extract a signal with a large enough amplitude to be readout.

Most of present-day semiconductor detectors are based on reverse biased p-n junction. The space charge region of the reverse biased p-n junction (depletion zone) forms the detection volume. [163] The electric field produced by the externally applied bias voltage ensures collection of the created charges on the electrodes and thereby produces a current signal. The width of the depletion zone depends on the concentration of n-type and p-type dopands and on the resistivity of the material. For the non-uniformly doped junction like a p^+ region on lightly doped n-type material, the width of the depletion zone if function of the bias voltage V_B, the resistivity of n-type material ρ_n, the electron mobility μ_e and the permittivity of silicon ε according $d = \sqrt{2\cdot\varepsilon\cdot\rho_n\cdot\mu_e\cdot V_B}$.

The signal created by a high-energy particle in a 300 μm thick, fully depleted silicon de-

tector has a Landau distribution with the most probable value around 22500 e^- [163]. For a 300 µm thick fully depleted silicon detector the collection time, i.e. the width of the current pulse to be readout by the electronics, is typically of the order of a few nanoseconds. The charge collection time depends on the electrical properties of the semiconductor material, the detector thickness, as well as on the applied bias voltage. Working with bias voltages higher than the full depletion voltage (over-depleted detectors) can reduce the charge collection time significantly, however increasing the bias voltage might lead to higher dark current and an increase of noise.

In practice the silicon detector thickness can vary between 100 µm to 500 µm depending on the application. These boundaries are determined by the mechanical properties of silicon (minimum achievable thickness for large detector area) as well as on the maximum affordable charge collection time, which is longer for thicker detectors.

The final choice of adopting a thin sensors of 200 µm was taken considering the advantages in terms of reduced leakage current compared to a thicker sensor, and in particular in order to reduce the material in the tracking volume [18], [19]. For the same reason in fact the front-end readout ASICs will be required to be thinned down to 200 µm and directly flip-chip bonded or wire-bonded without the usage of a package or interposer.

3.4 The p_T modules in the CMS outer tracker

As described in Section 3.8, the CMS outer-tracker will be composed in the region of $|z| < 1200$ mm by 6 cylindrical barrel layers to provide sufficient event reconstruction capability. In addition the barrel will be complemented by five "end-cap" double-discs, in the region of $1200 < |z| < 2700$ mm. Modules will be installed between $r \approx 21$ cm and $r \approx 112$ cm [15].

The selected number of sensitive layers is the minimum value able to ensure sufficiently robust track finding performance for the L1 trigger. Extensive studies performed with different detector configurations [165] have shown that with only five module layers the track finding performance for the L1 trigger would be heavily affected as soon as some parts of the detector become inefficient, while with six layers the performance is robust with respect to inefficiencies affecting one layer [166].

In order to optimize the amount of material in the tracker volume was decided to divide the outer-tracker in two zones. Only the three innermost layers ($r \in [200, 600]$ mm from the nominal interaction point) will will be able to evaluate the particle trajectory according both the ϕ and the z coordinates. The three outer layers ($r > 60$ cm) instead will be able exclusively to produce stubs and triggered data relative to the particle trajectory according the ϕ coordinate. For this reason, two different flavors of p_T-modules will be developed: the 2S modules and the PS modules.

The **Strip-Strip (2S) modules** will be composed by two micro-strip sensors of $10 \times 10\,cm^2$. The strips are disposed parallel to each other. The total sensitive area is $\sim 150\,m^2$. The connectivity between the sensor and the 2S Front-End hybrid [167] is implemented via wirebonds at one of the sensor extremities. A strip readout ASIC called CBC [168] allows to readout the charge deposition on the silicon sensor and

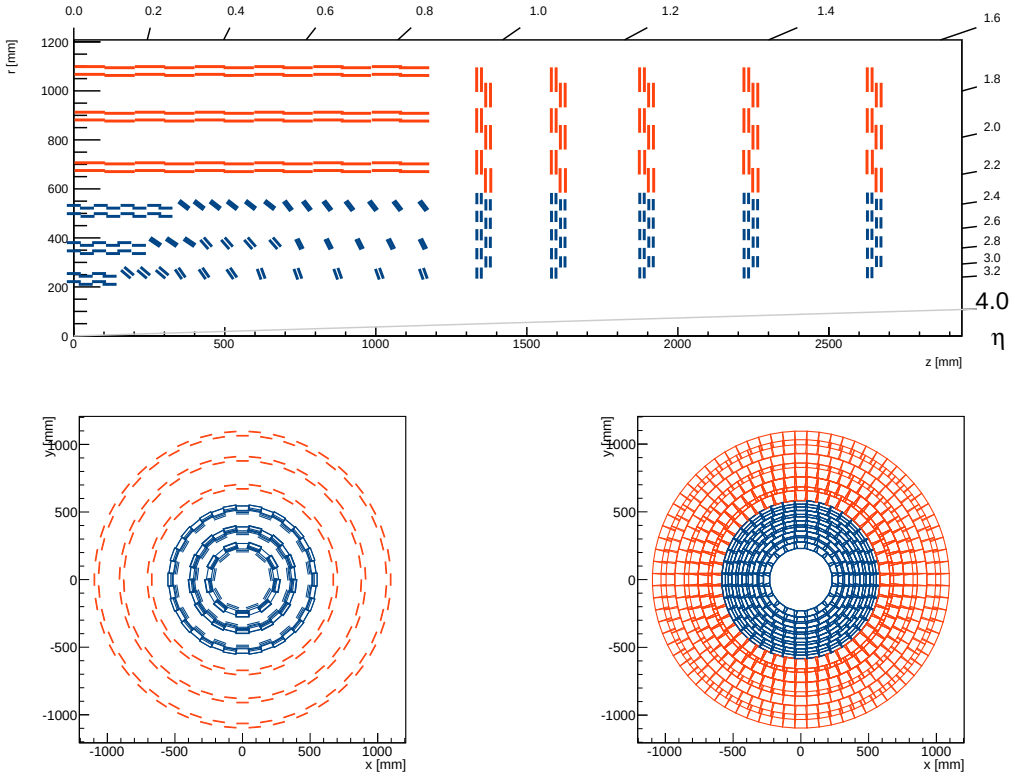


Figure 3.3. Tracker layout and p_T modules disposition. The figure on top shows the r-z view of the tracker, the left figure represents the x-y section of the barrel layers, the right figure shows the projection of the tracker end-cap disks. The blue lines correspond to the PS modules while the red lines to the 2S modules. Coordinate (0,0) is the nominal interaction point [164].

transmit encoded information to the tracker back-end. A single service hybrid carries a 5 Gb/s tranceiver (lpGBT [169]), an optical converter (VTRx+ [170]), and the DC/DC converter [171] that provides power to the module electronics.

The **Pixel-Strip (PS) modules** are composed of two different planar silicon sensors of $5 \times 10\,\mathrm{cm}^2$. The first layer is segmented in 1920 strips. The second layer instead is composed by 30720 macro-pixels of 100 µm×1.5 mm size. The electrical communication between the pixel sensor and the readout ASIC is implemented via C4 bumps. The pixel dimension was selected to allow the usage of a standard industrial flip-chip bumping technology process with consequent acceptable prototyping and scale production costs. As in the case of the 2S module, the connection between the micro-strip sensor and the strip readout ASIC can be implemented via wire-bonds between the sensor extremity and the front-end hybrid [172] on which the ASIC will be directly bumped. A 10 Gb/s serial transceiver [169] and the DC/DC converter [171] will be located in the module assembly. The total sensor area for the PS-module layers amount to $60\,\mathrm{m}^2$.

Figure 3.3.a shows one quarter of the tracker Layout $r-z$ section (in cylindrical coordinates) and the modules disposition within the volume (r represents the radial distance from the collision point while z represents the projection of the distance on the direction longitudinal to the proton beam. The blue lines correspond to the PS modules disposition while the red lines to the 2S modules. The usage of three pixelated sensor layers provide sufficiently precise measurements of the z coordinate. At the same time, the three additional strip-only layers able to estimate the particle transverse momentum are necessary for the track finding, offering enhanced robustness for the pattern recognition in a more cost effective way than extending the usage of pixel sensors to all the six layers. The PS-modules in all the tracker volume would in fact imply higher power consumption and higher material needed for the cooling.

Several possible variants have been modeled and studied [173]. In particular different geometries with different number of barrel layers, with or without end-cap, with different number and sizes of the end-cap disks. The solution shown in figure 3.3 is selected as the baseline for the design of the outer-tracker, since it provides efficient use of the silicon sensors while providing good tracking performance, low material budget and acceptable costs [173]. All the end-cap disks covers down to the lowest possible radius, to be compatible with an extension of the tracking acceptance up to

$\eta = 4$, while in the present tracker, no silicon sensor are placed at $\eta > 2.54$.

As evinced by Figure 3.3.b, the outer-tracker will consist in 15508 detector modules of which 8424 with the 2S flavor while 7084 with the PS flavor and will feature $218 \cdot 10^6$ pixels and $47.8 \cdot 10^6$ strips. Different values of the gap between the two sensors of a module are needed, in addition to a programmable acceptance window in the front-end ASICs, in order to implement a coherent p_T filtering in the whole outer-tracker volume. For this reason PS modules will be realized in three variants, with 1.6 mm, 2.6 mm and 4.0 mm gaps between the midplanes of the active volumes of the sensors.

3.5 The Pixel-Strip (PS) module design

The upgrade of the CMS tracker for the High Luminosity LHC, as described in Chapter 3, adopt an innovative approach for the particle finding, drastically reducing the transmission bandwidth by locally analyzing and rejecting information not necessary for the event reconstruction. The primary challenge for this system is the requirement of participating in the L1 event reconstruction requiring to implement an algorithm for stub finding which correlates the strip and pixel signals, and the development of a readout architecture to provide the found stubs at every event to the L1 trigger system at the 40 MHz bunch crossing rate. For the first time data coming from a tracker will be used in the L1 trigger decision of a high luminosity hadron experiment. Among the modules for the outer-tracker described in the CMS Technical Proposal [15], the Pixel-Strip modules are more technologically challenging and will combine a strip sensor with a pixelated one.

To match the requirements of the tracking performances, the PS-module layers will combine a sensor composed by 100 µm × 1.5 mm macro-pixels with a sensor composed by long strips of 2.5 cm and a pitch of 100 µm [9] to achieve a lower power density. Those values allow excellent performance in terms of spatial and p_T resolution for the L1 track finder and are driven by limitations in the bump density of the controlled collapse chip connection (C4) technology adopted for the PS-modules.

Figure 3.4 shows a simplified view of the readout electronic that will compose such a system, while Figure 3.5 summarize the role of the p_T-modules in the future CMS tracker readout scheme. A Front-End (FE) stage discriminate the particles hits accordingly to their charge deposition. The information from both layers is then digitalized

and transmitted including:

- A continuous transmission, for every event, of encoded information of particles with high transverse momentum towards the experiment back-end. The front-end electronics correlates the signals collected in the two sensors and select pairs compatible with particles above the chosen p_T threshold (stub) rejecting information not significant for the track reconstruction.
- A triggered readout. The complete raw event needs to be stored in the front-end readout ASICs and transmitted only when required by the trigger system. Assuming an average trigger rate of 750 kHz, around 2% of the events should be entirely transmitted with lossless encoding.

The combination of two sensors requires the design of two different ASICs, mostly due to mechanical assembly with the different types of sensors. The Macro Pixel ASIC, namely **MPA**, will be the pixel readout chip featuring on-chip real-time particle discrimination with trigger-less and zero suppressed readout. The Short Strip ASIC, namely **SSA**, will be the strip readout chip, designed in the same 65 nm technology, which provides real-time particle hit coordinates from a strip sensor to the MPA for the particle discrimination.

The two chips are strongly dependent on the other and need to be studied, designed

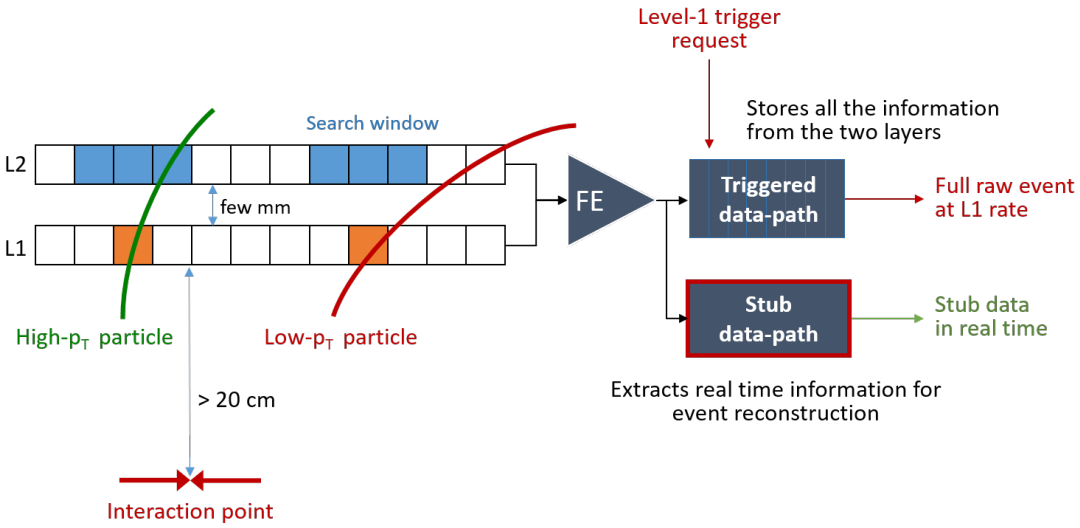


Figure 3.4. A simplified block diagram of the front-end electronics for transverse momentum discrimination.

and simulate together. Several architectures have been evaluated, as described in this chapter, to define which functionalities should be implemented in the MPA or in the SSA ASIC to minimize the bandwidth and the power consumption while reducing the inefficiency in terms of missing stubs. The large area of the sensors of 5×10 cm^2, tailored for the CMS outer-tracker requirements, makes necessary 16 MPAs as well as 16 SSAs chips for the full module readout and consequently a chip for data aggregation called Concentrator IC (CIC). Figure 3.6 shows the block diagram of the PS module readout system.

Since the communication between the pixelated silicon sensor and the MPA will be implemented via C4 bumps, the pixel front-end readout segmentation in the MPA ASIC is constrained by the granularity of the sensor. The ASIC size is limited by the planarity requirement for module assembly. Very large ASICs show warp, which makes the assembly of multi-chip modules very difficult. Consequently, given a pixel size of $100 \times 1467 \mu$m^2, the pixel array contains 16 rows and 118 columns per MPA. The total size of the chip is required to be 11.9 mm $\times$ 25.0 mm, which includes also a periphery of about 2 mm.

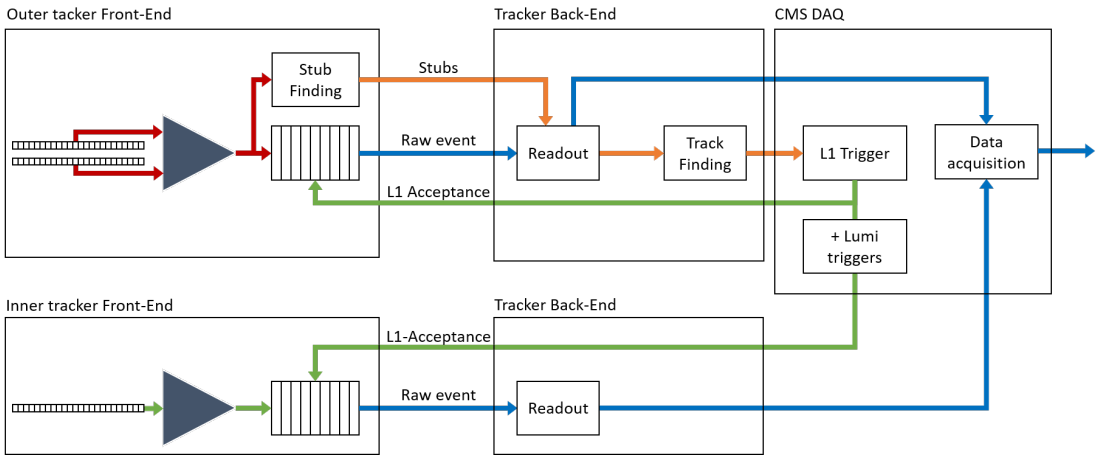


Figure 3.5. Block diagram of the tracker readout chain.

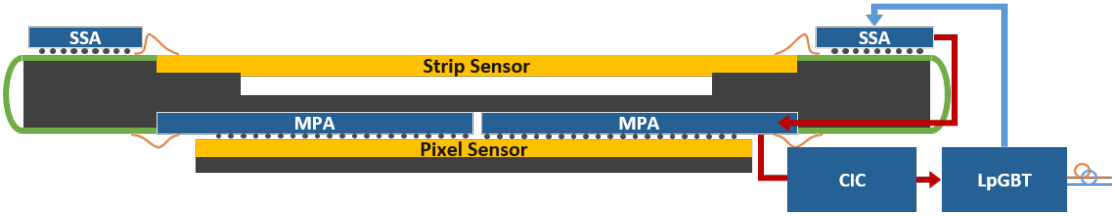


Figure 3.6. Section of the PS module and chip-set data flow.

The SSA ASIC, on each other hand, can be flip-chip bonded on the front-end PCB, simplifying the assembly procedure. The minimum die area can be therefore equal to 11.0 mm × 3.9 mm (significantly smaller than in the case of the MPA), and it is defined by the number of sensor input bumps and by the minimum bump pitch achievable on the hybrid flex PCB (200 µm [167]). The thickness of the ASICs is required to be 250 µm.

The multi-chip assembly (MaPSA) requirement imposes a lower limit to the spacing between MPAs of 100 µm. For each chip, the first and last macro-pixels cannot be connected to the readout electronics, due to the spacing between the chips (and associated margin). In order to not lose any active area, the unconnected sensor macro-pixels are shorted to their neighbour,resulting in a macro-pixel with double width at the edge of each macro-pixel row. As Section 3.8.1 will show, this will introduce some inefficiency in the particle recognition algorithm that needs to be taken into account in the studies to define the electronics architecture of the PS module.

The communication scheme between SSA and MPA is summarized in Figure 3.7. The SSA reads out the strip sensor signals, stores the strip L1 Data and sends strip Trigger-Data to the MPA. The latter reads out the pixel sensor, stores the pixel L1 data and processes the pixel and strip Trigger data: it correlates the pixel sensor hits with the strip sensor hits received from the SSA in order to reject low-p_T particles and provides only high-p_T particles data to the detector back-end electronics. L1 Data are encoded and sent to the detector back-end electronics when requested by a L1 trigger signal.

Considering the $32 \cdot 10^3$ channels of the Pixel-Strip module and an event rate of 40 MHz, the data produced is roughly 1.28 Tb/s per module, equivalent to approximately 25.6 Pb/s for the PS layers of the detector. A compression factor of at least 20× already in the FE ASICs is necessary to reach an almost lossless data communication.

The trigger-less readout path will represent the dominant contribution to the system power consumption due to the continuous data processing and transmission. Nevertheless, the front-end electronics preserve the triggered readout for the entire event as in the current tracker implementation. Its performance requires numerous improvements. The latency between the data acquisition and the reception of the trigger acceptance request is fixed. In the SST the L1 latency was 3.2 µs, while, in the upgrade it will be increase up to 12.8 µs. This change strongly impacts the storage capability

available on the front-end modules, already larger due to the use of a pixelated sensor and the increased granularity. The front-end ASICs are now required to maintain in memory the full sensor raw image for longer periods. For these reasons, L1 memories become another dominant contribution to the power consumption of the design.

The rate of Level 1 trigger should increase from 100 kHz to 750 kHz. This specification together with the higher granularity impact the size of the bandwidth needed for the on-module communication and between front-end modules and CMS back-end, forcing the use of zero suppression technique and the choice of a binary readout.

From the simulations of thermal performance and mechanical deformation described in [174] the maximum allowed power density for the readout chips is 100 mW/cm^2. The total power budget per MPA+SSA couple is 250 mW. The readout electronics is the main contribution to the power consumption of the full module (5 W of the 8 W estimated), hence it represents the main load for the power converters and for the cooling system (which are optimized for the estimated load). Any excess in power consumption of the electronics would overload the power converters and the cooling structure, increasing the temperature of the module. Such a problem must be strictly avoided because the sensor must be kept below a temperature around −20°C [9] to avoid breakdown or thermal runaway.

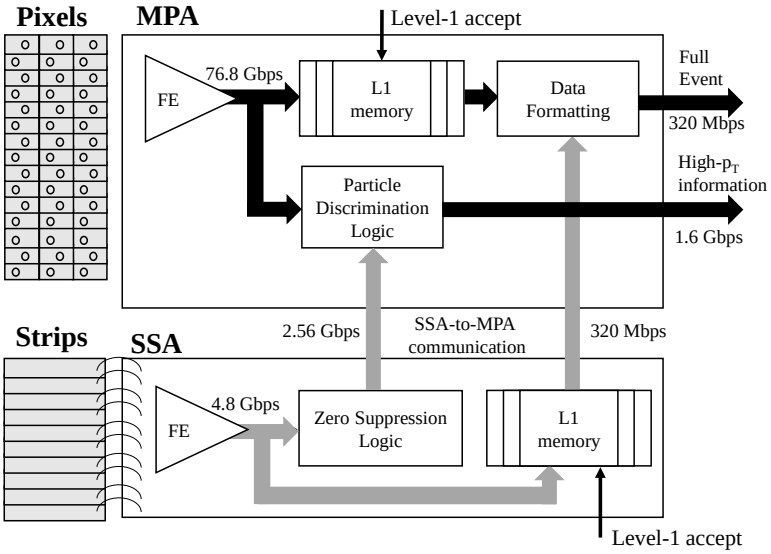


Figure 3.7. Block diagram of the SSA and MPA communication.

3.6 System-level modeling

Several design choices are necessary to optimize the PS module as one entire system. Functionalities like data elaboration for the particle recognition, data encoding, compression, storage, clustering, transmission, can be performed at different stages of the data path, utilizing different algorithms and be implemented partially into the SSA ASIC and partially into the MPA ASIC. At the initial stage, the number of transmission lines and the protocols between the two chips is not yet defined.

Most of the design choices are strictly related to the expected particle rates and characteristics, and the particle recognition requirements at the experiment back-end. In other words to the statistics of the system inputs and the requirements for the outputs in terms of acceptable losses, data streams, and error rates. For this reason, it was necessary to implement a functional model of the entire system readout chain and design a simulation tool to assist the system level studies and to evaluate the efficiency parameters based on realistic complex stimuli. Sections 3.6.1 – 3.6.6 describe the implementation of this simulation framework.

3.6.1 Multi-chip system level simulation framework for architecture studies and verification

The simulation of the passage of particles through matter using Monte Carlo methods is broadly used in the development of particle detectors for HEP experiments [175]. To develop the readout electronics for the CMS experiment at CERN, and to assist the design of the on-detector ASICs, the simulation framework build needs to be capable of linking the physics Monte Carlo simulations platforms with an industry standard EDA simulation tools.

Different parts of the design can benefit from a single versatile simulation environment without the need of developing multiple test-benches. The modular implementation and the configurable test scenarios allow focusing the simulation on the functionality of a specific subsystem and to verify its effect at the module level. A module level simulation allows moreover to verify, at clock-cycle level precision, the sub-system integration, the communication between modules and the communication protocols between chips.

Bandwidth and power limitations require to optimize the architecture of the system without affecting the overall efficiency. For this reason, it becomes necessary to evaluate the efficiency of the particle recognition algorithm and the data readout. The tool allows the comparison to an ideal reference model and to evaluate and study the efficiency at different stages of the chain.

The environment is based on the SystemVerilog [176] hardware description and verification language and on the Universal Verification Methodology (UVM) [177] from which it inherits the base classes. Additional analysis routines for statistical studies are implemented in Python. This approach was chosen because it allows combining in the same environment hardware modeling at behavioral Register Transfer Level (RTL) and at gate-level together with object-oriented constructs at Transaction Level Modeling (TLM) abstraction level. SV-UVM provides moreover application programming interfaces (APIs) to foreign programming languages and support for coverage evaluation, assertions based verification and constrained randomization, fundamental for the framework that have been developed. In its current implementation it required more than 100 k lines of code.

Implementation details of the simulation framework and examples reported in this section refer to the specific case of the CMS outer-tracker ASICs development. Nevertheless, as a result of the layer structure and the modular approach adopted, the framework usage can be extended to different particle pixel or strip sensor readout ASICs in the HEP community.

3.6.2 The framework implementation

A block diagram of the simulation framework is shown in Figure 3.8. The environment is composed by 4 main layers:

- The verification system that includes the UVM Verification Components (UVCs) related to the stimuli generation, the output monitors, the analysis component and the scoreboards.
- The reference model represents an high level description of the CMS outer-tracker readout system functionalities, without taking into account inefficiencies or limitations related to a particular implementation. It receives in input stimuli from the generation UVCs and provides the expected transactions for

each component of the module.

- The main test class creates the environment during its build phase (one of the built-in execution phases of the UVM methodology). Several test classes extend the main one, allowing to define multiple scenarios by configuring the UVCs and by constraining the stimuli generation.
- The Design Under Verification (DUV) instantiates the RTL description or the gate-level net-list of the CMS outer-tracker ASICs. It defines their inter-connectivity and it binds their building blocks to the framework components via interfaces.

The framework components are implemented at the Transaction Level Modeling (TLM) by extending the UVM base classes. At this level of abstraction channels hide the complexity of the protocols by implementing the communication in the form of function calls instead of signals. The communication among verification components, reference model and scoreboards is based on transaction objects. This approach, together with the high level of re-configurability, allows achieving a modular implementation easy to extend and reuse, while drastically reducing the simulation time compared to a more standard approach.

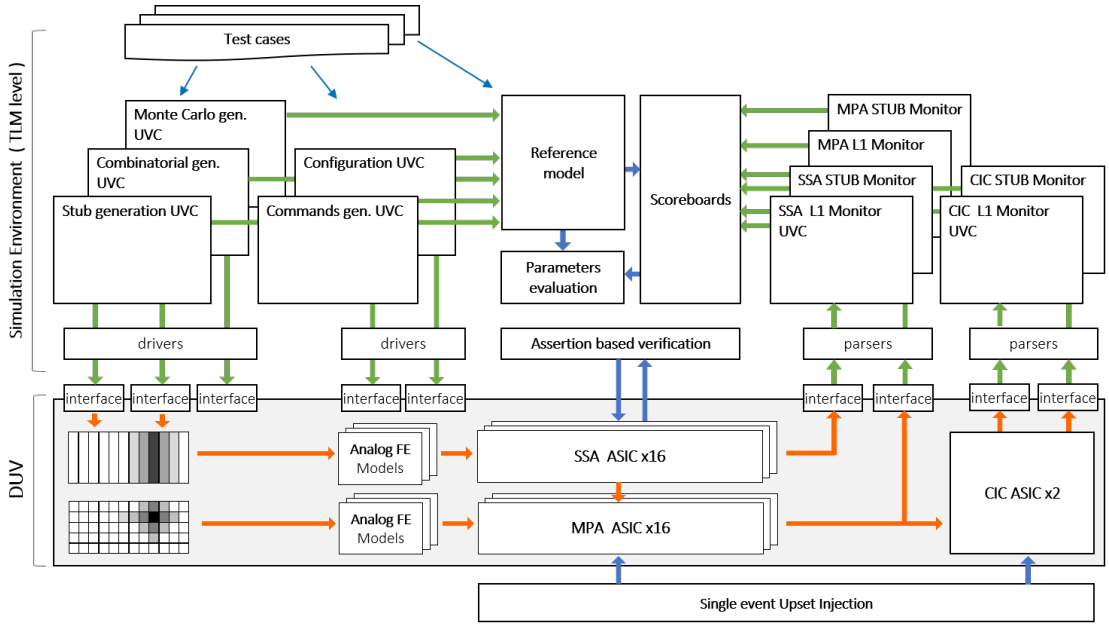


Figure 3.8. Block diagram of the simulation framework for the CMS outer-tracker detector readout chain.

3.6.3 Stimuli generation

Three main types of stimuli can be provided to the DUV:

- For functional verification, constrained random generated stimuli allow stressing the design and reach high coverage values.
- For performance evaluation, physics Monte Carlo simulation events are generated by the CMS tracker physics simulation toolkit and integrated in the System Verilog simulation environment. This allows performing system studies based on realistic stimuli and to evaluate the system performances in the target application.
- Global clock and control signals are generated for the operation of all ASIC components. This includes the generation of the system clock and reset signals and the sequences for the high speed control and for the serial configuration ports.

Each stimuli generation Agent UVC is composed by four main components as shown in Figure 3.9. The Sequence class, derived from the uvm_sequence, creates the series of transactions at TLM level. The sequencer allows randomizing the sequence items and to transmit the TLM transactions to the driver where are converted into the RTL signals provided in input to the DUV via interfaces. The main test class allows to control the configuration class via the UVM factory mechanism, an object oriented design pattern that provides the ability to configure the verification objects from anywhere else in the code. The configuration class determines the sequence item by constraining the UVC operations and the data randomization [5].

The stimuli components generate the pixel particle charge deposition matrix and the corresponding strip hits array, emulating the CMS outer-tracker double layer silicon sensors. The generated values are transmitted to the reference model in the form of TLM transactions and to the System Verilog models of the ASICs analog Front-Ends in the form of 32-bit signals representing the particle charge deposited on the sensors expressed in fC.

In order to reduce the simulation time, the TLM transactions are created only in relation to the generated hit clusters, avoiding to transmit the full matrix for each event. Each transaction carries the information related to the HL-LHC Bunch Crossing

reference cycle, the φand z coordinates of the particle clusters, the particle transverse momentum, the charge of the particle and time of arrival [5].

3.6.3.1 Random particle event generation

This stimuli generation UVC produces randomized transactions emulating detectors hits due to ionizing particles forming single tracks and crossing the detector with a certain angle. It is very important to highlight that this hit generator UVC, even if it aims to approximate physics input, can not substitute stimuli based on Monte Carlo simulations. It is just supposed to be a flexible and easy to use component capable to provide DUV stimuli that follows a realistic statistic. Compared to the Monte Carlo based stimuli described in Section 3.6.3.3, a much larger amounts of DUV stimuli can be produced allowing, for instance, performing coverage tests. It gives moreover the flexibility of driving the DUV with extreme particle rates or with very specific hit generation constraints to stress the design and evaluate its behaviour in the limit case.

This was very useful during the selection of the PS module electronics architecture and during the design of the MPA, SSA and CIC ASICs. It allowed taking design choices

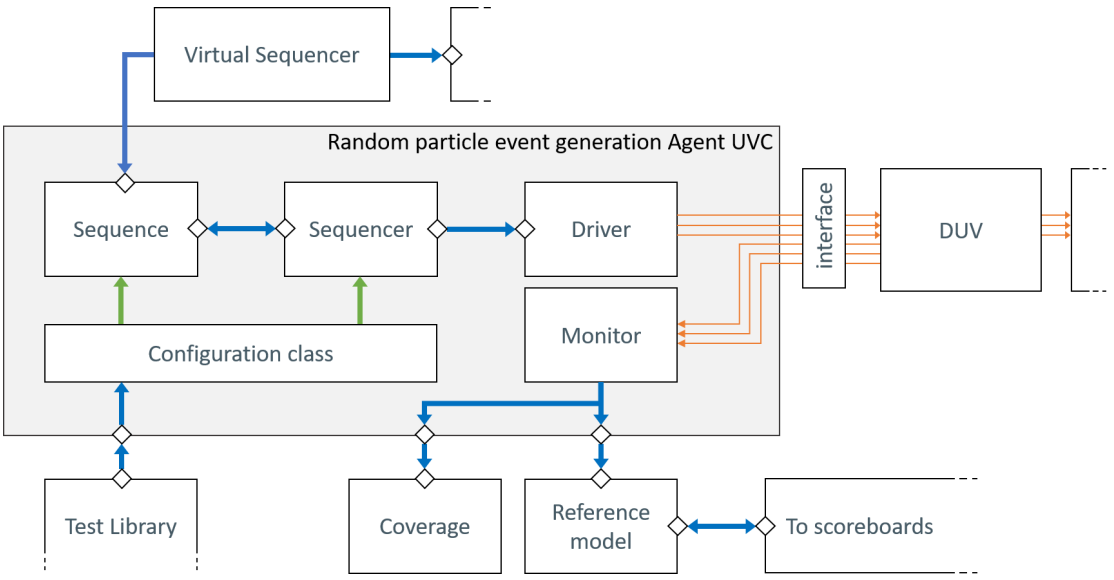


Figure 3.9. Agent UVM verification component block diagram. The communication among components is based on TLM transaction (in blue) over TLM analysis port/export (rhombus). The Driver converts to RTL signals (in orange).

optimized for the expected particle hit statistics but capable to handle more extreme situations, avoiding to lose synchronization between ASICs or driving the logic into some not handled state. At the same time it permitted to avoid over-design of the memory elements and FIFOs with consequent saving in therms of power consumption.

The average particle rates are configurable independently for high and low transverse momentum particles. Signatures related to high-p_T particles, namely stubs, represents the main primitives expected to be identified by CMS outer-tracker. Any missing stub at the output of the DUV may identify either a design error or an inefficiency of the particle recognition algorithm or of the implementation. These exceptions are handled and reported by the framework.

Low transverse momentum particles stimuli represent non-interesting event for the trigger reconstruction but should be transmitted when the DUV transmits the full raw sensor image upon trigger reception. The DUV ASICs should be able to correctly detect those hits, and by correlating the two layer, opportunely reject these information. Nevertheless, low transverse momentum hits need to be taken into account in the simulation since may saturate the DUV internal bandwidth or the FIFOs, reducing the recognition efficiency.

The stub generation sequencer allows generating the DUV stimuli computed starting from the randomization of an instance of the *hit_event* class. This class implements several variables correlated among each other whose randomization is constrained according to an approximation of the particle charge deposition statistics.

A set of parameters that allow controlling the randomization and constraints are configurable per test case. Those parameters are defined into within an UVM configuration object that can be can be overwritten at run-time via the UVM factory mechanism either by the test case or the scoreboard. The main randomized variables are:

Particle hit probability The density of stubs (and as well of low-p_T particles) follows a Poisson distribution with a configurable mean value. Indeed it approximate the probability of a number of independent particle events occurring within a fixed interval of time for a constant average rate. The events can be considered independent if neglecting the probability of particle charge deposition over the sensor ranging more

than one BX cycle and the probability of low energetic loopers confined within the tracker volume.

Cluster centroid coordinate The φ and z coordinates of the center of the charge deposition cluster are consider uniformly distributed variables at this stage. The module dimensions are small enough to assume a uniform hit probability per module. For detector studies, the particle hit probability is tuned accordingly to the central coordinate of the module that is currently under evaluation.

Cluster radius The cluster radius depends on two factors: the bending of the particle track with respect to the sensor surface and to the charge shearing and cross talk phenomena between electronic channels. The first cause can be easily taken into account considering that for lower transverse momentum and higher particle track bending, the probability of traversing multiple adjacent pixels or strips increases (accordingly to the sensor thickness). The cross-talk phenomena instead is due to the capacitive coupling between the routing lines and the strips p+ implant (or the strips metallisation) some of the signal induced in the strip or pixel is shared with adjacent strips. The randomization of the cluster radius is approximated in the framework with a Poisson distribution whose mean value can be configured on a per-test basis.

Time of arrival Represent the overlap of two effects: the actual particle-hit arrival time (ToA) within the bunch crossing window and the delay due to the sensor and analog front-end response. The first contribute can be neglect if we assume that the sampling clock utilized by the ASICs composing the PS module is correctly de-skewed accordingly to the module location within the tracker. This is mostly true for the final system but the environment needs to permit the front-ends verification in the edge cases. The second contribute is given by the fact that in a standard front-end, not only the output pulse amplitude, but as well its rising time is directly proportional to the input charge. Consequently the the difference between charge injection time and detection by the edge detector (commonly referred as timewalk) is dependent on the input charge. This effect can be initially taken into consideration by correlating it to the particle energy. For more accurate studies this parameter was disabled when the FE ASICs design reached a more advanced stage and an accurate Verilog-AMS model of the front-end was included in the simulation framework.

Charge deposition probability To correctly emulate the probability of charge deposi-

tion would require to implement a complex simulation of the particle interaction with the silicon. It goes out of the scope of such framework in particular considering that data extracted from simulation of the particle interaction with silicon can be parsed by the framework. For this reason, it is simply represented by its probability to be below the detection threshold, over the detection threshold or higher than the limit defined for high ionizing particles (HIP), according to what described in Section 4.2.1. The detection threshold depends on the minimum detectable charge and on the noise performance and mismatch of the sensor and of the front-end. At this stage is set just over zero since noise effect are considered into this digital simulation via the noise generation UVC (Section 3.6.3.2).

Transverse momentum Represent the particle p_T. Also in this case it is divided into two categories: high-p_T particles whose particle bending is randomized following a Gaussian distribution with mean 0 and configurable σ, and low-p_T particles whose bending is approximated with an uniform distribution across the module.

3.6.3.2 The combinatorial stimuli generation

This UVC generates randomized stimuli that follow a uniform distribution in terms of $\varphi$and z coordinate. It can be activated separately or in addition to the stub generation UVC. In the first case it allows stressing the DUV by generating events that do not represent necessarily the expected ones, permitting to reach higher levels of test coverage. This analysis is convenient to evaluate the maximum pixel hit occupancy that the ASICs are able to handle without saturating the internal FIFOs and transmission bandwidth. In the latter case, when the noise generation UVC is enabled together with the stub generation UVC, it allows emulating detector hits that do not represent valid stubs such as machine background or not interesting particles depositing charge on the sensors.

Generally the readout ASICs analog front-end is designed to minimize the input noise to detect small input charges. Providing this set of stimuli into the digital simulation is possible to evaluate as well the effect of noise hits on the digital processing circuit and the effect that is has on the particle recognition algorithm.

3.6.3.3 The Monte Carlo stimuli generation

A full Monte Carlo simulation of LHC events with high pileup gives the best prediction of the detector performance and overall physics capabilities of the upgraded CMS detector, once the detector response is known and correctly simulated.

In order to evaluate parameters based on the real physics events an additional stimuli generation component, referred in Figure 3.8 as Monte Carlo generation UVC, allows to import particle hits from Monte-Carlo (MC) programs for computer simulation of complex interactions in high-energy particle collisions. The data-sets provide event samples for the entire CMS outer-tracker [5].

The hits production can be simulated vie Geant [178], [179] accordingly to the geometry construction imported via XML files. Geant 4 is included in the CMSSW [180] software package via the OscarProducer [181], a Geant based detector simulation module. Generated particles are traced through the hierarchy of volumes and materials, and the physics processes that accompany particle passage through matter are modeled accordingly to the physical geometry [182]. The results of each particle's interactions with matter are recorded in the form of simulated hits [183]. Different events samples can be produced, for different pileup values and geometries.

The output simulation hit files in ROOT [184]–[189] format can now be analyzed via the Viret's RecoExtractor package [190]. It allows extracting information related to pixel and strip hits for specific locations within the defined geometry and produce front-end data files in the format defined in the CIC1 technical specification document [191].

The front-end data files can be imported and parsed by the simulation framework dedicated UVC. A driver object provide the correct temporization and converts the hits into RTL signals at the inputs of the the design model. Via the configuration mechanism it is possible to import stimuli related to different module position within the outer-tracker geometry allowing to verify the functionalities of the design with several configurations, input activities and module geometries.

3.6.3.4 Communication protocols and configuration

The outer-tracker readout ASICs require a fast command input signal, namely T1, in order to control their internal operations and the module functionality (i.e. the

complete pixel raw data transmission request, re-synchronization request, the shutter control and several others). The environment allows randomizing the commands generation taking into consideration the correlation with the input data, and to configure their average rate from the test cases. This allows evaluating the maximum trigger rate acceptable for a given bandwidth and eventually re-size the internal FIFOs.

The DUV ASICs implement a large number of control registers to program their functionalities and operating modes. Additional registers for each pixel allow configuring and equalizing the analog front-ends, modeled in the environment with a System Verilog description. The configuration UVC allows verifying the control protocol implementation and evaluating the functionalities of the DUV under different conditions and different operating phases. This component has the purpose of translating the test-case configurations into signals applied to the DUV in the format defined by the communication protocol. The same set of configuration parameters is then transmitted in form of TLM transactions to the stimuli generation, to the reference model and to the output monitors. The user can define simple test files to setup both the DUV and the simulation framework in a specific operating mode [5].

3.6.4 Reference model

A TLM reference model implements a high level description of the CMS outer-tracker readout functionalities. It receives as inputs the stimuli from the generation UVCs and generates the expected transactions for each component of the DUV.

At this stage no bandwidth limitations are foreseen. Several threads reproduce the different sub-systems functionalities by providing a set of TLM transaction to the scoreboard via analysis exports. In addition, possible sources of inefficiencies are evaluated and the correspondent transactions are flagged for more precise analysis in the scoreboards [5].

The analog functionalities are represented with their simplified behavior. The SSA, MPA and CIC ASICs embed several analog modules that requires to be accurately modeled in the environment (i.e. the analog front-ends, the biasing circuitry, the DLL for phase alignment and others). The analog functionalities are modeled with an accurate System Verilog description to drastically reduce the simulation time compared to a mixed signal simulation approach. In the case of the analog front-ends, for example,

the model approximates the internal response to the input charge according to configurable parameters as peaking-time, return-to-zero time, front-end amplifier gain and offset, comparator thresholds and input noise, and other parameters obtained from the analog circuit simulation.

3.6.5 Monitors, scoreboards and efficiency evaluation

The simulation framework implements several monitor objects connected to the output of each of the ASICs and to other critical nodes of the design. The monitors converts the RTL signals into TLM transactions that can be handled by the analysis components.

The CMS outer-tracker readout ASICs are required to provide at the same time: stub data (primitives of particles with high transverse momentum which are transmitted for every event) and L1 data (the complete pixel and strip events when requested by L1 trigger system). The monitors relative to the stub data path evaluate the signals in output at every clock cycle and decode their information. On the other hand, the monitors relative to the L1 data path implement an event-driven behavior which generates transactions only when triggered by the stimuli generation UVCs or when they detects activity on the monitored signals [5].

Several scoreboards allow performing conformity checks between predicted and actual DUV outputs. The results of the comparison are reported in the simulation logfiles for further analysis. A communication between scoreboard elements is necessary to identify the mismatch source in the case the issue propagates along the readout chain. Every mismatch can either represent an error in the design or a limitation of the ASICs implementation. Discrepancies are categorized as:

- Bandwidth limitations that can lead to missing stubs at the DUV outputs. For instance high trigger rates compared to the internal FIFO or high particle occupancy may lead to data losses in the data acquisition chain.
- Errors which represent the percentage of losses due to artifacts introduced by the algorithm implementation in the hardware. Among those, several checks are implemented to distinguish multiple error sources.
- Geometrical losses due to detector construction coming for example from the strip or pixel resolution that limits the tracks separation or the dead area among

ASICs due to mechanical requirements which can alter pixel centroids position.

- Efficiency limitations due to the stub recognition approach adopted or the algorithm implementation.

The effect of those discrepancy on the system efficiency are reported in the summary tables along with detailed statistics (stub occupancy, particle rates, noise, trigger rates, etc.). Additional detailed log-files reports the information needed to evaluate the cause. Multiple levels of details can be configured to monitor stimuli generation and the pipeline data at different stages of the system. Additional python scripts allows for further data analysis and plotting.

3.6.6 A test-cases library for functional verification

To allow for multiple simulation scenarios, the simulation framework implements a library of test file to easily configure the environment. The user can create new test scenarios without the need of the framework implementation knowledge. Tens of functions can be called to change the default behaviour of the stimuli generation, of the scoreboards checks and to configure the operating mode of the system. For the latter one, the environment internally handle the distribution of the configuration parameter to all components that requires it (monitor objects, reference model and scoreboards), and the configuration of the RTL models of MPA, SSA and CIC either by serial communication protocol of by directly forcing the value in the corresponding configuration register. Example of such parameters are: transmission mode control (synchronous or asynchronous), particle hit detection thresholds, cluster-size cut, high-p_T stub thresholds, transmission frequencies, phase alignment control and several others. The stimuli generation can be configure in terms of randomization mode, average particle rates, high-p_T and low-p_T stub rates, noise occupancy, average trigger rate, particle charge distribution, synchronous requests probability and many others. In addition, by overriding the constructor or specific functions of the stimuli generation class directly in the main test file, it is possible to change the stimuli randomization behaviour, allowing for more complex features. The specific test can be selected via the UVM configuration mechanism, called via makefiles or via the GUI provided by the Incisive vManager [192] tool which allows to launch multiples runs in a single session using a distributed resource manager and facilitate failure analysis by automatically extracting, filtering, and grouping key information from all log files.

3.7 Triggered transmission of full sensor data

The trigger system requires several microseconds to process the data and the trigger signal for the selection of the interesting events is propagated to the pixel/strip readout ASICs with a delay of several bunch crossing clock cycles. Compared to the current CMS detector implementation, the operation in the high luminosity conditions requires a substantial upgrade of the trigger system as described in the previous chapter. Higher trigger rates will allow transmitting to the experiment back-end a significantly higher amount of event data. An increase of the time available for data processing from the current 4 µs up to 12.6 µs [9] between the transmission of the trigger request and the corresponding event occurrence (L1 latency) is considered to be suitable to handle more complex real-time computations for the trigger decision. The hit information must be stored within the readout ASICs (MPA and/or SSA) during this fixed latency interval. Even if in average less than 2% of events will be required, multiple consecutive readout requests may occur. The front-end ASICs are required to be able to accept new triggers before the data of a previous request has been fully transmitted. The steps necessary for the L1 data transmission are summarized in Figure 3.10.

3.7.1 L1 data path architecture studies

For what concerns the L1 data transmission between the strip readout ASIC and the pixel readout ASIC, the most straightforward approach could consist in constantly transmitting, for every event, the data in a raw format without applying any zero-suppressing or compression. The raw data related to the strip sensor could be stored directly in the MPA ASIC.

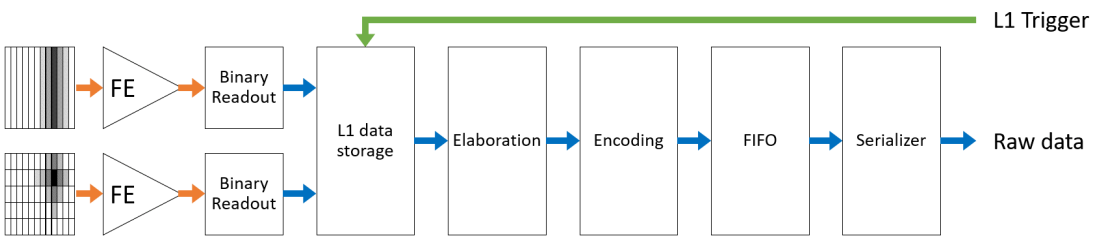


Figure 3.10. Block diagram of the main pipeline steps of the triggered readout data path at module level.

To represent both hits over the threshold and high energy particles hits for every strip 240 bits are necessary, requiring 30 differential lines between the two ASICs running at the maximum clock frequency available on the module (320 MHz). This number can be reduced to 23 lines if assuming that a detected HIP always implies a strip hit. The simulated power consumption for a radiation tolerant transmitter/receiver couple is ≈1.2 mW. This approach would require 29.9 mW, 12% of the total power budget of MPA and SSA just for the internal communication. If transmitting already encoded coordinates instead of raw data, 7 bits are required to identify the hit coordinate plus 1 bit to identify if the particle hit is due to a high ionizing particle. The number of differential lines scales with the maximum number of particle clusters to be transmitted. This value depends on the error that can be accepted for the offline analysis and the raw data transmission. Clearly, the latter case defines the upper limit.

Figure 3.11 shows the cluster multiplicity evaluated per single MPA-SSA couple. It is obtained for pileup 200 using a sequence of $50 \cdot 10^3$ clock cycles [194] and only physically interesting events. The data-set was produced using the most recent CMSSW release [180] based on the tilted geometry baseline setup [195] using the latest minimum bias tuning available [196]. To limit cluster losses probability to $< 10^{-6}$ (1ppm), the readout ASICs should be capable of transmitting up to 24 strip-cluster coordinates per bunch-crossing (considering a margin for eventual higher pileup scenarios). The required bandwidth between SSA and MPA ASIC results 10.56 Gb/s (assuming 7 bits for coordinate encoding, 3 for the cluster radius and 1 bit to flag HIPs), higher than the

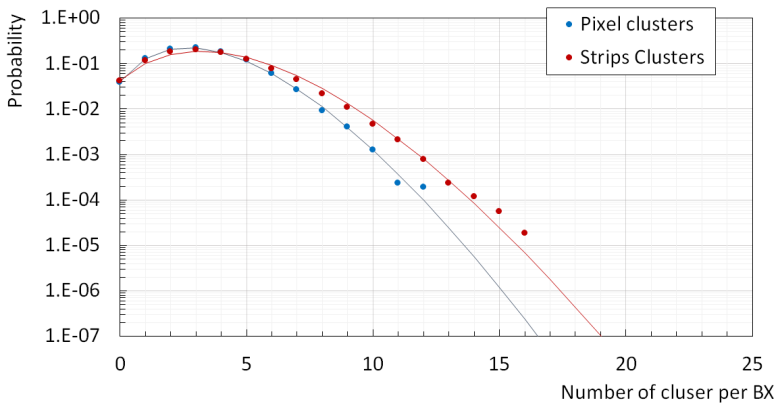


Figure 3.11. L1 data cluster multiplicities for the strip and pixel layer, from pileup 200 Monte Carlo simulation analysis.

bandwidth that would be required if transmitting unsparsified data, even if in more than 92% of the events, less than a 1/5 of the bandwidth would be utilized.

For those reasons, the first considered PS module architecture was reevaluated. Storing the strip hit information in the SSA could allow to drastically reduce the bandwidth. The full event raw data information transmission, in fact, could take place only when required by the L1 instead that for every event. It requires, on the other hand, to decouple the transmission of stub data for the trigger system from the transmission of the L1 data already in the SSA ASIC. In any case, as discussed in Section 3.8, 8 clusters per bunch-crossing are sufficient for the trigger decision.

The SSA can transmit the strip hit and HIP information to the MPA either unsparsified or applying zero suppression. If transmitting unsparsified data, the required bandwidth between strip readout ASIC and pixel readout ASIC is equal to 1.28 Gb/s per module. The same calculation could be repeated considering transmitting the coordinates of the center of the formed cluster and the cluster radius instead of the single hit coordinates. From the Monte Carlo events simulation at pileup 200, we can evaluate the probability that a certain number of hits should be expected per event on the strip sensor layer. The data is reported in Figure 3.11. It is immediate to evaluate

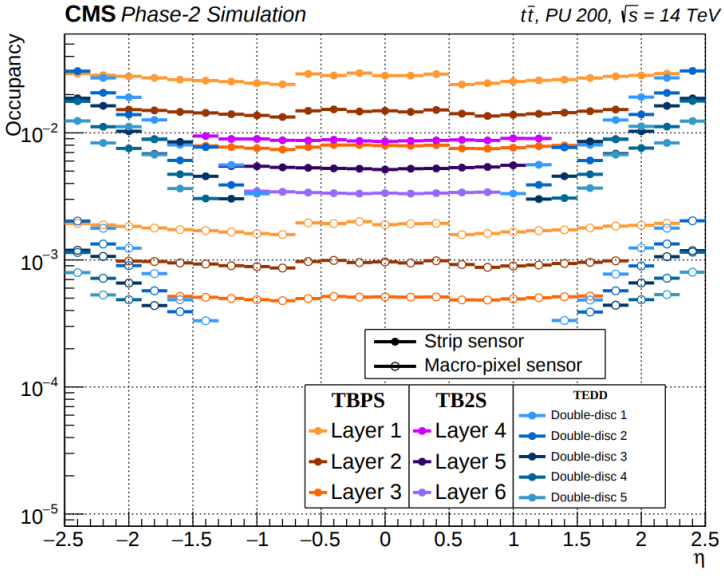


Figure 3.12. Hit occupancy defined as the fraction of channels containing a digitized hit, as a function of η for all pixel and strip layers for tt pileup 200 events [193].

the average payload size of 29.8 bits per L1 acceptance. The required bandwidth is equal to 357.6 Mb/s. The second approach described is clearly more convenient in terms of bandwidth. It introduces anyway complications in the SSA and MPA designs requiring to handle a variable size packet with variable latency.

One more consideration should be taken into account: the SLVS transmitters utilized in the designs provide a constant power consumption independently on the activity. The current depends on the differential mode defined by the SLVS standard (200 mV) and the termination impedance of 90 Ω. If utilizing a single transmitter the bandwidth is limited to 320 Mb/s, therefore the most simplistic approach, considering to transmit for each L1 packet as well 16 bits for the trigger counter, event counter and a minimum packet header header (256 bits in total) would limit the L1-trigger frequency that the SSA-MPA link could handle at $320\,\text{Mb/s}/256\,\text{b} = 1.26\,\text{MHz}$, higher than the 750 kHz L1 trigger frequency required by the CMS phase-2 upgrade, with a fixed packet length. If the SSA transmits a more extended data packet means that the probability of receiving one or more additional L1 trigger during the packet transmission is higher. Consequently, the FIFO size should be increased in the SSA to buffer new events waiting to be transmitted and in the MPA to buffer the pixel event while attending the completion of the SSA data reception.

From simulations performed using the the system model described in Section 3.6 based on Monte Carlo data, a mixed approach results to be more convenient in terms of overall power consumption: the information related to the hit detection threshold are transmitted without compression and with a fixed packet size since any loss-less encoding would require an equal or higher bandwidth. The signals related to HIPs

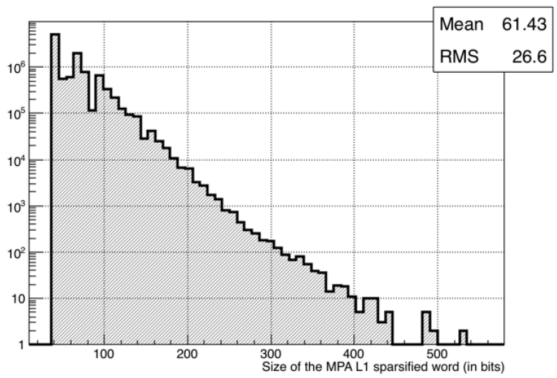


Figure 3.13. Size of the MPA L1 sparsified words for pileup 200 events.

are instead transmitted along the frame with a zero-suppression technique. The most efficient approach consists in transmitting a flag for the clusters where, in at least one channel, the charge deposition is higher than the high ionizing particle threshold. Even if the information relative to the exact particle hit coordinate is lost, the back-end reconstruction can link it to the cluster centroid coordinate, considering the deposition as Gaussian with mean in the centroid. The maximum number of HIP flags can be limited to the maximum cluster number fixed to 24.

The situation is very different in the case of the pixel layer where the unsparsified approach would require to transmit 1920 bits for each pixel plus the data received from the SSA, limiting the L1 rate to 148.15 kHz. In this case, it is necessary to apply encoding and zero suppression on the data. The average number of hits expected on the pixel layer and on expected on the strip layer is of the same order of magnitude since traversed by the same number of particles. Each pixel has a hit probability of about 1/16 compared to a strip. Transmitting only the coordinates of the clusters centroids and their radius is widely more optimal in the case of the pixels.

From Figure 3.11 previously described, it is possible to evaluate the probability of pixel clusters per BX and consequently the payload size at the MPA ASIC output. The size of the sparsified payload for the same pileup-200 simulation is reported in Figure 3.13. The average packet dimension is 61.43 bits.

3.8 Stub data path

The stub rate is an essential parameter for both the front-end and back-end electronics. At the front-end, it is critical to check that the average stub rate per module is well within the readout capacity of the detector. At the back-end, the stub multiplicity per trigger tower will impact the performance of the L1 tracking system directly, and must be a well controlled parameter.

The stub data path should provide the high-p_T information by sending out the position of the stubs which have been found with an estimation of their transverse momentum. The position is summarized with the coordinates of the point of incidence on the pixel sensor, while the momentum with the bending angle in the $r-\phi$ plane of the particle.

The Stub Finding algorithm can discriminate the particles accordingly to their bending:

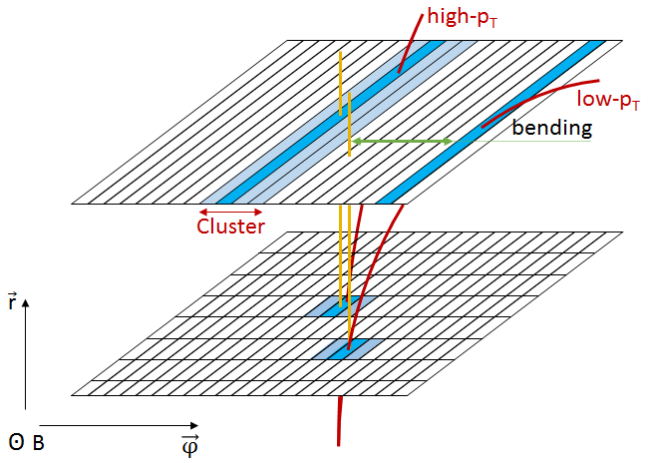


Figure 3.14. Example of the PS module track bending discrimination.

if it is lower than a defined threshold, the particle is accepted and the stub information is transmitted to the L1 Tracking. Otherwise the information is rejected. In order to build a stub, the SSA-MPA system must process the hit information from both pixel and strip sensors and evaluate the stub width (S_W) defined as the distance between the interaction point in the two layers. In output it provides the encoded position and bending of the stubs found (see Figure 3.14).

A cluster can be defined as a group of consecutive particle hits. It can be generated due to cross-coupling between adjacent pixels, by an high-p_T particle passing through two consecutive pixels or by a not interesting particle as a very low p_T or a secondary particle. In the first two cases, the algorithm must reduce the cluster to his geometric centre, called centroid, which approximate the real incidence point of the particle. In the other cases, the cluster must be discarded because it is generated by a not interesting particle. Particle clusters wider than a defined threshold (Section 4.3) can be rejected, while the centers of the remaining clusters are calculated. The width of the

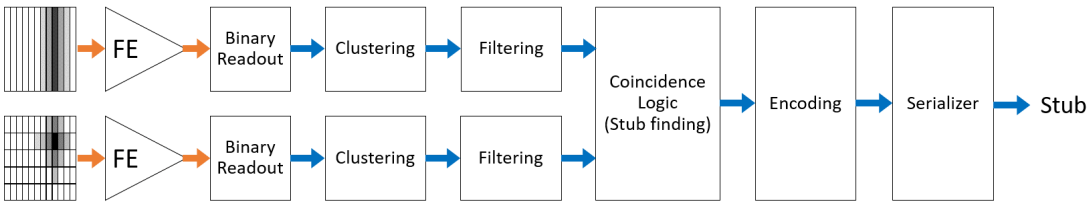


Figure 3.15. Block diagram of the main pipeline steps of the untriggered stub data path at module level.

accepted cluster depends on the coupling between pixels. Accepting larger clusters will reduce the data reduction capability of the clustering step, so cross-coupling among pixels must be reduced as much as possible. Figure 3.15 provides an overview of the necessary steps for the stub data path.

3.8.1 Stub-data bandwidth and efficiency studies across the detector

From the considerations expressed in Section 3.7.1, it is substantially more convenient in terms of power consumption to utilize an architecture where the SSA transmits L1 data to the MPA only when required by the L1 acceptance. It implies that information needed for the coincidence logic and the stub extraction needs to follow a separated data path, already at the stage of the SSA-MPA communication.

Defining the fraction of stub losses at the PS module level is acceptable for the L1 tracker reconstruction, is not straight forward. The pattern recognition algorithm studies and implementations are proceeding in parallel with the design of the front-end ASICs. At the moment, three different methods have been developed and demonstrated by different teams (an Associative Memory plus FPGA approach, an FPGA-based Hough transform approach, and an FPGA-based tracklet approach, whose description can be found in [197]–[199]).

Local stub losses at the level of the PS module lead to inefficiencies in the L1 trigger track finding. The layers redundancy may mitigates their effect. On this topic, extensive studies performed with different detector configurations have shown that five module layers in the barrel would provide sufficient efficiency of the track finding for the L1 trigger [15]. On the other hand, its performance would be profoundly affected by any in-layer localized failures. Six layers provide the necessary redundancy allowing for robust performance with respect to inefficiencies affecting one layer [165] (no particular advantages that justify the increase in material budget and cost are evident in implementing seven or more layers [200]). In addition, as discussed in Section 3.1, the L1 trigger system will combine tracker information with the energy data from the calorimeter layers providing an additional increase in the final L1 trigger efficiency.

The stub losses at PS module level should be kept as low as possible. The loss rate depends on the stub occupancy. Modules located in the innermost layer of the barrel

or in the first two end-cap disks, will experience in average more than 4 stubs per module per BX, while modules located farther from the vertex will experience one order of magnitude lower rates. The PS module should be designed for the worst case scenario. Stub losses at PS module level in the order of ~ 1% in the critical layers are considered acceptable since would not drastically affect the tracker reconstruction [194]. In particular, the probability of having additional information losses for the same particle trajectory in a second layer and utilizing the same module implementation is almost negligible in comparison.

Simulations with Monte Carlo events were carried out to estimate the losses according to the module location and the pileup. Figure 3.16 show the probability of having at least n stubs at the MPA output as function of n. The distribution is computed over Monte Carlo simulations of minimum bias events + 4 tops at pileup 200 obtained as described in Section 3.6.3.3. A cut of 2 GeV/c is applied for the stub selection. The effect on the bandwidth of the transverse momentum cut is discussed in Section 3.8.3.

Considering the half-pixel resolution required and assuming bending information encoded over 5 bits, a stub requires 17 bits for the encoding. A maximum of 5 differential lines are reserved for the stub data path between the MPA and CIC due to mechanical limitation in the hybrid design [172]. A maximum of 2 stubs per BX can

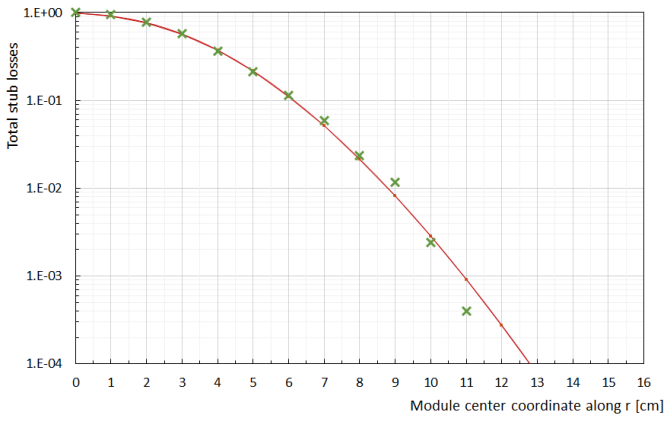


Figure 3.16. Probability of having more than n stubs as a function of r at the MPA output. The distribution is computed over Monte Carlo simulations of minimum bias events + 4 tops at pileup 200.

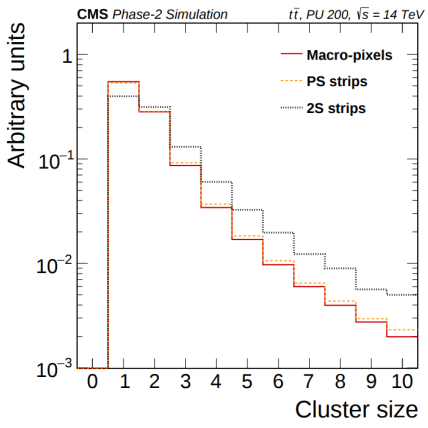


Figure 3.17. Charge cluster size distribution for the pixel and strip sensors of the PS and 2S modules, simulated for PU 200 [9].

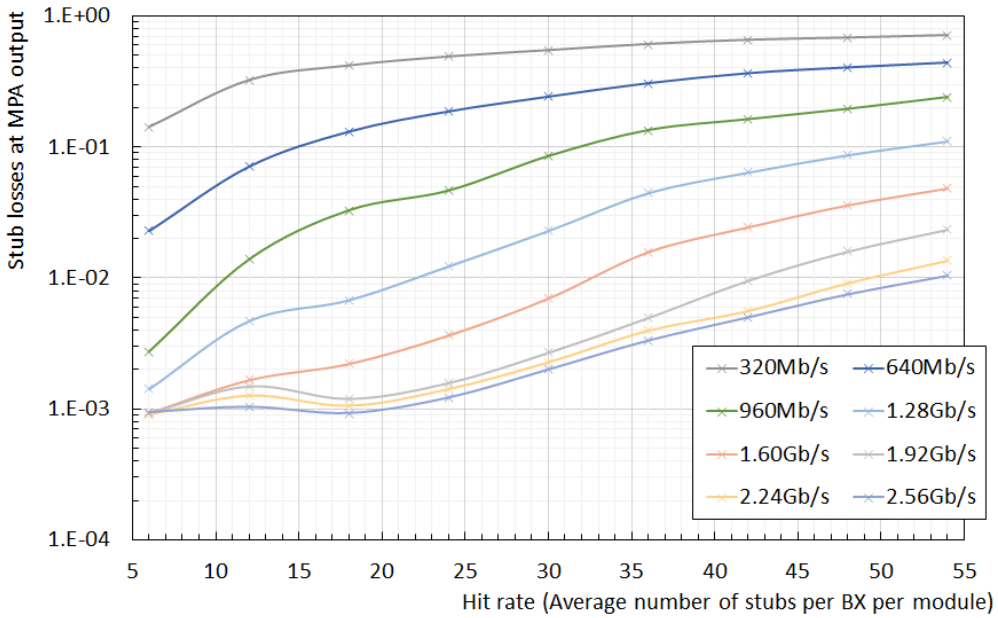


Figure 3.18. Average stub losses at the MPA output as a function of the strip hit rate occupancy and the SSA output bandwidth.

be transmitted by the MPA. From Figure 3.16, the average stub losses is ~ 5%, too high for the event reconstruction. To ensure losses below ~ 1%, the MPA needs to transmit at least 2.5 stubs per BX on average. Considering that the events can be assumed uncorrelated, a possible approach to achieve this result consist in transmitting up to 5 stubs in synchronous blocks of 2 clock cycles. Fitting into the bandwidth requires in addition to slightly reduce the resolution in the track bending value encoding it with 3 bits.

Concerning the communication between SSA and MPA, the situation is different. The SSA alone cannot evaluate a priori if the strip hit is due to a high-p_T particle. As shown in Figure 3.1 (Section 3.1), less than 10% of the particle tracks present a p_T greater than 2 GeV/c [156]. The SSA is required to face a higher bandwidth requirement.

A charge deposited by a particle on a single strip may induce parasitic signals on the neighbor strips as described in Section 4.3. A Poisson distribution can approximate the size of the charge deposition cluster. Figure 3.17 shows the simulated cluster size for the pixel and strip sensors assuming a 5% cross-talk. The mean of the distribution is ~ 2 strips. Clustering the strip hits directly in the SSA and transmitting encoded information of the clusters centroids allows for ~ 2× reduction in bandwidth.

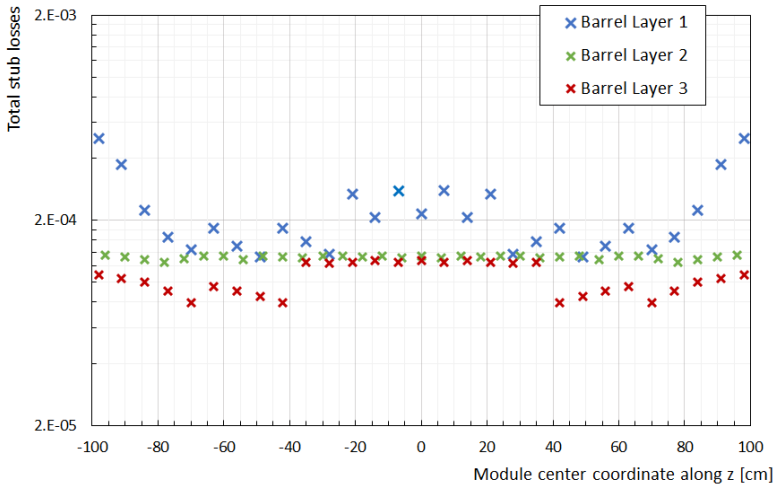


Figure 3.19. Expected stub losses as a function of the modules' z positions in the CMS outer tracker barrel.

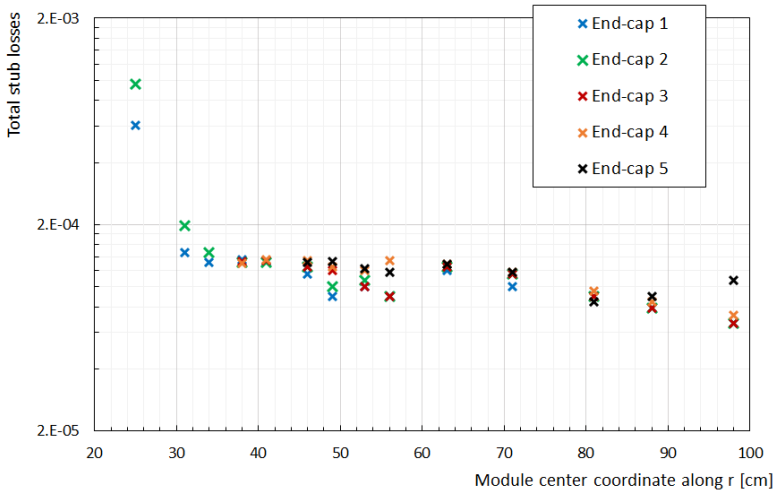


Figure 3.20. Expected stub losses as a function of the modules' r positions in the CMS outer tracker end-cap disks.

The hybrid design does not constrain the number of transmission lines among SSA and MPA. On the other hand, the differential transmitters represent a significant contribution to the power consumption of the ASIC. The average number of clusters per module per event is a function of the module location in the tracker as described by Figure 3.12. The communication needs to be sized for the worst case condition. The MPA+SSA model was simulated for different particle occupancy and different bandwidth between the ASICs. Figure 3.18 shows the evaluated stub finding efficiency

at the MPA output. To limit the losses below 1% in the inner barrel layer, a minimum bandwidth of ~ 1.9 Gb/s is required, corresponding to 6 differential transmitters. For higher values the losses due to the stub transmission bandwidth become dominant. To make the ASIC more general purpose, it will implement 8 SLVS transmitters, with the possibility to dynamically disable a certain number of drivers when not required accordingly to its location in the tracker.

With this implementation, it was possible to simulate the expected losses as a function of the module location within the tracker. Figure 3.19 shows the losses as a function of the module z coordinate with respect to the nominal interaction point, for the three different tracker barrel layers. Figure 3.20 instead describes the losses foreseen in the five barrel disks as a function of the radius.

3.8.2 Clustering across neighbouring ASICs

Due to the size of the planar silicon sensor of $5 \times 10\,\mathrm{cm}^2$, 16 SSAs, and 16 MPAs per module are necessary for the readout operation. To handle the clustering for a charge deposition across two ASICs, it can be beneficial to introduce a dedicated link between neighbouring ASICs transmitting the information related to the most peripheral channels. Besides, an offset, dependent on the module location, is required to be applied to centroids coordinates to correct the parallax error generated by approximating the cylindrical tracker geometry with planar pixel-strip sensors (see Section 4.3 for more details). To introduce those corrections, a lateral communication either or in both SSA and MPA becomes necessary.

The lateral communication has a cost mostly in terms of power consumption and assembly complexity. It requires additional transmitters, bumps and transmission lines on the hybrid for the SSA or even wire-bonds between the bumped dies for the MPA. For this reason, it is necessary to evaluate the stub recognition efficiency benefit.

Figure 3.21 shows three examples of situations where lateral communication in the SSA allows eliminating the boundaries errors. In the first case, a single particle cluster would generate two stubs instead of one. This effect could be compensated at back-end elaboration even if it introduces a bandwidth overhead, leading to saturation at lower occupancy. In the second case, a charged particle generates a large cluster. Particles with large curvature in the magnetic field can be eliminated (see Section 4.3)

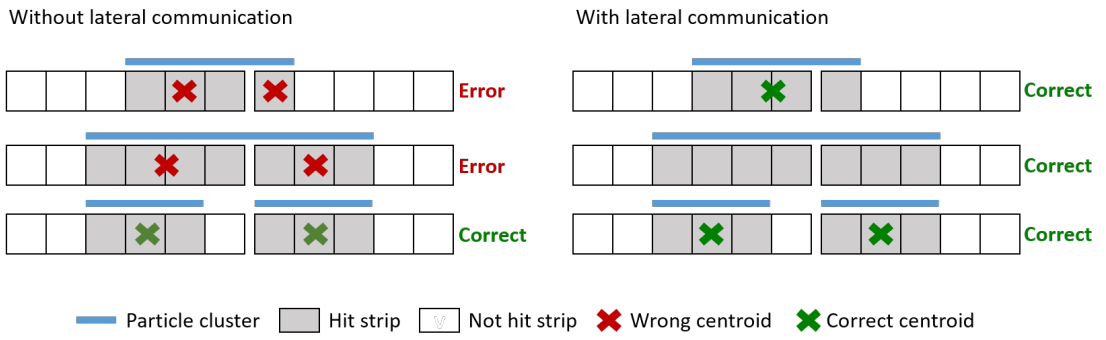


Figure 3.21. Example of cluster across neighbor SSAs.

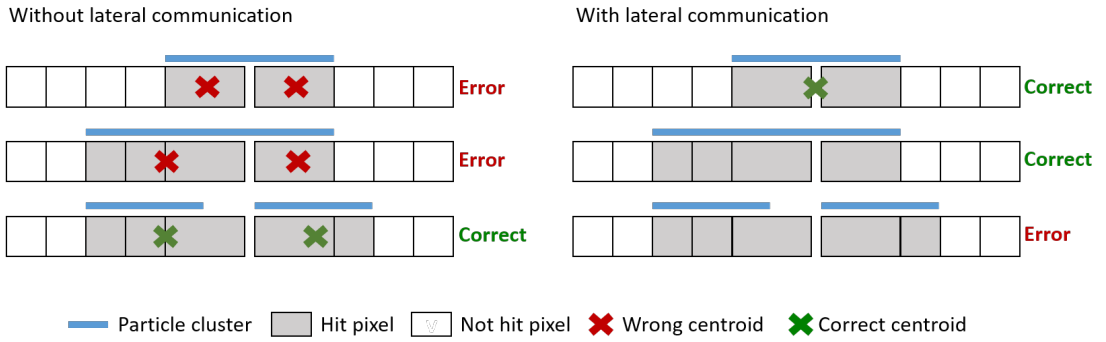


Figure 3.22. Example of cluster across neighbor MPAs.

with consequent saving in bandwidth and elaboration. Without introducing the lateral communication, such cluster will not be reject leading to a duplicated stub.

To evaluate the impact at the system level, the MPA+SSA model was simulated with and without the cross-chip clustering in the SSA. Figure 3.23 shows the stub recognition efficiency for different values of stub occupancy. The utilized ratio between stubs and pixel-strip hits due to particles that do not generate stubs is evaluated accordingly the Fluka 5.39 simulations. The clustering among neighboring SSAs allows for a recognition efficiency increment of ~ 1% independently from the occupancy, with the cost of two 320 MHz differential link per SSA.

The situation is different in the MPA ASIC where it would require 4 additional SLVS drivers to handle the clustering for the 16 rows, limiting to 8 clusters per BX. The simulation was repeated for the MPA, taking into consideration that, due to mechanical constraints of the assembly on the silicon sensor, the two most peripheral pixels are shorted together (to decrease the ASIC dimension accordingly the φ direction,

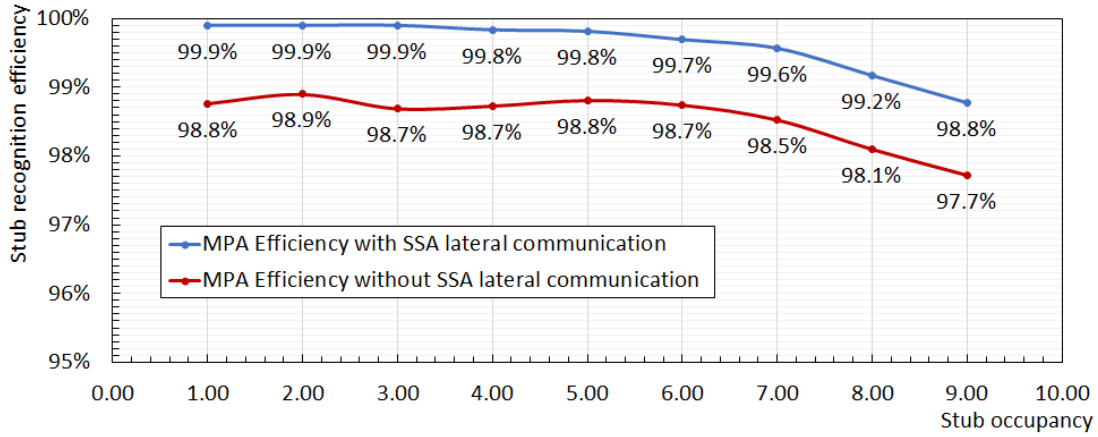


Figure 3.23. Stub recognition efficiency at the MPA output, with and without the SSA lateral communication and the clustering among neighboring SSAs.

allowing a margin of 100µm in the assembly procedure). Figure 3.22 shows the effect of the lateral communication in the MPA. In the first two cases, the clustering across neighboring chips allows to correct for the error, on the third case instead, two independent clusters are erroneously merged and eliminated.

The system level simulation framework permits to simulate the model to evaluate the predominant effect. It results that the lateral communication would increase not only the power consumption but also the rate of lost stubs of ~ 0.15%.

3.8.3 Particle cluster filtering and coincidence window

Considering the stub width S_W defined as the distance between the cluster centroid in the strip and pixel layers (see Section 3.8), the relation between the particle transverse momentum p_T and the stub width in strip units is well approximated by:

$$p_T = \frac{\sqrt{3}}{3} \cdot q \cdot r \sqrt{\left(\frac{\sin\theta_0}{\cos(\theta_0 - \alpha)}\right)^2 \cdot \frac{d^2}{(S_W \cdot l)^2}}$$

where θ_0 is the angle between the trajectory of the particle and the beam axis while α represents the angle between the normal to the module and the beam axis. q represents the particle's charge, l is the strip pitch given in millimetres, d is the distance between pixel and strip sensors and r is the radial coordinate of the center of the innermost sensor of the module.

It is possible to evaluate the stub window cut S_W^{max} that the SSA-MPA system has to apply to filter out all stubs induced by particles with a transverse momentum below a given threshold p_T^{min}, accordingly to the module position. Clearly a tighter cut will allow for a large reduction of the low-p_T stub rate, at the cost of a poorer momentum resolution at the back-end. On the other hand, large S_W^{max} may saturate the MPA and CIC bandwidth leading to efficiency losses due to missing high-p_T information.

To evaluate the impact of the window cut on the SSA-MPA bandwidth and the consequent stub recognition efficiency degradation, the system has been simulated for different stub occupancy and hit rates. Figure 3.24 shows the recognition efficiency at the MPA output in the assumption of a fixed bandwidth between SSA and MPA of 8 centroid coordinates per BX (2.56 Gb/s) and a bandwidth between MPA and CIC of 5 stubs every 2 BXs.

Figure 3.25 shows instead the tracker reconstruction efficiency for different window cuts, assuming no losses at module level. With a stub window cut of 2.5 SSAs-strips (green curve), the efficiency at 2.0 GeV/c is above the 99%. As the stub p_T resolution is not perfect, this cut enables the selection of stub coming from lower p_T particles. For instance, at 1.5 GeV/c the efficiency is still above 90%. A large amount of data due to low-p_T background is accepted. Reducing the S_W we can observe that the

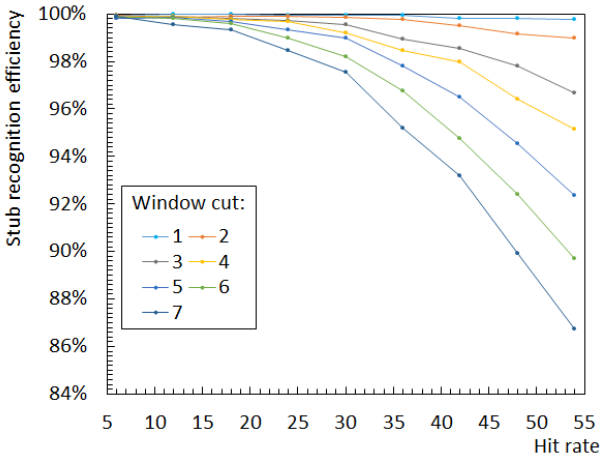


Figure 3.24. Stub recognition efficiency at the MPA output as a function of the particle hit rate, for multiple values of the stub window cut S_W^{max}.

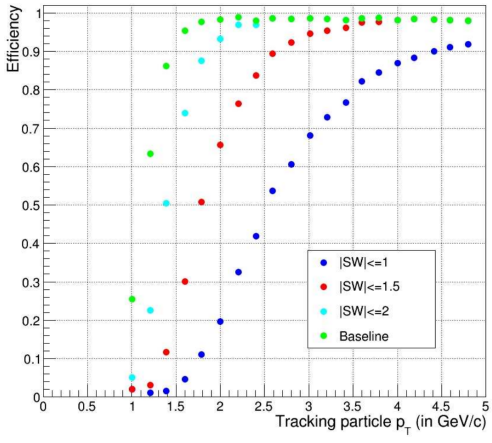


Figure 3.25. Stub efficiency in TIB1 for multiple window cuts S_W^{max} [201].

turn-on curve becomes less sharp, reducing the resolution. The light blue curve shows the turn-on curve for the same layer with an SW limit of 2 SSAs strips. The 99% plateau is reached at 2.5 GeV/c, so it is still acceptable for the L1 tracking ratio [194]. From the simulation in Figure 3.24 we can see that the losses due to bandwidth saturation for the hit rates expected in the same layer are reduced by 0.3%. A 2 GeV/c strips cut is reasonable for most detector locations. For more critical modules (as the innermost barrel layer or end-cap ring), or in the case of higher pileup, the losses due to bandwidth could be significant so a tighter cut should be applied. For the outermost radius, on the contrary, a lower cut is necessary to permit acceptable stub efficiency.

The following relation represents the particle transverse momentum dependency from the angular distance between the clusters on the pixel and strip layers δ_θ (measured in half SSA strips).

$$p_T = \frac{B \cdot r_C \cdot c \cdot d}{2\delta_\theta} \sqrt{1 + \frac{\delta_\theta^2}{d^2}}$$

where B is the magnetic field, r_C is the radius of the innermost cluster. For the outermost layers of the barrel, the bend cut corresponding to a stub p_T limit of 2 GeV/c is $\approx \pm 7$ strips. At this radious, the strip hit occupancy is lower ($< 0.8 \cdot 10^{-2}$ for pileup 200), never saturating the bandwidth. The SSA-MPA system needs to allow different stub window cuts according to the module location up to ± 7.

3.9 Description of the final PS module architecture

The block diagram in Figure 3.26 summarizes the chosen architecture for the PS module electronics. The combination of a strip and a pixel sensor requires the design of two different chips, the SSA and the MPA. The $5 \times 10\,\mathrm{cm}^2$ sensor area makes necessary 16 MPAs as well as 16 SSAs for the full module readout and consequently a chip for data aggregation called CIC. Mechanical and assembly issues are described in [20].

A Front-End (FE) stage, located in the SSA and MPA ASICs, reads-out the charge deposition on the silicon sensors and generate a pulse proportional to the particle charge. In the case of the pixel hits a discriminator allows to identify hits due to particles with an energy above a certain configurable threshold. On the other hand,

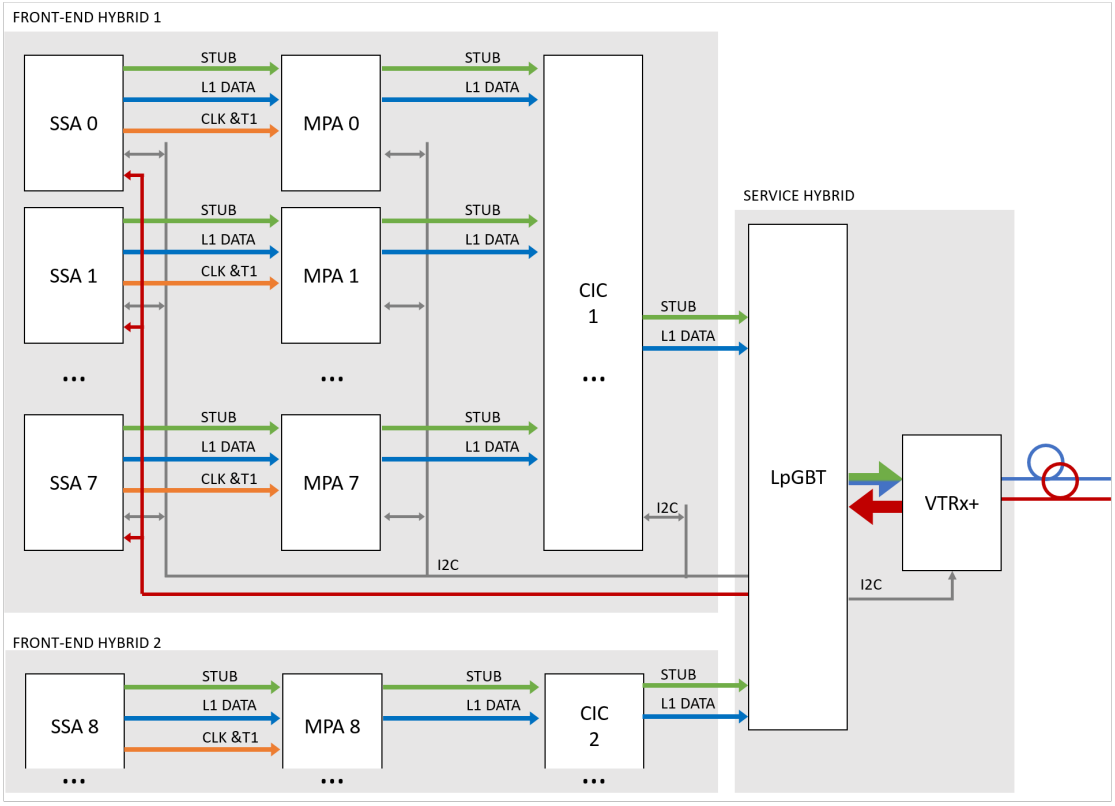


Figure 3.26. Block diagram of the PS module final architecture.

the SSA adopts ad a multi-threshold system to flag events due to High Ionizing Particles (HIP-Flags) for the reasons described inf in Section 4.2.

The information from both layers is then digitalized and split into two distinct data paths: the Stub data path and the triggered data path, implementing the concept described in Section 3.2. Figure 3.27 shows the final selected module architecture. In blueit the L1 triggered readout is represented while in orange the continuous transmission of stub data for the event reconstruction.

The SSA reads out the strip sensor with a double threshold binary system. Discriminator pulses are sampled with the 40 MHz bunch crossing (BX) clock and stored in an embedded memory element until the arrival of a L1 trigger. Detection threshold data, called strip data, are stored without any further compression, while HIP threshold data, called HIP data, are stored with an addition compression technique which limits to 24 HIP per BX.

Strip data from the detection threshold are also processed by the trigger data path

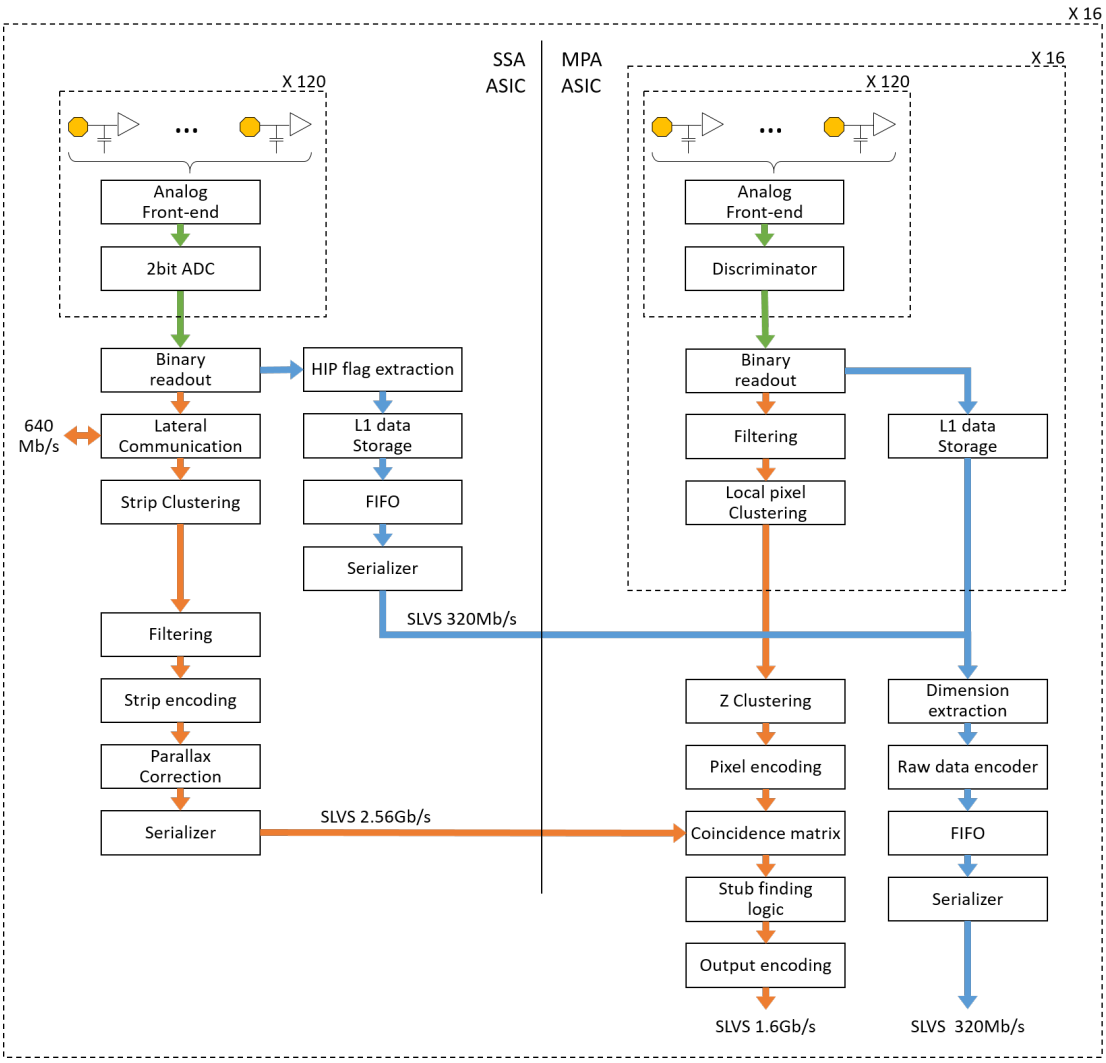


Figure 3.27. PS module final implementation diagram.

together with the strip data from neighbor chips. Two differential links, operating at 320 Mb/s, provide hit information from the two neighboring dies allowing the clustering among neighbour chips. Large clusters (approximately > 400 µm) are discarded, while the center positions of the remaining clusters are encoded. A configurable offset is applied to the centroids accordingly to the location of the module in the tracker volume. It allows correcting the parallax error generated by approximating the cylindrical geometry with planar sensors. This information is continuously sent to the MPA with eight differential SLVS links operating at 320 MHz. The total bandwidth between SSA and MPA is 2.88 Gb/s. The SSA transmits the L1-trigger and the synchronous commands to the MPA through a single differential link at 320 Mb/s.

The MPA reads out the pixel sensor with a single threshold binary system. As in the SSA, the pixel data are stored in radiation tolerant memory elements until the arrival of a L1 trigger. The L1 data logic processes events required by the L1 trigger. The same data processing is carried out on strip and pixel data: the cluster information is extracted and encoded with the position of the first pixel/strip in the cluster and its width. A HIP flag is added to the strip cluster to notify the presence of a HIP. L1 data are transmitted over a single 320 MHz differential link.

Large pixel clusters are discarded as in the SSA. The logic also gathers the strip clusters and selects only the pixel and strip cluster pairs which show a position difference below a certain programmable threshold to reject low-p_T particles and provides only high-p_T particle data to the detector back-end electronics. The position difference limit varies between 200 µm and 400 µm depending on the momentum threshold desired and on the module location within the tracker. The selected pairs are encoded as stubs which contain the position of the pixel clusters and the bending.

The MPA transmits the data in synchronous mode with five differential links and a bandwidth of 1.6 Gb/s. The stubs are aggregated over two consecutive bunch crossings,

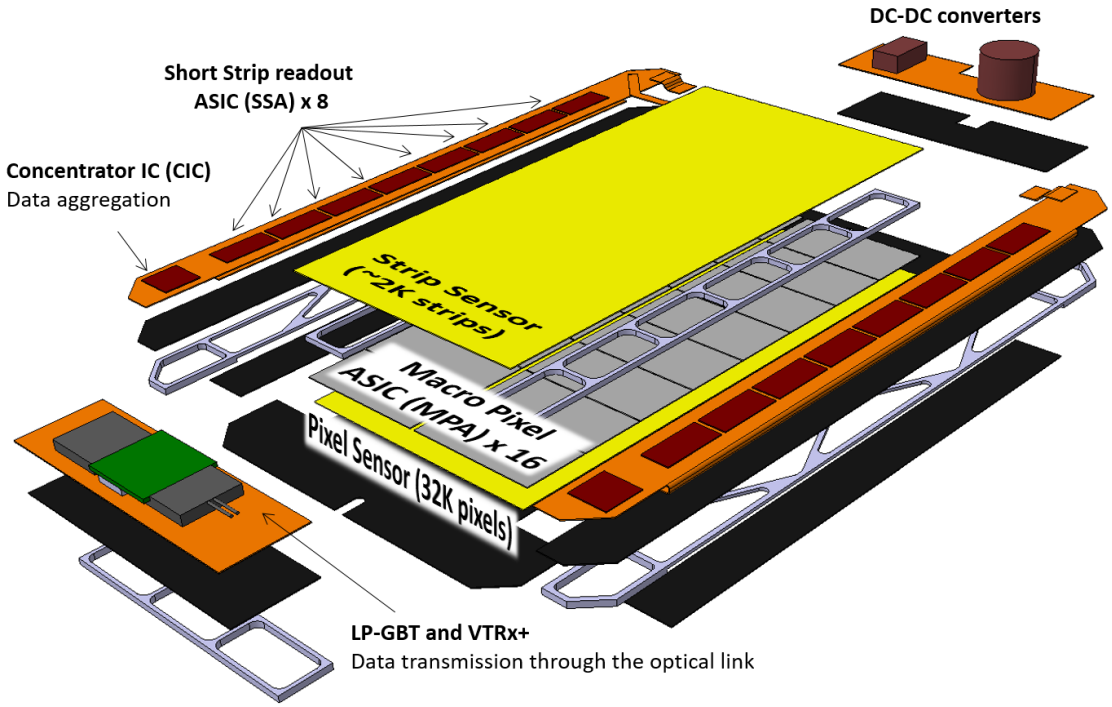


Figure 3.28. 3D rendering of the PS module.

hence smoothing the chip occupancy fluctuations in time. The total bandwidth towards the data aggregation chip (CIC) is 15.36 Gb/s.

The concentrator integrated circuit (CIC) [202] is the front-end chip for both PS and 2S modules. It collects the digital data coming from eight upstream FE MPAs and formats the signal in data packets containing the trigger information from 8 BX plus the raw data from events passing the first trigger level, and finally transmits them to the LpGBT [169] unit (rad-hard SerDes). Detailed technical specifications may be found in [191]. There will be 6 differential lines at 320-640 MHz between each CIC and the LpGBT. The 640 MHz lines will be required in the innermost detector regions in order to sustain lossless trigger data extraction. There will be two main structures in the chip: the FE blocks, and the output block. The FE block processes the data provided by each FE chip feeding the CIC. The output block groups the data retrieved from the eight FE blocks, and formats them in an output data packet. Output streams of trigger and L1 data are separate.

4 From the studies to the design of the SSA ASIC

This chapter describes the design and implementation of the Short-Strip-ASIC (SSA) for the readout of the silicon strip detector layer of the CMS outer-tracker Pixel-Strip (PS) module for the Phase-II upgrade in the high-luminosity LHC. The SSA operates in association with the Macro-Pixel-ASIC (MPA).

The SSA ASIC comprises a low-noise analog front-end followed by double-threshold discrimination circuits to detect and distinguish normal incidence particles from highly ionizing particles. Particle hits are sorted in clusters which are filtered using a programmable threshold aperture to reduce bandwidth and data processing. Encoded clusters are transmitted at the BX frequency to the MPA ASIC for correlation with hits from the pixel detector layer, thus allowing the on-detector rejection of non-interesting events with consequent data reduction by factor 20. Full sensor particle hits are also stored in the on-chip radiation tolerant memory, transmitted upon the reception of a L1 trigger command. Trigger rates up to 1 MHz and up to 16 consecutive L1 triggers can be accommodated without loss of triggered events. Readout mode, bias calibration and channel equalization are accessible via serial interface. An asynchronous operating is implemented to study and characterize the ASIC response to a know input charge.

To limit the power requirement, different data processing and storing architecture have been evaluated and compared according Monte Carlo generated stimuli to fulfill the very tight power consumption requirement of $< 60\,mW$.

A 65 nm technology has been selected as compromise between power consumption,

radiation tolerance and analog performances. The digital cell library has been characterized taking into consideration the temperature and radiation effects, and to evaluate the critical timing corners.

Radiation hardening design techniques have been employed to achieve the capability to resist up to an integrated ionizing dose of 100 Mrad. To mitigate the effect of radiation related Single Event Effects (SEE), the ASICs implement a Triple Module Redundancy (TMR) technique. The control logic, including the system clock (but not the sampling clock), and the configuration logic have been fully triplicated, while on the data only encoding techniques have been evaluated due to the power budget.

For the design implementation, a hierarchical Digital-On-Top flip-chip methodology was employed. A first silicon prototype incorporating all required functionalities for operation in PS modules has been realized in a 65 nm technology.

Publications related to this chapter: [2], [14], [4], [13]

4.1 Channel analog front-end

The silicon strip sensor can be modeled in first approximation with its capacitance, a diode and a constant current source representing the leakage current. The electrical field given by the sensor bias voltage imposes a drift current of the electron-hole pairs generated in into the sensor volume. A variable current source can be used to model the charge motion signal induced on the pixel. The signals depend on the physical properties of the sensor material, its thickness, the strip geometry and the charge deposition due to the particle interaction [85].

Two types of connectivity between the pixel-strip and readout electronics can be adopted. A DC-coupling has the advantage of simplifying sensor manufacturing. It requires the front-end electronics to be able to supply the detector leakage current from the input of the readout amplifier. A high level of dark-current will cause not only a higher level of noise, but could result in the total malfunctioning of the readout amplifier connected to the leaking strip. The usage of an AC coupling, on the other hand, requires extra processing steps in the manufacturing of the detector, in order to provide the DC bias for the readout strips (high-value resistors) and the capacitors for coupling the implanted diodes to the readout electronics [203].

Figure 4.1 shows a high-level block diagram of the analog front-end utilized to read out the charge deposited on a pixel or strip sensor. A charge sensitive amplifier represents the first stage. It has the purpose of converting the input charge Q_{in} into a voltage. The input of an individual readout amplifier will be loaded with the capacitance to the back-plane and two inter-strip capacitances with the neighboring channels. Assuming low input impedance of the front end electronics, which is required to collect all created charges efficiently, the total capacitance loading the individual

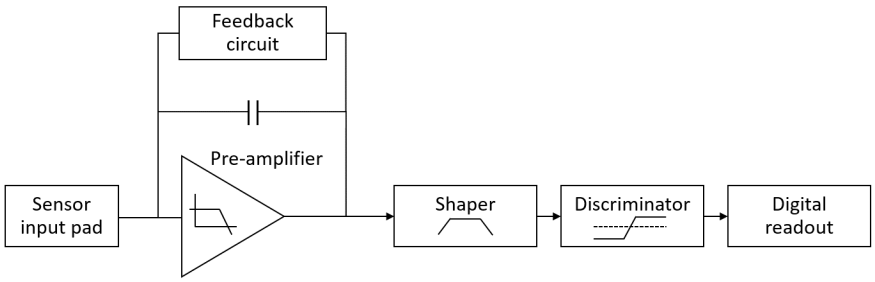


Figure 4.1. SSA analog front-end block diagram.

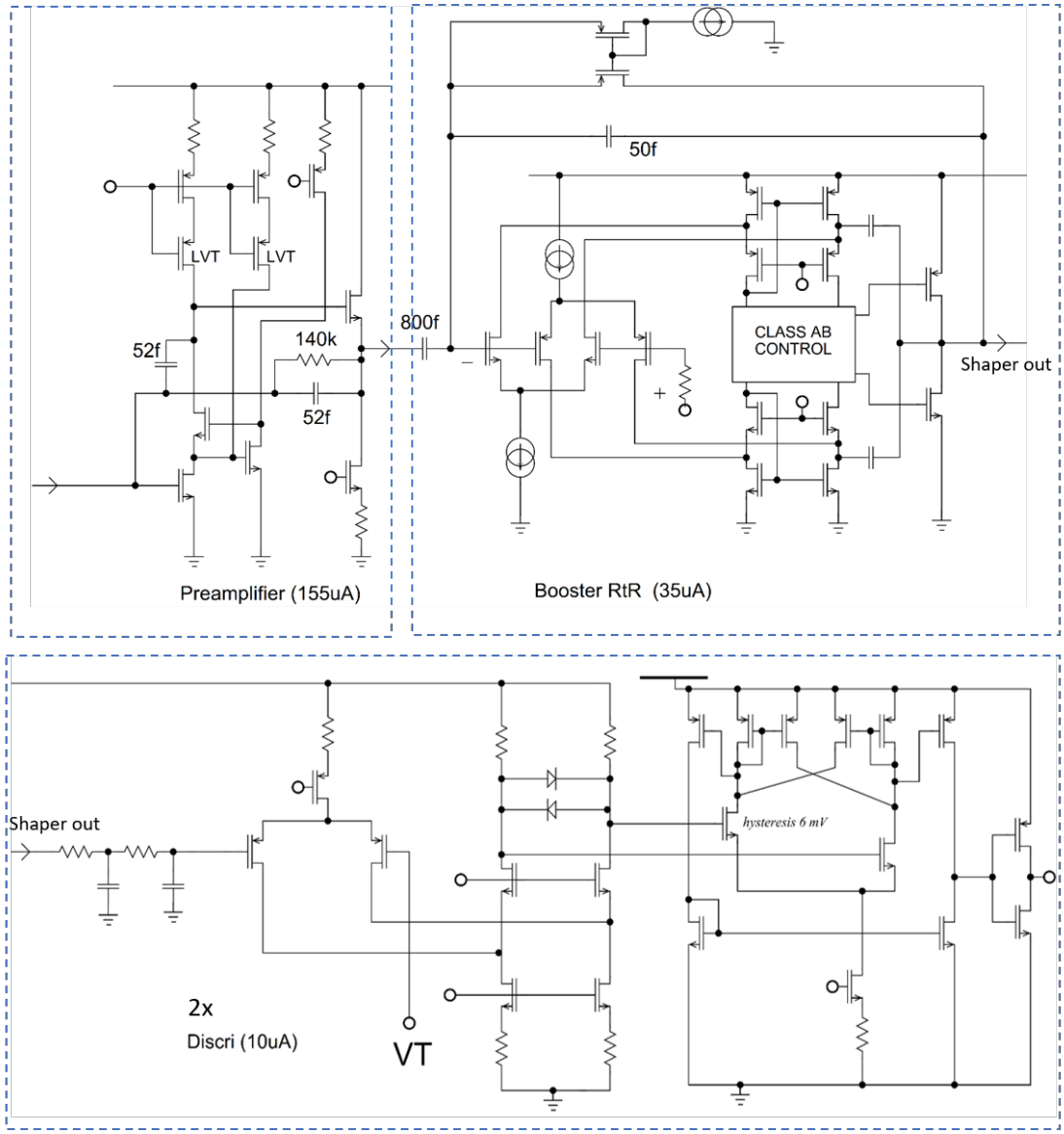


Figure 4.2. SSA analog front-end schematic.

amplifier input will be the sum of two inter-strip capacitances and the capacitance to the detector back-plane [204].

A feedback circuit is necessary to fix the DC operating point of the amplifier and to remove the signal charges from the input node. The discharging should be sufficiently slow to avoid degrading the shape of the signal at the output of the filter, and sufficiently fast to prevent the pre-amplifier saturation and non-linearity in the case of multiple consecutive hits.

In architectures where the pre-amplifier is DC coupled to the sensor, the sensor leakage current needs to be sourced by the electronics. Moreover, the input node voltage needs to be stabilized requiring a compensation circuit at the input node. In another case, the current would flow through the feedback circuit introducing a DC offset. For those reasons, for the SSA ASIC required to read-out the charge deposition on long strips that represent a high capacitance and high leakage current values, results more efficient to adopt an AC-coupling scheme. This approach allows to simplify the read-out electronics and to limit the equivalent noise values. In the case of the MPA ASIC instead, due to the lower dimension of the pixel, resulted more convenient to adopt a DC coupling avoiding to have for each pixel the required biasing structures and AC-coupling components. The amplification stage is followed by a filtering to limit the bandwidth of the signal in the output of the discriminator, and reduce the low frequency and high-frequency noise components introduced by the sensor leakage current. Higher order filters lead to shorter pulses for constant peaking time. This approach is convenient if high acquisition rates are required, in order to quickly restore the baseline. To avoid significant undershoots in the shaper response, often a pole-zero cancellation is adopted [85]. The signal in the output of the shaper is then ready to be digitalized.

The architecture of the single channel SSA analog front-end is presented in Figure 4.2. The channel consists of the trans-impedance charge-sensitive pre-amplifier, AC-coupled to the booster amplifier, enclosed with active-feedback providing attenuation of the overshoot. The amplified signal is applied through a passive low-pass filter to the inputs of the two-level discriminator. The first stage of the discriminator is built with a folded cascode differential amplifier loaded with resistors and swing limiter.

The common threshold voltage is applied to one of the input through a low-pass filter. The trimming voltage for the discriminator offset compensation is applied by the 5-bit current-DAC which supplies the current to the output of the booster amplifier, as a result of the low output impedance of this stage. It develops the DC drop voltage on the resistors used in the low pass filter. The peaking time and the gain can be adjusted by switching the capacitor matrix (4-bit resolution) in the RC filter.

The charge-sensitive pre-amplifier consists of a single-end regulated cascode chosen for its efficiency in terms of current consumption. The first stage is loaded with a degenerated pMOS self-cascode current source. The cascode M_C allows to stabilize

the voltage at the M_{IN} drain so the signal current flows to node generating the voltage signal. It allow increasing the output impedance and the DC-gain. An extra current source, supplying the input transistor, provides an additional bandwidth boosting.

The input device requires high trans-conductance to increase the bandwidth and to reduce the channel noise. It is implemented with a Triple-Well nMOS allowing reducing the coupling of the noise from the substrate into the sensitive input node. It features a 204 µm over 200 nm size biased with a 130 µA current, working in moderate inversion region.

The input and the cascode devices are layout with an enclosed geometry. The reason of this choice is to limit the leakage current after irradiation and in particular to limit the $1/f$ noise increase at high radiation levels, due to the interface charge trapped in the STIs [205]. The input transistor represents usually the dominant noise contribution, its size and its biasing condition must be chosen carefully [85]. A more detailed description about radiation effect and of the adopted design strategies in the SSA are reported respectively in Section 2.4 and in Section 4.6.3 of this manuscript.

A source-follower buffers the output signal to reduce the capacitive loading of the dominant node at the output of the gain stage, in order to increase the bandwidth. It simplify the transfer function by removing the direct path through the feedback circuit.

The pre-amplifier is enclosed with resistive and capacitive feedback (R_f = 140 Ω and a C_f = 52 fF) providing Miller compensation with poles splitting. The rise time of the pre-amplifier output signal depends in fact on its gain-bandwidth product and on the closed-loop gain, which is set, at first approximation, by the ratio between the sensor capacitance and the feedback capacitance.

The output voltage step can be approximated by:

$$\frac{\Delta V_{out}}{Q_{in}} \approx -\frac{1}{C_f}\frac{1}{1+\frac{1}{g_0}+\frac{C_{in}}{1+g_0C_f}} \xrightarrow{g_0C_f \gg C_{in}} \frac{1}{C_f} \quad \text{with } C_{in} = C_{detector} + C_{amp} + C_{par}$$

The condition $g_0C_f \gg C_{in}$ allows in particular to keep the voltage step at the input (ΔV_{in}) small and reduce the cross-coupling to neighboring strips via the inter-strip capacitance C_{s2s}.

The simulated open loop gain and the GBP of the stage are around 65 dB and 2.7 GHz respectively. The 60 mV voltage drop on the degenerating resistors, lowering the noise contribution from the active load, is compromised with the minimum voltage supply for the worst case process parameter corner and 1.15 V. The circuit is built with a mixture of regular threshold voltage (V_T), high-V_T, low-V_T devices, allowing for efficient use of the voltage supply (minimum 1.15 V, max 1.32 V).

4.2 Particles hit digitization

Following the analog conditioning, particle hits depositing a sufficiently high charge, could be detected. Further digital processing is necessary within the strip electronics. While the analog front-end implementation is usually similar between most of pixel or strip readout ASICs in literature, the digital processing and the readout architecture is strongly dependent on the target application.

4.2.1 A double threshold discrimination for high energy particles detection

To detect hits with a sufficiently high input charge, and to provide minimal information about the pulse amplitudes, the SSA implements a double level binary discriminator detection. All the interesting particles (for the standard physics) present a momentum (GeV/c $\propto \beta\gamma$) in the intermediate and higher regions, where the Bethe-Bloch formula well approximates the mean rate of ionization energy loss for charged particles (stopping power). For detectors of moderate thickness, as in the case of the SSA silicon strip sensor of 200 µm, the energy loss probability distribution $f(\Delta;\beta\gamma,x)$ (straggling function) is adequately described by the Landau distribution. The straggling functions in silicon for 500 MeV pions, normalized respect to the most probable $\Delta p/x$ were reported in Figure 2.7 for several values of the silicon detector thickness [80].

The average number of e^-h^+ pairs (J) is related to the deposited energy $\Delta$by J=Δ/P, where P represents the mean value of the energy needed for ionization, equal to $\sim$ 3.68 eV for the silicon [81]. The most probable number of e^-h^+ pairs generated for a MIP in silicon is 76 per 1 µm (see Section 2.3.1). A more detailed and accurate description of the charge generation and recombination in silicon can be found in

literature and will not be reported since it is out of the purpose of this chapter.

Figure 4.3 shows the signal distribution expressed in electrons for a minimum ionizing particle (MIP) and for a particle with a momentum equal to the double to the MIP momentum, simulated for a 200 µm silicon sensor from [206]. The red normal distribution, drawn on top, represents an example of the effect of the noise at the comparator input ($V^+ - V^- \approx 0$). The noise pedestal defines the lower limit to which could be set the detection threshold.

The low threshold, called detection threshold, is configured at the chip level and distributed to all channels. It is set as low as possible to maximize the detection efficiency but high enough to keep the rate of hits due to noise at an acceptable level. The nominal value for the SSA is around 0.7 fC.

All particles interesting for standard physics present an energy between the MIP and the Fermi plateau [15]. Physics beyond the standard model may present rather exotic

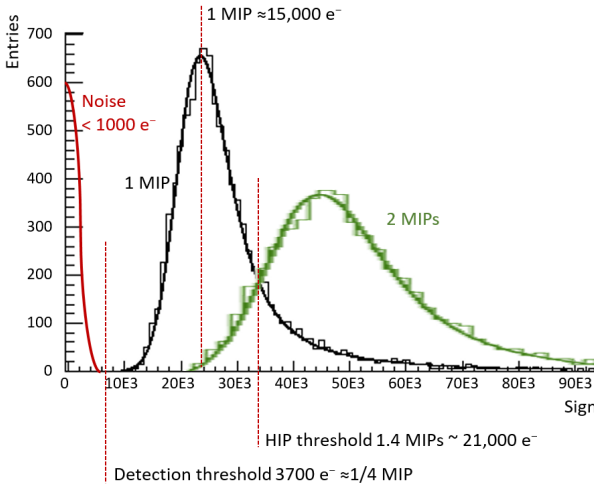


Figure 4.3. Signal distribution expressed in electrons for a MIP and for a particle with a momentum equal to the double to the MIP momentum, simulated for a 200 µm silicon sensor [206]. On the image are represented the optimal configurations for the SSA detection threshold ($\approx 3.7 \cdot 10^3 e^-$) and HIP threshold ($1.4\ MIP \approx 21 \cdot 10^3 e^-$)

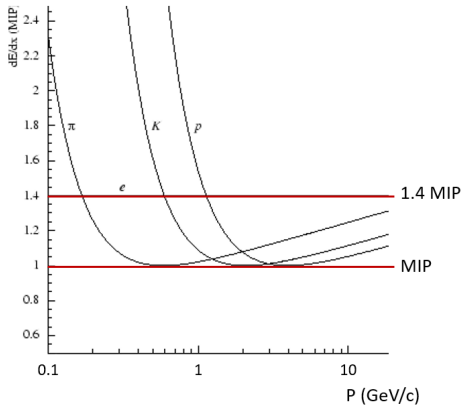


Figure 4.4. Most probable energy loss in silicon as a function of the charged particle energy, for different particles, for 200 µm silicon sensor, normalized to the minimum ionizing particle (MIP). The SSA 1.4 MIP threshold allows distinguishing most of the slow particles with substantial ionization.

signatures that may be undetectable with conventional analyses, and may involve the production of heavy and slow particles with large ionization [207]. For instance, such signature could be found in the production of heavy stable charged particles with rather long life time slowly traversing the detector [208]. Those products may strongly ionize the traversed sensor, leading to significant charge depositions. An example of such a particles can be found in the Split SUSY scenarios where the super-symmetric particles stau ($\tilde{\tau}$) and gluino ($\tilde{g}$) can have such characteristic signatures [209].

For this reason the SSA implements a second discriminator featuring a configurable threshold. This threshold will be set around 1.4 times the most probable charge deposited from a minimum ionizing particle at normal incidence, where it allows identifying hits due to High Ionizing Particles (HIPs). From Figure 4.3 it is evident that setting the threshold to this value, it is possible to maximize the HIP detection.

The two distribution overlap, so several measurements will be needed to reject lower energetic particles. The same concept is expressed by the example in Figure 4.4 where it is reported the average energy loss as a function of the energy for different charged particles. The higher threshold allows to exclude most particles with high energy, identifying heavy and slow particles with large ionization.

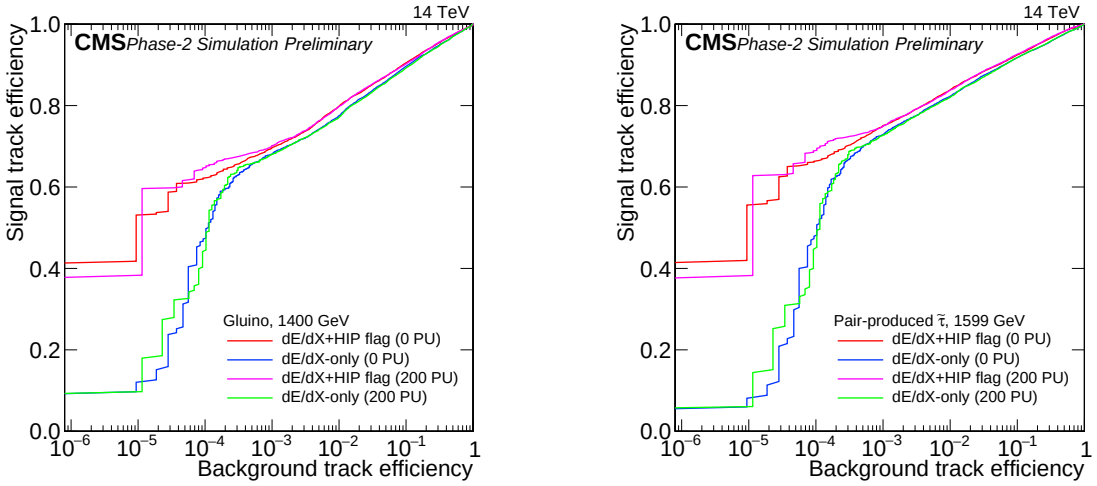


Figure 4.5. The signal track efficiency versus the background efficiency in selecting ($\tilde{g}$) and ($\tilde{\tau}$) [193] using data from the SSA HIP flag (purple, red) in addition to dE/dx data from the inner tracker, in comparison with a system trained to make use exclusively of data from the inner tracker (geen, blue) [193].

The HL-LHC will allow collecting large data sets of such events, even if the cross section for the processes is most likely very small. The Inner tracker detector readout ASIC implements time over threshold (ToT) measurement allowing for dE/dx measurements [210]. The SSA and MPA ASICs in the outer-tracker, instead, implement a binary readout due to the power budget limitations. To improve the sensitivity for signatures of anomalously high ionization loss, it is necessary that the SSA implements the additional programmable threshold and the consequent readout end encoding circuit.

The signal versus background efficiency performance curves in Figure 4.5 [193] shows that for a background efficiency of 10^{-6}, as in the analysis with the current detector, adding the HIP flag information from the SSA layers on top of the dE/dx measurement of the inner tracker, allows for a signal efficiency of 40%, approximately 8 times higher than without HIP flags [208]. In other words, to reach the same target without the HIP flags transmission from the SSA would be required a luminosity 64 times higher than in the phase-1 one, clearly not realistic.

Implementing a double threshold binary system in the MPA would have a significant cost in terms of power consumption, and no z resolution is expected to be needed for the analysis. The HIP threshold will be implemented only in the SSA.

4.2.2 Digital channel front-end

Figure 4.6 shows the block acting as interface between the analog front-end and the digital circuit. It synchronizes discriminator pulses with the acquisition clock synchronous with the 40 MHz event rate. From the outer-tracker simulations in the condition of $t\bar{t}$ events at pileup 200, we can evaluate the maximum average hit occupancy defined as the fraction of channels containing a digitized hit equal to $3 \cdot 10^{-2}$ for the micro-strip sensor and $2 \cdot 10^{-3}$ for the pixel sensor [9]. Considering that the particle hit cluster size is a Poisson variable with average 2, it is possible to calculate the probability of having more than one consecutive hit over threshold in the same strip due either for a particle hit on the strip or a particle hit in the proximity, resulting 4.7%. The error introduced by neglecting the second of two consecutive hits is clearly too high for the triggered data transmission. Slightly better is the situation for the stub generation where in average only 16% of the particle hits would generate

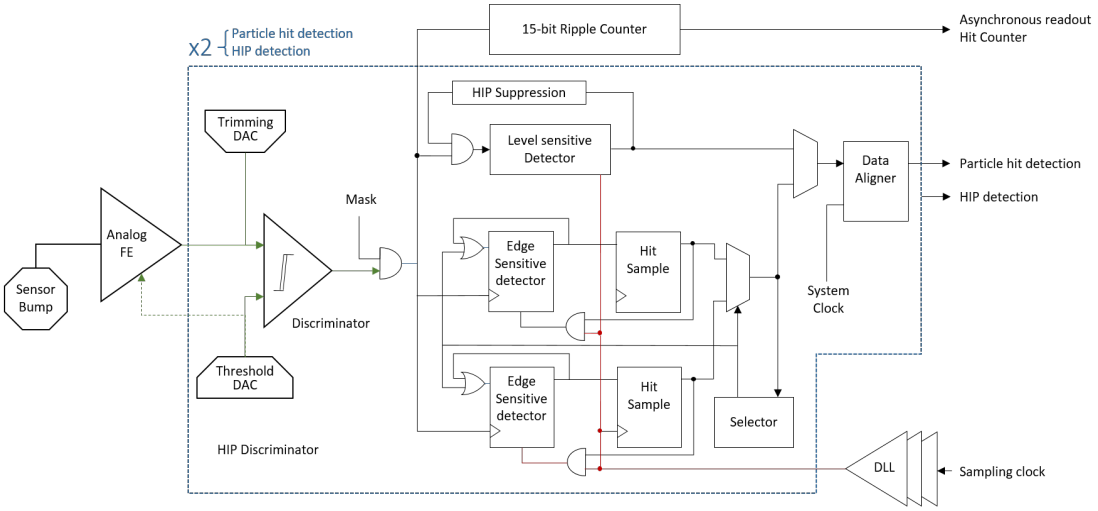


Figure 4.6. A block diagram of the SSA channel digital front-end. Following the analog conditioning of the charge-sensitive analog front-end, the signal pulse is digitalized. Two independent comparators define detection and HIP thresholds. The sampling combines a level sensitive featuring HIP suppression and edge sensitive binary readout. The sampling clock is de-skewed with 200 ps precision. A 15 bit ripple counter allows for asynchronous readout in calibration mode.

a stub (in the assumption of a 2 GeV/c p_T cut). On the contrary, in the case of the pixel sensor, neglecting the second of two consecutive hits lead to a data-loss of less than 0.31%. As a comparison the losses due to bandwidth at the CIC output for the same module location evaluated on the simulation framework described in Chapter 3 are in the order of 1.05%.

For this reason, for the MPA it was possible to relax the analog front-end shaper pulse rise-time and allow tails longer than 25 ns with consequent savings in terms of power consumption and design complexity. As well the binary front-end will not be required to sample two consecutive hits. In the case of the SSA instead, the front-end is required to limit the output pulse duration to less than 25 ns for any charge injected (or in the practice for any charge below 2 times the MIP).

The channel digital readout should guarantee as well the absence of dead cycles. As described in Image 4.6, after that the first branch detect an hit and produce the 1 BX long pulse, the second branch get activated and is ready to detect an eventual second hit on the same strip.

Two different operating modes can be activated independently: edge-sensitive and

level-sampling. In both cases, an additional flip-flop samples the first stage outputs with the rising edge of the 40 MHz sampling clock (Clk_{SMP}) syncronous to the bunch crossing.

A clock-domain crossing stage allows to synchronize the pulse with the ASIC clock distribution. In order to keep constant the latency and allow the correct sampling for any phase of Clk_{SMP} with respect to the system clock (Clk_{SYS}), a single or double stage re-sampling is inserted accordingly to the coarse deskewing and the DLL settings. The Clk_{SMP} phase is in fact controlled with 200 ps resolution across the 25 ns period for the reasons described in Section 4.2.3.

The level sampling does not allow distinguishing between consecutive particle hits and a single hit due to a HIP. In the latter case the deposited energy may be well above 2× the MIP one, and the shaper output voltage can be higher than the detection threshold for much more than 25 ns. A HIP suppression circuit rejects the tail of long pulses if the front-end pulse is above the HIP threshold and, at the same time, the comparator pulse is longer in time than 75 ns.

A set of registers per channel allows to store the configuration values. The registers are accessible via the Wishbone [211] interconnect fabric. Example of configurable parameters are: the trimming value for the thresholds adjustments (5 bit DAC per channel), the peaking time trimming (5 bit DAC per channel), the sampling mode control, the HIP suppression threshold, the strip mask (in case of noisy channels) and several other front-end controls and testability functionalities. In addition, 16-bit test vectors can be loaded for each channel interface to internally exercise the digital functionalities of the ASIC in calibration and testing phase.

4.2.3 Timewalk and clock de-skewing

The difference in time between the charge injection and the hit detection depends on the time dispersion of a discriminated pulse due to the combined effect of the pulse heights spread and the single threshold discrimination. It is generally referred to as timewalk. Due to the response time of the discriminator and the rising time of the amplifier of the SSA, hits with high amplitude (i.e. HIPs) lead to faster response compared to pulses just above threshold. The timewalk is, therefore, a function of the input charge.

Let us assume that the threshold is set at a specific value over the noise baseline as in Figure 4.7.a where a threshold is drown over the shaper output pulse obtained by simulating the single channel analog front-end for different charge values. Let us assume as well that the front-end is required to generate and transmit a hit for any pulse shape due to a charge deposition over 4 fC. It is evident that if the sampling of the pulse happen too close or too far from the charge injection, only pulses with high rising and falling time get sampled correctly. Slow rising pulses due to lower energetic particles are not detected. To guarantee that all charge deposition above the MIP average one is sampled correctly, the rising edge of Clk_{SMP} should follow within the unitary efficiency window. Figure 4.7.c represent an explanatory drawing of the efficiency of the hit sampling for a $-150\,mV$ threshold. For higher thresholds, the time-window become narrower leading to inefficiencies. The threshold should be set high enough to reject most of the noise hits.

In other words, the analog front-end should guarantee a good signal to noise ratio and a large enough time-over-threshold for input charge above the minimum detectable charge. The sampling clock should have enough timing resolution to guarantee unitary sampling efficiency. The time window needs to be large enough to provide margin for the clock jitter and for the channel to channel mismatch.

Process, voltage, temperature and radiation dose related variations do not allow to implement a clock tree distribution that guarantee a sampling in this range for all corners. In addition, modules located in different areas of the tracker will detect hits with different delays due to the particles time of flight (ToF). For this reason, the Clk_{SMP} phase is controlled on chip and a two-stage de-skewing is implemented. During the study phase of the SSA architecture, it has been required to the DAQ system to provide coarse control of the Clk_{SMP}-phase encoding in the fast-control commands its relation with the 320 MHz system clock. The sampling phase between modules is then equalized with a 3.125 ns precision. A loop-back mode implemented in the module allows the DAQ FPGAs to evaluate the cabling propagation delay. The variability introduced by the long cabling between the tracker layers and the CMS DAQ system located out of the cavern would not allow for an higher resolution. The on-module phase spread and the ToF is therefore compensated on-chip. The finer de-skewing is achieved as a result of an internal Delay Looked Loop (DLL) which allows, in combination with the coarse de-skewing, to achieve a 200 ps resolution over the whole 25 ns period. This resolution is sufficient assuming a $< 200\,ps$ clock jitter

in the worst case. The area occupied by the 120 strips in the case of the SSA is small enough to neglect the ToA difference.

During the implementation phase, it was necessary to guarantee that the skew of the clock at the front-end channels input is below the < 200 ps. Section 4.6.7 provides a

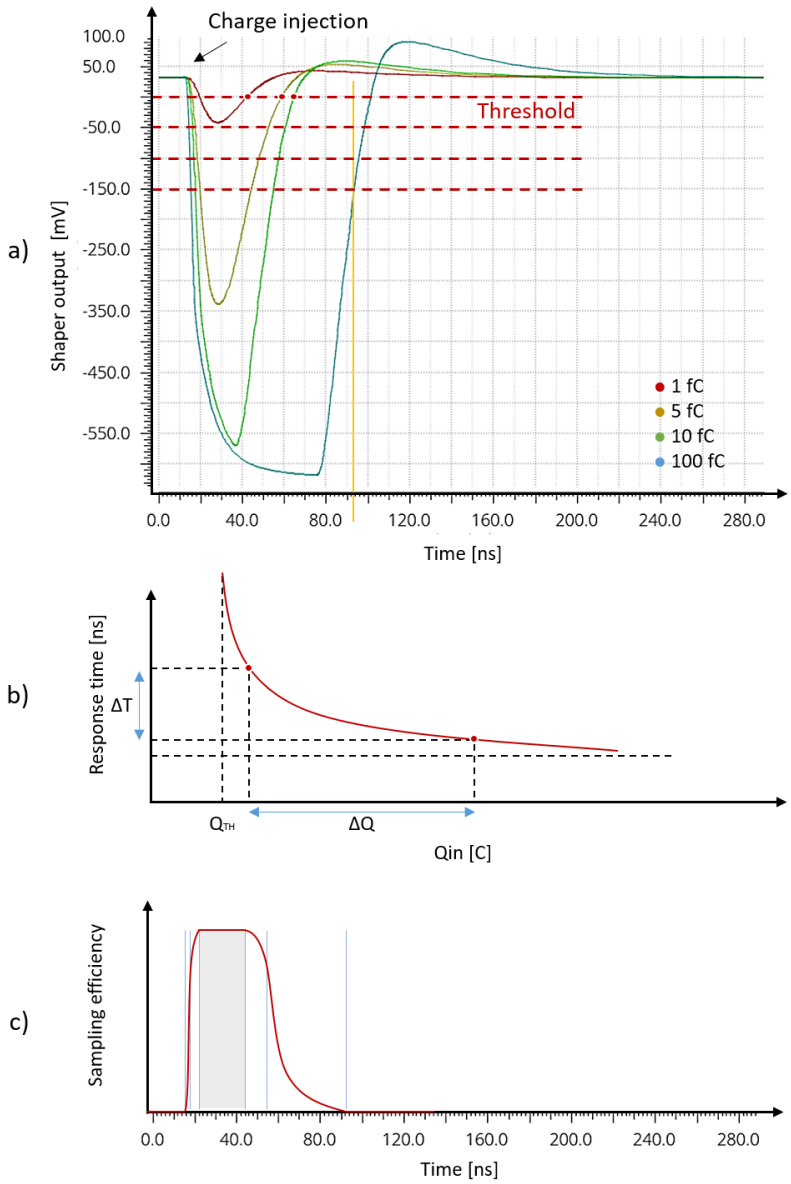


Figure 4.7. **a.** Shaper output pulse obtained by simulating the single channel analog front-end for different values of injected charge. – **b.** Front-end response time. – **c.** Efficiency of the hit sampling for a −150 mV threshold (drawing for explanation purposes).

description of the clock tree.

4.2.4 Asynchronous readout and channel equalization

To compensate the strip-to-strip threshold mismatch, a threshold equalization circuit is implemented. A 5-bits trimming DAC per channel allows injecting a current to the output of the booster amplifier, compensating for the discriminator offset.

The SSA implements a calibration system to evaluate the configuration value for the trimming DAC and to verify the correct operation of the ASIC during the test phase (when no sensor is available). A block diagram of the calibration circuit is shown in Figure 4.8.

Each channel input is equipped with a 52 fF calibration capacitor to a common chopper circuit through a switch controlled by the channel configuration registers, allowing to inject a known charge to the front-end channel input. An 8-bit DAC supplying a current to the 4.6 KΩ resistor controls the voltage on the capacitor terminal. The DAC is designed to guarantee an integral non-linearity (INL) of less than 0.5 LSBs.

A strobe signal, generated by the fast-command decoder module, allows triggering the charge injection. The "test-pulse" command is encoded in the synchronous commands received by the ASIC along with the L1 trigger, and others. The pulse duration is controllable by configuration as a result of a mono-stable circuit with a resolution of 3.125 ns.

A 6-bits delay line (DL) allows for the control of the injection phase. The DL design is based on a chain of current-starving inverter cells. The schematic of the DL design is presented in Figure 4.9. A 5-bits DAC controls the bias currents of the inverter chain allowing for compensation of the process parameter variation. The DL is capable to span from 1 ns to 30 ns, covering the whole bunch-crossing cycle.

A 15-bits asynchronous ripple counter per channel, connected to the low-threshold discriminator output, counts the number of hits within the shutter opening period (controlled as well by the fast-command interface). Via the internal wishbone fabric, the counters values are transferred from the channel cell to the ASIC periphery.

In the calibration mode, the counters values can be streamed-out via the stub data

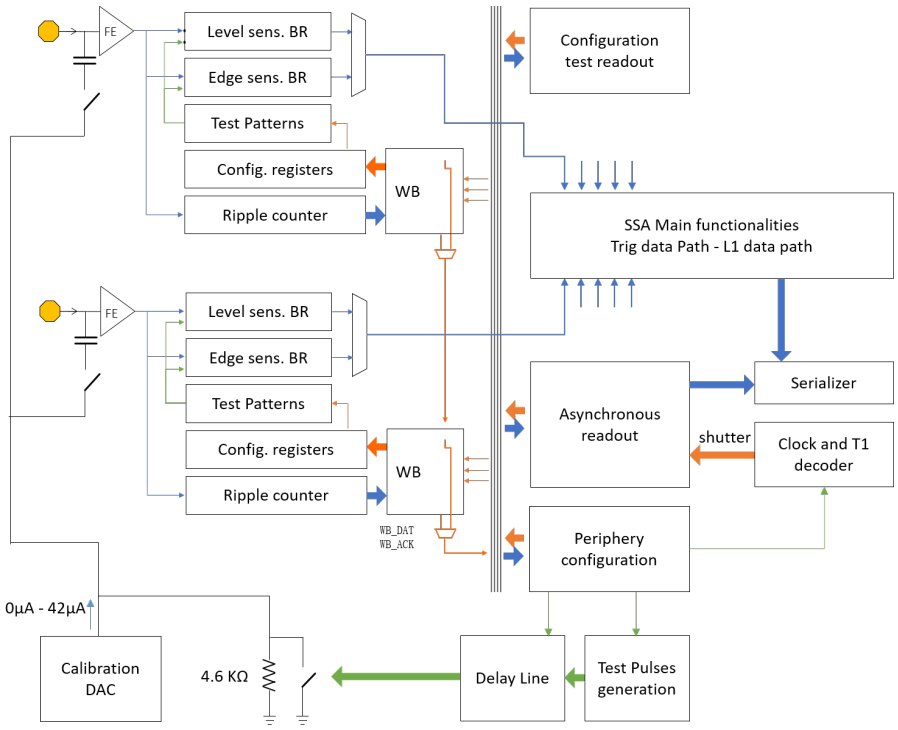


Figure 4.8. Block diagram of the SSA calibration circuitry and asynchronous readout data path.

path links to the experiment back-end. Since the MPA, the CIC [191] and the LpGBT [212], agnostic of the SSA operating mode, will need to re-buffer the packet, the transmission format and timing is optimized to guarantee no filtering along the chain. The CIC, in fact, perform an averaging between the data received over 8 BXs by the 8 FE ASICs to achieve a stub data compression from 25.6 Gb/s to 1.92 Gb/s.

By varying the threshold DAC value and the injected charge, it is possible to study the front-end response and the channel effective thresholds, allowing for the channels equalization even when no sensor is connected. The number of events sampled by the channel asynchronous counters for a known injected charge, and for different values of the threshold DAC, represents the probability of sampling a hit as a function of the threshold voltage.

Injecting a large number of calibration pulses into the SSA channel input and reading out the asynchronous counters, allows characterizing the front-end. In the ideal case when no noise is involved, it would lead to a step function shape. In the reality, assuming the noise contribute as a normally distributed variable, $V_{CompIn} = V_{peak} +$

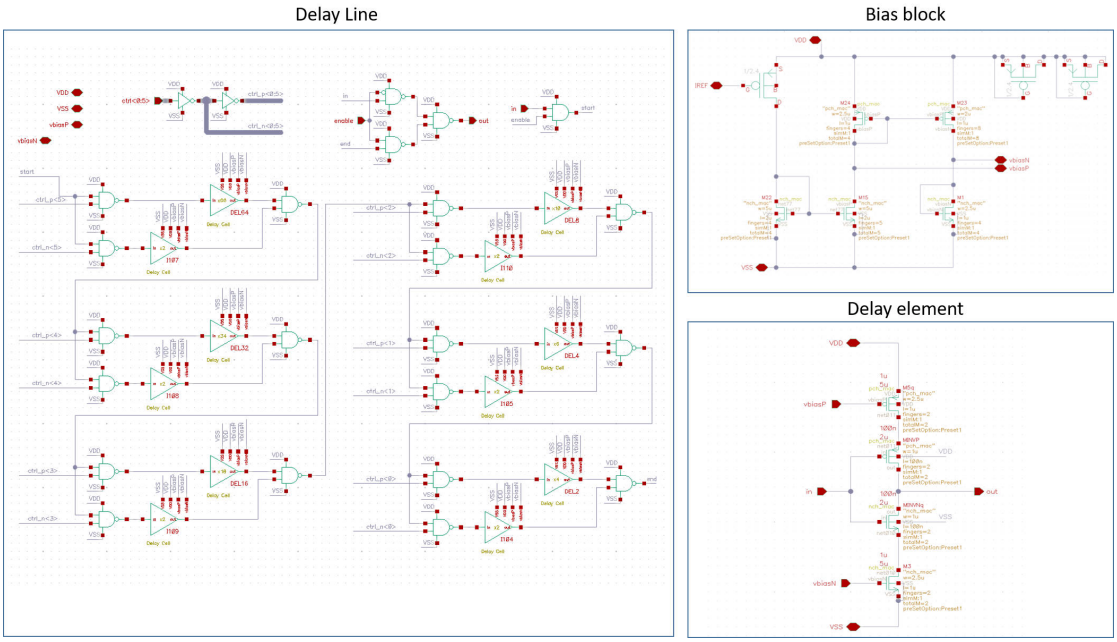


Figure 4.9. Schematic of the delay line (DL) design for calibration pulse injection control.

v_{noise} the curve represents the probability of V_{CompIn} to follow in the range $[V_{TH}, \infty)$. A complementary error function can, therefore, approximate it:

$$\text{Hit Count}_{\text{CH}}(V_{TH}) = \frac{2}{\sqrt{\pi}} \int_{V_{TH}}^{\infty} e^{t^2} dt$$

The standard deviation of the S-curves close to the threshold is proportional to the comparator input noise. The threshold value corresponding to the mean value of the S-curve for each channel represent the effective channel threshold. Due to on-chip mismatch, a variability between channels is expected. The SSA calibration circuit implements a 5-bit trimming DAC per channel capable of compensating for such a variation.

The dynamic range of the DAC is required to be sufficient to compensate for the maximum on-chip variation expected, with a resolution higher than the threshold DAC itself. A description of this procedure from the computational point of view is described in Chapter 5 along with the front-end characterization results.

4.3 Continuous transmission of high-p_T-particle primitives

When a high-p_T particle crosses the two parallel sensors it will generate hit clusters within a predefined range. The correlation logic located in the MPA ASIC evaluates the difference in the two layers centroids x coordinate. If the distance is below the defined p_T threshold, it generates a stub. The stub is composed by the x and z coordinates of the cluster centroid and by the bending information obtained as the difference in the centroid location in the two layers.

Particles with low energy and therefore large curvature in the CMS magnetic field may lead to charge deposition in several adjacent strips (Figure 4.10). Besides, a charge deposited by a particle on a single strip may induce parasitic signals on the neighbor strips due to the inter-strip capacitance as described in Section 4.1. This latter effect (cross-talk), may lead to errors in the reconstruction algorithm and to a substantial increase of the data produced.

To compensate for both those effects, the SSA performs a fast combinatorial clustering of the hits at the 40 MHz event rate. Particles with high traverse momentum and energy in the interesting range, have low probability to generate clusters larger than 400 µm, depending on the module position within the tracker and the distance from the collision point. The SSA can eliminate broader clusters at this stage with consequent

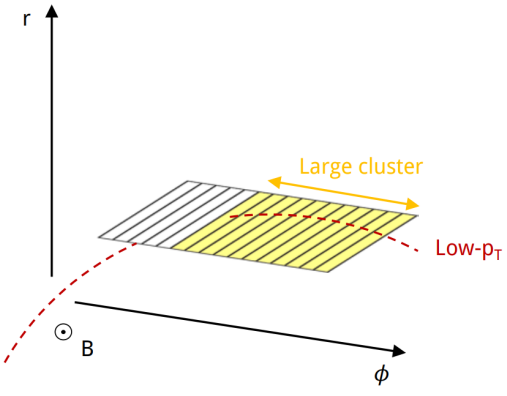


Figure 4.10. Example of a large cluster caused by low-p_T particle.

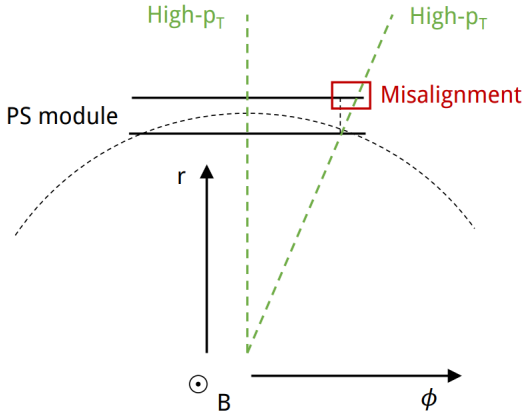


Figure 4.11. Example of the misalignment caused by approximating the cylindrical geometry of the tracker with a planar sensor.

save in terms of bandwidth and data processing power.

The cutting threshold can be configured. This operation may introduce an inefficiency when multiple particle trajectories are close to each other appearing on the sensor as a single wide cluster. However, this effect is negligible on the tracker event reconstruction, when the primitives from all the outer-tracker layers are combined together.

Since 1920 strips disposed within two columns compose the PS module strip sensor, 16 SSAs per module are necessary for the readout operation. To handle the clustering across two ASICs, the SSA implements a lateral communication path transmitting the information related to the eight most peripheral channels to the neighbor chips via a dedicated differential link operating at 320 MHz. Simulation studies in Section 3.8.2 shows the effects of the lateral communication the stub recognition efficiency.

The clustering needs to be implemented for each clock cycle over an input vector of 136 bits, considering the 120 channel detection-threshold signals, plus eight strip hits received from the two neighbouring SSAs. One clock cycle is required to perform this operation. Several combinatorial steps are implemented. The first stage of the clustering consists in identifying the transitions within the strip hit vector. For each channel are in parallel evaluated the outputs of the seven consecutive channels up to the first transition.

For the not filtered clusters, SSA calculates the coordinates of the centroids with half-strip precision. The operation is performed with a combinatorial priority encoder topology. The priority encoder can generate and order the coordinates of up to 8 clusters per bunch crossing. This number was selected as a compromise between the data loss probability and the power constraints. Section 3.8.1 shows the simulation results based on Monte Carlo events.

Other architectures for the centroid encoding have been evaluated. For instance, an approach based on a Mephisto encoder [213] topology, as was selected in the MPA ASIC [214], was studied. The Mephisto structure indeed is more power and area efficient, but it requires 4 BXs to encode the 8 coordinates (it can process up to 2 coordinates per clock cycle). A priority encoder topology instead can elaborate up to 8 coordinates in one single BX allowing to reduce the data latency. The coincidence logic in the MPA needs to wait for the coordinates from the SSA to evaluate the stubs.

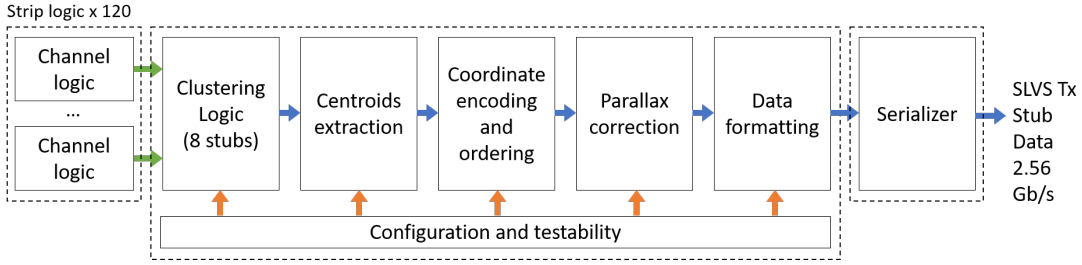


Figure 4.12. Block diagram of the SSA Stub data path (untriggered transmission of high-p_T particle primitives.)

Form a power evaluation it is noticeable that an increased latency in the SSA that would require a deeper FIFO at the MPA input, would have a stronger consequence on the total power consumption of the module. The FIFO on the MPA input should have, in fact, a width of 1926 bits.

An offset, dependent on the module location, is applied to centroids coordinates to correct the parallax error generated by approximating the cylindrical tracker geometry with planar pixel-strip sensors as described by Figure 4.11. The value of the offset depends on the distance from the nominal interaction point and the spacing between the sensors. A programmable shift must be applied to one of the two layers depending on their module coordinates. For a particle from the primary interaction point, the parallax correction (par) is given by:

$$par = \left(CL_{strip} - \frac{N_s}{2}\right) \frac{d}{r\sin\alpha + (z - z_0)\cos\alpha}$$

where Cl_{strip} is the coordinate of the cluster centroid on the strip layer, N_s represent the number of strips/pixels in the silicon sensor, r and z are the cylindrical coordinates of the center of the innermost silicon sensor, α is the angle between the beam axis and the normal to the module, d is the spacing between the sensors. The parameter z_0 represents the longitudinal impact parameter. In practice the origin of the particle is not known by the electronics in the SSA. The error introduced by approximating $(z - z_0) \approx z$ is

$$\epsilon = \left(1 - \frac{z_0}{z\tan(\alpha) + r}\right) < 25\% \quad \forall z$$

Figure 4.12 summarizes the SSA stub data path. The whole path composed by cluster-

ing, encoding, and parallax correction was split in a total of four pipeline stages as a compromise between the power consumption in the SSA itself, and the introduced latency that leads to higher power consumption in the following ASICs. The constrain is in fact on the total module current. Four pipeline stages are also adequate for the timing closure considering the 100 Mrad, slow-slow corner.

4.4 Triggered data readout

From the calculations based on Monte Carlo simulated events result that locally storing the raw information in the readout ASICs and transmitting elaborated and encoded data only when required by the L1 accept signal, allows to minimize the overall power consumption of the SSA+MPA chip-set. Detection threshold data, called L1 data, are transmitted without any further compression, while HIP threshold data, called HIP data, are transmitted with an addition compression technique which limits to 24 HIP flags per BX. The studies on the triggered readout data path at the system level are described in Section 3.7.1).

The embedded data storage element, located in the periphery of the SSA, stores the full raw sensor image for the time required for the trigger data-processing. It is configured to operate as circular buffers allowing to readout the raw information relative to the event stored 12.5 µs before the L1-trigger signal arrival. The latency value is configurable. When an L1 trigger decision is received, encoded in the fast-control input differential line, the raw data is transferred to the processing logic where is prepared for transmission. If after the latency period no L1 trigger requires it, the event is discarded. Consecutive locations stores the events for each bunch crossing. When the memory write-pointer reaches the word corresponding to the latency time, the pointer is reset, and the locations start to be overwritten.

4.4.1 Power optimization

The event storing methodology is a critical aspect in terms of power consumption. The event storing happens for every event so at 40 MHz rate while the read operation happens at the 750 kHz trigger rate. The first decision to take into consideration concerns the choice between implementing the memory element using a distributed flip-flop/latch based register file, or embedding a static random access memory

(SRAM) in the periphery of the design.

The radiation tolerance is as well a concern that should be evaluated in the choice together with the power requirements. The Single Event Upset (SEU) probability is directly proportional to the time window that the data spend in the memory. Applying redundancy to the memory element (triple module redundancy or forward error correction) is not preferable due to the power budget. Soft errors on the data bits are not critical since do not affect the system functionalities but can affect the track reconstruction if the bit error rate is greater than a few parts per million.

L1 data path with embedded SRAM and memory gating

The development of the radiation tolerant SRAM compiler in 65 nm technology is the result of a collaboration between CERN and IMEC institute [215]. The specifications provided for the memory requires dual-rate operations at 80 MHz, the capability to tolerate total doses up to 200 Mrad and a Linear Transfer Energy (LET) threshold > 15 MeV$\cdot$cm^2/mg. The design make use exclusively of standard-V_T devices, occupies the lowest four metal layers, and supports simultaneous read and write operations (dual rate).

TID effects as drive loss and V_T shift are limited avoiding the use of minimal width transistor. nMOS are larger than 200 nm and pMOS than 500 nm. The hardening for SEE of the addressing circuit is done by drive strength, while protection against latch-up is reached by placing p+ guard bands between n- regions. These strategies impact the area and the power consumption of the SRAM. The penalty in terms of area is not a problem for the SSA design where the ASIC dimensions are constrained by the sensor input-lines pitch on the hybrid flex design (neither in the MPA where the pixel-sensor define the dimensions). The power consumption, on the other hand, must be carefully evaluated. The power simulations on the memory provides the cost per operation: considering a write frequency of 40 MHz and a read frequency of 750 kHz, the total power consumption for a single 128 bits × 512 words memories in the typical case is 6.87 mW. If considering that between SSA and MPA designs would be necessary to use 18 memories of this size, the power consumption of just the storage element would require ≈123 mW, equivalent to 50% of the available power budget.

A possible technique to reduce the power consumption consists in gating the mem-

ory taking advantage of the low hit occupancy in the outer-tracker. As previously explained, the memory element can be controlled circularly, each location stores the event corresponding to a specific bunch-crossing cycle. By using an OR-tree, if a hit is detected a write operation is executed, otherwise the clock to the memory is gated. Since the memory is not re-written at every cycle, once the pointer has completed a full circle, the control logic could erroneously read out an outdated value. A tag should be saved along the data word to identify the location update time. When an L1 trigger occurs, the L1 process logic reads out the memory location and compare the tag. If the data stored in the memory location refers to an event occurred n_{TL} cycle before (where n_{TL} represents the trigger latency expressed in clock cycles) the value is processed. In other cases, means that no particles hit occurred during the required cycle and therefore the value is discarded. Since the tag is implemented with a synchronous counter, the control logic needs to refresh every 3 ms the full memory content by disabling the OR logic before that the counters overflows. The power consumption gain obtained by applying this method strongly depends on the hit occupancy and memory segmentation.

The estimated strip hit occupancy is $\sim 1.8 \cdot 10^{-2}$ for the external tracker barrel layers. The probability of having at least one hit in the event is $\approx 57\%$ Considering the overhead of the gating and control logic, to apply the gating technique to the whole memory does not necessarelly bring advantages. The situation is different for the HIP flags since their probability is approximately two order of magnitude lower than the hit probability. The estimated power consumption is ~ 6 times lower compared to the use of the same memory without applying any gating technique.

L1 data path with latch memory

Another possible approach may consist of utilizing a memory composed of latches. In typical applications as a processor data memory where the activity is typically above 10%, it is evident the power convenience of using a RAM compared to a register or latch implementation. A latch implementation could be potentially more optimal if considering the occupancy levels on the particle hit data.

Figure 4.13 shows the memory power consumption as a function of the average fraction of channels containing a digitized hit, for a 128×515 bits memory segmentation. The power estimation was obtained exercising the a place&routed instance of the

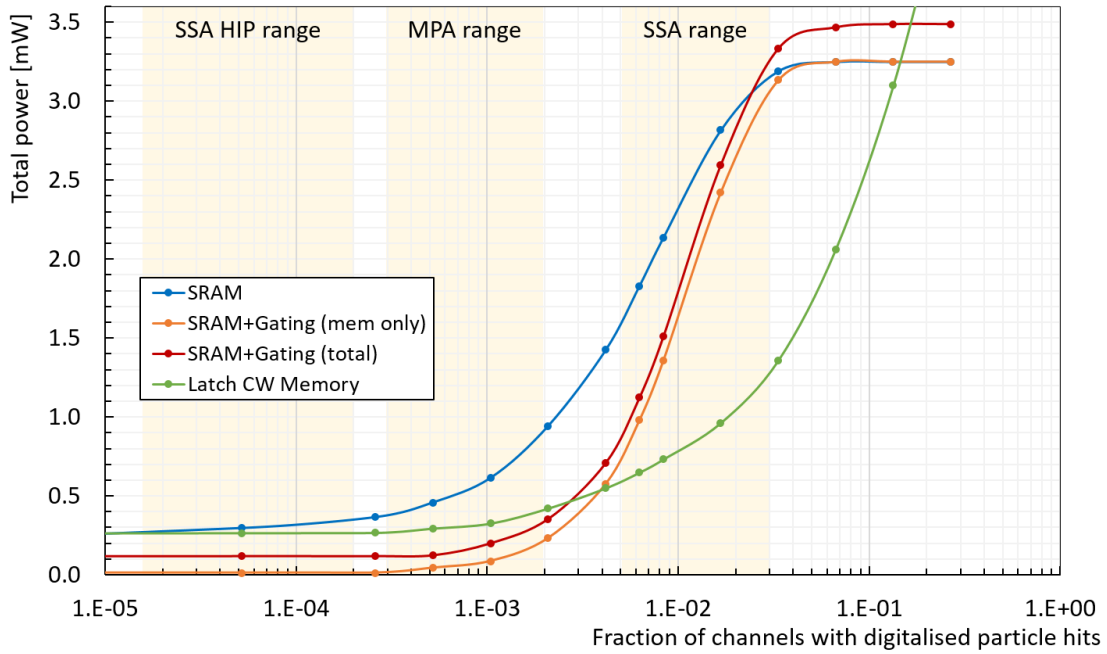


Figure 4.13. Comparison of the memory power consumption as a function of the occupancy in terms of the fraction of channels containing a digitized hit, for a 128 × 515 bits segmentation. In blue a radiation tolerant SRAM. In red the same SRAM applying external memory gating. In green a latch implementation (data memory + tag memory).

memory implementations with realistic stimuli as described in Chapter 3. A simulation with back-annotated SDF (Standard Delay Format) extracted delays allows to generate activity files in VCD (Value Change Dump) format utilized for the power analysis.

In the activity range where the SSA low threshold is foreseen to operate, it is evident that for a SRAM implementation the ASIC would not benefit from any gating technique. The control logic overhead lead to higher consumption compared to the power saving on the memory. In the same range can be noted that a latch implementation is more convenient, allowing for a ~ 27 mW saving per module in the innermost end-cap disks. A SRAM implementation results instead beneficial for the HIP flag memory.

The situation is very different for the MPA due to the higher granularity of the pixel sensor that leads to lower activity but 16 times larger memory depth. The usage of the SRAM combined with the memory gating technique allows in the worst case (fast-fast corner) for a power reduction of ~ 179 mW compared to a non-gating implementation

and a ~ 76 mW compared to a latch implementation.

The main issue related to the usage of a latch memory if the linear dependency from the activity that can affect the ASICs during the calibration phase. During this operation, the detection threshold may be set close to 0, leading to significant noise coupling and therefore memory activity over 10%. The power distribution greed should support the peak currents and avoid local voltage drops. The DC-DC converters could allow for a maximum 20% increase in the module digital power requirement, making the latch implementation possible only in the SSA (the MPA requires 16 times memory depth).

4.4.2 High ionizing particles flags

As described in Section 4.2.1, the SSA implements a double threshold discrimination system to identify high ionizing particles signatures. The probability of having a charge deposition passing the 1.4 MIP threshold is estimated to be approximately two order of magnitude lower than a hit over the minimum threshold. No precise estimation of the HIP occupancy is available at the moment. Starting from this assumption, we can evaluate the most optimal approach to store the HIP flag data.

From the SSA bandwidth studies described in Section 3.7.1 we can evince that to limit cluster losses to $< 10^{-6}$ (1 ppm), the SSA should be capable of transmitting at least 24 strip cluster centroid coordinates per each event required by the Level-1 trigger. The same limitation applies to the HIP information. Section 3.7.1 explains as well the reasons behind the choice of an unsparsified transmission for the L1 raw data and an encoded transmission of the HIP flags. Up to 24 flags tag the clusters where, in at least one channel, the collected charge is above the 1.4 times the MIP one. The coordinate information is lost. The back-end reconstruction can anyway associate the flag to the centroid coordinate assuming a Gaussian charge sharing with mean value in the centroid.

Also for the L1 data path, the SSA performs a fast clustering of the detection threshold data. For each channel in the cluster verify if it arises from a HIP, encode and reorder the flag information to allowing to be correctly associated with the cluster in the MPA independently from the actual location. The clustering and the tagging are implemented with a parallel architecture to ensure low latency. The first stage search

for transitions in the strip hit array at the channel front-end output. Consequently, the processing logic verifies the value at the output of the eight following channels and use it to define the mask applied to the HIP array. 120 6-bit OR-trees evaluate in parallel the flag value. The logic is gated and enabled only in the correspondence of the recognized cluster. Even considering the area and power overhead in comparison with a sequential solution, this method results to be more power efficient. It allows, in fact, the encoding of the 24 flags in two BX cycles, avoiding the introduction of pipeline stages for unsparsified strip vector in the output formatter.

Implementing the encoding before the latency memory allows for a factor 5 data reduction and memory width. It would anyway require the clustering and the encoding to operate at the 40 MHz event rate. Considering the low occupancy of the HIP information that makes convenient the usage of an SRAM with memory gating, there is not a significant advantage in reducing the memory size. On the contrary, gating the clock to the module and enabling the clustering and the encoding exclusively when the SSA receives an L1 trigger (750 kHz average rate) allow for more significant power optimization.

4.5 Control and calibration

4.5.1 Synchronous command and slow-control

The DAQ system transmits to the SSA a 320 MHz event-synchronous control stream (T1). It encodes timing critical requests with validity related to the specific event cycle. A four-digits sequence encodes the phase of the particle-hit sampling clock. The encoding makes sure that this sequence is unique and does not appear elsewhere in the stream. The table in Figure 4.14 summarize the synchronous requests implemented in the SSA. The ASIC provides the possibility to invert the sampling edge and shift the phase of the commands to compensate for eventual distribution delays.

To configure the internal parameters, the SSA implements a set of registers accessible through I^2C protocol [216]. A SEU-tolerant custom I^2C slave handle the write and read operations via Wishbone protocol [211] on the internal registers distributed both in the ASIC periphery and the front-end channels. The configuration values are directly transmitted to the specific interface according the sub-address MSBs. The module

ReSync	Soft reset signals. Resets the state machine without affecting the static configuration. Already started transmissions are completed while new frames in the FIFOs are suppressed.
Orbit Reset	The command follows the LHC LHC orbit period. The event counters and bunch crossing counters are reset. SSA, MPA and CIC ASICs are synchronized between each other.
L1 Trigger	Requires the readout of the raw sensor image of the event occurred n-µs before, where n represents the trigger latency in BX cycles. It increments the event counters.
Calibration	Strobe signal that triggers the charge injection at the front-end input. The duration and the phase of the charge injection are controlled by configuration with a resolution of 3.125 ns.
Shutter control	Defines the start or the end of the acquisition window when the SSA operates in asynchronous readout mode.
Start Readout	Triggers the transmission in asynchronous readout mode.
Clean	Resets the value of the channels counters.

Figure 4.14. List of the event-synchronous control commands implemented in the SSA.

supports multi-master multi-slave operating mode, and configurable sub-addressing with auto-increment to accelerate the ASIC configuration. The with the GBT-SCA [11], [17] and the LpGBT [169] master interfaces was verified with back annotates digital simulation.

The sub-addressing (described in Figure 4.15) is optimized for the most frequent operation consisting in the update of a register in multiple channels, as when loading the trimming and calibration values. The whole control path and the Wishbone interconnect fabric are gated and activated only when it detects activity on the I^2C lines or when an internal operation requires it for internal transfers (as in the asynchronous readout mode). A watchdog avoids lock situation in case of erroneous activity on the control lines.

Examples of configurable registers implemented in the front-end channels are the channel mask, sampling mode, signal polarity, analog and digital calibration con-

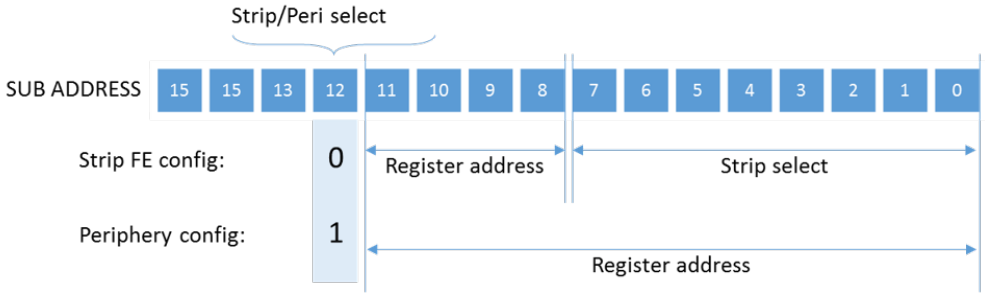


Figure 4.15. Slow-control interface sub-addressing scheme.

trol, the DC-output of the booster amplifier, the trimming of the pre-amplifier gain, the trimming of the comparators threshold, the HIP cut, test and calibration patterns. Examples of configuration registers implemented in the ASIC periphery are: the adjustments of multiple bias voltages to compensate for process and radiation variations, the test-points routing, the stub data and the HIP flags data-format, the control of the stub cluster width, parallax correction, readout mode, L1 trigger latency, sampling clock phase and the DLL charge pump control, and many others for a total of 1128 × 8-bit configuration registers.

4.5.2 Bias calibration

An analog bias block located in the SSA periphery generates the voltages and currents distributed to the front-end channels array. It allows compensating for process and temperature variations, as well to control the performance of the analog components like the channel pre-amplifier and the calibration voltages. Figure 4.16 shows the biasing circuit block diagram. The core of the bias block is the radiation tolerant bandgap reference circuit IP [217]. It generates the temperature compensated reference voltage. The buffered voltage is distributed to the six voltage-to-current converter circuits that provide a reference current for the six 5-bit current-DACs. These last are used for bias adjustment with respect to process and temperature variations. A set of local triplicated registers accessible via the Wishbone interconnect allows to control the digital to analog converters. In total, the calibration block provides 11 bias currents, 3 bias voltages, input reference for the booster amplifier, two threshold voltages and calibration circuits DC levels.

An analog multiplexer connects several internal nodes to a dedicated C4 bump pad

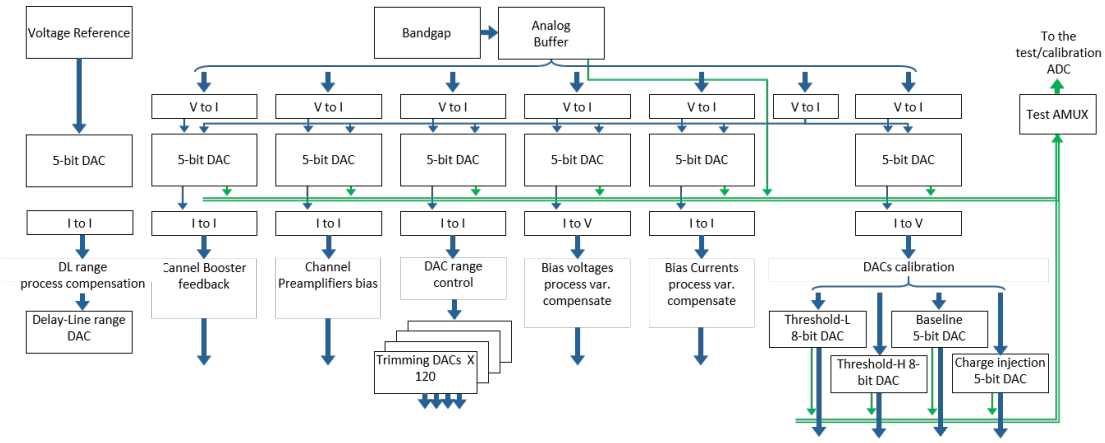


Figure 4.16. Block diagram of the SSA biasing and calibration block.

and to the corresponding wire-bond pad. The hybrid will route the test voltage to the ADC input of the LpGBT. For the production version of the SSA, the possibility of implementing an embedded trimmed ADC for auto-calibration is under evaluation. The current prototype relies on an external LpGBT measurement. Examples of accessible test points are: the calibration DACs outputs, the threshold voltages, the DC bias voltages for the pre-amplifiers, the baseline voltage for the booster amplifier in the channel front-end, the buffered bandgap reference voltage, and others.

4.6 ASIC implementation

4.6.1 Choice of the technology

A first element to take into consideration for the choice of the technology, is the possibility of accessing the mixed-signal design kits, support for software and design tools, legal support and radiation environment characterization via the CERN foundry service. The choice is therefore limited between a 250 nm (end of life support), 130 nm (from two different foundries), the 65 nm and a 28 nm technologies.

Since, in both SSA and MPA designs, the digital signal processing together with the memory elements represent a substantial part of the design and more than half of the power budget, it results convenient to move towards a down-scaled technology. From the simulations of thermal performance and mechanical deformation [174] the maximum allowed power density of the tracker is 100 mW/cm^2. Power density in this

context does not refers to the single junction, but the average energy dissipation of the dies where the cooling system is attached. From this point of view, selecting a more scaled technology would allow reducing the average switching current.

Clearly, the situation is different for the embedded analog circuits. The requirement of higher performance and area constraints has accelerated the scaling trends in most of the device parameters, such as the effective channel length, thickness of the gate dielectric, the supply voltage, the leakage currents, and others. At the same time the intrinsic precision of the components degrades. The signal dynamics also shrinks to avoid for intense electrical fields. At the same time, the threshold voltage reduces together with the transistor channel length, but not as fast as the supply voltages. As a consequence, in the analog domain, it is evident that the effect of the reduction of VDD/V_T ratio leads to operating point issues and dynamic range reduction. As devices become smaller and the total number of implant ions under the gate reduces, the threshold variations due to substrate effects play a stronger role in minimum area devices [218]. Considering devices of equal area for different technology nodes instead, we can see that the substrate doping density Nb is increasing under scaling. A consequence of increasing doping density means that the devices have smaller V_T variation, and therefore V_T matching for equal area devices is improving [219]. From a brief analysis, we can see that the power demand of a circuit given a specific dynamic range target, is approximately inversely proportional to the supply voltage in the hypothesis of a fixed gm/I_D (and therefore a fixed Vgs-V_T in strong inversion). However, with technology scaling, the f_T increase substantially. Porting an analog design to a shorter channel process, while keeping constant the bandwidth requirement, allows to bias the devices with a lower Vgs-V_T and higher gm/I_D keeping constant the f_T. In applications like the SSA front-end, which does not have high bandwidth requirements, working at high g_m/I_D or even going towards moderate or week inversion, greatly helps in reducing power consumption.

One more factor that should be taken into account is the performance of the technology to high radiation doses. The main TID related effects are caused by radiation-induced charge trapped both in the oxides present in the MOS structure and at the interface between these oxides and the silicon [132]. More detail can be found in the introductory section 2.4. The main consequence of charge trapped in the oxide is a negative threshold voltage shift. In nMOS devices due to positive charges that attract electrons from the bulk. In pMOS instead due to holes in the channel repelled by the

holes trapped in the oxide [135]. Since the gate thickness scales with the technology, it is evident that a more scaled technology presents a less prominent variation [140]. This requirement leads to exclude the use of any SOI technology. The SOI technologies present several advantages deriving from having active devices built on top of an insulating layer results in considerably less pn junction area and parasitic capacitance, making SOI devices more optimal for low-power applications compared to bulk technologies [220]. On the other hand, the insulating layer introduces an additional source for radiation-induced charge trapping. In particular positive charges trapped in the buried oxide that may lead in NMOS to an inversion of the back-channel interface of partially depleted devices leading to a conductive path between source and drain [221], [222]. This can lead to significant increases in leakage current. The charge trapping in fully depleted transistors will cause a decrease of the threshold voltage [223].

Besides, the possibility to share the prototyping cost among projects represents a critical factor to take into account. The MPA and the SSA need to be produced in the same technology to avoid duplication of the production costs. Due to the size of the MPA (25.0 mm × 11.9 mm) and of the SSA (11.0 mm × 11.0 mm), the ASICs cannot be prototyped with a common MPW. Scaled technologies as the 28 nm would ensure lower power consumption for this application, but it would sharply increase the prototyping cost and would require a new irradiation characterization campaign.

For these reasons a 65 nm technology has been chosen as the best compromise. This technology has already been fully characterized by radiation effects. Furthermore, the cost of prototyping can be shared with other projects in the HEP community.

4.6.2 Supply voltage scaling and temperature inversion effect

From the dynamic power analysis of the SSA ASIC implemented in a 65 nm technology, the digital functionalities, together with the memories and the IOs, consume roughly 58% of the power budget in the SSA (for an average input signal occupancy of 5 particle clusters per BX per module). A common technique for reducing power consumption in mostly-digital circuits, consists in reducing the supply voltage. For CMOS circuits, the cost of lower supply is lower performance. Scaling the voltage supply increases the delay of a gate, but, if the timing of a circuit is not marginal, the scaling will save

power without corrupting the design at a given frequency.

The main sources of power dissipation in CMOS circuit are static current, which results from resistive paths between power supply and ground, and dynamic power, which results from switching capacitive loads between different voltage levels. For a CMOS gate, the dynamic power is: $P = \alpha C V^2 f$ where α is the activity factor, C is the load capacitance, V is the supply voltage and f is the operating frequency. This equation shows as, if the supply is scaled by a factor x, the dynamic power consumption scales by x^2. Consequently, scaling the voltage to 0.8 V provides a gain in power consumption about 55%. On the other hand, the voltage scaling has a negative effect on the performance of the transistor, which must be studied to prove the feasibility of the design at a lower voltage supply.

To study the delay of a cell is necessary to study the behavior of its output current. For the purpose of this simple evaluation, the drain current can be represented as: $I_d = \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_t)^2$ where μ_n is the mobility, C_{ox} the oxide capacitance, W the transistor width, L the transistor length, V_{GS} the gate voltage and V_T the threshold voltage. The current is proportional to the mobility of the semiconductor. Lattice vibrations cause the mobility to decrease with increasing temperature. The cell delay increases with temperature due to the mobility [76]. The other parameter which

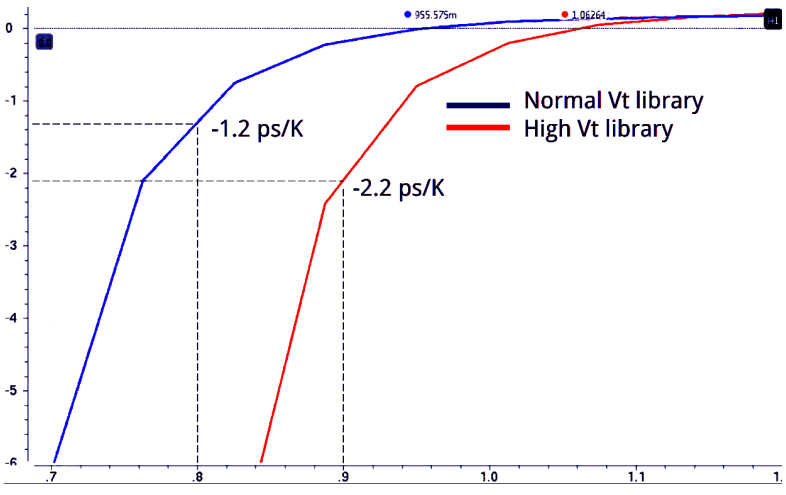


Figure 4.17. Temperature coefficient in ps/K for a digital library cell delay as a function of the V_{GS}. For the standard-V_T library, the temperature coefficient is negative for $V_{GS} < 940\,\text{mV}$. For the high-V_T library instead the temperature coefficient is negative already at $V_{GS} < 1.06\,\text{V}$.

changes with temperature is the threshold voltage: $V_t(T) = V_{t_0} + \alpha_{V_t}(T - T_0)$ where α_{V_t} is a constant variable which reduces the threshold voltage when the temperature increases ($\approx -3\,mV/^{\circ}C$) [76]. The final drain current depends on the dominating effect at a certain V_{GS}. In advanced technology node as the 65 nm one, the mobility effect is dominating only when the V_{GS} is large enough. In this case, the difference $(V_{GS} - V_t)$ is almost constant respect the temperature variation of V_t. Instead, if V_{GS} approaches V_t, the variation with temperature of the difference is larger. When the variation of the threshold dominates over the mobility, the cell delay decreases with high temperature and vice-versa. This condition is called temperature inversion effect [76].

Figure 4.17 shows the delay variation coefficient for different supply voltage in 65 nm, in the case of high-V_T and normal-V_T transistors. A negative coefficient indicates the temperature inversion effect. As expected, high-V_T transistor degrades more than normal-V_T. In the latter the inversion point is around 0.95 V. The coefficient amplitude is higher when the device is in temperature inversion respect the normal effect i.e the variation of the delay with temperature is larger in inversion than in the typical condition.

In the case of the SSA, where the cooling temperature is $-30^{\circ}C$, the temperature inversion effect plays a negative role. For this reason, the 0.8 V option was discarded as well as the use of high-V_T cells, at least in the low supply voltage domain. The choice for the supply voltage is orientated towards 1 V, where the normal-V_T transistor are not in temperature inversion. The power saving will be $\approx 30\%$ respect the nominal voltage of 1.2 V.

One of the main reason to exclude the 0.8 V supply is the performance degradation of the L1 memories when simulated in this condition. SEU resistance of DICE Flip-flop and Signal-to-Noise Margin (SNM) of memory cell are are not affected. On the contrary, the read and write operation timing at 40 MHz is marginal in typical condition (TT corner and $+25^{\circ}C$), while it does not fit the specification in the worst case condition (SS corner and $-30^{\circ}C$), where the memory is no more functional. Furthermore, due to the long transition, the design will be 4 times more sensitive to Singe Event Transient (SET). Also in the case of the memory, the optimal trade-off between power and performance is found with a supply voltage of 1 V.

4.6.3 Total Ionizing Dose tolerance

Radiation effects are one of the main challenges in the SSA design. The maximum Total Ionizing Dose (TID) foreseen in the CMS outer-tracker in 10 years of operation, is 57 Mrad. CMOS technologies are usually considered tolerant to differences in the radiation response of transistors exposed at the same TID but at different dose-rates [224]. Most of measurements in literature are performed at dose-rates magnitude higher than the one expected in the HL-LHC for obvious timing reasons. Recent studies on scaled technologies, anyway, reports dose-rate effects that could not be attributed to simple charge trapping and annealing processes [225]. In particular the work of Borghello and Faccio [226] describes how 65 nm MOS irradiated at low-dose-rate levels exhibit larger degradation of performance than devices exposed to high dose-rate irradiation, possibly related to charge trapped in the STI crossed by low electric fields [107]. For those reasons, a ×2 safety factor has been considered for the SSA design.

The degradation induced by high TID in 65 nm MOS transistors is strongly gate-length dependent. Studies on the radiation effects in 65 nm technology [227] prove that short channel-length (L) transistors suffers of a stronger degradation induced by high TID compared to devices with longer L. On the other hand, this relation is attenuated when the devices are irradiated at lower temperatures. From the studies reported in [107], we see that nMOS transistors have a variation in their performance almost independent of the temperature and, in any case, much lower than that shown by the pMOS, which are instead very sensitive to temperature increases. The SSA design is based on foundry standard cell libraries, so is not possible to freely tune the transistor dimensions. Based on the results of the DRAD [228], a 65 nm digital radiation test-chip, the 7-tracks foundry library shows an almost destructive degradation with radiation already at 100 Mrad compared to the 9-tracks and 12-tracks foundry libraries. Also in this

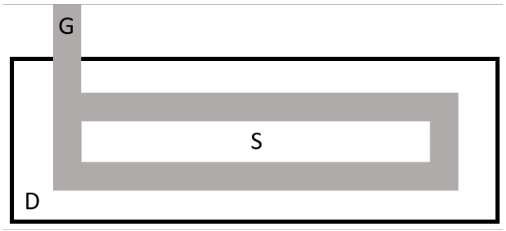


Figure 4.18. Example of Enclosed Layout Transistor (ELT).

case, the degradation is more prominent for devices irradiated at room temperature compared to devices irradiated at low temperature (−20°C). On on the other hand, the 12-tracks library adopts larger minimum width (700 nm compared to 210 nm for the pMOS and 390 nm compared to 190 nm for the nMOS) with consequent increase in power consumption.

Considering the low operating temperature of the tracker (−30°C), for the implementation of the digital functionalities of the SSA, the 9-tracks standard cell library has been selected, as compromise between expected radiation damage and power consumption. TID effects as drive loss and V_T shift are limited avoiding the use of minimal width transistor.

Due to the narrow-channels effects described in [229], small width buffers and delay elements have been excluded already in synthesis. Besides, delay cells featuring longer L, shows a different degradation compared to other cells of the same library. The simulations employing radiation device models described in Section 4.6.4 predict a frequency degradation around 40% at a TID 100 Mrad and a temperature of 0°C. In the memory element, the nMOS are larger than 200 nm and pMOS than 500 nm. The protection against latch-up is reached by placing p^+ guard bands between n^- regions.

In the analog domain, to prevent the radiation induced drain-to-source leakage current increase, the front-end channels utilizes Enclosed Layout geometries (ELT) for the amplifiers input stage (Figure 4.18). In ELT MOS the shallow trench isolation (STI) oxides do not face the channel [230], therefore, the charge trapped in the STI does not create leakage paths [231]. Besides, this technique is efficient to mitigate the $1/f$ noise increase on irradiated devices [232], due to side-effects associated to the shallow trench isolation region in nMOS operated at low drain current [205].

4.6.4 Timing corners for the low-temperature and high-radiation

According to Section 4.6.2, the SSA digital core operates at 1.0 V, selected as the optimal trade-off between power and performance. From the plot in Figure 4.17, the temperature delay coefficient [ps/K] for conventional V_T transistors is negative for a supply of 0.9 V, while it results positive for supplies above 1.0 V. It is not straight forward to define the worst case for setup analysis between the low temperature and the high temperature when operating in the SS-process at 1.0 V − 10%.

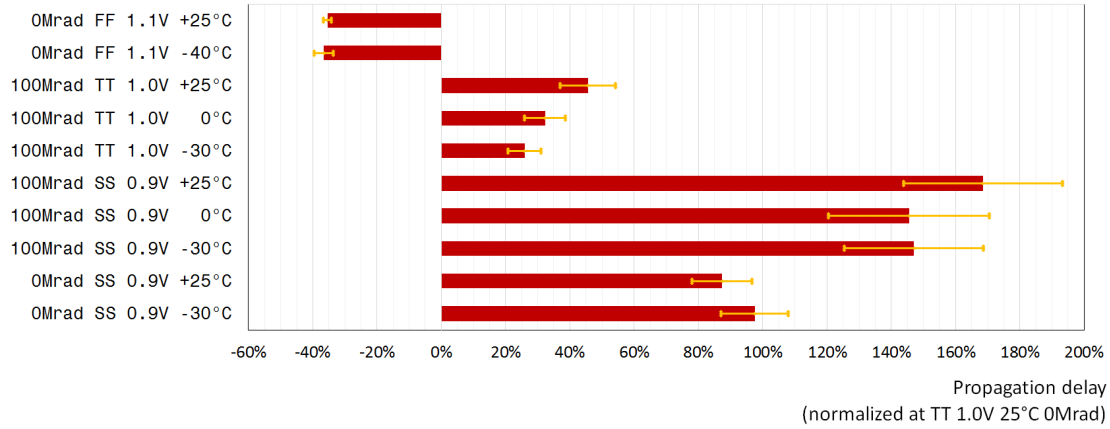


Figure 4.19. Average propagation delay difference for multiple timing corners with respect to the typical [TT, 1.0 V, +25°C, 0 Mrad] timing corner. The results are the average between the values evaluated for multiple input transitions between 6 ps and 0.69 ns and multiple load capacitance between 0.7 fF and 59 fF, for 792 digital library cells.

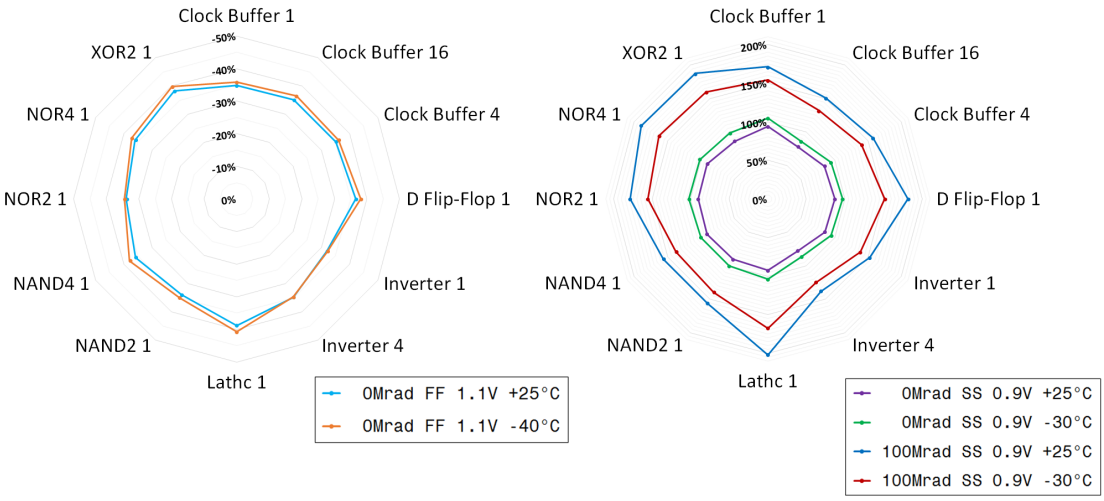


Figure 4.20. Propagation delay comparison between multiple timing corners and the typical [TT, 1.0 V, +25°C, 0 Mrad] timing corner for 12 representative standard cells from the digital library. The fastest is [FF, −30°C, 1.1 V, 0 Mrad]. The slowest before irradiation is [SS, −30°C, 0.9 V 0 Mrad]. The slowest after irradiation is [SS, +25°C, 0.9 V, 100 Mrad].

To reply to this question, a subset of the standard cells from the 9-tracks foundry library (including minimum and medium-size NAND, NOR, buffer, clock-buffer, flip-flop -and latch cells) was re-characterized at 0.9 V using a dedicated software tool. It resulted that the characterized cells operating at −40°C present a slower response compared to the same cells operating at +50°C but faster compared to the 125°C corner. Since the SSA will operate in the range between −30°C and 0°C, and wafer probing will be performed at room temperature, the worst case corner for the setup checks is the SS process, −40°C, 0.9 V.

Based on the irradiation results of 65 nm bulk CMOS devices described in [233], a collaboration between CERN and the technical university of Crete leaded to the development of new scalable BSIM6 [234] models which includes the threshold voltage shifts, sub-threshold slope degradation, mobility reduction, and degradation of leakage current due to radiations [235].

Before of adopting the radiation models for the final SSA implementation, they have been validated and the integrated in the CERN mixed signal design kit. Single devices simulation have been compared with the corresponding measurements for multiple devices sizes. The first prototype implementation of the SSA analog front-end have been re-simulated with the radiation models and the results compared with the measurements on the ASIC as a benchmark. In addition, simulated results have been compared with the measurements of the DRAD [228] chip. The simulation results are coherent with the expected behaviour, showing results in agreement with the measurements and, in general, a rather pessimistic response. This behaviour is expected since the models are based on measurements on devices biased with $|V_{GS}|=|V_{DS}|=|V_{DD}|$

Process	Voltage	Temperature	TID
FF	1.1 V	−40°C	0 Mrad
TT	1.0 V	+25°C	0 Mrad
SS	0.9 V	−40°C	0 Mrad
SS	0.9 V	+50°C	0 Mrad
TT	1.0 V	+25°C	100 Mrad
SS	0.9 V	0°C	100 Mrad

Figure 4.21. Summary of the PVT+Rad corners for the final-SSA digital-core sign-off timing analysis.

during irradiation, which is considered a worst case for TID degradation. Beside, annealing effects are not considered.

Using the radiation models, it has been possible to re-characterize the foundry digital cell libraries for different operating conditions. In particular, this operation was necessary to evaluate the degradation of the cells delay at 100 Mrad and generate a liberty (.lib) file that can be used in the SSA design (and other projects) for the timing analysis and the sign-off checks.

Figure 4.19 shows the percent propagation delay degradation at 100 Mrad in comparison to the typical timing corner (tt, 25°C, 1.0 V, 0 Mrad), for different irradiation temperatures. The reported results are the average between the values evaluated for multiple input transitions and load capacitance. It is evident that for all the cells, the irradiation at room temperature (+25°C) shows the worst degradation in terms of propagation delay, representing a worst case for the setup timing analysis.

Regarding the delay of the digital cells operating at −30°C, two different contrasting effects can be observed on the standard V_T library. At low radiation levels and at 0.9 V, considering the slow-process, the performance degradation due to the mobility (temperature inversion) effect is dominant. The library cells show an average delay ∼ 10% slower than at +50°C representing the worst-case corner for the setup analysis at 0 Mrad. The situation is inverted already at 1.0 V.

If considering as well the TID effects, the devices show a more significant degradation in terms of the threshold voltage and the g_m when irradiated at a higher temperature. Already at 100 Mrad, the TID induced effects become dominant. In particular, the delay at +25°C is in average ∼ 21% higher compared to the delay of the same cell irradiated at −30°C.

In conclusion, multiple corners need to be evaluated as the worst case for the setup and hold checks in the sign-off stage of the final SSA design, as summarized in Table 4.21. In this case, the [SS, 0.9 V, +25°C, 100 Mrad] corner has been excluded since too pessimistic considering the ×2 safety factor and the worst-bias condition represented by the models. The usage of this corner would, in fact, lead to an excessive power consumption to meet the timing closure.

4.6.5 Single Event effect hardening

Single Event Effects are caused by very localized event induced by a single particle. The particle interaction with the silicon lattice and the consequent SEE effects are described in Section 2.4.2. If the free electron-hole pairs generated by the interaction are in the proximity of a p-n junction the carriers will be collected leading to a current spike [236]. The probability of a particle causing one (or more) SEU is dependent mostly part on two parameters: how much energy the particle can transfer to the silicon and the minimum charge needed for a cell to flip the state. The energy transferred to the device per unit length as an ionizing particle travels through a silicon is called Linear Energy Transfer (LET), usually measured in $\mathrm{MeV} \cdot \mathrm{cm}^2/\mathrm{mg}$. The minimum LET to cause a detectable effect in a node is called LET threshold.

For a given LET, the cross section is the number of errors divided by the incoming particle fluence. In Section 2.4 the physical process that leads to SEUs is discussed. Experimental tests can be conducted to calculate the cross section of a device, which is a measure of the response of the device to the radiation. Section 5.6 describes the cross-section measurements and the computational method used to evaluate the expected error rates for the CMS-tracker particle spectrum.

To study which technique to implement and eventually which percentage of power consumption and the area we can trade to reach higher radiation tolerance, it is essential to evaluate the maximum error rates that can be accepted and eventually their consequences. Any upset in the control state machines may lead the ASIC to operate in an unknown state and eventually lead to a deadlock situation or system failure. If such a situation occurs, it may require to issue a reset signal to restore the correct operation, with consequent loss of the whole detector for an extended time window. Such a situation should be avoided. SEEs on the stub or L1 data paths instead can lead to erroneous information about a single strip or pixel, leading eventually to inefficiencies in the event reconstruction of a specific event. They will not affect anyway the tracker operation.

It is possible to make a first distinction between the SEE effects on combinatorial logic and the effects on memory elements in sequential circuits. In the latter one (SEUs) the logic state of the flip-flop or latch is corrupted. A refresh is required to correct the error. If the cell stores a state variable or data information, clearly, the effects on

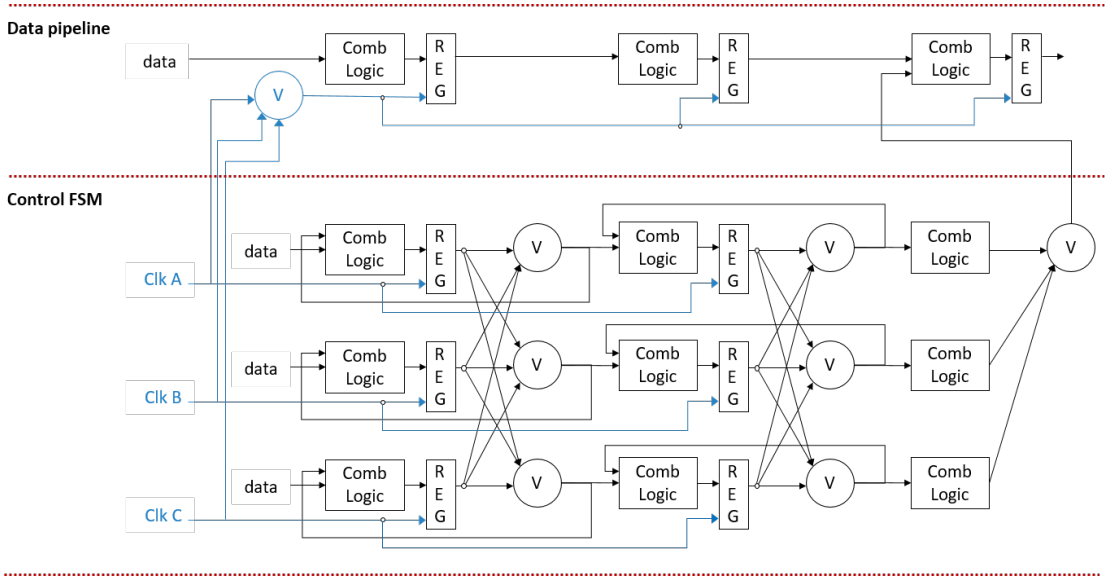


Figure 4.22. Example of the triple module redundancy implementation in the SSA. Control path and related clock distribution are fully triplicated. The data path is not triplicated.

the circuit is is different. The error probability is inversely proportional to the clock frequency since the rate is integrated into a more extended time window between consecutive refreshes.

For what concerns the combinatorial logic, the SSA design does not make use of dynamic cells where the information is stored in high-impedance nodes. Minimal charge injection is sufficient to affect the value that will propagate to the following cells. On the contrary, if a SEE occurs in a static combinatorial cell, it will exclusively lead to a glitch with a duration dependent on the charge injection and the driving strength of the cell. These phenomena are usually called Single Event Transient (SET). The glitch may propagate to the following cells and eventually arrive at a flip-flop. If the glitch duration is long enough and it overlaps with the sampling phase, it can lead to an error. The error probability for SETs is therefore directly proportional to the clock frequency.

SEU hardening technique are usually based on redundancy, either in space or in time. A common hardening technique is the Triple Module Redundancy (TMR). Each flip-flop or memory element is instantiated three times. A voting cell propagates the logic value present in two out of its three inputs. Due to the stringent power budget, it is not feasible to adequately protect the whole digital circuitry of the SSA. For this

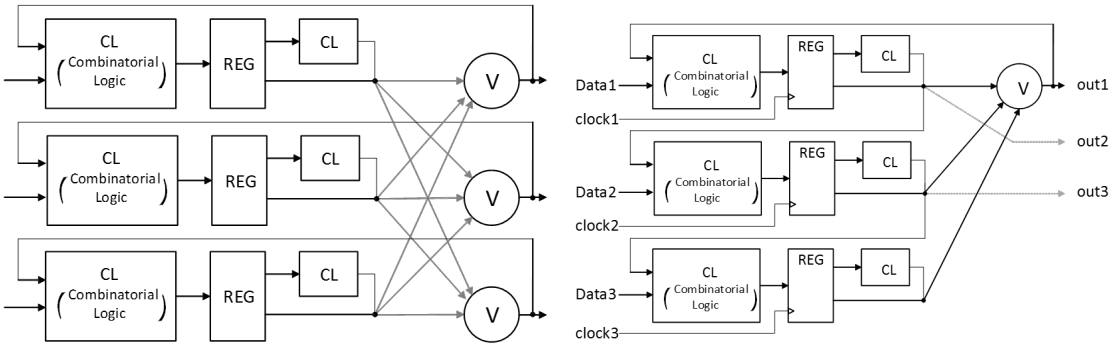


Figure 4.23. Comparison between the TMR standard approach utilizing three majority voter cells and a proposed approach which utilizes only a single voter and an asymmetric feedback loop capable of guaranteeing SEU tolerance in case of an upset on the voter cell.

reason, a TMR technique was applied exclusively to all the control state machines and the configuration registers at RTL level.

Figure 4.22 shows how this technique has been implemented in the more critical parts of the design. Three identical state machines are instantiated. If a fault caused by as SEU occurs in one, the error will be masked by the output voter. An upset on the state variables do not lead directly to a system fault as a result of the majority vote on the output signals. In the case that a second SEU occurs in the state machine, even farther away in time, the functionality of the system would be corrupted. All the state variables should be therefore periodically refreshed with their voted state, thus a feedback loop is required. The voter cell is triplicated as well to avoid that an eventual SET on the voter itself would propagate to all the three instances. Any error in the logic or in the state variable voter is overwritten by the feedback, while if an upset occurs in the output voter, it may lead to an error in the output data. For this reason, each state machine or pipeline stage implements triplicated input and output ports. The error at the second stage input is equivalent to an upset in only one of the instances and gets corrected at the next clock cycle. In the areas of the design where was possible to implement this approach, the triplication has been automatized at RTL level as a result of the use of a set of python scripts that implement a triplication tool called TMRG [237].

A modified technique was evaluated to mitigate the power consumption increment (Figure 4.23.b). Only a single voter is instantiated. The three state machines are interconnected with an asymmetric feedback loop to avoid a system failure in the

eventuality of a SET on the single voter. The voted value of the state variable is evaluated only by the first instance. The second ones receive in input the output of the first one and so on. If the voter is upset right around the sampling time, an error in the assessment of the current state occurs only in the first instance without affecting the other two. The first state machine may produce a wrong state at the following cycle that will propagate to the second instance while the first is refreshed. In a total of 3 clock cycles, the upset is cleaned. The first technique was selected since considered safer for the state machines operating at the low clock frequency of 40 MHz.

The described TMR techniques require an active clock to refresh the state variables. It is a too power hungry requirement for the static configuration registers. The SSA implements 1128 × 8-bit registers to store calibration, trimming and configuration according to the module location in the tracker. From a coarse estimation of the power requirement, it would require ~ 2.8 mW for the SSA and ~ 12.55 mW for the MPA, without considering the clock distribution buffering and routing. Clock gating is unavoidable. Three solutions have been taken into account.

Continuous refresh

A first approach may consist of gating the configuration without applying redundancy. The back-end control software can continuously refresh the configuration by writing one by one the values between triggers. Only registers under refresh receives the clock. This technique does not provide complete tolerance against SEU, but it guarantees that even if an upset occurs, its effect is limited in time. It implies a significant power overhead to keep always active the internal wishbone distribution and the input serial configuration interface. Besides, it introduces complexity at the system level. This technique is adopted in the RD53 pixel readout ASICs of the CMS inner-tracker [86]. In the case of the SSA and MPA where the area is not constrained while power consumption overhead may represent an issue, this technique is unsuitable.

Use of dual-interlocked (DICE) latches

An efficient way to implement a latch avoiding the propagation of errors is described by Figure 4.24. Such structure is usually called dual-interlocked (DICE) cell. The nodes A, B, C and D are fully equivalent while each NMOS gate is driven by the node on the

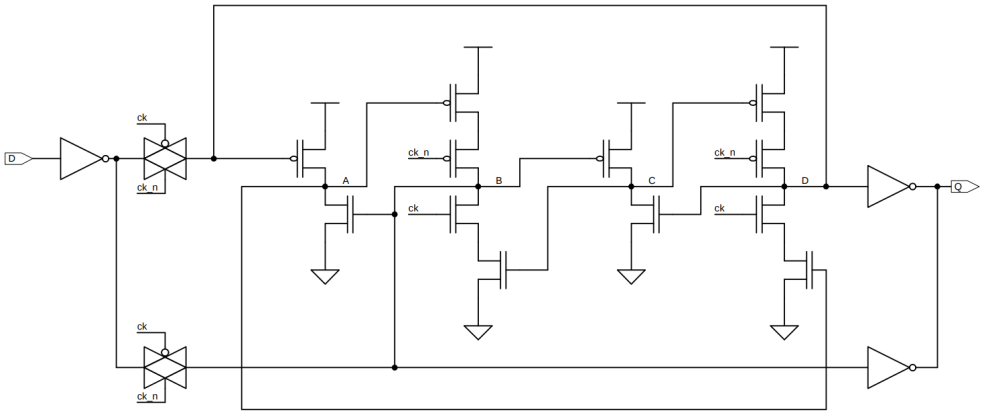


Figure 4.24. Example of a dual-interlocked (DICE) latch schematic [111].

left while every PMOS gate is driven by the node on its right. Each stage invert the propagated logic value. An SEU on one cell can propagate to maximum one stage and therefore effect maximum two stages [238]. If the charge collection affect two or more high impedance nodes, it can lead to an upset. The cell should be layout taking into considerations the space among equivalent nodes [239]. Clearly a dice cell requires a double of the area of a standard latch, burns almost twice more power and loads the clock lines with a double capacitance, but the area overhead is smaller in comparison with a full TMR. The use of a DICE cell represents a good solution for implementing configuration latches and has been used in the SRAM input stage.

Triple module redundancy with asynchronous self-refresh

An error detection logic evaluates eventual discrepancies among triplicated registers. If one of the three registers is upset, the error detection logic triggers an asynchronous pulse which locally re-enable the gated clock. In correspondence of the first clock edge, the register value is overwritten with the output of the voter cell. Three independent voters should be implemented to avoid upsets on the voter itself. Once the value is restored, the error detection logic output gets reset, and the clock is gated. It is convenient to latch the clock enable signal on the negative level of the clock to avoid glitches. The timing closure could be not straight forward and should be adequately constrained. For this reason, it may be convenient to synchronize the feedback. Figure 4.25 describes the technique. The gating could be implemented at the level of the single register, cluster of registers or chip level. The first introduces a significant

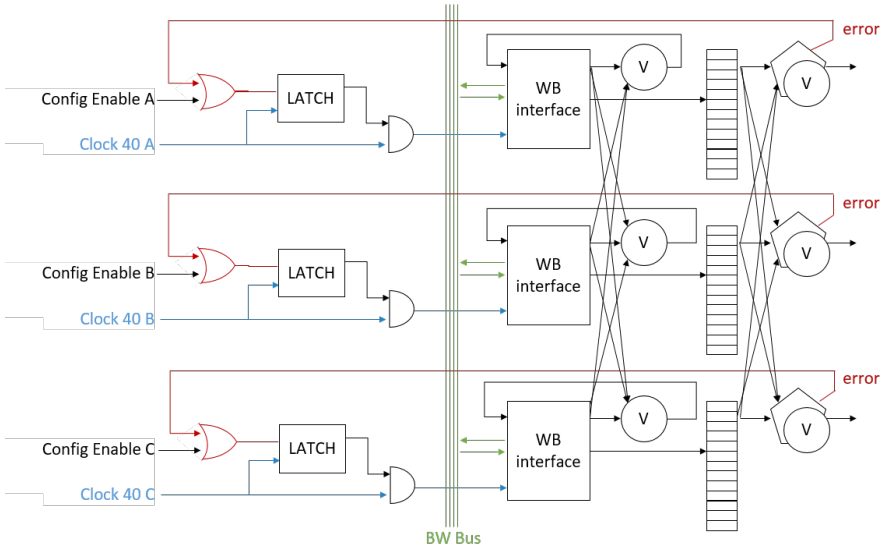


Figure 4.25. Triple module redundancy with self-refresh feedback. This approach was developed for the SSA and MPA configuration registers.

overhead with an impact on the power during the write operations. On another hand, the latter requires a deep OR-tree in the error detection logic to generate the enable pulse. The probability of having an upset within the register cluster increase with the number of registers. For every upset in any bit of the register cluster, the clock is enabled for all the registers. The usage of a triplicated set of configuration registers, gated with asynchronous refresh and split into clusters of 32 registers was selected as the best compromise for the power consumption.

Standard cell placement

TMR can protect from SEUs only if the distance among triplicated registers is sufficient to guarantee that the charge collected from a ionizing particle traversing the substrate could not upset more than one node at the same time. Specific constraints were developed for synthesis and standard cell placement in order to guarantee a minimum distance. Based on the the measurements of the RD53SEU [240] 65 nm test-chip, a 15 µm distance is considered to be large enough to reduce the probability of multiple register upset to few percents when a ionizing particle crosses the die.

A possible approach could consist in spatially separate the three instances of the state machine by constraining the placement. This solution may drastically complicate the routing and the timing closure. The solution implemented in the SSA instead consists

in dividing the triplicated registers in instance groups and constrain the relative placement exclusively within the instance group, utilizing a custom TCL script. It was possible to guarantee a distance among equivalent registers without over-constrain the standard cell placement. A script was also prepared to verify the correctness of the placement after the consecutive optimization steps.

L1 data path protection and encoding techniques

As previously discussed, eventual errors on the data path could be acceptable. This is valid for the data pipeline, where the information is stored in the internal registers only for the pipeline latency of 6 clock cycles. The L1 path stores the information in the embedded memory for the duration of the the Level-1 trigger latency. The error probability is integrated on a 12.8µs time window.

The first SSA silicon prototype, which cross-section measurements are described in Section 5.6, does not include further SEU hardening on the L1 path. The possibility of introducing encoding techniques for the final chip is under evaluation. At the time of this work, few detailed SEU cross section studies on ASICs developed in 65nm technology as [241] are available in literature. The SSA and MPA include features to evaluate the cross-sections and the performance of the proposed radiation hardening techniques. A heavy-ion irradiation campaign (Section 5.6) allowed to evaluate the prototype capability to auto-correct single event induced errors and the expected error rates for the tracker particle spectrum. It resulted that for an L1 latency of 2.5µs and 12.8µs, the extrapolated error rate respectively $9.3 \cdot 10^{-4}$ $s^{-1}Chip^{-1}$ and $1.59 \cdot 10^{-3}$ $s^{-1}Chip^{-1}$. Those values are comparable with the error rate introduced by the front-end noise. In any cases could be beneficial to introduce additional SEU protection on the data stored in the memory.

A possible approach may consist in implementing an encoding capable to provide forward error correction on the stored data. The theoretical limit to the number of errors the a code can correct is given by the hamming bound. The most efficient codes are those which respect the equality and are called perfect codes. The Hamming encoding [242] is a perfect code capable to provide single error-correction capability. The Hamming codes are limited to a ratio between the number of code bits n and the number of data bits k that respects $2^{n-k} = n+1$. Calling $d_1 - d_k$ the data to be encoded and $y_1 - y_n$ the encoded word, an RTL implementation may consist in copy the input

word over the codeword skipping the positions with index equal to a power of two:

$$\forall i \in \mathbb{N}, i < \log_2 n + 1 : \forall q \in \mathbb{N}, 1 \leq q < 2^i \quad : \quad y_{(2^i+q)} = d_{(2^i+q-i-1)}$$

or in other words, the bits of the code-words y_1, y_2, y_4,.., $y_{(n+1)/2}$ represents the parity bits that can be obtained by the XOR operation of some of the other bits of the code-word. The parity bits are defined by the set of equations [243]:

$$\forall i \in \mathbb{N}, i < \log_2 n + 1 : \qquad \sum_{p=0}^{2^i-1} \left(\sum_{q=0}^{2^i-1} c_{[s^i(2p+1)+q]} \right) = 0.$$

Each parity bit alternatively checks a number of bits equal to its index and then skips another number of bits equal to its index. For the SSA strip data where the array to be encode is composed by 120 bits, the optimal approach is to use a hamming encoding with 7 parity bits. No padding is necessary since $2^{n-k} = 1 + n$ is verified by $n = 127$, $k = 120$.

SEU simulation

The system level verification environment described in Section 3.6 allows to deposit values on random registers emulating SEU effects, or imposing a logic state for a defined period emulating SETs. With the support of this tool and utilizing the post-layout back annotated net-list, was possible to verify the SEU tolerance of the control path. The simulation was performed in the hypothesis that a single particle does not produce a multi-bit upset, since the simulation framework has no knowledge of the standard-cell placement.

4.6.6 The flip-chip floorplan and the power distribution

To match the requirements of the tracking performance, the PS module layers will combine a sensor composed by 100 µm × 1.5 mm macro-pixels with a sensor composed of long strips of 2.5 cm and a pitch of 100 µm [9]. The bump density of the Controlled Collapse Chip Connection (C4) technology used to directly flip-chip the MPA ASIC over the pixelated sensor limits the pitch to 100 µm. The SSA ASIC is required to utilize the same C4 process of the MPA, inheriting its constraints.

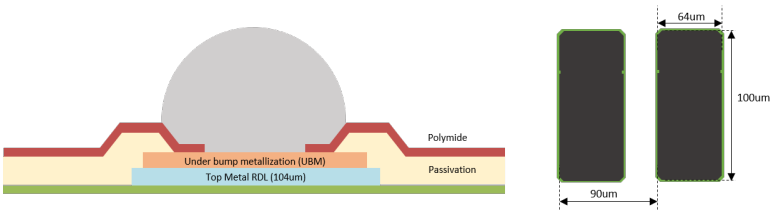


Figure 4.26. Implementation of the C4 Bump (left) and the wire-bond metallizations for the SSA ASIC.

The stringent material budget allowed in the tracker volume does not permit the use of packaging. The SSA bare-die will be directly bumped on the front-end hybrid flex PCBs. The short strip sensor presents a pitch of 100 µm and is directly wire-bonded to the front-end hybrids, avoiding the usage of pitch adapters or packaging that would drastically increase the quantity of material. The front-end channel placement within the SSA should follow the sensor strip disposition, with a minimal fan-in to guarantee a sufficient spacing among ASICs without over-constraining the front-end hybrids routing.

The final die dimensions including the seal-ring are 11.0 mm × 3.5 mm with a channel pitch of 90 µm and a bump pitch of 270 µm. The ASIC area is defined by the detector construction, leading to a low placement density. A passivation opening of 70 µm has been chosen to match the requirements of the bare-die assembly on the front-end module flex.

An additional row of wire-bond pads with a 90 µm pitch is added on the long side of the ASIC for testability and wafer probing purposes. Every ASICs is required in fact to be tested before the assembly process. The dicing will potentially eliminate the wire-bond row. Figure 4.26 shows the implementation of the bump cell and the wire-bond materialization. For the first prototype, the wire-bond pads are kept to facilitate the characterization of the ASIC and allow for irradiation tests. The charge deposition of heavy-ion beam utilized for single event upset tolerance characterization can penetrate only a few µm. The sensitive volume should be facing the beam directly. For the design implementation, a hierarchical Digital-On-Top methodology was employed. Figure 4.28 shows the final layout of the ASIC. The channel blocks include the full-custom analog front-end and the strip digital front-end circuitry which is independently placed and routed. The biasing block that provides the bias currents and the reference voltages to the strip channels is located in the periphery of the ASIC.

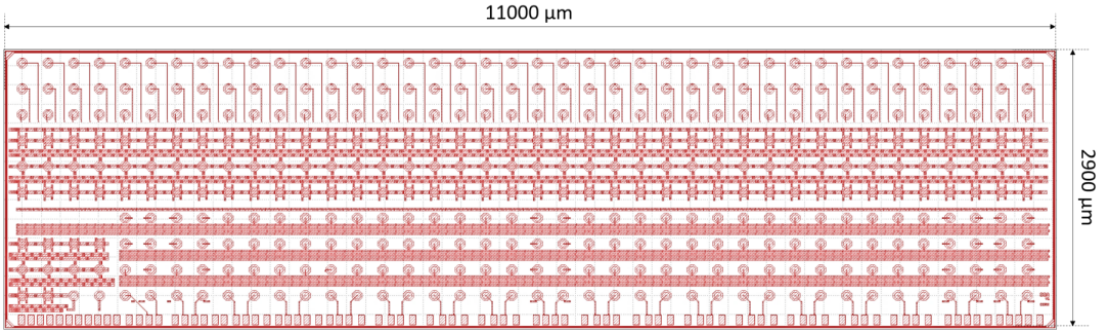


Figure 4.27. View of the final SSA ASIC top-metal layer (RDL), showing the bump connectivity and the ASIC dimensions.

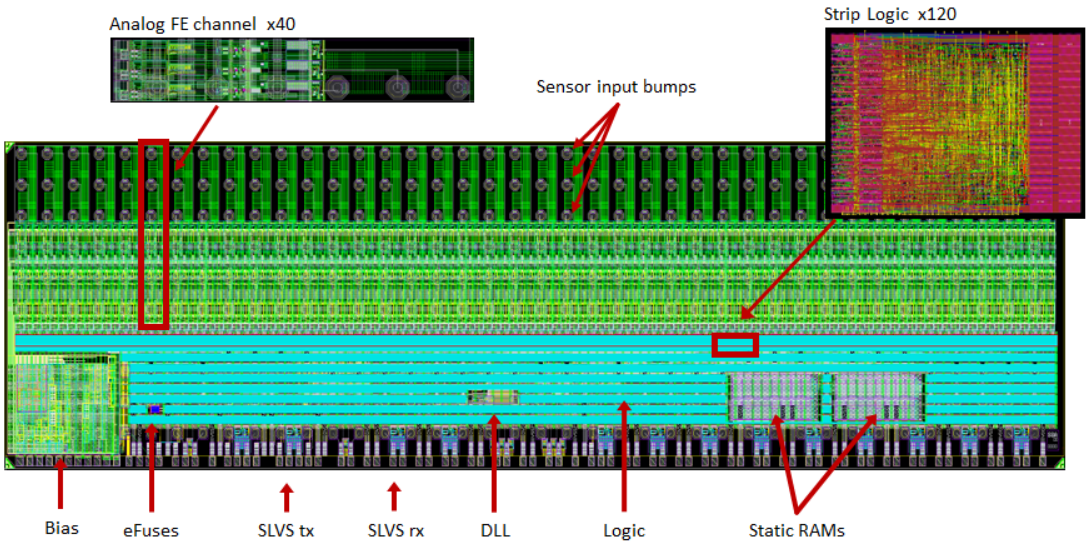


Figure 4.28. Final layout of the SSA ASIC and highlight of the hierarchical blocks.

The remaining area is occupied by the digital processing, the control interface and the data memories. Within the periphery are instantiated accessories IPs as the clock deskewing DLL and a set of e-fuses to store the unique chip identification number and the default configuration values.

The power distribution is implemented using the high thick and ultra-thick metal layers, reinforced with horizontal stripes in aluminum re-distribution layer. Since the power and ground bumps connect directly to the power distribution in order to reduce the voltage drop, rad-hard ESD protections [244] are connected to the horizontal rails in correspondence of the C4 bumps. The power rail connects directly to the C4 bumps

and as a result of the use of the re-distribution layer to the wire-bonds metallizations. The ESD protection for the digital core and analog supplies and grounds are placed in the proximity of the corresponding bump, to minimize the resistive path.

The ESD protection for the IO signals is instead placed inside the transmitters and receivers pads. The utilized ESD circuit provides protection for ±2 kV Human Body Model (HBM). To limit the radiation dose degradation, no thick-oxide is used in the pads. This choice introduces the limit of the IOs supply voltage to 1.2 V and to the CMOS output signals levels. For the same reason, it is not possible to use LVDS [245] or CML differential standards for the high-speed link operating at 320 MHz. Custom rad-hard scalable Low-Voltage Differential Signaling (sLVS) [246] transmitters and receivers [247] have been developed for this purpose. The SLVS pads, together with the custom CMOS radiation tolerant bi-directional IO pads [248] are placed in a single row in the ASIC periphery. The connection from the periphery-IO pads and the C4 bumps is implemented in re-distribution layer.

In the proximity of the IOs-row are placed the logic blocks operating in the 320 MHz clock domain as the serializers and deserializer and the command decoder. To minimize the skew between the output signals, in particular among the stub-data lines whose SLVS transmitters are distributed along the 11 mm of the ASIC bottom, a re-sampling element is placed in the proximity of the transmitters. The clock distribution for those flip-flops is routed to implement a fully balanced, triplicated and voted clock tree (Section 4.6.5 explains the clock tree triplication for radiation hardening reasons). The MPA ASIC which receive the signals cannot embed a phase aligner due to the strict power budget requirements. For this reason, it is mandatory to control the skew among the signals at the SSA output and between data and clock lines, for all operating corners and all operating temperatures.

The ASIC implement three independent power and ground domains for the IO pads, the digital core, and the analog front-ends and biasing circuits to minimize the noise injection into the channel analog front-end. The substrate isolation among ground domains is implemented with a double guard-ring with deep n-well and a 50 µm high resistivity trench isolation. The guard ring encloses the digital domain and, independently, each of the analog blocks.

4.6.7 Clock distribution and implementation flow

One of the main complications to achieve the timing closure in the SSA design was introduced by the variation of the propagation delay between corners. Due to the low operating voltage (1.0 V – 10%), the temperature inversion effect has a substantial impact on the cells propagation delay at −40°C. On top needs to be considered the degradation of the devices when exposed to radiations, the spread between the fastest and the slowest corner results in more than 120%.

The triplication of the clock distribution introduced an additional complication to the timing closure. For each state machine or pipeline stage in the control path, the output of the three redundant flip-flops is voted. The result of the voting operation is feedback to evaluate the next stage or transmitted to the next stage. The lunch path delay at a particular stage depends at the same time from the insertion delay related to three different, independent, clock trees. To minimize the skew among the three clock distributions has been necessary to heavily constrain the Clock Tree Synthesis (CTS) and make use of skew-groups. The usage of the CCOpt instead of the traditional CTS engine allows to directly manipulate launch/capture path delays and min/max logic path delays during CTS, allowing to achieve lower skews. A clock uncertainty and a transition time of 200 ps provides a sufficient margin in the clock modeling. Non-default rules has been used to shield the clock trunk and to increase the spacing on the branches, allowing to reduce cross-talk and gain in the incremental delay.

Due to the large size of the design (11 mm on the broader direction), it was essential to utilize QRC extracted information already at the optimization stage and not only in sign-off timing analysis. Multi-mode multi-corner (MMMC) based static timing

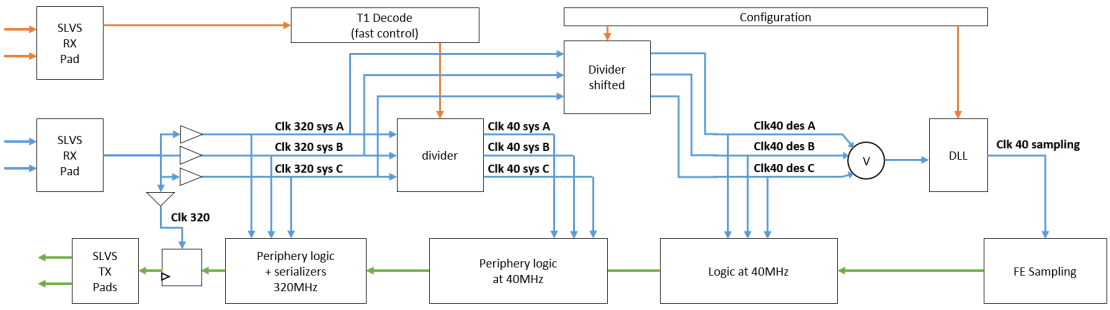


Figure 4.29. Block diagram of the SSA clock distribution. A total of 11 clock domains are implemented in the design due to the TMR methodology.

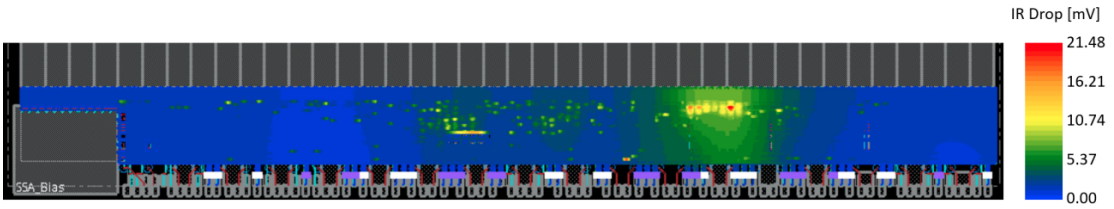


Figure 4.30. Dynamic IR-drop analysis results.

analyses and DRV checks allowed to verify the timing and design rules on the design. Since interconnect variations may affect the timing and cross-talk non-linearly, in sign-off analysis, the RC_{best} and RC_{worst} interconnect corners are considered in addition to the C_{best} and C_{worst}. Enabling on-chip variations and utilizing derate factors allowed to verify the timing closure by mixing the fastest launch path and slowest capture path for setup check, and slowest launch path and fastest capture path for hold check.

Formal Equivalence Checkings have been performed at different stages of the design and with the final netlist. Gate-level simulations with SDF back-annotated delays on the post-layout netlist are fundamental for the SSA ASIC. Static timing analysis and formal equivalence checking alone may not cover all design aspects. Gate-level simulations allowed to achieve trustability in the defined constraints and mostly to verify the capability of SSA and MPA ASICs to operate together as one system in all corners combinations (max-max, min-min, max-min, min-max).

Sign-off DRC and LVS checks have been performed with Calibre [249] utilizing a modified version of the rules in order to correctly extract Enclose Layout (ELT) devices and to include a more strict latch-up checks due to the radiation environment.

The first prototype of the SSA ASIC integrating all required functionalities for system level operation was submitted for prototyping in a common full-mask-set 65 nm engineering run along with the MPA and the RD53A [250] projects due to the size of the ASICs. A split-process was required due to the different metal stack adopted in the designs. The additional options selected are std-V_T, low-V_T, high-V_T devices, triple-well isolation, no polyimide, MOM capacitors.

Starting from the SSA scripted implementation flow has been derived the latest version of the CERN supported implementation flow available via the CERN ASIC support service [16], [251] for the institutes part of the collaboration.

5 Experimental result on the silicon prototype

The SSA ASIC, incorporating all the required functionality and the performance characteristics for the operation in the final readout system, has been prototyped. The ASIC performance has been characterized under the different working temperatures and the operating conditions, utilizing a custom made test bench. FPGA-firmware and software routines have been developed for these purposes.

The SSA front-end characterization with internal capacitance pulse injection matched simulations closely, with a strip threshold spread of 55 e^- r.m.s. after equalization, an equivalent electron noise < 330 e^- r.m.s. meeting the specification of noise performance. and a peaking time of 19 ns. Measurements show a front-end gain between 35 and 54 mV/fC and a peaking time of ≈ 19 ns for an injected charge between 0.5 fC and 8 fC allowing to detect the consecutive particle events in the combination with the zero dead-cycle binary readout. The measured power consumption is 55 mW and thus within the strict power budget of the PS modules.

Radiation tolerant design techniques were employed to mitigate Single Event Effects as well as Total Ionizing Dose effects for operation in the radiation environment of the HL-LHC CMS tracker. The ASIC radiation tolerance has been proved by irradiating the prototypes with X-Ray up to a total dose of 200 Mrad. The shift of the parameters are within the expected ranges and can be therefore compensated by the internal calibration circuit.

A heavy ion-based Single Event Upset experiment proved the prototype capability to auto-correct single event induced errors in control logic up to a effective LET

of $\sim 70\,\mathrm{MeV}\cdot\mathrm{mg}^{-1}\mathrm{cm}^{-2}$. Finally, a data error rate evaluation provides a SEU-related data-error probability lower than $5\cdot 10^{-11}$ for the ASIC operating in the CMS tracker environment.

Publications related to this chapter: [1], [3],

5.1 A custom setup for prototype characterization

A custom setup was developed to test and characterize the silicon prototypes in terms of functionality and performance. It allowed to perform radiation studies and evaluate the expected long term behavior and error rates for the PS module in the CMS outer-tracker. Before to describe the results of the characterization and the related studies, it is necessary to introduce the test setup developed for this purpose.

The setup is based on an FC7 µTCA FPGA card [252] mounting a Xilinx Kintex-7 [253] FPGA. Using an FC7 board allows to easily reuse most of the firmware blocks developed for the SSA and MPA test for the future CMS data acquisition system. A custom made interface board connects to the FC7 board via a high pin-count FMC [254] connector and allows for voltage level translation, supply control, and monitoring purposes. More details on the interface board design can be found in [255].

A dedicated firmware provides supply control and current monitoring by configuring the ADCs and DACs on the interface board. Different types of mezzanine can be plugged into the interface board PCI-Express [256] connector, allowing to adapt the test setup for several test cases with or without the sensor.

A single-SSA mezzanine was designed for the full characterization of the stand-alone SSA. While in the final application the ASIC will be flip-chipped on the hybrids, on this test board it is wire-bonded to facilitate its characterization under radiation sources

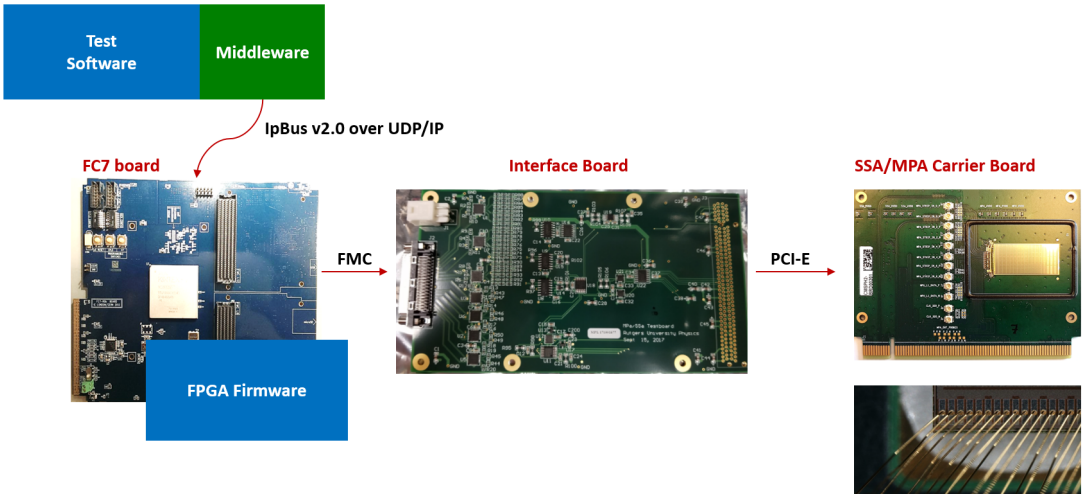


Figure 5.1. Hardware components of the SSA test system.

or ion beams. Since no sensor is present in this case, the input stimuli are generated by the FPGA.

An additional board mounting both the MPA and SSA ASICs was developed with the primary goal of verifying the communication protocols, the timing of the high-speed SLVS signaling, the phase tuning and the capability of MPA and SSA to operate together as one system. The differential clock and data lines between the two chips are equalized in length and drown to match the 90 Ω SSA IO impedance. The two ASICs are located within a distance of 3 cm, to reproduce operating conditions similar to the PS module hybrid.

Currently, an additional mezzanine card is under development by the CMS collaboration to characterize the SSA behavior together with the silicon strip sensor. In this case, the SSA is bumped on a custom glass interposer, and the silicon strip-sensor is

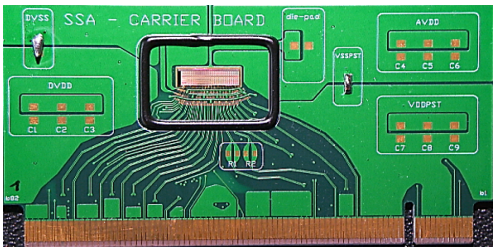


Figure 5.2. Custom carrier board designed for SSA characterization.

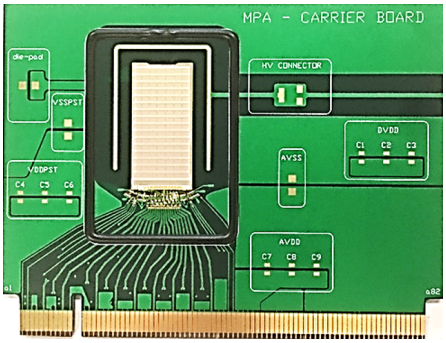


Figure 5.3. Custom carrier board designed for MPA characterization.

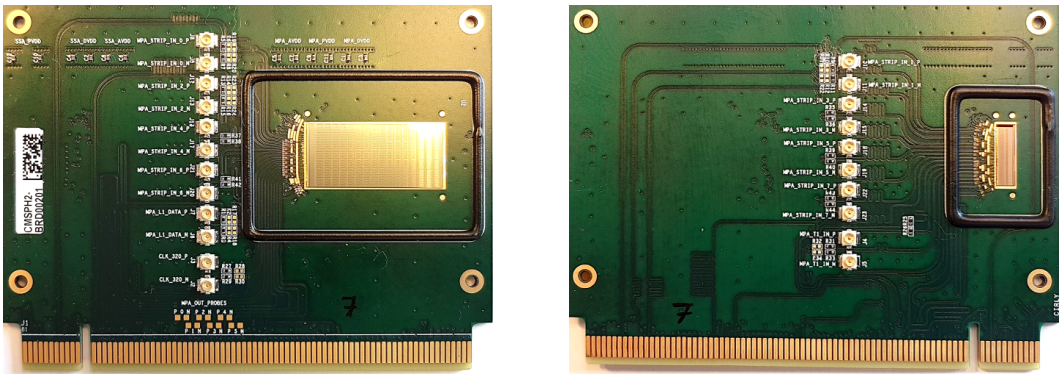


Figure 5.4. Custom carrier board designed for SSA to MPA communication studies and to verify the capability of the two ASICs to operate together.

wire-bonded to it. This design will allow to characterize the noise performance of the SSA with the input capacitance of the sensor and to perform test beams.

The FPGA firmware used in this test is developed as part of the D19C project [257]. The D19C firmware is aimed to form the foundation for test setups for all components of the CMS tracker Phase 2 upgrade: chips, hybrid, modules, and multi-modules testing, providing the basic communication and signal distribution blocks. Even if the D19C project is dedicated for testing purposes, the different composing blocks including the modules dedicated to the SSA readout, might be reused in the future in the DTC (Data Trigger and Control) system for the final CMS experiment.

The firmware generates and encode the packets transmitted to the ASIC and buffers its output data streams. When the system is used for the MPA characterization, it emulates the SSA ASIC frames and pixel sensor signals, while when the system is used for the SSA characterization, it emulates the strip sensor inputs. A dedicated block creates the fast commands at 320 MHz with a configurable phase relationship and forward them to the Physical Interface Abstraction Layer. PLLs embedded in the FPGA allows to control the phase of the clock and T1 commands transmitted to the DUT. A control block allows to access the configuration of all components on the PCB (voltage regulators, monitor ADCs, etc.) and the ASIC control registers via serial interface.

The firmware-software communication is based on the CMS IPbus protocol [258] over UDP/IP. The protocol lies in the application layer of the networking model and is network-agnostic. For data analysis, the firmware is limited to buffer the received data into its FIFOs and to performs only minimal consistency checks. All the data is transferred to the software routines for detailed analysis. The test rate is limited by the IPbus communication. To check the limits of the SSA capability and to maximize the coverage during radiation campaigns, it is necessary to use high-rate tests. In this case the SSA output vectors can be checked for each clock cycle against pre-loaded test vectors directly in the FPGA.

Custom middle-ware routines have been developed to provide access to the firmware control registers and data buffers via IPbus and to provide APIs for the test software running on top. It includes functions to access the serial interface used for configuring the components on the interface board, functions to control the fast-commands and control encoders, functions to read-out the data buffer and functions to control all

other firmware state machines. It allows moreover to configure the dedicated firmware module that controls the event rates, the phase relationship among commands, the repetitions and the delays of the trigger signals. On the physical abstraction layer several configuration are available for the transmitted and received data formats, sampling phases and time relations between the data and the control commands.

On the top of the middle-ware are implemented specific classes for the FC7 firmware control, for the SSA register mapped configuration, the control of the SSA internal bias generation block, the inputs generation and the output decoding. A dedicated block handles the calibration charge injection at the SSA analog front-end inputs and the digital test vectors injection. The decoding block allows to interpret the SSA outputs accordingly to the configuration settings and the registers values. It returns arrays of clusters/stubs, the raw sensor image vectors, the asynchronous event counting values. In addition it implements the methods for accessing external accessory instruments such as the X-Ray machine or the wafer probing station.

In the application layer, multiple software routines have been developed to study the MPA and SSA behavior, to test their functionality and to perform analysis on the collected data. The analysis routines allow to study and characterize the ASIC responses and to verify the digital operations. For the front-end characterization, it includes functions to study the front-end behaviour in terms of noise and mismatch, to study the DACs linearity, to extrapolate the analog front-end response and several other measurements. For what concerns the digital aspects, it allows to perform different types of tests on the memories, on the clock deskewing DLLs, on the clustering and on the encoding state machines. A reference behavioural model generates clusters, stubs and sensor raw-data accordingly to the configuration and it allows to compare the output vectors with the expected values. Dynamic power measurements allow to study the power consumption for different operating situations. In addition there have been implemented routines for the SSA calibration and trimming, and for analyzing the ASIC performances when exposed to X-ray or heavy ions.

5.2 Front-end characterization

The initial characterization of the SSA front-end channel was performed by taking advantage of the embedded calibration circuit. The ASIC implements a self-injection cir-

cuitry: each channel input is connected with 52 fF calibration capacitor to a common chopper circuit through a switch controlled by the channel configuration registers, allowing to inject a known charge into the front-end channel input. The amplitude of the voltage step is controlled by an 8-bit DAC supplying the current to a 4.6 KΩ resistor. The quantity of charge injected is determined simply by the relationship $Q_i = C_{CAL}V$, where V is the voltage determined by the calibration DAC in the periphery.

In this approach, the calibration DAC is an essential component for the front-end characterization. Its output voltage can be routed to a wire-bond connection or to an internal ADC allowing the measurement of the calibration DAC linearity, gain and offset errors. By acting on the internal bias block is possible to compensate for the errors introduced by the DAC. Calibration DAC measurements show a maximum Integral Non-Linearity (INL) of 0.5 LSB A strobe signal, generated by the fast-command decoder allows triggering the charge injection. A 6-bits delay line (DL) allows to select the injection timing. To enable the calibration and characterization of the prototype, the ASIC implements a 15-bits asynchronous ripple counter per channel connected to the low-threshold discriminator output as described in Section 4.2.4.

5.2.1 Shaper pulse reconstruction

The binary readout allows for timing characterization of the analog front-end. During this measurement, the front-end is set in edge-sensitive sampling mode and the internal injection of calibration pulses is enabled. To exclude any cross-talk effect between channels, only one channel at the time is active. The actual charge injection time can be controlled with a resolution of 1 ns as a result of the on-chip delay line (DL_{CAL}) that acts on the calibration pulses triggering the capacitor discharge. Clearly the DL_{CAL} needs to be previously calibrated by acting on the process-compensation DAC. The latter defines the bias of the block and acts on the current-starving delay cells to achieve the required resolution.

For a specific value of the channel discriminator threshold, shifting the pulse injection time between 0.0 ns and 30.0 ns it is possible to evaluate the delay that needs to be applied to the calibration pulse to sample the front-end output signal at the successive 40 MHz sampling-clock edge. Repeating the same operation for different values of the threshold-DAC, it was possible to reconstruct the shape of the analog front-end

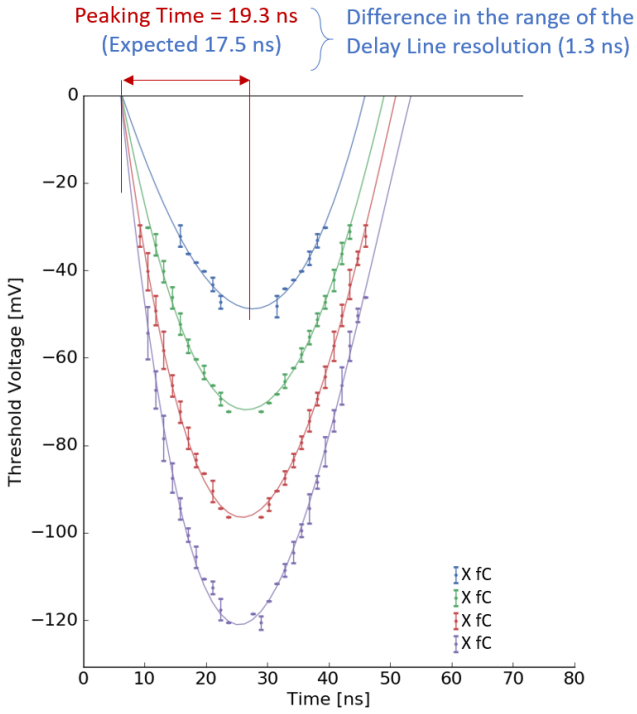


Figure 5.5. Indirect shaper output signal reconstruction for different input charges with a time resolution of 1 ns and a voltage resolution of 0.2 mV.

output signal for different values of the injected charge. In Figure 5.5 shows the shaper pulse reconstruction where 10^4 samples have been collected for each point to mitigate measurement noise.

The measured average peaking time is around 19.3 ns ±1.6 ns, as expected from the simulation. It is important to notice that the peaking time is independent of the input charge for the operating range.

5.2.2 Front-end noise studies

Figure 5.6 shows the number of events counted by the channel asynchronous counters for an injected charge of 1 fC and different values of the threshold-DAC. For each threshold value V_{TH}, 10^3 calibration pulses have been injected. The normalized curve represents therefore the probability of sampling one hit as a function of the threshold voltage. In the ideal case, when no noise is involved, it will assume a step function shape. Assuming the contributions of the noise v_{noise} to be a normally distributed variable and considering $V_{CompIn} = V_{peak} + v_{noise}$, the s-curve represents

the probability of V_{CompIn} to follow in the range $[V_{TH}, \infty)$. It can be therefore fit with a complementary error function:

$$\text{Hit Count}_{CH}(V_{TH}) = \frac{2}{\sqrt{\pi}} \int_{V_{TH}}^{\infty} e^{t^2} dt.$$

The standard deviation of the complementary error function fitting the S-Curves close to the threshold value allows evaluating the front-end noise. For a non-irradiated SSA operating at 25°C, the average noise measured on the silicon prototypes is ≈ 1.49 threshold-DAC counts. To convert this number in charge units, we need to multiply it for the threshold-DAC gain $G_{\text{TH-DAC}}$ and divide it by the gain of the front-end G_{FE} (pre-amplifier and sharper stages), for each channel, as:

$$\sigma_{e^-} = G_{\text{TH-DAC}} \left[\frac{\text{mV}}{\text{lsb}_{\text{TH-DAC}}} \right] \cdot \frac{\sigma_{CNT}[\text{lsb}_{\text{TH-DAC}}]}{G_{FE}\left[\frac{\text{mV}}{\text{fC}}\right]} \cdot (e^-)^{-1}.$$

The threshold-DAC is unique per chip and its gain error and linearity can be directly measured. The front-end gain instead may present an on-chip variability due to mismatch and needs to be therefore indirectly evaluated for each channel. Section 5.2.3 describes the G_{FE} measurements and variability. The average noise results in $\sigma_{e^-} = 330 \pm 11\ e^-$. This result is in agreement with the front-end simulations, assuming no capacitance at the input. Figure 5.8 shows the channel noise distribution across the ASIC. It is evident that the average noise is almost independent from the injected input charge. The noise map in Figure 5.7 can be used to identify eventual noisy strips.

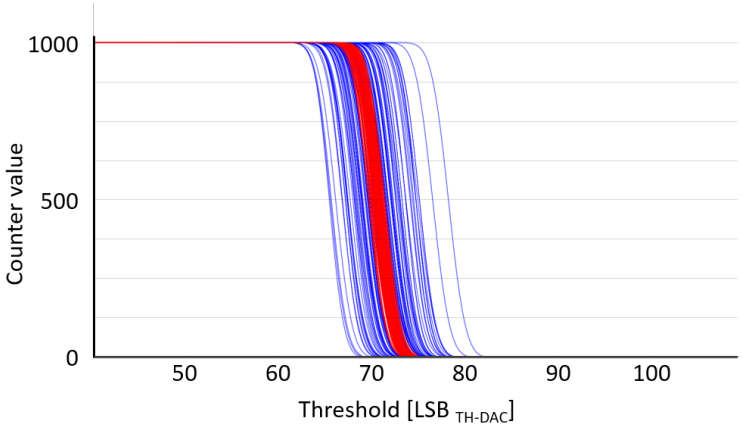


Figure 5.6. Complementary error function fitting of the number of events counted by the channel asynchronous counters for an injected charge of 1 fC and different values of the threshold DAC (S-curve).

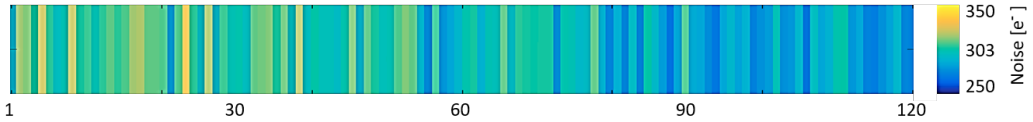


Figure 5.7. Front-End noise map across the SSA (0 fF input capacitance). It is calculated as the standard deviation of the error function fitting the S-curves around the threshold, for an injected charge of 2 fC.

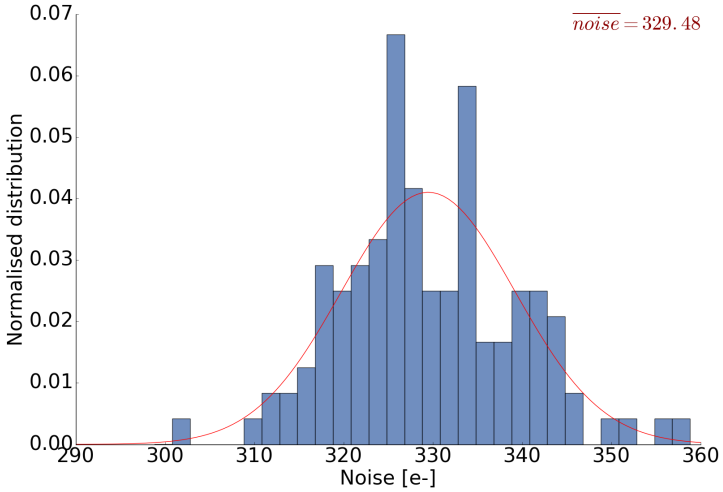


Figure 5.8. On-Chip distribution of the FE channel noise for an injected charge of 1.0 fC.

It is not the case for the chip presented in this example. In the target application with 5 pF sensor input capacitance, simulation results estimate an average of ENC of $\approx 900\,e^-$ fulfilling the application requirements.

5.2.3 Front-end gain indirect measurements and distribution

For different values of injected charge, it is possible to evaluate the comparator effective threshold in mV as the mean value of the S-curves fitting the counter for each channel. If the injected charge is within the linear response range of the charge-sensitive pre-amplifier, we can directly evaluate the front-end gain G_{FE} by linearly interpolating the threshold values. Figure 5.9 and Figure 5.10 shows respectively the S-curve measurements for different values of the input charge between 0.5 fC and 4.0 fC, and the G_{FE} measurement. Gain variation impacts the overall mismatch and

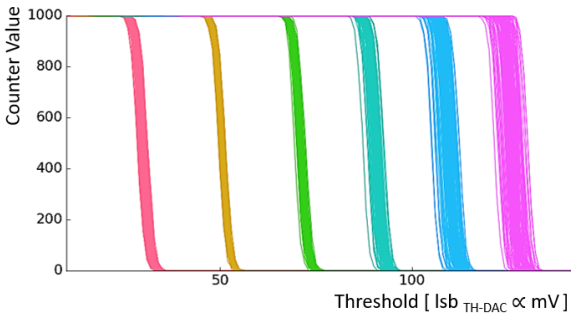


Figure 5.9. S-curves measured for different values of input charges. The mean value of the complementary error function fitting the counter values for each channel represents the effective threshold.

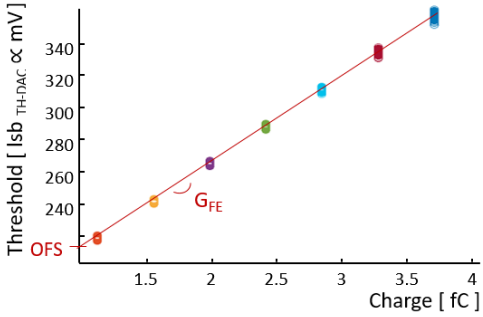


Figure 5.10. Front-End Gain and Offset measurement obtained by interpolating the average threshold value for different charges injected.

noise. Figure 5.11 shows the on-chip distribution of the gain for a not-trimmed ASIC. A 5-bit trimming-DAC per channel allows reducing the standard deviation of the G_{FE} to < 1 mV with a uniform distribution in the matrix. The average G_{FE} measured on the prototype is ≈ 54.53 mV/fC, in agreement with the simulation results.

5.2.4 Threshold mismatch, channels equalization, and minimum detectable charge

One DAC per chip controls the threshold voltage. To compensate for process and temperature variations, a process-compensation-DAC allows trimming the value of the threshold-DAC. It acts on its reference current generated from the embedded bang-gap voltage reference.

Due to on-chip variability and mismatch, the effective threshold may differ between the equally layout channels. The threshold (red and blue distributions in Figure 5.13) shows a standard deviation for a non calibrated ASIC $\sigma < 2.6\,\mathrm{LSB}_{\text{TH-DAC}}$ equivalent to $\approx 600\,e^-$ (for a measured $\overline{G_{FE}} = 54.53\,\mathrm{mV/fC}$ and $\overline{G_{\text{TH-DAC}}} = 1.923\,\mathrm{mV/LSB}$). This value proves to be within the range that the SSA front-end can compensate. Indeed, a 5-bits threshold-equalization DAC per channel allows correcting for the strip-to-strip threshold mismatch, even if no sensor is connected.

Figure 5.13-a shows the distribution of the threshold before and after applying the trimming procedure based on an iterative search of the optimal configuration. In par-

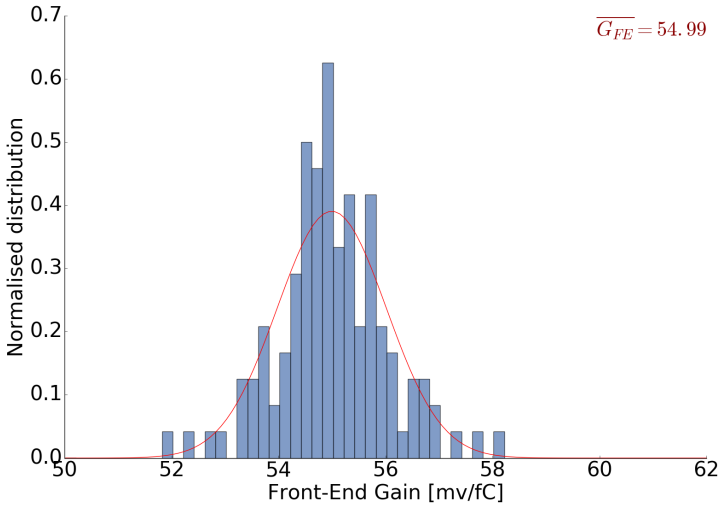


Figure 5.11. Front-end gain distribution for a non-trimmed SSA.

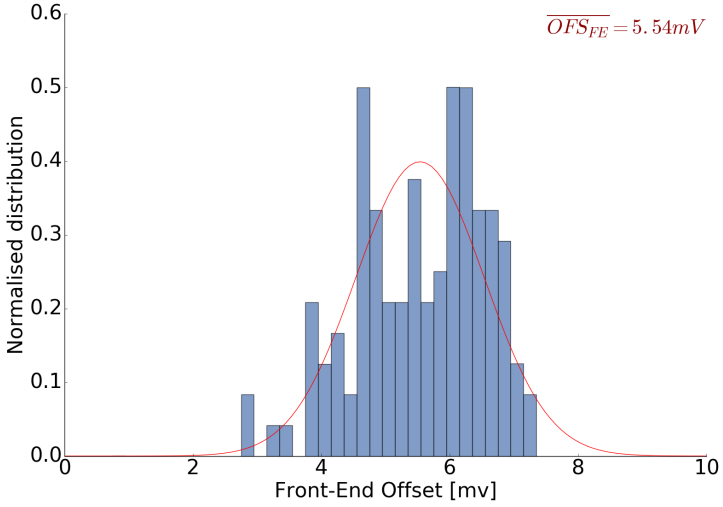


Figure 5.12. Front-end offset distribution for a non-trimmed SSA.

ticular, the green and red distribution are for a non-trimmed ASIC where all threshold-trimming DACs and all G_{FE} trimming DACs are set either to the minimum or maximum value. The blue plot shows the trimmed distribution achievable with three iteration steps. A $\sigma < 0.25\,\mathrm{LSB_{TH\text{-}DAC}} \approx 55\,e^-$ can be achieved.

The minimum detectable charge can be evaluated as the quadratic sum of mismatch and noise: $\overline{Q_{MIN}} \approx 355\,e^-$. It mostly depends on the noise performance. The dynamic range of the trimming-DAC proves to be sufficient to avoid degradation of this parameter.

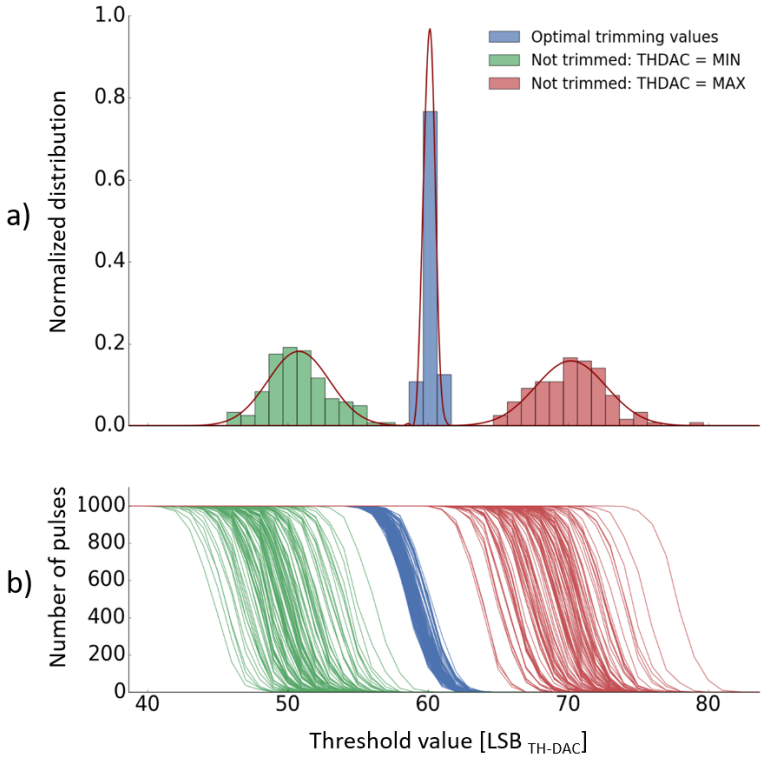


Figure 5.13. On-chip distribution of the effective channel threshold due to strip-to-strip threshold mismatch, before and after trimming procedure.

5.2.5 Bias variations and threshold-DACs linearity

An analog bias block located in the ASIC periphery generates the voltages and currents that are distributed to the strip array front-end channels. It allows compensating for process and temperature variation, as well to control the performance of the analog components like the channel pre-amplifier and the calibration voltages. Details on its implementation can be found in Section 4.5.2. Variability of the band-gap reference or of the threshold DACs may influence the gain and noise performance of the front-end. For this reason, it is necessary an accurate characterization of those components. The SSA provides accessibility of the internal bias voltages as a result of an accurately designed analog multiplexer that allows to make available several internal voltages to the dedicated wire-bond/bump pad. Figure 5.14 shows the integral non-linearity (INL) measured on the 8-bit threshold control DAC. As expected from simulation, the integral non-linearity is below 0.6 LSBs.

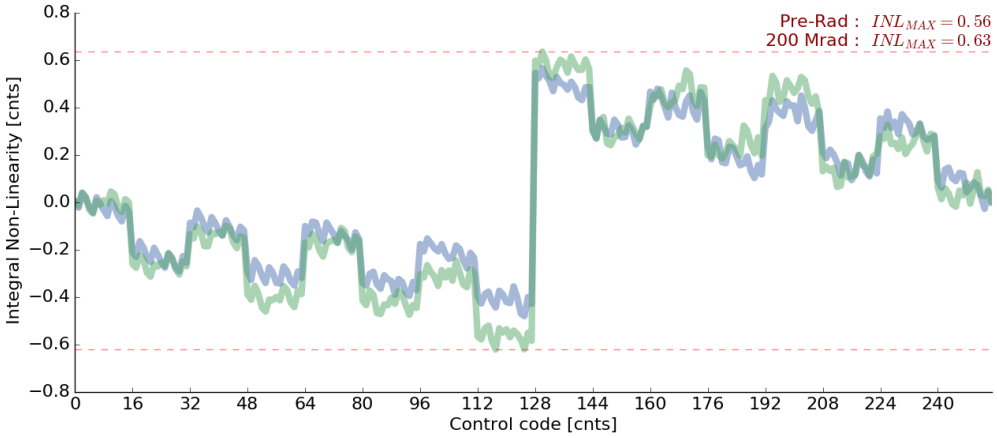


Figure 5.14. Threshold DAC integral non-linearity before and after irradiation at TID=100 Mrad

5.3 SSA-MPA and SSA-SSA communication

Two dedicated SLVS differential links operating at 320 MHz allows for lateral communication among SSAa while 9 differential links are implemented for the SSA to MPA communication. Clock and T1 synchronous commands are transmitted along the data lines.

Due to the strict power budget, neither the SSA lateral data receivers, nor the MPA stub and L1 receiver can implement phase aligners. For this reason, it is fundamental to guarantee that the information transmitted from the SSA to the MPA is equalized among the lines and in phase with the transmitted clock. The distribution of the clock to the re-sampling flip-flops located in the proximity of the drivers and the clock buffering was studied to guarantee a maximum skew of 0.4 ns in all operating corners while accepting larger variations in terms of absolute delay. For the lateral communication, where no clock is transmitted along the data, it was necessary to minimize the delay variations with the operating condition and guarantee, for every corner, that the signal gets sampled with the right phase. This requirement was achieved via a hand-made clock distribution. The SSA and MPA implement a minimal configurability to compensate for phase mismatches, including:

- sampling edge selection for T1 and data lines;
- sampling phase selection implemented with a four-bit shift register;
- transmission lines swapping;

- L1 data cycle alignment;
- BX and L1 Counters shift alignment;
- re-timing of the number of cycle pixel centroids should wait for strip centroids for the coincidence;

The SSA-SSA and the SSA-MPA communication was simulated with gate-level simulations with back-annotated delays for mixed corners (SSA max-MPA min, SSA min-MPA max, etc.)

The development of an additional carrier board mounting both ASICs allowed testing

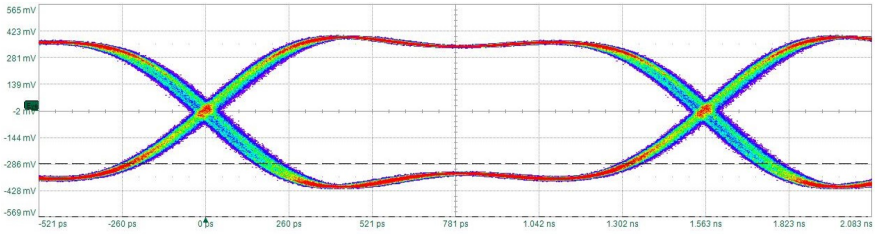


Figure 5.15. Eye diagram of the stub data-line at the SSA-output, MPA-input.

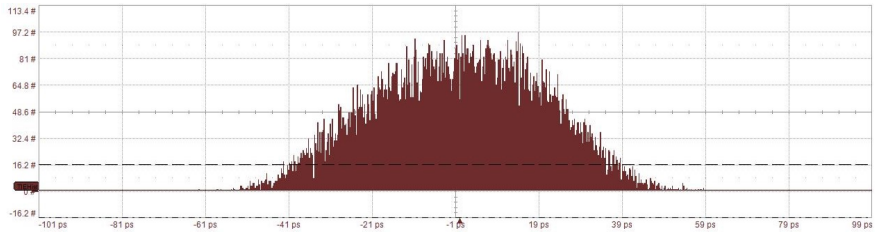


Figure 5.16. Jitter histogram measured on the stub data-line at the SSA-output, MPA-input.

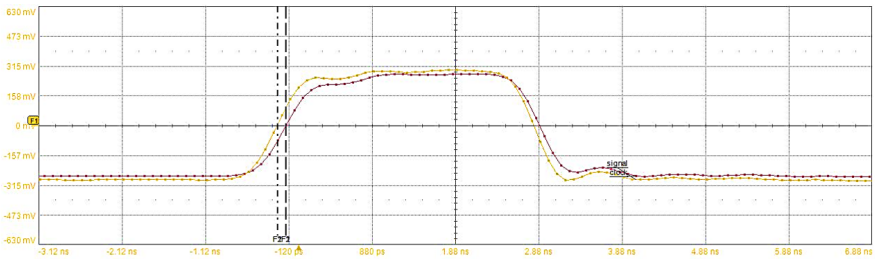


Figure 5.17. Phase difference (~ 100 ps) measured between the stub data-line 0 and the stub data-line 7, which SLVS drivers and bumps are located at the 9.3 mm of distance.

the communication between the silicon prototypes. Differential probe points provide accessibility to the signals. Figure 5.15 and Figure 5.16 show the eye diagram of the data at the SSA output and the jitter histogram. The average eye width is ~ 1.442 ns for the maximum driver current setting and ~ 1.430 ns for the minimum. The jitter is < ±60 ps (3σ). Figure 5.17 shows the phase difference (~ 100 ps) measured between the stub data-line 0 and the stub data-line 7, which drivers are located at the ASIC extremities with 9.3 mm of distance between each other. By injecting charge pulses at the front-end input of the SSA strip channels and of the MPA pixel front-ends, it was possible to generate and read-out correct stubs. No communication errors have been observed for SSA and MPA supply voltage down to 0.9 V.

The SSA implements the possibility to control the bias current for the SLVS transmitters. Higher current implies better signal integrity but higher power consumption. The SSA to MPA communication proved to work correctly as well at minimum bias current, allowing to save 27.2 mW per chip corresponding to ~ 436 mW per module. The lateral communication was verified with an additional carrier board where the two SSAs are connected to the PCB through the bump-bonded interposer. This design [259] will allow as well to characterize the SSA chip together with the silicon sensor.

5.4 Wafer probing results and production yield

The complete set of functional tests, bias measurements, calibration and front-end characterization has been performed on the 24 12-inches wafers produced as a result of the first prototyping engineering-run. A custom probe-card was designed while a test software was developed to automatize the wafer-probing procedure.

The procedure excludes in addition to non-functional chips, chips showing front-end

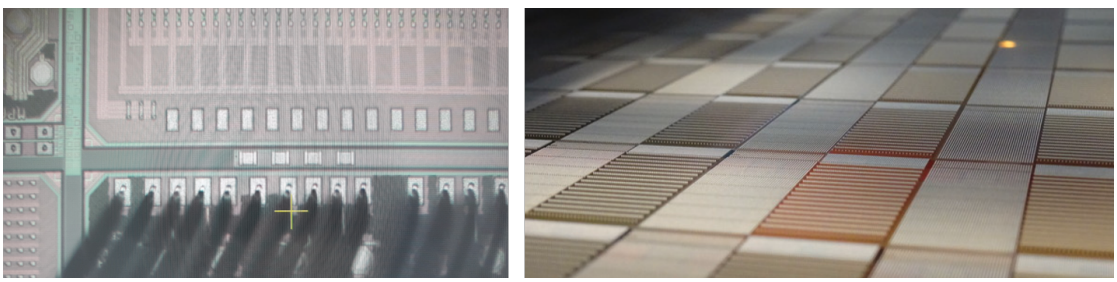


Figure 5.18. Microscope photo of the SSA wafer probing procedure.

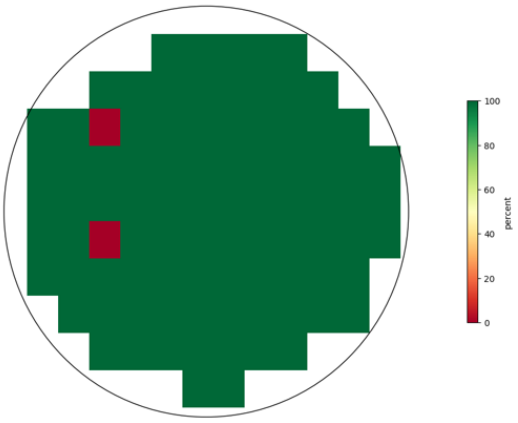


Figure 5.19. Digital functionalities test-results wafer map.

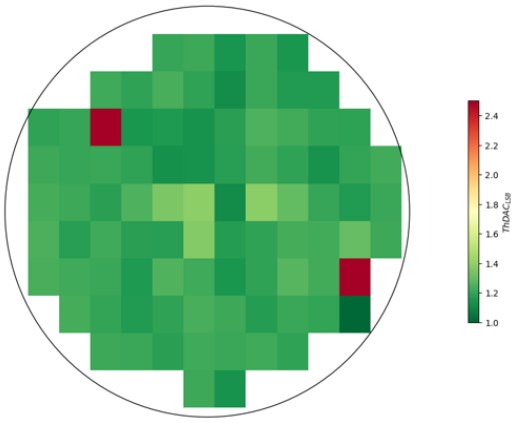


Figure 5.20. Average analog front-end noise wafer map.

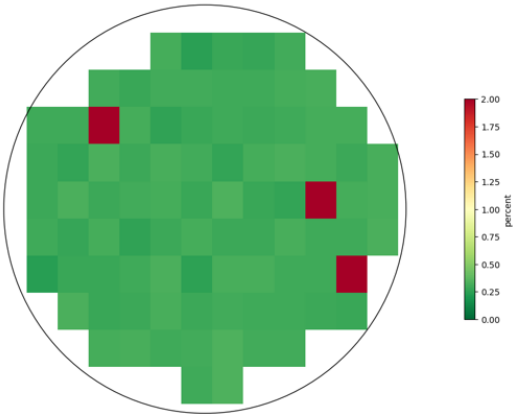


Figure 5.21. Wafer map of the achievable particle-hit detection threshold standard deviation after the calibration and the trimming procedures.

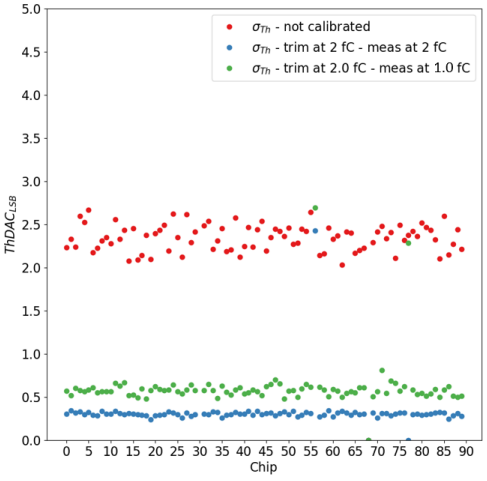


Figure 5.22. Average value of the particle-hit detection threshold standard deviation before and after the calibration and the trimming procedures.

circuits with a noise level above 400e$^-$, chips showing a threshold standard deviation above 0.6 THDAC$_{LSB}$ after trimming and chips showing parameters that, after calibration, does not fit in the defined operating range. The same system and procedure will be used in the final production testing. Figure 5.19 and 5.20 shows respectively the wafer map of the digital functionalities test results and of the average analog front-end noise. Figure 5.21 and Figure 5.22 show the wafer-map and the average values of the achievable particle-hit detection threshold standard deviation after applying

the self-calibration and the trimming procedures. The test results and the evaluated calibration values are stored on a database. A unique chip-ID is stored on the SSA e-fuses during the probing procedure allowing associating the database entries to the corresponding ASIC after dicing and module assembly. The overall yield, averaged over the 24 tested wafers, results in approximately 92%.

5.5 Total ionizing dose results

The expected dose in the CMS outer-tracker is obtained with the FLUKA simulation package [79]. Figure 2.5 shows the expected dose at 3000 fb^{-1} for the whole tracker. The worst case for the PS module is found in the first barrel layer at 23 cm from the vertex, corresponding to a total ionizing dose of < 100 Mrad. In order to irradiate the SSA and MPA prototypes up to such a dose was used an X-ray irradiation system (SEIFERT RP149), in which a 50 kV 3 kW X-ray tube uses a tungsten target [260].

The first SSA prototype was tested up to a total dose of 200 Mrad with a dose rate of 130 krad/min. After the irradiation, the chip was annealed for 24 hours at 100 ∘ C under bias. During the entire procedure, the logic was solicited continuously by injecting charge pulsed at the front-ends input and L1 trigger requests, in order to avoid unrealistic bias-dependent effects on the devices. The test system constantly monitored power consumption, front-end performance, and digital functionalities.

5.5.1 Effects on digital circuits

The performance degradation depends on the bias and temperature applied both during and after irradiation. Transistor studies show that p-type transistors with minimal dimensions have a I_{ON} degradation of more than 40% already at 100 Mrad. Since most of the standard cells in the digital libraries use minimum length transistor and width < 200 nm, similar results could also be expected for the digital logic. However, while single-device tests are performed at worst bias condition, the switching activity average the effect in the digital circuits.

The triggered readout and the continuous transmission of cluster centroids, together with all other digital functionality, did not show any failure during irradiation up to 200 Mrad at the operating frequency. The SSA digital circuit was indeed implemented

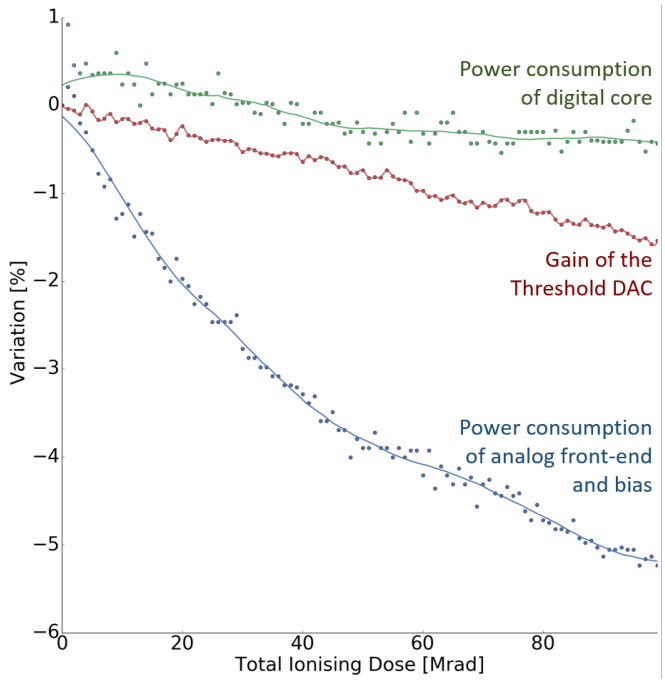


Figure 5.23. Percent variation of the power consumption of the digital core (green), the power consumption of the analog front-end and bias generation blocks (blue) and variation of the threshold DAC Gain $G_{TH\text{-}DAC}$ with respect to the total ionizing dose.

taking into consideration this degradation. Static timing analysis and the post-layout simulations were performed using a re-characterized digital cell library. A variation of <1% in the digital core power consumption and of up to ≈ 6% for the analog front-end current was observed during irradiation. Figure 5.23 shows their percent variation up to 100 Mrad. The internal band-gap reference voltage shows a very weak dependence on the radiation dose (< 1%). The gain of the threshold DAC, measured on the wire-bond test point, shows a variation of about 2% (red curve in Figure 5.23).

5.5.2 Effects on bias, analog front-end and noise performances

For what concerns the analog front-end, most of the studies described in the previous sections have been also repeated during the irradiation procedure. Figure 5.24 shows the effective threshold distribution across the ASIC before and after irradiation at +25°C (blue and green distributions). It is observable a shift in the threshold mean value and in its σup to ≈ 0.9 LSB_{THDAC}. This effect is certainly related to the variation of the biasing current supplied to the threshold DAC and the charge injection. The

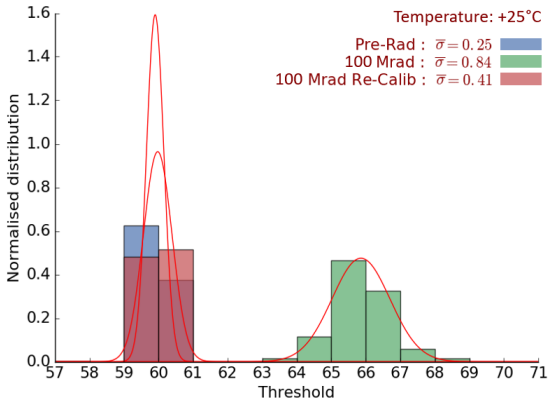


Figure 5.24. Distribution of the channel threshold value before and after irradiating the ASIC up to 100 Mrad at +25°C.

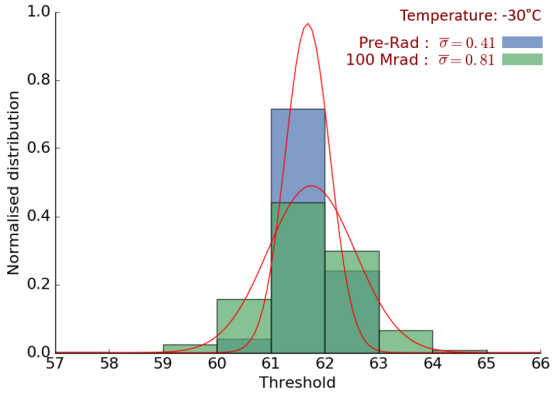


Figure 5.25. Distribution of the channel threshold value before and after irradiating the ASIC up to 100 Mrad at −30°C.

dynamic range of the bias DACs and the channel trimming DACs allows compensating for this error. The red histogram in Figure 5.24 shows the threshold distribution of the same irradiated ASIC, after repeating the calibration procedure. As shown in Figure 5.25, the effect is almost negligible when the ASIC is irradiated with a constant temperature of −30°C, in agreement with the results described in [8]. −30°C is indeed the temperature of the cooling system of the PS module.

As presented in Figure 5.26, a ≈ 20% increase of the average channel noise was measured on the ASIC irradiated at room temperature. This effect is due to the convolution of multiple factors: the decrease of the channel gain G_{FE}, the reduction of the biasing currents of the analog front-end and the increase of the noise in the pre-amplifier input stage. By re-calibrating the SSA bias block after the irradiation, it is possible to

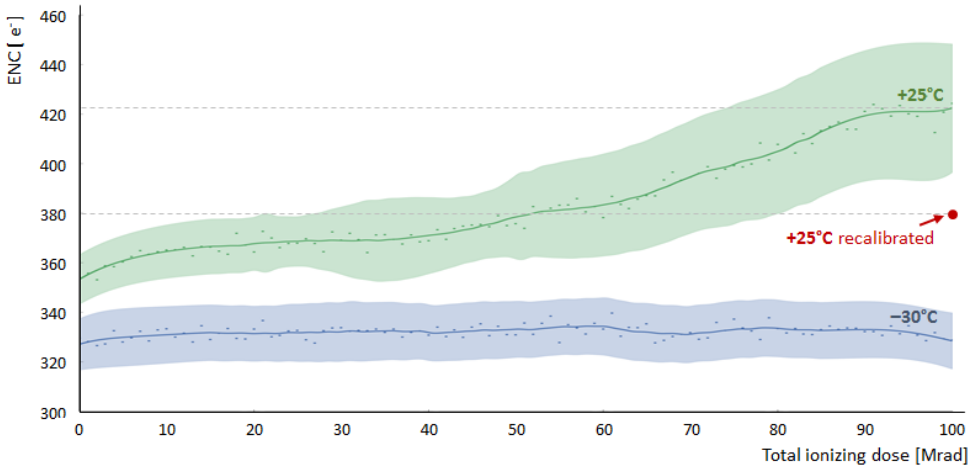


Figure 5.26. Front-End ENC respect to the cumulative ionizing dose for an ASIC irradiated at +25°C (green line) and at −30°C (blue line). The thick line represents the average measured ENC while the lighter filled area represent the 3σvariation around this value. The red dot located at 100 Mrad represents the measured ENC at +25°C after re-calibrating the bias circuit.

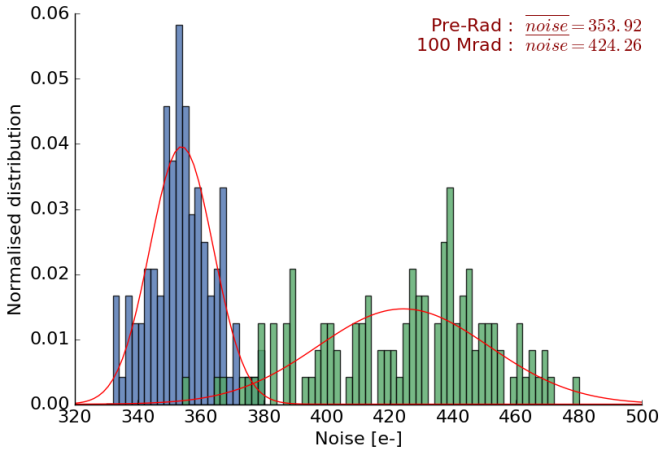


Figure 5.27. Front-End ENC distributions at pre-rad (blue histogram) and after a total dose of 100 Mrad (green histogram) for an SSA irradiated at at +25°C.

decorrelate the two factors and evaluate the actual noise increase due to the front-end. The red dot located at 100 Mrad in Figure 5.26 shows the actual increase in terms of ENC. Repeating the measurement on a different chip, this time calibrating the front-end for bias variation during the irradiation (Figure 5.28), the ENC degradation is less prominent.

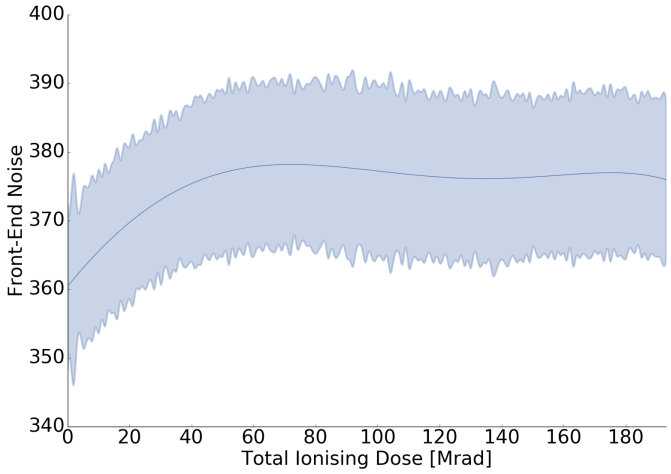


Figure 5.28. Front-End ENC degradation with TID up to 200 Mrad, measured at +25°C for a calibrated SSA ASIC. The thick line represents the average ENC while the lighter filled area represent the 3σmeasure error (10^3 samples per point)).

The reason for the ENC degradation is related to the flicker noise increase in the pre-amplifier input stage, rather than thermal noise. Measurements in this technology show a dependency of the NMOS $1/f$ noise performance by ionizing radiation because of effects associated with lateral isolation oxides (shallow trench isolation region) [205]. This mechanism is particularly evident in the low current density region (< 100 µA), where the front-end devices operate because of low power requirements [232]. The front-end input stage transistors are layout with an edge-less enclosed structure (ELT) to minimize this effect. As shown in Figure 5.28, the measured ENC in the SSA prototype increased mostly in the first part of the irradiation of about < 9%. This result is in agreement with the < 6% degradation observed in the MPA prototype. Compared with the +20 % ENC increase that was observed in the first MPA front-end prototype (MPA-Light) [8], where no enclosed-layout strategy was adopted, it proves the effectiveness of the ELT at the input stage.

5.6 Single-event radiation effects studies

As discussed in Chapter 4, the SSA ASIC implements a Single Event Upset (SEU) tolerant design. The amount of energy that an ionizing particle transfers to the material traversed per unit distance (dE/dx) is defined as the stopping power of the particles. The stopping power describes the energy loss of a particle per path length

and is approximated using the Bethe formalism. More important for the effects in silicon is the Linear Energy Transfer (LET). LET describes the energy transferred into a narrow region around the primary ion track. It represents, therefore, the retarding force acting on a charged ionizing particle traveling through the silicon [261].

The LET depends on the nature of the radiation as well as on the material traversed. While the LET of a pure beam of ions with fixed energy is well defined, the LET of a mixed radiation field is more complex, and the calculation has to be averaged over the different contributing ions.

The SEU sensitivity of a circuit can be tested by irradiating the device using heavy ions. Cyclotron facilities are suitable to irradiate components with several types of ions. The MPA and SSA ASICs have been tested at the UCL-CRC-HIF (Université catholique de Louvain – Cyclotron Resource Centre – Heavy Ion Facility) [262], where heavy ions are accelerated towards the target device located into a vacuum chamber. The beam was in first approximation uniform over a 2 cm diameter and feature a maximum fluence of $1.5 \cdot 10^4$ particles$\cdot$cm^{-2}s^{-1}. Table 5.29 summarizes the properties of the ion used for the SSA test. Considering fixed energy, each ion features characteristic LET. The usage of several ions allowed to extrapolate sufficient parameters to evaluate the sensitivity and the error rates that should be expected when the ASICs will operate in the CMS outer-tracker environment.

The SSA test setup has been adapted for SEU tests. A dedicated version of the test firmware allows to real-time check the ASIC output data against the expected patterns

Ion	Energy [MeV]	LET [MeV$\cdot$mg^{-1}cm^{-2}]	Range on silicon [µm]
$^{13}C^{4+}$	131	1.3	269.3
$^{22}Ne^{7+}$	238	3.3	202.0
$^{27}Al^{8+}$	250	5.7	131.2
$^{40}Ar^{12+}$	379	10.0	120.5
$^{53}Cr^{16+}$	513	16.0	107.6
$^{58}Ni^{18+}$	582	20.4	100.5
$^{84}Kr^{25+}$	769	32.4	94.2
$^{103}Rh^{31+}$	927	45.8	88.7
$^{124}Xe^{35+}$	995	62.5	73.1

Figure 5.29. Properties of the heavy ions utilized in the SSA and MPA SEU characterization.

minimizing the TCP/IP communication. It allowed for higher test rates (up to 40 MHz for the stub data and up to 1 Mframe per second for the L1 data) in order to fully exploit the time slot available for the SEU testing. A water cooling system allows to stabilize the temperature in the vacuum and remove the test-board and ASIC heat.

For each LET, a data acquisition window of ~ 20 minutes provided sufficient statistics, in particular at low LETs where the expected error rates are meager. To increase the number of measurements, the ASIC has been irradiated with multiple beam incident angles, allowing to exploit an increase in the LET. Due to the fluctuations of the ion beam, the test software regularly measured the beam flux allowing to normalize the acquired error rates.

For each run, the test procedure consisted of the readout of stub data and L1 raw data at the SSA/MPA output achieved by injecting random generated digital calibration pulses at the channel inputs. The L1 trigger rate was set to 1 MHz. Only frames including errors and statistics counters are saved in the FIFO (located in the DRAM memory on the FPGA board) and are accessible by the control software routines for further analysis. The BX counter values are stored along with the error frames and provide a time reference of where the SEU happened, allowing to verify if SEU could generate errors for multiple consecutive events.

Besides, the static configuration registers were regularly monitored reading out every 30 seconds the values via the serial interface. The SEU counter, implemented both in the SSA and MPA ASICs, increments for every upset on the configuration register that the logic has internally corrected.

5.6.1 SEU induced errors in control logic

The configuration logic is fully triplicated as described in Section 4.6.5. The triplication eliminates all single-bit upsets by refreshing the register value with the one obtained by the voting of the three instances, every time a discrepancy is detected. Only a multi-bit upset can lead to errors in the stored values.

As a first result from the heavy ion test campaign, configuration errors not corrected by the triplication logic have been observed on two registers. These multi-bit single event upsets have been traced back on the design and resulted to happen on flip-flops

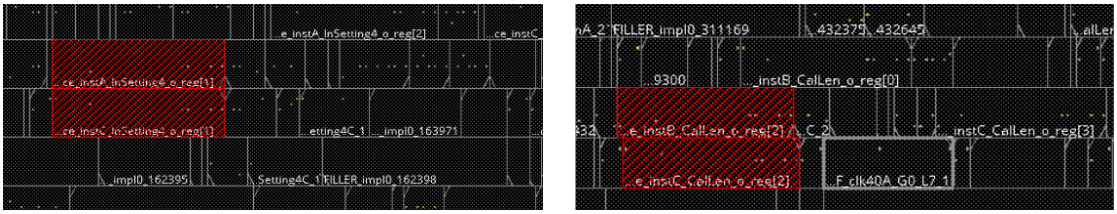


Figure 5.30. SEU-weak standard-cell placement observed for two flip-flops storing configuration values.

placed at a minimum distance between each other as visible in Figure 5.30. During the implementation, the standard cell placement has been constrained via instance groups to guarantee a minimum distance of 15 µm among triplicated instances. The successive post-routing optimization steps may move the standard cells to optimize the timing. Due to a bug in the design, the two registers showing the error were not adequately constrained in a fixed location. This bug is now corrected for the final version of the ASIC. In particular, it is more convenient to implement the configuration as a hierarchical block composed of 32×8 registers with auto-correction, simplifying the spacing constraining while allowing the optimization to freely move the cells composing the data path.

Besides, in 3 measurement runs out of the 128, was observed that parts of the state machines got reset, leading to a temporary loss of the functionalities and partial loss of the configuration. The effect was traced back on the design to an erroneous constraining of the reset distribution that leads to a simplification of the reset tree during optimization. As well in this case, the bug has been corrected for the final version. Furthermore, the reset input CMOS-pad radiation tolerance will be improved.

5.6.2 Cross-section measurements

The SSA and MPA data path is not directly protected against single event effects due to the strict power budget. An upset in the data pipeline may lead to an erroneous event without affecting the ASIC functionalities. It is necessary to evaluate the ASIC data-path sensitivity to SEU to derive the expected error rates. Looking at the average number of particle N_S scattered into the solid angle $d\Omega$ in the unit of time, the differential cross-section is defined as [263]:

$$\frac{d\sigma}{d\Omega}(E,\Omega) = \frac{1}{F}\frac{dN_S}{d\Omega}$$

The integral over the solid angle represents the total cross section:

$$\sigma(E,\Omega) = \int \frac{d\sigma}{d\Omega} d\Omega$$

The total cross section has the dimension of an area and can be considered as the section normal to the beam direction outside of that the particle is not deflected. However, despite this definition, we can think the cross section as a measure of the interaction probability [264]. The SEU cross-section σ can be therefore calculated as the ratio between the number of soft-errors N_{SEU} counted during a defined the time window T and the particle flux ϕ,

$$\sigma = \frac{N_{SEU}}{\phi \cdot T}.$$

Since the ion beam flux showed significant fluctuations during the test, the results are normalized according the integrated flux. The measured SEU cross-section as a function of the heavy ions LET are presented in Figure 5.31-5.32 for the SSA ASIC and in Figure 5.33-5.36 for the MPA ASIC. The measurement error on the cross section values is related to the the uncertainty on the fluence value (assumed $100\,s^{-1}cm^{-2}$), the Poisson error on the counts, and the variability of the measurement time (1 s).

Experimental SEU cross-section data as function of the deposited energy can be fit with a integral Weibull distribution:

$$\sigma = \sigma_0 \left(1 - e^{-\left(\frac{E_{dep}-E_0}{W}\right)^s}\right),$$

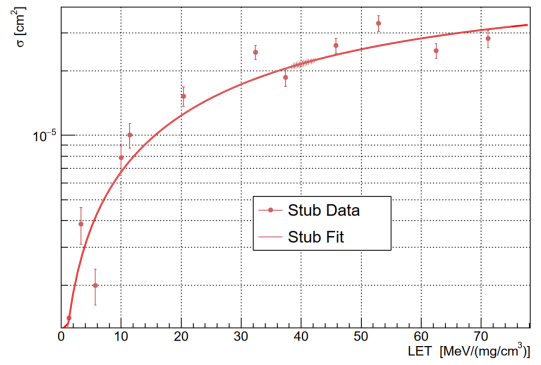
where E_{dep} is the deposited ionization energy, σ_0 is the saturation value of the SEU cross section, E_0 is the SEU threshold energy for $E_{dep} \mid \sigma(E_{dep}) \to 0$ and W and s are parameters directly dependent on the sensitive volume depth and shape. The Weibull function provides excellent flexibility in the fit of the cross-section turn-on and its plateau [265]. The free parameters obtained by the fitting are reported for each plot.

The deposited energy value under which the probability of an upset tends to zero represents the minimum energy required to change the state of a node in the circuit. In other words, the minimum energy required by an ionizing particle for generating the minimum number of $e^- h^+$ pairs collected at the junction, capable to alter the logic level. The threshold LET represents therefore the LET value for the most sensitive

region of the ASIC. The linear energy transfer at which 50% of the cell in the design gets upset, represents the charge deposition needed to upset the median cell of the design. For higher values of deposited energies, the SEU upset rate increases with an asymptotic behavior. The saturation value is reached at the LET where all sensitive areas of the circuit can get upset when hit by an ion capable of depositing that energy per unit of area. A further increase of LET would not have any additional effects.

The SEU rate can be calculated using the differential rate of each sensitive region, in combination with an integral weighting where the weights are obtained by the Weibull fitting of the measured cross-section values [265] The cross-sectional area can be calculated as the ratio between the Weibull fit saturation value σ_0 and the total number of sensitive nodes in the circuit.

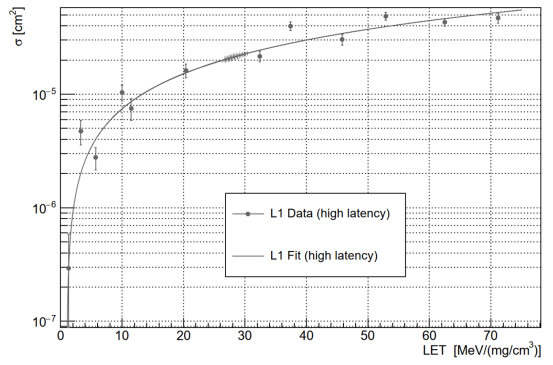
The heavy ion irradiation does not provide information regarding the sensitive volume integrity. It may refer to a few sensible cells or multiple smaller sub-cells [266]. In the hypothesis of a thin absorber in comparison to the particle range, we can approximate the sensitive volume by multiplying the cross-sectional area by the thickness of the sensitive depth of the die d. Making use of the same approximation, the deposited energy can be related to the LET as: $E_{dep} = \text{LET} \cdot \rho_{Si} \cdot d \quad \text{mg} \cdot \text{cm}^{-2}$, where $\rho_{Si} =$



SSA STUB Cross-Section fitting parameters

NAME	VALUE	ERROR
W	8.37092e+01	1.59949e+01
s	7.42178e-01	3.23398e-02
σ_0	5.13792e-05	6.50029e-06
E_0	6.31081e-01	1.55660e-01

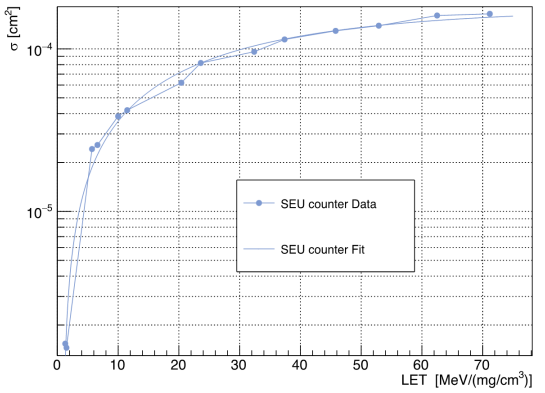
Figure 5.31. Measured cross-section as function of the LET for the SSA Stub-data clusters.



SSA L1 HIGH LATENCY Cross-Section fitting parameters

NAME	VALUE	ERROR
W	5.20368e+05	3.96484e+05
s	9.51533e-01	5.48353e-02
σ_0	2.52762e-01	2.22431e-01
E_0	1.00781e+00	3.45747e-01

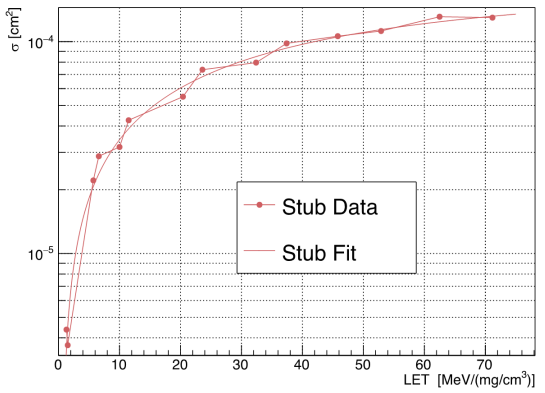
Figure 5.32. Measured cross-section as a function of the LET for the SSA output L1 data (SSA configured for 12.6µs latency operating mode).



MPA SEU COUNTER Cross-Section fitting parameters

NAME	VALUE	ERROR
1 W	3.50011e+01	4.52655e-01
2 s	1.10139e+00	4.06457e-03
3 σ_0	1.77200e-04	1.44235e-06
4 E_0	9.35516e-01	5.52530e-03

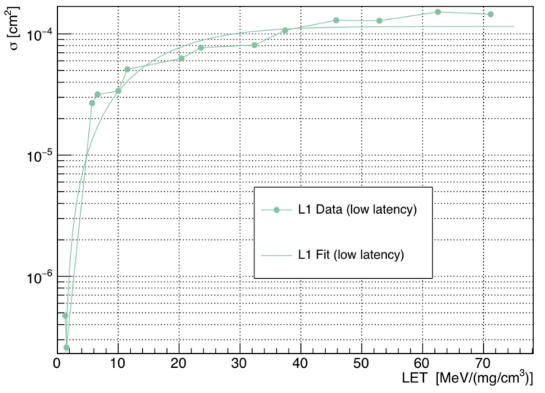
Figure 5.33. Measured cross-section as a function of the LET for the MPA Stub-data clusters.



MPA STUB Cross-Section fitting parameters

NAME	VALUE	ERROR
W	5.28951e+01	1.73172e+00
s	9.00631e-01	6.17349e-03
σ_0	1.81448e-04	3.31325e-06
E_0	6.21185e-01	1.41624e-02

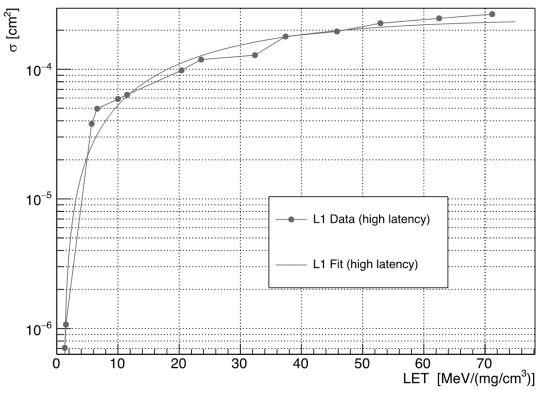
Figure 5.34. Measured cross-section as a function of the LET for the MPA counter of internally corrected SEUs.



MPA L1 LOW LATENCY Cross-Section fitting parameters

NAME	VALUE	ERROR
W [Ev]	1.77973e+01	1.90756e-01
s	1.55999e+00	7.42936e-03
σ_0 [cm²]	1.15184e-04	7.35651e-07
E_0 [Ev]	1.06672e+00	5.98670e-03

Figure 5.35. Measured cross-section as a function of the LET for the MPA output L1 data (MPA configured in 1.0µs latency operating mode).



MPA L1 HIGH LATENCY Cross-Section fitting parameters

NAME	VALUE	ERROR
W	2.91564e+01	3.94305e-01
s	1.19111e+00	4.06719e-03
σ_0	2.44381e-04	2.16112e-06
E_0	1.11564e+00	3.14482e-03

Figure 5.36. Measured cross-section as a function of the LET for the MPA output L1 data (MPA configured in 12.6µs latency operating mode).

$2.32\,\mathrm{g}\cdot\mathrm{cm}^{-3}$ is the density of the silicon. Clearly this approximation is quite strong.

From Figure 5.35 and Figure 5.36, the cross-section plateau σ_0, and consequently the error rate, for an SSA or MPA configured to operate with a 12.6µs trigger latency is about two times higher compared to the cross-section for the same ASIC operating at 1µs trigger latency. This behavior is explained by the time that the data spend into the embedded memory before to be transmitted. From the difference, it is possible to evaluate the contribution of the memory to the SEU-related error rate and decouple it from the pipeline.

Due to the limited statistics on the SSA data at low latency, the Weibull distribution fitting is not accurate at low LET and it is not reported here. The situation is different for the MPA that, featuring an area 16 times larger area due to the assembly constraints, shows a more significant sensibility to SEU. The analysis based on the high latency data can be assumed as an upper limit for the error rate.

5.6.3 Error rates evaluation

In a simplistic approach, the probability of having an SEU correspond to the probability that the charge collected at a given node is higher than the minimum charge needed to upset its logic state. This critical energy (E_{crt}) depends on the circuit characteristics and the material. Not taking into consideration the efficiency of the charge collection and its time constant, the SEU probability is equivalent to the probability that the energy deposition within a sensitive volume exceeds a E_{crt}. In the step-like critical energy approximation, the SEU rate for a specific ion with a certain energy is given by the probability to have an energy deposition greater than E_{crt} multiplied by the ion flux. Taking into account the efficiency of the charge collection in the calculation is not trivial. It requires the knowledge of the sensitive nodes of the circuit. Such calculation could be performed for a simple device but becomes impossible when characterizing a complex digital circuit. Heavy-ion experimental data, anyway, implicitly includes information concerning the charge collection within the sensitive volume.

Multiplying the upset cross-section for the average hadron fluxes at the LHC peak luminosity gives a coarse approximation of the upset rate. It allows noticing that the contribution given by high energy hadrons is dominant with at least one order of mag-

nitude compared to the contribution of low energy hadrons (< 20 MeV) to the upset rate. For this reason, in the following calculation, only hadrons with energy > 20 MeV are considered. In addition, experimental results on a DRAM test chip from literature [266] and in the work described in [266], has shown that the measure SEU rates are dominated in all regions of CMS by hadrons above 20 MeV.

The cross-section for a specific particle and energy Σ can be approximated as the convolution of the Weibull distribution as a function of the E_{dep} and the energy deposition probability as:

$$\Sigma = \int_0^\infty \frac{1}{A} P(E_{dep}) \sigma(E_{dep}) dE_{dep},$$

where P represent the energy deposition probability and A the cross-sectional area of the sensitive volume used in the simulation of the energy deposition probability ($1 \times 1 \times 1\,\mu m^3$). The same expression can be extended in the case of a radiation environment composed of multiple particle types (n), in the assumption that their effects are independent:

$$\Sigma = \int_0^\infty \sum_n \left[\frac{1}{A} P(n, E_{dep}) \sigma(E_{dep}) \right] dE_{dep}.$$

We can, therefore, multiply for each energy bin j, the energy deposition probability P_j by the increase of sensitive area within the same energy interval $\Delta\sigma_i = (\sigma_{i+1} - \sigma_i)/\sigma_0$ from the Weibull fitting of the SSA experimental data, and approximate the SEU cross-section for a given energy and particle as:

$$\Sigma \approx \sigma_0 \sum_{j=0}^{\infty} \frac{P_j \cdot \Delta\sigma_j}{A}.$$

To evaluate the error rate specifically for the CMS outer-tracker region and for 13 TeV proton-proton collisions, the Weibull fit needs to be convoluted with the probability distribution of Figure 5.37. It represents the probability of having, within a volume of $1 \times 1 \times 1\,\mu m^3$, an ionizing deposition per unity of flux greater or equal of E_{dep}, taking into consideration only hadron with energy higher than 20 MeV in the CMS tracker.

Considering low energy neutron reactions (E<20 MeV) in the calculation would have introduce a significant error due to its strong dependency on the die sensitive depth. The value used is, in fact, an approximated guess and it is strongly dependent on the

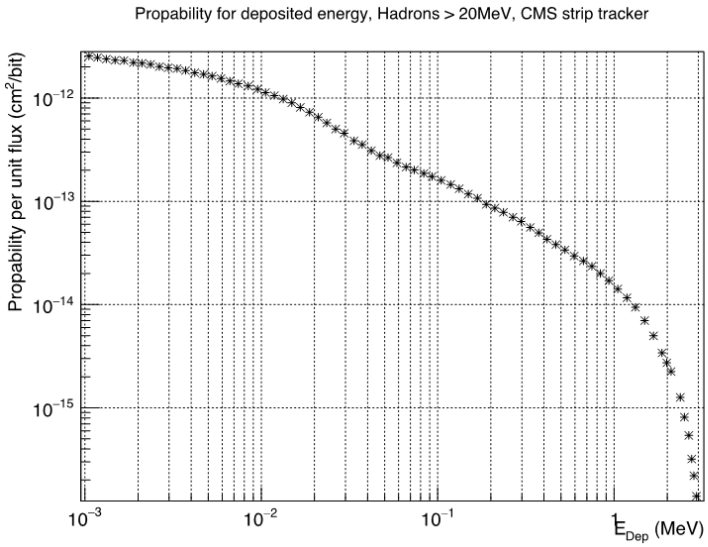


Figure 5.37. Energy deposition probability distribution for the CMS outer-tracker spectrum. The curve shows the probability to have within the sensitive volume an ionizing deposition greater or equal to the indicated E_{dep} value, considering all Hadrons with an energy higher than 20 MeV

specific electronic device. The dependency from the sensitive depth becomes rapidly less significant for more energetic recoils emitted in high energy scattering [266]. The cross-section values for SSA and MPA ASICs are summarized in the table in Figure 5.38.

In the CMS experiment, the composition of the radiation is dependent on the distance r from the nominal interaction point and from the pseudorapidity η. It can be assumed as uniform for this calculation if considering a small section as the PS barrel layers ($200 < r < 600\,\text{mm}, \eta < 3.2$). On the contrary, the flux is strongly dependent from r and z as represented by Figure 5.39 form the FLUKA [78] simulations obtained using the OT tkLayout version 614 [267] for a 13 TeV pp collision, in the volume of interest. As expected, PS modules located on the inner barrel layers at $r = 21\,\text{cm}$) will see the highest fluxes. Figure 5.40 reports the maximum expected flux as a function

	SEU Counter	Stub data	L1 data (1 µs)	L1 data (12.6 µs)
MPA	$6.77 \cdot 10^{-11}\,\text{cm}^2$	$7.92 \cdot 10^{-11}\,\text{cm}^2$	$5.59 \cdot 10^{-11}\,\text{cm}^2$	$9.55 \cdot 10^{-11}\,\text{cm}^2$
SSA	-	$2.74 \cdot 10^{-11}\,\text{cm}^2$	$0.82 \cdot 10^{-11}\,\text{cm}^2$	$1.39 \cdot 10^{-11}\,\text{cm}^2$

Figure 5.38. MPA and SSA SEU cross-section values for the CMS outer-tracker particle spectrum for 13 TeV proton-proton collisions.

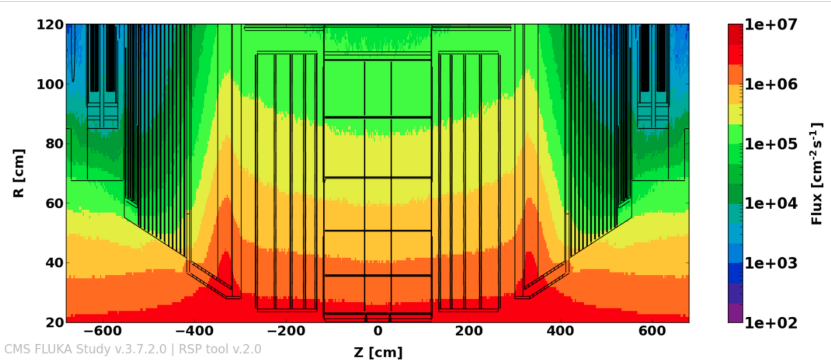


Figure 5.39. r-z flux map [cm^{-2}s^{-1}] for Hadrons with E>20 MeV in the CMS tracker for a 13 TeV p-p event, $10 \cdot 10^5$ μb^{-1}s^{-1} [267].

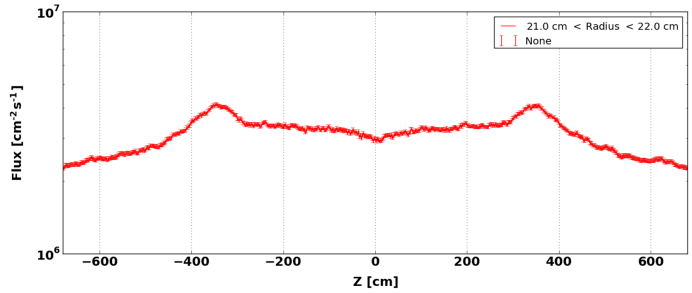


Figure 5.40. Flux [cm^{-2}s^{-1}] for hadrons with E>20 MeV in the CMS tracker for a 13 TeV p-p event as function of z coordinate, $10 \cdot 10^5$ μb^{-1}s^{-1}.

of z for hadrons > 20 MeV and $r = 22$ cm. The peak, located at $z = 265$ cm, is equal to $\sim 1.6 \cdot 10^7$ cm^{-2}s^{-1}.

The SEU upset rates for MPA and SSA can be directly calculated from the cross-section and the particle flux. The results are presented in the table in Figure 5.41 for $r = 210$ mm and $r = 600$ mm. The error rate at the PS module output is given by the combined effect of the error on the SSA, on the MPA and the CIC. An error in the SSA is not necessarily translated to an error at the module output. In the hypothesis that:

- errors due to SEUs in MPA and in SSA are not correlated. The ASICs do not physically overlap in a module. In any case, the effects on the digital circuit would be independent;
- the concentrator ASIC CIC is not taken into account for this analysis. No data is available at the moment concerning the CIC sensitivity;
- The CIC is agnostic of SEUs in MPA. The MPA is agnostic of SEUs in SS;
- The strip and pixel occupancy is such that the CIC is operating at the bandwidth

limit where it is just able to pass all the stub and L1 data received (worst-case);

we can calculate the L1 raw data error rate as the sum of the MPA and SSA error rates, multiplied by the number of ASICs transmitting to a single CIC and normalized to an event which does fit the maximum CIC output bandwidth. The MPA and SSA test were in fact carried at an extreme occupancy to maximize the data samples in the irradiation time. Using the high latency value as the most conservative and most representative for the operation in CMS, the upset rate normalized for the module output bandwidth is $\sim 2.5 \cdot 10^{-3}\,\mathrm{s}^{-1}$ per module.

For what concerns the stub data-path, the calculation is more complicated. Not every error in the SSA generate an error at the CIC input. Three categories can be identified.

- SSA fake hits that appear within the search window of the MPA stub-finding logic, leading to a fake stub:

$$P_{[StubErr|SSA+]} = \frac{\mathrm{SW}}{120}\, P_{[ClusterErr_{MPA}]}\, P_{[ClusterErr_{SSA}]},$$

  with SW = Stub Search Window
- SSA errors that lead to a stub cancellation:

$$P_{[StubErr|SSA-]} = \sum_{i=1}^{max} \overline{N_{Stub_i}}\ \overline{W_{\mathrm{Cl}_i}} (P_{[ClusterErr_{MPA}]} P_{[ClusterErr_{SSA}]})$$

- SEUs that affect the data packets directly in output (output formatter, FIFO or serializers): $P_{[DataErr_{SSA}]}$

For the MPA, the error rate already take into consideration all components weights

	R [cm]	Z [cm]	Hadrons E>20 Mev [$\mathrm{s}^{-1}\mathrm{cm}^{-2}$]	Er. rate Stub [$\mathrm{s}^{-1}\mathrm{Chip}^{-2}$]	Er. rate L1 [$\mathrm{s}^{-1}\mathrm{Chip}^{-2}$]	Er. rate L1 [$\mathrm{s}^{-1}\mathrm{Chip}^{-2}$]
MPA	21	265	$1.67 \cdot 10^{-7}$	$1.32 \cdot 10^{-3}$	$9.33 \cdot 10^{-4}$	$1.59 \cdot 10^{-3}$
	60	265	$2.32 \cdot 10^{-6}$	$1.83 \cdot 10^{-4}$	$1.29 \cdot 10^{-4}$	$2.21 \cdot 10^{-4}$
SSA	21	265	$1.58 \cdot 10^{-7}$	$4.58 \cdot 10^{-4}$	$1.36 \cdot 10^{-4}$	$2.32 \cdot 10^{-4}$
	60	265	$2.32 \cdot 10^{-6}$	$6.35 \cdot 10^{-5}$	$1.88 \cdot 10^{-5}$	$3.21 \cdot 10^{-5}$

Figure 5.41. PS module expected error rates for the CMS outer-tracker particle spectrum and fluxes.

since, during the test, the MPA was receiving SSA emulated data frames from the FPGA. To decouple different SSA related error sources and evaluate their effects at the MPA output is unfortunately not possible with the available data, due to limitations in the digital circuit observability. For a worst case analysis it can be assumed that:

$$P_{[MPA-StubErr]} = (P_{[MPA-StubErr|SSA]} + P_{[MPA-StubErr|MPA]}) \leq (P_{[ClusterErr_{MPA}]} P_{[ClusterErr_{SSA}]})$$

The probability of having a stub error at the MPA output is always smaller than the sum of the probabilities of having a cluster error in the two ASICs. $P_{[MPA-StubErr]}$ should then be normalized for the maximum CIC stub data input bandwidth of 25.6 Gb/s. Table in Figure 5.42 summarizes the worst case error rates expected at the PS module output. This results in an upset rate of $< 1.3 \cdot 10^{-3} s^{-1}$ per CIC and in an upset rate of $< 2.7 \cdot 10^{-3} s^{-1}$ per PS module.

	Unit	MPA	SSA	PS module
Stub data	Per second [s^{-1}]	$1.32 \cdot 10^{-03}$	$4.58 \cdot 10^{-04}$	$< 2.5 \cdot 10^{-03}$
	Per event [BX^{-1}]	$3.31 \cdot 10^{-11}$	$1.14 \cdot 10^{-11}$	$< 6.3 \cdot 10^{-11}$
	Total*	$1.06 \cdot 10^{+05}$	$3.66 \cdot 10^{+04}$	$< 2.0 \cdot 10^{+05}$
L1 data	Per second s^{-1}	$1.59 \cdot 10^{-03}$	$2.32 \cdot 10^{-04}$	$< 2.7 \cdot 10^{-03}$
	Per event BX^{-1}	$3.99 \cdot 10^{-11}$	$5.79 \cdot 10^{-12}$	$< 6.8 \cdot 10^{-11}$
	Total*	$1.28 \cdot 10^{+05}$	$1.85 \cdot 10^{+04}$	$< 2.2 \cdot 10^{+05}$

* integrated over the total time necessary to reach an integrated luminosity of $4 \cdot 10^3 fb^{-1}$ corresponding to $8 \cdot 10^7$ s.

Figure 5.42. Maximum error rates due to SEU expected at the PS module output for the CMS outer-tracker particle spectrum and fluxes, for a module located at $z = 265$ cm, $r = 21$ cm and for an instantaneous luminosity of $5 \cdot 10^4 \mu b^{-1} s^{-1}$.

6 Summary and conclusions

Particle tracking detector for high energy physics needs a new readout technique to cope with the increase of collision rate foreseen for the High Luminosity LHC upgrade. In particular, the selection of interesting physics events at the first trigger stage becomes extremely challenging at high luminosity, not only because of the rate increase, but also because the selection algorithms become inefficient in high pileup conditions. A substantial increase of latency and trigger rate provides an improvement that is not sufficient to preserve the tracking performance of the current system. A possible solution consists of using tracking information for the event selection. This technique will allow to provide more accurate measurements of new particles and enable the observation of rare processes that occur below the current sensitivity level.

Given a limited bandwidth, the use of tracking information for the event selection implies that the tracker has to send out self-selected information for every event. This is the reason why front-end electronics need to perform a local data reduction. This functionality relies on the capability of continuous particle discrimination on-chip based on transverse momentum. This novel concept requires the front-end electronics to include the intelligence for discriminating particles. The capability to compute higher level information directly in the detector readout ASICs enables the possibility of local rejection of signals related to particles which are unnecessary for the trigger system and the offline analysis reconstruction. This will consequently reduce the required bandwidth of more than one order of magnitude.

The PS module, the detector unit that implement this concept, is composed of two closely spaced silicon sensors in a strong magnetic field providing sufficient sensitivity to measure particles transverse momentum over the small sensor separation. Such a module can be constructed using a pixel layer and a strip layer sensor. This solution combines the resolution of the pixels with the lower power density of the strips.

Two different readout ASICs, SSA and MPA, allow to readout the sensors and perform the on-detector particle discrimination based on the transverse momentum. This feature, introduced for the first time in an HEP readout ASIC, allows to drastically reduce the readout bandwidth, increase the tracker event reconstruction efficiency in the high luminosity and enable additional physics analysis possibilities.

Several architectures for particle tracking have been investigated using Monte Carlo simulations physics events, to identify the implementation that minimize power consumption and bandwidth requirements. For this purpose, a system-level simulation framework was developed to study and optimize the system architecture and to assist and verify the design of the multiple ASICs composing it. The chosen architecture reaches a particle selection efficiency of > 98% while providing a data compression from $\sim 30\,\mathrm{Gb}\cdot\mathrm{s}^{-1}\mathrm{cm}^{-2}$ to $0.7\,\mathrm{Gb}\cdot\mathrm{s}^{-1}\mathrm{cm}^{-2}$.

Two full-size and full-functionalities prototype, called MPA and SSA, have been designed, produced and tested. These two readout front-end ASICs perform pixel-strip sensors binary readout, full-event storage with triggered readout and continuous data selection with trigger-less readout. The very low power requirement of $< 100\,mW/\mathrm{cm}^2$ drive the choice of a 65 nm CMOS technology. The complex environment foreseen in the CMS outer-tracker, represented by a high ionizing radiation dose up to 100 Mrad (1 MGy) and temperatures reaching the $-40°\mathrm{C}$, made necessary further studies on the technology and the digital library characterization.

The SSA ASIC comprises a low-noise front-end followed by double-threshold discrimination circuits to detect and distinguish normal incidence particles from highly ionizing particles. Particle hits are sorted in clusters which are filtered to reduce bandwidth and data processing. Encoded clusters are continuously transmitted for correlation with the pixel layer information, allowing for the on-detector transverse momentum discrimination. In parallel, a triggered readout with a programmable latency up to 12.8 µs at 40 MHz event rate, provides the entire event with a maximum trigger rate of 1 MHz.

To mitigate the effect of radiation related Single Event Effects (SEE), the ASICs implement a triple module redundancy technique. The control and configuration logic, including the system clock, have been triplicated, while a full TMR has been excluded due to the restricted power budget.

The SSA ASIC tests consisted of a functional verification of the digital circuitry and performance characterization of the analog front-end circuitry using embedded charge injection capacitor circuits. For this scope, a custom test-bench and control firmware was developed.

The SSA front-end characterization with internal capacitance pulse injection matched simulations closely, with a strip threshold spread of 55 e^- r.m.s. after equalization, an equivalent electron noise of 330 e^- r.m.s., and a peaking time of 19 ns. The power consumption is lower than 60 mW per chip and fullfil the very strict CMS Tracker requirements.

The shift of the parameters with a total ionizing dose up to 200 Mrad, evaluated during a dedicated X-ray test campaign, are within the expected ranges and can be therefore compensated by the internal calibration circuit.

In addition, heavy ion-based Single Event Upset experiment proved SEU tolerance up to a effective LET of $\sim 70\,\mathrm{MeV \cdot mg^{-1}cm^{-2}}$. Finally, a data error rate evaluation provides a SEU related data error probability lower than $5 \cdot 10^{-11}$.

According to the current planning, the installation of the Phase-2 outer-tracker and Pixel Detector is expected in late 2024. The final SSA ASIC will enter in production by middle 2020, enabling the finalization of the hybrid circuits, module assembly and system testing. A period of about three years is allocated for module production and system test up to the commission of the detector prior to installation in CMS.

Bibliography

References to the author's publications

[1] A. Caratelli, S. Scarfi', D. Ceresa, J. T. De Clercq, M. Haranko, J. Kaplon, K. Kloukinas, and Y. Leblebici, "Characterization of the first prototype of the ilicon-Strip readout ASIC (SSA) for the CMS Outer-Tracker phase-2 upgrade", *PoS*, vol. TWEPP-18, 2019. [Online]. Available: http://cds.cern.ch/record/2650963.

[2] A. Caratelli, D. Ceresa, J. Kaplon, K. Kloukinas, Y. Leblebici, J. Murdzek, and S. Scarfi, "Short-Strip ASIC (SSA): A 65nm silicon-strip readout ASIC for the Pixel-Strip (PS) module of the CMS Outer Tracker detector upgrade at HL-LHC", *PoS*, vol. TWEPP-17, 031. 5 p, 2018. DOI: 10.22323/1.313.0031.

[3] D. Ceresa, A. Caratelli, J. T. De Clercq, D. Giovinazzo, M. Haranko, J. Kaplon, K. Kloukinas, J. Murdzek, and S. Scarfi', "Characterization of the MPA prototype, a 65 nm pixel readout ASIC with on-chip quick transverse momentum discrimination capabilities", *PoS*, vol. TWEPP-18, Oct. 2018. [Online]. Available: http://cds.cern.ch/record/2658203.

[4] D. Ceresa, A. Caratelli, J. Kaplon, K. Kloukinas, J. Murdzek, and S. Scarfi, "Design and simulation of a 65 nm Macro-Pixel Readout ASIC (MPA) for the Pixel-Strip (PS) module of the CMS Outer Tracker detector at the HL-LHC", *PoS*, vol. TWEPP-17, 032. 5 p, 2017. DOI: 10.22323/1.313.0032.

[5] A. Caratelli, S. Scarfi, D. Ceresa, K. Kloukinas, and Y. Leblebici, "System level simulation framework for the asics development of a novel particle physics detector", pp. 49–52, 2018. DOI: 10.1109/PRIME.2018.8430367.

[6] A. Caratelli, D. Ceresa, J. Kaplon, K. Kloukinas, and S. Scarfi, "Readout architecture for the Pixel-Strip module of the CMS Outer Tracker Phase-2 upgrade", *PoS*, vol. Vertex2016, p. 066, 2017. DOI: 10.22323/1.287.0066.

[7] A. Caratelli, S. Scarfi', D. Ceresa, J. T. De Clercq, M. Haranko, J. Kaplon, K. Kloukinas, and Y. Leblebici, "Low-power SEE hardening techniques and error rate evaluation in 65nm readout ASICs", *Submitted for PoS*, vol. TWEPP-19, 2019.

[8] D. Ceresa, J. Kaplon, A. Caratelli, R. Francisco, K. Kloukinas, and A. Marchioro, "A 65 nm pixel readout ASIC with quick transverse momentum discrimination capabilities for the CMS tracker at HL-LHC", *Journal of Instrumentation*, vol.

11, no. 01, pp. C01054–C01054, Jan. 2016. DOI: 10.1088/1748-0221/11/01/c01054.

[9] CMS tracker collaboration *et al.*, "The Phase-2 Upgrade of the CMS Tracker", CERN, Geneva, Tech. Rep. CERN-LHCC-2017-009. CMS-TDR-014, Jun. 2017. [Online]. Available: https://cds.cern.ch/record/2272264.

[10] A. Caratelli, "Design of a radiation tolerant control ASIC for high energy physics experiments", *Master Thesis*, 2014. [Online]. Available: https://etd.adm.unipi.it/t/etd-08182014-164101/.

[11] A. Caratelli, S. Bonacini, K. Kloukinas, A. Marchioro, P. Moreira, R. D. Oliveira, and C. Paillard, "The GBT-SCA, a radiation tolerant ASIC for detector control and monitoring applications in HEP experiments", *Journal of Instrumentation*, vol. 10, no. 03, pp. C03034–C03034, Mar. 2015. DOI: 10.1088/1748-0221/10/03/c03034.

[12] S. Scarfi', A. Caratelli, L. Caponetto, D. Ceresa, G. C. Galbit, K. Kloukinas, Y. Leblebici, B. Nodari, and S. Viret, "A System-Verilog Verification Environment for the CIC Data Concentrator ASIC of the CMS Outer Tracker Phase-2 Upgrades", *PoS*, vol. TWEPP-18, 2019. [Online]. Available: http://cds.cern.ch/record/2644445.

[13] A. Caratelli, D. Ceresa, J. Kaplon, K. Kloukinas, Y. Leblebici, J. Murdzek, and S. Scarfi, "MPA: Design and implementation of a pixel readout ASIC, on a 65 nm technology, featuring on-chip real time particle discrimination.", *Submitted for Journal of Instrumentation*, 2019.

[14] A. Caratelli, D. Ceresa, J. Kaplon, K. Kloukinas, Y. Leblebici, J. Murdzek, and S. Scarfi, "SSA: design and implementation of a strip sensor readout ASIC for on-detector particle discrimination", *Submitted for Journal of Instrumentation*, 2019.

[15] CMS collaboration *et al.*, "Technical Proposal for the Phase-II Upgrade of the CMS Detector", Geneva, Tech. Rep. CERN-LHCC-2015-010. LHCC-P-008. CMS-TDR-15-02, Jun. 2015. [Online]. Available: https://cds.cern.ch/record/2020886.

[16] A. Caratelli, K. Kloukinas, T. Poikela, and A. Fioriti, *CERN IC Technologies and design support*. [Online]. Available: https://espace.cern.ch/asics-support/ (visited on 05/01/2019).

[17] J. M. Mendez, S. Baron, A. Caratelli, and P. V. Leitao, "New slow-control FPGA IP for GBT based system and status update of the GBT-FPGA project", *PoS*, vol. TWEPP-17, 083. 5 p, 2018. DOI: 10.22323/1.313.0083.

[18] W. Adam, T. Bergauer, E. Brondolin, *et al.*, "P-type silicon strip sensors for the new CMS tracker at HL-LHC", *Journal of Instrumentation*, vol. 12, no. 06, P06018–P06018, Jun. 2017. DOI: 10.1088/1748-0221/12/06/p06018.

[19] W. Adam, T. Bergauer, E. Brondolin, *et al.*, "Characterisation of irradiated thin silicon sensors for the CMS phase II pixel upgrade", *The European Physical Journal C*, vol. 77, no. 8, p. 567, 2017. DOI: 10.1140/epjc/s10052-017-5115-z.

[20] A. M. Sirunyan, W. Adam, E. Asilar, T. Bergauer, *et al.*, "Mechanical stability of the cms strip tracker measured with a laser alignment system", *Journal of Instrumentation*, vol. 12, 2017. DOI: 10.1088/1748-0221/12/04/P04023.

[21] A. M. Sirunyan *et al.*, "Search for Higgs and Z boson decays to J/ψ or Υ pairs in proton-proton collisions at $\sqrt{s}$ = 13 TeV", 2019. arXiv: 1905.10408 [hep-ex].

[22] A. Sirunyan, A. Tumasyan, W. Adam, *et al.*, "Precision measurement of the structure of the CMS inner tracking system using nuclear interactions", *Journal of Instrumentation*, vol. 13, no. 10, P10034–P10034, Oct. 2018. DOI: 10.1088/1748-0221/13/10/p10034.

References

[23] S. J. Duclos, "Scintillator phosphors for medical imaging", *Interface-Electrochemical Society*, vol. 7, no. 2, pp. 34–39, 1998.

[24] N. D. Gupta and S. Ghosh, "A report on the wilson cloud chamber and its applications in physics", *Reviews of Modern Physics*, vol. 18, no. 2, p. 225, 1946. DOI: 10.1103/revmodphys.18.225.

[25] C. D. Anderson, "The positive electron", *Physical Review*, vol. 43, no. 6, p. 491, 1933. DOI: doi.org/10.1103/physrev.43.491.

[26] R. H. Dalitz, "Kaon physics—the first 50+ years", *Kaon Physics*, p. 5, 2001. DOI: doi.org/10.1007/978-3-642-84741-7_7.

[27] D. A. Glaser, "Some effects of ionizing radiation on the formation of bubbles in liquids", *Physical Review*, vol. 87, no. 4, p. 665, 1952. DOI: doi.org/10.1103/physrev.87.665.

[28] A. Pinkard, *Invention and history of the bubble chamber*, Jul. 2006. [Online]. Available: https://www2.lbl.gov/Publications/Currents/Archive/Jul-21-2006.html.

[29] F. Hasert, S. Kabe, W. Krenz, J. Von Krogh, D. Lanske, J. Morfin, K. Schultze, H. Weerts, G. Bertrand-Coremans, J. Sacton, *et al.*, "Observation of neutrino-like interactions without muon or electron in the gargamelle neutrino experiment", *Nuclear Physics B*, vol. 73, no. 1, pp. 1–22, 1974. DOI: 10.1016/0550-3213(74)90038-8.

[30] H. Wenninger, "In the tracks of the bubble chamber", *CERN Cour.*, vol. 44, pp. 26–29, 2004. [Online]. Available: http://inspirehep.net/record/658966/.

[31] *Conference on the bubble chamber and its contributions to particle physics*, 1994. [Online]. Available: https://cds.cern.ch/record/232652.

[32] H. Geiger and W. Mlerler, "Elektronenz a tube for measuring blackness a th", *Science*, vol. 16, no. 31, pp. 617–618, 1928.

[33] A. Wright, *The photomultiplier handbook*. Oxford University Press, 2017. DOI: 10.1093/oso/9780199565092.001.0001.

[34] F. Sauli, "Principles of operation of multiwire proportional and drift chambers", Cern, Tech. Rep., 1977. DOI: 10.1142/9789814355988_0002.

[35] R. C. Fernow *et al.*, *Introduction to experimental particle physics*. Cambridge university press, 1989. DOI: 10.1017/cbo9780511622588.002.

[36] M. Hauschild, *History of particle detectors*, May 2018. [Online]. Available: https://indico.cern.ch/event/43007/contributions/1065007/.

[37] H. Aihara, M. Alston-Garnjost, D. Badtke, J. Bakken, A. Barbaro-Galtieri, A. Barnes, B. Barnett, B. Blumenfeld, A. Bross, C. Buchanan, *et al.*, "Spatial resolution of the pep-4 time projection chamber", *IEEE Transactions on Nuclear Science*, vol. 30, no. 1, pp. 76–81, 1983. DOI: 10.1109/TNS.1983.4332223.

[38] Y. Giomataris, P. Rebourgeard, J. P. Robert, and G. Charpak, "Micromegas: a high-granularity position-sensitive gaseous detector for high particle-flux environments", *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 376, no. 1, pp. 29–35, 1996. DOI: 10.1016/0168-9002(96)00175-1.

[39] F. Sauli, "Gem: a new concept for electron amplification in gas detectors", *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 386, no. 2-3, pp. 531–534, 1997. DOI: 10.1016/s0168-9002(96)01172-2.

[40] P. Abbon, E. Albrecht, V. Y. Alexakhin, Y. Alexandrov, G. Alexeev, M. Alekseev, A. Amoroso, H. Angerer, V. Anosov, B. Badełek, *et al.*, "The compass experiment at cern", *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 577, no. 3, pp. 455–518, 2007. DOI: 10.1063/1.53682.

[41] C. K. Transfer, *A versatile gas detector*, 2017. [Online]. Available: https://kt.cern/success-stories/versatile-gas-detector.

[42] S. Amendolia, G. Batignani, F. Bedeschi, E. Bertolucci, L. Bosisio, C. Bradaschia, M. Budinich, F. Fidecaro, L. Foà, E. Focardi, *et al.*, "A multi-electrode silicon detector for high energy experiments", *Nuclear Instruments and Methods*, vol. 176, no. 3, pp. 457–460, 1980. DOI: 10.1016/0029-554X(80)90368-7.

[43] G. Arnison, A. Astbury, B. Aubert, C. Bacci, G. Bauer, A. Bezaguet, R. Böck, T. Bowcock, M. Calvetti, P. Catz, *et al.*, "Experimental observation of lepton pairs of invariant mass around 95 gev/c2 at the cern sps collider", *Physics Letters B*, vol. 126, no. 5, pp. 398–410, 1983. DOI: 10.1016/0370-2693(83)90188-0.

[44] E. Belau, J. Kemmer, R. Klanner, U. Kötz, G. Lutz, W. Männer, E. Neugebauer, H. Seebrunner, and A. Wylie, "Silicon detectors with 5 μm spatial resolution for high energy particles", *Nuclear Instruments and Methods in Physics Research*, vol. 217, pp. 224–228, 1983. DOI: 10.1016/0167-5087(83)90138-2.

[45] M. Turala, "Silicon tracking detectors - historical overview", *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 541, no. 1-2, pp. 1–14, 2005. DOI: 10.1016/j.nima.2005.01.032.

[46] J. Krige, *History of cern, iii*. Elsevier, 1996.

[47] CERN Collaboration, *The CERN member states*, 2018. [Online]. Available: https://home.cern/about/who-we-are/our-governance/member-states (visited on 2019).

[48] O. Bruning, H. Burkhardt, and S. Myers, "The Large Hadron Collider", *Prog. Part. Nucl. Phys.*, vol. 67, pp. 705–734, 2012. DOI: 10.1016/j.ppnp.2012.03.001.

[49] G. Aad, T. Abajyan, B. Abbott, J. Abdallah, S. A. Khalek, A. A. Abdelalim, O. Abdinov, R. Aben, B. Abi, M. Abolins, *et al.*, "Observation of a new particle in the search for the standard model higgs boson with the atlas detector at the lhc", *Physics Letters B*, vol. 716, no. 1, pp. 1–29, 2012. DOI: 10.1016/j.physletb.2012.08.020.

[50] P. W. Higgs, "Broken symmetries and the masses of gauge bosons", *Physical Review Letters*, vol. 13, no. 16, p. 508, 1964. DOI: 10.1103/PhysRevLett.13.508.

[51] F. Englert and R. Brout, "Broken symmetry and the mass of gauge vector mesons", *Physical Review Letters*, vol. 13, no. 9, p. 321, 1964. DOI: 10.1103/PhysRevLett.13.321.

[52] CMS collaboration *et al.*, "The cms experiment at the cern lhc", *Jinst*, vol. 3, S08004, 2008. DOI: 10.1007/978-88-7642-482-3_2.

[53] G. Aad, J. Butterworth, J. Thion, U. Bratzler, P. Ratoff, R. Nickerson, J. Seixas, I. Grabowska-Bold, F. Meisel, S. Lokwitz, *et al.*, "The atlas experiment at the cern large hadron collider", *Jinst*, vol. 3, S08003, 2008. DOI: 10.1088/1748-0221/3/08/S08003.

[54] T. L. W. G. for Higgs, A. Collaboration, D. Collaboration, L. Collaboration, O. Collaboration, *et al.*, "Search for the standard model higgs boson at LEP", *Physics Letters B*, vol. 565, pp. 61–75, 2003. DOI: 10.1063/1.43422.

[55] A. A. Alves Jr, L. Andrade Filho, A. Barbosa, I. Bediaga, G. Cernicchiaro, G. Guerrer, H. Lima Jr, A. Machado, J. Magnin, F. Marujo, *et al.*, "The lhcb detector at the lhc", *Journal of instrumentation*, vol. 3, no. 08, S08005, 2008. DOI: 10.1088/1748-0221/3/08/S08005.

[56] K. Aamodt, A. A. Quintana, R. Achenbach, S. Acounis, D. Adamová, C. Adler, M. Aggarwal, F. Agnese, G. A. Rinella, Z. Ahammed, *et al.*, "The alice experiment at the cern lhc", *Journal of Instrumentation*, vol. 3, no. 08, S08002, 2008. DOI: 10.1016/b978-0-444-51343-4.50019-3.

[57] L. Evans and P. Bryant, "LHC Machine", *JINST*, vol. 3, S08001, 2008. DOI: 10.1088/1748-0221/3/08/S08001.

[58] O. S. Brüning, P. Collier, P. Lebrun, S. Myers, R. Ostojic, J. Poole, and P. Proudlock, *LHC Design Report*, ser. CERN Yellow Reports: Monographs. Geneva: CERN, 2004. [Online]. Available: http://cds.cern.ch/record/782076.

[59] S. Ulmer, "Base annual report 2018", Tech. Rep., 2019. DOI: http://cds.cern.ch/record/2654098.

[60] J. Haffner, "The CERN accelerator complex. Complexe des accélérateurs du CERN", Oct. 2013, General Photo. [Online]. Available: https://cds.cern.ch/record/1621894.

[61] S. P. Summers, "Application of FPGAs to Triggering in High Energy Physics", PhD thesis, Imperial Coll., London, 2018. [Online]. Available: http://cds.cern.ch/record/2647951.

[62] G. Apollinari, I. Béjar Alonso, O. Brüning, P. Fessia, M. Lamont, L. Rossi, and L. Tavian, "High-Luminosity Large Hadron Collider (HL-LHC)", *CERN Yellow Rep. Monogr.*, vol. 4, pp. 1–516, 2017. DOI: 10.23731/CYRM-2017-004.

[63] G. Apollinari, I. Béjar Alonso, O. Brüning, M. Lamont, and L. Rossi, *High-Luminosity Large Hadron Collider (HL-LHC): Preliminary Design Report*, ser. CERN Yellow Reports: Monographs. Geneva: CERN, 2015. [Online]. Available: http://cds.cern.ch/record/2116337.

[64] B. Schmidt, "The high-luminosity upgrade of the lhc: physics and technology challenges for the accelerator and the experiments", in *Journal of Physics: Conference Series*, IOP Publishing, vol. 706, 2016, p. 022 002. DOI: 10.1088/1742-6596/706/2/022002.

[65] D. Braga, "Development of the readout electronics for the high luminosity upgrade of the cms outer strip tracker", PhD thesis, Imperial College London, 2016. [Online]. Available: https://ethos.bl.uk/OrderDetails.do?uin=uk.bl.ethos.689133.

[66] M. Krammer, "The update of the european strategy for particle physics", *Physica Scripta*, vol. 2013, no. T158, p. 014 019, 2013. DOI: 10.1088/0031-8949/2013/t158/014019.

[67] CMS collaboration *et al.*, "Technical proposal for the phase-II upgrade of the CMS detector", *CERN, CERN-LHCC-2015-010. LHCC-P-008*, 2015.

[68] T. Sakuma and T. McCauley, "Detector and event visualization with SketchUp at the CMS experiment", *Journal of Physics: Conference Series*, vol. 513, no. 2, p. 022 032, Jun. 2014. DOI: 10.1088/1742-6596/513/2/022032. [Online]. Available: https://doi.org/10.1088%5C%2F1742-6596%5C%2F513%5C%2F2%5C%2F022032.

[69] CMS collaboration *et al.*, "Particle-flow event reconstruction in cms and performance for jets, taus and met", CMS-PAS-PFT-09-001, Tech. Rep., 2009. DOI: https://cds.cern.ch/record/1194487?ln=en.

[70] D. Bertolini, P. Harris, M. Low, and N. Tran, "Pileup per particle identification", *Journal of High Energy Physics*, vol. 2014, no. 10, p. 59, 2014. DOI: 10.1007/jhep10(2014)059.

[71] V. Karimäki, "The cms tracker system project: technical design report", CMS-TDR-005, Tech. Rep., 1997.

[72] K. Kloukinas, "Kchip: a radiation tolerant digital data concentrator chip for the cms preshower detector", 2003. [Online]. Available: https://proj-kchip.web.cern.ch/proj-Kchip/preshower/doc/Kloukinas-1.pdf.

[73] M. M. Angarano, C. T. Collaboration, *et al.*, "The silicon strip tracker for cms", *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 501, no. 1, pp. 93–99, 2003. DOI: 10.1016/S0168-9002(02)02016-8.

[74] K. Klein, "The cms silicon strip tracker-overview and status", *ArXiv preprint physics/0610259*, 2006. DOI: 10.22323/1.021.0378.

[75] M. French, L. Jones, Q. Morrissey, A. Neviani, R. Turchetta, J. Fulcher, G. Hall, E. Noah, M. Raymond, G. Cervelli, *et al.*, "Design and results from the apv25, a deep sub-micron cmos front-end chip for the cms tracker", *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 466, no. 2, pp. 359–365, 2001. DOI: 10.1016/s0168-9002(01)00589-7.

[76] D. Ceresa, "Electronic systems for intelligent particle tracking in the high energy physics field", PhD thesis, Politecnico di Torino, 2016.

[77] S. Mersi, CMS Collaboration, *et al.*, "Phase-2 upgrade of the cms tracker", *Nuclear and particle physics proceedings*, vol. 273, pp. 1034–1041, 2016. DOI: 10.1016/j.nuclphysbps.2015.09.162.

[78] T. Böhlen, F. Cerutti, M. Chin, A. Fassò, A. Ferrari, P. Ortega, A. Mairani, P. R. Sala, G. Smirnov, and V. Vlachoudis, "The FLUKA code: developments and challenges for high energy and medical applications", *Nuclear data sheets*, vol. 120, pp. 211–214, 2014. DOI: 10.1016/j.nds.2014.07.049.

[79] A. Ferrari, P. Sala, A. Fassò, and J. Ranft, "FLUKA: A multi-particle transport code", 2005. DOI: 10.2172/877507.

[80] M. Tanabashi, K. Hagiwara, K. Hikasa, K. Nakamura, Y. Sumino, F. Takahashi, J. Tanaka, K. Agashe, G. Aielli, C. Amsler, M. Antonelli, D. Asner, H. Baer, *et al.*, "Review of particle physics", English (US), *Physical Review D*, vol. 98, no. 3, Aug. 2018, ISSN: 2470-0010. DOI: 10.1103/PhysRevD.98.030001.

[81] S. Meroli, "Scaled cmos technology", 2002. [Online]. Available: http://meroli.web.cern.ch/.

[82] F. Hartmann, *Evolution of silicon sensor technology in particle physics*. Springer, 2009, vol. 43. DOI: 10.1007/978-3-319-64436-3.

[83] A. Peisert, "Silicon microstrip detector, instrumentation in high-energy physics", *World Scientific*, 1992. DOI: 10.1016/j.nima.2011.11.005.

[84] G. Lutz *et al.*, *Semiconductor radiation detectors*. Springer, 1999, vol. 40. DOI: 10.1007/978-3-540-71679-2.

[85] L. Rossi, P. Fischer, T. Rohe, and N. Wermes, *Pixel Detectors*. 2006. DOI: 10.1007/3-540-28333-1.

[86] E. Conti, P. Pangaud, P. Breugnon, M. Menichelli, G. De Robertis, S. Orfanelli, Z. Janoska, F. Licciulli, T. Hemperek, F. Fahim, *et al.*, "Development of a large pixel chip demonstrator in rd53 for atlas and cms upgrades", *PoS*, p. 005, 2017. DOI: 10.22323/1.313.0005.

[87] D. Hynds, "Silicon pixel R&D for the CLIC detector", *PoS*, vol. Vertex2016, no. CLICdp-Conf-2016-017, p. 049. 9, Dec. 2016. DOI: 10.22323/1.287.0049.

[88] C. Brönnimann, R. Baur, E. Eikenberry, S. Kohout, M. Lindner, B. Schmitt, and R. Horisberger, "A pixel read-out chip for the pilatus project", *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 465, no. 1, pp. 235–239, 2001. DOI: 10.1016/s0168-9002(01)00396-5.

[89] M. Campbell, E. Heijne, G. Meddeler, E. Pemigotti, and W. Snoeys, "Readout for a 64/spl times/64 pixel matrix with 15-bit single photon counting", in *1997 IEEE Nuclear Science Symposium Conference Record*, IEEE, vol. 1, 1997, pp. 189–191. DOI: 10.1109/nssmic.1997.672566.

[90] M. Lindner, L. Blanquart, P. Fischer, H. Krüger, and N. Wermes, "Medical x-ray imaging with energy windowing", *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 465, no. 1, pp. 229–234, 2001. DOI: 10.1016/S0168-9002(01)00395-3.

[91] D. W. Clark and L.-J. Weng, "Maximal and near-maximal shift register sequences: efficient event counters and easy discrete logarithms", *IEEE Transactions on Computers*, vol. 43, no. 5, pp. 560–568, 1994. DOI: 10.1109/12.280803.

[92] P. Delpierre, J. Berar, L. Blanquart, N. Boudet, P. Breugnon, B. Caillot, J. Clemens, C. Mouget, R. Potheau, and I. Valin, "Large surface x-ray pixel detector", *IEEE Transactions on Nuclear Science*, vol. 49, no. 4, pp. 1709–1711, 2002. DOI: 10.1109/nssmic.2001.1009701.

[93] L. Collaboration, "LHCb VELO Upgrade Technical Design Report", Tech. Rep. CERN-LHCC-2013-021. LHCB-TDR-013, Nov. 2013. [Online]. Available: http://cds.cern.ch/record/1624070.

[94] C. Patauner, A. Marchioro, S. Bonacini, A. U. Rehman, and W. Pribyl, "A lossless data compression system for a real-time application in hep data acquisition", *IEEE Transactions on Nuclear Science*, vol. 58, no. 4, pp. 1738–1744, 2011. DOI: 10.1109/rtc.2010.5750389.

[95] A. Kluge, G. A. Rinella, S. Bonacini, P. Jarron, J. Kaplon, M. Morel, M. Noy, L. Perktold, and K. Poltorak, "The tdcpix readout asic: a 75 ps resolution timing front-end for the na62 gigatracker hybrid pixel detector", *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 732, pp. 511–514, 2013. DOI: 10.1016/j.nima.2013.06.089.

[96] P. Valerio, R. Ballabriga, and M. Campbell, "Design of the 65 nm clicpix demonstrator chip", Nov. 2012. [Online]. Available: http://cds.cern.ch/record/1507691.

[97] X. Llopart, R. Ballabriga, M. Campbell, L. Tlustos, and W. Wong, "Timepix, a 65k programmable pixel readout chip for arrival time, energy and/or photon counting measurements", *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 581, no. 1-2, pp. 485–494, 2007. DOI: 10.1016/j.nima.2007.08.079.

[98] T. Poikela, M. De Gaspari, J. Plosila, T. Westerlund, R. Ballabriga, J. Buytaert, M. Campbell, X. Llopart, K. Wyllie, V. Gromov, *et al.*, "Velopix: the pixel asic for the lhcb upgrade", *Journal of Instrumentation*, vol. 10, no. 01, p. C01057, 2015. DOI: 10.1088/1748-0221/10/01/C01057.

[99] G. Mazza, D. Calvo, P. De Remigis, M. Mignone, J. Olave, A. Rivetti, R. Wheadon, and L. Zotti, "The topix v4 prototype for the triggerless readout of the panda silicon pixel detector", *Journal of Instrumentation*, vol. 10, no. 01, p. C01042, 2015. DOI: 10.1088/1748-0221/10/01/C01042.

[100] V. Khachatryan, D. Anderson, A. Apresyan, A. Bornheim, J. Bunn, Y. Chen, J. Duarte, A. Mott, H. Newman, C. Pena, *et al.*, "The cms trigger system", *Journal of Instrumentation*, vol. 12, no. 1, Art–No, 2017. DOI: 10.1088/1748-0221/12/01/P01020.

[101] R. Dinapoli, M. Campbell, E. Canatore, V. Cencelli, E. Heijne, P. Jarron, P. Lamanna, V. O'Shea, V. Quiquempoix, D. S. S. Bello, *et al.*, "A front-end for silicon pixel detectors in alice and lhcb", *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 461, no. 1-3, pp. 492–495, 2001. DOI: doi.org/10.1016/S0168-9002(00)01281-X.

[102] G. Aad, M. Ackers, F. Alberti, M. Aleppo, G. Alimonti, J. Alonso, E. Anderssen, A. Andreani, A. Andreazza, J. Arguin, *et al.*, "Atlas pixel detector electronics and sensors", *Journal of Instrumentation*, vol. 3, no. 07, P07007, 2008. DOI: 10.1088/1748-0221/3/07/P07007.

[103] F. Hügging, A. P. Collaboration, *et al.*, "Front-end electronics and integration of ATLAS pixel modules", *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 549, no. 1-3, pp. 157–164, 2005. DOI: 10.1016/j.nima.2005.04.045.

[104] M. Barbero, W. Bertl, G. Dietrich, A. Dorokhov, W. Erdmann, K. Gabathuler, C. Hörmann, R. Horisberger, H. C. Kästli, D. Kotlinski, *et al.*, "Design and test of the cms pixel readout chip", *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 517, no. 1-3, pp. 349–359, 2004. DOI: 10.1016/j.nima.2003.09.043.

[105] D. Hits and A. Starodumov, "The cms pixel readout chip for the phase 1 upgrade", *Journal of Instrumentation*, vol. 10, no. 05, p. C05029, 2015. DOI: 10.1088/1748-0221/10/05/C05029.

[106] M. Garcia-Sciveres, D. Arutinov, M. Barbero, R. Beccherle, S. Dube, D. Elledge, J. Fleury, D. Fougeron, F. Gensolen, D. Gnani, *et al.*, "The FE-I4 pixel readout integrated circuit", *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 636, no. 1, S155–S159, 2011. DOI: 10.1016/j.nima.2010.04.101.

[107] G. Borghello, "Ionizing radiation effects in nanoscale CMOS technologies exposed to ultra-high doses", PhD thesis, University of Udine, Dipartimento Politecnico di Ingegneria e Architettura, Udine, Italy, 2018.

[108] F. P. La Torre, "Study of induced radioactivity in proton accelerator facilities", Universität Bern, Tech. Rep., 2014. [Online]. Available: http://inspirehep.net/record/1296409/files/CERN-THESIS-2014-009.pdf.

[109] E. Benton and E. Benton, "Space radiation dosimetry in low-earth orbit and beyond", *Nuclear Instruments and Methods in Physics Research Section B: Beam Interactions with Materials and Atoms*, vol. 184, no. 1-2, pp. 255–294, 2001. DOI: 10.1016/S0168-583X(01)00748-0.

[110] J. Srour, C. J. Marshall, and P. W. Marshall, "Review of displacement damage effects in silicon devices", *IEEE Transactions on Nuclear Science*, vol. 50, no. 3, pp. 653–670, 2003. DOI: 10.1109/TNS.2003.813197.

[111] S. Bonacini, "Development of single-event upset hardened programmable logic devices in deep submicron cmos", Nov. 2007. [Online]. Available: http://inspirehep.net/record/774171.

[112] E. A. Burke, "Energy dependence of proton-induced displacement damage in silicon", *IEEE Transactions on Nuclear Science*, vol. 33, no. 6, pp. 1276–1281, Dec. 1986, ISSN: 0018-9499. DOI: 10.1109/TNS.1986.4334592.

[113] G. P. Summers, E. A. Burke, C. J. Dale, E. A. Wolicki, P. W. Marshall, and M. A. Gehlhausen, "Correlation of particle-induced displacement damage in silicon", *IEEE Transactions on Nuclear Science*, vol. 34, no. 6, pp. 1133–1139, Dec. 1987, ISSN: 0018-9499. DOI: 10.1109/TNS.1987.4337442.

[114] G. P. Summers, E. A. Burke, P. Shapiro, S. R. Messenger, and R. J. Walters, "Damage correlations in semiconductors exposed to gamma, electron and proton radiations", *IEEE Transactions on Nuclear Science*, vol. 40, no. 6, pp. 1372–1379, Dec. 1993, ISSN: 0018-9499. DOI: 10.1109/23.273529.

[115] I. Lazanu, S. Lazanu, U. Biggeri, E. Borchi, and M. Bruzzi, "Non-ionising energy loss of pions in thin silicon samples", *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 388, no. 3, pp. 370–374, 1997, Radiation Effects on Semiconductor Materials, Detectors and Devices, ISSN: 0168-9002. DOI: 10.1016/S0168-9002(96)01251-X.

[116] J. R. Srour and J. W. Palko, "Displacement damage effects in irradiated semiconductor devices", *IEEE Transactions on Nuclear Science*, vol. 60, no. 3, pp. 1740–1766, Jun. 2013, ISSN: 0018-9499. DOI: 10.1109/TNS.2013.2261316.

[117] C. J. Dale, P. W. Marshall, E. A. Burke, G. P. Summers, and E. A. Wolicki, "High energy electron induced displacement damage in silicon", *IEEE Transactions on Nuclear Science*, vol. 35, no. 6, pp. 1208–1214, Dec. 1988, ISSN: 0018-9499. DOI: 10.1109/23.25441.

[118] M. Huhtinen and P. Aarnio, "Pion induced displacement damage in silicon devices", *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 335, no. 3, pp. 580–582, 1993, ISSN: 0168-9002. DOI: 10.1016/0168-9002(93)91246-J.

[119] J. R. Srour and J. W. Palko, "A framework for understanding displacement damage mechanisms in irradiated silicon devices", *IEEE Transactions on Nuclear Science*, vol. 53, no. 6, pp. 3610–3620, Dec. 2006, ISSN: 0018-9499. DOI: 10.1109/TNS.2006.885796.

[120] S. R. Messenger, M. A. Xapsos, E. A. Burke, R. J. Walters, and G. P. Summers, "Proton displacement damage and ionizing dose for shielded devices in space", *IEEE Transactions on Nuclear Science*, vol. 44, no. 6, pp. 2169–2173, Dec. 1997, ISSN: 0018-9499. DOI: 10.1109/23.659032.

[121] G. P. Summers, S. R. Messenger, E. A. Burke, M. A. Xapsos, and R. J. Walters, "Low energy proton-induced displacement damage in shielded gaas solar cells in space", *Applied Physics Letters*, vol. 71, no. 6, pp. 832–834, 1997. DOI: 10.1063/1.119660.

[122] I. Jun, "Effects of secondary particles on the total dose and the displacement damage in space proton environments", *IEEE Transactions on Nuclear Science*, vol. 48, no. 1, pp. 162–175, Feb. 2001, ISSN: 0018-9499. DOI: 10.1109/23.907581.

[123] V. A. V. Lint, "The physics of radiation damage in particle detectors", *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 253, no. 3, pp. 453–459, 1987, ISSN: 0168-9002. DOI: 10.1016/0168-9002(87)90532-8.

[124] G. Lindström, M. Moll, and E. Fretwurst, "Radiation hardness of silicon detectors – a challenge from high-energy physics", *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 426, no. 1, pp. 1–15, 1999, ISSN: 0168-9002. DOI: 10.1016/S0168-9002(98)01462-4.

[125] F. A. Junga and G. M. Enslow, "Radiation effects in silicon solar cells", *IRE Transactions on Nuclear Science*, vol. 6, no. 2, pp. 49–53, Jun. 1959, ISSN: 0096-2015. DOI: 10.1109/TNS2.1959.4315679.

[126] W. Rosenzweig, H. K. Gummel, and F. M. Smits, "Solar cell degradation under 1-mev electron bombardment", *The Bell System Technical Journal*, vol. 42, no. 2, pp. 399–414, Mar. 1963, ISSN: 0005-8580. DOI: 10.1002/j.1538-7305.1963.tb00506.x.

[127] G. Xin, F. Zhan-zu, C. Xin-yu, Y. Sheng-sheng, and Z. Lei, "Performance evaluation and prediction of single-junction and triple-junction gaas solar cells induced by electron and proton irradiations", *IEEE Transactions on Nuclear Science*, vol. 61, no. 4, pp. 1838–1842, Aug. 2014, ISSN: 0018-9499. DOI: 10.1109/TNS.2014.2306991.

[128] C. Dale, P. Marshall, B. Cummings, L. Shamey, and A. Holland, "Displacement damage effects in mixed particle environments for shielded spacecraft ccds", *IEEE Transactions on Nuclear Science*, vol. 40, no. 6, pp. 1628–1637, Dec. 1993, ISSN: 0018-9499. DOI: 10.1109/23.273497.

[129] J. Bogaerts, B. Dierickx, G. Meynants, and D. Uwaerts, "Total dose and displacement damage effects in a radiation-hardened cmos aps", *IEEE Transactions on Electron Devices*, vol. 50, no. 1, pp. 84–90, Jan. 2003, ISSN: 0018-9383. DOI: 10.1109/TED.2002.807251.

[130] C. Virmontois, V. Goiffon, P. Magnan, S. Girard, C. Inguimbert, S. Petit, G. Rolland, and O. Saint-Pe, "Displacement damage effects due to neutron and proton irradiations on cmos image sensors manufactured in deep submicron technology", *IEEE Transactions on Nuclear Science*, vol. 57, no. 6, pp. 3101–3108, Dec. 2010, ISSN: 0018-9499. DOI: 10.1109/TNS.2010.2085448.

[131] F. Faccio, B. Allongue, G. Blanchot, C. Fuentes, S. Michelis, S. Orlandi, and R. Sorge, "Tid and displacement damage effects in vertical and lateral power mosfets for integrated dc-dc converters", in *2009 European Conference on Radiation and Its Effects on Components and Systems*, Sep. 2009, pp. 46–53. DOI: 10.1109/RADECS.2009.5994551.

[132] T.-P. Ma and P. V. Dressendorfer, *Ionizing radiation effects in mos devices and circuits*. John Wiley & Sons, 1989. DOI: 10.1148/radiology.174.3.886.

[133] J. Schwank, “Basic mechanisms of radiation effects in the natural space radiation environment”, Jun. 1994.

[134] P. V. Dressendorfer, “Basic mechanisms for the new millennium”, Sep. 1998. [Online]. Available: https://www.osti.gov/biblio/658465.

[135] T. R. Oldham, *Ionizing radiation effects in mos oxides*. World Scientific, 1999, vol. 3. DOI: 10.1142/3655.

[136] T. R. Oldham and F. McLean, “Total ionizing dose effects in MOS oxides and devices”, *IEEE transactions on nuclear science*, vol. 50, no. 3, pp. 483–499, 2003. DOI: 10.1109/tns.2003.812927.

[137] H. J. Barnaby, “Total-ionizing-dose effects in modern cmos technologies”, *IEEE Transactions on Nuclear Science*, vol. 53, no. 6, pp. 3103–3121, Dec. 2006, ISSN: 0018-9499. DOI: 10.1109/TNS.2006.885952.

[138] J. R. Schwank, M. R. Shaneyfelt, D. M. Fleetwood, J. A. Felix, P. E. Dodd, P. Paillet, and V. Ferlet-Cavrois, “Radiation effects in mos oxides”, *IEEE Transactions on Nuclear Science*, vol. 55, no. 4, pp. 1833–1853, Aug. 2008, ISSN: 0018-9499. DOI: 10.1109/TNS.2008.2001040.

[139] D. M. Fleetwood, “Total Ionizing Dose Effects in MOS and Low-Dose-Rate-Sensitive Linear-Bipolar Devices”, *IEEE Transactions on Nuclear Science*, vol. 60, no. 3, pp. 1706–1730, Jun. 2013, ISSN: 0018-9499. DOI: 10.1109/TNS.2013.2259260.

[140] N. Saks, M. Ancona, and J. Modolo, “Radiation effects in MOS capacitors with very thin oxides at 80 k”, *IEEE Transactions on Nuclear Science*, vol. 31, no. 6, pp. 1249–1255, 1984. DOI: 10.1109/tns.1984.4333491.

[141] J. M. Benedetto, H. E. Boesch, F. B. McLean, and J. P. Mize, “Hole removal in thin-gate mosfets by tunneling”, *IEEE Transactions on Nuclear Science*, vol. 32, no. 6, pp. 3916–3920, Dec. 1985, ISSN: 0018-9499. DOI: 10.1109/TNS.1985.4334043.

[142] N. S. Saks, M. G. Ancona, and J. A. Modolo, “Generation of interface states by ionizing radiation in very thin mos oxides”, *IEEE Transactions on Nuclear Science*, vol. 33, no. 6, pp. 1185–1190, Dec. 1986, ISSN: 0018-9499. DOI: 10.1109/TNS.1986.4334576.

[143] D. B. Brown and N. S. Saks, “Time dependence of radiation-induced interface trap formation in metal-oxide-semiconductor devices as a function of oxide thickness and applied field”, *Journal of Applied Physics*, vol. 70, no. 7, pp. 3734–3747, 1991. DOI: 10.1063/1.349226.

[144] D. M. Fleetwood, “Evolution of total ionizing dose effects in mos devices with moore’s law scaling”, *IEEE Transactions on Nuclear Science*, pp. 1–1, 2017, ISSN: 0018-9499. DOI: 10.1109/TNS.2017.2786140.

[145] R. C. Lacoe, J. V. Osborn, D. C. Mayer, S. Brown, and D. R. Hunt, “Total-dose radiation tolerance of a commercial 0.35 µm cmos process”, in *1998 IEEE Radiation Effects Data Workshop. NSREC 98. Workshop Record. Held in conjunction with IEEE Nuclear and Space Radiation Effects Conference (Cat. No.98TH8385)*, Jul. 1998, pp. 104–110. DOI: 10.1109/REDW.1998.731487.

[146] G. U. Youk, P. S. Khare, R. D. Schrimpf, L. W. Massengill, and K. F. Galloway, "Radiation-enhanced short channel effects due to multi-dimensional influence from charge at trench isolation oxides", *IEEE Transactions on Nuclear Science*, vol. 46, no. 6, pp. 1830–1835, Dec. 1999, ISSN: 0018-9499. DOI: 10.1109/23.819161.

[147] F. Faccio and G. Cervelli, "Radiation-induced edge effects in deep submicron CMOS transistors", *IEEE Transactions on Nuclear Science*, vol. 52, no. 6, pp. 2413–2420, 2005. DOI: 10.1109/tns.2005.860698.

[148] F. Faccio, G. Borghello, E. Lerario, D. M. Fleetwood, R. D. Schrimpf, H. Gong, E. X. Zhang, P. Wang, S. Michelis, S. Gerardin, A. Paccagnella, and S. Bonaldo, "Influence of LDD spacers and H+ transport on the total-ionizing-dose response of 65 nm MOSFETs irradiated to ultra-high doses", *IEEE Transactions on Nuclear Science*, vol. 65, no. 1, pp. 164–174, Jan. 2018, ISSN: 0018-9499. DOI: 10.1109/tns.2017.2760629.

[149] S. Diehl, A. Ochoa, P. Dressendorfer, R. Koga, and W. Kolasinski, "Error analysis and prevention of cosmic ion-induced soft errors in static CMOS RAMs", *IEEE transactions on nuclear science*, vol. 29, no. 6, pp. 2032–2039, 1982. DOI: 10.1109/tns.1982.4336491.

[150] S. Bonacini, F. Faccio, K. Kloukinas, and A. Marchioro, "An seu-robust configurable logic block for the implementation of a radiation-tolerant fpga", *IEEE Transactions on Nuclear Science*, vol. 53, no. 6, pp. 3408–3416, 2006. DOI: 10.1109/tns.2006.884097.

[151] A. Rácz and P. Sphicas, "Cms the tridas project: technical design report, volume 2: data acquisition and high-level trigger", CMS-TDR-006, Tech. Rep., 2002. [Online]. Available: http://cds.cern.ch/record/578006.

[152] V. Gori, "The cms high level trigger", in *International Journal of Modern Physics: Conference Series*, World Scientific, vol. 31, 2014, p. 1 460 297. DOI: 10.1142/S201019451460297X.

[153] M. Pesaresi, "Tracking trigger upgrade plans for CMS at SLHC", *PoS*, p. 047, 2010. DOI: 10.22323/1.113.0047.

[154] S. Mersi, D. Abbaneo, N. De Maio, and G. Hall, "CMS Tracker layout studies for HL-LHC", *Physics Procedia*, vol. 37, pp. 1070–1078, 2012. DOI: 10.1016/j.phpro.2012.03.729.

[155] S. Mersi, "CMS silicon tracker upgrade for HL-LHC", *PoS*, p. 030, 2011. [Online]. Available: http://cds.cern.ch/record/1462792.

[156] M. Pesaresi and G. Hall, "Simulating the performance of a pt tracking trigger for cms", *Journal of Instrumentation*, vol. 5, no. 08, p. C08003, 2010. DOI: 10.1088/1748-0221/5/08/C08003.

[157] N. Pozzobon, "Development of a Level 1 Track Trigger for the CMS experiment at the high-luminosity LHC", *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 732, pp. 151–155, 2013. DOI: 10.1016/j.nima.2013.06.010.

[158] M. Pesaresi, "Development of a new silicon tracker at cms for super-lhc", PhD thesis, Imperial Coll., London, 2010.

[159] A. Marchioro, "A hybrid module architecture for a prompt momentum discriminating tracker at SLHC", *PoS*, p. 037, 2011. DOI: 10.1088/1748-0221/7/09/C09001.

[160] A. Marchioro, "Architecture of a module with momentum discrimination for the cms tracker upgrade", *WIT 2010 Workshop on Intelligent Trackers*, p. 037, Feb. 2010.

[161] T. Eichhorn, "Silicon strip sensor simulations for the cms phase-ii tracker upgrade", in *Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC), 2012 IEEE*, IEEE, 2012, pp. 1664–1669. DOI: 10.1109/NSSMIC.2012.6551395.

[162] K.-H. Hoffmann, "Development of new sensor designs and investigations on radiation hard silicon strip sensors for CMS at the Large Hadron Collider during the high luminosity phase", Tech. Rep., 2013. DOI: http://inspirehep.net/record/1339777/.

[163] A. H. Van Roermund, A. Baschirotto, and M. Steyaert, *Nyquist AD converters, sensor interfaces, and robustness: advances in analog circuit design, 2012*. Springer Science & Business Media, 2012. DOI: 10.1007/978-1-4614-4587-6.

[164] CMS collaboration *et al.*, *CMS tracker layout repository*, 2016. [Online]. Available: http://cms-tklayout.web.cern.ch/cms-tklayout/layouts-work/cmssw-models/.

[165] A. Belloni, "Cms upgrade plans & potential", in *Fourth Annual Large Hadron Collider Physics*, SISSA Medialab, vol. 276, 2017, p. 043. DOI: 10.22323/1.276.0043.

[166] A. Dominguez, D. Abbaneo, K. Arndt, N. Bacchetta, A. Ball, E. Bartz, W. Bertl, G. M. Bilei, G. Bolla, H. W. K. Cheung, M. Chertok, S. Costa, N. Demaria, D. D. Vazquez, K. Ecklund, W. Erdmann, K. Gill, G. Hall, K. Harder, F. Hartmann, *et al.*, "CMS Technical Design Report for the Pixel Detector Upgrade", Tech. Rep. CERN-LHCC-2012-016. CMS-TDR-11, Sep. 2012. [Online]. Available: http://cds.cern.ch/record/1481838.

[167] G. Blanchot, D. Braga, A. Honma, M. Kovacs, and M. Raymond, "Hybrid circuit prototypes for the cms tracker upgrade front-end electronics", *Journal of Instrumentation*, vol. 8, no. 12, p. C12033, 2013. DOI: 10.1088/1748-0221/8/12/C12033.

[168] D. Braga, G. Hall, L. Jones, P. Murray, M. Pesaresi, M. Prydderch, and M. Raymond, "CBC2: a microstrip readout ASIC with coincidence logic for trigger primitives at HL-LHC", *Journal of Instrumentation*, vol. 7, no. 10, p. C10003, 2012. DOI: 10.1088/1748-0221/7/10/c10003.

[169] P. Moreira, "The LpGBT project status and overview", in *ACES*, 2016. [Online]. Available: https://indico.cern.ch/event/468486/.

[170] J. Troska, A. Kraxner, A. Brandon-Bravo, S. Detraz, C. Scarcella, C. Sigaud, C. Soos, F. Vasey, and L. Olanterä, "The VTRx+, an optical link module for data transmission at HL-LHC", *PoS*, p. 048, 2017. DOI: 10.22323/1.313.0048.

[171] F. Faccio, S. Michelis, S. Orlandi, G. Blanchot, C. Fuentes, S. Saggini, and F. Ongaro, "Development of custom radiation-tolerant dcdc converter asics", *Journal of Instrumentation*, vol. 5, no. 11, p. C11016, 2010. DOI: 10.1088/1748-0221/5/11/C11016.

[172] M. Kovacs, G. Blanchot, T. Gadek, A. Honma, and A. Koliatos, "HDI flexible front-end hybrid prototype for the PS module of the CMS tracker upgrade", *Journal of Instrumentation*, vol. 12, no. 02, pp. C02029–C02029, Feb. 2017. DOI: 10.1088/1748-0221/12/02/c02029.

[173] D. Contardo and J. Spalding, "CMS Phase 2 Upgrade: Preliminary Plan and Cost Estimate", Tech. Rep., 2013. [Online]. Available: http://cds.cern.ch/record/1605208/files/CERN-RRB-2013-124.pdf.

[174] A. Mussgiller, "Detector Modules for the CMS Phase II Outer Tracker", no. DESY-2014-03109, 2014. [Online]. Available: https://bib-pubdb1.desy.de/record/170990.

[175] S. Marconi, E. Conti, P. Placidi, A. Scorzoni, J. Christiansen, and T. Hemperek, "A systemverilog-uvm methodology for the design, simulation and verification of complex readout chips in high energy physics applications", in *Applications in Electronics Pervading Industry, Environment and Society*, A. De Gloria, Ed., Cham: Springer International Publishing, 2017, pp. 35–41, ISBN: 978-3-319-47913-2. DOI: 10.1007/978-3-319-47913-2_5.

[176] IEEE, "IEEE Standard for SystemVerilog–Unified Hardware Design, Specification, and Verification Language", *IEEE Std 1800-2017 (Revision of IEEE Std 1800-2012)*, pp. 1–1315, Feb. 2018. DOI: 10.1109/IEEESTD.2018.8299595.

[177] IEEE, "IEEE standard for universal verification methodology language manual", *IEEE Std 1800.2-2017*, pp. 1–472, May 2017. DOI: 10.1109/IEEESTD.2017.7932212.

[178] S. Agostinelli, J. Allison, K. Amako, J. Apostolakis, H. Araujo, Arce, *et al.*, "Geant4 - a simulation toolkit", *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 506, no. 3, pp. 250–303, 2003. DOI: 10.1016/S0168-9002(03)01368-8.

[179] G. Amadio, Ananya, J. Apostolakis, M. Bandieramonte, S. Behera, A. Bhattacharyya, R. Brun, P. Canal, F. Carminati, *et al.*, "GeantV alpha release", *Journal of Physics: Conference Series*, vol. 1085, p. 032 037, Sep. 2018. DOI: 10.1088/1742-6596/1085/3/032037.

[180] CMS collaboration *et al.*, *CMSSW Application Framework*, 2019. [Online]. Available: https://twiki.cern.ch/twiki/bin/view/CMSPublic/ (visited on 2019).

[181] CMS collaboration *et al.*, *OscarProducer: Geant4-based Detector Simulation Module*, 2009. [Online]. Available: https://twiki.cern.ch/twiki/bin/view/CMSPublic/SWGuideOscarProducer (visited on 2019).

[182] O. Shadura and F. Carminati, "Stochastic performance tuning of complex simulation applications using unsupervised machine learning", pp. 1–8, Dec. 2016. DOI: 10.1109/SSCI.2016.7850200.

[183] J. Yarba, *Oscarproducer: geant4-based detector simulation module*, Sep. 2009. [Online]. Available: https://twiki.cern.ch/twiki/bin/view/CMSPublic/SWGuideOscarProducer.

[184] O. Shadura, V. Vassilev, and B. P. Bockelman, "Continuous performance benchmarking framework for root", *ArXiv preprint arXiv:1812.03149*, 2018. [Online]. Available: https://arxiv.org/abs/1812.03149.

[185] O. Shadura, B. P. Bockelman, and V. Vassilev, "Extending root through modules", *ArXiv preprint arXiv:1812.03145*, 2018. [Online]. Available: https://arxiv.org/abs/1812.03145.

[186] O. Shadura and B. P. Bockelman, "Root i/o compression algorithms and their performance impact within run 3", *ArXiv preprint arXiv:1906.04624*, 2019. [Online]. Available: https://arxiv.org/abs/1906.04624.

[187] B. Bockelman, Z. Zhang, and O. Shadura, "Speeding hep analysis with root bulk i/o", *ArXiv preprint arXiv:1906.08169*, 2019. [Online]. Available: https://arxiv.org/abs/1906.08169.

[188] R. Brun and F. Rademakers, "Root-an object oriented data analysis framework", *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 389, no. 1-2, pp. 81–86, 1997. DOI: 10.1016/S0168-9002(97)00048-X.

[189] Y. Takahashi, V. Vassilev, O. Shadura, and R. Isemann, "Optimizing frameworks performance using c++ modules aware root", *ArXiv preprint arXiv:1812.03992*, 2018. [Online]. Available: https://arxiv.org/abs/1812.03992.

[190] S. Viret, *HLLHC Tuto 920*, 2016. [Online]. Available: https://sviret.web.cern.ch/sviret/Welcome.php?n=CMS.HLLHCTuto920 (visited on 2019).

[191] L. Caponetto, G. Galbit, B. Nodari, S. Scarfi, and S. Viret, "CIC1 technical specification", *CMS INTERNAL NOTE*, 2017. [Online]. Available: https://espace.cern.ch/Tracker-Upgrade/Electronics/CIC/Shared%5C%20Documents/Specifications/CIC_specs_v3.pdf.

[192] Cadence, "Incisive vManager User Guide - Product Version 15.20", in *ACES*, Feb. 2017. [Online]. Available: https://manualzz.com/doc/29859260/incisive-vmanager-user-guide.

[193] CMS collaboration *et al.*, *Public Figures from CMS Tracker TDR (TDR-17-001)*, 2017. [Online]. Available: https://twiki.cern.ch/twiki/bin/view/CMSPublic/TDR17001Preliminary (visited on 2019).

[194] S. Viret, "Data transmission efficiency of the phase II tracker front-end system for the tilted geometry", *CMS INTERNAL NOTE*, Jan. 2017.

[195] G. Hugo on behalf the CMS collaboration, *Tilted geometry for the phase II tracker*, 2016. [Online]. Available: http://ghugo.web.cern.ch/ghugo/ (visited on 2019).

[196] CMS collaboration *et al.*, "Underlying event tunes and double parton scattering", *CMS Physics Analysis Summary CMS-PAS-GEN-14-001*, 2014.

[197] R. Aggleton, L. Ardila-Perez, F. Ball, M. Balzer, G. Boudoul, J. Brooke, M. Caselle, L. Calligaris, D. Cieri, E. Clement, *et al.*, "An FPGA based track finder for the L1 trigger of the CMS experiment at the High Luminosity LHC", *Journal of Instrumentation*, vol. 12, no. 12, P12019, 2017.

[198] F. Palla, M. Pesaresi, and A. Ryd, "Track finding in CMS for the level-1 trigger at the HL-LHC", *Journal of Instrumentation*, vol. 11, no. 03, pp. C03011–C03011, Mar. 2016. DOI: 10.1088/1748-0221/11/03/c03011.

[199] A. Andreani, A. Andreazza, A. Annovi, M. Beretta, V. Bevacqua, G. Blazey, M. Bogdan, E. Bossini, A. Boveia, V. Cavaliere, F. Canelli, F. Cervigni, Y. Cheng, M. Citterio, F. Crescioli, M. Dell'Orso, *et al.*, "The fasttracker real time processor and its impact on muon isolation, tau and b-jet misc selections at atlas", *IEEE Transactions on Nuclear Science*, vol. 59, no. 2, pp. 348–357, Apr. 2012, ISSN: 0018-9499. DOI: 10.1109/TNS.2011.2179670.

[200] E. Brondolin, "Track reconstruction in the cms experiment for the high luminosity lhc", PhD thesis, TU Vienna.

[201] S. Viret, "Data transmission efficiency of the phase II tracker front-end system", *CMS INTERNAL NOTE*, Oct. 2014.

[202] B. Nodari, L. Caponetto, G. C. Galbit, S. Scarfi', and S. Viret, "A 65 nm Data Concentration ASIC for the CMS Outer Tracker Detector Upgrade at HL-LHC", no. CMS-CR-2018-278, Oct. 2018. [Online]. Available: http://cds.cern.ch/record/2650712.

[203] J. Kaplon, "Fast bipolar and cmos rad-hard front end electronics for silicon strip detectors", PhD thesis, CERN, 2004. [Online]. Available: http://cds.cern.ch/record/806282.

[204] H. Spieler, *Semiconductor detector systems*. Oxford university press, 2005, vol. 12. DOI: 10.1093/acprof:oso/9780198527848.001.0001.

[205] V. Re, M. Manghisoni, L. Ratti, V. Speziali, and G. Traversi, "Total ionizing dose effects on the noise performances of a 0.13/spl mu/m cmos technology", *IEEE transactions on nuclear science*, vol. 53, no. 3, pp. 1599–1606, 2006. DOI: 10.1109/tns.2006.871802.

[206] D. Abbaneo, *dE/dx flags in the SSA layers*, https://indico.cern.ch/event/522485/contributions/2145776/, 2016. (visited on 2019).

[207] G. Giudice and A. Romanino, "Erratum to:" split supersymmetry"[nucl. phys. b 699 (2004) 65]", *Nuclear Physics B*, vol. 706, pp. 487–487, 2005. DOI: doi.org/10.1016/j.nuclphysb.2004.11.048.

[208] X. C. Vidal, M. D'Onofrio, P. Fox, R. Torre, K. Ulmer, A. Aboubrahim, A. Albert, J. Alimena, B. Allanach, M. Altakach, *et al.*, "Beyond the Standard Model Physics at the HL-LHC and HE-LHC", *ArXiv preprint arXiv:1812.07831*, 2018. [Online]. Available: http://cds.cern.ch/record/2650173.

[209] N. Arkani-Hamed and S. Dimopoulos, "Supersymmetric unification without low energy supersymmetry and signatures for fine-tuning at the LHC", *Journal of High Energy Physics*, vol. 2005, no. 06, p. 073, 2005. DOI: 10.1088/1126-6708/2005/06/073.

[210] J. Chistiansen and M. Garcia-Sciveres, "RD Collaboration Proposal: Development of pixel readout integrated circuits for extreme rate and radiation", no. CERN-LHCC-2013-008. LHCC-P-006, Jun. 2013. [Online]. Available: http://cds.cern.ch/record/1553467.

[211] Opencores, "The WISHBONE System-on-Chip (SoC) Interconnect Architecture for Portable IP Cores", 2008. [Online]. Available: http://opencores.org/opencores/wishbone.

[212] LpGBT team, *The LpGBT Project*. [Online]. Available: https://espace.cern.ch/GBT-Project/LpGBT/.

[213] P. Fischer, G. Comes, and H. Krüger, "Mephisto–a 128-channel front end chip with real time data sparsification and multi-hit capability", *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 431, no. 1-2, pp. 134–140, 1999. DOI: 10.1016/s0168-9002(99)00262-4.

[214] D. Ceresa, A. Marchioro, K. Kloukinas, J. Kaplon, W. Bialas, V. Re, G. Traversi, L. Gaioni, and L. Ratti, "Macro Pixel ASIC (MPA): The readout ASIC for the pixel-strip (PS) module of the CMS outer tracker at HL-LHC", *Journal of Instrumentation*, vol. 9, no. 11, p. C11012, 2014. DOI: 10.1088/1748-0221/9/11/c11012.

[215] R. Brouns *et al.*, "Development of a radiation tolerant low power sram compiler", 2014.

[216] N. Semiconductors, "UM10204 I2C-bus specification and user manual", *Rev*, vol. 3, p. 19, 2014. [Online]. Available: https://www.nxp.com/docs/en/user-guide/UM10204.pdf.

[217] T. Vergine, M. De Matteis, S. Michelis, G. Traversi, F. De Canio, and A. Baschirotto, "A 65 nm rad-hard bandgap voltage ref. for lhc environment", *IEEE Transactions on Nuclear Science*, vol. 63, no. 3, pp. 1762–1767, Jun. 2016, ISSN: 0018-9499. DOI: 10.1109/TNS.2016.2550581.

[218] A. Baschirotto, P. Delizia, S. D'Amico, V. Chironi, G. Cocciolo, and M. De Matteis, "Low power analog design in scaled technologies", 2009. DOI: 10.5170/CERN-2009-006.103.

[219] H. Casier, "Technology and other limitations for analog design. Advanced CMOS", Analog IC Design MEAD course, EPFL, Tech. Rep., 2016. [Online]. Available: http://mead.ch/MEADNEW/.

[220] O. Rozeau, J. Jomaah, S. Haendler, J. Boussey, and F. Balestra, "SOI technologies overview for low-power low-voltage radio-frequency applications", *Analog Integrated Circuits and Signal Processing*, vol. 25, no. 2, pp. 93–114, 2000. DOI: 10.1023/A:1008376514991.

[221] J. Schwank, V. Ferlet-Cavrois, M. Shaneyfelt, P. Paillet, and P. Dodd, "Radiation effects in soi technologies", *IEEE Transactions on Nuclear Science*, vol. 50, no. 3, pp. 522–538, 2003. DOI: 10.1109/tns.2003.812930.

[222] J. Felix, J. Schwank, C. Cirba, R. Schrimpf, M. Shaneyfelt, D. Fleetwood, and P. Dodd, "Influence of total-dose radiation on the electrical characteristics of SOI MOSFETs", *Microelectronic Engineering*, vol. 72, no. 1-4, pp. 332–341, 2004. DOI: 10.1016/j.mee.2004.01.013.

[223] S. S. Rathod, A. Saxena, and S. Dasgupta, "Radiation effects in MOS-based devices and circuits: A review", *IETE Technical Review*, vol. 28, no. 6, pp. 451–469, 2011. DOI: 10.4103/0256-4602.90747.

[224] D. M. Fleetwood, P. S. Winokur, and J. R. Schwank, "Using laboratory x-ray and cobalt-60 irradiations to predict cmos device response in strategic and space environments", *IEEE Transactions on Nuclear Science*, vol. 35, no. 6, pp. 1497–1505, Dec. 1988, ISSN: 0018-9499. DOI: 10.1109/23.25487.

[225] S. C. Witczak, R. C. Lacoe, J. V. Osborn, J. M. Hutson, and S. C. Moss, "Dose-rate sensitivity of modern nmosfets", *IEEE Transactions on Nuclear Science*, vol. 52, no. 6, pp. 2602–2608, Dec. 2005, ISSN: 0018-9499. DOI: 10.1109/TNS.2005.860709.

[226] G. Borghello, F. Faccio, E. Lerario, S. Michelis, S. Kulis, D. M. Fleetwood, R. D. Schrimpf, S. Gerardin, A. Paccagnella, and S. Bonaldo, "Dose-rate sensitivity of 65-nm mosfets exposed to ultrahigh doses", *IEEE Transactions on Nuclear Science*, vol. 65, no. 8, pp. 1482–1487, Aug. 2018, ISSN: 0018-9499. DOI: 10.1109/TNS.2018.2828142.

[227] F. Faccio, G. Borghello, E. Lerario, D. M. Fleetwood, R. D. Schrimpf, H. Gong, E. X. Zhang, P. Wang, S. Michelis, S. Gerardin, *et al.*, "Influence of ldd spacers and h+ transport on the total-ionizing-dose response of 65-nm mosfets irradiated to ultrahigh doses", *IEEE Transactions on Nuclear Science*, vol. 65, no. 1, pp. 164–174, 2018. DOI: 10.1109/TNS.2017.2760629.

[228] L. Casas, D. Ceresa, S. Kulis, S. Miryala, J. Christiansen, R. Francisco, and D. Gnani, "Characterization of radiation effects in 65 nm digital circuits with the DRAD digital radiation test chip", *Journal of Instrumentation*, vol. 12, no. 02, p. C02039, 2017. DOI: 10.1088/1748-0221/12/02/c02039.

[229] F. Faccio, S. Michelis, D. Cornale, A. Paccagnella, and S. Gerardin, "Radiation-induced short channel (RISCE) and narrow channel (RINCE) effects in 65 and 130 nm MOSFETs", *IEEE Transactions on Nuclear Science*, vol. 62, no. 6, pp. 2933–2940, 2015. DOI: 10.1109/tns.2015.2492778.

[230] W. Snoeys, F. Faccio, M. Campbell, E. Cantatore, L. Casagrande, A. Cavagnoli, S. D. Liberto, F. Formenti, *et al.*, "Layout techniques to enhance the radiation tolerance of standard CMOS technologies demonstrated on a pixel detector readout chip", *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 439, no. 2, pp. 349–360, 2000, ISSN: 0168-9002. DOI: https://doi.org/10.1016/S0168-9002(99)00899-2.

[231] W. J. Snoeys, T. A. P. Gutierrez, and G. Anelli, "A new nmos layout structure for radiation tolerance", in *2001 IEEE Nuclear Science Symposium Conference Record (Cat. No.01CH37310)*, vol. 2, Nov. 2001, 822–826 vol.2. DOI: 10.1109/NSSMIC.2001.1009683.

[232] V. Re, L. Gaioni, M. Manghisoni, L. Ratti, V. Speziali, and G. Traversi, "Review of radiation effects leading to noise performance degradation in 100-nm scale microelectronic technologies", in *Nuclear Science Symposium Conference Record, 2008. NSS'08. IEEE*, IEEE, 2008, pp. 3086–3090. DOI: 10.1109/nssmic.2008.4775008.

[233] M. Bucher, A. Nikolaou, A. Papadopoulou, N. Makris, L. Chevas, G. Borghello, H. D. Koch, and F. Faccio, "Total ionizing dose effects on analog performance of 65 nm bulk cmos with enclosed-gate and standard layout", in *2018 IEEE International Conference on Microelectronic Test Structures (ICMTS)*, Mar. 2018, pp. 166–170. DOI: 10.1109/ICMTS.2018.8383790.

[234] Y. S. Chauhan, S. Venugopalan, M.-A. Chalkiadaki, M. A. U. Karim, H. Agarwal, S. Khandelwal, N. Paydavosi, J. P. Duarte, C. C. Enz, A. M. Niknejad, *et al.*, "BSIM6: Analog and RF compact model for bulk MOSFET", *IEEE Transactions on Electron Devices*, vol. 61, no. 2, pp. 234–244, 2014. DOI: 10.1109/ted.2013.2283084.

[235] A. Nikolaou, M. Bucher, N. Makris, A. Papadopoulou, L. Chevas, G. Borghello, H. D. Koch, K. Kloukinas, T. S. Poikela, and F. Faccio, "Extending a 65nm cmos process design kit for high total ionizing dose effects", in *2018 7th International Conference on Modern Circuits and Systems Technologies (MOCAST)*, May 2018, pp. 1–4. DOI: 10.1109/MOCAST.2018.8376561.

[236] D. Felici, S. Bertazzoni, S. Bonacini, A. Marchioro, P. Moreira, and M. Ottavi, "A 20 mw, 4.8 gbit/sec, seu robust serializer in 65nm for read-out of data from lhc experiments", *Journal of Instrumentation*, vol. 9, no. 01, p. C01004, 2014. DOI: 10.1088/1748-0221/9/01/c01004.

[237] S. Kulis, "Single Event Effects mitigation with TMRG tool", *Journal of Instrumentation*, vol. 12, no. 01, p. C01082, 2017. DOI: 10.1088/1748-0221/12/01/c01082.

[238] P. Hazucha, T. Karnik, S. Walstra, B. A. Bloechel, J. W. Tschanz, J. Maiz, K. Soumyanath, G. E. Dermer, S. Narendra, V. De, *et al.*, "Measurements and analysis of SER-tolerant latch in a 90-nm dual-V/sub T/CMOS process", *IEEE Journal of Solid-State Circuits*, vol. 39, no. 9, pp. 1536–1543, 2004. DOI: 10.1109/jssc.2004.831449.

[239] R. Velazco, T. Calin, M. Nicolaidis, S. Moss, S. LaLumondiere, V. Tran, and R. Koga, "SEU-hardened storage cell validation using a pulsed laser", *IEEE Transactions on Nuclear Science*, vol. 43, no. 6, pp. 2843–2848, 1996. DOI: 10.1109/23.556875.

[240] S. Miryala1, T. Hemperek, and M. Menouni, "Characterization of Soft Error Rate Against Memory Elements Spacing and Clock Skew in a Logic with Triple Modular Redundancy in a 65nm Process", *PoS*, vol. Twepp-17, 2018. [Online]. Available: https://pos.sissa.it/343/029/pdf.

[241] S. Bonacini, P. Valerio, R. Avramidou, R. Ballabriga, F. Faccio, K. Kloukinas, and A. Marchioro, "Characterization of a commercial 65 nm CMOS technology for SLHC applications", *Journal of Instrumentation*, vol. 7, no. 01, P01015–P01015, Jan. 2012. DOI: 10.1088/1748-0221/7/01/p01015.

[242] R. W. Hamming, "Error detecting and error correcting codes", *The Bell system technical journal*, vol. 29, no. 2, pp. 147–160, 1950. DOI: 10.1002/j.1538-7305.1950.tb00463.x.

[243] G. C. Clark Jr and J. B. Cain, *Error-correction coding for digital communications*. Springer Science & Business Media, 2013. DOI: 10.1007/978-1-4899-2174-1.

[244] CERN ASIC Support, "ESD Clamp datasheet", CERN Internal IP documentation library, Tech. Rep., 2018. [Online]. Available: https://espace.cern.ch/asics-support.

[245] Texas Instruments, "LVDS application and data handbook", *Literature Number: SLLD009*, 2002. DOI: 10.1016/b978-0-12-800629-0.00049-8.

[246] JEDEC Standard, "Scalable Low-Voltage Signaling for 400 mV (SLVS-400)", *JESD8-13, O ctober*, 2001. [Online]. Available: https://www.jedec.org/standards-documents/docs/jesd-8-13.

[247] G. Traversi, S. Bonacini, F. De Canio, L. Gaioni, K. Kloukinas, M. Manghisoni, L. Ratti, and V. Re, "Design of low-power, low-voltage, differential I/O links for High Energy Physics applications", *Journal of Instrumentation*, vol. 10, no. 01, p. C01055, 2015. DOI: 10.1088/1748-0221/10/01/c01055.

[248] I. Kremastiotis and CERN ASIC Support, "CERN IO-Pads, RadTol 1.2V CMOS pads in 65nm technology", CERN Internal IP documentation library, Tech. Rep., 2015. [Online]. Available: https://espace.cern.ch/asics-support.

[249] M. Graphics, *Calibre verification user's manual*, 2008. [Online]. Available: https://www.mentor.com/.

[250] L. Gaioni, RD53 Collaboration, *et al.*, "Test results and prospects for RD53A, a large scale 65 nm CMOS chip for pixel readout at the HL-LHC", *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, 2018. DOI: 10.1016/j.nima.2018.11.107.

[251] A. Caratelli, K. Kloukinas, T. Poikela, and A. Fioriti, *CERN IC Technologies and design support community forum*. [Online]. Available: https://asicsupport-community.web.cern.ch/ (visited on 05/01/2019).

[252] M. Pesaresi, M. B. Marin, G. Hall, M. Hansen, G. Iles, A. Rose, F. Vasey, and P. Vichoudis, "The FC7 AMC for generic DAQ & control applications in CMS", *Journal of Instrumentation*, vol. 10, no. 03, p. C03036, 2015. DOI: 10.1088/1748-0221/10/03/c03036.

[253] Xilinx, *7 Series FPGAs Data Sheet DS180 (v2.6)*, Feb. 2018. [Online]. Available: https://www.xilinx.com/ (visited on 2019).

[254] *FPGA Mezzanine Card (FMC) standard*. Fountain Hills, AZ: VITA, 2008, Approved in 2008, revised in 2010. [Online]. Available: https://cds.cern.ch/record/1172409.

[255] A. Canepa, Y. Gershtein, and P. Merkel, "OT Electronics: Technical Overview", Fermilab, Tech. Rep., Sep. 2017. [Online]. Available: https://indico.fnal.gov/ (visited on 2019).

[256] National Instruments, *PCI Express - An Overview of the PCI Express Standard*, Nov. 2014. [Online]. Available: http://www.ni.com/white-paper/3767/en/ (visited on 2019).

[257] L. Charles, J. De Clercq, M. Haranko, J. Luetic, and S. Mersi, "D19C User's and Developer's manual", CMS collaboration, Tech. Rep., Jul. 2018. [Online]. Available: https://gitlab.cern.ch/cms%5C_tk%5C_ph2/d19c-firmware/blob/master/doc/d19c%5C_manual.pdf (visited on 2019).

[258] C. G. Larrea, K. Harder, D. Newbold, D. Sankey, A. Rose, A. Thea, and T. Williams, "IPbus: a flexible ethernet-based control system for xTCA hardware", *Journal of Instrumentation*, vol. 10, no. 02, pp. C02019–C02019, Feb. 2015. DOI: 10.1088/1748-0221/10/02/c02019.

[259] M. A. Osherson, E. Bartz, E. Halkiadakis, Y. Gershtein, and B. Harrop, *2xSSA Module Status and Plans*, Feb. 2008.

[260] L. J. Palkuti and J. J. LePage, "X-Ray Wafer Probe for Total Dose Testing", *IEEE Transactions on Nuclear Science*, vol. 29, no. 6, pp. 1832–1837, Dec. 1982, ISSN: 0018-9499. DOI: 10.1109/TNS.1982.4336456.

[261] International Commission on Radiation Units and Measurements, "Fundamental quantities and units for Ionizing Radiation - Report 85", *Journal of the International Commission on Radiation Units and Measurements*, vol. 11, NP, 2011. DOI: 10.1093/jicru/ndr012.

[262] M. Huyse and R. Raabe, "Radioactive ion beam physics at the cyclotron research centre Louvain-la-Neuve", *Journal of Physics G: Nuclear and Particle Physics*, vol. 38, no. 2, p. 024 001, 2011. DOI: 10.1088/0954-3899/38/2/024001.

[263] W. R. Leo, *Techniques for nuclear and particle physics experiments: a how-to approach*. Springer Science & Business Media, 2012. DOI: 10.1007/978-3-642-57920-2.

[264] S. Meroli, "The cross section for silicon particle detector", 2012. [Online]. Available: http://meroli.web.cern.ch/.

[265] E. L. Petersen, J. C. Pickel, J. H. Adams, and E. C. Smith, "Rate prediction for single event effects-a critique", *IEEE Transactions on Nuclear Science*, vol. 39, no. 6, pp. 1577–1599, Dec. 1992, ISSN: 0018-9499. DOI: 10.1109/23.211340.

[266] M. Huhtinen and F. Faccio, "Computational method to estimate Single Event Upset rates in an accelerator environment", *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 450, no. 1, pp. 155–172, 2000. DOI: 10.1016/s0168-9002(00)00155-8.

[267] CMS collaboration *et al.*, *Radiation Simulation Plotting tool v.2.0*, 2019. [Online]. Available: https://cms-project-fluka-flux-map.web.cern.ch/.

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EXPERIENCE

Digital IC design

CERN (European Organization for Nuclear Research)

2014 – 2019 Geneva, Switzerland

- Design of an intelligent particle tracker detector readout ASIC: architecture studies, RTL description, design implementation in 65 nm technology and sign-off. Low-power and radiation tolerance design techniques have been employed to fulfill the very tight power requirement and to mitigate total ionizing dose and single particle event effects.
- Simulations, studies and optimization of the electronic system architecture of an innovative silicon particle detection system, capable of providing information regarding the particle trajectory and transverse momentum for the CMS detector.)
- Design and implementation of a multi-purpose radiation tolerant mixed-signal control and monitoring ASIC for multiple high energy physics experiments.
- FPGA RTL design for multiple projects.
- Test software and PCB development for ASICs performance characterization.
- RTL and software for a SoC based control unit for the LHCb experiment.

PDKs maintenance and design support

CERN (European Organization for Nuclear Research

2018 – 2019 Geneva, Switzerland

- Design and EDA tools support for CERN projects and European institutes part of the collaboration.
- CERN mixed-signal design kits maintenance.
- Scripted design flows releases.

EDUCATION

Ph.D. candidate in Microsystems and Microelectronics

EPFL – Ecole Polytechnique Fédérale de Lausanne
Microelectronic Systems Laboratory

Lausanne, Switzerland

M.Sc. cum Laude in electronic engineering

University of Pisa

Pisa, Italy gpa: 28.5/30

B.Sc. cum Laude in electronic engineering

University of Pisa

Pisa, Italy gpa: 29.3/30

TECHNICAL SKILLS

Hardware design

System Verilog | Verilog | VHDL | UVM methodology | IC implementation | sign-off | FPGAs (Xilinx/Altera) | SoC

Programming and scripting

C | C++ | Python | Bash | TCL

Software and EDA tools

Cadence Genus | Innovus | Voltus | Tempus | Incisive | Virtuoso | Conformal | Calibre | Xilinx Vivado | Intel Quartus II | Altium | MATLAB | LabVIEW | Android Studio | Visual Studio

Operating systems

Arch Linux | RedHat | Ubuntu

LANGUAGES

English
Italian
French
Spanish
Russian

OTHER ACTIVITIES

Embedded software

rLoop team

- Took part in the design of a prototype capsule for the concept of a magnetic levitation transport system in vacuum tube. Innovation award at the Space-X Hyperloop pod competition.

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