Multiport Energy Gateway

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Abstract

The global problem of energy supply and the reduction of the carbon footprint can only be solved by a massive replacement of fossil fuels and nuclear energy by renewable resources such as solar or wind energy sources. As these latter are mostly weather-dependent, they are uncontrollable and unpredictable in the long term. Their relative volatility can be mitigated with their spreading in terms of number and in terms of geographical location, as well as with the use of storage elements. These being mostly DC, their integration would be considerably eased by the use of DC grids which would allow the synchronization of resources to be avoided and would eliminate line impedance effects, proper to AC systems, and thus allowing the energy to be transferred over longer distances and through meshed networks more complex and requiring new types of interfaces or converters.

Indeed, in the past, voltage step-up and step-down transformations were only possible with the help of low-frequency (50-60Hz) and bulky transformers, which are still used nowadays in most AC grids. But the progresses of the last two decades in the field of power semiconductors now allow the realization of high-performance DC-DC converters with increasingly high voltages. A promising concept is the solid-state-transformer (SST), which uses a multi-modular structure integrating multiple medium-frequency transformers and offers an efficient and compact solution for voltage adaptation. While several researches on this particular subject have been done or are in progress for bi-port converters, the multiport version of it, which would allow the integration of storage elements directly on the additional port(s), has been only very few studied.

Therefore, this thesis proposes a new converter structure which combines on one hand the SST principle, in order to reach medium voltage ratings and on the other hand the multiport resonant conversion principle in order to limit switching losses and achieve higher switching frequencies necessary for an increased power density.

After a brief overview of existing storage technologies and multiport converters topologies, a description of the proposed structure and its operating principle are presented. The structure is composed by multiple identical submodules, connected in series on the MV side, in parallel on the LV side and each able to inteface a storage element on an extra port. This results in a relatively simple operation based on operating modes depending on the direction of the energy flow and allowing the independent use of one or more storage elements. Then, the mathematical models required to describe the converter are developed for each of these operating modes and make it possible to highlight the operating regions benefiting from soft switching and having a higher efficiency. This area is defined by the ratio of the impedances of the split resonant tank distributed between the three ports of each submodule. These models are also used to define sizing criteria which are applied for the design of a prototype converter for the medium-voltage grid and which parameters are used as the basis for the simulation. Finally, a detailed description of the converter dynamics is presented and simplified into models from which a control structure can derived and the controller parameters are calculated. In order to illustrate each of the elements developed in this work, a low-voltage prototype is designed and experimental results support most of the outcomes of this work.

Keywords: multi-port resonant converter, medium-voltage DC grids, power electronics, soft switching

Résumé

La problématique globale de l'approvisionnement en énergie et la réduction de l'empreinte carbone ne peuvent être résolus que par un remplacement massif des énergies fossiles ou atomiques par des ressources renouvelables. Ces dernières étant pour la majeure partie dépendantes de la météo, elles sont non contrôlables et imprévisibles à long terme. Cette volatilité peut être palliée avec l'intégration d'un nombre élevé de ces ressources, leur répartition géographiquement décentralisée, ainsi que l'utilisation d'éléments de stockage. Ceci serait facilité par l'utilisation de réseaux à courant continu (DC) qui permettraient de s'affranchir de la synchronisation des ressources et supprimeraient les effets d'impédance de ligne, autorisant ainsi le transport de l'énergie sur des distances plus grandes et à travers des réseaux maillés plus complexes nécessitant de nouveau types d'interfaces ou convertisseurs.

En effet, dans le passé, l'élévation et l'abaissement de tension n'étaient possible que via des transformateurs basse-fréquence, utilisé aujourd'hui encore dans la plus part des réseaux à courant alternatif (AC). Mais les progrès faits durant ces deux dernières décennies dans le domaine des semiconducteurs de puissance permettent maintenant la réalisation de convertisseurs DC-DC performants et atteignant des tensions de plus en plus élevées. Un concept prometteur est le solid-state-transformer (SST). Il inclut une structure multi-modulaire intégrant de multiple transformateurs moyenne-fréquence et offre un moyen d'adaptation de tension efficace et compact. Mais si de nombreuses recherches sur le sujet ont été faite ou sont en cours pour des convertisseurs bi-port, la version multiport, qui permettrait l'intégration d'éléments de stockage directement sur les ports additionnels, n'a été que très peu été étudiée.

Cette thèse propose donc une nouvelle structure de convertisseur combinant à la fois le principe de SST destiné à la moyenne-tension et le principe de convertisseur résonant multiport permettant de limiter les pertes par commutation et d'atteindre des fréquences de commutation plus élevées, synonymes d'une densité de puissance accrue. Après un bref aperçu des technologies de stockage et des convertisseurs multiports existants, une description de la structure proposée ainsi que son principe de fonctionnement sont présentés. La structure est constituée de plusieurs sous-modules identiques connectés en série du côté moyenne-tension, en parallèle du côté basse tension et pouvant interfacer chacun un element de stockage sur un port additionel. Il en résulte un fonctionnement simple basé sur des modes d'opération dépendants de la direction du flux d'énergie et qui permet l'utilisation des éléments de stockage de manière indépendante. Ensuite, les modèles mathématiques nécessaires à la description du convertisseur sont élaborés pour chacun de ces modes de fonctionnement et permettent de mettre en évidence les zones d'opération bénéficiant de commutation douce d'un rendement plus élevé. Cette zone est définie par le rapport des impédance des circuits résonants répartis entre les trois port de chaque sous-module. Ces modèles servent aussi à définir des critères de dimensionnement qui sont appliqués pour la conception d'un convertisseur prototype destiné au réseau moyenne-tension et dont les paramètres sont utilisés comme base pour la simulation. Finalement, une description de la dynamique du convertisseur est présentée à l'aide de modèles simplifiés à partir desquels la structure de contrôle est dérivée et les paramètres des régulateurs sont calculés. Dans le but d'illustrer chacun des éléments développés dans ce travail, un prototype basse-tension est conçu et permet d'appuyer la majeure partie des conclusions de ce travail par des résultats expérimentaux.

Mots-clés: convertisseur multiport résonant, réseaux continus moyenne tension, électronique de puissance, commutation douce

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List of Abbreviations

AC	alternating current
BESS	battery energy storage system
BOM	bill of material
CAES	compressed air energy storage
DAB	dual active bridge
DC	direct current
DCM	discontinuous conduction mode
DISO	dual-input-single-output
EDLC	electrical double layer capacitor
ES	energy storage
FHA	first harmonic approximation
HESS	hybrid energy storage system
HVDC	high voltage DC
IGBT	insulated-gate bipolar transistor
IPOS	input-parallel-output-series
ISOP	input-series-output-parallel
LV	low voltage
LVDC	Low voltage DC
MAB	multiple-active-bridge
MEG	Multiport Energy Gateway
MFT	medium frequency transformer
MV	medium voltage
MVDC	medium voltage DC

NPC	neutral point clamped
PV	photo-voltaic
QAB	quadruple-active-bridge
SFOE	Swiss Federal Office of Energy
SIDO	single-input-dual-output
SISO	single-input-single-output
SNSF	Swiss National Science Foundation
SOC	state-of-charge
SRC	series resonant converter
SST	solid state transformer
TAB	triple-active-bridge
UPS	uninterruptible power supply
ZCS	zero-current-switching
ZVS	zero-voltage-switching

List of Symbols

A_{core}	Cross section of one element of the ferrite core of a MFT
B_{max}	Maximum flux density, tesla
C_r	Resonant capacitance
$C_{DC,i}$	Capacitance of the DC-bus on port i
C_{com}	Common mode equivalent resonant capacitor
C_{dif}	Differential mode equivalent resonant capacitor
$C_{oes,i}$	Output capacitance of the IGBT i
$C_{r,p}$	Resonant capacitance located on the primary side of the MFT
$C_{r,s}$	Resonant capacitance located on the secondary side of the MFT
$C_{r,x}$	Resonant capacitance located the port x of the MFT
E_{cond}	Conduction losses of a semiconductor
E_{off}	Turn-off losses of a semiconductor
E_{on}	Turn-on losses of a semiconductor
E_{rr}	Reverse recovery losses of a diode
I_{base}	Current normalization base
K_f	waveform coefficient
L_σ	Leakage inductance
L_m	Magnetizing inductance
L_r	Resonant inductance
L_{com}	Common mode equivalent resonant inductor
L_{dif}	Differential mode equivalent resonant inductor
$L_{r,p}$	Resonant inductance located on the primary side of the MFT
$L_{r,s}$	Resonant inductance located on the secondary side of the MFT
$L_{r,x}$	Resonant inductance located the port x of the MFT
N_c	Number of parallel ferrite element in a MFT core
N_s	Number of cascaded submodule of a MEG converter
P_{max}^{air}	Maximal losses dissipation of an air-cooled system
P_{max}^{water}	Maximal losses dissipation of a water-cooled system
P_{ES}	Power from the energy storage elements
P_{LV}	Power from the low-voltage port
P_{MV}	Power from the medium-voltage port
P_{com}	Common mode equivalent power

P_{dif}	Differential mode equivalent power
$P_{k.n}$	Power from the port k of submodule n
Q_a	Available charges in a soft-switched current
Q_{oes}	Stored charges is a semiconductor
Q	quality factor of a RLC circuit
R^{th}_{c-f}	Thermal resistance between module case and heat-sink fin
R^{th}_{f-a}	Thermal resistance between fin and air
R^{th}_{j-c}	Thermal resistance between semiconductor junction and module case
R_{com}	Common mode equivalent parasitic resistor
R_{core}	Reluctance of a ferrite core
R_{dif}	Differential mode equivalent parasitic resistor
R_{gap}	Reluctance of the air gap
R_{on}	On-state resistor of an IGBT
$T_{dt,i}$	Deadtime of the semiconductor i
T_{res}	Resonant period
T_{sw}	Switching period
V_{base}	Voltage normalization base
$V_{dc,k}$	DC bus voltage on the port k
V_{dif}	Differential voltage between the DC bus of two ports
V_f	Forward voltage of an IGBT
Δ_T	Temperature elevation
α	Damping attenuation of a RLC circuit
μ_0	Permeability of air
μ_r	Relative permeability
ω_0	Resonant angular frequency
ω_d	Damped resonant angular frequency
ζ	Damping factor of a RLC circuit
d_i	Duty-cycle of the DC-DC stage on port i
f_{Bi}	Switching frequency of the regulation stage on the port i
f_r	Switching frequency
f_{sw}	Switching frequency
$i^x_{ac,k}$	Resonant current in the port k during interval x
i_{com}	Common mode current
i_{dif}	Differential mode current

$i_{k.n}$	Current through the port k of submodule n
l_{core}	Magnetic path length in a ferrite core
l_{gap}	Air gap length
$v_{ac,k}^{X}$	AC voltage applied to the port k of the resonant stage during the interval X
$v_{k.n}$	Voltage at the terminals of port k of submodule n

Contents

1 Introduction

1.1 Background and motivation

The global awareness of environmental issues and energy supply has led to many changes in the policies and strategies of governmental energy offices and at every link in the chain from producers to consumers. With regard to Switzerland, the evolution of the energy policy is dictated by two goals: First, the 2050 Energy Strategy (SE2050), signed in 2007 and reinforced in 2011 after the Fukushima nuclear disaster, aims for a gradual, but complete, exit of the nuclear power generation by 2050. Secondly, the ratification of the Paris Agreements in 2015 (COP21), aims for a 50% reduction in the emission of CO_2 and greenhouse gases resulting from the use of fossil fuels (petroleum), by 2030 (see **Fig. 1.1**). This implies a complete replacement of nuclear energy generation as well as a partial or complete replacement of fossil fuels by renewable energies. These latter being currently very limited, it also implies a reduction of the energy consumption per capita by almost 54% by 2050 (see **Fig. 1.2**) and a decrease in electricity consumption by 18% [1]. These goals can only be achieved with an increase in efficiency and therefore a reduction in losses, as well as with a smarter use of the resources in all areas. This includes the energy transport (efficiency of whole chain from production to distribution and the resulting conversion steps) through improved infrastructures, and the end use of it in the households (certified appliances), in the transportation (hybrid or purely electric vehicles) as well as in the construction (thermal insulation).

Although the trend in energy consumption is not yet declining despite these strategic measures and the favorable climate of recent years (which required less heating energy) [3], it is stabilizing compared to previous years demographic and economic growth of the country. On the other hand, the substitution of fossil fuels by electricity is clearly visible in all domains [2], [4], such as households, industry, services or transport (with a growing tendency to favor electric vehicles for both public and individual transportation). These provisions will result in the end in a growing share of electricity in terms of final consumption and an energy production mostly from renewable resources.

Unlike controllable resources, from which the available energy can be estimated and which production can be controlled accordingly (e.g. hydro-power, biomass and geothermal), stochastic resources (such as wind-turbines or solar plants, which potential varies with the climate and the weather) cannot be controlled to meet a specific demand, although its production can be estimated on a very short horizon. Thus, the eventual mismatch between the production and the consumption, in terms of peak power or timing, can be overcome with the use of storage elements. In addition, the decentralization of these resources and storage elements is expected. This, by playing on the fact that with an increasing number of resources and their distribution over a large geographical area, the probability that the energy needed at a given time is available somewhere in the network is increased [5], [6]. The Swiss

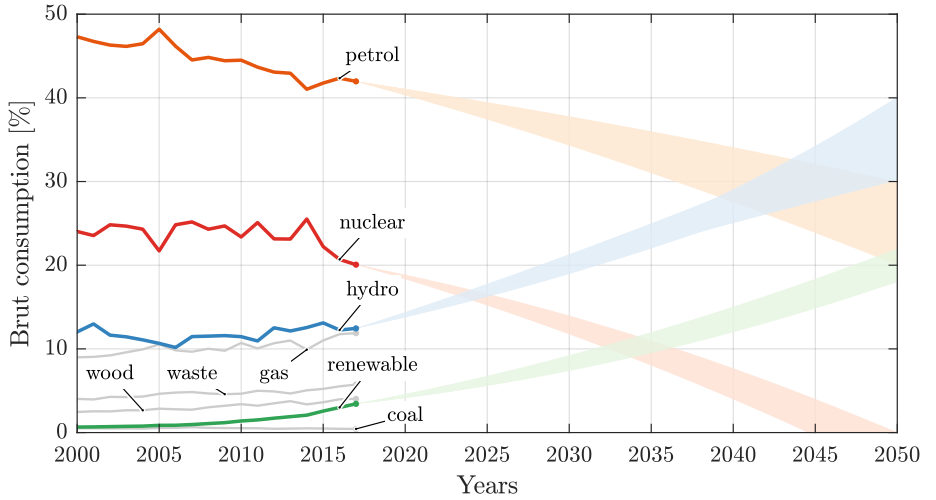


Figure 1.1 Part of the primary consumption (form of energy before conversions, transportation and storage) of Switzerland: actual number for past 15 years [2], and the objectives according to ES2050 scenario and COP21 for the future.

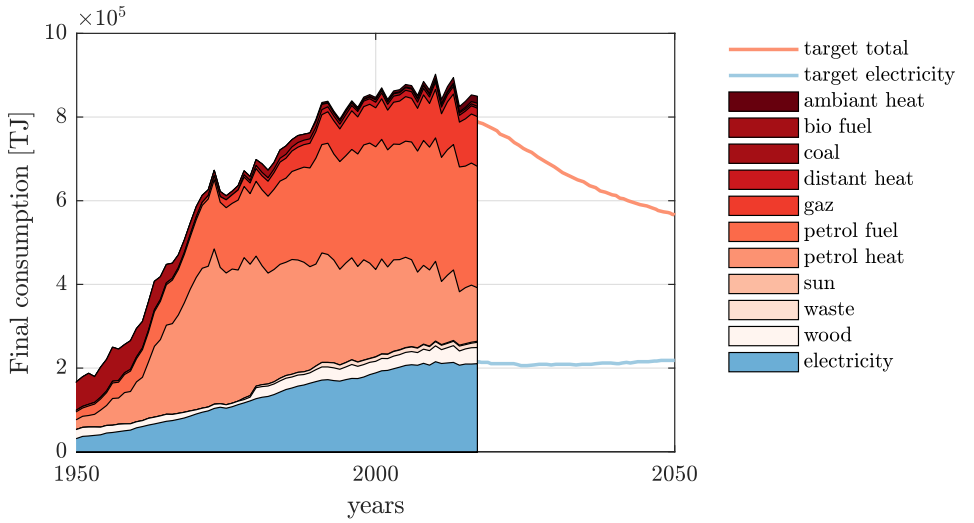


Figure 1.2 Energy consumption in its final form and its targeted evolution according the Swiss Federal Council [1].

Federal Office of Energy (SFOE) predicts that by 2050, 10% to 20% of total Swiss production will come from distributed generation.

In addition to an increased stability and redundancy by means of the use of multiple and widespread elements, the local consumption of local production can help in terms of decongestion of the grid. The principle of self-consumption [7] may be implemented in the case of some buildings or groups of buildings where the use of energy from their own production is made possible thanks to the integration of storage elements such as batteries. It also makes it possible to play with market prices by using storage to store energy from the grid only when the prices are advantageous, thus indirectly

contributing to the stability of the grid. Decentralization, which concerns both renewable energy sources and storage elements, requires a good integration of these resources into the overall system and necessitates thus a powerful control structure and hardware with increased features.

From the software point of view, the digitalization of the world (IoT), which produces a constant flow of information (production, consumption, availability, etc...) is a dominant factor in progress [8]. With a smart analysis, it enables a more and more accurate forecast of the production allowing its optimization while giving flexibility to the demand. A national research project (NRP70) [9] funded by the Swiss National Science Foundation (SNSF) is currently developing a communication protocol between sources and loads and a control structure able to regulate electrical grids or islanded micro-grids with very low inertia, and with very high penetration rate of renewable energy (up to 100%) by monitoring in real-time the available potential of the sources, by controlling the demand accordingly and by playing with storage elements with various time constants such as thermal inertia of buildings, stationary electric vehicle battery or even a so-called "virtual storage" by shifting, over the time, the energy demand of non-critical applications.

If the evolution of the grid goes hand in hand with the development of control strategies, whose progress is already consequent with the concepts of smart-grids and smart-meters [10], it also goes with the upgrade of the hardware and the infrastructures. This is reflected with the need for new conversion and interconnection systems capable of providing highly dynamic control, increased reliability and high efficiency. The standard production-transport-distribution-consumption chain must evolve into a more complex meshed system with bidirectional links and nodes that can be both sources and loads, thus requiring new infrastructures or the modification of the existing ones. This is where the progress made in recent years in the fields of semiconductors and power electronics are key factors allowing a conversion with very high efficiency while providing high power density [11]. Indeed, if in the past, step-up and step-down conversion was not easily possible in direct current (DC) because of the absence of semiconductors, today's voltage and current levels reachable in the semiconductor field enable very high power DC/DC conversion without the need for the low frequency (50-60Hz) transformers which are used in alternating current (AC) domain.

Hence, DC technologies are promising solutions for the grids of the future: on one hand, at high and very high voltage, they allow a more efficient transport of bulk energy over long distances, getting rid of line effects and reactive power flows affecting AC systems [12]. The first high voltage DC (HVDC) transport lines have been commissioned already in the last century and are becoming more widespread for offshore transmission, reaching powers in the range of multiple of GW. On the other hand Low voltage DC (LVDC) distribution allows easy connection of storage elements that are inherently low voltage and DC (e.g. batteries and super-capacitors). It also reduces the number of conversion stages for the distribution to the loads which are also either DC (e.g. servers, computers and TV's) or using variable frequency and are therefore requiring a DC stage (e.g. rotating machines and household appliances). Additionally, the energy savings obtained using LVDC micro-grids at the level of residential buildings, or a group of them, haven been proven [13]. Therefore, the medium voltage DC (MVDC) grids come as a natural interface between the bulk transport using HVDC lines and the LVDC storage elements, loads or micro-grids. They allow a simplified interconnection of intermittent and variable voltage sources while avoiding the synchronization necessary for the AC grid which becomes very complex with a high number of resources, and therefore offers increased stability. If the current grids still use mainly AC, it is mainly for historical and cost reasons and the future scenario of DC grids or micro grids is taken very seriously [14].

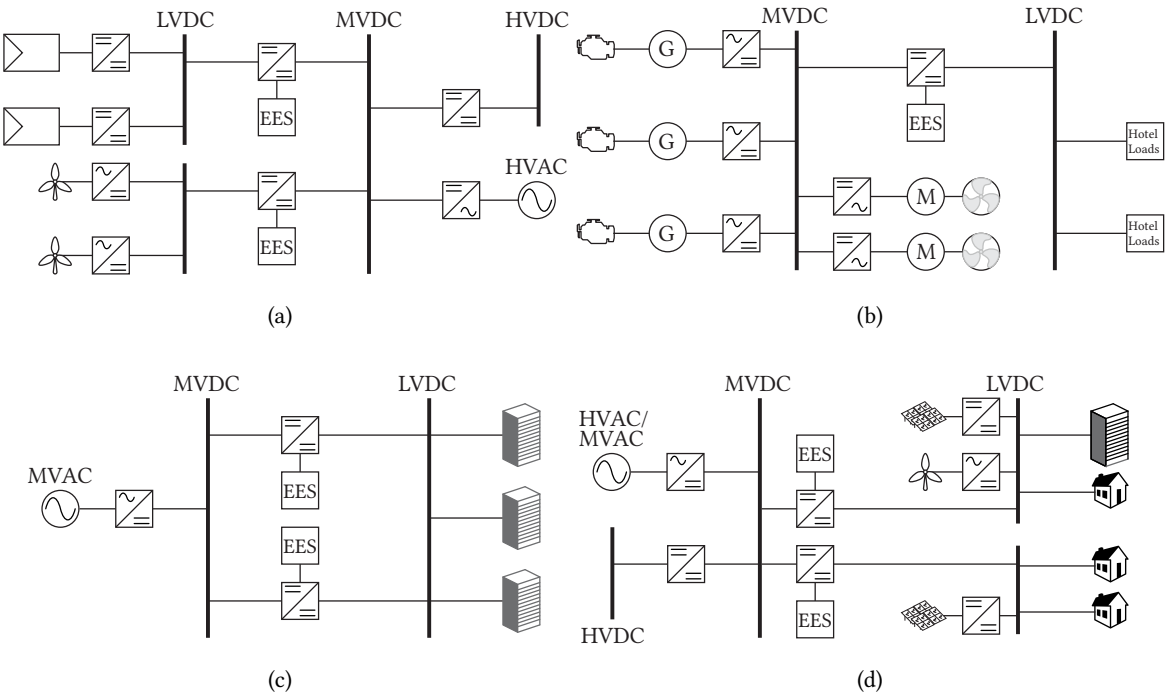


Figure 1.3 Various applications where MVDC technologies are promising and where the integration of storage will help in terms of performances: (a) Renewable generation: In the case of PV generation, the integration of storage will increase power quality, providing an energy buffer in order to be able to run, on one side, the MPPT algorithm and inject on the other side, a stable and controlled amount of power. Additionally, bulk power storage can compensate the drop of production in case of quick and partial shading [15]. In the case of large scale off-shore wind farms, the volatility of wind energy generation, either at LV or MV, would benefit from integrated energy buffer [16]. (b) Marine: The on-board MVDC grids will allow further frequency decoupling of the generation and distribution, improving the overall fuel efficiency. Moreover, the integration of storage will allow for regenerative breaking, peak shaving and support for black-start conditions. (c) Datacenters: The power to the chip is very critical, and storage elements can greatly increase the reliability of such systems with high power uninterruptible power supply (UPS). (d) DC micro-grids: Behaving part of the day as a source thanks to the renewable energy resources and part of the day as a load, due to the peaks of energy consumption during critical hours (home appliance, lighting, heating), micro-grids are relying on the integration of storage elements. They are key elements allowing the auto consumption of the energy produced inside the micro-grid and helping toward the decongestion of the distribution grid.

With regard to MVDC applications, one example is the first DC datacenter, built by ABB and Green CH [17], which has been in operation in Zurich area already for a few years. Often requiring installed powers above 1 MW, datacenters power supply is one of the most critical application and the use of storage elements can greatly improve the reliability. All CPUs, memory chips, and disk drives consume direct current, and the power-to-the-chip requires numerous conversion step in the conventional AC structure to achieve the low voltage levels required [18]. In this sense, DC systems enable a reduction in the number of conversion stages, a higher efficiency and a reduced volume while allowing an eased integration of UPS with hybrid storage elements [19].

Concerning MVDC grids or micro-grids, the most relevant example that can be mentioned is the marine field where on-board DC grids have many advantages [20], [21]. The electric ships have

the advantage of proposing not only a spatial decoupling of the generation and propulsion which offers great flexibility in ship design for a better spatial distribution of the loads, but also a frequency decoupling, which permits for the AC generators to run at optimal speed, improving the overall fuel efficiency. In addition, the integration of storage elements allows the support of power peaks due to startup sequences as well as the recovery of energy during braking.

At the distribution level, MVDC technologies are seen as good alternatives or complements to the existing grid. As a matter of fact, Siemens also recently announced one of the first commercial solutions for MVDC distribution networks [22].

1.2 The thesis

1.2.1 Scope

The few examples mentioned earlier and depicted in **Fig. 1.3** highlight two main ideas:

- MVDC grids are a promising intermediary step between the HV (AC or DC) bulk transportation and the distribution or the collection. They allow great flexibility and ease the connection of volatile resources while providing a good efficiency.
- LVDC grids or micro-grids are a promising solution for the integration of local storage and renewable resources. They are, together with the storage, key elements allowing local consumption of the local production.

The interconnection of a MVDC grid, a LVDC grid and various storage elements reveals the need of new interfaces able to provide bidirectional power flow and good controllability while being able to withstand MV rating and provide high efficiency. The progress done in the domain of semiconductors during the past decades allows us now to handle higher voltages at higher frequencies, making the emerging concept of solid state transformer (SST) even more promising for further developments of the future grids [23]. The idea of increasing the efficiency and the reliability of the cycle storage-restitution by decreasing the number of conversion stages motivates the development of a fully bidirectional multiport power electronics interface. Moreover, the state-of-the-art developments propose either MV rated bi-port converters or LV and low power multiport converters, but no converters able to withstand MV rating while providing additional power ports has been reported so far.

Taking, as background scenario, the application of the interface between a LVDC micro-grid and a MVDC grid with integrated storage such as depicted in **Fig. 1.4**, this work focuses on the elaboration of a new topology, inspired from said SST and derived to a multiport version, in order to provide full bidirectionality, galvanic isolation, compactness and efficiency.

The LVDC micro-grid, in the range of 750 V and 0.5 MW, represents a group of elements comprising resources such a PV arrays or wind-turbines and loads such as domestic consumers and servers. The LVDC side may behave either as a load or as a source depending on the time of the day and is subject to rapid variations in both production (quick cloud shading on the PV arrays) and consumption (inrush power, black start of machines, servers computation processes) in the range of seconds to several minutes.

The MVDC grid, characterized in the range of 10 kV, is a multi-terminal MVDC grid (of a ship for instance) or the intermediary stage between the HVAC transportation lines and the LV grid (such as in **Fig. 1.3d**). It is considered as a stiff grid, its voltage remains fixed and stable, and is bidirectional. In order to increase the stability and the power quality in this MVDC grid, the power flow from/to the LVDC grid has to be smoothed thanks to the storage elements.

The energy storage (ES) elements is a mix of batteries and super-capacitors able to absorb abrupt peaks of power as well as compensate slower small variations. They are considered as a support to the main power flow between the LVDC grid and the MVDC grid, and their power ratings are therefore reduced (20% of the nominal power).

The thesis is focused on the multiport DC-DC converter and especially on the proposition of the core structure: a multiport resonant DC-DC transformer. Although resonant converter topologies have been studied in the past, their multiport version is novel and only few literature references deal with its design and even less about its control. Thus, the main effort of this work is to assess the feasibility, the practicality and the relevance of such topology while developing models, design rules and a possible control structure. The assessments of the theoretical outcomes of the research are supported by the realization and the tests on a LV prototype of a single stage.

1.2.2 Objectives of the thesis

The objectives of the thesis are:

- The elaboration of the structure of a converter comprising a MVDC terminal, a LVDC terminal and one or multiple terminal dedicated to the connection of LV storage elements. This structure has to provide:
  - 10 kV from/to 750 V voltage adaptation for a rated power of 0.5 MW.
  - Galvanic isolation between the various ports.
  - Complete bidirectionality.
  - Simple controllability of the various power flow.

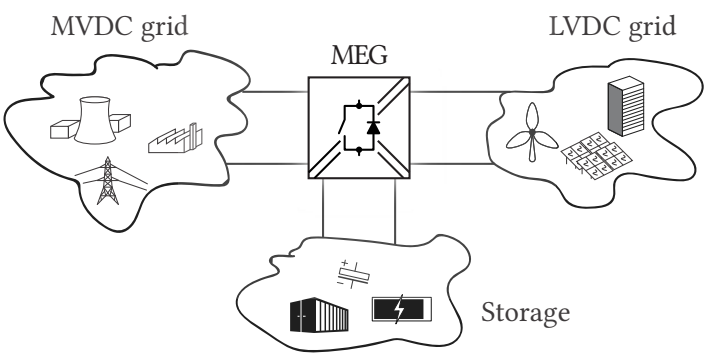


Figure 1.4 Scope of the thesis. The MEG as an interface between the storage and the future DC grids.

- The assessment of this structure in terms of feasibility, advantage over prior art structures, as well as its limits and drawbacks, by simulations and experiments.
- The elaboration of a control structure able to operate in all the modes operation linked to the targeted field of application.
- The development of tools and models necessary for further design and optimization of the developed topology.

The thesis focus on the overall topology at the system level. Therefore the following topics are excluded from the scope of this research:

- The design of the MFTs, their specification (dimensions, number of windings, sections), choice of the materials (core, isolation), their thermal analysis. The MFT models used in this work are thus ideal model without deep consideration of these last points.
- The storage technology and its design. The choice of the technology as well as the sizing in terms of power and energy are driven by specifications linked to the final application and are therefore not addressed in this work.
- The precise characterization of the hardware component, especially the semiconductors. The models of the devices used in this work are their ideal models, sometimes taking into account the losses parameters form the commercial datasheets. But no precise TCAD models are considered.
- The safety mechanism and the degraded operation of the converter. Over-voltage and short-circuit events are not addressed in this work.

1.2.3 Main contributions

With respect to the objectives mentioned earlier, the main contributions of this thesis are:

- The proposal of a new structure of DC-DC converter designated by "Multiport Energy Gateway" or MEG (see publication **[C2]**), as depicted in **Fig. 1.5**. Its novelty sits in the input-series-output-parallel (ISOP) combination of multiple resonant converters operated as DC-transformers. This makes it possible to interface a MV rated grid on one side, a LV rated grid on the second side and multiple LV storage elements on the additional ports. The topology and its modes of operation are presented and the main features as well as the principal operating constraints are highlighted.
- The proposal of the extension of the well-known LLC converter to a multiport version of it (see publication **[C4]**). The coupling of a third winding on the medium frequency transformer (MFT) and the splitting of the resonant tank between the three sides enable a single stage, fully bidirectional and isolated interface between three different ports. The use of a resonant structure, enabling soft switching, makes possible the operation of such converter at relatively high frequencies, synonymous of compactness and efficiency.
- A simplified model and derived analytical expressions of this novel multiport resonant converter: the precise mathematical expressions of the voltage and current waveforms inside the multiport converter allow for the characterization of the natural power sharing (see publications **[C1]**

and **[J2]**), the zero-voltage-switching (ZVS) operation and the dynamics of the system. By extension, the model leads to some insights to derive design rules.

- The proposal of a control structure and strategy for the Multiport Energy Gateway (MEG) topology: a control method involving multiple cascaded PI loops is presented. It makes it possible to operate the converter in all the various modes needed by the application and allows an independent control of each storage element (see publications **[C3]** and **[J1]**).
- The theoretical design of two converters: the first one, corresponding to targeted application, is rated for 0.5 MW, 10 kV and serves as a study case for simulation examples. The second one is a 10 kW/360 V lab-scale prototype built in order to provide experimental results.

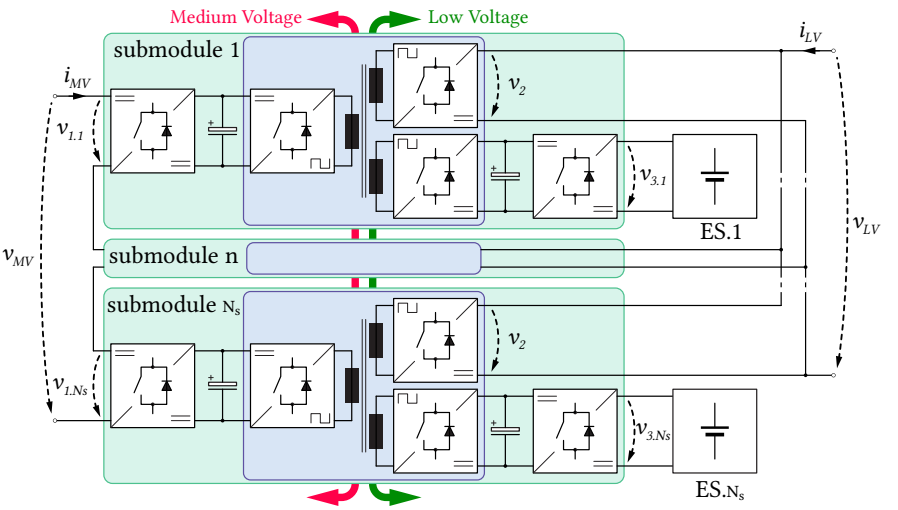


Figure 1.5 The MEG converter: an ISOP combination of multiport submodules, able to interface a MV grid, a LV grid and multiple storage elements.

1.2.4 Structure of the thesis

The rest of this thesis is organized as follows:

The chapter 2 presents a brief overview of the state-of-the-art storage technologies and topologies used for MVDC/LVDC, multi-port and resonant conversion. The promising concept of SST and the examples of multiport resonant converter motivates the development of a topology based on the mix of both.

The chapter 3 presents the MEG topology, its principle and its use in all the modes of operation. Each functional block is described and the possible features are explained. A resonant stage is responsible for the voltage adaptation and the galvanic isolation, while additional regulation stages control the power flows.

The chapter 4 provides a detailed mathematical model of the multiport resonant DC-DC converter. It reveals that the natural power sharing ratio is depending on the ratio of the resonant impedances and their repartition between the different ports. This gives practical insights for the elaboration of design rules and control structures. Additionally, the ZVS operation range can be derived

from the mathematical model, which allows a rough estimation of the efficiency. The focus is on the particular operating mode where two ports are actively feeding the third one.

The chapter 5 presents the sizing rules of the different parts of the system for a functional design. First, the choice of the various voltage levels and the number of submodules is explained and followed by the specific design of the regulation stage and the resonant conversion stage. It results in a set of realistic parameters which are used as a study case in the next chapter.

The chapter 6 proposes a control structure and its associated strategy. After the derivation of the dynamics model and the transfer functions, a control structure is proposed. The design of the various controllers are presented and assessed with simulations and experimental results. It is shown that this type of multiport converter can be controlled with a relatively simple structure, comprising only PI regulators. Moreover, even though the bandwidth is rather slow, only a limited number of measurements is required.

The chapter 7 concludes the work, highlights the main outcomes from the project and gives an overview of the future research perspectives or improvement opportunities on the topic.

The appendix A gives some detailed mathematical derivations used to model the converter.

The appendix B presents the lab-scale setup. The selection and the design of the components of the LV prototype are briefly explained.

1.2.5 List of publications

Conference papers:

C1. Y. Tran, F. D. Freijedo, and D. Dujic, "Open-loop power sharing of three-port dc-dc resonant converters," in *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2019, pp. 2138–2144

C2. Y. Tran and D. Dujic, "A multiport medium voltage isolated dc-dc converter," in *IECON 2016 - 42nd Annual Conference of the IEEE Industrial Electronics Society*, Oct. 2016, pp. 6983–6988

C3. Y. Tran and D. Dujic, "A multiport isolated dc-dc converter," in *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2016, pp. 156–162

C4. Y. Tran, D. Dujić, and P. Barrade, "Multiport resonant dc-dc converter," in *IECON 2015 - 41st Annual Conference of the IEEE Industrial Electronics Society*, Nov. 2015, pp. 003 839–003 844

Journal papers:

J1. Y. Tran, F. D. Freijedo, and D. Dujic, "Multiport energy gateway," *IET Electric Power Applications*, Apr. 2019

J2. Y. Tran, F. D. Freijedo, and D. Dujic, "Open-loop power sharing characteristic of a three-port resonant llc converter," *CPSS Transactions on Power Electronics and Applications*, vol. 4, no. 2, pp. 171–179, Jun. 2019

2
State of the art

This chapter presents a short overview of conventional storage technologies as well as a brief state-of-the-art in the field of high-power DC-DC conversion and more specifically multiport topologies. With the goal of developing a new structure to interface a medium-term storage (seconds to tens of minutes), a MVDC grid and a LVDC grid, the different existing technologies are compared and evaluated, leading to the proposal of the MEG topology which is studied in this thesis.

2.1 Storage elements and their integration

As mentioned in the introductory chapter, the transition to a fully renewable energy generation goes hand-in-hand with the integration of energy storage solutions. Currently, the storage technologies are of various natures, physics, and have very different specifications [24]. The **Fig. 2.3** presents a classification of different storage technologies [25], [26]. They are mainly of three different types: mechanical, electro-chemical, and electrical technologies. A mix of them is also an interesting option, often referred as hybrid storage.

2.1.1 Mechanical storage technologies

Mechanical technologies include kinetic energy storage (Flywheel) [27]–[29], potential energy storage (pumped hydro storage in accumulation lakes) [30]–[32] and compressed air energy storage (CAES) [33]–[35], as summarized in **Fig. 2.1**. Some of these technologies have the advantage of having a very large storage capacity (tens of GWh) as well as very large installed powers (up to several hundred MW). They are long-established and have proven their longevity and their high efficiency. Nevertheless, they require a conversion of the energy from its electrical form to its mechanical form and vice versa. This necessitates the use of rotating machines involving large, often complex, installations and therefore requires a consequent financial investment, a significant geographical impact and a very high maintenance. And even though their integration into DC grids would require less conversion steps than for conventional grids, the AC nature of the rotary machine necessitates more complex (four-quadrants) power electronics converters compared to DC only storage.

2.1.2 Electrical storage technologies

Electrical technologies include capacitive and inductive storage. Capacitive storage consists of storing the energy in the electric field between two electrodes separated by a dielectric. Thus, the storage

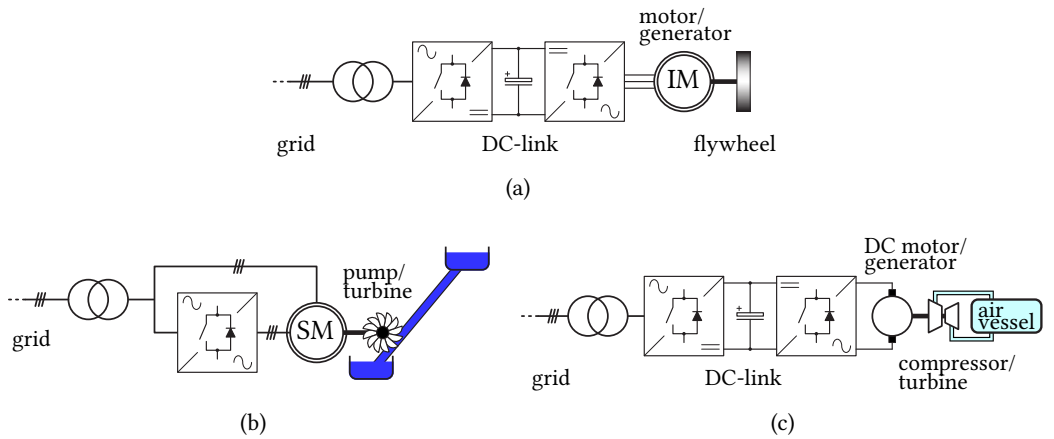


Figure 2.1 Examples of mechanical storage technologies: (a) Flywheel for grid support, (b) pumped hydro for seasonal storage, (c) compressed air as shown in [33].

capacity relies mainly on the surface area of the electrodes and the distance between them. Advances in materials science offer porous materials with larger surfaces, known as electrical double layer capacitor (EDLC), and make this type of storage very attractive for application needing reduced volumes/weight, thanks to its power density, despite a reduced energy density. In terms of integration with the grid, this technology, intrinsically DC, requires only a two-quadrant DC-DC converter which makes it compelling for DC-grid. Inductive storage (SMES) [36], [37], which consists of storing energy in the magnetic field resulting from the flow of a current through an inductor, is ideal for high current and high power applications. However, these high currents require the use of (expensive) superconducting materials to avoid Joule losses and therefore necessitate installations at very low temperatures, which makes the use of these technologies very complex [38], [39] even though solutions integrating SMES are usually controlled with very simple power converters (chopper).

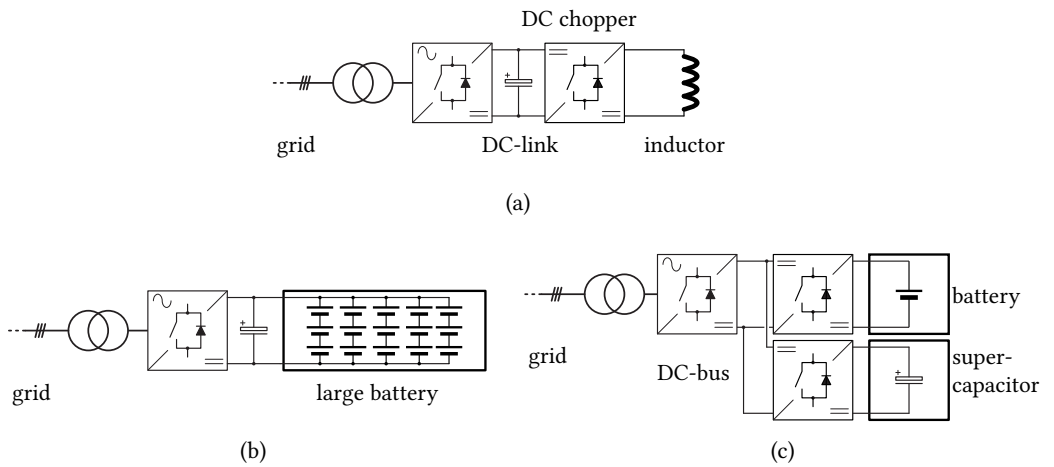


Figure 2.2 Examples of electrical and electrochemical storage technologies: (a) SMES, (b) BESS, (c) Hybrid storage

2.1.3 Electrochemical storage technologies

Electrochemical technologies include battery storage and hydrogen storage. Battery storage is one of the oldest technologies. It uses the energy to be stored to generate a chemical reaction that separates the ions from two electrodes through an electrolytic material. Several processes and types of chemistry are used: lead, lithium-ion, nickel-cadmium, among others, and each has different power density, energy density and lifetime. The main advantage is a high energy density, which makes it the main technology used in electric mobility. This technology, referred as battery energy storage system (BESS) has also recently become an attractive option for mass storage in applications that complement renewable resources [40], support the grid [41]–[43] or provide secured power for critical applications such as datacenters [44]. Like EDLC, BESS are inherently DC and are thus easy to interface with DC grids. Nevertheless, their operation voltages are relatively low and require isolated converters when connected to high power and medium voltage applications or grids.

Hydrogen storage (fuel cell) consists in using the energy to be stored to electrolyze water and thus produce oxygen on one side and hydrogen on the other side, which will either be used as fuel for a combustion engine or used to reproduce electricity by a reverse process [45]. Possible applications range from 100 W to 100 kW, and from micro-grid support [46] to transportation [47]. The advantage is mainly the low standby hydrogen loss, however, the efficiency of the charge/discharge cycle as well as the operating voltages are relatively low.

2.1.4 Hybrid Storage

For the use of a storage element in a medium power application, such as peak-shaving systems for intermittent renewable production [48]–[50] or distribution system stabilization [51], the storage system must support high power while providing good energy density and low standby loss, with time constants ranging from seconds to a few hours.

This is where the interest lies in a hybrid storage solution, also called hybrid energy storage system (HESS), combining both the advantages of batteries and those of super-capacitors [52]. Indeed, batteries, benefiting from a high energy density, are used for low power and long-terms balancing, while super capacitors, benefiting from a high power density, provide balancing during abrupt peaks of high power, such as partial shading on photo-voltaic (PV) farms or black-start of the machines in marine applications [53], for instance. In both production and distribution, systems have been set up and new techniques are constantly evolving. Research activities are mostly focused on the optimal ratio battery/super-capacitors [54] to be considered in the system and on the optimal control, power sharing [55], in order to benefit from better performance and longer component lifetime [56]. The advantages of hybrid storage systems have proven their effectiveness in the low voltage application field and therefore motivate the development of systems based on the same principle, mixing super-capacitors and batteries, for higher power ratings and for applications at the medium voltage (MV) collection and distribution level. Hybrid storage elements being mostly LVDC, the research has to focus on the interface between LVDC elements and MVDC grids.

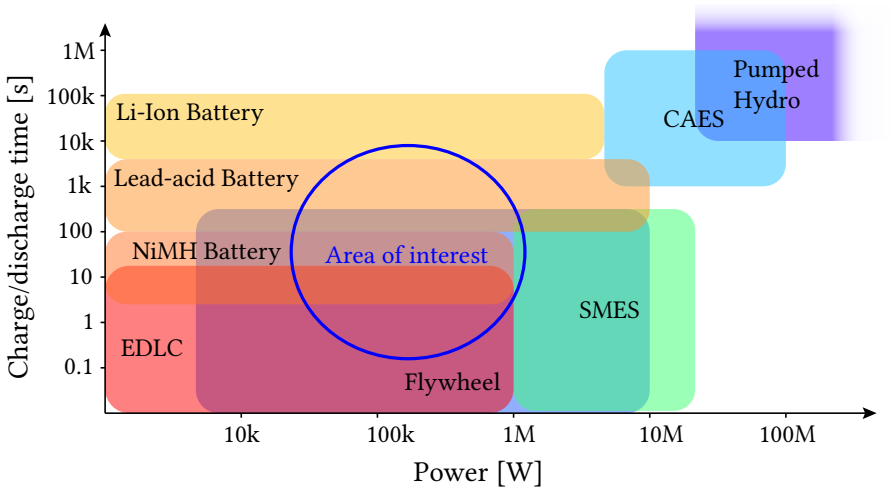


Figure 2.3 Area of use of the different storage technologies. In the case of medium power peak shaving application, hybrid solutions based on super-capacitors and batteries seem relevant.

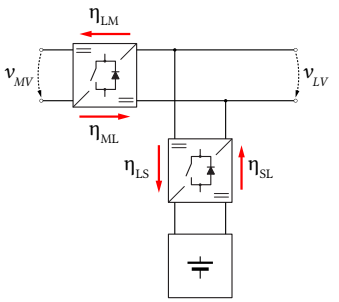
2.2 Topologies of multiport DC-DC converters

Except in the case of direct connection of storage elements to the application such as in [57], which imposes a voltage fluctuation with the state-of-charge, an interface between the storage elements and the grid(s) is necessary. In the case of a peak-shaving application, two grids are considered, one with a stochastic production or consumption of power and the other which power must be controlled and smoothed [58] with the help of storage elements. Three elements must therefore be interfaced and in this case provide a MV/LV voltage adaptation as well. When it comes to systems capable of interfacing more than two elements and in a bidirectional way, the concept of multiport converter appears as a logical and a necessary step to increase performance and reduce the footprint. Indeed, multiport converters are promising in terms of reliability, thanks to the reduction in the number of active components and therefore in the number of sources of failure, in terms of density, by the reduction of components in general (reduction of bill of material (BOM)) and in terms of efficiency, by reducing the number of conversion steps and therefore the losses of the overall charge/discharge cycle (cf. **Fig. 2.4**).

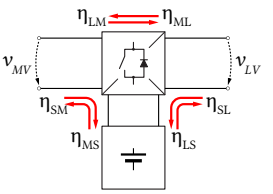
Examples of multiport converters for various applications and powers are referenced in the literature and can be classified into two families. The first is based on the interconnection of the different ports through a common DC bus (non-isolated converters) [59], and the second is based on the magnetic coupling of the different ports through a transformer (isolated converter).

2.2.1 Non-isolated converters

The general principle consists in connecting the N ports to a common DC bus via simple elementary converters (DC-DC converters). The power of each port can be controlled independently and the stability of the system is ensured by controlling the DC bus voltage (cf. **Fig. 2.5**). Although the simplicity of control and the small number of semiconductors are real advantages, this type of conversion topology is limited in terms of voltage range and DC bus voltage selection. The lack of



(a)



(b)

	classical	multiport
η_{MSL}	$\eta_{ML}\eta_{LS}\eta_{SL}$	$\eta_{MS}\eta_{SL}$
η_{MSM}	$\eta_{ML}\eta_{LS}\eta_{SL}\eta_{LM}$	$\eta_{MS}\eta_{SM}$
η_{LSM}	$\eta_{LS}\eta_{SL}\eta_{LM}$	$\eta_{LS}\eta_{SM}$
η_{LSL}	$\eta_{LS}\eta_{SL}$	$\eta_{LS}\eta_{SL}$

(c)

Figure 2.4 Relative efficiency of the cycle charge/discharge of the storage from/to either MV grid or LV grid for the classical method (a) and with a multiport converter (b). Since each conversion step involves different voltage levels, the losses and thus the efficiency are considered different in both directions (i.e. $\eta_{xy} \neq \eta_{yx}$, where η_{xy} is the efficiency of the conversion from the voltage level x to the voltage level y). The overall efficiency of a charge/discharge cycle is given by the product of the efficiency of each conversion step (c). Intuitively, a reduction in the number of conversion steps would improve final performance. In this sens, multiport converters interfacing any of its ports through a single conversion step should be of some advantage compared to classical systems.

galvanic isolation makes this type of topology unsafe and therefore not feasible for high voltage levels and is only suitable for low voltage systems.

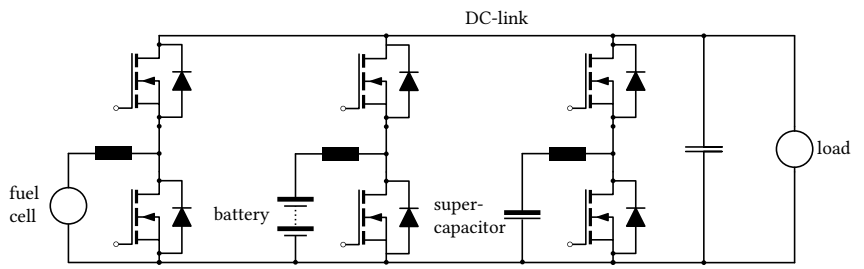


Figure 2.5 Non-isolated multiport converter as in [60] which presents a fuel cell propulsion system with braking regeneration for electric vehicle.

2.2.2 Isolated converters

In the case of isolated converters, the galvanic isolation is achieved by means of a transformer (magnetic coupling) which also allows much more freedom for the voltage transformation ratio. In addition, the high frequency applied to the transformer allows a reduction in the size of the magnetic components. The literature reports numerous converter examples, using a MFT for voltage adaptation and isolation [61]–[63]. These converters are generally composed of an active stage on the primary and a rectifier on the secondary side of the MFT. The bidirectionality of the system is based on the possibility to switch actively the secondary side switching cell in order to be able to reverse the power flow.

In the presence of several sources with the same voltage range, they can be combined on the MFT primary as in [64] where several sources are coupled in parallel. Based on the same topology, the converter presented in [65] incorporates not only a source-side storage element as an energy buffer but also a secondary active rectifier for voltage regulation. However, even if the isolation allows higher voltages and powers, only sources within the same voltage range can be connected together and the converter is unidirectional.

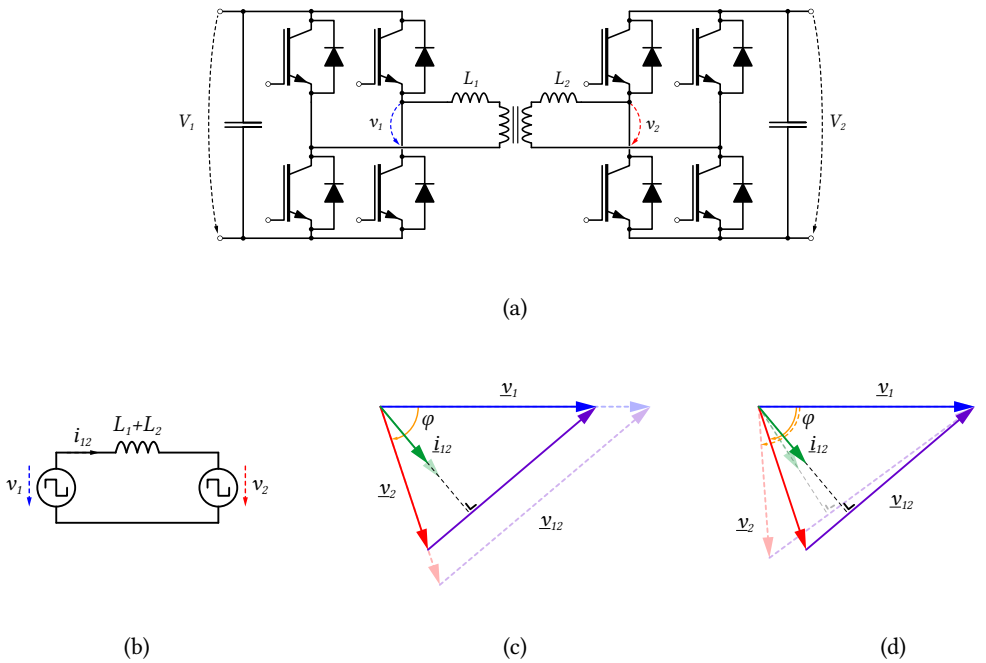


Figure 2.6 (a) structure of a DAB converter. (b) equivalent circuit for the representation of the power flow. (c) vector representation on the duty-cycle control. (d) vector representation on the phase-shift control.

The Dual Active Bridge (DAB) topology is one of the best known and most widespread isolated bidirectional topology. With active switching cells on both sides of the MFT, it allows the voltage and the power flow to be controlled through the duty-cycle and the phase shift angle between the square-wave voltages applied on the primary and secondary, such as depicted in **Fig. 2.6**. In addition to the voltage adaptation possible through the MFT turn ratio, the dual active bridge (DAB) structure can be implemented in a modular way by connecting several DAB modules in series on the MV side to achieve higher voltage levels or reduce voltage stress on the semiconductors and by connecting them in parallel (ISOP structure) on the low voltage side to support large currents [66], such as depicted in **Fig. 2.10c**. This also allows to increase the overall reliability by adding redundant stages. The distribution of thermal stresses on the different stages is also possible. This is the principle used by the SST concept where the isolation stage is a combination of several DAB submodules [23], [67], [68].

The presence of a MFT allows a third port (or even more) to be coupled directly by an additional winding, resulting in an isolated and compact multiport structure (cf. **Fig. 2.10b**). This advanced version of DAB is reported in the literature as triple-active-bridge (TAB) [69], quadruple-active-bridge (QAB) [70] or generally multiple-active-bridge (MAB). Multiple windings offer great freedom in terms

of adaptation ratios and allow grids to be interfaced over a wide range of voltages. This is the case of the converter proposed by the authors of [70] which presents a QAB capable of interfacing, in theory, a high voltage grid, a low voltage grid and PV panels and a battery. Generally, in MAB structures, power control is performed by using phase shift methods, as presented in [71] and [72] (cf. **Fig. 2.7a**). A centralized control system allows the implementation of more complex controls (phase shift and duty cycle), in particular to improve the efficiency of the system by ZVS methods [73]. In addition, one way to reduce the number of semiconductors is to use half-bridges as indicated in [74] (cf. **Fig. 2.7b**), imposing a 50% duty-cycle. A three-phase version of this structure in order to achieve a higher power level is presented in [75].

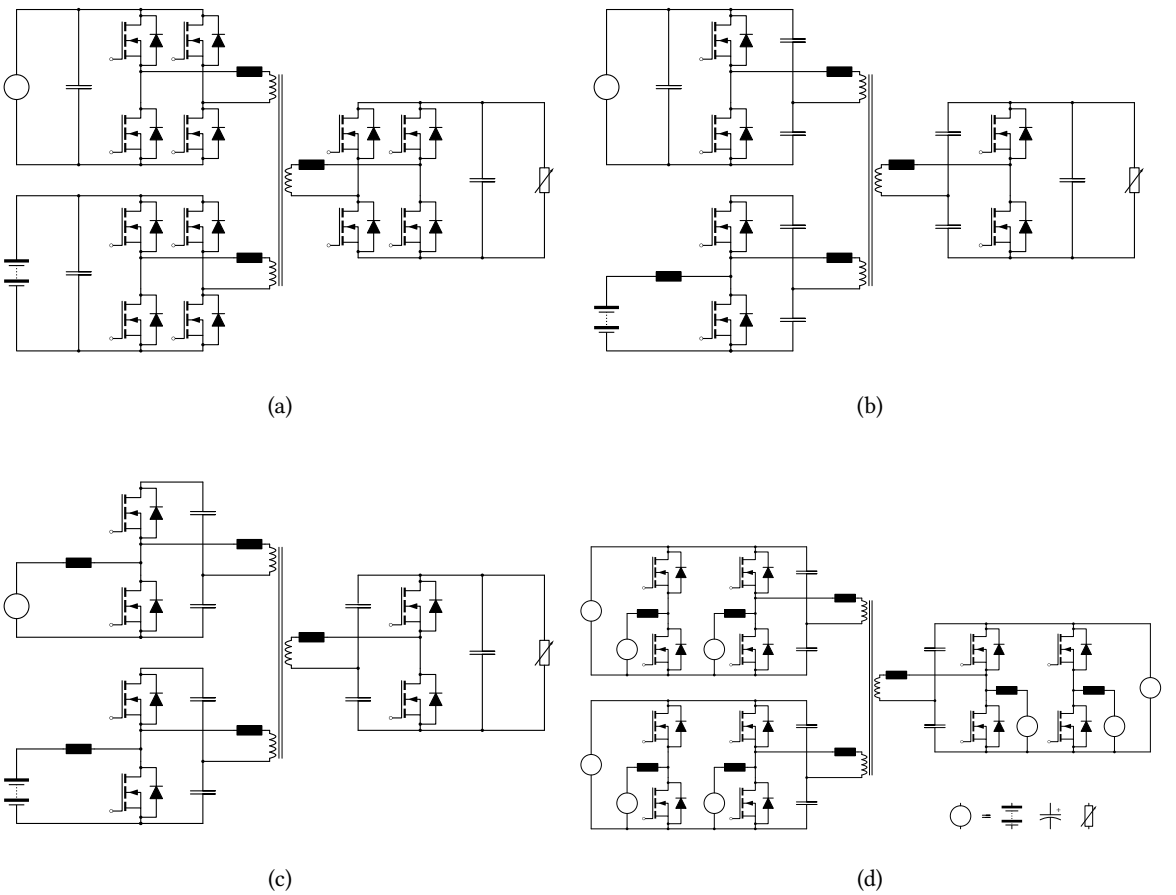


Figure 2.7 Various topologies based on DAB: (a) Triple-active-bridge as presented by [71]. (b) Triple-half-bridge as presented by [74]. (c) Triple-half-bridge with current fed converters as presented in [76](2kW/280V/20kHz). (d) TAB structure with three isolated DC-Bus couple converters as presented in [59].

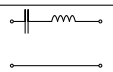
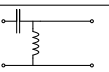
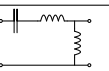
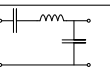
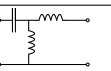
Half-bridges also allow the use of current-fed structures using them in boost converter mode, as demonstrated by the authors of [76](cf. **Fig. 2.7c**). [59] presents a mix of isolated and non-isolated converter structure. Several sources and loads within the same voltage range are connected to each other by a common DC bus, while the different DC buses (of different voltages) are interfaced by a TAB stage (cf. **Fig. 2.7d**).

If the DAB has led to the SST for MV ratings, a multi-modular ISOP, or input-parallel-output-series (IPOS) combination of several MABs is very difficult to operate because of the instability consequent from the degree of freedom offered by power control. Indeed, an additional complex balancing stage for the different DC buses would be required. The authors of [77] show an example of the use of MABs in an ISOP structure, but only to share the stresses between the different ports and not in a multiport way (only one power flow is considered).

2.2.3 Resonant converters

Although the DAB structure is relatively simple and the use of full-bridges and improved modulation schemes allow ZVS, the soft switching operation range remains limited and the trapezoidal waveforms make switching currents relatively high and cause substantial switching losses. In addition, the semiconductors suffer from high dv/dt constraints and voltage over-shoots [78]–[80]. These are some of the reasons to drive interest towards resonant converters. First, they offer extended soft switching operation range, and therefore benefit from limited switching losses which allow to reach higher switching frequencies [81]. Second, the resonant behavior offered by those structures implies quasi-sinusoidal current waveforms, and therefore a limited harmonic content requiring less filtering. Both result in a reduced volume dedicated the magnetics and passive components. This is why they are often used for high efficiency of high power density applications.

Table 2.1 Different types of implementation of the resonant tank

	LC series (SRC)	LC parallel (PRC)	LLC	LCC	CLL
					
Frequency variation	wide	wide	moderate	narrow	moderate
Component stress	lowest	high	low	highest	high
Soft Switching	ZCS	ZVS	ZVS & ZCS	ZVS	ZVS & ZCS

The series resonant converter (SRC) uses a resonant tank composed by the series connection of the transformer's leakage inductance and an additional resonant capacitor, and lead to the resonant topology that provides the smallest stresses on the components (cf. Table **2.1**). SRC type is therefore particularly applicable for high voltage and high power converters [82]. Since the DC gain of such a structure is frequency sensitive (see **Fig. 2.8a**), it is generally operated at a fixed frequency and in discontinuous conduction mode (DCM) mode in order to benefit from ZCS for all transitions. In this operating mode, the voltage ratio is fixed and the output voltage closely follows the input voltage. Indeed, the amplitude of the resonant current, which is proportional to the power, depends on the excitation voltage applied to the resonant circuit, which relies on the voltage difference between the input and output DC buses. An increase in the load creates a slight drop in the voltage of the output bus and therefore an increase in the excitation voltage which leads to an increase in the power transferred. In other words, the power automatically adapts itself so that the two voltages are equal (except for any deviation due to losses) [83]. This behavior is associated with the DC transformer concept, which is characterized by its low output impedance and the lack of controllability of the system. Thus, the voltage regulation must be carried out on one side or the other by an additional stage. This is what is proposed in [84] which presents a SST based on the ISOP combination of

submodule whose isolation stage is a SRC circuit. The balancing is ensured by this property of tight coupling of the inputs and the outputs while the voltage regulation must be carried out via the AC/DC input stage or the DC/AC output stage. Despite the advantages of soft-switching offered by the SRC circuits, the use of insulated-gate bipolar transistor (IGBT) results in switching losses due to the charges stored in the semiconductor [85], which explains an increased interest towards LLC topology.

The LLC converter is a special case of the SRC family in which the magnetizing inductance is used as part of the resonant tank (cf. Table **2.1**) and is dimensioned in such a way that the magnetizing current at switching instants is large enough to charge and discharge the output capacitances of the device to be turned off and the one to be turned on, respectively, in order to benefit from a zero voltage turn-on (ZVS) which becomes even more beneficial with high voltage class semiconductors[86]. Its characteristic allows a variable voltage gain through the switching frequency as shown in **Fig. 2.8c**. This is the principle commonly used at low voltage and low power in the field of switched-mode power supply with a wide range of voltage gain.

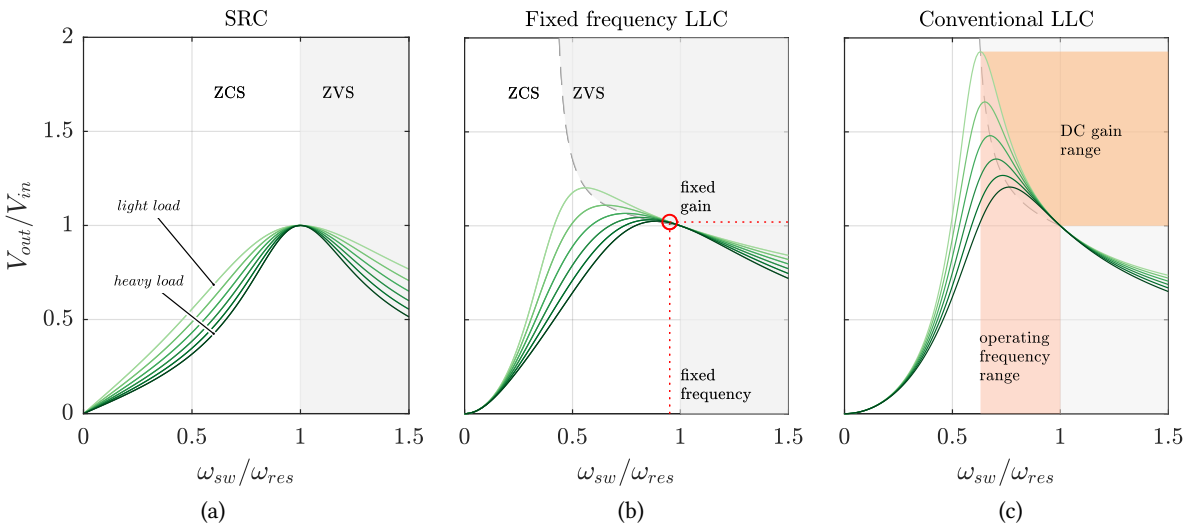


Figure 2.8 DC gain characteristic over the normalized switching frequency for SRC converter (a), fixed frequency LLC converter (b) and conventional LLC converter (c). A capacitive behavior of the resonant tank (left hand side of the peak gain) implies that the voltage lags on the resonant current which allows for a ZCS turn-off of the primary side semiconductor. At the opposite, an inductive behavior (right hand side of the peak gain, gray area) implies that the resonant current lags on the voltage, which allows for ZVS turn-on of the primary side semiconductors. The operation of the converter below the resonant frequency allows a discontinuous conduction mode (DCM) of operation that ensures soft switching on the secondary side but forces a capacitive behavior in the case of the SRC whose peak gain is at $\omega_{sw} = \omega_{res}$ for any load. In the case of the LLC converter, the displacement of the peak gain to the left thanks to the presence of the magnetizing inductance allows the converter to operate below the resonance frequency while remaining in the inductive area benefiting from ZVS. In addition, the fixed frequency operation allows a DC gain almost independent from the load, in contrast to the conventional LLC converter, which allows the DC gain to be varied with the switching frequency but becomes very sensitive to the load.

However, it is also possible to use an LLC converter in "DC transformer" mode by operating it at a fixed frequency and close to the resonant frequency (cf. **Fig. 2.8b**). In this case, the DC gain becomes quasi independent from the load and the tight coupling between input and output voltages is achieved,

as in the case of the SRC converter, while having the advantage of the ZVS. Even though phase shift control methods (needing therefore active rectification) or PWM modulation methods are feasible on the resonant stage [87]–[89], they go against the principle of load independent behavior offered by a DC-transformer. This is why, like the SRC topology, an LLC converter operated at a fixed voltage ratio requires an additional stage for the voltage regulation.

This additional stage introduces more complexity and losses but allows also a functional separation between the regulation stage and the isolation plus voltage adaptation stage which facilitates an optimal design of the components [90]. This is what the authors of [91], [92] propose with the concept of power electronic traction transformer (PETT). This SST concept dedicated to traction and consisting of an ISOP combination of submodules each including a DC transformer has been demonstrated at the industrial level with a MV prototype in [93]. Using nine submodules with 6.5 kV semiconductors, MV voltages of 15 kVac for a power of 1.2 MV A were achieved.

The authors of [94] demonstrate the use of an LLC converter in a bidirectional manner which shows its feasibility and its ZVS performances with a split resonant tank distributed on both the primary and the secondary of the MFT. The authors of [95] shows how to use a bidirectional LLC converter, but with a single tank. They prove the feasibility of such operation, but also point out of the higher switching losses in backward mode since the turn-off current (magnetizing current) is much higher on the low voltage side. In addition, the use of a full bridge for voltage control makes this solution less attractive, in terms of efficiency, than the basic DAB converter, for bidirectional use.

Nevertheless, the use of a fixed switching frequency implies the possibility of extending the concept to a multiport. As its frequency is common to all the ports and does not vary, the resonant tank can be distributed over several ports.

A three-port LLC converter was introduced in [97] and consists of a three-winding medium-frequency transformer with distributed resonant capacitors tuned to the leakage inductors to create a resonant tank. Each electrical port can be configured as a half or full bridge, and all ports are switched to the resonant frequency with the same phase and a duty cycle of 50%. The authors presented the configuration in which one port acts as a source, while two other ports act as a load. Experiments with a low power setup (300W) show good load self-regulation. In addition, the authors of [96] demonstrate

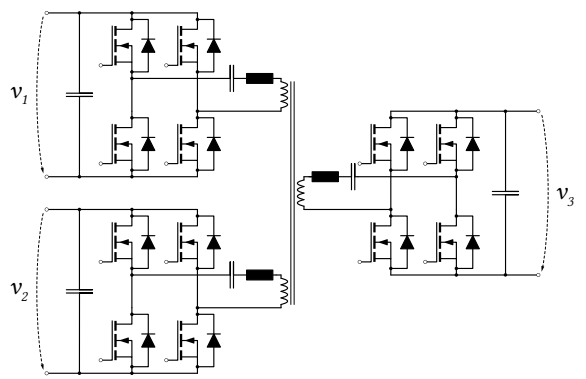


Figure 2.9 Multiport resonant converter such as considered in [96]. The resonant tank is split between the three sides.

the operation of a similar topology in both single-input-dual-output and dual-input-single-output modes and highlight the good ZVS capabilities over the full power range for these two operating modes.

In addition to the work presented in [98],the authors of [99] present a similar topology where two ports are configured as sources and are equipped with resonant capacitors, while the third behaves like a load and has only one rectifier. They demonstrated that it is possible to regulate the power flow and distribute the load between the sources by means of phase shift control but at the cost of the loss of part of ZVS capabilities.

In brief, the DAB structure has proven its performances and it controllability as isolation stage and voltage adaptation stage for DC-DC converters. This structure has been used first in multi-modular type of converters, resulting in the concept of SST, and second as a possible way to provide multiport conversion with the various MAB converters. Additionally the ISOP combination of multiple MAB has been explored with the cascaded half-bridge rectifier (CHBR-MAB) in [77] but remains feasible only in a single-input-single-output structure, without providing additional power ports. The **Fig. 2.10** gives an overview of the various converters based on the DAB structure.

On the other hand, the increased efficiency provided by the SRC or LLC structure and it simplicity of control when used in DC-transformer has lead to the development of multi-modular structures [91] and multiport SRC converters [96]. The MEG converter presented in this work is the multi-modular-multiport version of the LLC converter with the advantage, in relation to DAB based structures, to provide additional power ports, dedicated to storage elements. The **Fig. 2.11** summarizes multi-modular and multiport converters based on a resonant structure.

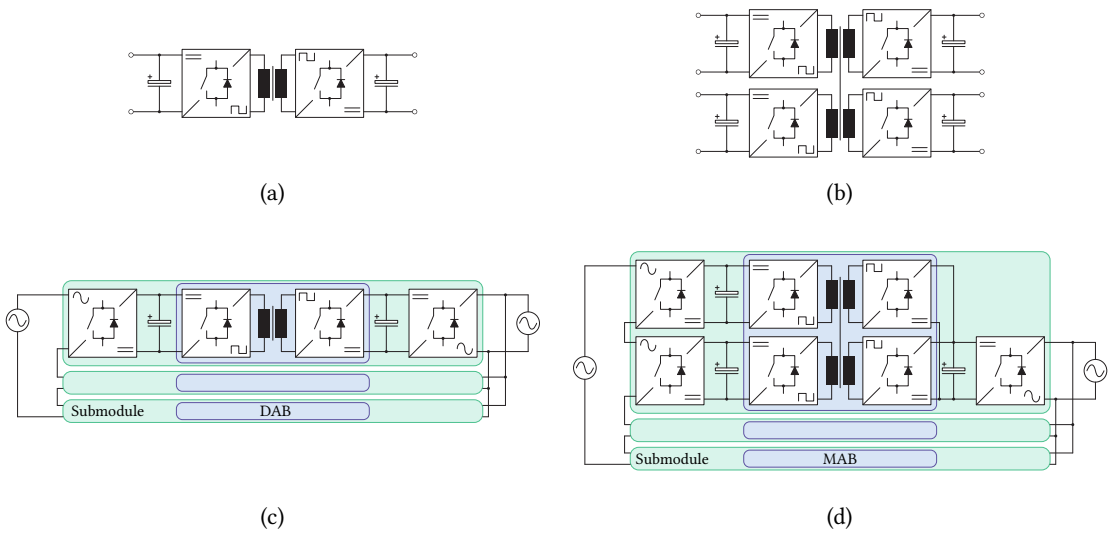


Figure 2.10 Various converters based on DAB structure. (a) basic DAB, (b) MAB: the multiport version of the DAB, (c) SST [67]: the ISOP version of the DAB, (d) CHBR-MAB [77]: the multiport-ISOP version of the DAB.

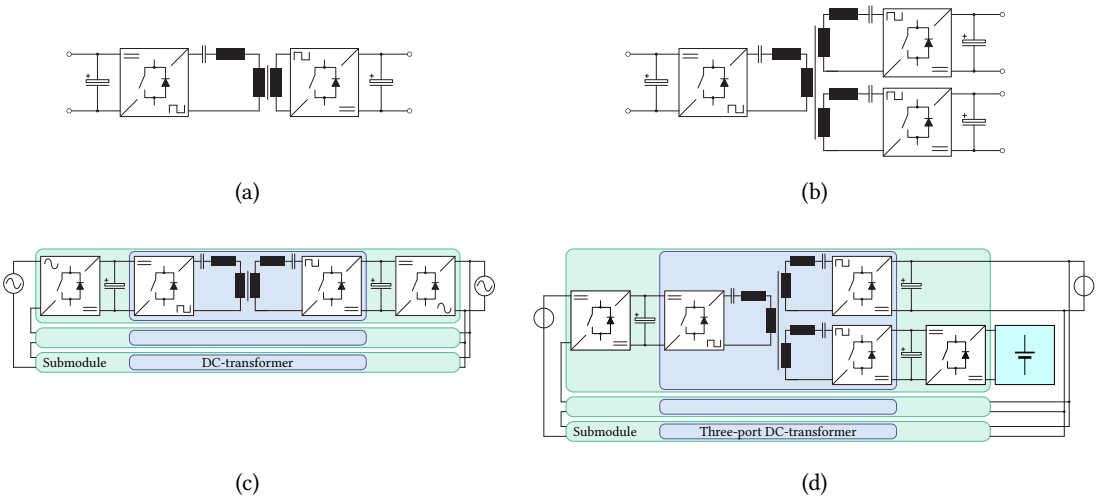


Figure 2.11 Various converters based on LLC structure. (a) SRC/LLC converter. basic structure of the DC transformer, (b) three-port resonant converter, (c) PETT [91]: the ISOP version of the DC-transformer, (d) proposed MEG: the multiport-ISOP version of the DC-transformer with integrated storage.

2.3 Basic switching cells topologies

The isolation stage, MFT or resonant stage are usually driven by two-levels or three-levels elementary converters which comprise the half-bridge (HB), the full-bridge (FB) and the neutral-point-clamped converter (NPC).

The first type, the half-bridge consists of two switches and two capacitors that can be arranged in two different ways: in series-output configuration, or split DC-bus configuration. In the first case, one of the capacitors sees all the voltage of the DC-bus and the other, placed at the output of the converter serves to filter the DC voltage and sees only half of the DC-bus voltage but is crossed by the entire current (cf. **Fig. 2.12a**). In the second case, both capacitors are placed in series and both see half of the DC-bus voltage as well as half of the current. For this reason this structure is preferable in high power applications, when voltages and currents are high and thermal stresses need to be well distributed (cf. **Fig. 2.12b**). In both cases, only two levels of voltages are possible at the output ($+V_{DC}/2$ and $-V_{DC}/2$) and the lack of substantial modularity is often compensated by a gain in efficiency when used in resonant structures.

The second type, the full-bridge (cf. **Fig. 2.12c**), requires four switches but no split DC-bus. It allows three output voltage levels $+V_{DC}$, $-V_{DC}$ and 0, when the current flows through one of the freewheeling diodes. This type of converter therefore allows a modulation controlled in duty cycle (including zero vector), and is commonly used in applications requiring pulsed modulation.

The third type, the neutral point clamped (NPC), is more complex since it includes four controlled switches with their anti-parallel diodes, two capacitors and two additional diodes (cf. **Fig. 2.12d**). Since the switches are configured in series, the structure can handle higher voltage levels for the same device blocking voltage, making it a popular converter in MV applications. This structure allows three output voltage level, $+V_{DC}/2$, $-V_{DC}/2$ and 0, or in other terms according to the switch configuration, $+V_{DC}$, $-V_{DC}$ and 0. The DC-bus voltage is equal to $2V_{DC}$ in comparison to the full-bridge.

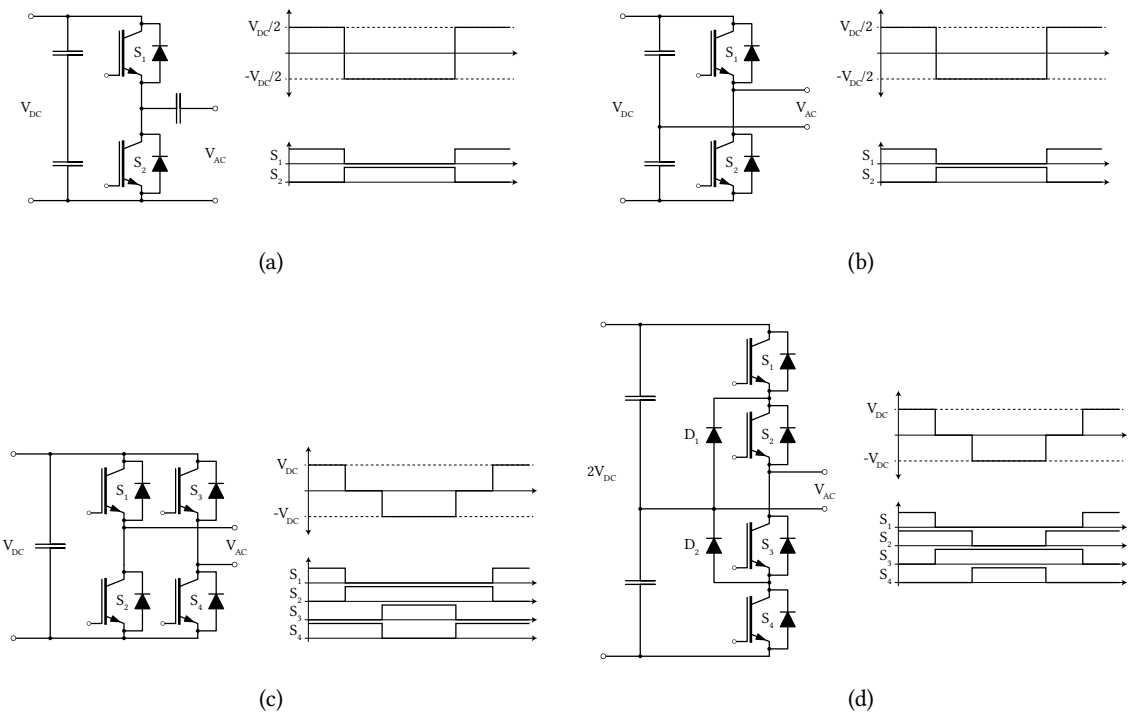


Figure 2.12 (a) Half-Bridge with series-output capacitor. (b) Half-Bridge with split DC-bus. (c) Full-Bridge. (d) Neutral Point Clamped.

A LLC converter operated as a DC-transformer needs only two levels modulation on the primary side, without any active rectification or phase shift/duty cycle control [100]. Thus, on the secondary side, the stage behaves as passive rectifier and, in terms of switching pattern, there is no difference between converters based on half-bridges (cf. **Fig. 2.13a**) or full-bridges (cf. **Fig. 2.13b**). Moreover, resonant circuits driven by a NPC stage have also been explored in [101], but only in order to decrease the voltage stress on the semiconductors.

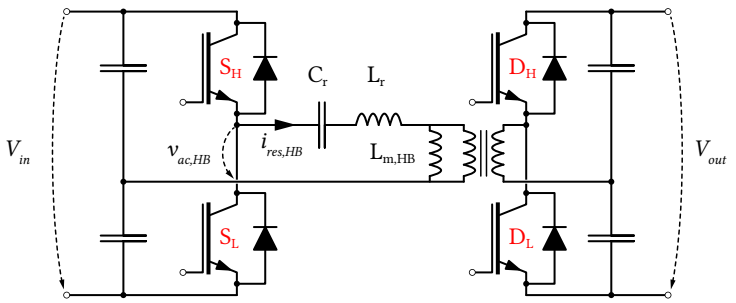
In the case of a full-bridge input stage, the full input voltage V_{in} is applied to the resonant circuit, instead of the half of it in the case of the half-bridge, which implies that the current (and its RMS value) is twice smaller for the same rated power for the half-bridge (cf. **Fig. 2.14**). The conduction losses may therefore be expected (at the level of the transformer) four times smaller considering a full-bridge (and twice at the level of the semiconductors, since the branch comprises two semiconductors an thus twice the junction voltage drop).

The switching losses are mostly relying on the turn off current i_{off} of the primary switches, and therefore relying on the magnetizing current (cf. **Fig. 2.15**). The soft switching condition (at the turn-on of those primary side switches) being influenced by the slope of the resonant current (see Chapter 4) which is slightly lower for a full-bridge converter, i_{off} may be also reduced, decreasing the switching losses per switch. But the full-bridge counts twice the number of semiconductors which increase the total amount of switching losses.

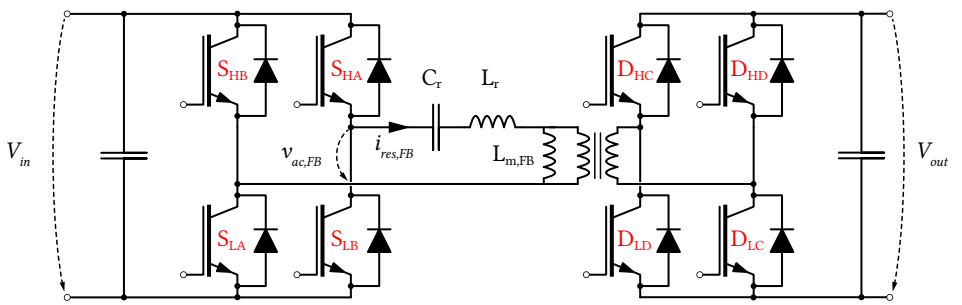
In other terms the uses of full-bridge decrease the conduction losses but increase the total switching losses. Only an overall optimization taking precisely into account the losses repartition on the

specific semiconductors would reveal the advantage of one topology or the other. Nevertheless, when considering DC-transformer, the limiting factor is the switching losses which increase with the frequency. Thus, in this case, full-bridges are of less advantage and half-bridges are usually adopted. This is even more true with high power semiconductors which switching losses are drastically higher than the conduction losses.

Considering the secondary side stage, used as passive rectifier, it is clear that the reduction of conduction losses thanks to a full-bridge is advantageous, since almost no switching losses affect this part. But in the case of a fully bidirectional converter, both side of the transformer are sized in order to be used as an active stage and therefore should follow above mentioned consideration. This is why, in the case of the MEG, all the ports are equipped with half-bridges.

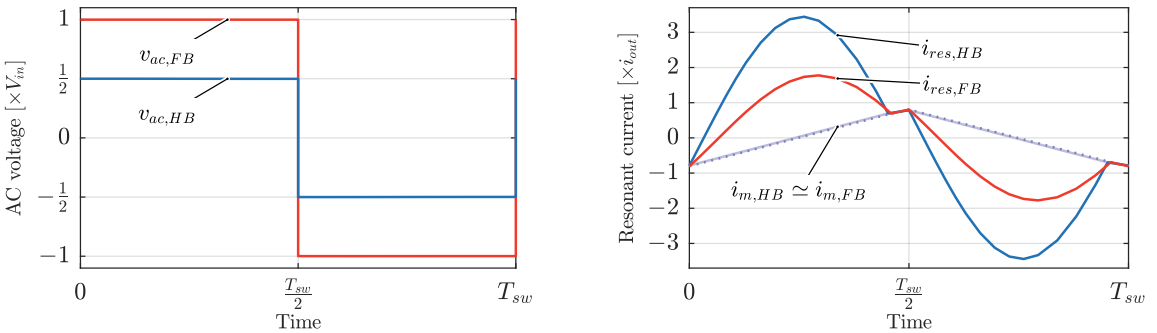


(a)



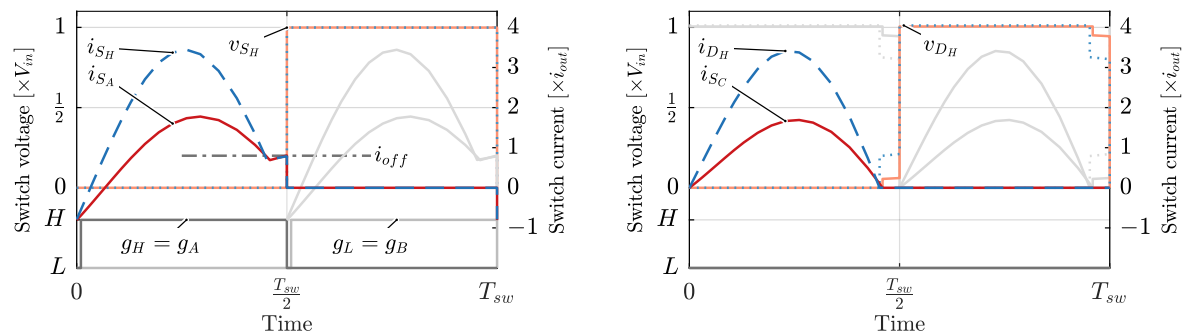
(b)

Figure 2.13 LLC converters driven by half-bridges (a) or full bridges (b). In both case, the secondary side semiconductors can be used as rectifier without active switching. In this case, only the diodes are considered.



(a) (b)

Figure 2.14 Comparison of the voltage applied to the resonant circuit (a) and the resonant current waveforms (b) driven by half-bridge converter (in blue) or full-bridge converter (in red). Both converter are operated at the same power and both resonant circuits are sized for the same magnetizing current (i.e. $L_{m,FB} = \frac{1}{2}L_{m,HB}$).



(a) (b)

Figure 2.15 Voltage and current across the semiconductors at a switching instant for the primary side switches (a) and the secondary side diodes (b). The waveform in the case of a half-bridge are in blue and the ones in the case of the full-bridge are in red. The gate signal g_H applied to the upper switch of the half-bridge converter is the same as the gate signal g_A applied to the branch A of the full bridge.

2.4 Semiconductors

In the case of a half-bridge operated resonant DC-transformer, the semiconductors of the secondary side of the transformer (or the multiple secondary sides in the case of a multi-port DC-transformer) may be used as a diode rectifier. Therefore, the current rating of the reverse diode must be equal to the current capacity of the transistor. In addition, the ISOP structure, comprising complex magnetic elements (MFT) in each submodule, a trade-off must be made between the number of stages and voltage class (blocking voltage) of the semiconductor [102]. A high number of submodules allows the use of relatively low class semiconductor but it results in a high volume due to the number of transformers. On the other hand, a reduced number of stages allows a reduced number of magnetics, but requires the use of high voltage semiconductors. In the case of a multiport DC-transformer, the magnetics part is even more important and a reduced number of stages and the use of high voltage

class semiconductors will therefore be encouraged. The aim being to study the feasibility of a structure using widespread market products, silicon device are preferred compared to wide-bandgap devices and the choice of semiconductor is made for IGBTs (see **Fig. 2.16**).

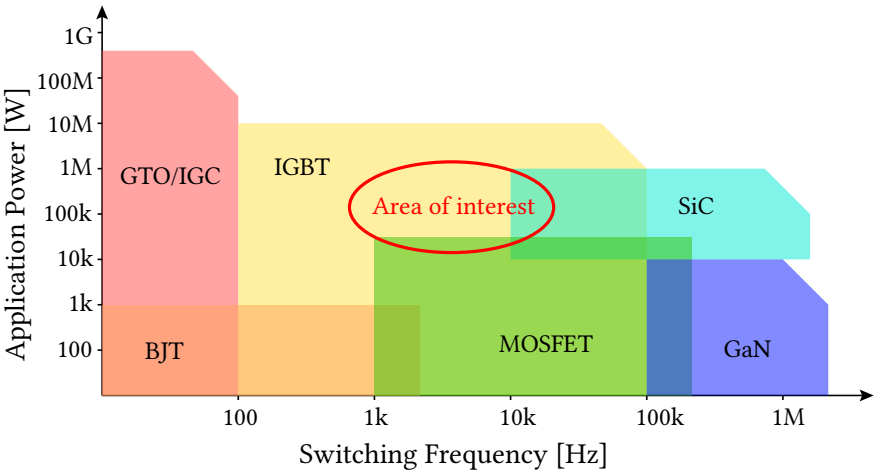


Figure 2.16 Area of use of the different semiconductors types in terms of switching frequency and power. The MEG is aiming for medium-frequency and **500 kW** range so IGBT technology seems the most adequate.

2.5 Discussion

The MEG concept, proposed in this thesis, incorporates the advantages of soft switching and tight voltage coupling of an LLC circuit. The principle is applied to a three-port MFT, two of which are equipped with an additional voltage regulation stage, thus forming a submodule with the characteristic of a three-port DC transformer. Several of these submodules are then combined in a multi-modular structure similar to PETT [91] benefiting this way from ISOP/IPOS stability [103] and hence offering an MV-low voltage (LV) interface integrating as well additional ports for energy storage elements. These additional ports can be used to connect either super-capacitors, or batteries, or a mix of both. In the case of a DC-transformer operated at a fixed frequency and with a constant 50% duty-cycle, only two-voltage-level converters are required. The basic switch topology adopted for the multi-port resonant converter is thus the half-bridge, reducing in this way the number of active components to a minimum. Finally, the targeted operating voltage and frequency lead the choice for an IGBT based converter. The detailed description of the proposed topology as well as its operation are presented in the next chapter.

3

Multiport Energy Gateway: topology and operating principles

This chapter introduces the topology, the functional blocks and the operating principles of the MEG converter. The complete converter is first presented and then the detailed structure of the submodules is explained. The operation of each functional stage is introduced and supported by open loop simulation results. Finally, the rating of the two sets of ratings used in the rest of the thesis, namely the low voltage prototype and the medium voltage converter are presented.

3.1 Converter structure

The MEG, shown in **Fig. 3.1**, is a multiport DC-DC converter, interfacing a MV grid, a LV grid, and integrating energy storage (ES) elements. To reach required voltage and power levels, a multilevel ISOP structure is adopted. An number N_s of identical submodules (c.f. **Fig. 3.2**) are connected in series on the MV side to handle the high voltage levels. They are connected in parallel on the LV side. The port dedicated to the ES of each submodule can be kept independent from the others and thus allow the connection to N_s separated ES elements. Alternatively they can also be combined in series or in parallel depending on the nature of the storage element(s) and their voltage and power levels.

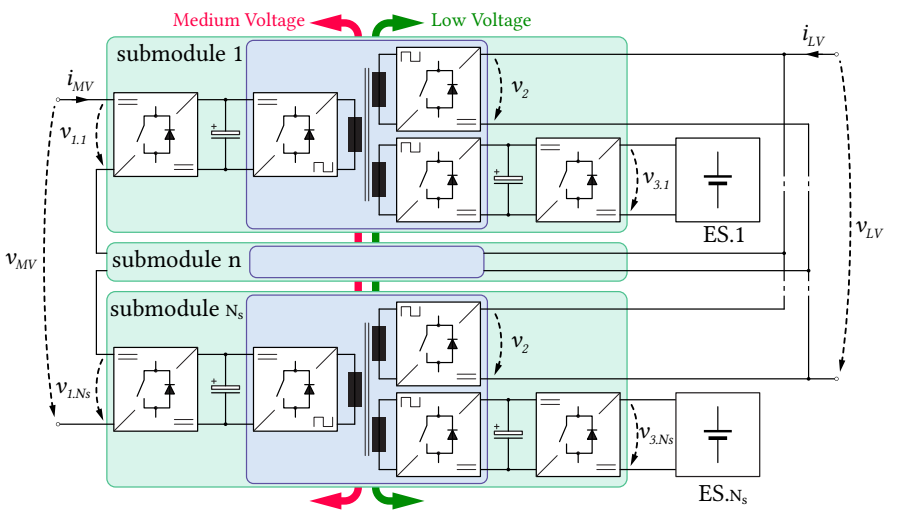


Figure 3.1 General structure of the MEG converter.

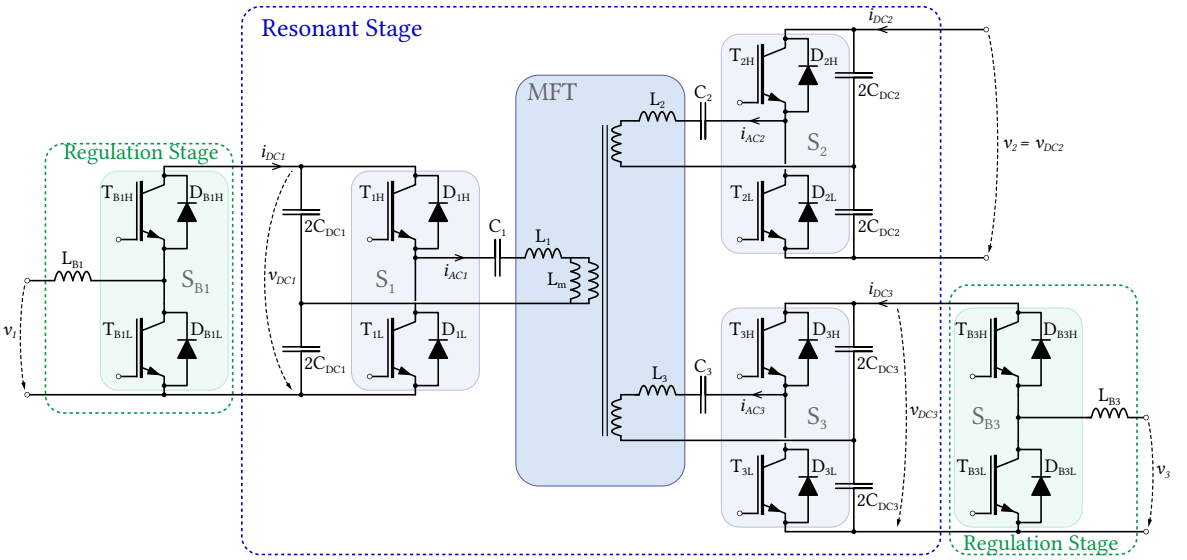


Figure 3.2 Detailed topology of one submodule of the MEG.

Regarding the nomenclature for the rest of this work, all that refers to the MV port is identified by the index x_{MV}, all that refers to the LV port by the index x_{LV}, all that refers to the storage port are identified using the $x_{ES.n}$ index with n in the range going from 1 to N_s.

3.2 Submodule structure

From a functional point of view, a submodule is divided into three stages having different tasks. Each submodule consists of:

- A **resonant stage** comprising a MFT with three windings, a resonant circuit distributed over the three ports and the three associated switching cells. This stage is only responsible for the galvanic isolation and the voltage adaptation. No active control feature is associated with this stage. Since it is behaving as a DC-transformer, the voltage v_{DC2} is following v_{DC1} and v_{DC3} with a DC-gain quasi load independent.
- A **regulation stage** on the MV port, comprising a switching cell and its inductor filter, responsible of the regulation of the power from/to the MV port through the precise control of v_{DC1} with the current i_{b1}.
- A **regulation stage** on the ES port, comprising a switching cell with an inductor filter, regulating the power from/to the storage element through the precise control of v_{DC3} with the current i_{b3}.

For the nomenclature at the submodule level, and to differentiate itself from the notation at the level of the whole converter, the elements concerning the MV port are referenced with the index x_1, the one for the LV port with the index x_2 and the ES port with the index x_3.

It has to be noted that only the functional structure is presented here. In practice, the implementation

of such converter would need additional safety stages. Indeed, the interruption of the power flow, for safety reason, can be stopped between the three sides (MV,LV, ES) by blocking the semiconductors. But, in order to protect the converter from short-circuit or over-voltage on the MV or the LV grid, the use of external breakers and short-circuit protections is needed.

The black-start of the converter would also need an additional switch. Indeed, one possibility is to consider a start-up sequence where the MV side is disconnected. The DC-buses of the resonant stage are gradually charged from the LV port. When the nominal voltage is reached, the MV port is then connected to the MV grid.

3.2.1 Resonant stage

The resonant stage consists of a MFT with three windings having a turn-ratio $n_1 : n_2 : n_3$ according to the three desired DC-bus voltages v_{DC1}, v_{DC2} and v_{DC3}. Each of the ports i of the MFT is equipped with a resonant tank made of a capacitor C_i combined with a resonant inductor L_i formed by the leakage inductance $L_{\sigma i}$ of the corresponding MFT winding and eventually an external physical component if required inductance cannot be achieved by the MFT alone. The resonant tank could have been located only on one or two ports of the MFT as presented in [97] and [96]. To benefit from a total bidirectionality on each of the ports, the resonant tank is distributed between each of the three ports so as to provide the similar resonant behavior whatever the configuration, as well with an unused port, and whatever the direction of the power flow. This implies that the resonant frequency f_r must be the same for the three resonant tank.

$$2\pi f_r = \omega_r = \frac{1}{\sqrt{L_1 C_1}} = \frac{1}{\sqrt{L_2 C_2}} = \frac{1}{\sqrt{L_3 C_3}} \tag{3.1}$$

This resonant frequency, common to the three ports, imposes an identical switching frequency f_{sw} for the three switching cells (S_1, S_2, S_3) and thus frequency control is not considered since it does not affect the power flow. or duty-cycle control are not considered. Moreover the LLC resonant structure benefits from soft switching (ZCS) on the secondary side thanks to the diode rectifier, so active rectification and phase-shift control seems to be in contrast with the primary purpose of this structure, even though they are possible [104]. This way, only two levels modulation is needed (such as mentioned in Chapter 2) and thus half-bridges structures are selected for S_1, S_2, S_3 are consisting of two IGBTs ($T_{i,H}$) and ($T_{i,L}$).

No control function is associated with this stage, except for the presence or the absence of switching action depending on the direction of the power flow. By convention, input powers are positive and output powers are negative (cf. equation (3.5)). When a port is active, (positive power), the corresponding switching cell is actively switched with a fixed switching frequency f_{sw} and a duty cycle of about 50% (slightly less, taking into account the dead times). When a port is passive (load, or negative power), its semiconductors are not activated and the switching cell acts as a passive diode rectifier. There are three possible modes of operation:

- **SISO** (*single input single output*): when only one port is a source, its switching cell is actively switched and only one port acts as a load and draws power. The third port neither injects nor consumes any power. Its DC bus is then charged to a voltage level that does not allow conduction through its rectifier (or very little, so as to cover the losses, such as the DC-bus leakage current only).

- **SIDO** (*single input dual output*): when one port is a source and supplies the other two. The input port switching cell is actively switched, while the semiconductors of the two load ports are used as passive rectifiers.

- **DISO** (*dual input single output*): When two ports see a positive power and a single port acts as a load. The switching cells of the two active ports are switched at the same times. The power consumed by the third port is equal to the sum of the power injected by the two active ports. In other terms, the power drawn by the load port is shared between the two sources. The proportion of each depends on the resonant circuit parameters as well as DC bus voltages and is described in details in Chapter 4.

Seen from the outside, this stage behaves like a DC-transformer allowing an isolated voltage adaptation between v_{DC1}, v_{DC2} and v_{DC3}. Apart from the presence or the absence of switching, only the voltages of the DC-buses affect the power flows, in the same manner as communicating vessels where the one with the highest level naturally fills the others. At the complete converter level, the N_s resonant stages are connected in parallel via their port 2 (LV side). Thus, in order to considerably reduce the ripple of the voltages on the concerned DC-bus, it is possible to introduce a phase shift of $\frac{2\pi}{N_s}$ between the carrier signals of each level. In this way, the converter benefits from an effective interleaving such as illustrated in **Fig. 3.3**.

3.2.1.1 Resonant frequency

This part has the particularity of linking two or three different voltage levels, which implies that the semiconductor class used on port 1 (3.3 kV-6.5 kV) is different from the one used on port 2 (1.2 kV-1.7 kV). Potentially, a third class of semiconductors can be considered on port 3 (600 V). Since the high-voltage semiconductors can usually be operated at a lower frequency than the semiconductor of the lower class, the choice of the switching frequency f_{sw}, and the corresponding resonant frequency f_r is therefore the result of a trade-off (cf. **Fig. 3.4**) taking in account, among others, the number of submodules, the minimum dead-time and the switching losses of the semiconductors of each side. Only an overall optimization considering the application specifications and the optimization targets cost, volume, weight and efficiency can highlight the best solution. This has not been done in the context of this thesis but the topic is discussed in Chapter 5.

3.2.2 Regulation stages

In order to control the power flow, the ports 1 and 3 are equipped with the additional switching cells S_{B1} and S_{B3} and corresponding inductor filters L_{B1} and L_{B3} (see **Fig. 3.2**). Depending on the direction of the power flow, they act either as a buck converter (the high-side transistor $T_{Bx,H}$ is actively switched and the low-side switch behaves as a passive diode $D_{Bx,L}$) or as a boost converter (only the low-side transistor is actively switched). The currents i_{B1} and i_{B3} can thus be controlled with the duty-cycle D_1 and D_3 in order to regulate the power from/to port 1 and port 3 respectively.

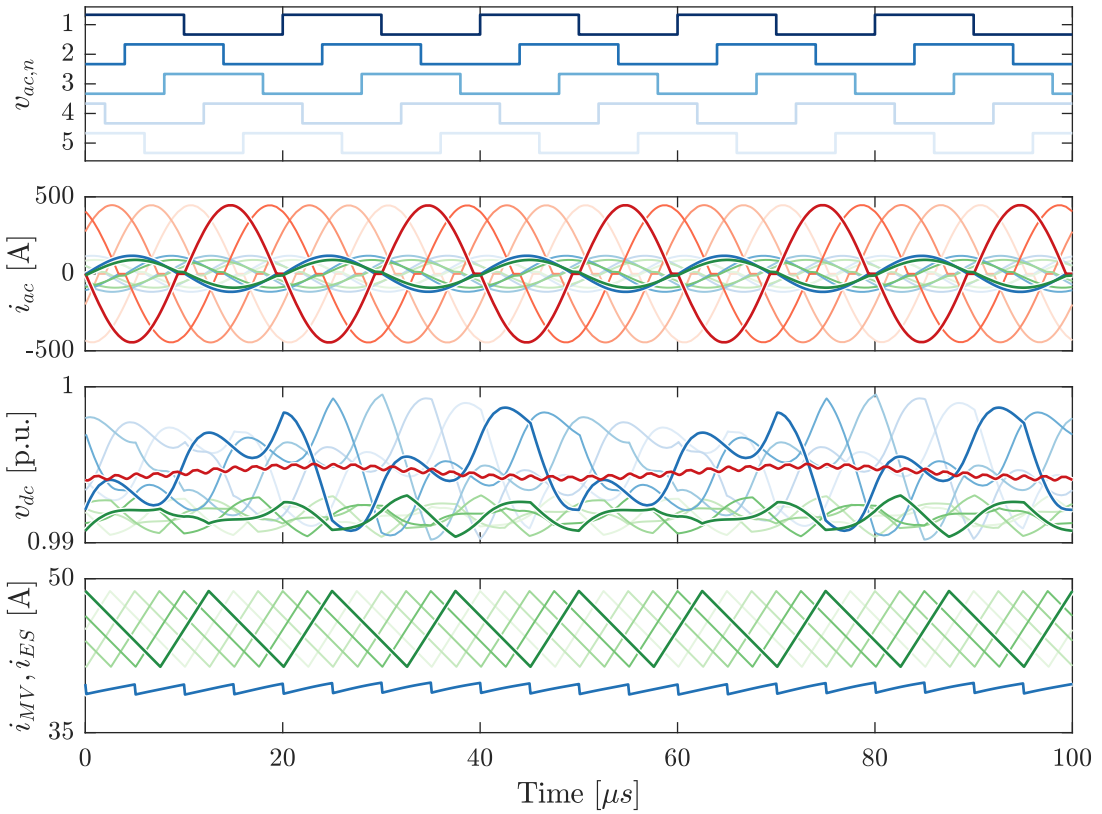


Figure 3.3 Typical voltage and current waveforms in the converter, in this case with 5 submodules, in open loop and DISO1 mode. The figure on top shows the square-wave voltage applied on the port 1 of the resonant stage of the 5 submodule. The signal of each submodule is shifted with a $2\pi/5$ angle. The second figure shows the resonant current in the port 1 (in blue), the port 2 (in red) and the port 3 (in green) for each submodule. The interleaving of the resonant stage allows to reduce considerably the ripple on the output voltage, as shown in the third figure which shows the voltage of each DC-bus reported to their nominal value (port 1 in blue, port 2 in red and port 3 in green). The bottom figure shows the current of the stacked boost stage on the MV port (i_{MV}, according to **Fig. 3.1**, in blue) and the five currents though the storages side regulation stages (i_{ES} in green). The ripple on the MV side current is also considerably decreased thanks to the interleaving of the stacked boost stage. A comparison with the case without interleaving is presented in the Chapter 5.

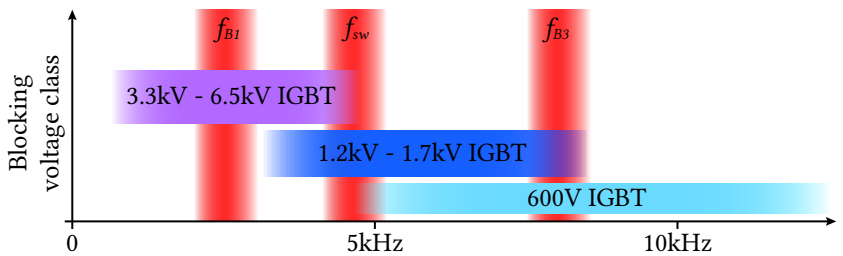


Figure 3.4 Switching frequency range.

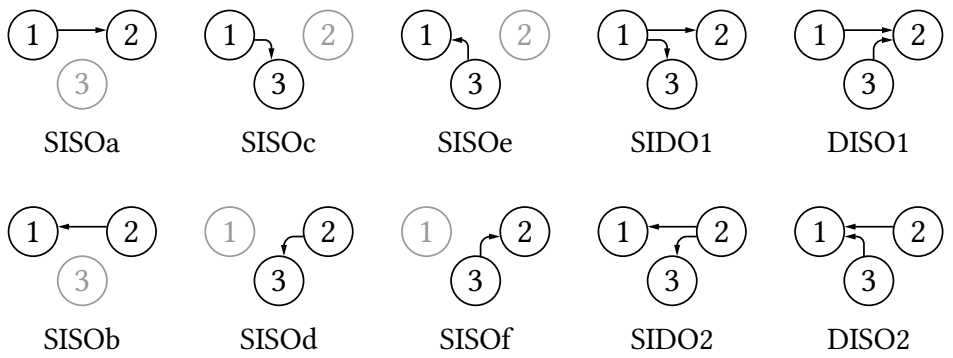


Figure 3.5 Operating modes of a MEG submodule.

Table 3.1 Operating Modes

Mode	S_1	S_2	S_3	S_{B1}	S_{B3}
SISOa	Active	Passive	Passive	Boost	Off
SISOb	Passive	Active	Passive	Buck	Off
SISOc	Active	Passive	Passive	Boost	Buck
SISOd	Passive	Active	Passive	Off	Buck
SISOe	Passive	Passive	Active	Buck	Boost
SISOf	Passive	Passive	Active	Off	Boost
SIDO1	Active	Passive	Passive	Boost	Buck
SIDO2	Passive	Active	Passive	Buck	Buck
DISO1	Active	Passive	Active	Boost	Boost
DISO2	Passive	Active	Active	Buck	Boost

3.2.2.1 Modes of operation

The operating modes of the regulation stages are associated with the direction of the power flow and are therefore related to the mode of operation of the resonant stage (see **Fig. 3.5**). A summary of these modes is given in Table 3.1.

The application aimed by the MEG converter is the support of a main power flow between two grids (MV and LV) using the storage port. In this sens, two main scenarios are considered. The first when the LV grid is acting as a load and is supplied from the MV grid. In the nominal operation, the storage port is in standby (mode *SISOa*). In the case of sudden peaks of consumption on the LV side, the power is compensated by the storage port (in the mode *DISO1*), while in the case of sudden drops of consumption, the excess of power from the MV side is absorbed by the storage port (mode *SIDO1*). The second scenario is when the LV grid is injecting power to the MV grid. The nominal operation is in the mode *SISOb*. Any drops of production on the LV side is compensated by the storage (in mode *SIDO2*) while any peaks of production are absorbed by the storage (in the mode *DISO2*).

The access to the storage port is insured also in degraded mode, when one of the two grids is out of

service. The storage element can be charged or discharged with either the MV port or the LV port completely disconnected with the modes *SISOd*, *SISOf* and respectively *SISOc*, *SISOe*.

Even though all the cases of power flow between the three ports are technically possible, the case where the storage is discharged into both grids and the case where the storage is charged from the two grids are not taken into account because they are not relevant in terms of application. Considering an application where the storage port is used only as a support of the main power flow, the power ratings of this third port are reduced compared to the main ports (ports 1 and 2). In this case, the storage could be used only with a reduced power and for a short amount of time (considering reduced energy capacity of the storage elements) which does not reflect any sustainable situation. Therefore, the modes *SIDO3* and *DISO3* are not considered.

3.2.2.2 Switching frequency

Unlike f_{sw} which results from a compromise between the three ports, the choice of the frequency f_{B1} and f_{B3} is independent and can be subject to an overall optimization of the converter. Indeed, f_{B1} and f_{B3} are chosen according to voltage class of the selected semiconductor technologies to minimize losses associated with S_{B1} and S_{B3} (c.f. **Fig. 3.4**).

At the level of the entire converter, the regulation stage of the port 1 of the N_s submodules are connected in series and share the same current i_{MV} (cf. **Fig. 3.6**). The N_s cells S_{B1} are therefore switched with a duty cycle D_1 common to all the submodules. A phase shift of $\frac{2\pi}{N_s}$ can also be introduced between the N_s carriers, with the effect of reducing the voltage seen by the inductors L_{B1} and thus reducing the current ripple on i_{MV} (or, reciprocally, the size of the L_{B1} needed a given ripple specification).

The converter does not need any active balancing of MV side voltages. Indeed, thanks to the ISOP structure and the fixed-frequency operation of the resonant stage, the DC-bus on the MV side are seen as connected together through a low impedance and therefore benefit from a natural self balancing [105], [106]. It has to be noted that if the LV side ports are not connected in parrallel, a common voltage cannot be imposed to all the submodule which could lead to the lost of the power balancing and consequent lost of stability.

Even if a practical realization will inherently produce a certain deviation of the components from the expected/designed values, as long as these are within a certain margin, the balancing is maintained, only at the cost of a circulation of power between the different submodules. Thanks to this same property, it is possible to charge a storage element at the same time as the discharge of another ES element. In other words, it is possible to operate the different submodules simultaneously in different modes, but only under certain conditions which are described in details in the chapter 6.

The powers from/to each ports are defined as in (3.2) to (3.4)

$$P_{MV} = v_{MV} i_{MV} = i_{MV} \sum_{n=1}^{N_s} v_{1.n} \tag{3.2}$$

$$P_{LV} = v_{LV} i_{LV} = v_{LV} \sum_{n=1}^{N_s} i_{2.n} \tag{3.3}$$

$$P_{ES} = \sum_{n=1}^{N_s} P_{3.n} = \sum_{n=1}^{N_s} v_{3.n} i_{3.n} \tag{3.4}$$

with the condition (in the ideal lossless case) of (3.5).

$$P_{MV} + P_{LV} + P_{EV} = 0 \tag{3.5}$$

3.2.2.3 Power ratings

Finally, to illustrate the theoretical developments of this work, the simulations are based on a case study of a converter interfacing a 10 kV medium-voltage grid, a 750 V low-voltage grid for a power of 0.5 MW. The storage elements are designed for a reduced power (20% of the nominal power) and work between 200 V and 450 V. Table **3.2** summarizes the ratings at the converter level and the ratings at the submodule level.

Table 3.2 Converter and submodule ratings

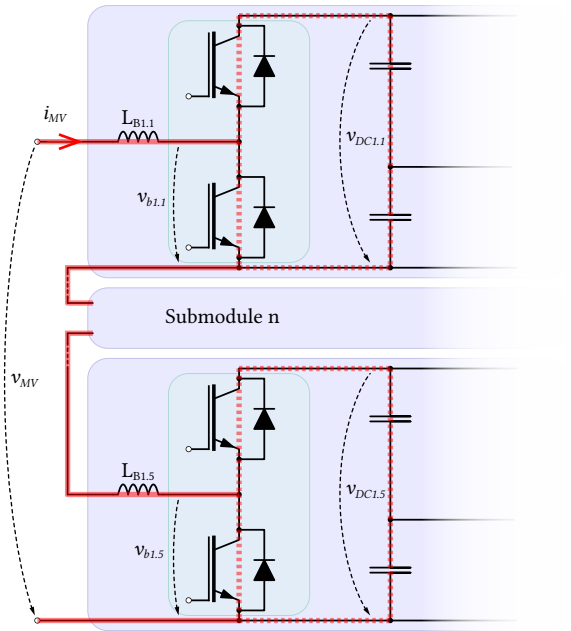
Port i	P_i	v_i	i_i
MV	500 kW	10 kV	50 A
LV	500 kW	750 V	750 A
ES	100 kW	450 V	500 A

Port k	P_k	v_k	v_{DCk}	i_k
1	100 kW	2 kV	2.5 kV	50 A
2	100 kW	750 V	750 V	150 A
3	20 kW	450 V	750 V	100 A

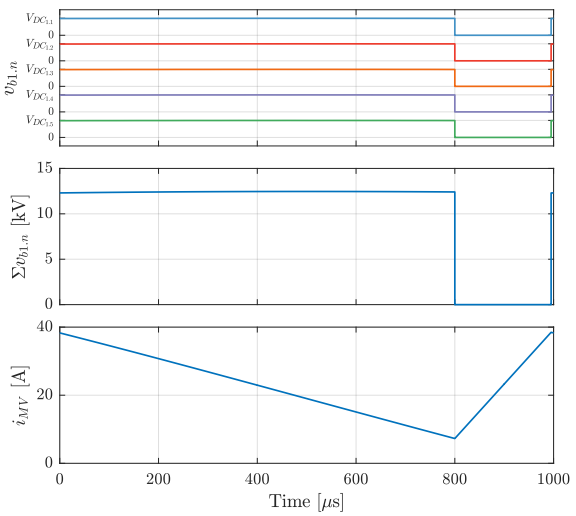
The experimental results are obtained using a low-voltage prototype of a single submodule, described in the Appendix B and its ratings are given in Table **3.3**.

Table 3.3 Low voltage prototype ratings

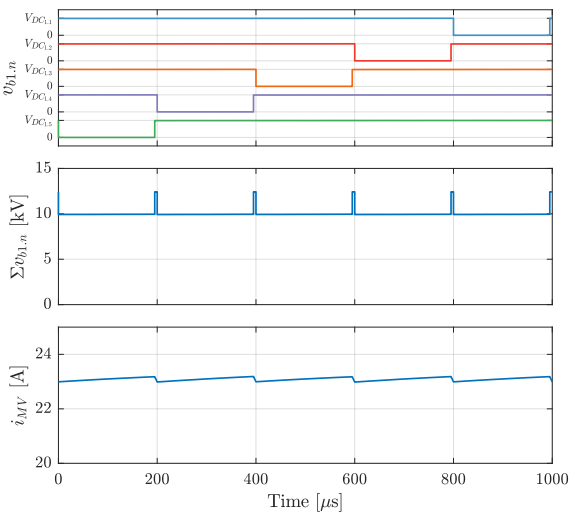
Port k	P_k	v_k	v_{DCk}	i_k
1	10 kW	200 V	360 V	50 A
2	10 kW	360 V	360 V	28 A
3	5 kW	200 V	360 V	50 A



(a)



(b)



(c)

Figure 3.6 (a) Structure of the stacked regulation stages of the MV port. L_{B1} is the sum of the five $L_{B1.n}$. (b) Waveforms without interleaving of the voltage $v_{b1.n}$. (c) Waveforms with interleaving. It should be noticed that the current ripple is drastically descreased thanks to the interleaving, first because the apparent frequency is multiplied by five and second because the voltage applied to L_{B1}, namely $v_{MV} - \Sigma v_{b1,n}$ is divided by five.

3.3 Discussion

This chapter presents the topology, its functional blocks and its operating principle. Each stage is divided in three functional blocks, including a resonant stage that make the link between the three ports, performs the voltage adaptation, provides galvanic isolation and including as well two additional control stages which purpose is to regulate the power of the MV and ES ports. This separation of the functions allows for further optimization of each stage in terms of component sizing and switching frequency according to their respective power and voltage ratings. The operation of the converter is divided into ten different modes based on the direction of the power flow. The main difference between the modes is essentially the number of active/passive ports for the resonant stage and the buck or boost operation for the control stages. Thus only the ports that supply power are actively switched, the other acting as passive diode rectifier with the aim to limit the switching losses. Theoretically the different modes can applied independently to each submodule with the only restriction that the mode of S_{B1} has to be the same for all the submodules. For instance one submodule can be in SIDO1 mode while another submodule is in DISO1 mode and the rest is in SISOa mode. At the opposite, the case of one submodule in SIDO1 mode and the other in SIDO2 mode would lead to an instability and is therefore not allowed. This implies that in the case of a simultaneous charge/discharge of several storage elements, the main power flow between the MV and the LV ports has to be greater than the circulating power between the storage elements.

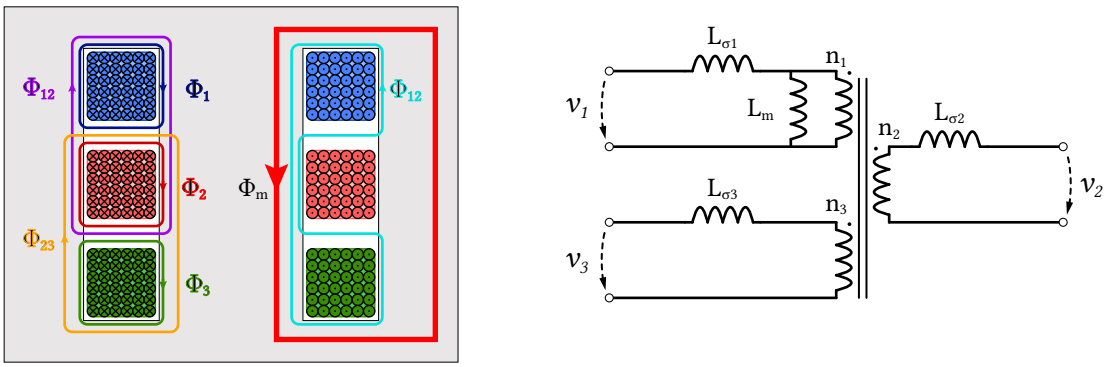
4

Modeling of the three-port resonant converter

This chapter proposes a model of the resonant stage developed to approximate the waveforms of the currents and the voltages in each of the operating modes of the converter. The natural power sharing characteristics, i.e. in absence of any control loops, is highlighted by the proposed model which also provides the level of detail necessary for the description and the characterization of the soft switching operation region. It, therefore, gives an insight of the efficiency over the operating range. It also makes it possible to highlight certain conditions on the circuit parameters required for the soft switching operation, that will be used as design rules in Chapter 5.

4.1 Model of the resonant stage

As described in the previous chapter, the essential part of a MEG submodule is the multiport resonant stage. The literature mentions the feasibility of such principle [96], [97] but no detailed model is described. Since the resonant stage is operated in open loop, the power flow and its sharing between the three ports has to be characterized in function of the parameters of the circuit and the voltages that are applied to it. Standard (bi-port) LLC converters are commonly used for DC-DC conversion with a wide voltage range [82], [107], [108]. Thus, the models mentioned in the literature mainly focus on the description of the DC gain as a function of the switching frequency and the load conditions. The analysis method, commonly used and referenced as first harmonic approximation (FHA)[109], considers only the main harmonic of the excitation voltage applied at the primary side and compares the resonant circuit to a bandpass filter assuming, for the sake of simplicity, its response at the switching frequency only. This method gives a good approximation of the power flow and makes it possible to characterize roughly the soft switching operation range but it lacks precision when it comes to the description of the currents and the voltages waveforms. Moreover, in the case of the application of a DC-transformer-alike resonant converter, the switching frequency is not only fixed, but also very close to the resonant frequency. At this frequency, the DC-gain is very close to 1 and the effects of the load conditions are very small. So the information that can be drawn from the FHA model is not sufficient. To analyze the soft switching operating range, the semiconductors turn-off currents and the timing of the zero crossings are important (see section 4.5). Thus, a more precise model providing this level of details is needed. In addition, a multiport system will undeniably involve a circulating power that will influence this soft switching region and also will require detailed modeling of the circulating currents. This is why the chapter presents the description of the current waveforms in each mode and for the complete operation range.



(a) (b)

Figure 4.1 Magnetic flux of a three-winding MFT (a) and equivalent 'T' model (b).

4.2 Three winding transformer

The detailed modeling of the MFT with three windings is not in the scope of this thesis. Thus, the model of the transformer used in this study is based on the 'T' model presented in [110]. According to [111], the study of the total magnetic fluxes of a transformer as represented in **Fig. 4.1a**. leads to a complete model that takes into account the coupling of each winding between them, which is tightly depending on the geometry of the core and the windings. Nevertheless, once these coupling coefficients are known (by measurements or FEM simulations), the model can be simplified according to [110] to obtain the 'T' model as presented in **Fig. 4.1b** and presenting only five parameters, namely the turn ratio ($n_1 : n_2 : n_3$), the magnetizing inductance seen from one on the port L_m and the three leakage inductance corresponding to each port, $L_{\sigma 1}$, $L_{\sigma 2}$, $L_{\sigma 3}$. For the rest of this work, it is assumed that any magnetizing inductance or leakage values can be obtained either directly through the design of the windings or by the addition of external inductors. So the model of the transformer used is limited to the parameters L_1 (comprising $L_{\sigma,1}$ and eventual external inductor), L_2, L_3 and L_m without going into more details (see **Fig. 4.2**).

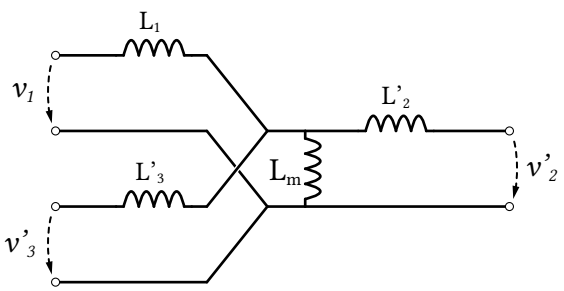


Figure 4.2 Equivalent circuit of a three-winding MFT as used to model the MEG converter. The leakage inductances $L_{\sigma 2}$ and $L_{\sigma 3}$ are reported to the primary taking into account the turn ratios.

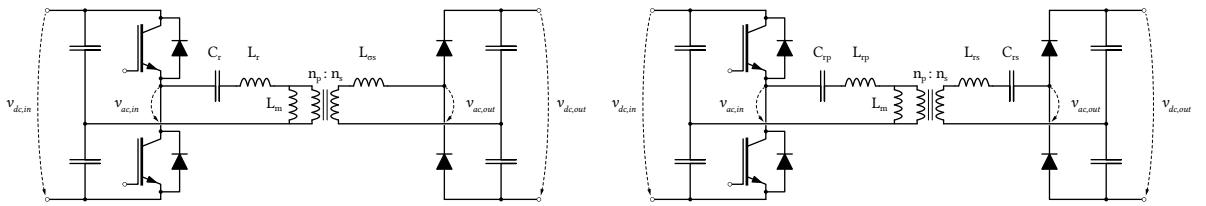


Figure 4.3 LLC converters with a single resonant tank (a) or a split resonant tank (b).

4.3 LLC Resonant Converter

The first mode to be analyzed is the simplest case, when the power is flowing only between two ports. In this single-input-single-output (SISO) mode, the DC-bus of the inactive port is charged up to the voltage which blocks its rectifier for the entire switching period. Even though in practice the DC-bus leakage current would imply a short conduction to maintain this voltage, the port is considered as completely disconnected from the system and can be neglected. In this case, only one port is actively switched and one port is a passive rectifier. The behavior of the converter is the same as a standard bi-port LLC converter, which is described in the following section.

The basic structure of the bi-port LLC converter described here is composed of following main elements:

- On the primary side, an active switching cell (half-bridge) which generates an AC-voltage $v_{ac,in}(t)$ characterized by its switching frequency f_{sw} and its amplitude imposed by the input DC-bus voltage $v_{dc,in}(t)$.
- On the secondary side, an output DC-bus characterized by its voltage $v_{dc,out}(t)$ and supplied by the current from the resonant circuit $i_{out}(t)$ rectified by a passive diode rectifier.
- A MFT with the turn ratio $n_p : n_s$ and its magnetizing inductance L_m seen from the primary. It is equipped with either a single resonant tank (cf. **Fig. 4.3a**) characterized by the resonant elements L_r and C_r or a split resonant tank (cf. **Fig. 4.3b**) characterized by the resonant elements located on the primary $L_{r,p}$, $C_{r,p}$ and on the secondary $L_{r,s}$, $C_{r,s}$. In the case of a single resonant tank, a leakage inductance L_σ has to be considered on the secondary.

Both configurations, with a single resonant tank or a split resonant tank are depicted in **Fig. 4.3**.

The circuits of **Fig. 4.3** can be both simplified to an equivalent circuit, depicted in **Fig. 4.4** where the element of the secondary side are reported to the primary side according to the method presented in [112], further referred as "T-shape to Γ-shape transformation". The transformer turn ratio n is given by (4.1).

$$n = \frac{n_p}{n_s} \tag{4.1}$$

The transformation coefficient γ is defined as (4.2) for the single tank converter (cf. **Fig. 4.3a**) and as

(4.3) for the split tank converter (cf. **Fig. 4.3b**).

$$\gamma = \frac{L_m}{L_m + L_{\sigma s}} \tag{4.2}$$

$$\gamma = \frac{L_m}{L_m + L_{r,s}} \tag{4.3}$$

So L'_m, the magnetizing inductance seen from the primary side taking into account the effect of the secondary side impedance, is given by (4.4).

$$L'_m = \gamma L_m \tag{4.4}$$

Finally, the resonant components of both sides are reported to the primary and combined together to make an equivalent circuit. It includes a transformed resonant inductor L'_r and a transformed resonant capacitor C'_r. In the case of the single resonant tank (cf. **Fig. 4.3a**), L'_r is the resonant inductor L_r combined with the leakage inductor of the secondary side $L_{\sigma s}$ reported to the primary through the transformation, while C'_r is not affected by the presence of any capacitor from the secondary side (4.5).

$$\begin{aligned} L'_r &= L_r + \gamma L_{\sigma s} n^2 \\ C'_r &= C_r \end{aligned} \tag{4.5}$$

In the case of the split resonant tank (cf. **Fig. 4.3b**), the resonant components of the secondary side $L'_{r,s}$ and $C'_{r,s}$ have to be first reported to the primary side through (4.6).

$$\begin{aligned} L'_{r,s} &= \gamma n^2 L_{r,s} \\ C'_{r,s} &= \frac{C_{r,s}}{\gamma n^2} \end{aligned} \tag{4.6}$$

They are then combined with $L_{r,p}$ and $C_{r,p}$ with (4.7).

$$\begin{aligned} L'_r &= L_{r,p} + L'_{r,s} = L_{r,p} + \gamma n^2 L_{r,s} \\ C'_r &= \frac{C_{r,p} C'_{r,s}}{C_{r,p} + C'_{r,s}} = \frac{C_{r,p} C_{r,s}}{\gamma n^2 C_{r,p} + C_{r,s}} \end{aligned} \tag{4.7}$$

And the output voltages are also reported to the primary using (4.8).

$$\begin{aligned} v'_{ac,out} &= n\gamma v_{ac,out} \\ v'_{dc,out} &= n\gamma v_{dc,out} \end{aligned} \tag{4.8}$$

It may be noted that usually, in the design of SRC converters or LLC converters, the resonant inductors L_r or the leakage inductances L_σ are often chosen considerably smaller than the magnetizing inductance. This implies that γ is very close to 1 , and may be neglected. It may also be noted that in the case of the split tank, with the condition that the resonant frequency is the same on both primary side ($\omega_{r,p}$) and secondary side ($\omega_{r,s}$), the resulting resonant frequency ω'_r is also the same.

$$L'_r C'_r = L_{r,p} C_{r,p} = L_{r,s} C_{r,s} \implies \omega'_r = \omega_{r,p} = \omega_{r,s} \tag{4.9}$$

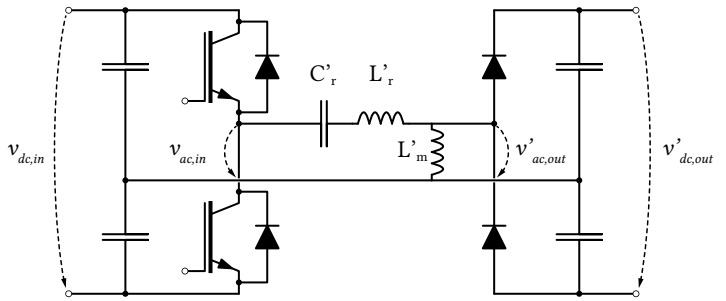


Figure 4.4 Transformed LLC converter equivalent, considering the same ground for both sides of the converter.

This means that for a given design of L'_r and corresponding C'_r, as long as the frequencies of the sub-tanks respect the equality (4.9), the splitting of the resonant elements and their distribution on each side of the transformer can be done arbitrarily.

For this circuit, typical voltage and current waveforms are depicted in **Fig. 4.5**.

Four main intervals, or two intervals per half switching period are then identified, the other two being similar but with opposite polarity. The two intervals of the half switching period are:

- The resonant pulse interval (*RP*) during which the rectifier of the secondary is conducting. The energy transfer to the secondary is performed during this interval. This interval can be decomposed into two subintervals: RP_d, from $t = 0$ to $t = t_1$, when the primary current is negative and flows through the anti-parallel diode and the interval RP_i, from $t = t_1$ to $t = t_2$, when the current is positive and goes through the active device. When the output resonant current reaches zero, at $t = t_2$, the diode rectifier stops conducting and the next interval starts.
- The non-conduction interval (*NC*) during which the secondary rectifier is blocked. The secondary side is disconnected from the primary and no active power is transferred. Only the magnetizing current is present in the circuit.

An equivalent circuit can be identified for each of the intervals. They are depicted in **Fig. 4.6**. It may be noticed that considering ideal switches, and thus neglecting both forward voltages of the diode and the IGBT, the equivalent circuit for the intervals RP_d and RP_i are identical. Moreover, since the capacitors of the DC bus are designed much larger than the resonant capacitors, the input voltage $V_{DC,in}$ may be considered as constant over the switching period. The voltage $v_{ac,in}(t)$ applied to the resonant tank is considered as a square wave voltage source:

$$v_{dc,in}(t) \approx V_{dc,in} \tag{4.10}$$

$$v_{ac,in}(t) = \operatorname{sgn}\left(\sin\left(\omega_{sw} t\right)\right) \frac{V_{dc,in}}{2} \tag{4.11}$$

By inspection of **Fig. 4.6a**, the circuit differential equations are given in (4.12), (4.13) and (4.14) for the interval *RP*. Applying Kirchhoff law on the input loop gives (4.12).

$$0 = -\frac{V_{dc,in}}{2} + \frac{1}{C_r}\int i_{in}^{RP}(t)dt + L_r\frac{di_{in}^{RP}(t)}{dt} + R_s i_{in}^{RP}(t) + v_{L_m}(t) \tag{4.12}$$

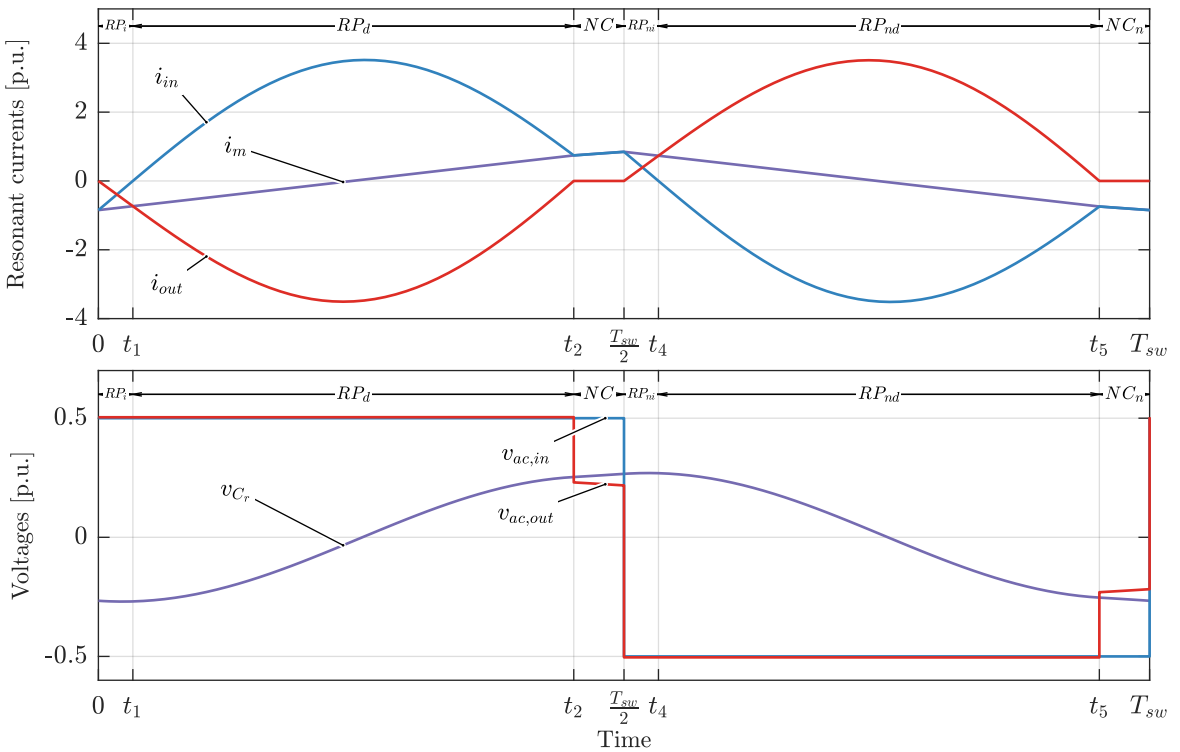


Figure 4.5 SISO mode: typical voltage and current waveforms and corresponding sub-intervals.

Applying Kirchhoff law on the output loop gives (4.13), where the voltage applied to the magnetizing inductor is the output voltage.

$$0 = -\frac{V_{dc,out}}{2} + v_{L_m}(t) \tag{4.13}$$

With $v_{L_m}(t)$ coupling both input and output loops through (4.14)

$$v_{L_m}(t) = L_m \frac{di_m^{RP}(t)}{dt} = L_m \left(\frac{di_{in}^{RP}(t)}{dt} + \frac{di_{out}^{RP}(t)}{dt} \right) \tag{4.14}$$

The initial condition (at $t = 0$) are defined in (4.15).

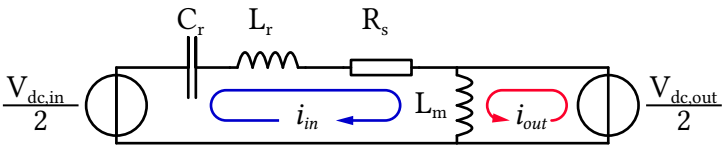
$$\begin{aligned} i_{in}^{RP}(0) &= i_m^{RP}(0) \\ i_{out}^{RP}(0) &= 0 \end{aligned} \tag{4.15}$$

The solutions of the system (4.12) to (4.14) results in (4.16). The input current, given by (4.16), is a damped sinusoid with the damping factor α_{RP} and the resonant frequency ω_{RP} as defined by (A.4) in the appendix A.

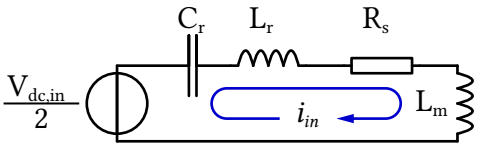
$$i_{in}^{RP}(t) = e^{-\alpha_{RP}t} \left(i_m^{RP}(0) \cos\left(\omega_{RP}t\right) + \frac{(V_{dc,in} - V_{dc,out} - v_{C_r}^{RP}(0) - R_s i_m^{RP}(0)/2)}{L_r \omega_{RP}} \sin\left(\omega_{RP}t\right) \right) \tag{4.16}$$

The magnetizing current is a linear function of the time depending on the output voltage (4.17).

$$i_m^{RP}(t) = i_m^{RP}(0) + \frac{V_{dc,out}t}{2L_m} \tag{4.17}$$



(a)



(b)

Figure 4.6 equivalent circuits for interval RP (a) and interval NC (b).

The output current $i_{out}^{RP}(t)$ is given by (4.18).

$$i_{out}^{RP}(t) = i_{m}^{RP}(t) - i_{in}^{RP}(t) \tag{4.18}$$

The initial conditions ($i_{m}^{RP}(0)$ and $v_{C_r}^{RP}(0)$) are dependent on the load conditions (namely the operating power and voltage). The length of the interval *RP*, being defined by the zero crossing of the output current (4.19) depends also on the load conditions which makes its exact calculation not explicit.

$$i_{out}^{RP}(t_1) = 0 \tag{4.19}$$

For the interval *NC*, the circuit differential equations are given by (4.20) and (4.21). The input voltage is applied to the resonant tank in series with the magnetizing inductor.

$$v_{ac,in}^{NC}(t) = \frac{V_{dc,in}}{2} = v_{C_r}^{NC}(t) + L_r \frac{d i_{in}^{NC}(t)}{dt} + R_s i_{in}^{NC}(t) \tag{4.20}$$

And the current charges the resonant capacitor.

$$i_{in}^{NC}(t) = C_r \frac{d v_{C_r}^{NC}(t)}{dt} \tag{4.21}$$

Considering the initial conditions $i_{in}^{RP}(t_1)$, this leads to the solutions in (4.22) with an output current equal to zero, since the rectifier is in blocking state.

$$\begin{aligned} i_{in}^{NC}(t) &= e^{-\alpha_{NC}(t-t_1)} \left(i_{in}^{RP}(t_1) \cos\left(\omega_{NC}(t-t_1)\right) + \frac{V_{dc,in} - v_{C_r}^{RP}(t_1) - R_s i_{in}^{RP}(t_1)/2}{(L_r + L_m)\omega_{NC}} \sin\left(\omega_{NC}(t-t_1)\right) \right) \\ i_{out}^{NC}(t) &= 0 \\ i_{m}^{NC}(t) &= i_{in}^{NC}(t) \end{aligned} \tag{4.22}$$

In order to ease the calculation of the initial conditions in steady-state, the assumptions (4.23) and (4.24) are taken. First, the effect of the losses on the waveform is rather small and may be neglected (lossless case).

$$\begin{aligned} R_s &<< L_r \\ R_s &\approx 0 \end{aligned} \tag{4.23}$$

Then, the converter is operated close to the unity DC gain, so the input and output voltages are very similar and can be approximated by V_{dc}

$$V_{dc,out} \simeq V_{dc,in} \approx V_{dc} \tag{4.24}$$

This implies that the damped resonant frequency can be approximated by the initial resonant frequency:

$$\omega_{RP} \approx \omega_0 = \frac{1}{\sqrt{L_r C_r}} \tag{4.25}$$

Which means the time instant t_1 is load independent and is given by the tank parameters. The length of the two main intervals are given by:

$$T_{RP} = t_1 - t_0 \approx \frac{1}{2} T_r = \pi\sqrt{L_r C_r} = f_n \frac{T_{sw}}{2} \tag{4.26}$$

$$T_{NC} = t_2 - t_1 \approx \frac{T_{sw}}{2} - T_{RP} = (1 - f_n)\frac{T_{sw}}{2} \tag{4.27}$$

And thus, the current waveforms are simplified in (4.28) and (4.29). Assuming (4.24), the input current from (4.16) becomes (4.28) and is depending only on the initial condition $i_m(0)$ and $v_{C_r}(0)$.

$$i_{in}^{RP}(t) \approx i_m(0)\cos\left(\omega_0 t\right) - \frac{v_{C_r}(0)}{L_r \omega_0}\sin\left(\omega_0 t\right) \tag{4.28}$$

The magnetizing current $i_m^{RP}(t)$ is approximated by (4.29).

$$i_m^{RP}(t) \approx i_m(0) + \frac{V_{dc}}{2L_m} t \tag{4.29}$$

As depicted in **Fig. 4.5**, in steady state conditions, the waveforms during the second half switching period (intervals RP_n ans NC_n) can be obtained by a symmetry around zero from the first half switching period. It implies that at $t = t_2 = T_{sw}/2$, all variables have the same value as the initial condition at $t = t_0$ with an opposite sign (4.30).

$$\begin{aligned} i_{in}(t_2) &= -i_{in}(t_0) \\ i_{out}(t_2) &= -i_{out}(t_0) \\ i_m(t_2) &= -i_m(t_0) \\ v_{C_r}(t_2) &= -v_{C_r}(t_0) \end{aligned} \tag{4.30}$$

This allows the evaluation the initial value of the magnetizing current $i_m(0)$ in steady state as (4.31).

$$i_m(0) = -\frac{V_{dc} T_{RP}}{8 L_m} \tag{4.31}$$

Then, the output power, which is null during NC and NC_n intervals, is given in (4.32).

$$P_{out}(t) = \begin{cases} i_{out}(t)\frac{V_{dc,out}}{2} & , 0 < t < t_1 \\ 0 & , t_1 < t < \frac{T_{sw}}{2} \\ i_{out}(t)\frac{-V_{dc,out}}{2} & , \frac{T_{sw}}{2} < t < t_3 \\ 0 & , t_3 < t < T_{sw} \end{cases} \tag{4.32}$$

The average power can be calculated with (4.33) and simplified considering (4.31).

$$\begin{aligned} \langle P_{out} \rangle &= \frac{1}{T_{sw}} \int_0^{T_{sw}} P_{out}(t) dt \\ &\approx \frac{V_{dc}}{T_{sw}} \int_0^{t_1} i_{out}(t) dt \approx \frac{V_{dc}}{T_{sw}} \int_0^{t_1} \left(i_{in}(t) - i_m(t) \right) dt \\ &\approx \frac{V_{dc}(8 L_m v_{C_r}(0) + L_r \pi^2 V_{dc} + 4 i_m(0) L_m L_r \pi \omega_0)}{4 L_m L_r T_{sw} \omega^2} \\ &\approx \frac{2 V_{dc}}{T_{sw} L_r \omega_0} v_{C_r}(0) \end{aligned} \tag{4.33}$$

which implies that $v_{C_r}(0)$ can be expressed in function of the power in (4.34).

$$v_{C_r}(0) = P_{out} \frac{T_{sw} L_r \omega_0^2}{2 V_{dc}} \tag{4.34}$$

And finally

$$i_{in}^{RP}(t) = -\frac{V_{dc} T_{RP}}{8 L_m} \cos\left(\omega_0 t\right) + P_{out} \frac{T_{sw} \omega_0}{2 V_{dc}} \sin\left(\omega_0 t\right) \tag{4.35}$$

$$i_m^{RP}(t) = -\frac{V_{dc} T_{RP}}{8 L_m} + \frac{V_{dc}}{2 L_m} t \tag{4.36}$$

$$i_{out}^{RP}(t) = i_{in}^{RP}(t) - i_m^{RP}(t) \tag{4.37}$$

This model of the SISO mode allows to approximate the current waveform in steady state based on the circuit parameters and the average power. **Fig. 4.7** shows a comparison between switched circuit model (PLECS simulation) and approximated waveform based on the model.

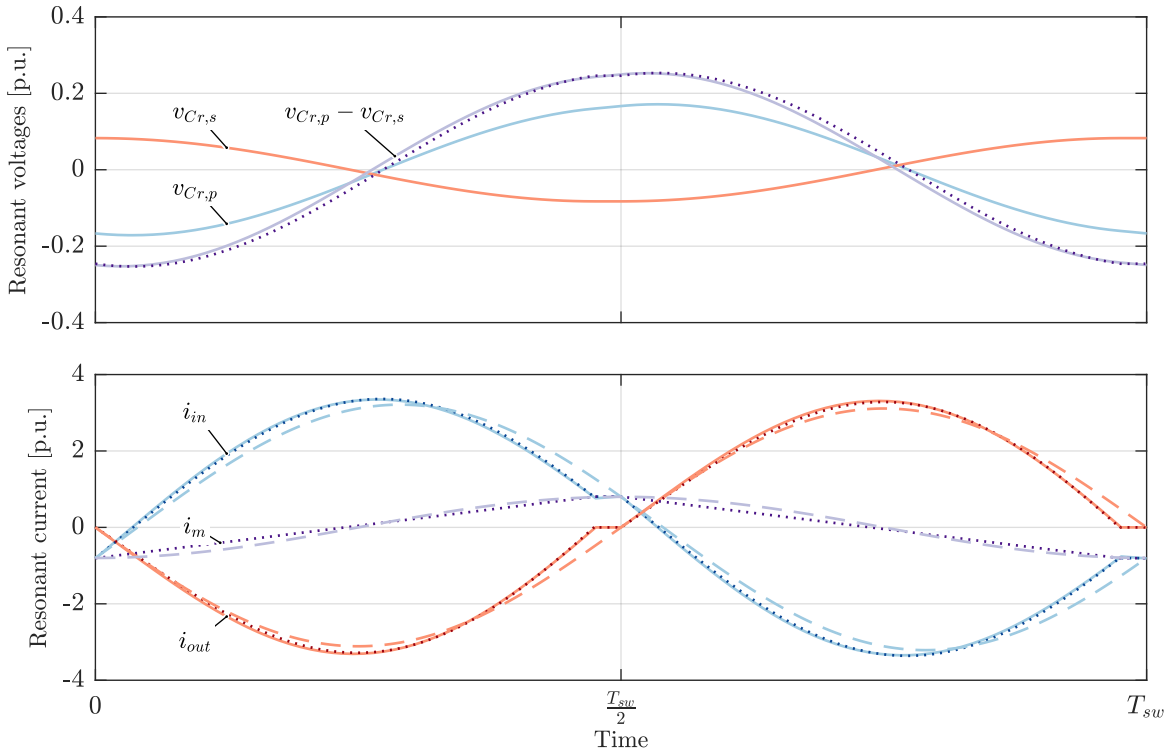


Figure 4.7 Comparison between the resonant capacitors voltage and current waveform in the normalized base and for f_n = 0.95, from the proposed model (in dotted lines), from PLECS simulation (plain lines) and from FHA (dashed line). It may be seen that the model is more accurate for the description of the timing and the zero-crossing.

4.4 Three-port LLC Converter

In the same way as for the bi-port LLC converter, the interval-by-interval analysis can be applied for the converter when three ports are used. In DISO mode, the discontinuities are introduced by the rectifier on the single output port, while in SIDO mode, the intervals are defined by the behavior of the rectifiers of the two output ports. So both modes have to be modeled separately.

4.4.1 Model in DISO mode

For the DISO mode, the DC-transformer part can be modeled with the circuit depicted in **Fig. 4.8**. It comprises two input ports and one output port, all characterized by their DC-bus voltages, respectively $V_{dc,in,1}$, $V_{dc,in,2}$ and $V_{dc,out}$, as well as a three-winding MFT with the turn ratio $n_{in,1} : n_{in,2} : n_{out}$ equipped with a resonant tank split between the three ports and composed by $L_{in,1}$, $C_{in,1}$, $L_{in,2}$, $C_{in,2}$, L_{out} and C_{out}. For the sake of simplification, it is considered that all the elements have already been reported to one side of the converter according to the turn ratio. The three resonant tanks have the exact same resonant frequency given in (4.38).

$$\omega_r = \frac{1}{\sqrt{L_{in,1}C_{in,1}}} = \frac{1}{\sqrt{L_{in,2}C_{in,2}}} = \frac{1}{\sqrt{L_{out}C_{out}}} \tag{4.38}$$

The typical voltage and current waveforms in steady state are depicted in **Fig. 4.9**. The same way as for the LLC converter of Section 4.3, two main intervals (and their equivalent, with opposite polarity) can be identified.

- During interval *RP*, both active ports are conducting and supporting the load as well as the magnetizing current. Since all the resonant tanks have the same resonant frequency, the length of the *RP* interval is approximatively the same for both active ports.
- During interval *NC*, the rectifier of the load port is not conducting and the port is disconnected. The magnetizing current i_m is shared between the two input ports.

The equivalent circuits for both *RP* and *NC* interval are depicted in **Fig. 4.10**. From those circuits, the differential equations system can be identified for *RP* interval in (4.39) and for *NC* interval in (4.40). During the interval *RP* (cf. **Fig. 4.10a**) the three voltages $V_{dc,in,1}$, $V_{dc,in,1}$ and $V_{dc,out}$ are applied to the circuit and the current loops $i_{in,1}$, $i_{in,2}$, and i_{out} are coupled through the magnetizing inductance.

$$\begin{aligned}
v^{RP}_{ac,in,1}(t) &= \frac{V_{dc,in,1}}{2} = v^{RP}_{C_r,in,1}(t) + L_{r,in,1}\frac{di^{RP}_{in,1}(t)}{dt} + R_{in,1}i^{RP}_{in,1}(t) + v^{RP}_{L_m}(t) \\
v^{RP}_{ac,in,2}(t) &= \frac{V_{dc,in,2}}{2} = v^{RP}_{C_r,in,2}(t) + L_{r,in,2}\frac{di^{RP}_{in,2}(t)}{dt} + R_{in,2}i^{RP}_{in,2}(t) + v^{RP}_{L_m}(t) \\
v^{RP}_{ac,out}(t) &= \frac{V_{dc,out}}{2} = v^{RP}_{C_r,out}(t) + L_{r,out}\frac{di^{RP}_{out}(t)}{dt} + R_{out}i^{RP}_{out}(t) + v^{RP}_{L_m}(t) \\
v^{RP}_{L_m}(t) &= L_m\frac{d}{dt}\left(i^{RP}_{in,1}(t) + i^{RP}_{in,2}(t) + i^{RP}_{out}(t)\right)
\end{aligned} \tag{4.39}$$

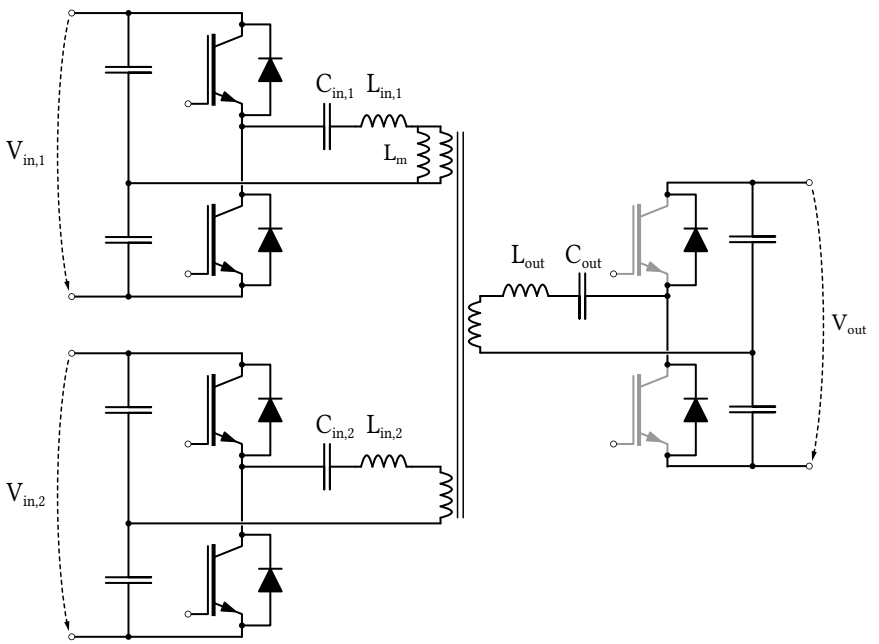


Figure 4.8 Topology of a three-port resonant DC-DC converter operated with two active ports. All voltages, currents and components located on the active ports are referenced with the index x_{in} whereas the elements of passive port are indicated with the index x_{out}.

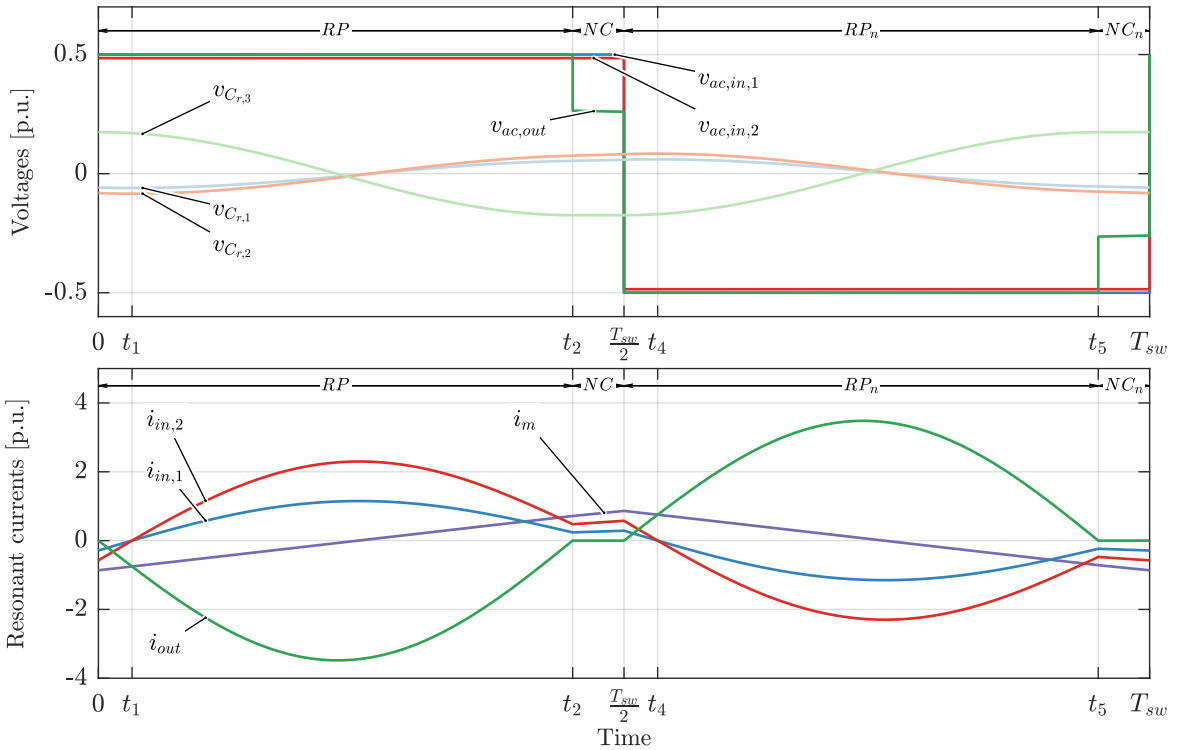


Figure 4.9 Typical voltage and current waveforms and corresponding sub-intervals in DISO mode.

During interval NC, $V_{dc,out}$ is disconnected and the corresponding current i_{out} is zero. The magnetizing current is the sum of both input currents and the resulting voltage v_{L_m} interfere in both current loops $i_{in,1}$ and $i_{in,2}$.

$$\begin{aligned}
v^{NC}_{ac,in,1}(t) &= \frac{V_{dc,in,1}}{2} = v^{NC}_{C_r,in,1}(t) + L_{r,in,1}\frac{di^{NC}_{in,1}(t)}{dt} + R_{in,1}i^{NC}_{in,1}(t) + v^{NC}_{L_m}(t) \\
v^{NC}_{ac,in,2}(t) &= \frac{V_{dc,in,2}}{2} = v^{NC}_{C_r,in,2}(t) + L_{r,in,2}\frac{di^{NC}_{in,2}(t)}{dt} + R_{in,2}i^{NC}_{in,2}(t) + v^{NC}_{L_m}(t) \\
v^{NC}_{L_m}(t) &= L_m\frac{d}{dt}\left(i^{NC}_{in,1}(t) + i^{NC}_{in,2}(t)\right)
\end{aligned} \tag{4.40}$$

The complexity of both systems (4.39) and (4.40) makes it very difficult to find the initial conditions for the steady state as it has been done for the two-port LLC converter. Indeed, during each interval, the three currents $i_{in,1}(t)$, $i_{in,2}(t)$ and $i_{out}(t)$ are coupled through the magnetizing inductor which makes it impossible to find an individual solution for each port. More over, the two intervals are coupled through the boundary conditions at t_1, $\frac{T_{sw}}{2}$, t_4 and T_{sw} (c.f **Fig. 4.9**).

4.4.1.1 Proposed model

In order to simplify the analysis, a change of variable is proposed aiming to decouple the currents and to represent them by simpler circuits having a single input and a single output. It is then proposed

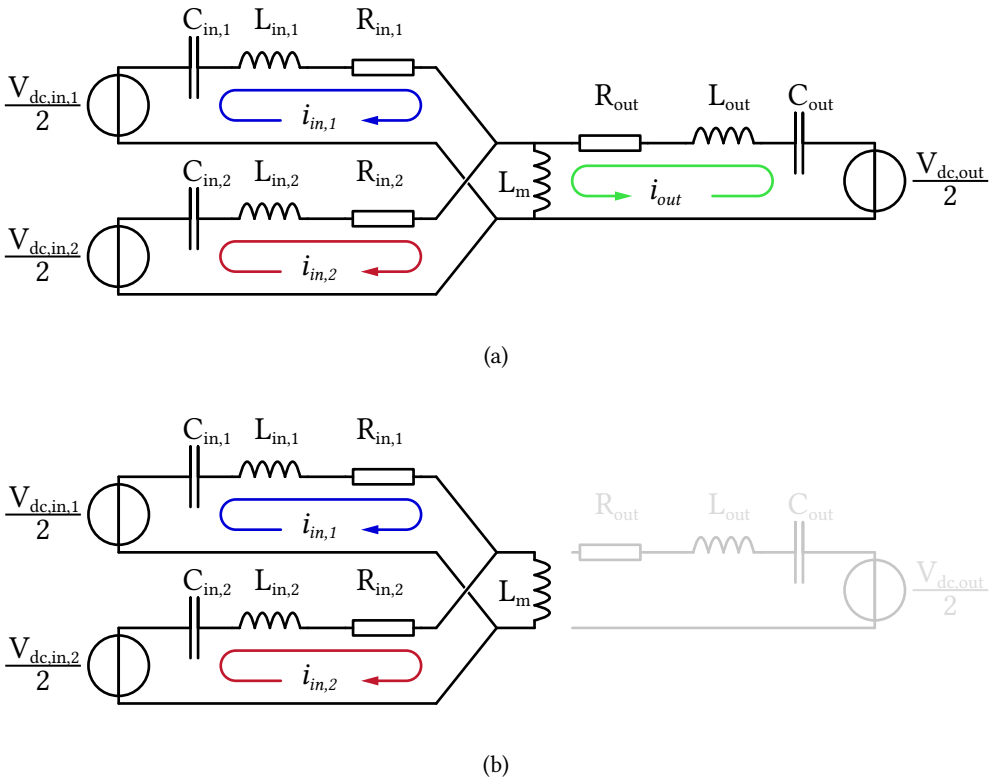


Figure 4.10 Equivalent circuit for interval RP (a) and NC (b).

to represent the two input currents and the output current as the superimposition of a common mode system, which represents the total power flow from the active ports to the output port and a differential system, which represents the circulating power flow between the two active ports.

Thus, for the common-mode equivalent circuit, a single input voltage source $V_{com,in}$ is considered. Its voltage is the output of the voltage divider composed by the impedances ($Z_{in,1}$ and $Z_{in,2}$) of the resonant tanks of the two inputs, such as expressed in 4.41. If the converter was switched exactly at resonant frequency, this ratio would be corresponding to the ratio of the resistors $R_{in,1}$ and $R_{in,2}$. But since the converter is switched below the frequency and assuming that the resistors are much smaller than the reactance at this frequency, the ratio of the impedance can be approximated by the ratio of the two corresponding inductances.

$$\begin{aligned} Z_{in,i} &= \omega_r L_i + R_i \quad \text{with} \quad R_i << \omega L_i \\ V_{com,in} &= \frac{Z_{in,2} V_{dc,in,1}(t) + Z_{in,1} V_{dc,in,2}(t)}{Z_{in,1} + Z_{in,2}} \approx V_{dc,in,1} \frac{L_{in,2}}{L_{in,1} + L_{in,2}} + V_{dc,in,2} \frac{L_{in,1}}{L_{in,1} + L_{in,2}} \end{aligned} \tag{4.41}$$

Since the two active ports are switched at the same time, this definition is also valid for the voltage

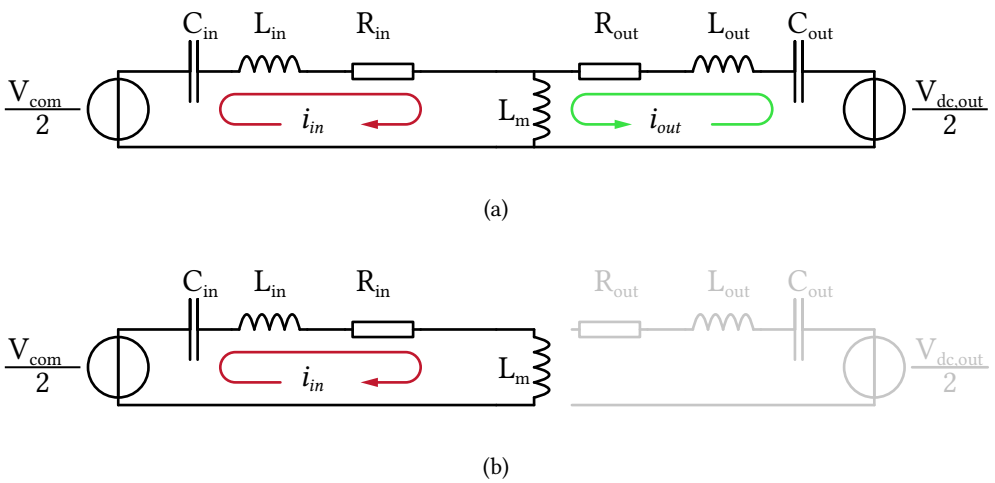


Figure 4.11 Split resonant tank equivalent circuits in common mode for the intervals RP (a) and NC (b).

$v_{ac,in,com}(t)$ applied to the resonant circuit.

$$v_{ac,in,com}(t) = v_{ac,in,1}(t)\frac{L_{in,2}}{L_{in,1} + L_{in,2}} + v_{ac,in,2}(t)\frac{L_{in,1}}{L_{in,1} + L_{in,2}} \tag{4.42}$$

The resonant tank seen from the common-mode input port is thus the combination of the two input resonant tanks and is described with the parameters L_{in} and C_{in}. Both L_{in} and C_{in} are the parallel combination of $L_{in,1}$, $L_{in,2}$ and respectively $C_{in,1}$, $C_{in,2}$ such as given in (4.43).

$$\begin{aligned} L_{in} &= \frac{L_{in,1}L_{in,2}}{L_{in,1} + L_{in,2}} \\ C_{in} &= C_{in,1} + C_{in,2} \end{aligned} \tag{4.43}$$

The same combination is applied to the parasitic resistance of the two input ports in (4.44)

$$R_{in} = \frac{R_{in,1}R_{in,2}}{R_{in,1} + R_{in,2}} \tag{4.44}$$

The circuits of **Fig. 4.10** with two inputs and three resonant tanks become then such as depicted in **Fig. 4.11**, with one input port, one output port and their corresponding resonant tanks.

After a circuit transformation, the resonant components of the output port (L_{out}, C_{out}) are combined to the input ones (L_{in}, C_{in}) and the circuit becomes a single resonant tank equivalent circuit with the parameters L_{com} and C_{com}given in (4.45) and as illustrated in **Fig. 4.12**.

$$\begin{aligned} L_{com} &\approx \frac{L_{in,1}L_{in,2}}{L_{in,1} + L_{in,2}} + L'_{out} \\ C_{com} &\approx \frac{(C_{in,1} + C_{in,2})C'_{out}}{C_{in,1} + C_{in,2} + C'_{out}} \end{aligned} \tag{4.45}$$

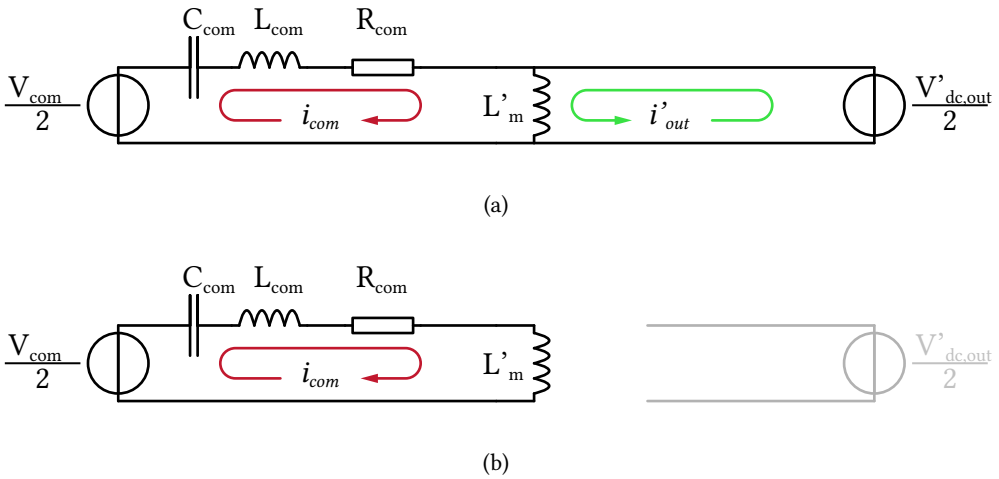


Figure 4.12 Single resonant tank equivalent circuits in common mode for the intervals RP (a) and NC (b).

The same is applied to the parasitic resistance of both input and output ports in (4.46).

$$R_{com} \approx \frac{R_{in,1}R_{in,2}}{R_{in,1} + R_{in,2}} + R'_{out} \tag{4.46}$$

The input current of this circuit is the sum of both actual active ports input currents (4.48).

$$i_{in,com}(t) = i_{in,1}(t) + i_{in,2}(t) \tag{4.47}$$

$$i_{out,com}(t) = i_{out}(t) \tag{4.48}$$

The common mode circuit represents the total power flow ($P_{in,1} + P_{in,2}$) from the active ports to the load. It can be described as a standard LLC converter the same way as for the SISO mode (cf. Section 4.3), with the input voltage $V_{com,in}$ and the output voltage $V_{com,out}$. Both are approximated by V_{com} thanks to the unity DC-gain simplification (4.24). Using (4.37) for the expression of the waveforms and (4.31), (4.34) for the initial conditions, the common mode input and output currents can be expressed in function of the common mode power in (4.49) to (4.51). The common mode input current $i_{com,in}(t)$ is given by (4.49).

$$i_{com,in}(t) = -\frac{V_{com}T_r}{8L_m}\cos(\omega_0 t) + \frac{P_{out}T_{sw}\omega_0}{2V_{com}}\sin(\omega_0 t) \tag{4.49}$$

The magnetizing current is given by (4.50).

$$i_m(t) = -\frac{V_{com}T_r}{8L_m} + \frac{V_{com}}{2L_m}t \tag{4.50}$$

And the output current in common mode corresponds to the actual output current $i_{out}(t)$ is given by the difference of i_m and $i_{com,in}$ (4.51).

$$i_{out}(t) = i_{com,out}(t) = i_m(t) - i_{com,in}(t) \tag{4.51}$$

The average power $\langle P_{com} \rangle$ through the common mode equivalent converter is defined as in (4.52) which can be simplified in (4.53) since the waveforms are the same during both half switching periods but with opposite signs.

$$\langle P_{com} \rangle = \frac{1}{t_{sw}} \int_0^{t_{sw}} v_{ac,in,com}(t) i_{com,in}(t) dt \tag{4.52}$$

$$\langle P_{com} \rangle = \frac{V_{com}}{t_{sw}} \int_0^{t_{sw}/2} i_{com,in}(t) dt = \frac{V_{com}}{2} \bar{i}_{com,in} \tag{4.53}$$

The deviations of $V_{in,1}$ and $V_{in,2}$ from V_{com} are applied to a circuit which comprises the resonant tanks of both input ports and cause the differential current $i_{dif}(t)$ to flow from one input to the other as depicted in **Fig. 4.13a**.

The circuit can be simplified to the equivalent depicted in **Fig. 4.13b**, with a single voltage source V_{dif}, given in (4.54).

$$V_{dif} = V_{dc,in,1} - V_{dc,in,2} \tag{4.54}$$

And a single resonant tank, which is the series combination of both actual tanks, with the parameters L_{dif}, C_{dif}, R_{dif} as given in (4.55).

$$\begin{aligned} L_{dif} &= L_1 + L_2 \\ C_{dif} &= \frac{C_{in,1} C_{in,2}}{C_{in,1} + C_{in,2}} \\ R_{dif} &= R_1 + R_2 \end{aligned} \tag{4.55}$$

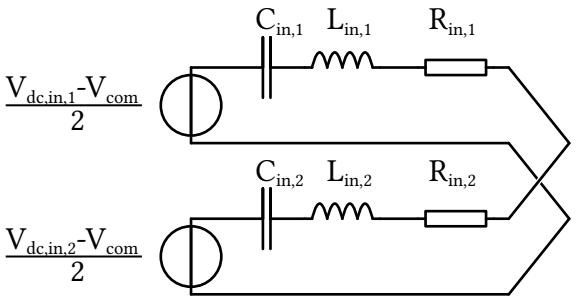
One may note that this circuit does not depend on the load P_{out} or the output voltage V_{out} at all. The discontinuity caused by the rectifier does not affect this system and the circuit of **Fig. 4.13b** is valid for both RP and NC interval. The circuit can be analysed as a RLC circuit under square-wave voltage excitation. The differential equation of the circuit is given in (4.56) and leads to the solution in (4.57) with the initial conditions $i_{dif}(0)$ for the current and $V_{C_{dif}}(0)$ for the capacitor voltage.

$$V_{dif} = v_{R_{dif}}(t) + v_{L_{dif}}(t) + v_{C_{dif}}(t) = R_{dif} i_{dif}(t) + L_{dif} \frac{d i_{dif}(t)}{dt} + \frac{1}{C_{dif}} \int_0^t i_{dif}(t) dt \tag{4.56}$$

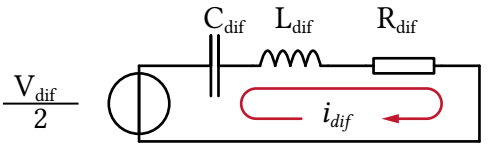
$$i_{dif}(t) = e^{-\alpha t} \left(i_{dif}(0) cos(\omega t) + \frac{(V_{dif} - V_{C_{dif}}(0) - R_{dif} i_{dif}(0)/2)}{L_{dif} \omega} sin(\omega t) \right) \tag{4.57}$$

In steady state, the boundary conditions are given by (4.58).

$$\begin{aligned} i_{dif}(0) &= -i_{dif}(T_{sw}/2) \\ V_{C_{dif}}(0) &= -V_{C_{dif}}(T_{sw}/2) \end{aligned} \tag{4.58}$$



(a)



(b)

Figure 4.13 Equivalent circuits in differential mode (a) and simplified circuit (b) according to (4.54) and (4.55).

The solution of the system composed by (4.57) in (4.58) gives (4.59) and highlights the coefficients of proportionality k_{idif} and k_{vdif}.

$$\begin{aligned} i_{dif}(0) &= -\frac{V_{dif} e^{\frac{\alpha T_{sw}}{2}} \sin\left(\frac{T_{sw}\omega}{2}\right)}{L_{dif}\omega\left(e^{\alpha T_{sw}} + 2e^{\frac{\alpha T_{sw}}{2}} \cos\left(\frac{T_{sw}\omega}{2}\right) + 1\right)} = k_{idif} V_{dif} \\ V_{C_{dif}}(0) &= \frac{V_{dif}\left(R_{dif} e^{\frac{\alpha T_{sw}}{2}} \sin\left(\frac{T_{sw}\omega}{2}\right) - L_{dif}\omega\left(e^{\alpha T_{sw}} - 1\right)\right)}{2L_{dif}\omega\left(2e^{\frac{\alpha T_{sw}}{2}} \cos\left(\frac{T_{sw}\omega}{2}\right) + e^{\alpha T_{sw}} + 1\right)} = k_{vdif} V_{dif} \end{aligned} \tag{4.59}$$

The differential current can thus be characterized in function of the differential voltage V_{dif} applied to the circuit thanks to k_{idif} and k_{vdif} which depend only on the parameters of the two input resonant tanks and the switching frequency. The effect of V_{dif} is depicted in **Fig. 4.14**.

The average differential current can be evaluated with (4.60).

$$\bar{i}_{dif} = \frac{1}{t_{sw}} \int_0^{t_{sw}} i_{dif}(t)dt = \frac{2}{t_{sw}} \int_0^{\frac{t_{sw}}{2}} i_{dif}(t)dt \tag{4.60}$$

This results in (4.61) where the coefficient k_{pdif}, depending on k_{idif} and k_{vdif} can be highlighted in (4.62).

$$\bar{i}_{dif} = V_{dif} k_{pdif} \tag{4.61}$$

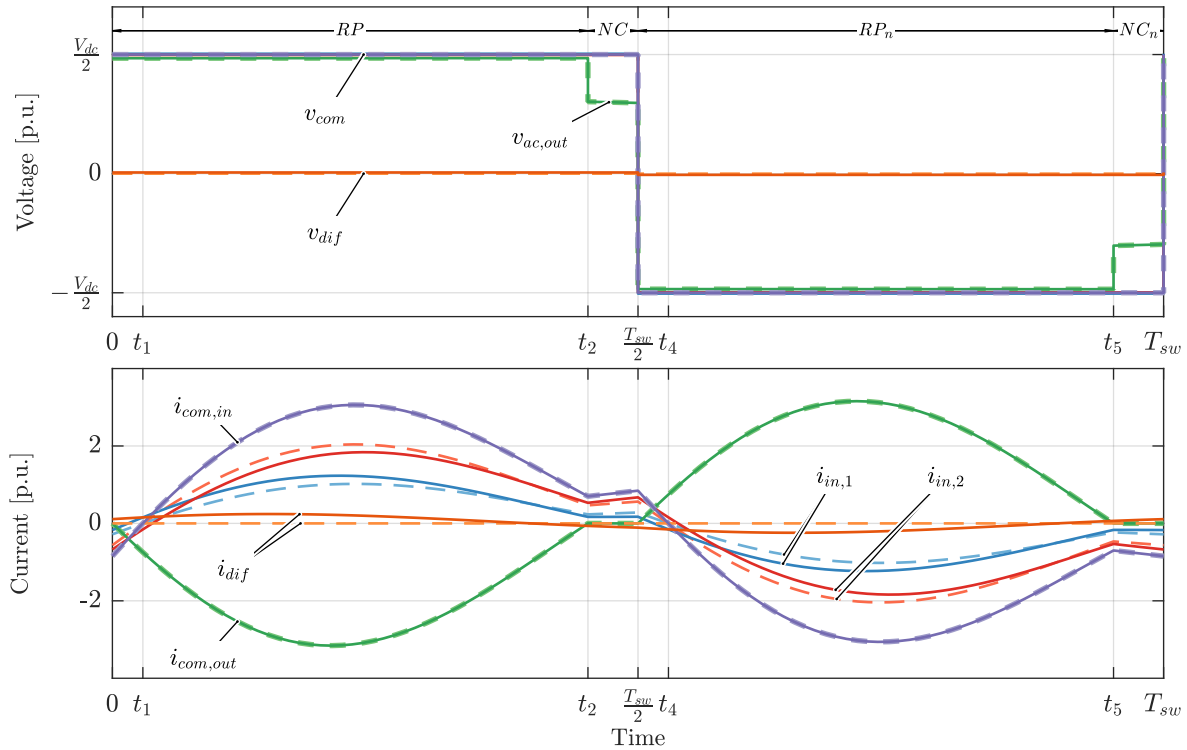


Figure 4.14 Common and differential mode voltages and currents waveform, from PLECS simulation, for $V_{dif} = 0$ in dashed line and $V_{dif} = 0.05$ p.u. in plain line. $v_{ac,out}$, $i_{com,in}$ and $i_{com,out}$ are not affected by the presence of a differential power flow.

$$k_{pdif} = \frac{e^{-\frac{\alpha t_{sw}}{2}}\left(\sin\left(\frac{\pi}{f_n}\right)\left(\alpha(k_{idif}R_{dif} + 2k_{vdif} - 2) + 2k_{idif}L_{dif}\omega^2\right)\right)}{L_{dif}t_{sw}\omega(\alpha^2 + \omega^2)} + \frac{e^{-\frac{\alpha t_{sw}}{2}}\left(\omega\left(\cos\left(\frac{\pi}{f_n}\right) - e^{\frac{\alpha t_{sw}}{2}}\right)(-2\alpha k_{idif}L_{dif} + k_{idif}R_{dif} + 2k_{vdif} - 2)\right)}{L_{dif}t_{sw}\omega(\alpha^2 + \omega^2)} \tag{4.62}$$

The average differential power $\langle P_{dif}\rangle$ may be expressed in function of the average current $\bar{i}_{dif}$ as in (4.63).

$$\begin{aligned}\langle P_{dif}\rangle &= V_{com}\bar{i}_{dif} \\ &= V_{com}k_{pdif}V_{dif}\end{aligned} \tag{4.63}$$

The coefficient k_{idif}, k_{vdif} and k_{pdif} are depending only on the circuit parameters and the switching frequency, which means that for a given design, the differential current can be calculated for any operation point with a given P_{dif}.

Using the inverse of the change of variables of (4.45) and (4.55), the actual currents in the converter

can be expressed in terms of i_{com} and i_{dif} in (4.64).

$$\begin{aligned} i_{in,1}(t) &= \frac{L_{in,2}}{L_{in,1}+L_{in,2}} i_{com,in}(t) + i_{dif}(t) \\ i_{in,2}(t) &= \frac{L_{in,1}}{L_{in,1}+L_{in,2}} i_{com,in}(t) - i_{dif}(t) \\ i_{out}(t) &= i_{com,out}(t) \end{aligned} \tag{4.64}$$

The ratio of the resonant inductors $L_{in,1}$ and $L_{in,2}$ appears then as the sharing ratio of the common mode current $i_{com,in}$ between the two inputs. In order to simplify the notation, the sharing ratio k_{12} and its complementary part k_{21} are defined in (4.65).

$$\begin{aligned} k_{12} &= \frac{L_{in,2}}{L_{in,1}+L_{in,2}} \\ k_{21} &= \frac{L_{in,1}}{L_{in,1}+L_{in,2}} = 1 - k_{12} \end{aligned} \tag{4.65}$$

This leads to the expression of the average power provided by the two active ports in (4.66)

$$\begin{aligned} \langle P_{in,1} \rangle &= \frac{1}{t_{sw}} \int_0^{t_{sw}} v_{ac,in,1}(t) i_{in,1}(t) dt = \frac{V_{in,1}}{t_{sw}} \int_0^{t_{sw}/2} i_{in,1}(t) dt \\ &= \frac{V_{in,1}}{t_{sw}} \int_0^{t_{sw}/2} k_{12} i_{com,in}(t) + i_{dif}(t) dt \\ &= \frac{V_{in,1}}{2} k_{12} \bar{i}_{com,in} + \frac{V_{in,1}}{2} \bar{i}_{dif} \\ \langle P_{in,2} \rangle &= \frac{V_{in,2}}{2} k_{21} \bar{i}_{com,in} + \frac{V_{in,2}}{2} \bar{i}_{dif} \end{aligned} \tag{4.66}$$

Introducing the inverse of the change of variables for the voltages, given in (4.67),

$$\begin{aligned} V_{in,1} &= V_{com} + \frac{L_{in,1}}{L_{in,1}+L_{in,2}} V_{dif} = V_{com} + k_{21} V_{dif} \\ V_{in,2} &= V_{com} - \frac{L_{in,2}}{L_{in,1}+L_{in,2}} V_{dif} = V_{com} - k_{12} V_{dif} \end{aligned} \tag{4.67}$$

the expressions of the powers become (4.68) and (4.69).

$$\begin{aligned} \langle P_{in,1} \rangle &= k_{12} \frac{V_{com}}{2} \bar{i}_{com} \quad + k_{12} k_{21} \frac{V_{dif}}{2} \bar{i}_{com} + \frac{V_{com}}{2} \bar{i}_{dif} \quad + k_{21} V_{dif} \bar{i}_{dif} \\ &= k_{12} \langle P_{com} \rangle \quad + k_{12} k_{21} \frac{V_{dif}}{2} \bar{i}_{com} + \langle P_{dif} \rangle \quad + k_{21} V_{dif} \bar{i}_{dif} \end{aligned} \tag{4.68}$$

$$\begin{aligned} \langle P_{in,2} \rangle &= k_{21} \frac{V_{com}}{2} \bar{i}_{com} \quad - k_{12} k_{21} \frac{V_{dif}}{2} \bar{i}_{com} - \frac{V_{com}}{2} \bar{i}_{dif} \quad + k_{12} V_{dif} \bar{i}_{dif} \\ &= k_{21} \langle P_{com} \rangle \quad - k_{12} k_{21} \frac{V_{dif}}{2} \bar{i}_{com} - \langle P_{dif} \rangle \quad + k_{12} V_{dif} \bar{i}_{dif} \end{aligned} \tag{4.69}$$

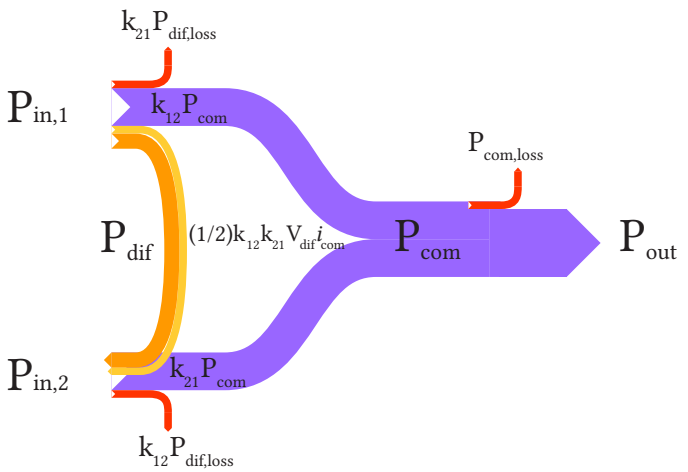


Figure 4.15 The different components of the power flow in DISO mode. When no differential voltage is applied between the two input ports, only P_{com} is flowing from the input to the output and is shared between the two input ports with respect to k_{12} and k_{21}. When a differential voltage is applied, P_{dif} is flowing from the input 1 to the input 2 and is subject to the losses $P_{dif,loss}$ also shared between the two ports.

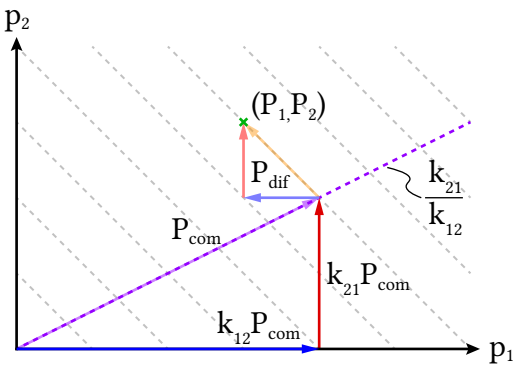


Figure 4.16 Graphical presentation of P_{com} and P_{dif}. Any operating point, defined by (P_1,P_2), not located on the axis given by k_{12} and k_{21} imply a circulation on P_{dif}.

The graphical representation of these power components is depicted in **Fig. 4.15**.

k_{12} and k_{21} are the natural power sharing ratios of the resonant stage (cf. **Fig. 4.16**). If no circulating power is introduced by the imposition of a (controlled) differential voltage V_{dif}, the power is shared between the input port according to k_{12} and k_{21}. More over, the product $V_{com} \cdot \bar{i}_{dif}$ appears as the circulating power flowing from input 1 to input 2, and $V_{dif}\bar{i}_{dif}$ represents the losses due to the circulation of power. Keeping in mind that V_{dif} remains rather small compared to V_{com}, the losses remain reasonable (4.70).

$$\frac{P_{dif,loss}}{P_{dif}} = \frac{V_{dif}\bar{i}_{dif}}{V_{com}\bar{i}_{dif}} = \frac{V_{dif}}{V_{com}} \tag{4.70}$$

4.4.2 Experimental Results

An experimental validation is carried out using the LV prototype described in the appendix B. The experiment consists of supplying the DC buses of the two input ports with a regulated voltage source enabling a fixed and adjustable voltage to be imposed. A resistive load corresponding to powers of 1, 2, 3 and 4 kW is connected to the output port. The parameters of Table **4.1** are used for the resonant circuit. In this case, no resonant (L_{out}, C_{out}) tank has been placed on the output port. It modifies slightly the P_{com} component, but does not affect the sharing or the differential circuit.

Table 4.1 Resonant tank parameters for the experiment

L_m	$L_{in,1}$	$C_{in,1}$	$L_{in,2}$	$C_{in,2}$
400 µH	17.5 µH	5 µF	35 µH	2.5 µF

Resonant currents waveforms are captured using an oscilloscope and are used to calculate P_{com} and P_{dif} for various V_{dif}. Two operating points are shown in **Figs. 4.17a** and **4.17b**. **Fig. 4.17c** shows the evolution of P_1 and P_2 as a function of P_{com}, and **Fig. 4.17d** presents P_{dif} as a function of V_{dif}.

4.4.3 Model in SIDO mode

In single-input-dual-output (SIDO) mode, the topology under study is as presented in **Fig. 4.18**. It comprises an active switching cell generating a square-wave voltage $v_{ac,in}(t)$ on the input, and two passive rectifiers on the outputs. The typical voltage and current waveforms are illustrated in **Fig. 4.19**.

Four main intervals (two per half-switching period) can be identified:

- The *RP* interval during which the two rectifiers are conducting. The power is transferred during this time interval. The two rectifiers do not necessarily stop conducting at the same time, which implies the presence of a sub-interval during which only one of the rectifiers conducted. Nevertheless, the resonant frequencies being identical for the resonant tanks of the three ports, this interval difference is very small and negligible and the *RP* interval can be considered as common to the two output ports.
- The *NC* interval during which the secondary side rectifiers are in blocking state. The input current is equal to the magnetizing current.
- The interval RP_n which is similar to interval *RP* with opposite signs
- The interval NC_n which is similar to interval *NC* with opposite signs

The simplified equivalent circuits for intervals *RP* and *NC* are illustrated in **Fig. 4.20**.

In the same way as for the dual-input-single-output (DISO) mode and in order to get rid of the solving of a very complex differential equation system, it is proposed to decouple the system into a common mode equivalent and a differential mode equivalent. For the common mode equivalent, the resonant tanks of the two output ports as well as the parasitic resistors are combined to form a single output

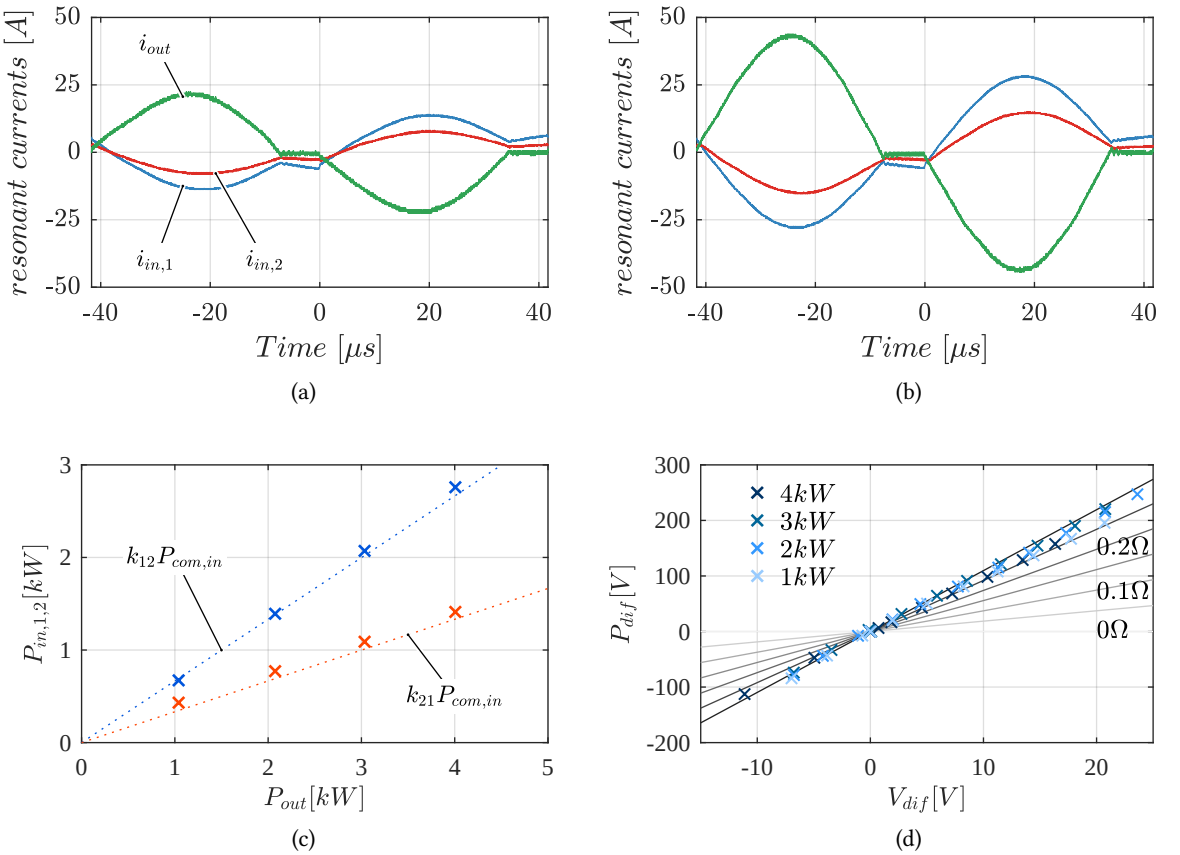


Figure 4.17 (a) and (b) show the resonant current waveforms for a load corresponding to **2 kW** and **4 kW**, respectively. (c) shows the evolution of the natural sharing ratio (V_{dif} = 0) as a function of the total load. The proportion remains constant for any output power (k_{12} = **2/3**, k_{21} = **1/3**) even if a slight deviation is visible. This deviation can be explained by the presence of losses. (d) shows the evolution of P_{dif} for various V_{dif} and various P_{com}. P_{com} has no influence on P_{dif} and the relation between P_{dif} and V_{dif} is clearly linear. The evaluation of corresponding k_{pdif} allows for an estimation of R_{dif} around **0.55** Ω.

tank with the parameters L_{out} and C_{out} given in (4.71).

$$\begin{aligned} L_{out} &= \frac{L_{out,1}L_{out,2}}{L_{out,1} + L_{out,2}} \\ C_{out} &= C_{out,1} + C_{out,2} \end{aligned} \tag{4.71}$$

while the output voltages become $v_{ac,out}(t)$ and $V_{dc,out}$, as expressed in (4.72).

$$\begin{aligned} v_{ac,out}(t) &= v_{ac,out,1}(t)\frac{L_{out,2}}{L_{out,1} + L_{out,2}} + v_{ac,out,2}(t)\frac{L_{out,1}}{L_{out,1} + L_{out,2}} \\ V_{dc,out} &= V_{dc,out,1}\frac{L_{out,2}}{L_{out,1} + L_{out,2}} + V_{dc,out,2}\frac{L_{out,1}}{L_{out,1} + L_{out,2}} \end{aligned} \tag{4.72}$$

The circuit of **Fig. 4.20**, with two outputs and their resonant tanks, becomes as illustrated in **Fig. 4.21** with a single output and two resonant tanks. After a transformation such as (4.7) all the elements of

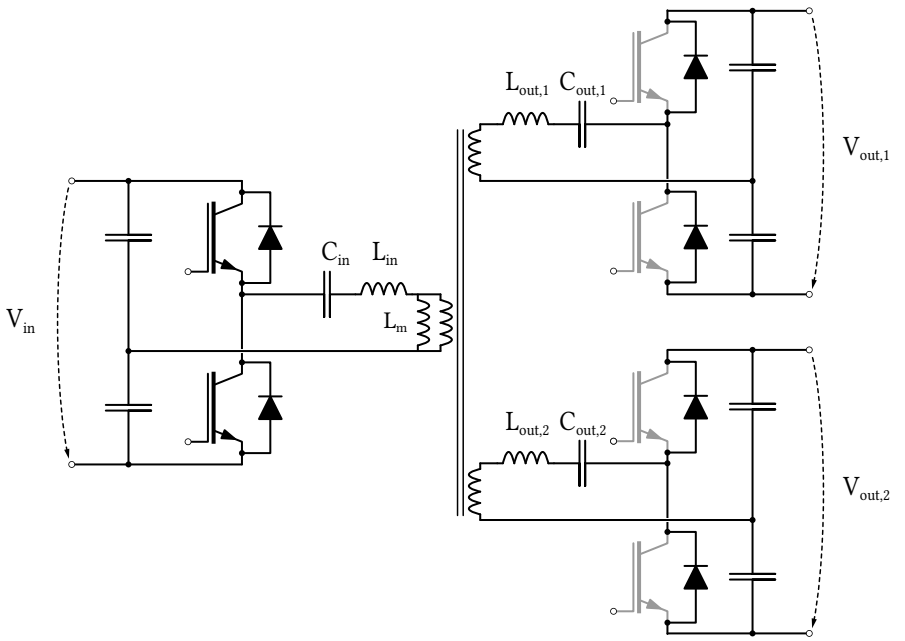


Figure 4.18 Topology of a three-port resonant DC-DC converter operated with one active ports and two load ports.

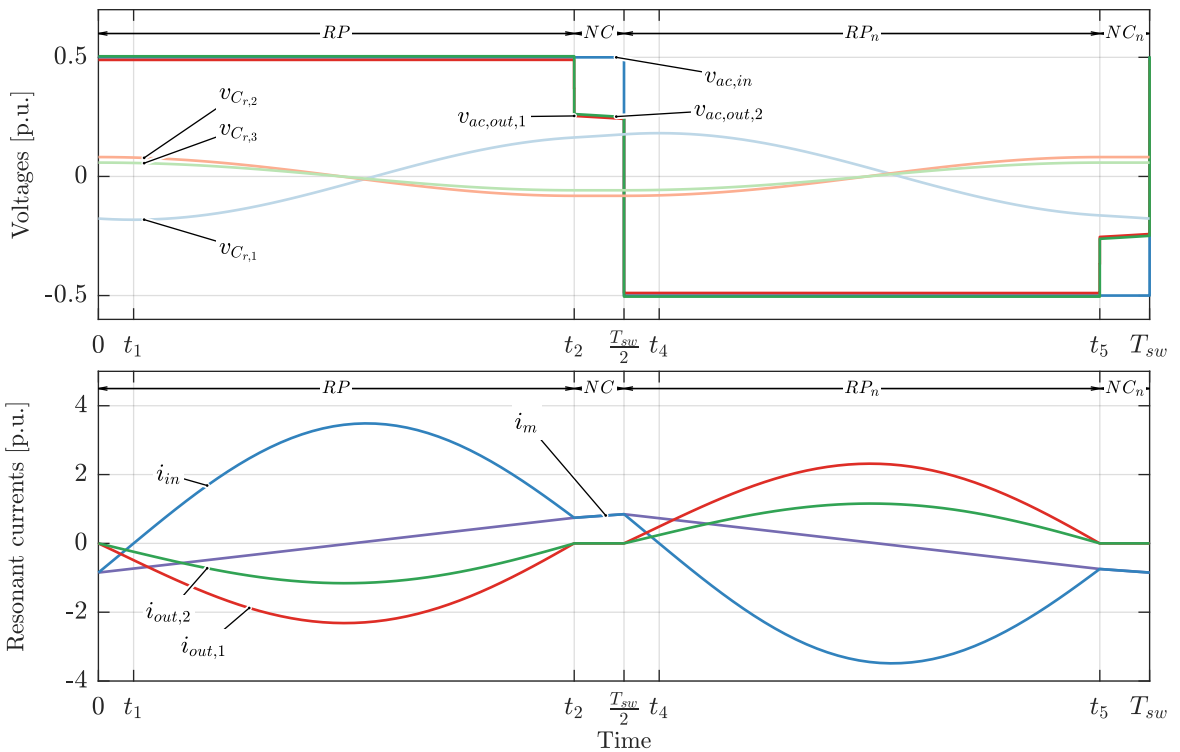


Figure 4.19 Typical voltage (a) and current (b) waveforms and corresponding sub-intervals, in SIDO mode.

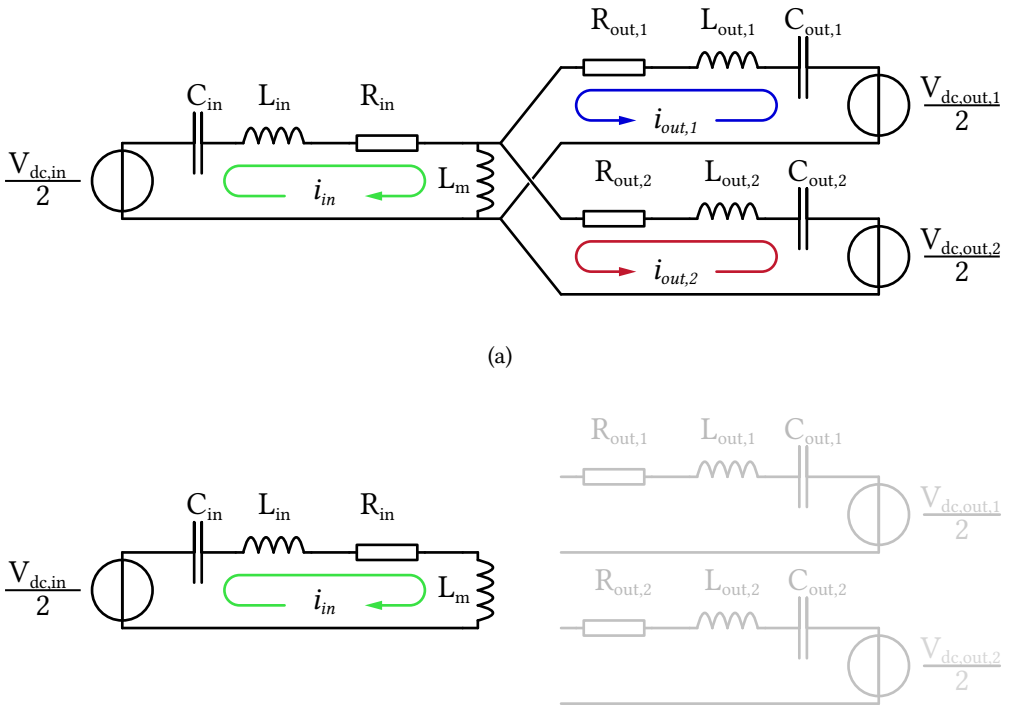


Figure 4.20 Equivalent circuit for the interval *RP* (a) and the interval *NC* (b) in SIDO mode.

the secondary are transferred to the primary to be combined into a single resonant tank. The resonant parameters L_{com} and C_{com} of the resulting resonant tank are calculated using (4.73).

$$\begin{aligned} L_{com} &\approx L_{in} + L'_{out} = L_{in} + \frac{L'_{out,1} L'_{out,2}}{L'_{out,1} + L'_{out,2}} \\ C_{com} &\approx \frac{C_{in} C'_{out}}{C_{in} + C'_{out}} = \frac{C_{in}(C'_{out,1} + C'_{out,2})}{C_{in} + C'_{out,1} + C'_{out,2}} \end{aligned} \tag{4.73}$$

The same is applied to the parasitic resistances in

$$R_{com} \approx R_{in} + R'_{out} = R_{in} + \frac{R'_{out,1} R'_{out,2}}{R'_{out,1} + R'_{out,2}} \tag{4.74}$$

Thus, the split tank circuit of **Fig. 4.21** becomes as depicted in **Fig. 4.22** with a single resonant tank.

The circuit can be then described as a standard LLC circuit using (4.37) for the expression of the waveforms and (4.31), (4.34) for the initial conditions. Finally, the common mode input and output currents can be expressed in function of the common mode power, given by (4.75), in (4.76) to (4.78).

$$P_{com} = P_{out,1} + P_{out,2} \tag{4.75}$$

The common mode input current $i_{com,in}(t)$ is given by the approximation in (4.76).

$$i_{com,in}(t) \approx -\frac{V_{com} T_r}{8 L_m} \cos(\omega_0 t) + \frac{P_{com} T_{sw} \omega_0}{2 V_{com}} \sin(\omega_0 t) \tag{4.76}$$

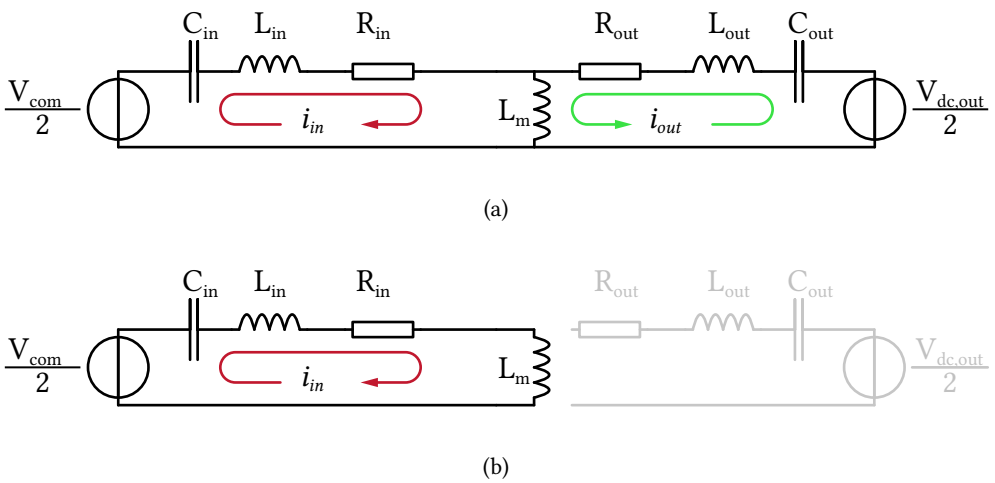


Figure 4.21 Split resonant tank equivalent circuits in common mode for the intervals *RP* (a) and *NC* (b) for the SIDO mode.

The magnetizing current is given by (4.77).

$$i_m(t) \approx -\frac{V_{com} T_r}{8 L_m} + \frac{V_{com}}{2 L_m} t \tag{4.77}$$

And the output current in common mode $i_{com,out}(t)$ is given by the difference of these two latter (4.78).

$$i_{com,out}(t) = i_{com,in}(t) - i_m(t) \tag{4.78}$$

Depending on the loads present on the two output ports, the voltages $V_{dc,out,1}$ and $V_{dc,out,2}$ may be different from each other. Their deviations from $V_{dc,out}$ as defined in (4.72) may be represented using a differential mode circuit which includes only the secondary components as depicted in **Fig. 4.23**. The resonant tanks ($L_{out,1}$, $C_{out,1}$) and ($L_{out,2}$, $C_{out,2}$) of the two ports can be combined in series to form a single resulting tank which resonant inductance L_{dif} and resonant capacitance C_{dif} are given by (4.79).

$$\begin{aligned} L_{dif} &= L_{out,1} + L_{out,2} \\ C_{dif} &= \frac{C_{out,1} C_{out,2}}{C_{out,1} + C_{out,2}} \end{aligned} \tag{4.79}$$

The voltage deviations are combined into a voltage source V_{dif} given by (4.80).

$$V_{dif} = \left(V_{dc,out,1} - V_{dc,out}\right) - \left(V_{dc,out,2} - V_{dc,out}\right) = V_{dc,out,1} - V_{dc,out,2} \tag{4.80}$$

The resulting circuit is illustrated in **Fig. 4.24**. This circuit is only valid for the *RP* interval. The rectifiers of the two output ports being blocked during *NC* interval, no differential power flow is present during this period of time. The voltage $v_{ac,dif}(t)$ applied to the circuit can thus be given by

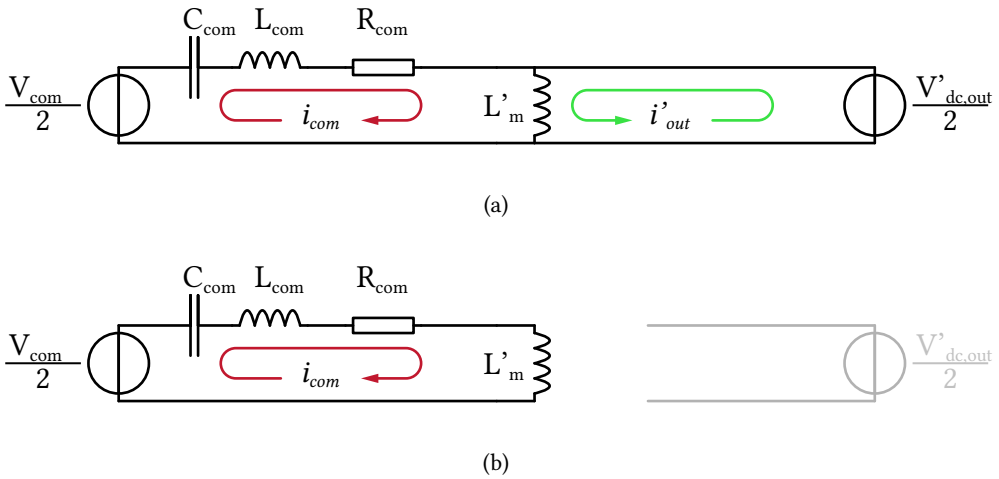


Figure 4.22 Single resonant tank equivalent circuits in common mode for the intervals *RP* (a) and *NC* (b) for the SIDO mode.

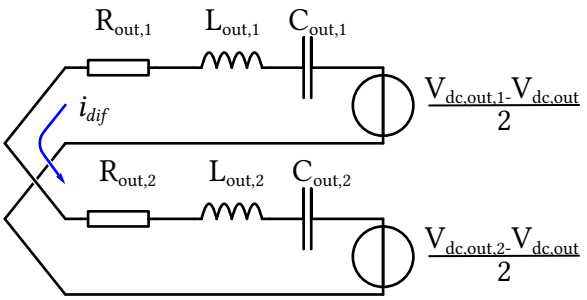


Figure 4.23 Differential mode circuit, during interval *RP*.

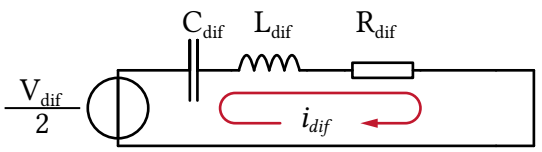


Figure 4.24 Differential mode equivalent circuit, during interval *RP*.

(4.81).

$$v_{ac,dif}(t) = \begin{cases} \frac{V_{dif}}{2} & , 0 < t < t_2 \\ \nexists & , t_2 < t < \frac{T_{sw}}{2} \\ \frac{-V_{dif}}{2} & , \frac{T_{sw}}{2} < t < t_5 \\ \nexists & , t_5 < t < T_{sw} \end{cases} \tag{4.81}$$

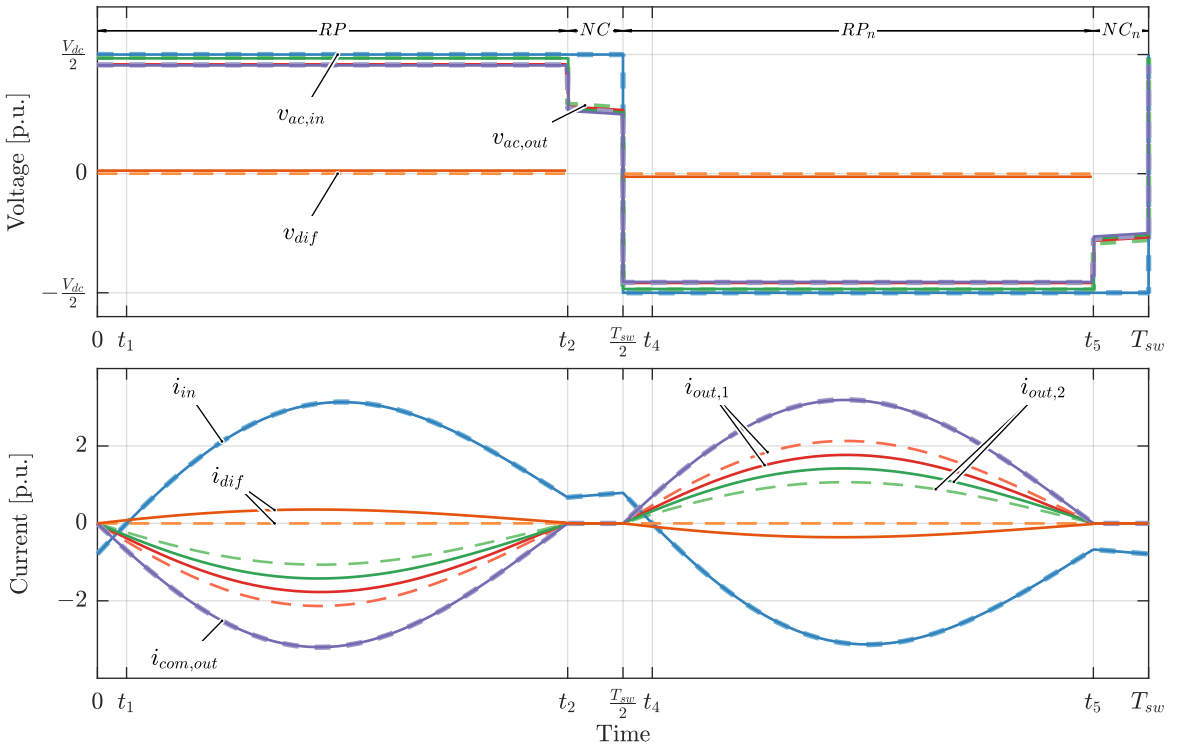


Figure 4.25 Common and differential mode voltages and currents waveform in *SIDO* mode for V_{dif} = 0 in dashed line and V_{dif} = 0.05 p.u. in plain line. $v_{ac,in}$, $i_{com,out}$ and i_{in} are not affected by the presence of a differential power flow.

the resulting current $i_{dif}(t)$ is thus given by (4.82).

$$i_{dif}(t) = \begin{cases} i_{dif}(0)\cos(\omega_0 t) + \frac{-v_{C_{dif}}(0)}{L_{dif}\omega_0}\sin(\omega_0 t) & , 0 < t < t_2 \\ 0 & , t_2 < t < t_3 = \frac{T_{sw}}{2} \\ i_{dif}(t_2)\cos(\omega_0 t) + \frac{-v_{C_{dif}}(t_2)}{L_{dif}\omega_0}\sin(\omega_0 t) & , \frac{T_{sw}}{2} < t < t_5 \\ 0 & , t_5 < t < T_{sw} \end{cases} \tag{4.82}$$

By approximation, the duration of the interval RP (t_2-t_0) is the same as the half resonant period which implies that the initial condition for i_{dif} is zero.

$$i_{dif}(0) = i_{dif}(t_2) = i_{dif}(t_3) = i_{dif}(t_5) = 0 \tag{4.83}$$

The differential current and the corresponding power flow are therefore in phase with the resonant pulse of the common mode circuit and does not influence the boundaries conditions of actual currents $i_{out,1}$ and $i_{out,1}$ given by (4.84) and illustrated in **Fig. 4.25**.

$$\begin{aligned} i_{out,1} &= k_{12} i_{out} + i_{dif} \\ i_{out,2} &= k_{21} i_{out} - i_{dif} \end{aligned} \tag{4.84}$$

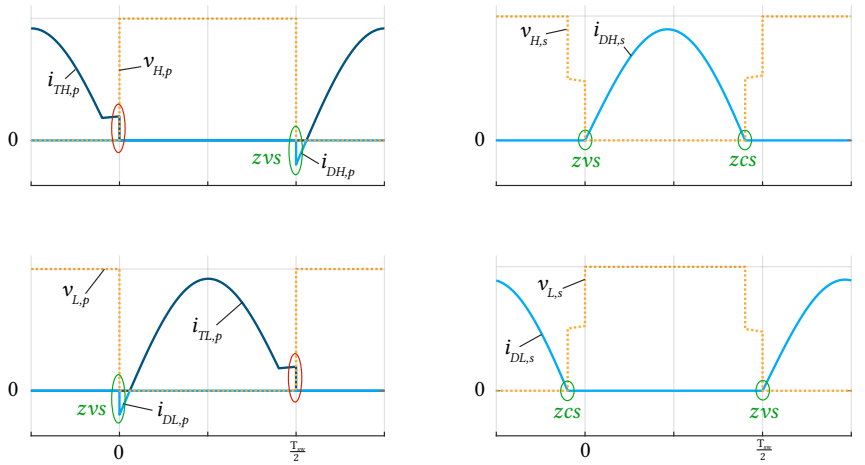


Figure 4.26 IGBT (index T) and diode (index D) voltage and current transitions for the high-side (index H) and the low-side (index L) semiconductor on the primary (index p) and the secondary (index s) of a LLC converter operated below resonant frequency.

4.5 Soft switching operation region

The standard LLC topology is known for its benefits in terms of soft switching. Indeed, in an optimal operation, only two commutations per period are made in a hard way (see **Fig. 4.26**). On the primary side, the semiconductors are hard-switched off while they benefit from ZVS when switching on. The switching losses E_{off} are depending on the turn-off current, mostly related to the magnetizing current, and are therefore related to the design of the circuit and are almost independent from the load conditions. On secondary side, the diode rectifier benefits from ZVS at the turn-on and zero-current-switching (ZCS) at the turn-off.

4.5.1 ZVS conditions

On the primary side, for the active switching cells, the circuit benefits from ZVS if the semiconductors can be turned-on under zero voltage. The condition for this being that the turn-on of the semiconductor concerned is triggered after the opposite semiconductor is completely off and thus its output capacitor C_{oes} is charged up to V_{dc}. In addition, the free-wheeling diode of the concerned switch must be in on-state, which implies that its output capacitor is discharged. In order to characterize this behavior from the models previously developed in this chapter, and which do not take into account the precise dynamics of semiconductors (ideal components), two criteria are set to verify the ZVS conditions. Firstly, the current flowing through the switch during the deadtime T_{dt} must be large enough to charge the C_{oes} of the switch turning off from 0 to V_{dc} and discharge the C_{oes} of the switch turning on from V_{dc} switch to 0. This implies the condition in (4.85) where the integral of the current during T_{dt} is referred as a charge Q_a.

$$Q_a = \int_0^{T_{dt}} i_{in}(t)dt > 2V_{dc}C_{oes} = Q_{oes} \tag{4.85}$$

Secondly, the turn-on of the semiconductor must be done before the current goes through zero. In other words, the dead time T_{dt} imposed by the dynamics of the semiconductor must be smaller than t_{RPd}, the duration of the interval RP_d.

$$t_{RPd} > T_{dt} \tag{4.86}$$

Since the calculation of the duration of the RP_d interval is not explicit, it is proposed to estimate it linearly. Indeed, since the current waveform is quasi sinusoidal, its approximation by its tangent at t = 0 gives a pessimistic, but acceptable, approximation of t_{RPd}. Taking the approximation of $i_{in}(t)$ from (4.37), its slope at t=0, namely $\dot{i}_{in0}$, is given by (4.87).

$$\dot{i}_{in0} = \frac{di_{in}(0)}{dt} = \frac{PT_{sw}\omega^2}{2V_{dc}} \tag{4.87}$$

From this, t_{RPd} can be estimated as in (4.88).

$$t_{RPd} \approx \frac{-i_m(0)}{\dot{i}_{in}} = \frac{V_{dc}^2 f_n}{4L_m P\omega^2} \tag{4.88}$$

This gives a design criterion for L_m, which must be chosen so that $t_{RPd} > T_{dt}$ under the conditions of maximum power $P = P_{max}$.

$$t_{RPd} > T_{dt} \implies L_m < \frac{V_{dc}^2 f_n}{T_{dt} 4P_{max}\omega^2} \tag{4.89}$$

Following the same assumption, the charge Q_a can be approximated by the area of the trapeze defined by (4.90) and depicted in **Fig. 4.27**:

$$Q_a \approx \frac{T_{dt} i_m(0)}{2} + \frac{T_{dt}^2 i_m(0)}{2t_1} = \frac{T_{dt} i_m(0)}{2}\left(1 + \frac{T_{dt}}{t_1}\right) \tag{4.90}$$

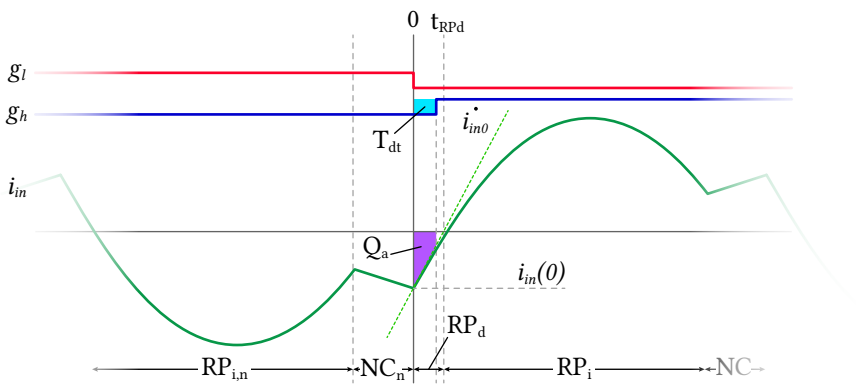


Figure 4.27 Approximation of the charge Q_a, taking in account the dead-time T_{dt} between the turn-off event of the low-side transistor and the turn-on event of the high-side transistor. The gate signals are represented by g_l and g_h.

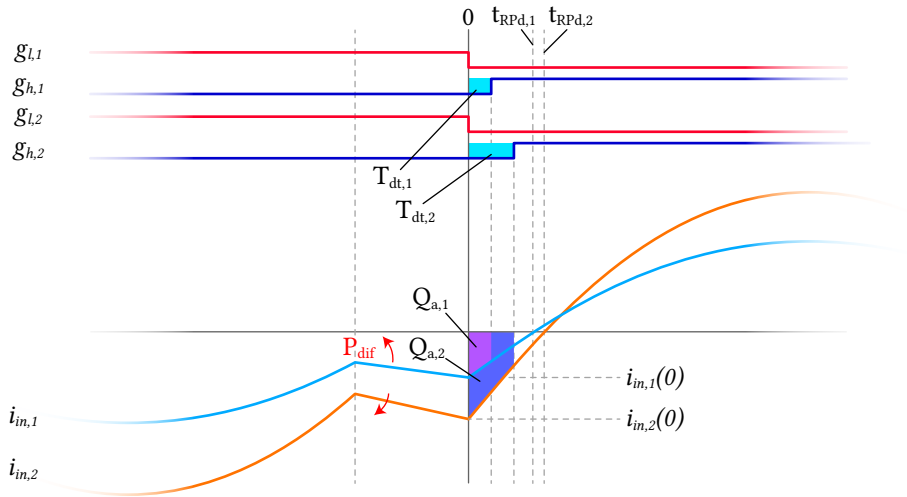


Figure 4.28 Conditions to benefit from ZVS in *DISO* mode. The dead-times $T_{dt,1}$ and $T_{dt,2}$ may vary from one port to the other since they are linked to the blocking voltage class of semiconductor used.

4.5.2 ZVS operation region

In the case of the DISO mode, the conditions (4.85) and (4.86) must be applied to the semiconductors of both active ports.

$$\begin{aligned} Q_{a,1} &= \int_0^{T_{dt,1}} i_{in,1}(t)dt > 2V_{dc,in,1}C_{oes,1} = Q_{oes,1} \\ Q_{a,2} &= \int_0^{T_{dt,2}} i_{in,2}(t)dt > 2V_{dc,in,2}C_{oes,2} = Q_{oes,2} \\ t_{RPd,1} &> T_{dt,1} \\ t_{RPd,2} &> T_{dt,2} \end{aligned} \tag{4.91}$$

With $V_{dc,in,2}$ and $C_{oes,2}$ referred to the primary according to the turn ratio of the transformer. The turn-off current (magnetizing current) being shared between the two input ports, these conditions become intuitively more restrictive than in SISO mode. Moreover, the presence of a differential current will tend to increase the Q_a from one of the port while decreasing the other, as depicted in **Fig. 4.28**. This could lead to the loss of ZVS on this last port.

The linear approximation proposed in (4.87) can also be applied to the current $i_{in,1}$ and $i_{in,2}$ which are given by the model in (4.64).

$$\begin{aligned} i_{in,1}(t) &= k_{12}\, i_{com,in}(t) + i_{dif}(t) \\ i_{in,2}(t) &= k_{21}\, i_{com,in}(t) - i_{dif}(t) \end{aligned} \tag{4.92}$$

And their derivatives are given by:

$$\begin{aligned} \frac{di_{in,1}(t)}{dt} &= k_{12}\frac{di_{com,in}(t)}{dt} + \frac{di_{dif}(t)}{dt} \\ \frac{di_{in,2}(t)}{dt} &= k_{21}\frac{di_{com,in}(t)}{dt} - \frac{di_{dif}(t)}{dt} \end{aligned} \tag{4.93}$$

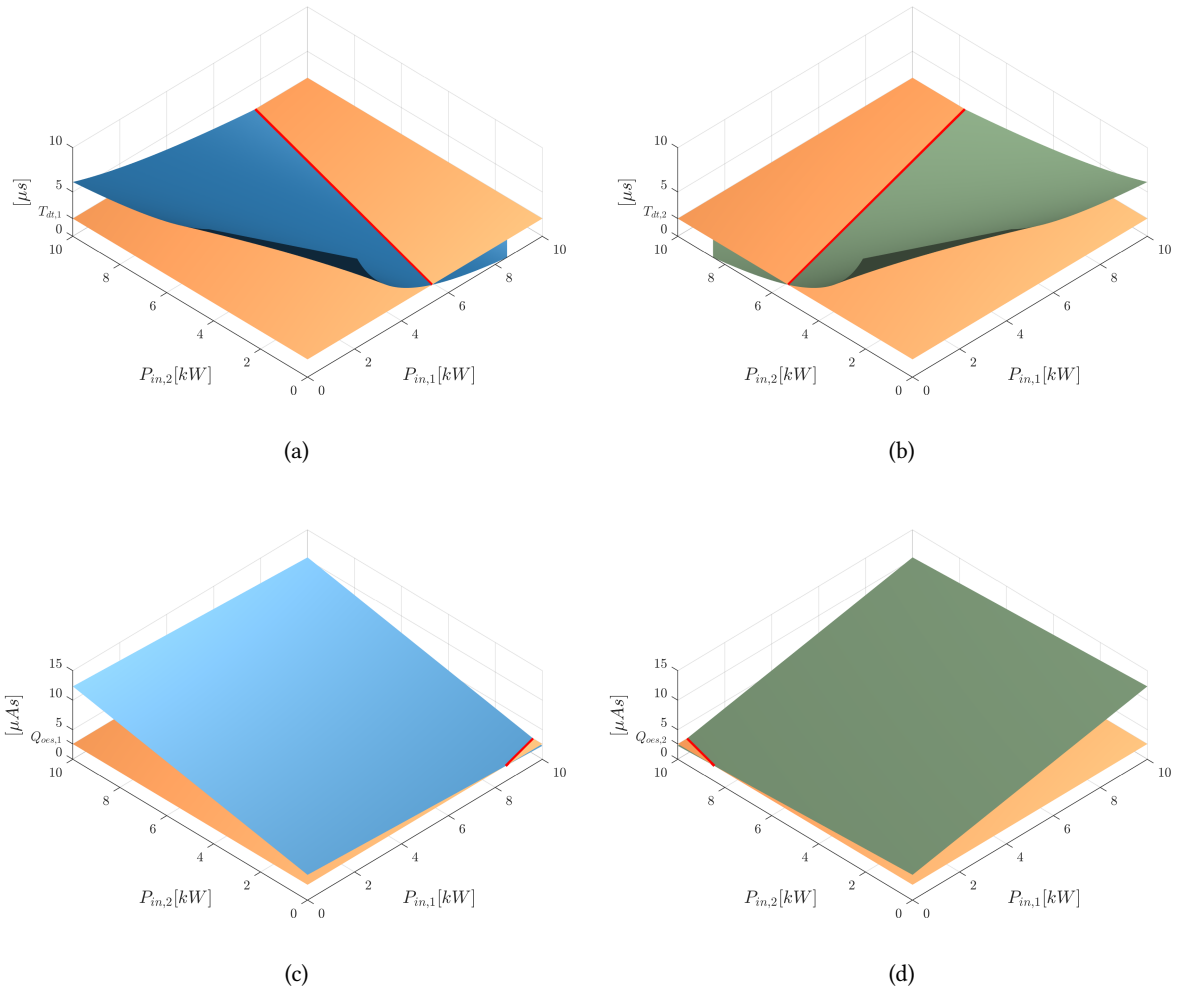


Figure 4.29 Soft switching conditions. The conduction intervals of the diode $t_{RPd,1}$ and $t_{RPd,2}$ are compared with $T_{dt,1}$ (a) and $T_{dt,2}$ (b), which then appear as minimum thresholds. It is the same for $Q_{a,1}$ (c) and $Q_{a,2}$ (d) which are compared with the fixed threshold $Q_{oes,1}$ and $Q_{oes,2}$.

While, the derivative of i_{com} can be evaluated using (4.87) with P_{com}, the derivative of i_{dif} is given by (4.94).

$$\dot{i_{dif}}(t) = \frac{di_{dif}(t)}{dt} \approx -\omega i_{dif}(0)sin(\omega t) + \frac{(V_{dif} - V_{C_{dif}}(0) - R_{dif}i_{dif}(0)/2)}{L_{dif}}cos(\omega t) \tag{4.94}$$

Which gives (4.95) for $t = 0$, with k_{vdif} and k_{idif} such as defined in (4.59).

$$\begin{aligned}\dot{i_{dif}}(0) &= -\omega i_{dif}(0)sin(0) + \frac{(V_{dif} - V_{C_{dif}}(0) - R_{dif}i_{dif}(0)/2)}{L_{dif}}cos(0) \\ &= \frac{V_{dif}(1 - k_{vdif} - k_{idif}R_{dif}/2)}{2}\end{aligned} \tag{4.95}$$

It is thus possible to approximate $Q_{a,1}$ and $Q_{a,2}$ analytically as well as $t_{RPd,1}$ and $t_{RPd,2}$ and to compare

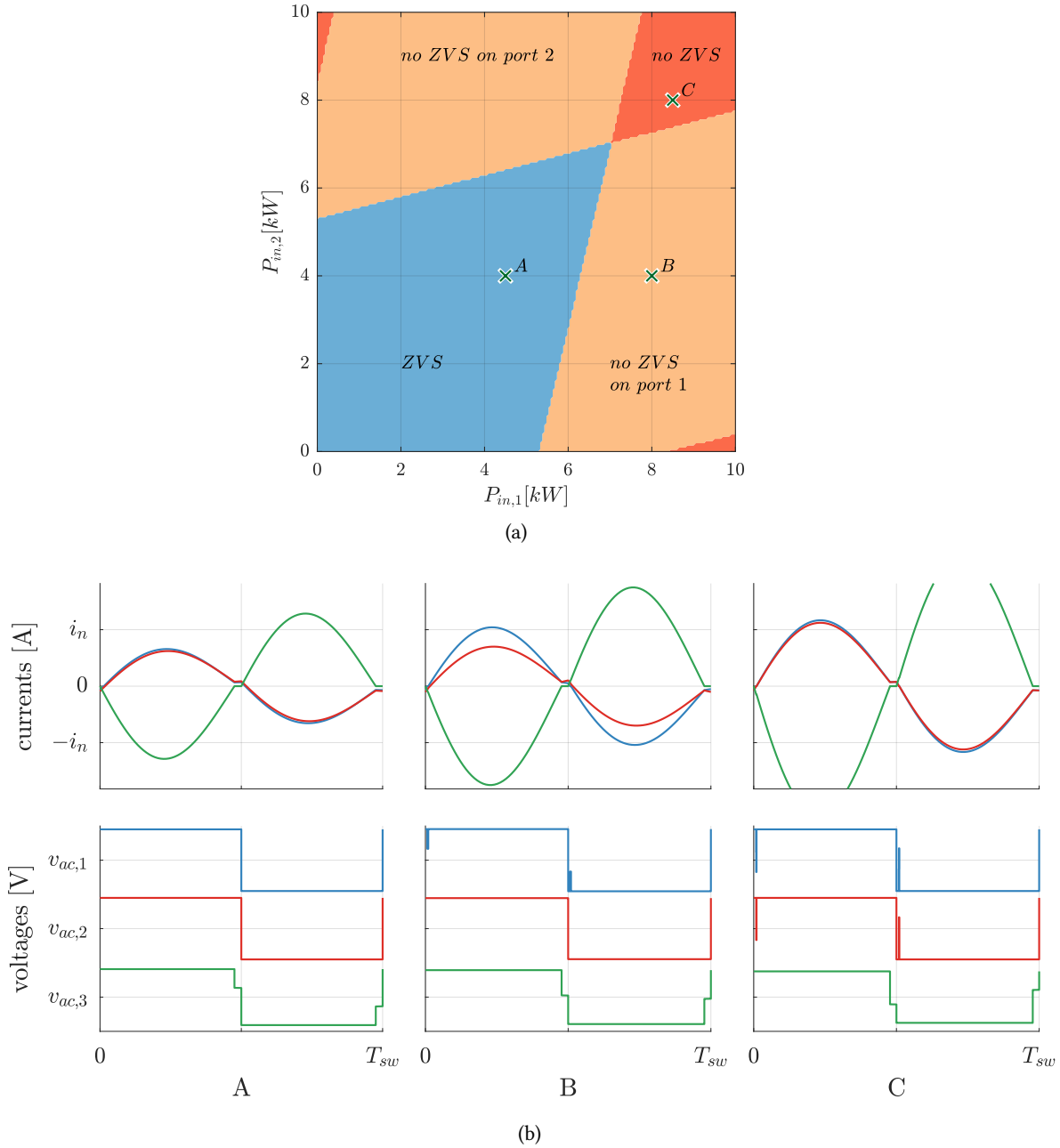


Figure 4.30 Soft switching region (a) and simulated waveforms ($i_{in,1}$ in blue, $i_{in,2}$ in red, i_{out} in green) for various operating points. The example considers a resonant stage with a (1:1:1) turn ratio MFT operated at 5 kHz, for 360 V DC-buses. The resonant tanks are identical on the two input ports, hence the symmetry around the diagonal $P_{in,1} = P_{in,2}$. At the operation point *A*, both ports benefit from ZVS. At the operation point *B*, the interval $t_{RPd,1}$ is shorter than the dead-time, and the ZVS is lost on port 1. At operation point *C*, the load is such that the slopes at the switching instant of the two currents is too large, $t_{RPd,1}$ and $t_{RPd,2}$ are too short and the soft switching is lost on both ports.

them to $Q_{oes,1}$ and $Q_{oes,2}$, and respectively $T_{dt,1}$ and $T_{dt,2}$ over the entire operating range defined by $P_{in,1}$ and $P_{in,2}$. The **Fig. 4.29** illustrates the trend of these four variables on the plane ($P_{in,1}$, $P_{in,2}$).

If any of the conditions are not satisfied, then the soft switching is lost on one of the two ports. An area of ZVS operation can thus be characterized for a given R_{dif} as illustrated in **Fig. 4.30**. This ZVS area can be used to establish an approximation of the efficiency over the operation plane.

4.5.3 Efficiency approximation

As shown before, the ZVS behavior and the efficiency in DISO mode are relying on the parasitic resistor R_{dif}. The value of R_{dif} comprises all the various losses affecting the circulating power flow between the two input ports and is therefore difficult to be evaluated based on theoretical parameters only. Nevertheless, the measurement of experimental values from a prototype can give a good estimation of the coefficient k_{pdiv} and k_{idiv} introduced in (4.59) and (4.62). The **Fig. 4.31** depicts some measurements from the LV prototype described in Appendix B. The experiment considers a submodule in DISO1 mode, so the two inputs are the port 1 and 3, while the port 2 is the load port.

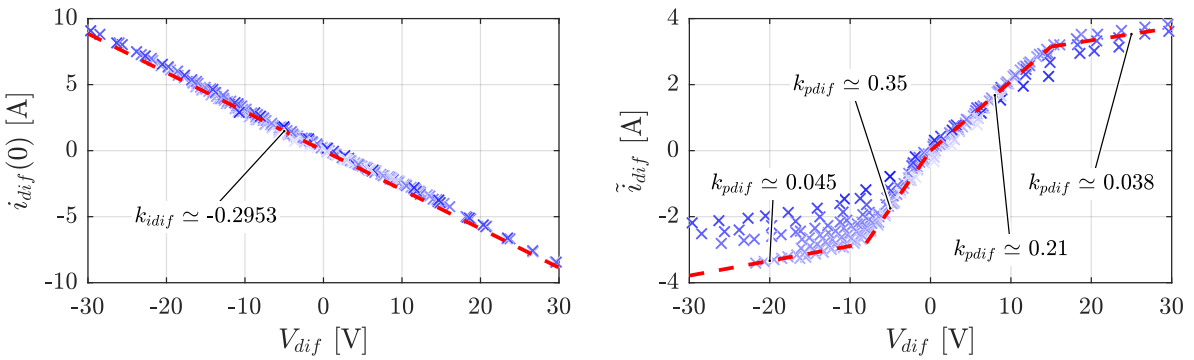


Figure 4.31 (a) differential current at the switching instant $i_{dif}(t = 0)$ in function of the differential voltage V_{dif} applied between the two input ports. k_{idif} can be estimated around -0.2953, from the measurements. (b) RMS value of the differential current $\tilde{i}_{dif}$ in function of the differential voltage. In contrast to k_{idif}, k_{pdif} is greatly influenced by R_s which explains the different slopes above $V_{dif} = 20$ V and below $V_{dif} = -8$ V. Indeed, in these two regions, the ZVS is lost which has the effect of increasing drastically the losses and thus the value of R_{dif}, decreasing consequently the slope k_{pdif}. In other terms, when the ZVS is lost, more differential voltage is needed for the same amount of circulating power. From the values presented in this figure, R_{dif} can be estimated using (4.59): $k_{pdif} = 0.045 \Rightarrow R_s = 14.3\Omega$, $k_{pdif} = 0.35 \Rightarrow R_{dif} = 0.22\Omega$, $k_{pdif} = 0.21 \Rightarrow R_{dif} = 0.11\Omega$, and $k_{pdif} = 0.038 \Rightarrow R_{dif} = 15.9\Omega$.

The measurement show clearly the relation between V_{dif} and the circulation current i_{dif}, and the coefficients can be identified from the curves and be used to calculate the theoretical turn-off currents for both input ports over the whole operation plane. The **Fig. 4.32** shows a comparison between measured values from the experiment and the theoretical values using those linear approximations of k_{pdiv} and k_{idiv}.

From those turn-off currents $i_{off1,3}$ and the ZVS conditions described in Section 4.5.2, the efficiency can be evaluated using the characteristics specified in the semiconductors datasheets, namely the

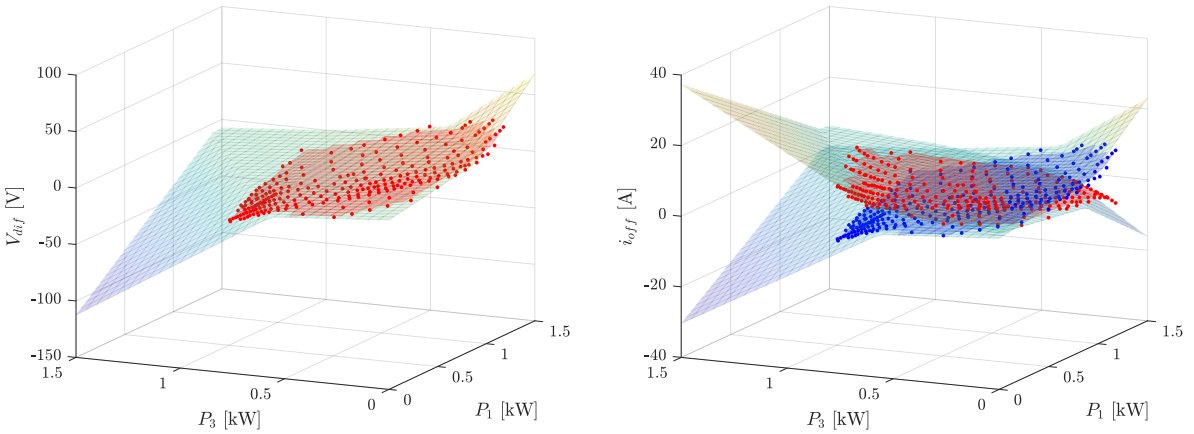


Figure 4.32 (a) Differential voltage over the operating plane. As mentioned in **fig. 4.31b**, a higher differential voltage is needed when the ZVS is lost (on the upper left and lower right corners of the plane (P_1,P_3)). The points in red are experimental results and are well in accordance with the model. (b) i_{off1} (in red) and i_{off3} (in blue) over the operating plane. The experimental results are also well in accordance with the model.

on-state resistance R_{on}, the forward voltage $V_{ce,on}$ and the switching losses $E_{on}(i, v)$ and $E_{off}(i, v)$. In the ZVS area, only turn-off losses and conduction losses are counted for the two input ports while only conduction losses are counted for the output port. It gives for the ZVS area:

$$\begin{aligned} P_{loss_1} &= P_{cond_1} + P_{off_3} &&\approx \tilde{i}_1^2 R_{on,1} + \tilde{i}_1 V_{ce,on,1} + 2 f_{sw} E_{off,1}(i_{off1}, V_{dc1}) \\ P_{loss_3} &= P_{cond_3} + P_{off_3} &&\approx \tilde{i}_3^2 R_{on,3} + \tilde{i}_3 V_{ce,on,3} + 2 f_{sw} E_{off,3}(i_{off3}, V_{dc3}) \\ P_{loss_2} &= P_{cond_2} &&\approx \tilde{i}_2^2 R_{on} + \tilde{i}_2 V_f \end{aligned} \tag{4.96}$$

In the area where the ZVS is lost for one of the two input ports, the turn-off losses are replaced by reverse-recovery losses and turn-on losses. It gives for instance in the area where the ZVS is lost for port 3:

$$\begin{aligned} P_{loss_1} &= P_{cond_1} + P_{off_3} &&\approx \tilde{i}_1^2 R_{on} + \tilde{i}_1 V_{ce,on,1} + 2 f_{sw} E_{off,1}(i_{off1}, V_{dc1}) \\ P_{loss_3} &= P_{cond_3} + P_{on_3} + P_{rr_3} &&\approx \tilde{i}_3^2 R_{on} + \tilde{i}_3 V_{ce,on,3} + 2 f_{sw} E_{on,3}(-i_{off3}, V_{dc3}) + 2 f_{sw} E_{rr,3}(i_{off3}, V_{dc3}) \\ P_{loss_2} &= P_{cond_2} &&\approx \tilde{i}_2^2 R_{on} + \tilde{i}_2 V_f \end{aligned} \tag{4.97}$$

It has to be noted that since $i_{off1} + i_{off3}$ is equal to the magnetizing current i_m at the switching instant and is therefore constant and depending only on the design of the transformer. It means that when the ZVS is lost for the port 3, i_{off3} becomes negative and i_{off1} becomes bigger than the magnetizing current. In other terms, not only reverse recovery losses appear on the port 3, but the turn-off losses on the port 1 are further increased. This has the effect of drastically decreasing the efficiency in this operation region.

Finally, the theoretical efficiency is given by:

$$\eta = \frac{P_1 + P_3 - P_{loss_1} - P_{loss_3} - P_{loss_3}}{P_1 + P_3} \tag{4.98}$$

The **Fig. 4.33** depicts the efficiency in DISO1 mode, from the model and from the experimental results. Even though the efficiency of the LV prototype is rather low , namely 94% at maximum (it has to be reminded that it is not resulting from any optimal design), some qualitative conclusions can be drawn.

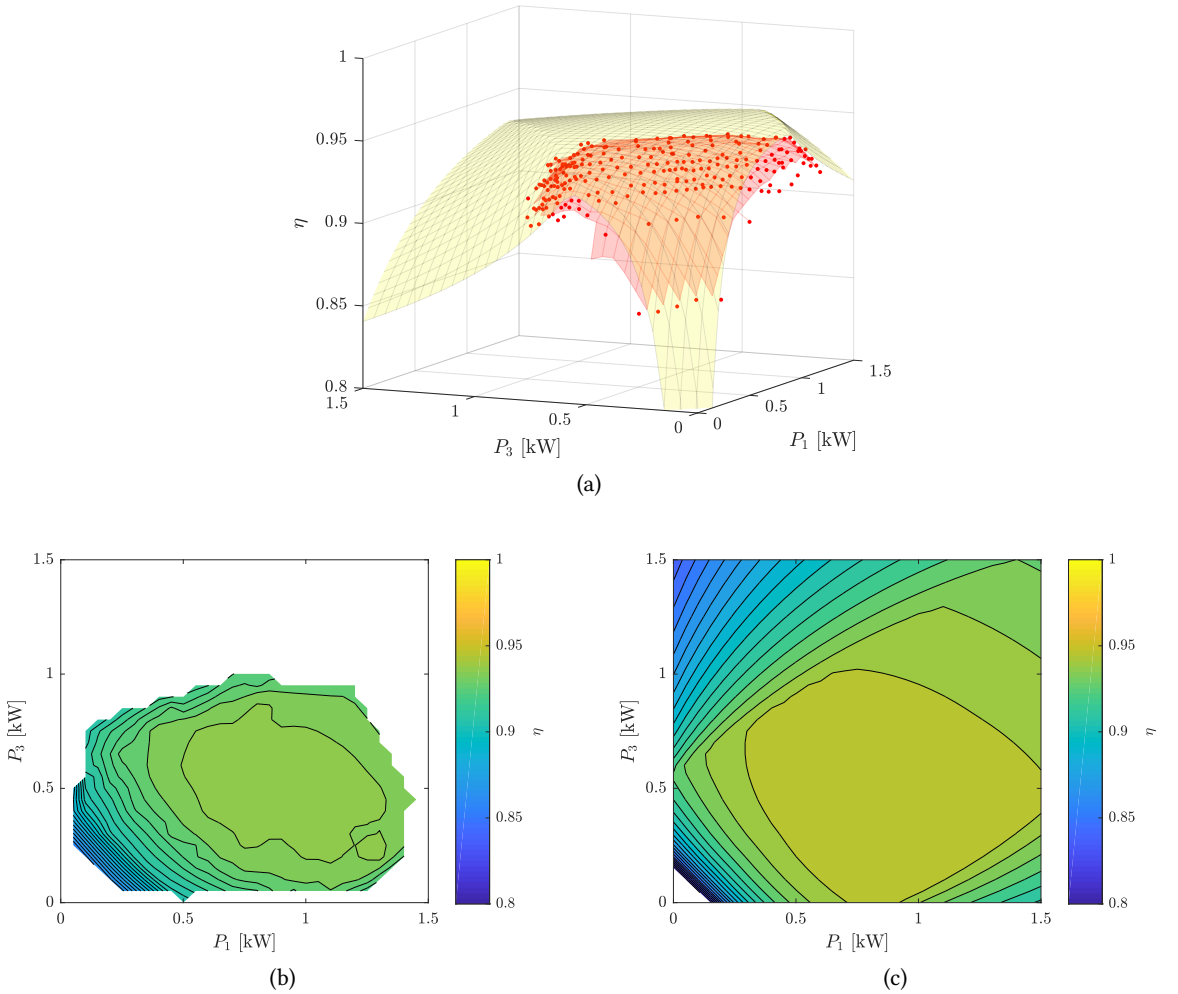


Figure 4.33 (a) The theoretical (in yellow) and experimental (in red) efficiency of the DC-transformer part over the whole operation plane. The theoretical efficiency is slightly higher than the reality, but the general shape is well in accordance which confirms the validity of the model. (b) experimental efficiency. (c) theoretical efficiency. From both (b) and (c), it may be noticed that the efficiency is very low for light load and when the ZVS is lost. It is also decreasing at higher loads, mainly because of the conduction losses on the output port. Indeed, the forward voltage and the on-state resistance of the semiconductors used as diode rectifier on the port 2 become higher than the one of the IGBT of the port 1 and 3. Finally, it has to be noticed that the area with the highest efficiency is located on the axis ($P_1 = \frac{2}{3}P_{tot}$,$P_3 = \frac{1}{3}P_{tot}$) defined as the natural power sharing ratio.

4.6 Discussion

This chapter proposes the models of the resonant stage, in all the modes of operation, based on the assumption that the three resonant tanks have the same resonant frequency. This makes it possible to derive equivalent circuits common to all the ports and to limit the number of different intervals to two per half-period, and makes the analytical approximation of the waveforms in steady state possible. The three modes SISO, DISO and SIDO are modeled separately. In the case of DISO and SIDO modes, the models highlight that the power is shared in a natural way according to fixed ratios that depend on the system parameters. The presence of a differential voltage between the inputs (in the case DISO) or between the outputs (in the case SIDO) implies a circulating power flow which allows to move away from the initial sharing ratio. If in SIDO modes this circulating power does not affect the soft switching operation, in DISO mode, it can lead to the loss of ZVS conditions on one of the ports. A characterization of the operating region benefiting from ZVS is also possible thanks to the proposed model, but it relies highly on the value of R_{dif} which depends on the losses (conduction and switching) of the semiconductors as well as the losses linked to the MFT (core and winding losses). The proper characterization of R_{dif} would need the detailed model of the semiconductor losses (LTspice) and the MFT (FEM) or can be based on experimental measurement such as presented in **Fig. 4.31**. Then, the efficiency can be estimated in a relatively precise way over the whole operation plane. This helps to highlight the areas suffering from poor performances, namely when power sharing ratio is far from the one defined by the resonant tank parameters. At the opposite, the conditions are better around the axis defined by the resonant inductors ratio. This criterion has to be taken in account for the design of such topology.

5
MEG design rules and guidelines

This chapter presents the sizing of all the elements of the MEG converter, based on the specifications from a case study application. First, the number of submodules and the blocking voltage class of the semiconductors are chosen, based on commercial devices. The switching frequencies of the three different stages are selected in accordance with the thermal dissipation capability of the chosen semiconductors. Then, the design of the resonant stage is presented using the theoretical outcomes from the Chapter 4. Finally, the components of the regulation stages are sized to meet current and voltage ripples specifications.

5.1 Converter ratings

To demonstrate the design rules for the MEG, ratings are selected in a way to be illustrative of medium voltage applications as well as in accordance with available laboratory infrastructures, for future developments. Thus, 10 kV is considered on the side of the MVDC grid and 750 V on the side of the LVDC grid for a total power (P_{main}) of 500kW. The presence of galvanic isolation by means of MFTs, allow for variety of voltage levels to be selected for the storage side. This voltage has been limited to 450 V for a power $P_{storage}$ of 100 kW, corresponding to the maximal ratings of a super-capacitor bank, also part of the laboratory infrastructure. A summary of the ratings used for the case study and the simulation is given in Table **5.1**, which also shows the currents corresponding to the required powers.

Table 5.1 Rating at the full converter level used for the case study.

Port i	Nominal power	v_i	i_i
MV	P_{main} = 500 kW	10 kV	50 A
LV	P_{main}	750 V	750 A
ES	$P_{storage}$ = 100 kW	450 V	500 A

It has to be noted that both MV and LV ports have to withstand a maximum power equal to P_{main} + $P_{storage}$, in SIDO and DISO modes for instance.

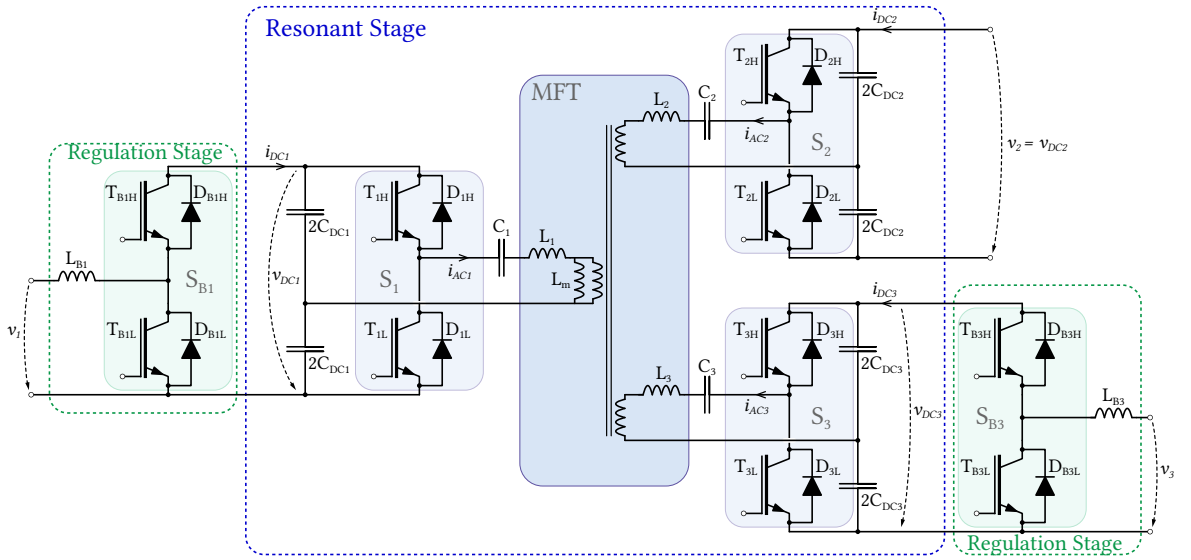


Figure 5.1 One MEG submodule. The number N_s of submodule defines the voltage ratings of the DC-bus from which all the component are sized.

5.2 Number of levels and the semiconductors voltage class

The number N_s of submodules, the DC-bus voltage and therefore the semiconductor blocking voltage class are closely related. Indeed, an increased number of submodules implies a reduced MV side DC-bus voltage and therefore the use of lower blocking voltage class semiconductors which can be operated at higher frequencies. A global optimization of the system, taking into account all the losses (magnetic, conduction and switching) as well as volumes and weights would be necessary in order to define an optimal N_s. For the present case study, the aim is only to propose a design method as proof of concept and not to present any optimization process. Thus, the selection of N_s is essentially based on the availability of commercial devices meeting voltage and current requirements.

In terms of voltage, without considering any redundancy by the addition of extra submodules, the DC-bus voltage on the MV side is selected so that the converter can be operated in degraded mode with a bypassed submodule. In this case, the sum of the remaining DC-buses of the $N_s - 1$ submodules must be greater than the MV grid voltage v_{MV}.

$$V_{DC,1} \geq \frac{v_{MV}}{N_s - 1} \tag{5.1}$$

Then, the maximum value of the average current though the MV side switching cells (S_1 and S_{B1}) can be approximated by (5.2).

$$i_{dc,1} = \frac{P_{main} + P_{storage}}{N_s V_{DC,1}} \tag{5.2}$$

The Table **5.2** gives the semiconductors specification in function of the number of submodules.

Table 5.2 MV side semiconductors requirements in function on the number of cascaded submodules. V_1 is the submodule input voltage, $v_{DC,1}$ is the DC-bus voltage according to (5.1), V_b is the blocking voltage class, $i_{dc,1}$ is the average current according to (5.2) and f_s is the expected and achievable operating frequency for the corresponding semiconductor class.

N_s	V_1 [kV]	$V_{DC,1}$ [kV]	V_b [kV]	$i_{dc,1}$ [A]	f_s [kHz]
2	5	10	20	30	
3	3.33	5	10	40	
4	2.5	3.33	6.5	45	1
5	**2**	**2.5**	**4.5**	**48**	**5**
7	1.43	1.66	3.3	52	10
11	0.91	1	1.7	55	25

The choice of 2 or 3 submodules implies the use of high-voltage wide band-gap semiconductors which are not yet commercially available and which are thus not considered in the scope of this work. Moreover, the relatively limited switching frequency of the 6.5 kV IGBTs make them not attractive for a multiport resonant converter aimed to be operated at high frequency. Thus, N_s is chosen as 5, which implies the use of 4.5 kV semiconductors. Some IGBT modules from the market fulfill the requirement (4.5 kV, 50 A) and are thus considered as candidates for the switching cell S_1 and S_{B1}:

- ABB 5SNG0150P450300
- Powerex QID4515001
- Hitachi MBM200H45E2-H

On the LV side, the DC-bus is directly connected to the low voltage grid, which imposes its voltage.

$$V_{DC,2} = v_{LV} = 750\,\text{V} \tag{5.3}$$

Thus, 1.7 kV semiconductors are required on the port 2. The average current through the port 2 is given by:

$$i_{dc,2} = \frac{P_{main} + P_{storage}}{N_s V_{DC,2}} = 160\,\text{A} \tag{5.4}$$

For the port dedicated to the energy storage, the DC-bus voltage must be higher than the maximum voltage v_{ES} (i.e. 450 V). Technically, a lower (and faster) semiconductor class than the one used for the LV port could have been used, but the switching frequency of the resonant stage being limited because of the (slow) semiconductor of port 1, this becomes of less advantage. The chosen semiconductor class is therefore the same as for the port 2 and the DC-bus voltage of the storage ports is set with:

$$V_{DC,3} = 750\,\text{V} \tag{5.5}$$

And the maximal value of the average current in the port 3 is given by:

$$i_{dc,3} = \frac{P_{storage}}{N_s V_{DC,3}} = 27\,\text{A} \tag{5.6}$$

Following commercial IGBT modules fulfill the requirements and are thus considered as candidates for the switching cell S_2, S_3 and S_{B3}:

- Fuji 2MSI400VE-170-53
- Semikron SKM 400GB176D
- ABB 5SND 0800M170100

The ratings at the submodule level (see **Fig. 5.1**), considering a number of submodules N_s equal to 5, are given in Table **5.3** and are used for the design of the DC-transformer stage in the next section.

Table 5.3 Ratings at the submodule level, considering $N_s = 5$

Port k	P_k	v_k	v_{DCk}	i_k
1	100 kW	2 kV	2.5 kV	50 A
2	100 kW	750 V	750 V	160 A
3	20 kW	450 V	750 V	100 A

Depending the voltage adaptation ratio (MV/LV), the DC-transformer part may suffer from non-optimal design on various aspects:

- As mentioned in Chapter 3, the choice of the switching frequency is the result of a trade-off, which means that none of the semiconductors are used at their optimal operation point.
- The soft switching conditions of the active port(s) depend on the parasitic capacitance of the semiconductors and on the turn-off current in the resonant circuit which leads to the design of the magnetizing inductance of the MFT. If it is sized in order to benefit from ZVS on one port, this current will not be the optimal one on the other ports, due the turn ratio of the MFT. For instance, when the MFT and its magnetizing inductance is dimensioned in order to benefit from ZVS on the MV side, where the voltage is higher, the turn-off current will be higher on the LV side when the power is flowing on the other direction. The LV side will still benefit from ZVS, but the turn-off losses won't be reduced to their minimum.
- Resonant converters have the particularity to have most of their switching losses on the primary side, which has to be designed (thermally) consequently. In order to provide a fully bidirectionality, all ports have to be sized as an input stage, which means that when a port is an output, its thermal design is greatly over-sized. This implies that the converter is never used at optimal conditions, in terms of power to volume ratio or power to weight ratio, on all the ports.

The class of semiconductors of the LV side and the ES side are set by their respective voltage specifications. The only degree of freedom is the number of submodules connected in series on the MV side and in parallel on the LV side. Therefore, this number affects the DC bus voltage and the choice of the blocking voltage class used on the MV port as well as the current ratings of the semiconductors of the LV side.

Intuitively, the best conditions, in terms of switching mechanism, are reached when the DC-bus voltage is the same on the port 1 (MV side) and 2 (LV side) of the submodule, the third being of

less importance since its power rating specifications are limited. In this case, the turn ratio of the MFT is 1:1:x, the device voltage and current specifications are the identical and the same model of semiconductors can be used on both main sides of the MFT, thus benefiting from the optimal switching frequency, and the good blocking voltage to maximum current ratio. Additionally, the magnetizing inductance of the MFT is the same, seen from both main ports, and can be designed to produce the optimal turn-off current for both power flow directions.

Nevertheless, the insulation requirements is not affected by the number of submodules and each MFT isolation has to withstand the entire MV voltage. Even though with increasing number of submodule, the section of the winding and the distance between the turns could be reduced, the isolation distance or the thickness of the material between the primary and secondary sides have to be maintained. This could result in an increased volume, weight and cost, when considering a big number of submodules.

Only an overall optimization considering the application requirements and specific targets in terms of cost, volume, weight and efficiency can highlight the best solution. This work is focused on the system concept and is only providing a possible design guideline, so the numbers defined in the beginning of this chapter are used without further optimization.

5.3 Resonant stage - DC transformer

5.3.1 Switching frequency

The factors limiting the switching frequency are the switching losses on the MV side. In order to select the maximum achievable switching frequency, the maximum dissipable losses power $P_{loss,max}$ must be determined.

The specifications of the three commercial modules candidates for S_1, in terms of junction-to-case and case-to-heat-sink thermal resistance, are given in the Table **5.4**.

Table 5.4 Thermal specification of **4.5 kV** IGBT candidates

Model	I_c [A]	R^{th}_{j-c} [°C/W]	R^{th}_{c-f} [°C/W]	P_{tot} [W]
ABB 5SNG0150P450300	150	0.062	0.048	1450
Powerex QID4515001	150	0.087	0.018	1440
Hitachi MBM200H45E2-H	200	0.052	0.032	

In the case of a water-cooled system, the maximum loss power P^{water}_{max} could be close to P_{tot}, but in the case of forced air cooling, the thermal resistance of the heat-sink has to be taken into account. For a surface corresponding to the chosen package (140 mm×73 mm) can be approximated around 0.04 °C/W[113]. And the maximum power that can be dissipated may be estimated using (5.7).

$$P^{air}_{max} \simeq \frac{\Delta_T}{\frac{R^{th}_{j-c}}{2} + R^{th}_{c-f} + R^{th}_{f-a}} \tag{5.7}$$

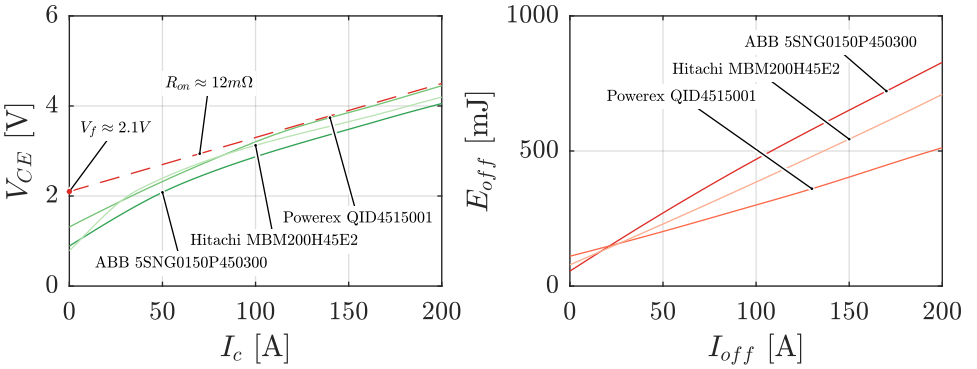


Figure 5.2 Voltage drop and turn-off losses characteristics for the S_1 candidates. The voltage drop can be linearized using R_{on}.

It results in a value around 860 W for the losses per module for the *ABB 5SNG0150P450300*[114] model for a 100 °C temperature rise. The loss power produced by the switching cell S_1 of the submodule can be calculated from the datasheet information and from the approximate current waveforms. The voltage drop V_{CE} on the active switch is linearly approximated in function of the current (5.8) with the on-state resistor R_{on}, and the forward voltage V_f as shown in **Fig. 5.2**.

$$V_{CE} = V_f + R_{on} I_c \tag{5.8}$$

The worst case in terms of losses for the S_1 switching cell is the mode SISO1, when the port 1 is providing the main power and supporting the magnetizing current as well. In this case, the current waveform used for loss calculation is approximated over a half switching period by:

$$i_{S_1}(t) \approx \hat{i}_{S_1} \sin\left(2\pi f_{sw} t\right) - i_{off} + \frac{4 i_{off}}{T_{sw}} \quad \text{with} \quad \hat{i}_{S_1} = \pi i_{dc,1} \tag{5.9}$$

where i_{off} is the magnetizing current at the switching instant. The average current $\bar{i}_{S1}$ and RMS current $\tilde{i}_{S1}$ through the IGBTs of S_1 can be evaluated with

$$\begin{aligned} \bar{i}_{S1} &= \frac{2}{T_{sw}} \int_0^{T_{sw}/2} i_{S1}(t) dt = \frac{2\hat{i}_{S1}}{\pi} \\ \tilde{i}_{S1} &= \sqrt{\frac{2}{T_{sw}} \int_0^{T_{sw}/2} i_{S1}^2(t) dt} = \frac{\sqrt{3\hat{i}_{S1} + 2 i_{off}^2}}{\sqrt{6}} \end{aligned} \tag{5.10}$$

The conduction losses are thus evaluated using the forward voltage V_f and the on-state resistance R_{on} of the IGBT of S_1

$$P_{cond} = \bar{i}_{S1} V_f + \tilde{i}_{S1}^2 R_{on} \tag{5.11}$$

Thanks to ZVS behavior, the switching losses are limited to the turn-off losses of the active port and thus depend essentially on the magnetizing current as described with (5.12). The turn-off energy is extrapolated from component datasheet curves (cf. **Fig. 5.2**)

$$P_{sw} = 2 f_{sw} E_{off}(i_{off}) \tag{5.12}$$

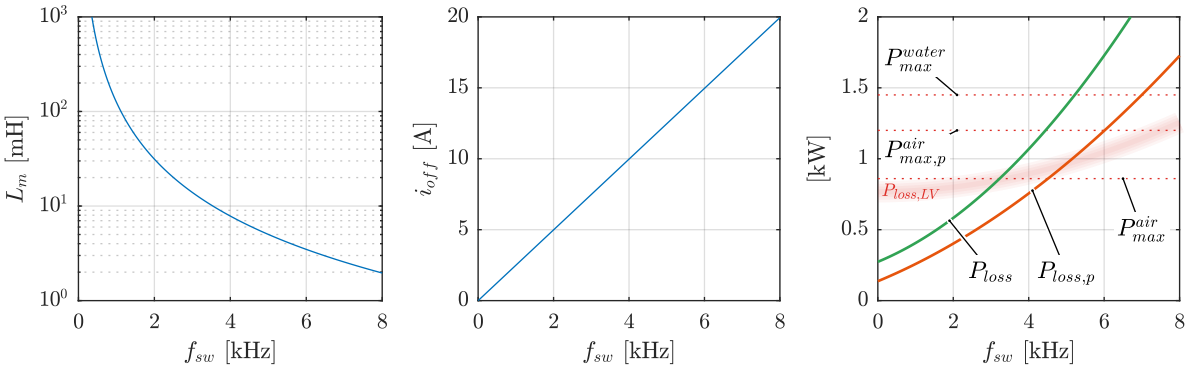


Figure 5.3 Maximal L_m, minimal turn-off current and losses over the frequency. The losses on the LV side are evaluated the same way as for the MV side, considering SISO2 mode. Below **3 kHz**, the losses are larger on the LV side than on the MV size which means that the benefits from ZVS in terms of enabling higher switching frequencies are not fully exploited.

With the turn-off current i_{off} given by:

$$i_{off} = \frac{v_{DC,1}}{8 f_{sw} L_m} \tag{5.13}$$

where L_m is given according to the ZVS criterion defined in (4.89). The losses per module, given by:

$$P_{loss} = P_{cond} + P_{sw} \tag{5.14}$$

are illustrated in function of the switching frequency in **Fig. 5.3**. It is visible that the maximum dissipable power is reached at around 3 kHz. Thus, it is proposed to use two modules in parallel, in order to obtain a larger dissipation surface and lower losses per module. The loss power per module becomes $P_{loss,p}$ and the dissipable power is increased to $P_{max,p}^{air}$. This way, the system can be operated at a higher frequency and f_{sw} is set at 5 kHz which corresponds to the switching frequency for which the losses per module on the MV side are similar to losses per module on the LV side ($P_{loss,LV}$).

5.3.2 Choice of L_m

The choice of L_m is essentially based on the criterion defined in Chapter 4 by (4.89). L_m must be such that the current through the device to be turned on is negative (anti parallel diode conduction) during the entire dead-time T_{dt}. This condition leads to the criterion:

$$t_{RPd} > T_{dt} \implies L_m < \frac{V_{dc}^2 f_n}{T_{dt} 4 P_{max} \omega^2} \tag{5.15}$$

The dead-times are taken from the datasheets and are given in (5.16) for the MV side IGBT (ABB 5SNG0150P450300 [114]) and the LV side IGBT(Semikron SKM 400GB176D [115]) with a safety margin coefficient k_s of 1.2.

$$\begin{aligned} T_{dt,MV} &= k_s \left((t_{fall,max} - t_{rise,min}) + (t_{delay,off} - t_{delay,on}) \right) \\ &= 1.2 \times ((590\,\text{ns} - 120\,\text{ns}) + (1720\,\text{ns} - 510\,\text{ns})) \approx 2\,\mu\text{s} \\ T_{dt,LV} &= 1.2 \times ((145\,\text{ns} - 55\,\text{ns}) + (880\,\text{ns} - 330\,\text{ns})) \approx 770\,\text{ns} \end{aligned} \tag{5.16}$$

The $T_{dt,MV}$ being the most restrictive, it is used to size L_m with a certain margin in (5.17) with f_n = 0.95 (cf. (5.24)).

$$L_m \leq \frac{V_{DC,1}^2 f_n}{T_{dt,MV} 4(P_{main} + P_{storage})(2\pi f_{sw})^2} = 7.5\,\text{mH} \implies L_m = 5\,\text{mH} \tag{5.17}$$

5.3.3 Power sharing ratio

The model presented in Chapter 4 shows that the natural power sharing in DISO mode is depending on the ratio of the resonant inductances. This ratio also defines the distribution between the common mode power P_{com} and the circulating power P_{dif} for any operating point.

As show in Chapter 4, the efficiency is higher on the axis defined by the ratio, for which the circulating power is zero, first because the ZVS is ensured in this region, second because there is no conduction loss due to the circulating current. The two modes $DISO1$ and $DISO2$ consider the power sharing between P_{main} and $P_{storage}$ (or P_1,P_2 and P_3 at the submodule level). Thus, by defining the inductance ratio equal to the power ratio, an optimal behavior is ensured when both input ports are at rated power.

It gives, with L_3 reported to the primary as L_3':

$$\begin{aligned} k_{13} &= \frac{P_{main}}{P_{main} + P_{storage}} = \frac{L_3'}{L_1 + L_3'} = \frac{5}{6} \\ k_{31} &= \frac{P_{storage}}{P_{main} + P_{storage}} = \frac{L_1}{L_1 + L_3'} = \frac{1}{6} \end{aligned} \tag{5.18}$$

The same applies for the port 2, since the power ratings are the same for LV and MV ports, with:

$$\begin{aligned} k_{23} &= \frac{P_{main}}{P_{main} + P_{storage}} = \frac{L_3''}{L_2 + L_3''} = \frac{5}{6} \\ k_{32} &= \frac{P_{storage}}{P_{main} + P_{storage}} = \frac{L_2}{L_2 + L_3''} = \frac{1}{6} \end{aligned} \tag{5.19}$$

This allows to highlight the ratio k which is given by the ration of the powers:

$$\frac{L_3'}{L_1} = \frac{L_3''}{L_2} = \frac{P_{main}}{P_{storage}} = 5 = k \tag{5.20}$$

which also implies that the resonant inductances of ports 1 and 2 (reported on one side or the other) have the same value.

$$L_2' = L_1 \tag{5.21}$$

Finally, the inductance ratio is set and the three inductance values can be given as a function of a resonant tank parameter L which is further designed in next section.

$$\begin{aligned} L_1 &= L \\ L_2' &= L \\ L_3' &= kL \end{aligned} \tag{5.22}$$

5.3.4 Sizing of the resonant tank

The first step in the sizing of the resonant tank is the choice of the resonant frequency. In order to benefit from ZCS on the secondary side, the conduction period, referred as "interval *RP*" in Chapter 4 and equal to half of the resonant period T_r, must be shorter than the switching period T_{sw} and therefore f_n, defined as the ratio between the switching frequency and the resonance frequency must satisfy the condition:

$$f_n = \frac{T_r}{T_{sw}} = \frac{f_{sw}}{f_r} = \frac{2\pi f_{sw}}{\omega_r} \leq 1 \tag{5.23}$$

In practice, the resonant frequency may vary slightly. First, because of the losses that act as a damping resistance and tend to lengthen the switching period. Second, because of the tolerances on components that can introduce further deviation from ideal conditions. Based on the standard tolerances τ of 5%, f_n is calculated with the following margin:

$$f_n = 1 - \tau = 0.95 \tag{5.24}$$

Then, the resonant frequency being common to the three resonant tanks, such as described in (5.25)

$$\omega_r = \frac{1}{\sqrt{L_1 C_1}} = \frac{1}{\sqrt{L_2 C_2}} = \frac{1}{\sqrt{L_3 C_3}} = \frac{1}{\sqrt{L_r C_r}} \tag{5.25}$$

The value of C_1, C_2 and C_3 is deducted according to L_1, L_2 and L_3 which are linked together by the L parameter of (5.20). The last step in the design of the resonant tank is then to choose this L with a value insuring ZVS behavior over the entire range of use in SISO and SIDO mode.

For the six SISO modes (see Chapter 3), the equivalent resonant inductance is given by (5.26) with γ that can be approximated by 1 if the resonant inductance is considerably smaller than L_m. In addition, they can be expressed according to the parameters L and k from (5.20).

$$\begin{aligned} L_{SISOa} &= L'_{SISOb} = L_1 + \gamma L'_2 \approx L_1 + L'_2 = 2L \\ L_{SISOc} &= L'_{SISOe} = L_1 + \gamma L'_3 \approx L_1 + L'_3 = (1+k)L \\ L_{SISOd} &= L'_{SISOf} = L_2 + \gamma L''_3 \approx L_2 + L''_3 = (1+k)L'' \end{aligned} \tag{5.26}$$

In SIDO mode, the equivalent resonant inductances are given by L_{com} in (4.73) and become:

$$\begin{aligned} L_{SIDO1} &= L_1 + \gamma \frac{L'_2 L'_3}{L'_2 + L'_3} \approx L_1 + \frac{L'_2 L'_3}{L'_2 + L'_3} = L \frac{1+2k}{1+k} \\ L_{SIDO2} &= L_2 + \gamma \frac{L''_1 L''_3}{L''_1 + L''_3} \approx L_2 + \frac{L''_1 L''_3}{L''_1 + L''_3} = L'' \frac{1+2k}{1+k} \end{aligned} \tag{5.27}$$

LLC topology is commonly used for converters with a wide output voltage range. Therefore, LLC converters are generally designed with a frequency controlled variable DC gain, but with the drawback of losing the load-independent behavior provided by the fixed frequency operation. Nevertheless, common LLC converters design tools can help the description of this DC-gain. The main method is the FHA[116], with which the circuit can be described as in **Fig. 5.4**.

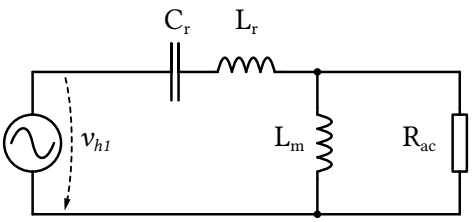


Figure 5.4 Equivalent circuit according to FHA.

The input square-wave voltage is approximated by its first harmonic only (sinusoidal waveform) and the load is represented by a resistor:

$$\omega_{sw} = 2\pi f_{sw} \tag{5.28}$$

$$v_{h1}(t) = \frac{2}{\pi} V_{DC} \sin(\omega_{sw} t) \tag{5.29}$$

$$i_{h1}(t) = \pi I_{DC} \sin(\omega_{sw} t) \tag{5.30}$$

$$R_{DC} = \frac{V_{DC}^2}{P} \tag{5.31}$$

$$R_{AC} = \frac{v_{h1}}{i_{h1}} = \frac{2}{\pi^2} R_{DC} \tag{5.32}$$

where V_{DC} is the DC bus voltage.

The DC gain can be expressed, according to [116], as:

$$\frac{V_{DC,out}}{V_{DC,in}} = \frac{V_{AC,out}}{V_{AC,in}} = M(\lambda, Q, f_n) = \frac{1}{\sqrt{\left(1 + \lambda - \frac{\lambda}{f_n^2}\right)^2 + Q^2 \left(f_n - \frac{1}{f_n}\right)^2}} \tag{5.33}$$

Where the quality factor Q and the inductance ratio λ are given by:

$$\begin{aligned} Q &= \frac{\omega_r L_r}{R_{AC}} \\ \lambda &= \frac{L_r}{L_m} \end{aligned} \tag{5.34}$$

The ZVS is ensured in the region to the right of the resonance peak [109]. This resonant peak moves to the right with increased load represented by $\frac{1}{R_{AC}}$ which influences the Q (see **Fig. 5.5**). The frequency $\hat{f}$ corresponding to this maximum gain is given by:

$$\hat{f}(\lambda, Q) = \sqrt{\frac{Q^2 - \lambda(1+\lambda) + \sqrt{(Q^2 - \lambda(1+\lambda))^2 + 4Q^2\lambda^2}}{2Q^2}} \tag{5.35}$$

However, in the present case, L_m is already set, $R_{AC,min}$ is given by the maximum power required, so the peak-gain-frequency $\hat{f}(L_r)$ can be expressed in function of the resonant inductor L_r. We can

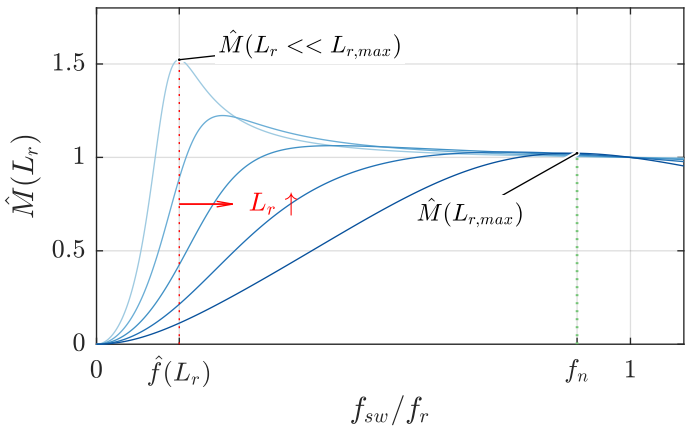


Figure 5.5 DC gain M for the maximal load (Q_{max}) in function on the switching frequency for various L_r from $L_{r,max}/10$ to $L_{r,max}$.

therefore calculate the L_r for which the gain $\hat{M}$ is at the frequency f_n for a maximum Q given by $R_{ac,min}$ corresponding to the maximum power. By solving

$$\hat{f}(L_{r,max}) \longrightarrow f_n \tag{5.36}$$

we obtain $L_{r,max}$ which corresponds to the maximum value for the resonant inductance which ensures an inductive behavior and therefore a ZVS operation for all operating points within the maximum ratings.

$$L_{r,max} = \frac{f_n^2 L_m R_{ac}^2}{(1-f_n^2)(R_{ac}^2 + f_n^2 L_m^2 \omega^2)} \tag{5.37}$$

This $L_{r,max}$ can be evaluated for each port by taking in account the R_{AC} corresponding to the maximum power in each mode (i.e. P_{main} or $P_{storage}$). Thus, for example, for port 1, which corresponding modes are SISOa, SISOc and SIDO1:

$$\begin{aligned}
L_{SISOa} = 2L &\leq \frac{f_n^2 L_m (\frac{2V_{DC,1}^2}{\pi^2 P_{main}})^2}{(1-f_n^2)((\frac{2V_{DC,1}^2}{\pi^2 P_{main}})^2 + f_n^2 L_m^2 \omega^2)} \\
L_{SISOc} = (1+k)L &\leq \frac{f_n^2 L_m (\frac{2V_{DC,1}^2}{\pi^2 P_{storage}})^2}{(1-f_n^2)((\frac{2V_{DC,1}^2}{\pi^2 P_{storage}})^2 + f_n^2 L_m^2 \omega^2)} \\
L_{SIDO1} = L\frac{1+2k}{1+k} &\leq \frac{f_n^2 L_m (\frac{2V_{DC,1}^2}{\pi^2 (P_{main}+P_{storage})})^2}{(1-f_n^2)((\frac{2V_{DC,1}^2}{\pi^2 (P_{main}+P_{storage})})^2 + f_n^2 L_m^2 \omega^2)}
\end{aligned} \tag{5.38}$$

This is applied for port 2 and 3 with inductances L_{SISOb}, L_{SISOd}, L_{SISOe}, L_{SISOf} and L_{SIDO2} which allows to define a maximum L. This L is used to calculate the three resonant inductances L_1, L_2 and L_3 using

(5.20) with $k = 5$.

$$\begin{aligned} L_1 &= L \implies L_1 = 104\,\mu\text{H} \\ L_2 &= \frac{n_2^2}{n_1^2} L \implies L_2 = 9.4\,\mu\text{H} \\ L_3 &= \frac{n_3^2}{n_1^2} kL \implies L_3 = 46.8\,\mu\text{H} \end{aligned} \tag{5.39}$$

And the resonant capacitors are sized in order to match the resonant frequency.

$$\begin{aligned} C_1 &= \frac{1}{\omega_r^2 L_1} \implies C_1 = 8.8\,\mu\text{F} \\ C_2 &= \frac{1}{\omega_r^2 L_2} \implies C_2 = 97.6\,\mu\text{F} \\ C_3 &= \frac{1}{\omega_r^2 L_3} \implies C_3 = 19.5\,\mu\text{F} \end{aligned} \tag{5.40}$$

It has to be noted that the value of L is not much influencing the shape of the resonant current. This permits great freedom in the choice of L and allows for other design criteria to be applied, such as the maximum ratings of physical components used. For instance, with L having the maximum value, the resonant capacitors have the smallest value and are subject to the maximum resonant voltage. If this voltage is too high compared to the ratings of the physical components to be used, L can be slightly reduced until acceptable resonant voltages are obtained on each port. On the other hand, a too small resonant inductance involves a MFT with a very high coupling factor, will be difficult to implement in the case of a system requiring a high isolation degree.

Based on the method presented in the Chapter 4, the ZVS operation plane is evaluated for the parameters obtained and is depicted in **Fig. 5.6**.

5.3.5 DC bus capacitors $C_{DC,2}$

The DC bus capacitors are sized in order to fulfill voltage ripple specification. In the present case, the ripple has been arbitrarily chosen to be below 1% of the DC voltage:

$$\Delta V_{DC_2} = V_{DC_2} \times 1\% = 7.5\,\text{V} \tag{5.41}$$

On the port 2, the main source of ripple is the resonant current which is pulsating with the frequency f_{sw}. Since all the capacitors of the LV side are connected together in parallel, in the ISOP configuration, the actual capacitance on the LV side is $N_s \cdot C_{DC,2}$, so their value can be reduced by the factor N_s. The value of $C_{DC,2}$ can be sized using common voltage ripple expressions [117].

$$C^*_{DC_2} = \frac{I_{LV}}{N_s 2 f_{sw} \Delta V_{DC_2}} \implies C^*_{DC_2} = 360\,\mu\text{F} \tag{5.42}$$

In order to decrease the ripple on the voltage of the LV side (port 2), the gate signal of the resonant stage of the multiple submodules can be shifted with a phase shift of $2\pi/N_s[rad]$ (see **Fig. 5.8**).

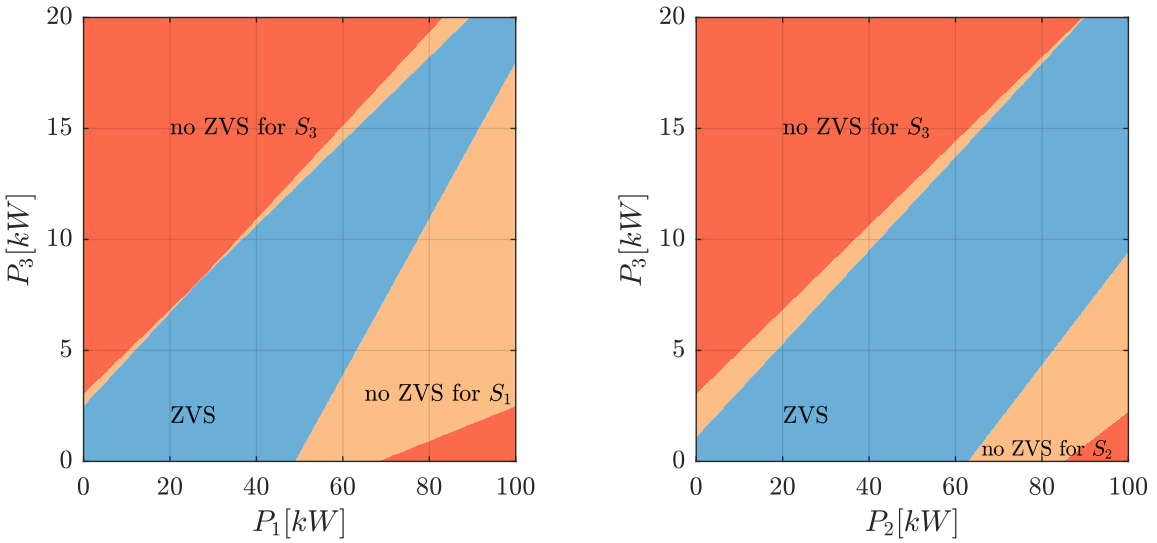


Figure 5.6 ZVS area for the mode DISO1 (a) and DISO2 (b). The ZVS operation is maintained around the ratio $P_3/P_1 = 1/5$ and $P_3/P_2 = 1/5$.

Thanks to the interleaving the apparent frequency is multiplied by N_s and the capacitor $C^*_{DC_2}$ (without interleaving) can be reduced again by a factor N_s to C_{DC_2}(5.43).

$$C_{DC_2} = \frac{I_{DC_2}}{N_s^2 2 f_{sw} \Delta V_{DC_2}} \implies C_{DC_2} = 72\,\mu\text{F} \tag{5.43}$$

5.4 Regulation stage of the MV side

5.4.1 Switching frequency f_{B_1}

The switching frequency f_{B1} is chosen so as not to exceed the maximum dissipable power, evaluated around 900 W for the resonant stage.

In both buck and boost mode, the waveforms in the stage are as illustrated in the **Fig. 5.7**. The losses are the biggest at maximum power $P_{main} + P_{storage}$. The average current at this power is given by:

$$\bar{i}_{b1,max} = \frac{P_{main} + P_{storage}}{v_{MV}} = \frac{600\,\text{kW}}{10\,\text{kV}} = 60\,\text{A} \tag{5.44}$$

which allows to calculate the RMS current, given by:

$$\tilde{i}_{b1} = \frac{\sqrt{(12 + \Delta_{ib1})\bar{i}^2_{b1,max}}}{2\sqrt{3}} \tag{5.45}$$

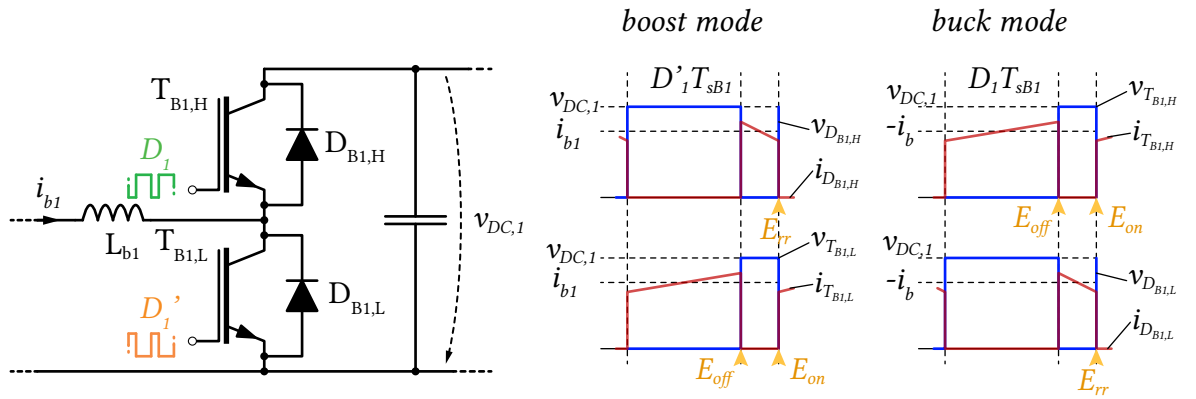


Figure 5.7 Regulation stage and typical current and voltage waveforms in the semiconductors. Turn-on and turn-off losses are present on the active transistor while reverse recovery losses are present on the diode of the opposite switch.

where δ_{ib1} is the relative current ripple, arbitrarily chosen below 10%. Since the current is distributed between the diode and the IGBT according to the duty cycle, the conduction losses of the stage S_{B1} depend on:

$$P_{cond} = D_1 P_{cond,T} + (1 - D_1) P_{cond,D} \tag{5.46}$$

Thus, the conduction losses can be considered as the worst between both. Considering the datasheet parameters, the conduction losses for the rated power are:

$$\begin{aligned} P_{cond,T} &= \bar{i}_{b1,max} V_{f,T} + \tilde{i}_{b1}^2 R_{on,T} = 170\,\mathrm{W} \\ P_{cond,D} &= \bar{i}_{b1,max} V_{f,D} + \tilde{i}_{b1}^2 R_{on,D} = 162\,\mathrm{W} \end{aligned} \tag{5.47}$$

The inspection of the waveforms (cf. **Fig. 5.7**) shows that the stage is subject to turn-on and turn-off loss at the transistor as well as the reverse recovery loss on the diode. The energy given by the datasheet for the switching currents are:

$$\begin{aligned} E_{on}(\bar{i}_{b1}(1 - \Delta_{ib1}/2), v_{DC,1}) &\simeq 222\,\mathrm{mJ} \\ E_{off}(\bar{i}_{b1}(1 + \Delta_{ib1}/2), v_{DC,1}) &\simeq 290\,\mathrm{mJ} \\ E_{rr}(\bar{i}_{b1}(1 - \Delta_{ib1}/2), v_{DC,1}) &\simeq 180\,\mathrm{mJ} \end{aligned} \tag{5.48}$$

The power of the switching losses being given by:

$$P_{sw,b1} = f_{B1} \left(E_{on} + E_{off} + E_{rr} \right) \tag{5.49}$$

the maximum losses for the stage S_{B1} can be estimated by

$$P_{SB1} = P_{sw,b1} + P_{cond} \tag{5.50}$$

This allows the maximum operating frequency of the buck/boost stage 1 to be calculated.

$$f_{B1} \leq f_{B1,max} = \frac{P_{max}^{air} - P_{cond}}{E_{on} + E_{off} + E_{rr}} = 1\,\mathrm{kHz} \tag{5.51}$$

5.4.2 Inductor filter L_{B_1}

The cascaded regulation stage on the MV port can be considered as a single buck or boost converter with a low side voltage given by v_{MV} and a high side voltage equal to $N_s \cdot v_{DC,1}$. Moreover, the inductors L_{B_1} of each submodule are connected in series, so the effective filter inductor the MV side has the value

$$L_{B_1,tot} = N_s L_{B_1} \tag{5.52}$$

$L_{B_1,tot}$ can be sized in order to fulfill a relative current ripple specification of $\delta_{ib1} = 5\%$, following to standard rules [117] with:

$$L_{B_1,tot} = \frac{N_s V_{DC,1}}{4\delta_{ib1} i_{dc,1} f_{B_1}} \tag{5.53}$$

which implies that the L_{B_1} (without interleaving) of each submodule should be:

$$L_{B_1}{}^* = \frac{L_{B_1,tot}}{N_s} = 260\,\text{mH} \tag{5.54}$$

Thank to the interleaving of the N_s submodule and a phase shift of $\frac{2\pi}{N_s}$ between their modulation carrier, the voltage effectively applied to the inductor $L_{B_1,tot}$ is reduced by a factor $\frac{1}{N_s}$. Additionally, the apparent frequency is multiplied by N_s, so in the case of interleaving, the inductors can be reduced by N_s^2

$$L_{B_1} = \frac{L_{B_1}{}^*}{N_s^2} = \frac{L_{B_1,tot}}{N_s^3} = 10.5\,\text{mH} \tag{5.55}$$

5.4.3 DC bus capacitors $C_{DC,1}$

The DC-bus capacitors C_{DC_1} are sized in order to fulfill voltage ripple specifications ΔV_{DC_1} given in (5.56), with a δ_{Vdc1} arbitrarily chosen equal to 1%.

$$\Delta V_{DC_1} = V_{DC_1} \times \delta_{V_{dc1}} = 25\,\text{V} \tag{5.56}$$

On the port 1, since f_{B_1} is normally smaller than f_{sw}, the main source of voltage ripple ΔV_{DC_1} is the pulsed current through the buck/boost stage S_{B1} at the frequency f_{B_1}. Thus, the C_{DC_1} are sized according to (5.57) where D_1 is the duty cycle in steady state and $i_{dc,1}$ is given in (5.2).

$$C_{DC_1} = \frac{i_{dc_1}(1 - D_1)}{f_{B_1} \Delta V_{DC_1}} \implies C_{DC_1} = 160\,\mu\text{F} \tag{5.57}$$

5.5 Regulation stage of the ES side

5.5.1 Switching frequency f_{B_3}

The switching frequency for regulation stage for the energy storage port is dimensioned in the same way as for the MV port in section Section **5.4**, taking into account the rating of port 3 and the

characteristics of the module *Semikron SKM 400GB176D*[115]. For a ripple δ_{ib3} of 10%, the average current and RMS are similar and are given by

$$\tilde{i}_{b3} \simeq \bar{i}_{b3} = \frac{P_{storage}}{v_{ES,min}} = \frac{20\,\text{kW}}{200\,\text{V}} = 100\,\text{A} \tag{5.58}$$

Thus, the conduction losses, at rated power, are given by

$$\begin{aligned} P_{cond,T} &= \bar{i}_{b3,max} V_{f,T} + \tilde{i}_{b3}^2 R_{on,T} = 150\,\text{W} \\ P_{cond,D} &= \bar{i}_{b3,max} V_{f,D} + \tilde{i}_{b3}^2 R_{on,D} = 125\,\text{W} \end{aligned} \tag{5.59}$$

Then, the losses are calculated by using the switching energy curves given by the datasheet resulting in:

$$\begin{aligned} E_{on}(\bar{i}_{b3}(1 - \delta_{ib3}/2), v_{DC,3}) &\simeq 32\,\text{mJ} \\ E_{off}(\bar{i}_{b3}(1 + \delta_{ib3}/2), v_{DC,3}) &\simeq 30\,\text{mJ} \\ E_{rr}(\bar{i}_{b3}(1 - \delta_{ib3}/2), v_{DC,3}) &\simeq 22\,\text{mJ} \end{aligned} \tag{5.60}$$

This allows the maximum operating frequency of the buck/boost stage of port 3 to be calculated and f_{B3} is finally set just below.

$$\begin{aligned} f_{B3,max} &= \frac{P_{max}^{air} - P_{cond}}{E_{on} + E_{off} + E_{rr}} = 8.5\,\text{kHz} \\ f_{B3} &= 8\,\text{kHz} \end{aligned} \tag{5.61}$$

5.5.2 Inductor filter L_{B_3}

For the storage port, L_{B_3} is calculated for a current ripple specifications δ_{ib3} of 5% using the common ripple derivation of a buck converter [117]:

$$\begin{aligned} \Delta_{ib3} &= \delta_{ib3} i_{b3} = 5\,\text{A} \\ L_{B_3} &= \frac{V_{DC,3}}{4 f_{B_3} \Delta_{ib3}} \implies L_{B_3} = 17\,\text{mH} \end{aligned} \tag{5.62}$$

5.5.3 DC bus capacitors $C_{DC,3}$

The DC bus capacitors $C_{DC,3}$ is sized in order to fulfill the voltage ripple specification of 1%:

$$\Delta V_{DC,3} = V_{DC,3} \times 1\% = 7.5\,\text{V} \tag{5.63}$$

On the port 3, f_{B_3} is normally higher than f_{sw}, so the main source of voltage ripple $\Delta V_{DC,3}$ is the resonant current through the resonant stage. C_{DC_3} is sized according to (5.64).

$$C_{DC_3} \geq \frac{i_{dc,3}}{2 f_{sw} \Delta V_{DC,3}} \implies C_{DC_3} = 360\,\mu\text{F} \tag{5.64}$$

The DC-bus capacitors C_{DC_i} are connected in series with the resonant tank and are affecting the resonant frequency. Thus, the actual components C_{r_i} have to be adjusted following (5.65) to match the C_i given in (5.40).

$$C_{r_i} = \frac{C_i 4 C_{DC_i}}{4C_{DC_i} - C_i} \tag{5.65}$$

5.6 Summary of the designed parameters

In order to reach the rating of 10 kV/750 V for a power of 500 kW, a structure with $N_s = 5$ submodules has been adopted. The 5 submodules are identical and the parameters used for the resonant stage are summarized in Table **5.5** and the parameters used for the two regulation stage are summarized in Table **5.6**. Simulation results are presented in **Fig. 5.8** and show voltage and current ripple with and without interleaving (respectively with $C_{DC,2}$, L_{B_1} for interleaved mode and with $C_{DC,2*}$, L_{B_1*} for non-interleaved mode).

Table 5.5 Resonant stage parameters

f_{sw}	f_n	f_r	Port	L_m	L_1	C_1
5 kHz	0.95	5.25 kHz	1	5 mH	104 µH	8.8 µF
			2		9.4 µH	97.6 µF
			3		46.8 µH	19.5 µF

Table 5.6 Regulation stage parameters

f_{B_1}	L_{B_1}	$C_{DC,1}$	f_{B_3}	L_{B_3}	$C_{DC,3}$	$C_{DC,2}$
1 kHz	10.5 mH	160 µF	8 kHz	18 mH	360 µF	72 µF

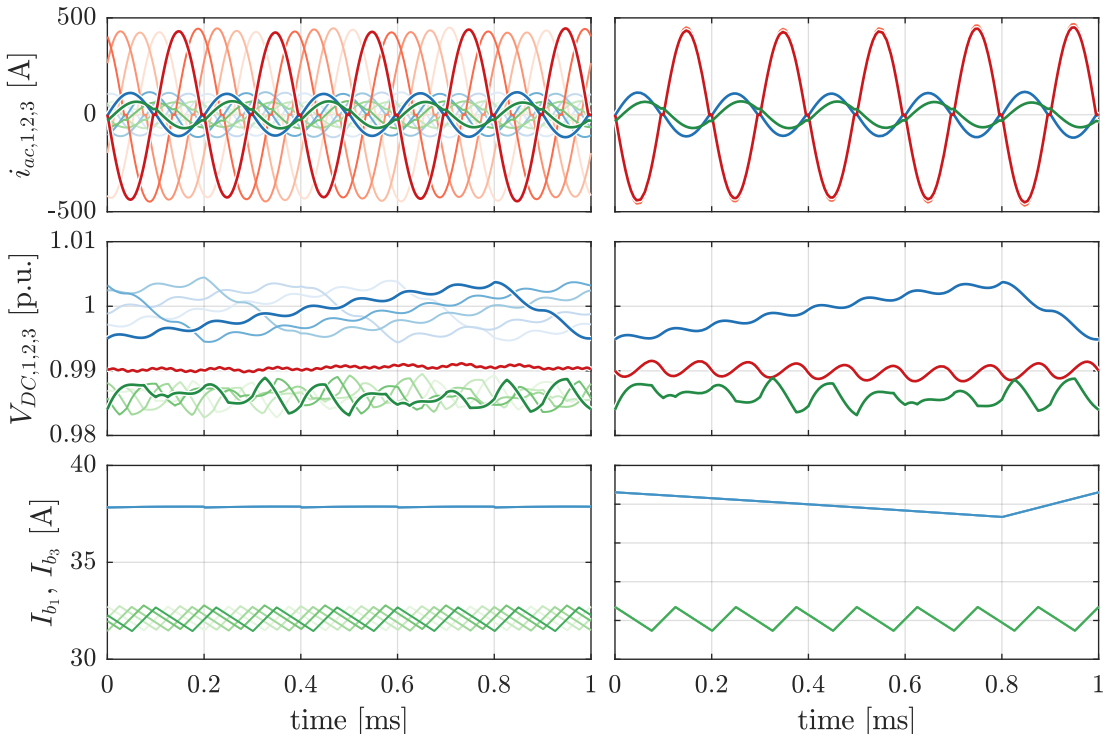


Figure 5.8 Comparison of the waveforms with interleaving (on the left-hand side) and without (on the right-hand side). The resonant currents for the five submodules are depicted on top figures (port 1 in blue, port 2 in red and port 3 in green). The DC-bus voltage, reported to their nominal value, are depicted in the middle (with the same color code). On the bottom figures, the DC current from the MV grid (in blue) and the 5 storage elements (in green).

5.7 Discussion

This chapter presents a design methodology for the complete MEG converter. The number of submodule, the class of semiconductor and the switching frequencies are essentially sized to meet criteria based on losses and power that can be dissipated. Then, the resonant tanks are sized using criteria based on the conditions for soft switching to minimize switching losses. The criteria are based on the traditional techniques used for conventional LLC, namely the FHA. Thus, the ZVS is ensured for SISO and SIDO modes. The soft switching operating area in DISO mode is evaluated by taking into account the physical parameters of the selected semiconductors and shows that the converter also benefits from ZVS around the axis $p_1 = 5p_3$. Finally, the DC components are dimensioned to meet ripple specifications. Simulation results show the current and voltage waveforms with the parameters obtained and highlight the benefit of the interleaving of the submodules.

6

Control system design

This chapter presents the development of a control structure for the MEG converter. The converter and its dynamic behavior are modeled first at the level of the submodule, and second at the level of the entire converter. The control structure is proposed subsequently and the controller gains are calculated. The proposed control structure is verified by using the low voltage prototype for experimental results at the level of the submodule and by simulation at the level of the entire converter.

6.1 Plant modeling

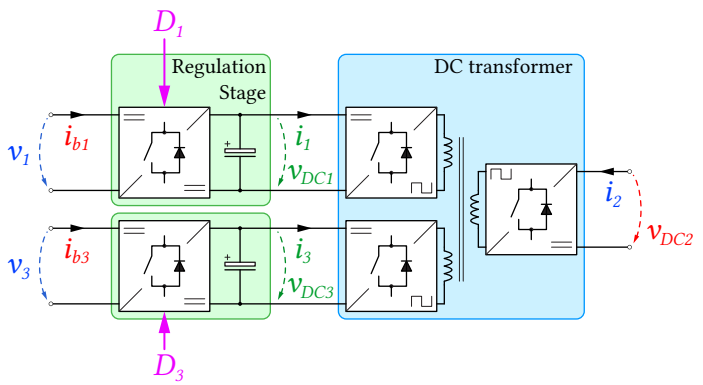


Figure 6.1 Power inputs (in blue), power outputs (in red) and control inputs (in pink) of a submodule.

First, the dynamic model of a submodule as illustrated in **Fig. 6.1** is developed. As already mentioned before, the only two control inputs are the duty-cycles D_1 and D_3 of the two regulation stages. The two regulation stages allow the current to be controlled according to the input voltage using the duty-cycle. In the meantime, the DC transformer only adapts the voltage to generate an output voltage $v_{DC,2}$ from the two input voltages $v_{DC,1}$ and $v_{DC,3}$. The DC buses appear as a connection element between the regulation stages and the DC-transformers, $v_{DC,1}$ and $v_{DC,3}$ being outputs for the regulation stages and inputs for the DC transformer and inversely for the currents i_1 and i_3. Thus, the dynamics model of the regulation stages is done using the duty-cycle-to-dc-bus-voltage transfer function and the DC transformer model is done using the dc-bus-voltage-to-output-voltage transfer function.

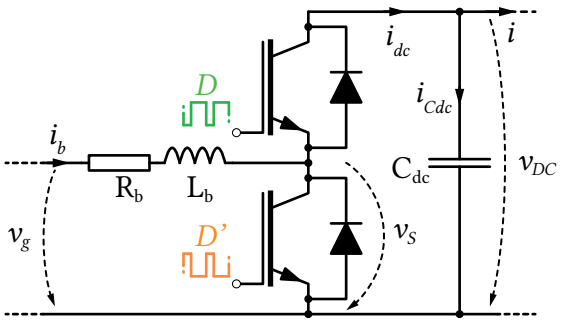


Figure 6.2 Circuit of the regulation stage (boost/buck converter) of one submodule.

6.1.1 Regulation stage

The regulation stages S_{B1} and S_{B3}, which structure is depicted in **fig. 6.2**, act either as a buck converter or as a boost converter depending on the direction of the power flow. In buck mode the action variable is the duty-cycle D_1 (respectively D_3) associated with the upper switch, the bottom switch being passive (diode). Reciprocally, in boost mode, the upper switch is passive and the action variable is the duty cycle D_1' (respectively D_3') given by (1-D_1) associated with the lower switch. The moving average of the switching-cell output voltage v_S is given by:

$$\langle v_S \rangle = D \cdot v_{DC} \tag{6.1}$$

In boost mode, for small inductor currents (below $i_{b,crit}$, given in (6.2)) the converter enters in discontinuous conduction mode (DCM), and (6.1) is not valid anymore which results in a non-linearity difficult to model and control.

$$i_{b,crit} = \frac{v_g D D'}{2 L_b f_B} \tag{6.2}$$

In order to avoid DCM and keep (6.2) valid for any loads, both switches (upper with D_1' and lower D_1) are actively switched when the average current through the inductor is between 0 and $i_{b,crit}$.

Thus, generally speaking, for ports 1 and 3, the average voltage applied at the inductor terminals can be given as a function of the input voltage v_g, the voltage drop on R_b, the DC bus voltage v_{DC} and the duty cycle D.

$$\langle v_{L_b} \rangle = v_g - \langle v_{R_b} \rangle - \langle v_S \rangle = v_g - R_b \langle i_b \rangle - D \cdot v_{DC} \tag{6.3}$$

With the current through the inductor $i_b(t)$ given, in the time domain, by:

$$i_b(t) = \int_0^t \frac{1}{L_b} v_{L_b} dt \tag{6.4}$$

In Laplace domain, this results in following expression for $\langle i_b \rangle$:

$$\langle i_b \rangle(s) = \frac{1/L_b}{s + R_b/L_b} (v_g(s) - D \cdot v_{DC}(s)) \tag{6.5}$$

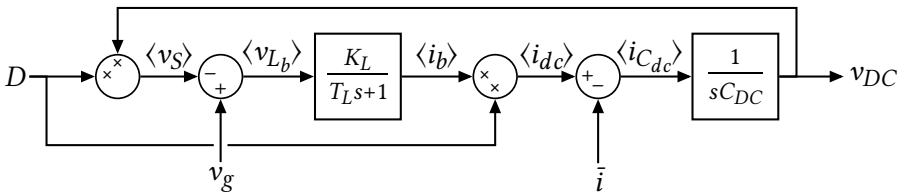


Figure 6.3 Block diagram of the average model of the regulation stage.

or

$$\langle i_b \rangle(s) = \frac{K_L}{T_L s + 1} \langle v_{L_b} \rangle(s) \quad \text{with} \quad K_L = \frac{1}{R_b} \quad \text{and} \quad T_L = \frac{L_b}{R_b} \tag{6.6}$$

following standard gain and time-constant notation.

Finally, the current through the DC bus capacitor $\langle i_{C_{dc}} \rangle$ is given by the difference between the current of the buck/boost stage and the current to/from the resonant stage $\bar{i}$ and the voltage v_{DC} across the capacitor is resulting from the accumulation of the charges from $i_{C_{dc}}$ in C_{dc}.

$$\begin{aligned} \langle i_{C_{dc}} \rangle &= \langle i_{dc} \rangle - \bar{i} = \langle i_b \rangle D - \bar{i} \\ v_{DC}(t) &= \frac{1}{C_{dc}} \int_0^t i_{C_{dc}} dt \end{aligned} \tag{6.7}$$

giving in Laplace domain:

$$v_{DC}(s) = \frac{1}{sC_{dc}} \langle i_{C_{dc}} \rangle \tag{6.8}$$

Thus, the dynamics of the regulation stage can be represented by the block diagram of the **Fig. 6.3**, where the voltage at the terminals of C_{dc} can be regulated with the current i_b, controlled via the duty-cycle D.

In the case of the storage port, the input voltage v_g is given by the voltage at the terminals of the batteries or super-capacitors storage elements, which implies that it may vary considerably with the state-of-charge.

In the case of the MV port, the 5 cascaded converters are controlled using the same duty-cycle D_1. As the current i_{MV} is common to the 5 inductors, they can be considered as a single regulation stage with the following parameters:

$$\begin{aligned} L_b &= \sum^{N_s} L_{b1} \\ v_g &= v_{MV} \\ v_{DC} &= \sum^{N_s} v_{DC,1} \end{aligned} \tag{6.9}$$

6.1.2 DC transformer in SISO mode

In SISO mode, only two ports are present. The topology considered is such as illustrated in **Fig. 6.4a**. In order to better describe the dynamic behavior of the DC-transformer stage, a DC average model

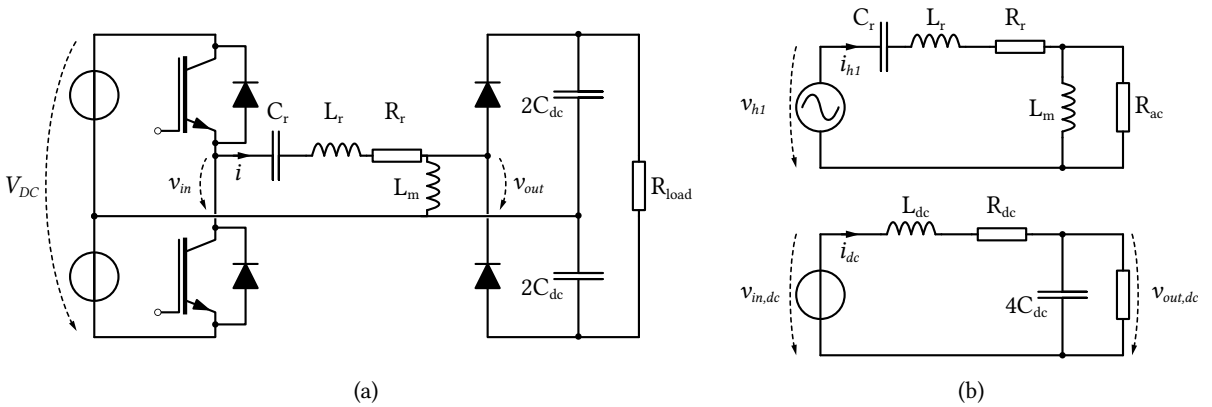


Figure 6.4 Simplified LLC circuit in SISO mode (a), FHA and DC equivalent circuits (b). The models reflect the effect of the input voltage on the current and on the output voltage, and thus the DC-bus capacitors of the input port are not taken in account here.

can greatly simplify the approach. A method proposed in [118] and well illustrated in [83] consists in averaging the currents and voltages over the half period to obtain a DC model that reproduces the piecewise current . Following this approach, the equivalent circuit is such as shown in **Fig. 6.4b**. The elements R_{dc} and L_{dc}, DC equivalent of the resonant circuit consisting of L_m, L_r, C_r and R_r, must describe the same terminal behavior as the real system and must therefore capture the two phenomena of energy loss associated with R_r and storage in the resonant tank that are generally associated with a given power. In the real circuit, resistive losses are associated with the RMS current $\tilde{i}$ and the energy stored in the resonant circuit is linked to the peak current $\hat{i}$.

$$\begin{aligned} \langle P_{loss} \rangle &= R_{in} \tilde{i}^2 \\ E_{stored} &= \frac{1}{2} L_r \hat{i}^2 = \frac{1}{2} C_r \hat{v_{Cr}}^2 \end{aligned} \tag{6.10}$$

In the case of the DC circuit, these values are associated with the DC current i_{dc} flowing through the circuit:

$$\begin{aligned} P_{loss,dc} &= i_{dc}^2 R_{dc} \\ E_{stored,dc} &= i_{dc}^2 L_{dc} \end{aligned} \tag{6.11}$$

However, the equivalence of the two circuits requires that the DC current has to be equal to the local average current (piecewise).

$$i_{dc} = \bar{i} \tag{6.12}$$

This allows to calculate the elements R_{dc} and L_{dc} which can be obtained in (6.13) by equalizing (6.10) and (6.11). It defines as well the coefficients α and β.

$$\begin{aligned} R_{dc} &= \beta^2 R_r = \frac{\tilde{i}^2}{\bar{i}^2} R_r \\ L_{dc} &= \alpha^2 L_r = \frac{\hat{i}^2}{\bar{i}^2} L_r \end{aligned} \tag{6.13}$$

For the calculation of $\bar{i}$, $\hat{i}$ and $\tilde{i}$ from the resonant circuit, the waveforms of the FHA equivalent (see **Fig. 6.4b**) of the system can be considered. The voltage is given by:

$$v_{h1} = \hat{v} \sin(\omega t) = \frac{2}{\pi} V_{DC} \sin(\omega t) \tag{6.14}$$

and the current by:

$$i_{h1} = \hat{i} \sin(\omega t + \varphi) \tag{6.15}$$

with a peak value and an angle given by:

$$\hat{i} = \left| \frac{\hat{v}}{Z} \right| \quad \text{and} \quad \varphi = \arg\left(\frac{\hat{v}}{Z} \right) \tag{6.16}$$

This allows to calculate the piecewise average current:

$$\bar{i} = \frac{2}{T} \int_0^{\frac{T}{2}} i_{h1}(t) dt = \frac{2}{\pi} \hat{i} \cos(\varphi) \tag{6.17}$$

and the RMS current:

$$\tilde{i} = \sqrt{\frac{2}{T} \int_0^{\frac{T}{2}} i_{h1}^2(t) dt} = \frac{\hat{i}}{\sqrt{2}} \tag{6.18}$$

In the case of the LLC circuit, the impedance Z is given by the sum of the load impedance and the resonant circuit:

$$Z = Z_r + Z_{load} \tag{6.19}$$

The resonant impedance depends on the resonant frequency and the switching frequency. These two being fixed and well defined, Z_r can be calculated with it:

$$Z_r = R_r + j\omega L_r + \frac{1}{j\omega C_r} = R_r + j\omega_r L_r \left(f_n - \frac{1}{f_n} \right) \tag{6.20}$$

On the other hand, Z_{load} is depending on the load power represented by R_{load} and modeled with R_{ac} in the FHA equivalent circuit.

$$Z_{load} = \frac{R_{ac} j\omega_{sw} L_m}{R_{ac} + j\omega_{sw} L_m} \tag{6.21}$$

Z_{load} is depicted as a function of the operating point in **Fig. 6.5a**.

The coefficients α and β are load dependent, so it is proposed to evaluate them as a function of the transferred power (cf. **Fig. 6.5b**) and approximate them with a fixed value over a given operating range. Thus, $\bar{\alpha}$ and $\bar{\beta}$ are calculated for a R_{load} corresponding to half the nominal power of the SISO mode. The **Fig. 6.6** shows the comparison of the DC system and the actual system for an input voltage step followed by an output power step.

The consideration of the DC system allows to calculate a transfer function that links the input voltage to the output voltage, as shown in the block diagram of **Fig. 6.7**.

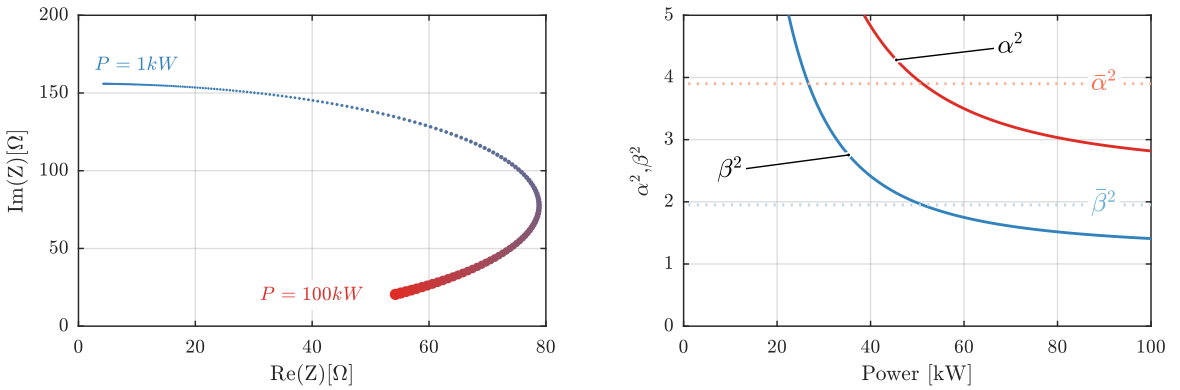


Figure 6.5 Input impedance in function on the load (a) and α^2 and β^2 in function of the load (b). $\bar{\alpha}^2$, $\bar{\beta}^2$ are chosen for $P = 50\,\mathrm{kW}$.

$Y_M(s)$ represents the transfer function that links a variation in input voltage Δv to the average current $\bar{i}$ between the two DC-buses and is given as a function of the parameters L_{dc} and R_{dc} with:

$$\frac{\bar{i}}{\Delta v} = \frac{1/L_{dc}}{s + R_{dc}/L_{dc}} = Y_M(s) \tag{6.22}$$

The output current loads the capacitor of the output DC-bus whose voltage v_{out} is then applied to the load which dynamic is represented by $Y_L(s)$.

The transfer function of $Y_M(s)$ also represents the dynamic of the power flow reversal. If the power between the port 1 and 2 changes its sign, the variation of power will be limited by these R_{dc} and L_{dc}. In terms of modulation, this power reversal sequence will imply that semiconductors of both ports are actively operated. The magnetizing current of the MFT will be shared between both port which imply a possible loss of ZVS, but does not interfere with the dynamics.

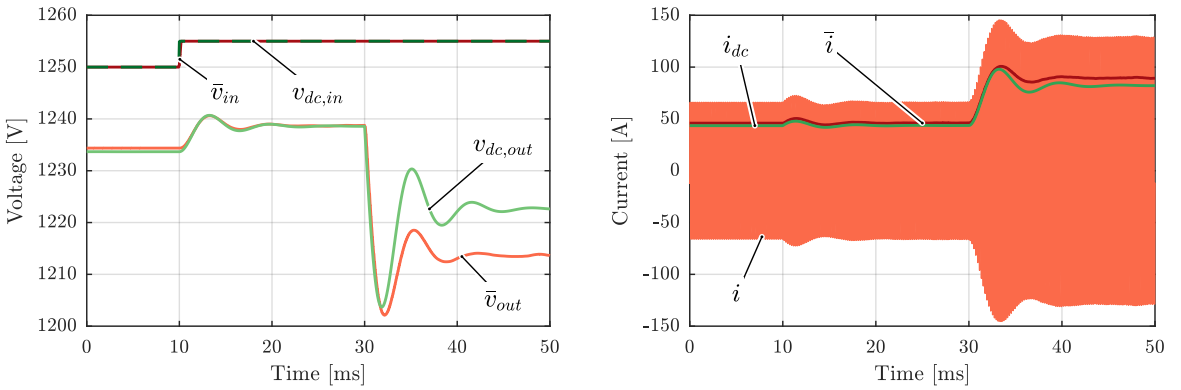
6.1.3 DC transformer in DISO mode

For the DISO model, the approach is based on the separation of the common and differential components introduced in Chapter 4. The dynamic of the common mode circuit is similar to the one of the SISO mode and a DC circuit can be identified with the parameters $R_{dc,com}$ in $L_{dc,com}$ given by:

$$\begin{aligned} R_{dc,com} &= \beta_{com}^2 R_{com} \\ L_{dc,com} &= \alpha_{com}^2 L_{com} \end{aligned} \tag{6.23}$$

with R_{com} and L_{com} as defined in (4.45). The transfer function that links the current i_{com} to the input voltage is given by:

$$\frac{\bar{i}_{com}}{\Delta v_{com}} = \frac{1/L_{dc,com}}{s + R_{dc,com}/L_{dc,com}} = Y_{com}(s). \tag{6.24}$$



(a) (b)

Figure 6.6 Voltage in the actual circuit and the DC equivalent (a) and the current in both (b). Before t = **30 ms**, the load is corresponding P = **50 kW**, so $\bar{\alpha}^2$, $\bar{\beta}^2$ match exactly α^2, β^2 and the DC model response fits well the switched model response. After t = **30 ms**, the load corresponds to P = **100 kW**. $\bar{\alpha}^2$, $\bar{\beta}^2$ are not matching perfectly α^2, β^2 and a DC-gain error is thus visible. Nevertheless, the dynamic of the system, stays accurate in terms of timing.

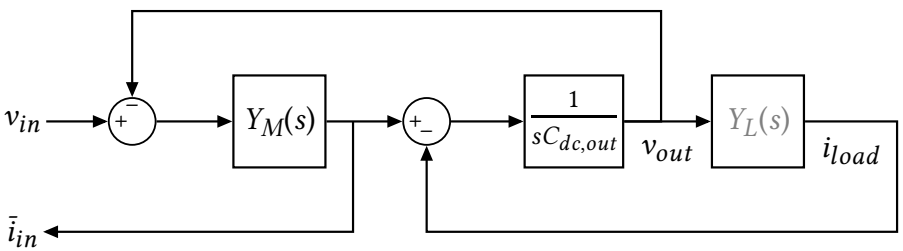


Figure 6.7 Block diagram of the resonant stage in SISO mode.

The differential circuit can also be modeled by a DC equivalent. And in this case, the resonant impedance is fixed and is given as a function of R_{dif} and L_{dif} as defined by (4.55).

$$Z_{r,dif} = R_{dif} + j\omega_r L_{dif}\left(f_n - \frac{1}{f_n}\right) \tag{6.25}$$

so the α_{dif} and β_{dif} are fixed and do not depend on the load.

$$\frac{\bar{i}_{dif}}{v_{dif}} = \frac{1/L_{dc,dif}}{s + R_{dc,dif}/L_{dc,dif}} = Y_{dif}(s) \tag{6.26}$$

Therefore, the behavior of the DC transformer in DISO mode can be represented by the block diagram in **Fig. 6.8** including the transfer functions $Y_{com}(s)$ and $Y_{dif}(s)$. The two controllable inputs are the voltage $v_{DC,in,1}$ and $v_{DC,in,2}$ and the corresponding reactions are respectively $\bar{i}_{in,1}$ and $\bar{i}_{in,2}$. The system output is $v_{DC,out}$ which is then applied to the load whose behavior is modeled by $Y_L(s)$

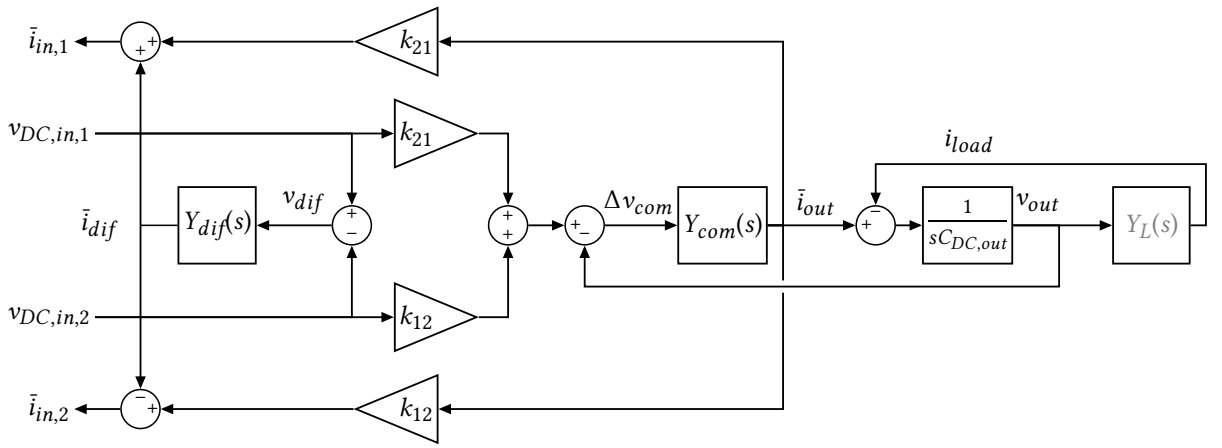


Figure 6.8 Block diagram of the resonant stage in DISO mode, with all the variables referred to one side of the MFT.

6.1.4 DC transformer in SIDO mode

For DISO mode, the same method is applied with the definition of the transfer functions $Y_{com}(s)$ and $Y_{dif}(s)$ using common and differential mode parameters given by (4.73) and (4.79). The main difference is the sharing of the common mode current according to k_{12} and k_{21} that occurs physically on the secondary side of the MFT and therefore after the transfer function $Y_{com}(s)$ in the block diagram presented in **Fig. 6.9**. In the mode SIDO1, for instance, in which the port 1 is feeding ports 2 and 3, the function $Y_{L,1}$ would represent the grid impedance on the LV side, and $Y_{L,2}$ would represent the impedance of the regulation stage on the storage side and would be depending on charging/discharging current and the SOC of the storage element.

6.1.5 DC Approximation

After combining the block diagrams of the control stage and the DC transformer, the relation between the input current of the DC transformer, i_{in}, and the output voltage in SISO mode can be represented using the block diagram of the **Fig. 6.10**. Its inspection reveals that at low frequency (below the pole defined by $\frac{R_{dc}}{L_{dc}}$), the transfer function $Y_M(s \longrightarrow 0)$ acts as a large gain $\frac{1}{R_{dc}}$. In other words, the impedance placed between the DC input and output buses becomes very low for low frequency or DC and the input-voltage-to-output-voltage transfer function can be approximated by a unit DC gain (taking into account the turn ratio of the MFT). This also applies in SIDO and DISO mode, with Y_{com} and Y_{dif} having the same behavior.

From this, a simplified model of the resonant stage can be developed by considering that all DC bus capacitors are connected in parallel or through a very low impedance. The capacitors of the three ports (two ports in SISO mode) of the submodule can be replaced by a single capacitor which value

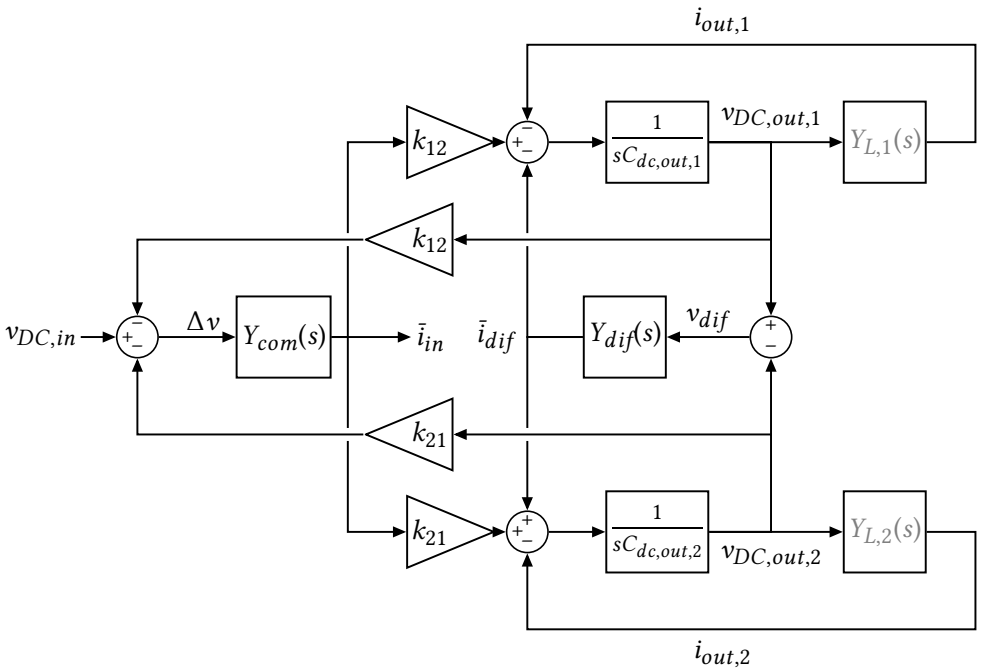


Figure 6.9 Block diagram of the resonant stage in SIDO mode, with all the variable referred to one side of the MFT.

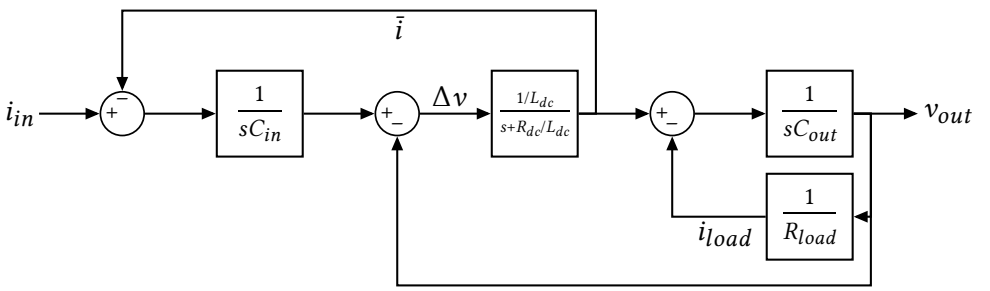


Figure 6.10 Input current to output voltage transfer function for a sub module in SISO mode.

(seen from port 1) is given by:

$$\begin{aligned} C_{SM} &\simeq C_{DC_1} + C'_{DC_2} + C'_{DC_3} = C_{DC_1} + \frac{n_2^2}{n_1^2} C_{DC_2} + \frac{n_3^2}{n_1^2} C_{DC_3} \\ C_{SISO} &\simeq C_{DC_1} + C'_{DC_2} = C_{DC_1} + \frac{n_2^2}{n_1^2} C_{DC_2} \end{aligned} \tag{6.27}$$

Thus, the transfer function of the **Fig. 6.10** is simplified to the one of the **Fig. 6.11**. The **Fig. 6.12** shows the frequency response of the last two circuits and highlights the validity domain of the approximation of the two DC buses by C_{SISO}.

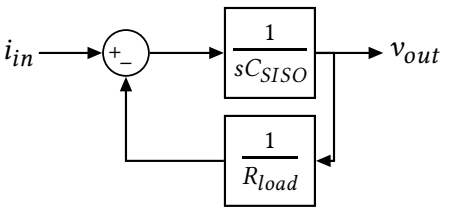


Figure 6.11 Simplified block diagram of the input current to output voltage transfer function for a sub module in SISO mode, considering a single capacitor C_{SISO}.

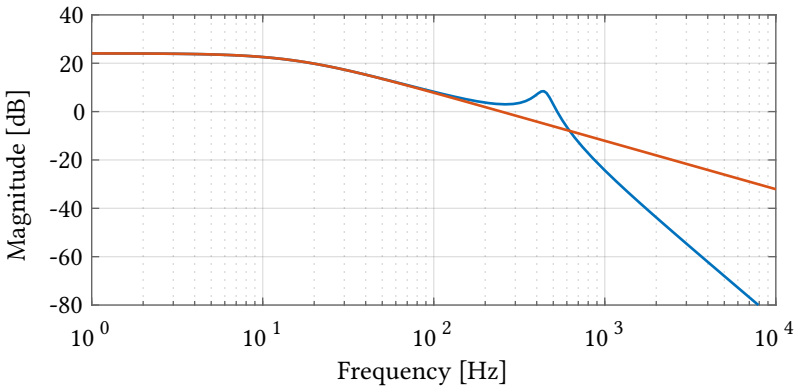


Figure 6.12 Bode plot of the input current to output voltage transfer function. The model considering the resonant tank is in blue and the simplified model with a unique DC-bus capacitor C_{SM} is in red. It can be seen that below **100 Hz**, both are identical which validates the approximation.

6.1.6 Complete converter model

From the previous approach, the structure of the entire converter can be simplified as shown in the diagram of **Fig. 6.13**. Since all the N_s submodules, and their respective C_{SM}, are connected in parallel on the LV side, the plant can be seen as a single equivalent capacitor:

$$C_{MEG} = n_{siso}C_{SISO} + (N_s - n_{siso})C_{SM} \tag{6.28}$$

where n_{siso} is the number of submodules in SISO mode, which depends entirely on the operation strategy and the control layer. Thus, the state variable to be controlled is the voltage at the terminal of the capacity C_{MEG} (common to all DC buses, taking the turn ratio into account) and the control input are N_s+1 duty-cycle D_1 and $D_{3,1-N_s}$ via the currents injected or extracted from the MV port and the different ES ports. The current from/to the low voltage grid appears here as a perturbation.

In terms of dynamics, the difference between DISO and SIDO modes is only the direction of the currents i_{b1} and i_{b3}. This redefinition of the system to be controlled allows a much more efficient strategy for the external control loop. In other words, it is possible to use one of the degrees of freedom to control the output voltage and while keeping the N_s remaining inputs for the control of the power or the state-of-charge (SOC) of the storage elements.

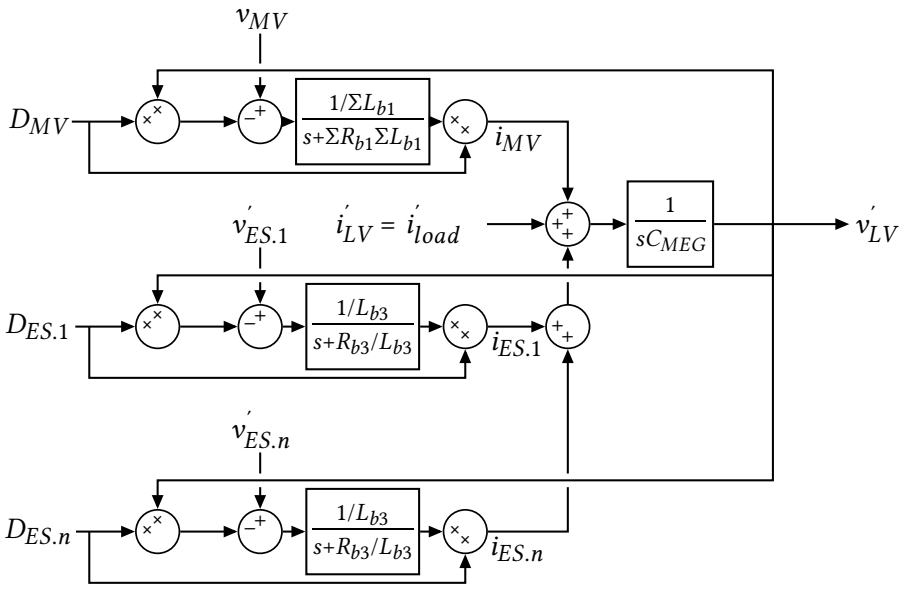


Figure 6.13 Simplified plant model for the complete converter.

6.2 Control Structure

The proposed control structure is as presented in the **Fig. 6.14**. A regulator $K_{v_{LV}}$ with lower bandwidth (external loop) regulates the voltage v_{LV} (i.e. the voltage at the capacity terminal C_{MEG}). The gain of $K_{v_{LV}}$varies in function of the mode of operation (SISO or other) in order to have the appropriate dynamic corresponding to the good time constant due to the variable C_{MEG}. The output of $K_{v_{LV}}$ is a total current setpoint $i^*_{C_{MEG}}$. This current setpoint is then distributed between the N_s storage ports and the MV port according to an upper layer strategy implemented in the Energy Management System (EMS). This block is responsible of the control of the sharing of the current between the grid and the storage elements following strategies and setpoints specific to the application. The N_s+1 port are independent by approximation which allows great freedom for the current sharing strategy. It is possible, for example, to allocate the current of the MV port to the voltage regulation and to manage the SOC of the storage elements independently.

Then, the N_s+1 currents of the MV and the ES ports (through the inductance L_{b1} and L_{b3}) are regulated using regulators $K_{i_{MV}}$ and $K_{i_{ES.1-n}}$ and through a higher bandwidth inner control loop acting on the duty cycles of S_{B1} and $S_{B3.1-n}$.

Thus, only the DC currents of the control stages need to be measured as well as the voltages at the grids terminals and storage element.

6.2.1 Controllers gain design

Since the control strategy refers to DC quantities, the controllers are all of PI type of the form:

$$K(s) = \frac{k_p s + k_i}{s} \tag{6.29}$$

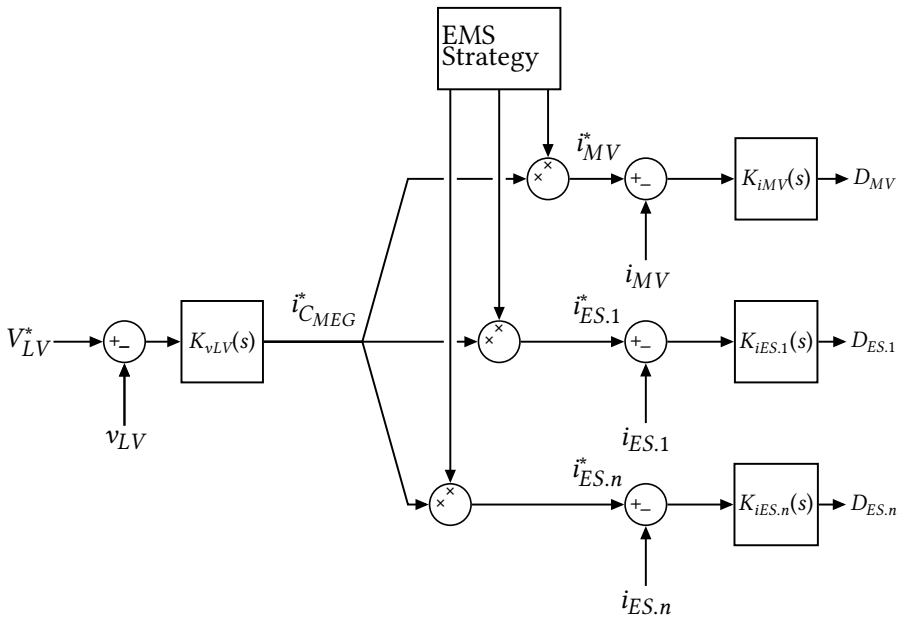


Figure 6.14 Proposed MEG control structure.

For the tuning of the inner loop, the system can be linearized around a DC operating point: $v_{DC,1}$ and $v_{DC,3}$ are considered constant. Thus, the transfer function of the control stages is an inductive filter (low pass) defined by L_b and R_b, the resistance representing the losses of the stage. The proportional gain k_p and integral gain k_i are calculated according to the method of [119], from the theoretical bandwidth α_i. For the MV port, it gives:

$$\begin{aligned} k_{p,i1} &= \alpha_i N_s L_{b1} \frac{1}{V_{DC_1}} \\ k_{i,i1} &= \alpha_i N_s R_{b1} \frac{1}{V_{DC_1}} \end{aligned} \tag{6.30}$$

and for ES ports:

$$\begin{aligned} k_{p,i3} &= \alpha_i L_{b3} \frac{1}{V_{DC_3}} \\ k_{i,i3} &= \alpha_i R_{b3} \frac{1}{V_{DC_3}} \end{aligned} \tag{6.31}$$

In practice, the values of R_{b1} and R_{b3} are difficult to measure and therefore require an empirical approximation and manual tuning of the full gain.

According to the "one-to-tenth" rule, α_i should not exceed one tenth of the switching frequency of the regulation stage (f_{B1} and f_{B3}). In addition, α_i must not be larger than the band allowed by the approximation of C_{SM} shown in the **Fig. 6.12**. So, for the simulation, α_i is given by:

$$\alpha_i \leq 2\pi 100\,\text{Hz} \tag{6.32}$$

For the outer voltage control loop, the plant is a function of the total capacitor C_{MEG} and the nominal

load $R_{load,nom}$:

$$\begin{aligned} k_{p,v} &= \alpha_v C_{MEG} \\ k_{i,v} &= \frac{\alpha_v}{R_{load,nom}} \end{aligned} \tag{6.33}$$

with α_v which, according to the one-to-tenth rule, should not exceed $\frac{1}{10}\alpha_i$. A different $k_{p,v}$ is obtained depending on the number of submodule in SISO mode and corresponding C_{MEG}. The controller's state machine selects the good one on-line. Following values the simulations:

$$\begin{aligned} k_{p,i1} &= 0.016 & k_{i,i1} &= 0.012 \\ k_{p,i3} &= 0.015 & k_{i,i3} &= 0.008 \\ k_{p,v} &= 0.062 & k_{i,v} &= 1 \end{aligned} \tag{6.34}$$

The stability of the system using this set of coefficients and considering a resistive load, is verified in DISO mode using Nyquist criteria in **Fig. 6.15**.

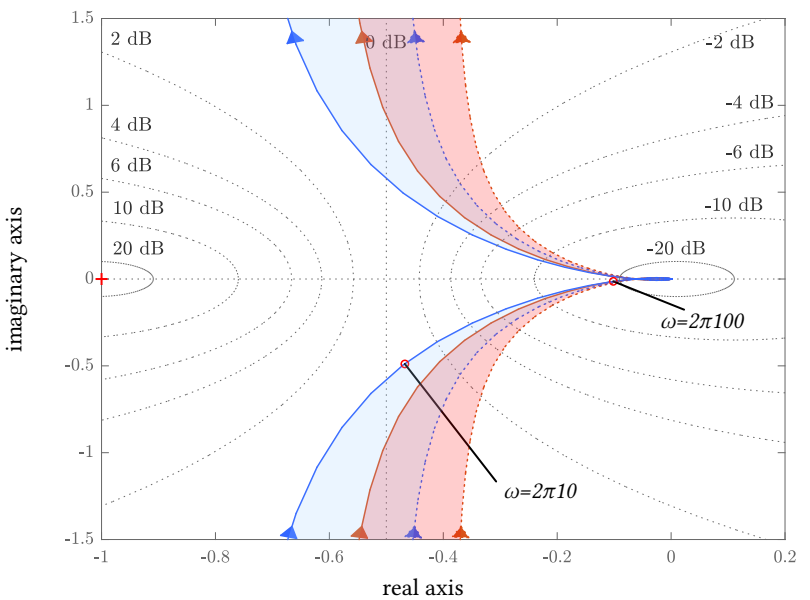


Figure 6.15 Nyquist plot of the system $K_{vLV}(s)H_{MEG}(s)$ with $H_{MEG}(s)$ representing a single capacitor as in **Fig. 6.13** in blue and with $H_{MEG}(s)$ using the structure of **Fig. 6.8** in red. In both cases, the system has been linearized around the operating points where no power is delivered by the ES ports (dashed line) and where the maximum power is delivered by the ES ports (plain line). It may be noticed for low frequencies (bandwidth defined by α_v), Nyquist criterion can be used on the approximated model (in blue) ensuring a certain margin compared to the complete model (in red). For higher frequencies, those margins cannot be ensured since the two plots are crossing.

6.3 Simulation results

In order to verify the complete control structure, the converter using the ratings presented in Chapter 5 is simulated on PLECS. Since the time scale is relatively short, the voltages $v_{ES.1-5}$, usually depending on the SOC of the storage elements, are considered constant. The regulation of the voltage v_{LV} with respect to a load step on the LV port is demonstrated in the **Fig. 6.16**, while the independent use of the ports dedicated to the storage elements is shown in **Fig. 6.17** with zoom-in views in **Fig. 6.18**. The parameters used for the simulations are given in Table **6.1** andTable **6.2**.

Table 6.1 Case study converter ratings

Port i	Nominal power	v_i	$i_{dc,i}$	$v_{DC,i}$
MV	500 kW	10 kV	50 A	2.5 kV
LV	500 kW	750 V	750 A	750 V
ES	100 kW	450 V	500 A	750 V

Table 6.2 Submodule parameters

f_{sw}	f_n	f_r	Port	L_m	L_i	C_i	f_{B_i}	L_{B_i}	$C_{DC,i}$
5 kHz	0.95	5.25 kHz	1	5 mH	104 µH	8.8 µF	1 kHz	10.5 mH	160 µF
			2		9.4 µH	97.6 µF			72 µF
			3		46.8 µH	19.5 µF	8 kHz	18 mH	360 µF

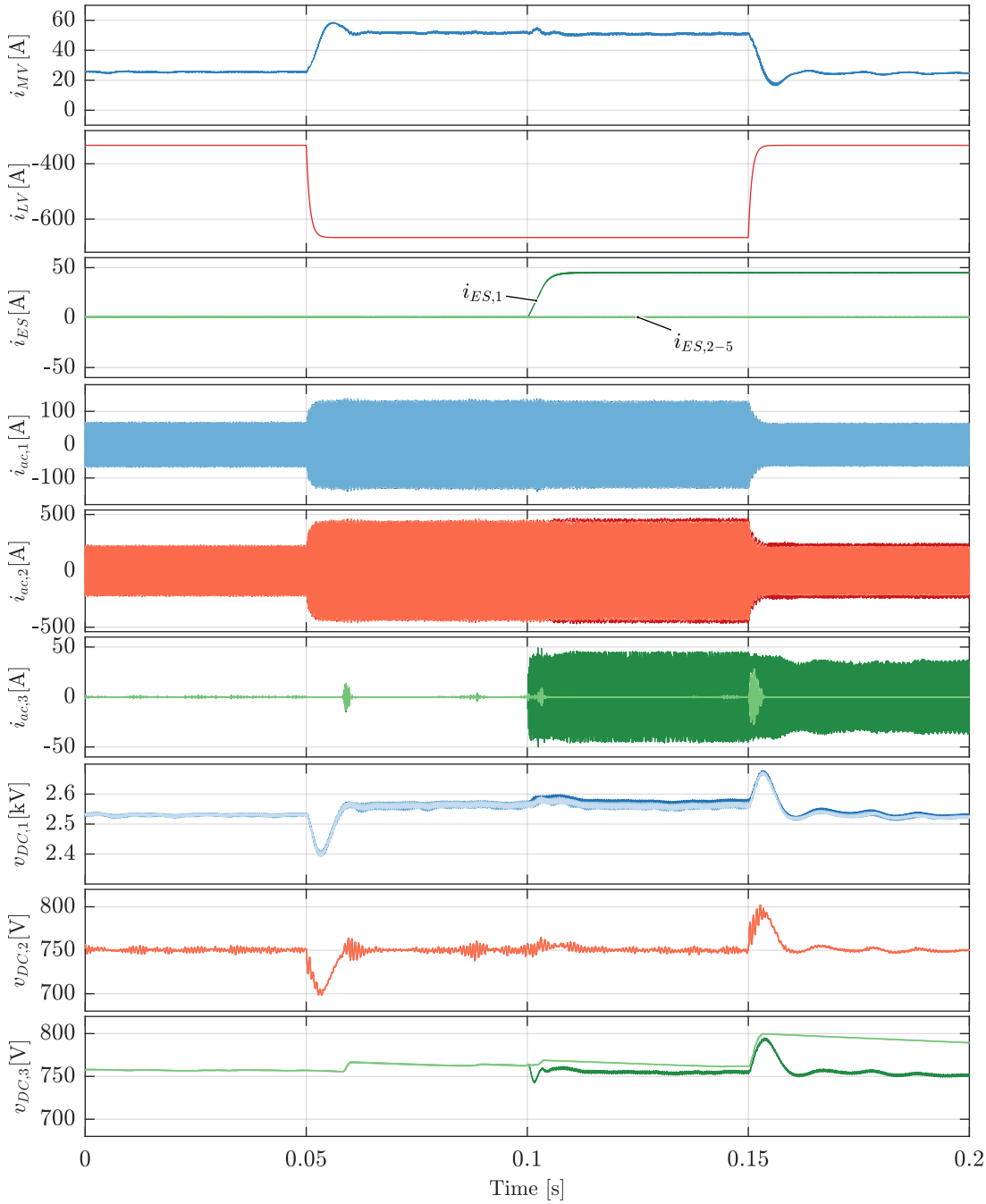


Figure 6.16 From t = 0 to t= 0.05s, the LV port draws a power equal to half of its nominal power (250 kW, corresponding to 333 A). At t = 0.05s, this power is increased to the nominal power of 500 kW, which causes the voltage $v_{DC,2} = v_{VL}$ to drop from 6%. Then the controller increases the current i_{MV} to compensate for this power and brings $v_{DC,2}$ back to 750 V. At = 0.1, storage element 1 starts injecting power (20 kW) and a slight drop in current i_{MV} is observed. finally at t = 0.15, the current i_{MV} suddenly returns to 333 A and an over-voltage is observable on $v_{DC,2}$.

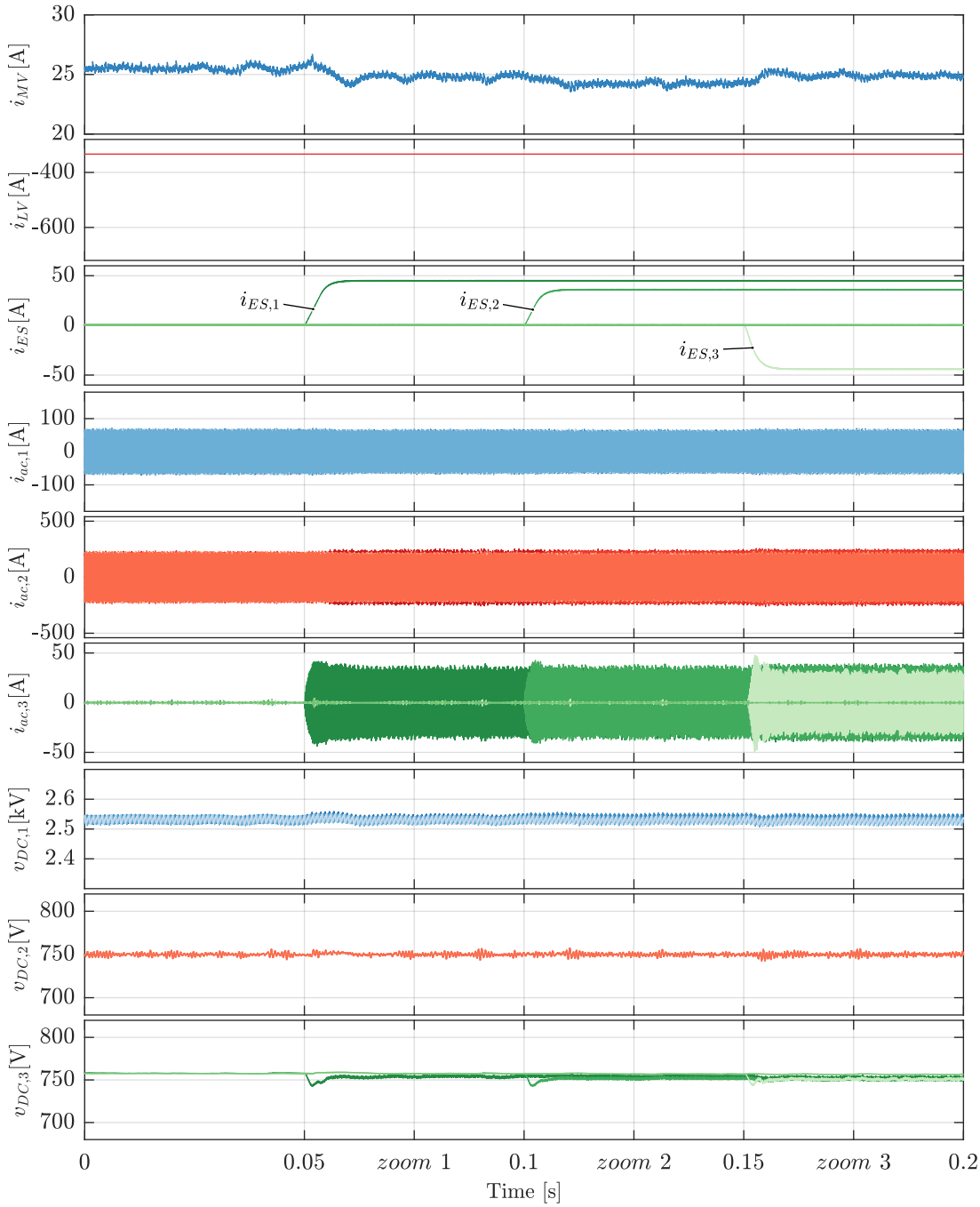


Figure 6.17 At t = 0.05s, the power from the ES.1 port is increased to **20 kW**, which causes a slight disturbance on the current i_{MV}. At t = 0.1s, the power of the port ES.2 is increased to **16 kW**, which implies a slight decrease in current i_{MV}. At t = 0.015s, the ES.3 port begins to draw a power equal to **20 kW** and the current from MV port is increased again. The power extracted for the MV port remains constant to **250 kW** and its voltage is well regulated to **750 V**.

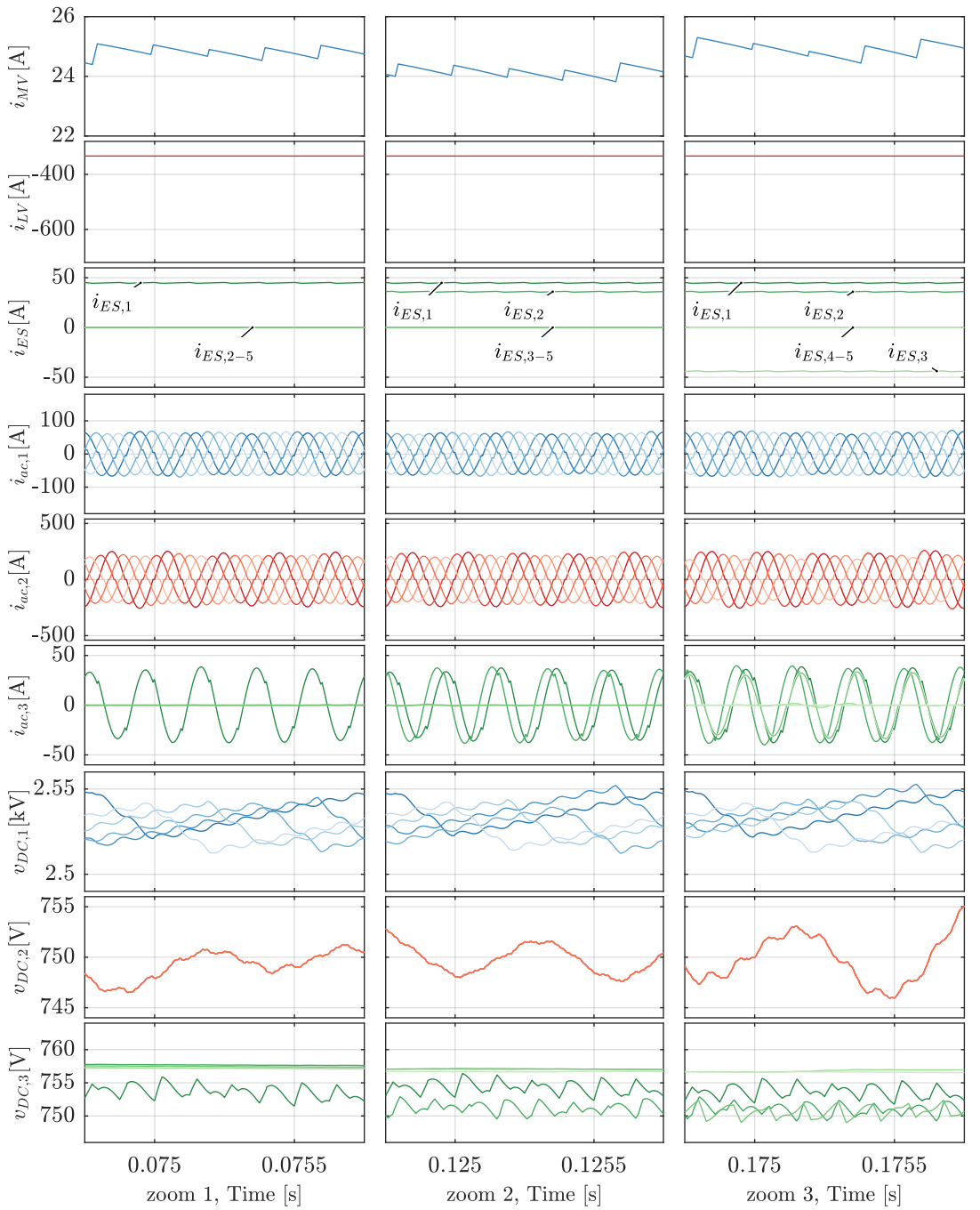


Figure 6.18 **Zoom 1**: all submodules except the number 1 are in SISO1 mode. The submodule 1 is in DISO1 mode and it $v_{DC,3}$ is subject to ripple, whereas the third port of submodule 2-5 are disconnected. **Zoom 2**: the submodule is also in DISO1 mode and the MV current is slightly decreased. **Zoom 2**: submodules 1 and 2 are in DISO1 mode while the port 3 is in SIDO1 mode. The current $i_{ES,3}$ is thus negative. In all the cases, the ripple is well in accordance with the theoretical predictions.

6.4 Experimental results

In order to verify the control principle for real, the proposed structure is implemented in a the control platform and tested for one submodule on the low voltage prototype described in the appendix B and depicted in **Fig. 6.19**. For the present experiment, a resistive load is connected on the port 2, a DC voltage source is connected on the port 1 and the super-capacitor is connected on the port 3. The voltage on the load (output voltage) v_{DC_2} is actively regulated to be 200 V while the super-capacitor on the port 3 is charged and discharged between 100 V and 150 V with a constant current. Oscilloscope measurements over the complete sequence are presented in **Fig. 6.20** while detailed view of the resonant current in the three modes presented are shown in **Fig. 6.21**.

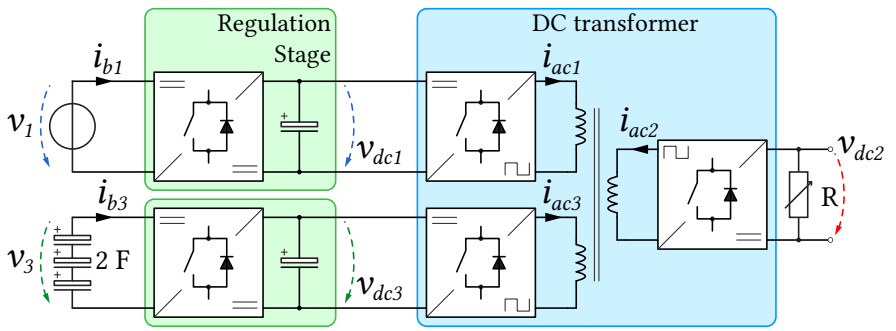


Figure 6.19 Low voltage setup as described in detail in appendix B. The super-capacitors on port 3 are charged and discharged, while the voltage on port 2 is regulated to a fix reference.

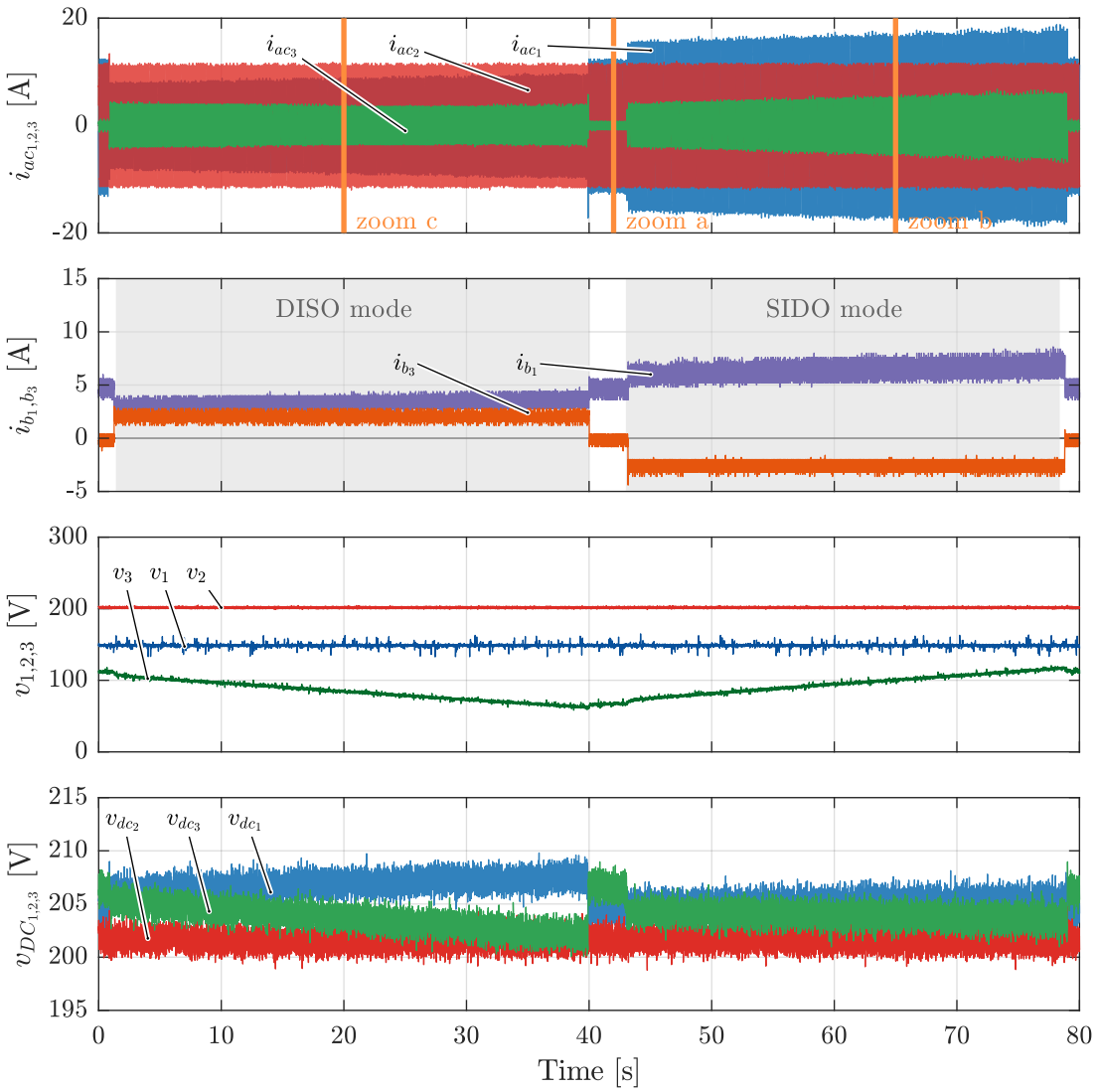


Figure 6.20 The super-capacitor bank is discharged from t = **1 s** to t = **40 s**. During this time, the submodule is in DISO mode and the current i_{b3} is regulated according to a positive constant setpoint. From t = **40 s** to t = **43 s**, the converter is in SIDO mode. the current i_{b3} and i_3 are zero and the power is flowing from port 1 to port 2 only. From t = **43 s** to t = **78 s**, the super-capacitor bank is charged, the voltage v_3 at its terminal increases and the converter is in SIDO mode. the current i_{b3} is regulated according to a negative constant setpoint. During the entire sequence, the output voltage v_2 is regulated according to the setpoint **200 V**. The voltages v_{dc1} and v_{dc3} of the DC buses evolve according to the v_{dif} necessary for the circulation of the requested currents. Detailed resonant waveforms corresponding to zoom a, zoom b and zoom c are illustrated in **Fig. 6.21**.

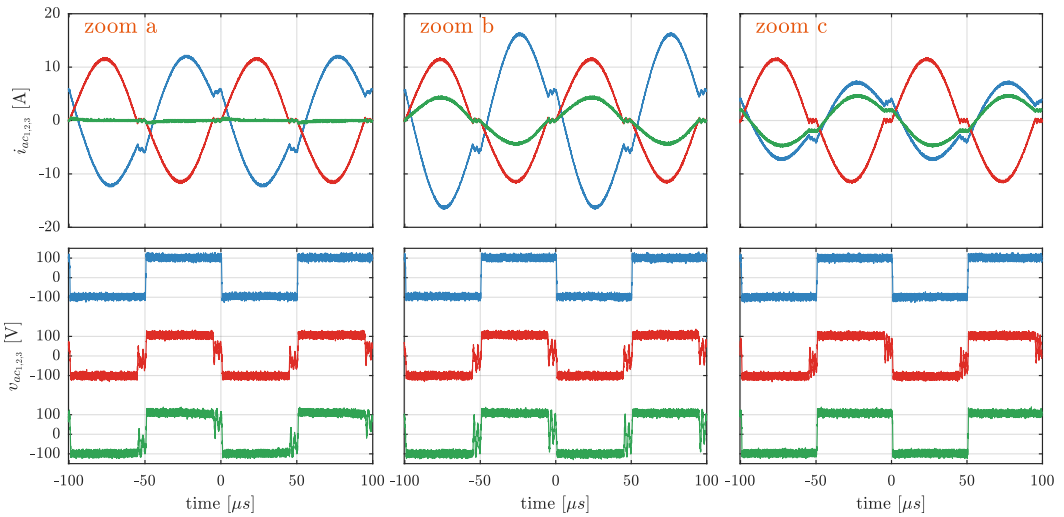


Figure 6.21 Resonant currents and AC voltages (port 1 in blue, port 2 in red, port 3 in green) in following modes: zoom a ⟶ SISOa, zoom b ⟶ SIDO1, zoom c⟶ DISO1. During the non conduction interval of the passive ports (rectifiers), their AC voltages are subjects to some oscillations between the resonant inductor and the output capacitance of the diodes.

6.5 Discussion

This chapter presents a model of the converter dynamics which simplification, by the approximation of the different DC buses with a single capacitor makes it possible to derive a relatively simple control structure. This structure allows to control the output voltage (for instance the voltage of the low voltage grid, in the simulated example) while independently controlling the currents to/from the storage elements. This leaves some degrees of freedom for an upper layer Energy Management System strategy or SOC control. In the example presented, the bandwidth of the controlled system is only 10 Hz. Nevertheless this seems enough considering storage applications which dynamic ranges from few seconds to minutes, like in the case of renewable resources. Moreover the proposed structure only requires the measurement of the DC currents at the regulation stage level and the voltages at the grids and storage elements terminals. The measurement of resonant currents would provide an estimation of the common-mode and differential-mode components that would allow a state control with a higher bandwidth but with a higher cost of implementation.

Simulation and experimental results validate the concept and show performances well in accordance with theoretical predictions for both case studies.

7 Conclusion

7.1 Summary and Contributions

The various scenarios of future MVDC grids and the targeted increasing penetration of renewable energy resources, such as presented in the *Chapter 1*, are driving the development of new types of converters, capable of interfacing both MV and LV grids, while flexibly integrating storage elements. In addition, the prospect of higher efficiency and reliability thanks to the reduction in the number of conversion stages motivates the study of solutions allowing an integrated connection of storage elements into the MV/LV converter and resulting in solutions based on multiport DC-DC-DC converters.

The *Chapter 2* presents a summary of existing or under-development topologies that have shown potential advantages in the field of medium-voltage and multiport DC/DC conversion. It appears that the recent progresses in the field of semiconductors make SST topology, mostly relying on power electronics components, a promising solution that provides a very high efficiency and a good power density thanks to the use of high frequency switching, positively impacting size of the MFT and the magnetics. In addition, its multi-modular structure, synonymous with redundancy, promises an increased reliability. When it comes to multiport topologies, it appears that most of proposed solutions are based on the DAB principle, extended to the multiport version of it and referred as MAB. These solutions allow galvanic isolation and a very effective regulation of the power flows through the various ports with phase-shift control but would become very complex in the case of a multi-modular structure, necessary to reach medium voltage.

In this way, the proposed structure is inspired by PETT, a particular case of SST where the galvanic isolation and voltage adaptation are performed with a resonant stage while the power and voltage are regulated through an additional control stage. The resonant stage is operated in a way to benefit from soft switching and tight DC voltage coupling. Its constant frequency operation then allows the integration of a third winding dedicated to a controlled port to which storage elements can be connected. As the structure is multi-modular, each level is equipped with an additional port, which enables the connection of several independent elements offering the opportunity to implement a hybrid storage solution. The voltage and power levels of the target application area as well as the willingness to use semiconductors from the market have led the development towards an IGBT-based solution that uses half-bridge switching cells.

The *Chapter 3* presents the topology, its functional blocks and its operating principle. Each stage is divided in three functional blocks, including a resonant stage that make the link between the three ports, performs the voltage adaptation, provides galvanic isolation and including as well two additional control stages which purpose is to regulate the power through the MV and ES ports. The

operation of the converter is divided into ten different modes based on the direction of the power flow which can be applied, under some restriction, independently to each submodule. The main difference between the modes is essentially the number of active/passive ports for the resonant stage and the buck or boost operation for the control stages. Thus, only the ports that supply power are actively switched. The others are acting as passive diode rectifiers, with the aim to limit the switching losses.

The *Chapter 4* proposes mathematical models of the resonant stage, in all the modes of operation. The approach makes it possible to derive equivalent circuits common to all the ports and to limit the number of different intervals to two per half-period, which makes the evaluation of the boundary conditions and the analytical approximation of the waveforms in steady state easier. The three modes SISO, DISO and SIDO associated to the resonant tank are modeled separately. In the case of DISO and SIDO modes, the models highlight that the power is shared in a natural way according to a fixed ratio which is set by the resonant tank parameters. In order to reach other operating points, namely with another sharing of the powers, the presence of a differential voltage between the inputs DC-bus (in the case of DISO mode) or between the outputs (case of SIDO mode) is necessary in order to force a circulation of power. In SIDO mode this circulating power does not affect the soft switching operation, while in DISO mode, it can lead to the loss of ZVS conditions on one of the ports and increase the turn-off current of the other which implies an increase of the switching losses on both of them. The characterization of the operating region benefiting from ZVS is possible thanks to the proposed model, but it relies highly on the value of parasitic resistance of the differential circuit which depends on the losses (conduction and switching) of the semiconductors as well as the losses associated to the MFT (core and winding losses). The proper characterization of the ZVS operating region and thus the identification of the losses would require the detailed simulation of the losses of both semiconductors and MFT or can be based on experimental measurement such as done in the chapter.

Nevertheless, clear insights of the ZVS operation area can be identified from the model and show that the conditions, in terms of efficiency, are better around the axis defined by the resonant inductors ratio. This criterion has been taken in account in the *Chapter 5* which presents a design methodology for the complete MEG converter targeting MV ratings. The number of submodule, the class of semiconductor and the switching frequencies are essentially sized to meet criteria based on losses and power that can be dissipated. Then, the resonant tanks are sized using criteria based on the ZVS conditions. These criteria are inspired from common techniques used for conventional bi-port LLC converters, namely the FHA. It allows to size a set of parameters which ensure ZVS for the complete operation range in SISO and SIDO modes. The soft switching operating area in DISO mode is evaluated by taking into account the physical parameters of the selected semiconductors and shows that the converter should also benefits from ZVS around the expected axis set by the tank parameters. Finally, the DC components are sized to meet ripple specifications and simulation results validate the performance of the design both with and without interleaving of the submodules.

The *Chapter 6* presents a model of the converter dynamics which simplification by the approximation of the different DC buses with a single capacitor makes it possible to derive a relatively simple control structure. This structure allows to control the output voltage (for instance the voltage of the LV grid in the simulated example) while controlling the currents to/from the storage elements independently. This keeps degrees of freedom for a upper layer strategy/SOC control. This simple concept is validated by simulation and experimental results which demonstrate good performances in terms of voltage regulation. Even though it has only a very limited bandwidth due to the approximation of the single

capacitor which is only valid at low frequency, the proposed structure only requires, in practice, DC current measurements at the regulation stage level as well as the grid voltage and the storage elements voltage.

7.2 Overall conclusion

The results obtained and the experiments carried out during this research show that the MEG principle, namely a multi-modular combination of multiport resonant converters, is feasible. It has also been shown that with a specific design, the ZVS operation is possible on all active ports, allowing both high blocking voltage class and lower blocking voltage class semiconductors to be used at a common frequency relatively high. In addition, the tight coupling of the DC buses of the different submodules makes the system very robust against voltage and current ripple as well as relatively easy to control thanks to its natural stability. However, it has also been shown that some operating range suffers from the loss of the soft switching which implies increased losses. In addition, the definition of this critical operating range depends on the parasitic parameters of the converter components and is therefore difficult to evaluate in a theoretical way. Even if the results are mitigated, this thesis validates the feasibility of the concept and some advantages and limits have been identified. Therefore, this topology deserves to be further explored in order to clearly establish its position in relation to other structures and this work provides good tools to start with.

7.3 Perspective of future works

In the immediate future, a detailed study of component losses, with T-CAD models for instance, and stresses as well as experimental validation would be required to complete the evaluation of the MEG topology.

This would then pave the way for the optimization of various parameters, including the optimal size of the magnetizing inductance (SRC vs LLC) and the resulting trade-off between turn-off losses and soft switching, or the choice of the switching frequency in relation to the resonant frequency, as well as the number of optimal submodule or the benefits of the use of wide band-gap semiconductors.

The optimization can also focus on the regulation stage where different converter structures than buck/boost could be used, such as composite converters, for instance, which is of particular interest in the case of converters with a duty-cycle almost constant, like for the regulation stage of the port 1.

The design of the MFT was not in the scope of this thesis. However, the three-winding is a key component of the MEG topology and its detailed study is necessary. Optimization and design of multi-winding MFTs is an interesting topic, considering need to precisely control various parameters.

In addition, the study of a topology similar to MEG in the case of a unidirectional application could reveal other advantages than the ones of a bidirectional system. For example, equipping the LV port with a simple diode rectifier, the bidirectionality of the main power flow would be lost but would allow to optimize the system for a buffered MV to LV conversion application.

Finally, the series or parallel coupling of the third port of each submodule also deserves to be studied. This solution would allow to couple other components than storage elements such as a second MV or

LV grid or even a third grid with an intermediate voltage.

Following the same idea, one possibility is use the MFT with additional windings and have more than three ports per submodules. This opens the door to various research on the realization of such MFT as well as the panel of application that such topology offers.

Above mentioned topics represent several possible future research directions in the field of multiport converters, and may lead to new discoveries in domains associated with research area covered in the thesis.

Appendices

A

RLC Circuit differential equations

In this appendix, the derivation of the theoretical inductor current and capacitor voltage waveforms is explained for a RLC circuit powered up with a square-wave voltage source.

The different state variables of the system are:

$v_o(t)$**:** voltage applied on the RLC circuit

$v_C(t)$**:** voltage across the capacitance

$v_L(t)$**:** voltage across the inductance

$v_R(t)$**:** voltage across the resistance

$i(t)$**:** current in the circuit

The differential equation in the RLC circuit are given in (A.1)

$$\begin{aligned} v_o(t) &= v_R(t) + v_L(t) + v_C(t) \\ &= Ri(t) + L\frac{di(t)}{dt} + \frac{1}{C}\int_0^t i(t)dt \end{aligned} \tag{A.1}$$

Since $v_o(t)$ is a square-wave voltage source, is can be considered as constant over its half period.

$$v_o(t) = V_o \tag{A.2}$$

In Laplace domain, A.1 gives (A.3).

$$\begin{aligned} v_o(s) &= v_C(s) + v_L(s) + v_R(s) \\ \frac{V_o}{s} &= \frac{V_{co}}{s} + \frac{1}{sC}i(s) + sLi(s) - Li_o + Ri(s) \end{aligned} \tag{A.3}$$

Introducing the damping factor α and the damped pulsation ω_d, given in (A.4), the current expression can be extracted from (A.3) in (A.5).

$$\begin{aligned} \alpha &= \frac{R}{2L} \\ \omega_0 &= \frac{1}{\sqrt{LC}} \\ \zeta &= \frac{\alpha}{\omega_0} \\ \omega_d &= \omega_0\sqrt{1-\zeta^2} \end{aligned} \tag{A.4}$$

$$\begin{aligned} i(s) &= \left(\frac{V_o}{s} - \frac{V_{co}}{s} + LI_o\right) \frac{1}{\frac{1}{sC} + sL + R} \\ &= \left(\frac{V_o - V_{co} - RI_o/2}{\omega_d L}\right) \frac{\omega_d}{(s+\alpha)^2 + \omega_d^2} + I_o \frac{s+\alpha}{(s+\alpha)^2 + \omega_d^2} \end{aligned} \tag{A.5}$$

Back in time domain, it gives (A.6) for the inductor current and (A.7) for the capacitor voltage.

$$i(t) = e^{-\alpha t}\left(I_o \cos\left(\omega_d t\right) + \frac{(V_o - V_{co} - RI_o/2)}{L_r \omega_d} \sin\left(\omega_d t\right)\right) \tag{A.6}$$

$$v_c(t) = e^{-\alpha t}\left((V_{co} - V_o))cos(\omega_d t) + (\frac{\alpha}{\omega_d}(-V_o + V_{co} + I_o R/2) + LI_o\omega_d)sin(\omega_d t)\right) + V_o \tag{A.7}$$

B
Low Voltage Prototype

In order to support the theoretical developments of this thesis by experimental results, a low-voltage prototype has been built. A complete submodule as illustrated in the **Fig. B.1** is implemented in a setup as depicted in **Fig. B.2**. The switching cells are half-bridges modules from the market and are described in Section B.1. The MFT is dimensioned with a very high coupling coefficient, in order to minimize the leakage inductances in a way to offer great freedom in the choice of resonant inductances by using external components. Its design is presented in Section B.2 and no thorough optimization is performed. The resonant tanks consist of discrete components in order to be able to test various combinations. Their selection is presented in Section B.3. The complete system is controlled with the help of a commercial control platform on which the state-machine as well as the control loops have been implemented such as described in Section B.4.

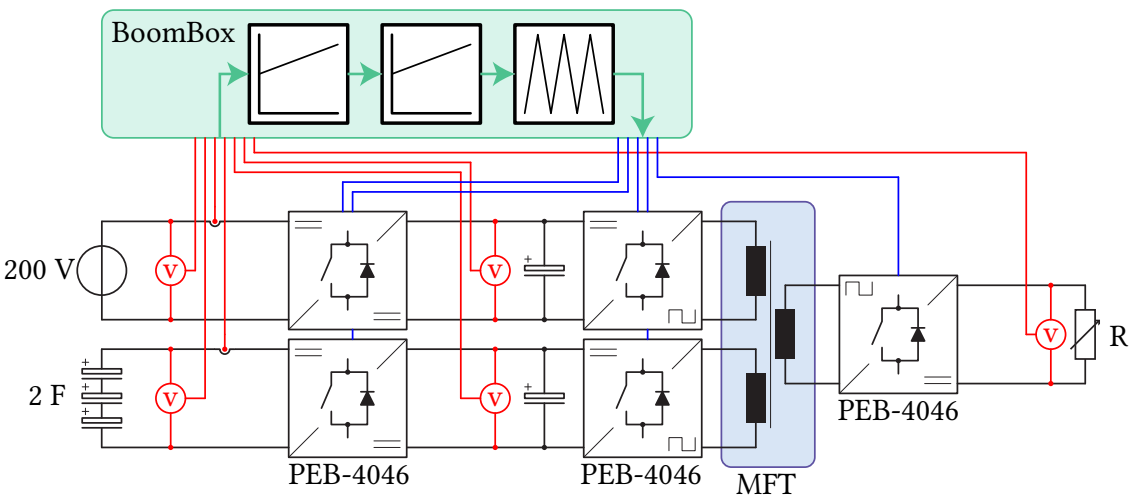


Figure B.1 Configuration of the low voltage prototype.

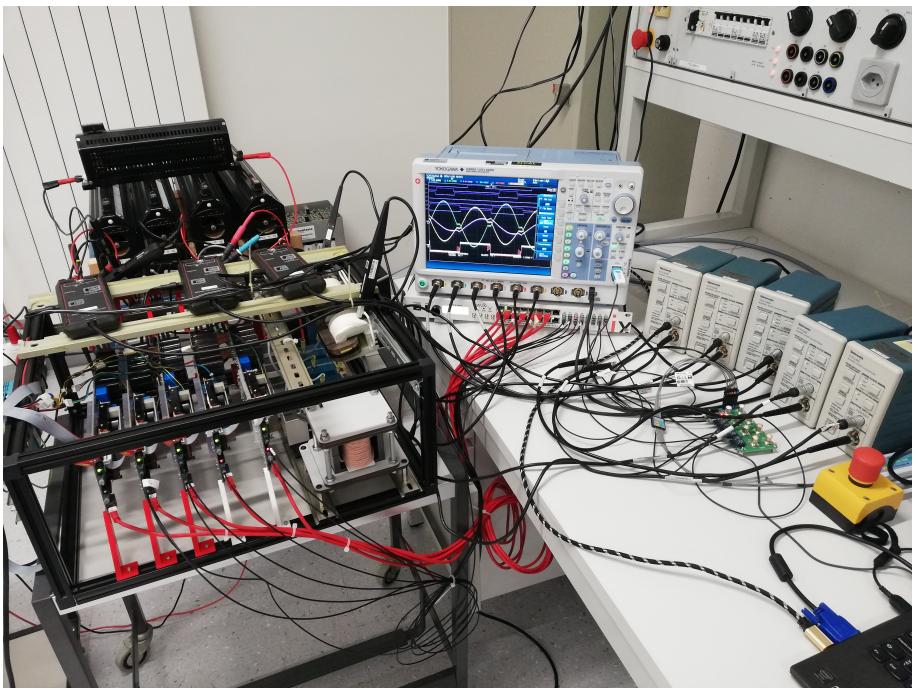


Figure B.2 Low voltage setup.

B.1 Switching Cells

The switching cells are implemented with the help of five commercial PEBBs (PEB-4046 modules) from Imperix [120]. Each PEBB integrates a half-bridge made out of two 600 V IGBTs (IXYS MMIX1X200N60B3H1 [121]) and DC-bus capacitors (C_{DC} = 825 µF). The gate signals are transmitted via an optical fiber interface and either DC-bus voltage or AC current measurements are available from built-in sensors.

Both regulation stages are equipped with inductor filters L_{b1} and L_{b3} both of 3 mH.

B.2 MFT

The MFT comprises three winding with the same number of turns n using a 60 strands 0.335 mm^2 Litz-wire (resulting section A_{wire} is equal to 21.3 mm^2). The E shape ferrite core chosen is the E80/38/20 from Epcos and the relevant informations from the datasheet [122] are given in Table **B.1**.

Table B.1 Parameters of the ferrite core E80/38/20

Material	μ_r	B_{max}	A_{core}	l_{core}	A_N
N87	1680	320 mT	320 mm^2	184 mm	1070 mm^2

The window area of the ferrite A_N gives the limit of the maximal number of turns, considering three

winding, in (B.1).

$$n_{max} = \frac{A_N}{3A_{wire}} = 16 \tag{B.1}$$

In order to stay below B_{max} and not enter the saturation region of the ferrite, a number N_c of cores can be put in parallel, increasing this way the cross section. The minimal number of turns to stay below B_{max} is given by (B.2) according to [123].

$$n_{min} = \frac{V_{in}}{K_f B_{max} f_{sw} A_{core} N_c} \tag{B.2}$$

The DC-bus are operated under 360 V which the voltages are square wave of amplitude V_{in} equal to 180 V. The waveform factor K_f is equal to 4 in the case of square wave voltage. This results in

$$\begin{aligned} N_c = 1 &\longrightarrow n_{min} = 30 \\ N_c = 2 &\longrightarrow n_{min} = 20 \\ N_c = 3 &\longrightarrow n_{min} = 10 \end{aligned} \tag{B.3}$$

The window area of the ferrite is too small for three windings with 20 or 30 turns ($n_{max} = 16$), so the last option is chosen:

$$\begin{aligned} N_c &= 3 \\ n &= 10 \end{aligned} \tag{B.4}$$

The reluctance of the core R_{core} and the air-gap R_{gap} are given by (B.5)

$$\begin{aligned} R_{core} &= \frac{l_{core}}{\mu_r \mu_0 N_b A_{core}} \\ R_{gap} &= \frac{l_{gap}}{\mu_0 N_b A_{core}} \end{aligned} \tag{B.5}$$

The magnetizing inductance can be expressed from the geometry of the core and the number of turn as

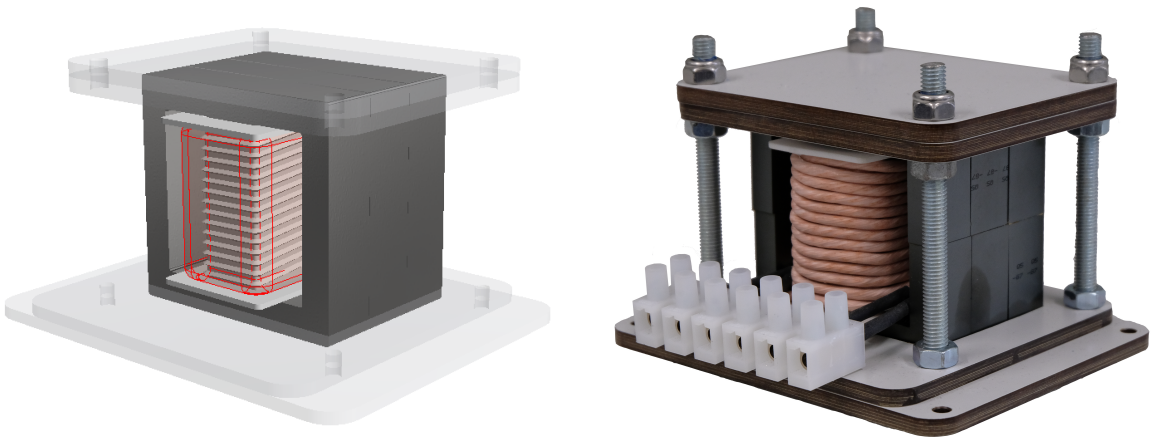
$$L_m = \frac{n^2}{R_{core} + R_{gap}} = \frac{n^2 \mu_0 N_c A_{core}}{\left(\frac{l_{core}}{\mu_r} + l_{gap}\right)} \tag{B.6}$$

This allows to calculate the air-gap necessary to match the required value for L_m according to the specification:

$$l_{gap} = \frac{n^2 \mu_0 N_b A_{core}}{L_m} - \frac{l_{core}}{\mu_e} = 258\,\mu\text{m} \tag{B.7}$$

In practice, the gap is realized with four layers of Kapton tape with a 65 µm thickness. This results in an effective gap of 260 µm corresponding to an effective L_m of 398 µH.

In order to be able to play on the resonant inductors value with external component, the three windings are wound in such way to provide a very good coupling and very low leakage inductances. No further isolation than the wire sheath is used, which is nevertheless sufficient for low voltage operation. The **Fig. B.3** show a 3D model and a photography of the actual three-winding MFT. Measured leakage inductances and parasitic resistors of the MFT are given in Table **B.2**.



(a) (b)

Figure B.3 CAD model of the three-winding MFT (a) and realization of it (b).

Table B.2 MFT parameters measured at **10 kHz**

L_m	$L_{\sigma,1}$	R_1	$L_{\sigma,2}$	R_2	$L_{\sigma,3}$	R_3
408 µH	0.8 µH	1.2 mΩ	0.7 µH	2.1 mΩ	1.7 µH	1.5 mΩ

B.3 Resonant Tanks

The three resonant tanks are designed to have a resonant frequency of 12 kHz. The inductance ratio is chosen so that, in *DISO* mode, the port 1 provides half the power supplied by the port 2. The result is the k factors, as defined in Chapter 4, given below:

$$\begin{aligned} k_{12} &= \frac{1}{3} \quad k_{21} = \frac{2}{3} \\ k_{13} &= \frac{1}{3} \quad k_{31} = \frac{2}{3} \\ k_{23} &= \frac{1}{2} \quad k_{32} = \frac{1}{2} \end{aligned} \tag{B.8}$$

This implies:

$$L_1 = L_2 = \frac{L_3}{2} \quad \text{and} \quad C_1 = C_2 = 2C_3 \tag{B.9}$$

The resonant tanks are finally implemented using discrete components (inductors Ticomel SD-48-15.0-35 [124] and film capacitors Kemet C4B [125]), combined in series or in parallel in order to obtain the ratios of (B.9). The resulting values (expected as well as measured) are given in Table **B.3**. The actual resonant frequency of the combination of the 3 resonant tanks is equal to 11.66 kHz.

Table B.3 Resonant tanks components

	f_{res}	L_1	C_1	L_2	C_2	L_3	C_3
expected values	12 kHz	35 µH	5 µF	35 µH	5 µF	70 µH	2.5 µF
measured values	11.66 kHz	37.91 µH	4.89 µF	37.86 µH	4.90 µF	78.54 µH	2.42 µF

B.4 Control Platform

The control loop is implemented using Imperix Boombox control platform which includes a programmable DSP. The current and voltage measurements required to control the system are collected from the PEBB on-board sensors and transmitted to the Boombox using proprietary protocol. The measurement processing, PI controllers and modulation index calculations are performed by the DSP in which the state machine and transitions between the different operating modes have been programmed. The algorithm operates synchronously with the switching of the resonant stage (i.e. at 10kHz). The Boombox finally provides the gate signals that are transmitted to the PEBBs via optical fibers.

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2017 BSc semester project supervision (*Mechanical integration of a super-capacitor bank*)

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Electrical design, control implementation, mechanical integration, mounting, commissioning of grid connected inverters (380V/120kW) for smart grid applications (fuel-Cell, batteries)

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PCB design, mounting and testing. Embedded programming

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