Impact of GigaRad Ionizing Dose on 28 nm Bulk MOSFETs for Future HL-LHC

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***Abstract*—The Large Hadron Collider (LHC) running at CERN will soon be upgraded to increase its luminosity giving rise to radiations reaching the level of GigaRad Total Ionizing Dose (TID). This paper investigates the impact of such high radiation on transistors fabricated in a commercial 28 nm bulk CMOS process with the perspective of using it for the future silicon-based detectors. The DC electrical behavior of *n*MOSFETs is studied up to 1 Grad TID. All tested devices demonstrate to withstand that dose without any radiation-hard layout techniques. In spite of that, they experience a significant drain leakage current increase which may affect normal device operation. In addition, a moderate threshold voltage shift and subthreshold slope degradation is observed. These phenomena have been linked to radiation-induced effects like interface and switching oxide traps, together with parasitic side-wall transistors.**

***Keywords*—high-k, HL-LHC, MOSFET, radiation, TID, total ionizing dose, 28nm bulk CMOS,**

I. Introduction

The Large Hadron Collider (LHC) at CERN is the largest scientific instrument ever built. It has been exploring the new energy frontier since 2010 and made possible the successful observation of the Higgs Boson in 2012. To extend its discovery potential, the LHC will need a major upgrade around 2020 to increase its luminosity (rate of collisions) by a factor of 10. The novel machine, called High Luminosity LHC (HL-LHC), will rely on a number of key innovative technologies, representing exceptional technical challenges. The higher event rates and event sizes will be a challenge for the trigger and Data Acquisition (DAQ) systems, which will require a significant expansion of their capacity. In particular, pixel read-out channels are required to sustain unprecedented radiation levels of 10 MGy (1 Grad) Total Ionizing Dose (TID) and 10^{16} neutrons/cm^2 in 10 years, a level of total dose that has never been experienced before.

In this context, the investigation in CMOS radiation-hardening has been following two parallel approaches. The first is related to circuital/layout techniques, while the second is devoted to CMOS technologies characterization. The former is devoted to circumvent radiation effects with dedicated solutions, aiming at reducing radiation-induced damages/errors or compensating for them. This has brought to specific techniques, like redundant digital blocks with inclusions of voters [1] or, more specifically, custom transistor layouts [2], which have been demonstrated to be effective. Unfortunately, some of the cited techniques (such as enclosed-layout transistors) have been rendered unfeasible

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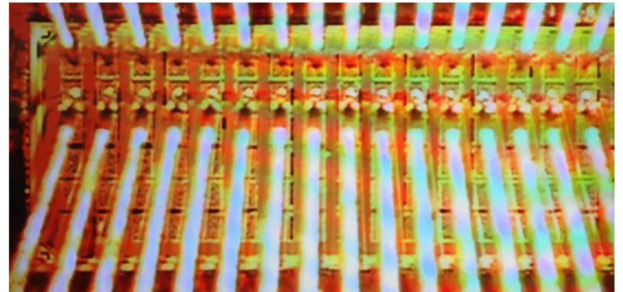

Fig. 1. Test chip under measurement probes

in ultra-scaled technology nodes, due to their stringent design rules constraints [3]. On the other hand, the latter branch has been focusing on characterization of specific CMOS technological nodes under radiation. In literature, it has been demonstrated that the radiation damage is larger for devices with thicker gate oxide, but in ultra-scaled technologies, SiO_2 gate dielectric has been replaced by high-k materials [4], whose TID-induced effects have yet to be investigated. Moreover, the latest CMOS technologies are available either in bulk or SOI processes. In [5], for the same feature size, bulk CMOS has been found more radiation-resistant than SOI. The effects due to ionizing radiation can hence be reduced by choosing an advanced bulk technology.

Only a few papers have indeed been dedicated to the effects in electronic devices at very high TID [5]–[8]. Moreover, to our knowledge, none have been published about the combination of high dose on nanoscale CMOS technology, especially 28 nm bulk CMOS. Consequently, the Scaltech28 and GigaRadMOST projects propose to investigate on a 28 nm bulk CMOS process, which is expected to be more radiation-resistant. Moreover, it should provide the highest bandwidth that can be exploited for shorter shaping time and hence better SNR in DAQs. It is important to note that this is the first characterization of a commercial 28 nm bulk high-k CMOS technology related to TID effects. It is focused on nMOSFETs, whose crucial design-related parameters variation versus TID is investigated via DC measurements including trends of threshold voltage, subthreshold slope, drain leakage and drive currents.

The paper has been organized as follows. Section II presents the measurement set-up whereas the DC measurements of nMOSFETs with respect to TID are discussed in Section III. A comparison with existing 65 nm node data is performed in Section IV, followed by conclusions.

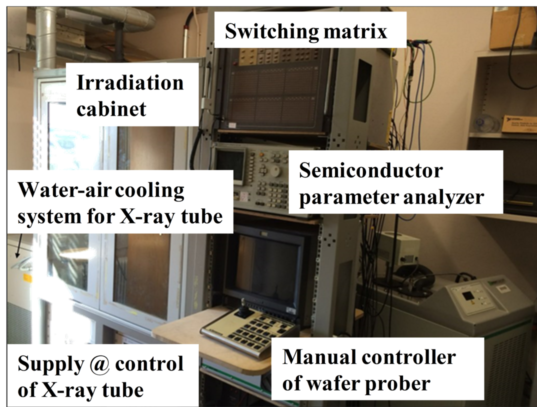

Fig. 2. Scheme of Irradiation and Measurement Setup from the CERN EP-ESE website (http://proj-xraymic.web.cern.ch/proj-xraymic/)

II. Measurements Setup

Test chips with a matrix of single devices (Fig. 1) have been fabricated in a high-performance 28 nm bulk-CMOS technology. The matrix is composed of six device clusters, as listed in Tab. I. These single transistors are designed in six rows with 24 access pads each. The first four clusters include two types of nMOSFETs and pMOSFETs: standard and high threshold voltage (V_{T0}). Devices in the same group share the source and the substrate contacts but have individual gate and drain contacts. Several widths (W) and lengths (L) have been chosen for all types of MOSFETs:

- L = 1 µm with W = 3 µm, 400 nm, 200 nm, and 100 nm
- L = 30 nm with W = 3 µm, 1 µm, 300 nm, and 100 nm
- L = 60 nm with W = 1 µm
- L = 90 nm with W = 1 µm.

The investigation has been focused on standard V_{T0} nMOSFETs. Both irradiation and measurements were conducted with the setup shown in Fig. 2. The chip was mounted on a Karl-Suss PA200 semi-automatic 8-inch wafer probe station with a custom prober card within an X-ray irradiation cabinet. The prober card includes 32 probe tips (two columns of 16). A Keithley 707 switching matrix connects the four Single-Measuring-Units (SMUs) of the semiconductor device analyzer (HP4145B) and the voltage supply to specific probe tips. In this way, each cluster can be biased correctly during irradiation and measurements, as shown in Fig. 1.

TABLE I. Chip clusters list

Cluster #	Devices
1	nMOSFET with standard V_{T0}
2	pMOSFET with standard V_{T0}
3	nMOSFET with high V_{T0}
4	pMOSFET with high V_{T0}
5	minimum-size nMOSFETs with standard V_{T0}
6	High Voltage MOSFETs, diodes, capacitors

A. Measurement protocol

The irradiation was conducted up to 1 Grad by using CERN's in-house 50 kV 3 kW X-ray generator (SEIFERT RP149). The absorbed dose rate was about 8.82 Mrad/h, referred to SiO_2. During irradiation, the chip was under the worst-case bias condition, with drain and gate biased at 20% more than the technology recommended supply voltage (1.2 V) while source and substrate terminals were grounded. This condition maximizes either the horizontal or vertical electric field applied to the devices. After reaching a certain total dose, the DC characterizations on all the transistors were individually performed. A voltage step of 25 mV was chosen as a suitable compromise between limiting annealing process and sufficient measurement resolution. The described procedure has been carried out cyclically, whilst the ambient temperature was kept at 25 °C. The whole setup was remotely controlled, enabling sequential and automatic irradiation steps and measurements.

III. nMOSFET Performance versus TID

A. Irradiation effects on $I-V$ characteristics

The main degradation mechanism caused by TID in MOSFETs is related to radiation-induced states of charge buildup inside the oxide (N_{ot}) and at the Si-oxide interface (N_{it}). The primary impact of inner oxide trapped charges on DC parameters is, for a fixed drain current, a V_G bias point shift to lower values for both n- and pMOSFETs. Namely, it corresponds to an absolute threshold voltage decrease for nMOSFETs and an increase for pMOSFETs.

Additionally, the primary effect of N_{it} is an increase in the subthreshold slope. Large concentrations of interface states has the effect of decreasing the carriers mobility and thereby increasing the threshold voltage in nMOSFETs. Moreover, switching oxide traps can also change the charge states, as the DC gate-to-source bias is varied. As a result, distinguishing the effects of interface traps and switching oxide traps is not trivial.

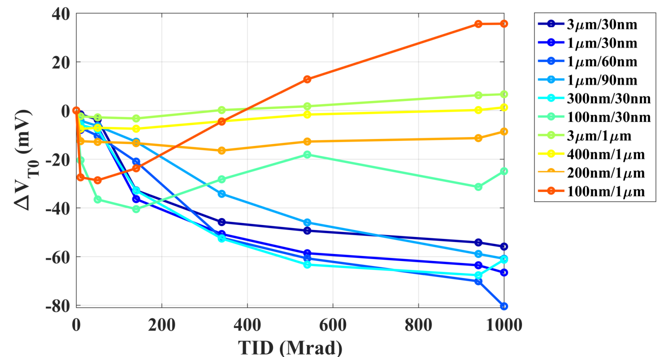

Fig. 3. Threshold voltage variation (V_{T0}) w.r.t. TID for different physical parameters at V_D=1.1 V.

B. Threshold voltage

In Fig. 3, the threshold voltage variation versus TID is shown for all measured devices. As mentioned previously, for nMOSFETs, trapped holes in oxide (N_{ot}) tend to reduce V_{T0}, whilst interface states (N_{it}) tend to increase it. As the trapped holes have a faster dynamic, they are dominant at the beginning of irradiation, as observed in Fig. 3 and 7. It is also clear that no general trend is experienced for V_{T0} variation with respect to TID. In fact, for some devices a general decrease is observed, however for others the trend is not monotonic due to superposition of the described effects. Namely, the trend is

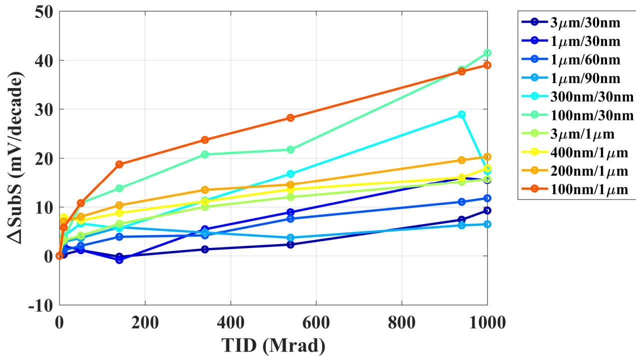

Fig. 4. Subthreshold slope variation ($SubS$) w.r.t. TID for different physical parameters at V_D=1.1 V.

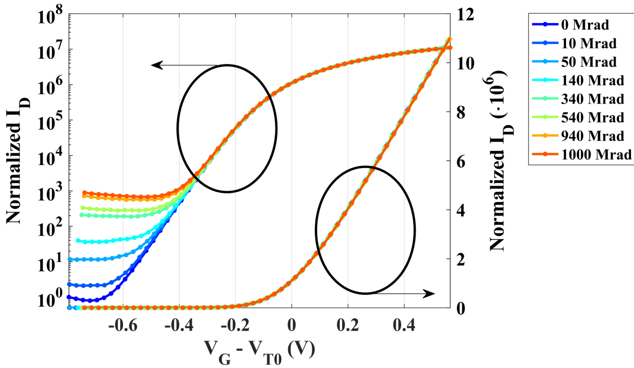

Fig. 5. Normalized I_D vs. V_G-V_{T0} curve w.r.t. TID for widest nMOSFET (3 μm/30 nm) at V_D=1.1 V.

opposite for large and short devices compared to narrow and long. It is important to note that the experienced V_{T0} variation is comparable with CMOS process-related spread [3].

C. Subthreshold slope

On the other hand, $SubS$ variation with respect to TID can be reasonably considered monotonic for all the devices, as depicted in Fig. 4. Then, in order to isolate V_{T0}-related effects from those related to $SubS$, the drain current with respect to $V_G - V_{T0}$ is plotted in Fig. 5 for the widest (3 μm/30 nm) and in Fig. 6 for the longest (100 nm/1 μm) device. In this way, the channel inversion conditions are comparable between the results at different TIDs. For the widest device case, the curves overlap (neglecting leakage region), meaning that TID affects mostly the V_{T0} rather than $SubS$. Moreover, the mobility reduction is basically negligible, as evinced from the strong inversion region (high $V_G - V_{T0}$). On the contrary, for the longest channel, the $SubS$ increase is noticeable and the mobility reduction effect also emerges, as evidenced in the drive current (I_{on}) shown in Fig. 7.

D. Drain leakage current and drive current

Radiation-induced degradation in oxides can cause a significant increase in drain leakage current of MOSFETs. Positively charged oxide defects invert an adjacent p-type silicon layer, enabling the current to flow from one isolated region to another. Therefore, charges trapped in the Shallow-Trench Isolation (STI) dielectric create a leakage path, which becomes

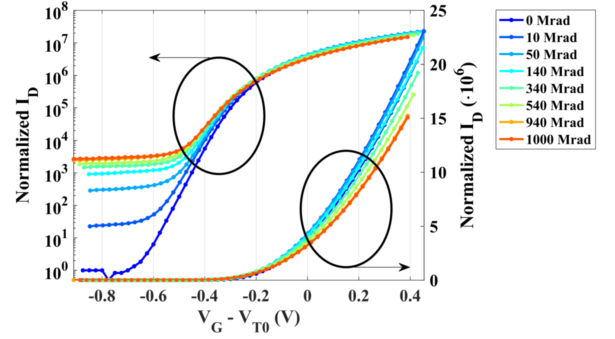

Fig. 6. Normalized I_D vs. V_G-V_{T0} curve w.r.t. TID for longest nMOSFET (100 nm/1 μm) at V_D=1.1 V.

the dominant contributor to off-state drain-to-source leakage current (I_{off}) in nMOSFETs. As illustrated in Fig. 8, I_{off} begins to show a monotonic increase versus TID.

Notice that, as mentioned, large concentrations of interface-trapped charges can decrease the carriers mobility and increase nMOSFET threshold voltage. These effects together will tend to make the drive current decrease. Moreover, positive charges trapped in the STI sidewall form a conductive channel through which the leakage current can flow from source to drain, when the lateral parasitic transistor is turned on. Therefore, as demonstrated by results obtained in other operating regions, such as moderate or strong inversion, ionizing radiation effects have a much smaller impact on drive current (see Fig. 7) than the previously analyzed parameters.

Overall, all tested devices withstand 1 Grad TID. This

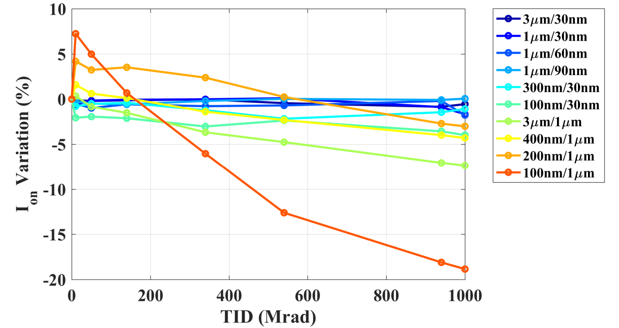

Fig. 7. Drive current variation (I_{on}) w.r.t. TID for different physical parameters at V_D=1.1 V.

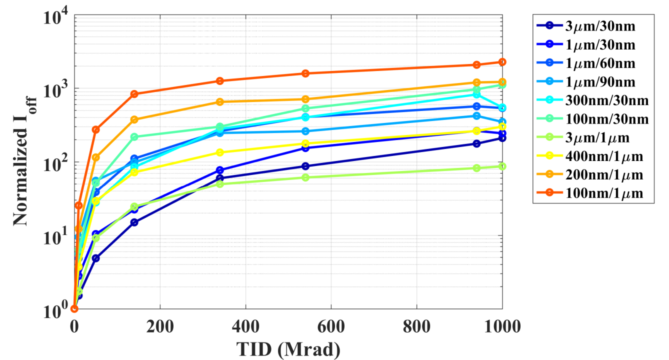

Fig. 8. Drain leakage current (I_{off}) w.r.t. TID for different physical parameters at V_D=1.1 V.

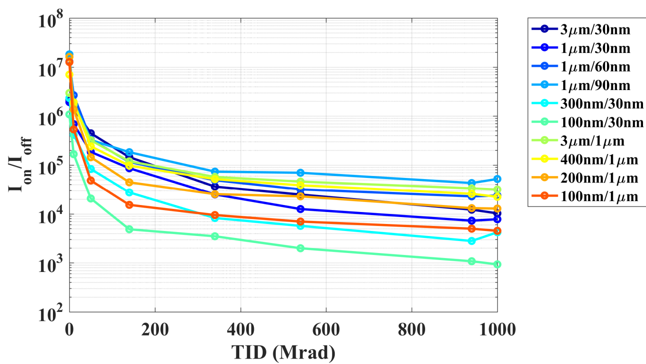

Fig. 9. I_{on}/I_{off} ratio w.r.t. TID for different physical parameters at V_D=1.1 V.

is confirmed in Fig. 9, where even if, in the worst case (minimum-size device), the I_{on}/I_{off} ratio degrades by four orders of magnitude, it remains greater than 10^3. It is also clear that this degradation is mainly caused by the increase in drain leakage current.

IV. Comparison with 65 nm node

To understand the scaling-down effect on performance versus TID, the comparison between this node and a 65 nm technology from the same manufacturer [6] is discussed below. Notice that for making the TID effect on I_{on} to emerge, it has been isolated from the V_{T0} variations, considering the drive current always in the same channel inversion conditions (constant $V_G - V_{T0}$). This allows for a fair comparison between different technology nodes, and a more detailed analysis of TID effects on mobility and external parasitic transistors.

A. Threshold voltage and subthreshold slope

The first difference is found in terms of V_{T0}, for which the trend is generally opposite between the two nodes. In fact, in the 65 nm node, an increase is experienced for wide devices (W/L=1 μm/60 nm), while for the same W and L in 28 nm node, the V_{T0} is monotonically decreasing (see Fig. 3). This would lead the oxide traps generation process to dominate over interface traps, as mentioned in Section III. Nevertheless, the global absolute V_{T0} variation for the 28 nm node is within 70 mV for all devices, whilst in the 65 nm node this spread can reach more than 300 mV.

The variation of $SubS$ shown in the 65 nm node nMOSFETs [6] is similar to the results obtained with the 28 nm node devices. In fact, the degradation reaches in both cases 40 mV/dec with respect to non-irradiated data.

B. Drain leakage current

Among all differences, certainly the most evident one is related to the drain leakage current. Indeed, the 28 nm node demonstrates a much larger leakage compared to the 65 nm node. For the same device dimensions (W and L), the leakage current in the 28 nm node is increased by three orders of magnitude. This is contradictory with respect to data available in the literature [6]. This could result from modifications of the Shallow-Trench-Isolations (STI) either in material or dimensions. Supposing the STI is bigger in the 28 nm node than in the 65 nm node, the density of positive charges generated near the STI-channel interface increases. The lateral parasitic transistor could be switched on, leading to a larger leakage current.

V. Conclusion

As a result of this analysis, which is the first dealing with TID-related effects on a 28 nm bulk CMOS technology, some crucial considerations can be carried out. First of all, standard V_{T0} nMOSFETs fabricated in this technology are tolerant to 1 Grad TID, paving the way for exploiting this 28 nm node in the design of radiation-tolerant devices to be included in the future HL-LHC experiment. Nevertheless, a significant degradation is observed in the drain leakage current, differently from what occurred in the 65 nm node and in older CMOS technologies. The trend regarding the subthreshold slope confirms data related to the 65 nm node, while the experienced threshold voltage shift, comparable with CMOS process-related variation, shall not compromise the nMOSFET normal operation. These effects are strictly linked to the generation of charge traps either inside oxides or at Si-oxide interfaces. In order to fulfill the characterization with further experimental evidences, pMOSFETs are currently under investigation.

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