A Low-Power Microwave *LC* Oscillator Operating Down to 1.4 K

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Abstract—High-electron-mobility transistors (HEMTs) based on 2-D electron gases (2DEGs) in III–V heterostructures have superior mobility compared with the transistors of silicon-based complementary metal–oxide–semiconductor technologies. The large mobility makes them attractive not only for low-noise and high-power microwave applications but also for low-power applications down to deep cryogenic temperatures. Here, we report on the design and characterization of a low-power HEMT *LC* Colpitts oscillator operating at 11 GHz whose minimum power consumption is 90 μW at 300 K and 4 μW at 1.4 K. The fully integrated oscillator is based on a single HEMT transistor having a gate length of 70 nm and realized using a 2DEG in $In_{0.7}Ga_{0.3}As$. The power consumption of the realized oscillator is the lowest reported in the literature so far for an *LC* oscillator operating in the same frequency range. In order to investigate the behavior of the oscillator, we also performed a detailed characterization of a stand-alone HEMT transistor from 1.4 to 300 K with a static magnetic field from 0 to 8 T. From the extracted values of the transistor parameters, we estimate and compare the minimum power necessary to start-up oscillations for two different Colpitts topologies.

Index Terms—Colpitts, high-electron-mobility transistor (HEMT), *LC* oscillator, low temperatures, ultralow power.

I. INTRODUCTION

HIGH-electron-mobility transistors (HEMTs) based on 2-D electron gases (2DEGs) in III–V heterostructures have superior charge carrier mobility compared with the silicon-based complementary metal–oxide–semiconductor (CMOS) technologies. The large mobility makes them particularly attractive for a variety of low-noise and high-power radiofrequency, microwave, and terahertz applications [1]–[4]. HEMTs are currently widely used also for cryogenic applications and considered as promising candidates for the cold read-out electronics of future quantum computers [5]–[13]. At temperatures of about 1.5 K and above, the cooling power of ^{4}He-based cooling systems can exceed 100 mW [14]. At temperature below 1.5 K, the effective cooling power available with ^{3}He and ^{3}He^{4}He dilution refrigerators is typically

below 1 mW [15]. Hence, for applications at temperatures in the order of 1 K and below, electronics has to be designed considering power dissipation as a major critical constraint.

In this paper, we investigate microwave *LC* oscillators based on HEMTs, with the goal of using them for low-temperature studies and applications. In particular, we report on the design and characterization of an ultra low power consumption HEMT-based *LC* Colpitts oscillator [16]–[18] operating at 11 GHz and in the temperature range from 1.4 to 300 K, at least. The achieved power consumption is of 90 μW at 300 K and 4 μW at 1.4 K.

In the design of integrated CMOS and HEMT microwave oscillators, the main effort is usually focused on the improvement of phase noise, output power, and tuning range [19]–[22]. Recently, motivated by their use in room temperature applications where power consumption is important (such as RF identification), several low-power consumption CMOS and HEMT designs have been reported [23]–[32]. For example, an HEMT oscillator operating at 4.7 GHz has achieved a power consumption of 2.7 mW [32], whereas the CMOS oscillators have achieved a power consumption of 280 μW at 40 GHz [23] and, very recently, 130 μW at 57.4 GHz [26]. A very limited literature exists on microwave oscillators operating at liquid helium temperature (i.e., 4.2 K) and below [13], [33]–[35]. The lowest reported power consumption is of about 7 mW [13]. Hence, the HEMT oscillator reported in this paper achieves a room temperature power consumption, which is slightly better than the state of the art, and significantly lower power consumption at low temperature.

Reducing the power consumption in *LC* oscillators is of crucial importance, e.g., for their application as single-chip electron spin resonance (ESR) spectroscopy detectors at low temperatures [36]–[41]. Exploring the behavior of microwave *LC* oscillators in cryogenic conditions is also interesting for studies of the phase noise of thermal and nonthermal origins [17], [42]. Particularly interesting would be the operation in the condition $\hbar\omega > k_B T$, which should result in a dramatic reduction of the phase noise of thermal origin, well beyond the linear dependence on T of the power spectral density in the condition $\hbar\omega < k_B T$ [43], [44], where k_B is Boltzmann's constant, T is the temperature, $\hbar$ is the reduced Planck constant, and ω is the oscillation angular frequency. The study of the zero-point quantum noise [43], [45]–[48], which, in this case, should be possibly present in the form of oscillator phase noise, would also be experimentally accessible.

II. Description of the Realized Devices and the Measurements Setup

In this paper, we designed and investigated the behavior of a stand-alone HEMT transistor and a microwave *LC* Colpitts oscillator based on a single HEMT transistor. In particular, we performed their characterization in the temperature range from 1.4 to 300 K and in the magnetic field range from 0 to 8 T. Both devices were manufactured using an HEMT technology having a minimum gate length of 70 nm (D007IH mHEMT, OMMIC, France). The transistor channels consist of a 2DEG in $In_{0.7}Ga_{0.3}As$. In [3] and [49], transistors and low-noise microwave amplifiers fabricated with the same technology are characterized in the temperature range from 20 to 300 K. In this paper, we extend the investigation to microwave oscillators, enlarging also the temperature range and adding a strong magnetic field as a means to extract useful information about the properties of the transistors.

Fig. 1(a) shows the layout of the stand-alone HEMT transistor, which consists of four fingers having a width of 15 μm, a drain–source distance of 2.5 μm, and a gate length of 70 nm. The properties of this stand-alone HEMT transistor as a function of the temperature (1.4 to 300 K) and the magnetic field (0 to 8 T) are investigated in Section III.

Fig. 1(b) and (d) show a photograph of the realized HEMT *LC* Colpitts oscillator and its detailed schematics, respectively. As shown in Fig. 1(d), the oscillator consists of a single HEMT transistor, a single-turn planar coil inductor, a resistor, and two capacitors. The realized common-drain Colpitts topology achieves low output impedance without loading the *LC* resonator. The capacitors C_1 and C_2 not only provide positive feedback to the amplifier but also form the resonator with the inductor. The inductor is connected to ground by means of metalized holes (vias) connecting the top side to the bottom side of the chip. These metalized holes are useful to avoid the use of bonding wires for ground connections, hence allowing the implementation of nondifferential topologies with low parasitics. Since the source–drain ON-resistance of the HEMT transistor and the dc resistance from gate to ground are very low, the 500 Ω resistor determines the dc operating point of the oscillator and acts as a current source. The operating frequency of the oscillator depends on the bias voltage V_{DD} and on the temperature, with an overall range from 11.2 to 11.7 GHz. The integrated Colpitts *LC* oscillator has a size of 0.8×0.5 mm^2 [see Fig. 1(b)]. A conductive epoxy (Epo-Tek, H20E-FC) is used to glue the chip to a standard FR4 printed circuit board. Au wires having a diameter of 20 μm are used for wedge–wedge bonding of the chip to the board.

Fig. 1(c) shows the block diagram of the setup used to characterize the stand-alone HEMT transistor and the HEMT *LC* Colpitts oscillator. The stand-alone transistor is connected to a semiconductor parameter analyzer in Kelvin four-wire configuration. The signal at the output of the oscillator is downconverted to 200 MHz to match the central frequency of a homemade delay-line-discriminator (DLD) [50], [51], which performs the frequency-to-voltage conversion. The amplifiers shown in the block diagram are used to match the dynamic range of the frequency dividers and of the analog-to-digital-converters of the acquisition board. The filters are used to improve the spectral purity of the signals. The divide-by-32 divider is used to get a lower frequency signal, which can be measured by the frequency counter embedded in the multifunction data-acquisition board.

III. HEMT Transistor Characterization and Parameters Extraction

In this section, we report the characterization of the stand-alone HEMT transistor shown in Fig. 1(a) (finger width: 15 μm, the number of fingers: 4, total width: 60 μm, source–drain distance: 2.5 μm, and gate length: 70 nm) in the temperature range from 1.4 to 300 K. A static magnetic field from 0 to 8 T is used to measure its geometrical magnetoresistance (i.e., only due to the Lorentz force) and its Shubnikov–de-Haas (SdH) resistance oscillations. The former is a standard approach, which allows to extract the effective drain–source mobility as an independent variable, whereas the latter leads to the extraction of the charge carriers density as an independent parameter from mobility (i.e., a necessary condition to cross-check the obtained results with the mobility and the conductivity measurements). Indeed, as we will show in the following, the values of these parameters extracted from magnetoresistance measurements are in good agreement with those obtained from the dc characterization of the transistor at zero magnetic field.

Fig. 2 shows the dc characterization (I_{DS}–V_{DS} curves for different V_{GS} values) from 1.4 to 300 K of the HEMT transistor, as shown in Fig. 1(a). V_{DS} is swept from 0 to 1 V, whereas V_{GS} spans from -0.4 to 0 V. For a given bias condition (V_{GS} and V_{DS}), the drain current I_{DS} is almost constant from 1.4 to 30 K and increases from 30 to 300 K. The kink effect with hysteresis [52] is visible below 10 K.

According to the level 1 Shichman–Hodges model [53]–[55], we extract the threshold voltage V_{th}, the intrinsic β, and the channel length modulation factor λ from the dc characterization at temperatures from 1.4 to 300 K, as shown in Fig. 2. The extraction of these parameters aims at extending the applicability of the models provided by the foundry down to deep cryogenic conditions. In order to extract V_{th}, we plot the $I_{DS} - V_{GS}$ curves from the data shown in the $I_{DS} - V_{DS}$ characterization, and we identify the tangent line with the maximum slope for $V_{DS} = 10$ mV. The latter intercepts the V_{GS} axis at the point which corresponds to the threshold voltage V_{th} [56]. The value of β is directly extracted from the source–drain resistance $R_{DS} = V_{DS}/I_{DS}$ when the transistor is polarized in the triode region ($V_{DS} \ll V_{GS} - V_{th}$), i.e., $\beta = 1/(R_{DS}(V_{GS} - V_{th}))$. The channel length modulation factor is extracted in deep saturation ($V_{DS} \gg V_{GS} - V_{th}$) and can be written as $\lambda = 2\Delta I_{DS}/(\Delta V_{DS}\beta(V_{GS} - V_{th})^2)$. From the experimental data, we obtain $V_{th} = -0.22$ V at 300 K and $V_{th} = -0.07$ V at 1.4 K. A similar behavior has been already reported in the literature for both CMOS and HEMT transistors at low temperature [57]–[59]. The extracted value of β is 0.28 A/V^2 at 300 K and 0.47 A/V^2 at 1.4 K. λ is approximately 10 V^{-1} at 300 K and 2 V^{-1} at 1.4 K.

Fig. 3(a) shows the measured HEMT transistor source–drain resistance R_{DS} as a function of the static magnetic field
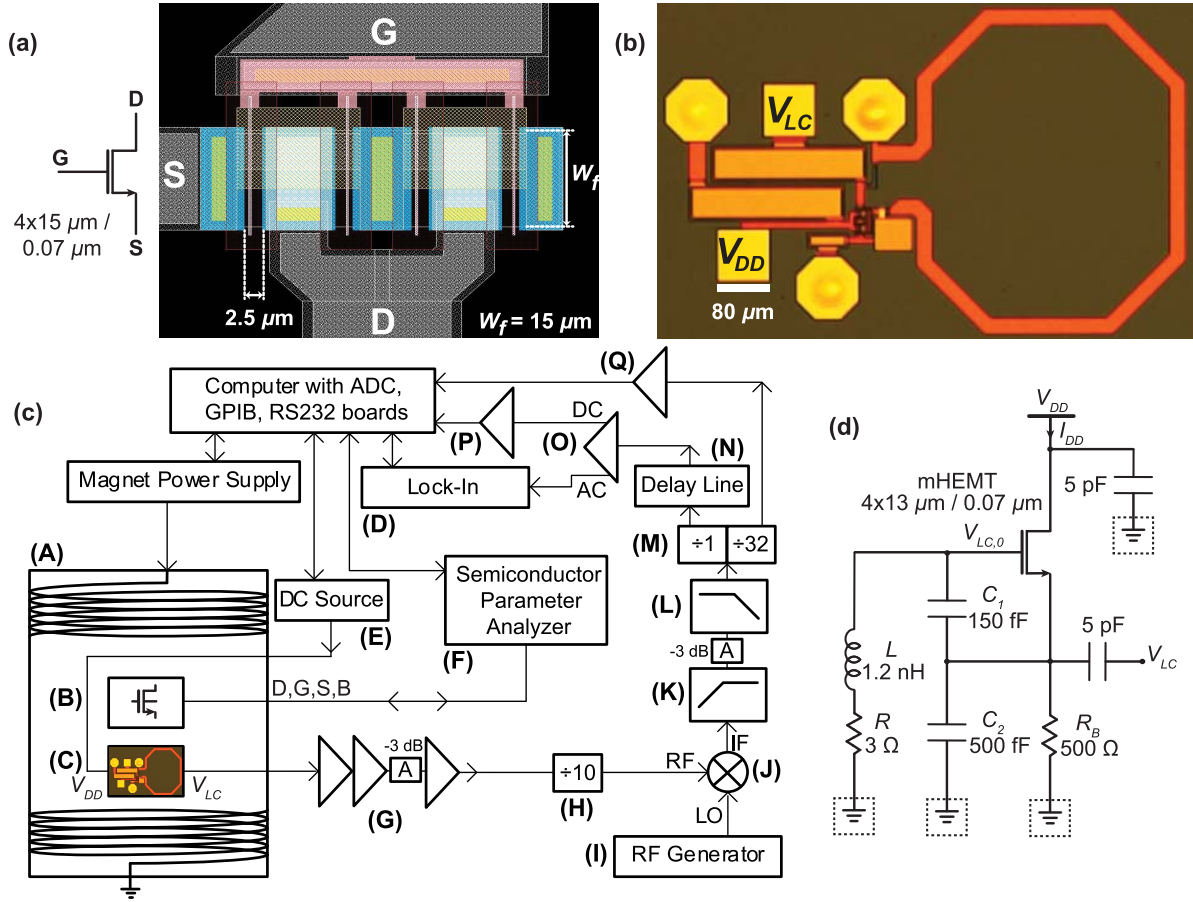
Fig. 1. Schematics and photograph of the realized HEMT structures. (a) Symbol and layout of the stand-alone HEMT transistor of four fingers. The finger width W_f is 15 μm, the source–drain distance is 2.5 μm, and the gate length is 70 nm. (b) Photograph of the HEMT LC Colpitts oscillator. The oscillator chip size is 0.8 mm $\times$ 0.5 mm, whereas the coil size is 400 μm $\times$ 480 μm. The chip has a thickness of 100 μm. Three metalized holes (vias) having a diameter of 100 μm and visible as yellow hexagons in the photograph connect the top side of the chip to its bottom side. The bottom side of the chip is covered with a 3.5 μm-thick layer of Au acting as a ground plane. The bias and output bonding pads are yellow squares having a side of 80 μm. (c) Block diagram of the complete setup for the characterization of the stand-alone transistor and of the LC oscillator. (A) Superconducting magnet with variable temperature insert (1.4–300 K, 0–9.4 T, Cryogenic Ltd.). (B) Stand-alone HEMT transistor. (C) HEMT LC Colpitts oscillator. (D) Lock-in amplifier (EG&G 7265 up to 250 kHz, Stanford Research Systems SR844 up to 10 MHz). (E) DC power supply (Keithley 2400). (F) Semiconductor parameter analyzer (HP 4156A). (G) RF amplification stage composed of three RF amplifiers (Analog Devices, HMC-C001) and a 3-dB attenuator. (H) Frequency divider (Analog Devices, HMC-C040). (I) RF generator (R&S, SMR-20). (J) Mixer (Mini-Circuits ZFM-2000+). (K) 100-MHz high-pass filter (Crystek CHPFL-0100). (L) 300-MHz low-pass filter (Crystek CLPFL-0300). (M) Frequency divider (Valon Technology 3010). (N) Homemade DLD [50], [51] (200-MHz central frequency, 1-MHz detection range, and 5-MHz FM bandwidth). (O) Amplifier (Stanford Research Systems SR560) (not used for phase noise characterization above 250 kHz). (P) Amplifier (EG&G 5113). (Q) Amplifier (NF 5305). (d) Detailed schematic of the HEMT LC Colpitts oscillator. It consists of an inductor L with a series resistance R, forming a resonator with the capacitors C_1 and C_2, a single HEMT transistor, and a bias resistor R_B. The transistor has a gate length of 0.07 μm and a total gate width of 52 μm (four fingers, each 13 μm wide). The oscillator is power-supplied from a dc source (current: I_{DD}, voltage: V_{DD}).

B applied in the direction orthogonal to the 2DEG plane. If the magnetic field is applied parallel to the 2DEG plane, a much smaller change of R_{DS} is measured (about 2.5% from 0 to 8 T). This indicates that the observed resistance variation is due to the geometrical magnetoresistance (i.e., the Hall effect). The measurement of the geometrical magnetoresistance is widely used as a method for the extraction of the charge carrier mobility [60]–[62]. In order to model the device and extract the carrier mobility, we used the equivalent circuit described in [63]. Such a model, which can be implemented in any electronic-design-automation (EDA) simulator, consists of a network of identical magnetic-field-dependent resistors and current-controlled-current sources. The extracted mobility value is 0.65 m^2/Vs at 300 K and 1.2 m^2/Vs at 1.4 K. This result is coherent with the extracted

β value, which also increases by a factor of two at low temperature.

The drain–source resistance R_{DS} is approximately 8 Ω at zero field, regardless of the temperature [see Fig. 3(a)]. Since the conductivity is defined as $\sigma = en\mu$ (where e is the elementary charge, n is the density of carriers, and μ is the mobility) and the resistance is $R_{DS} = L_{SD}/W\sigma$ (where $L_{SD} = 2.5$ μm and $W = 60$ μm are the transistor source–drain distance and width, respectively), we estimate a density of carriers of about 5×10^{16} m^{-2}. In order to cross-check such a result, we measured the periodicity of the SdH oscillations [60], [64]. In our case, the SdH oscillations are the oscillations of R_{DS} as a function of the applied magnetic field, which we measured at 1.4 K. As shown in Fig. 3(d)–(f), we observe SdH oscillations for magnetic
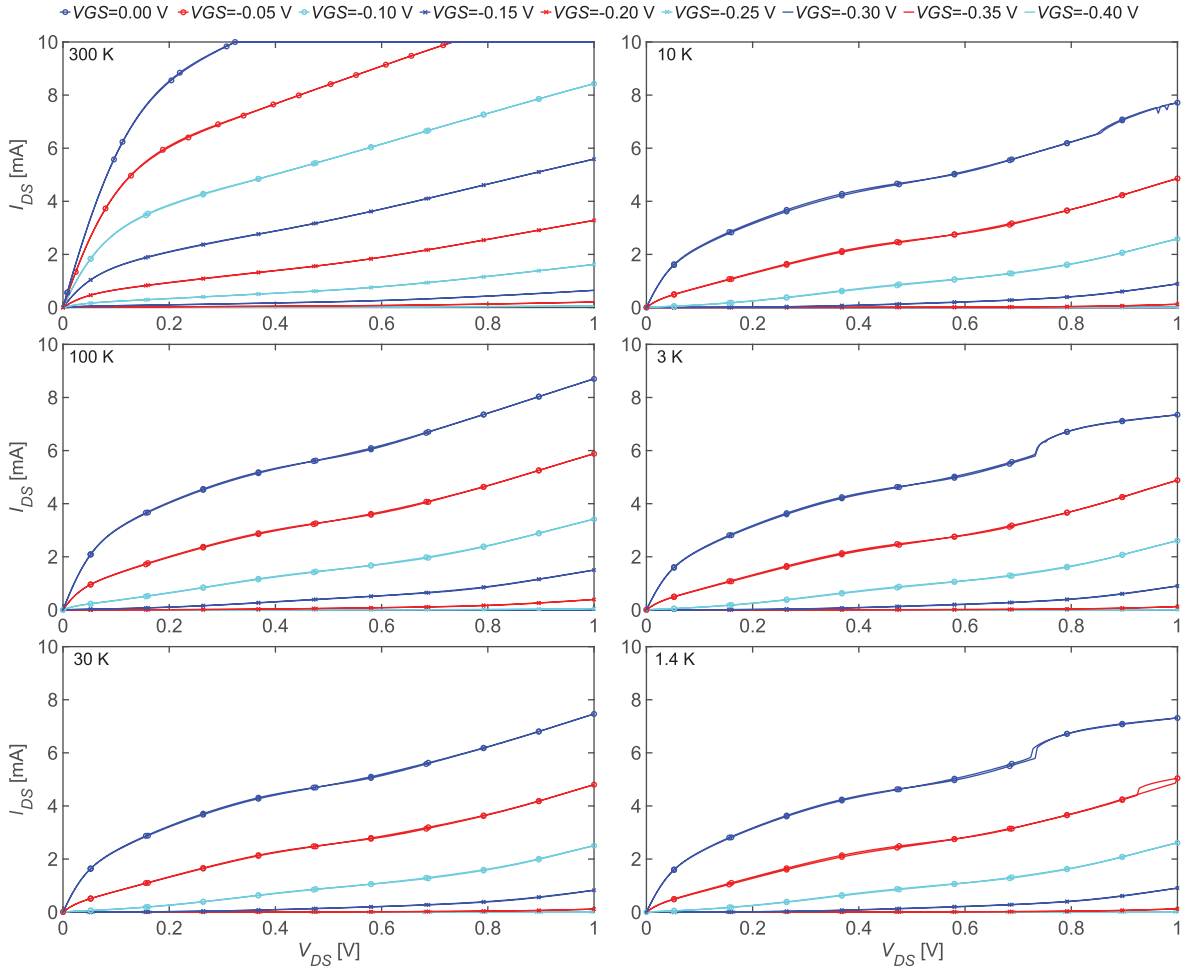
Fig. 2. Characterization of the stand-alone HEMT transistor. The dc drain–source current I_{DS} is shown as a function of the drain–source voltage V_{DS} for different gate–source voltages V_{GS} from 1.4 to 300 K. The transistor is composed of four fingers (each having a width of 15 μm for a total width of 60 μm), and it has a source–drain distance of 2.5 μm and a gate length of 70 nm [see Fig. 1(a)].

field values above 5 T, at 1.4 K, and for V_{DS} values of 50 mV (i.e., at an electric field of 2×10^{-2} V/μm) and 4 mV (i.e., at an electric field of 16×10^{-4} V/μm). The periodicity is more evident at the lower electric field. Performing the fast Fourier transform (FFT) of $d^2 R_{DS}/dB^2$, plotted as a function of $1/B$, allows to extract the oscillation frequency. As shown in Fig. 3(e) and (f) there is a main frequency component at about 70 T^{-1}. According to [64], we compute the density of carriers as $n \cong (2e/h/\Delta(1/B)) \cong 3.5 \times 10^{16}$ m^{-2}, where h is the Planck constant and $\Delta(1/B)$ is the periodicity of the SdH oscillations. This value for the density of carriers is in good agreement with the above-estimated one, obtained from the measurements of the resistance (i.e., 5×10^{16} m^{-2}). The SdH oscillations reported in this paper are significantly smaller than those reported in previous publications [64]–[68]. This might be due to the larger electric fields applied to the HEMT transistor with respect to those usually reported in the literature. In [65]–[67], it is shown that the SdH oscillations are reduced when the applied electric field is increased. In our measurements, the minimum practically applicable electric field is approximately 10^{-3} V/μm. Indeed, in our experimental setup, at lower V_{DS} and, hence, at lower electric fields,

the magnetoresistance measurements are too noisy to allow for the extraction of the charge carrier density.

IV. HEMT LC COLPITTS OSCILLATOR CHARACTERIZATION

In this section, we report the results of measurements performed on the LC Colpitts oscillator, as shown in Fig. 1(d). In particular, we investigated the start-up condition as a function of temperature and the oscillation frequency as a function of the supply voltage.

In Table I, we report the key features of the realized system. In particular, the HEMT LC Colpitts oscillator shows a minimum (i.e., start-up) power consumption of 90 μW at 300 K ($V_{DD} = 220$ mV and $I_{DD} = 400$ μA) and 4 μW below 30 K ($V_{DD} = 40$ mV and $I_{DD} = 110$ μA). Close to the start-up, the power efficiency is in the order of 5%, and hence, the minimum power consumption is essentially identical to the minimum power dissipated by the oscillator. The aforementioned power consumption is, to the best of our knowledge, the lowest reported to date for an LC oscillator working in the same frequency range.
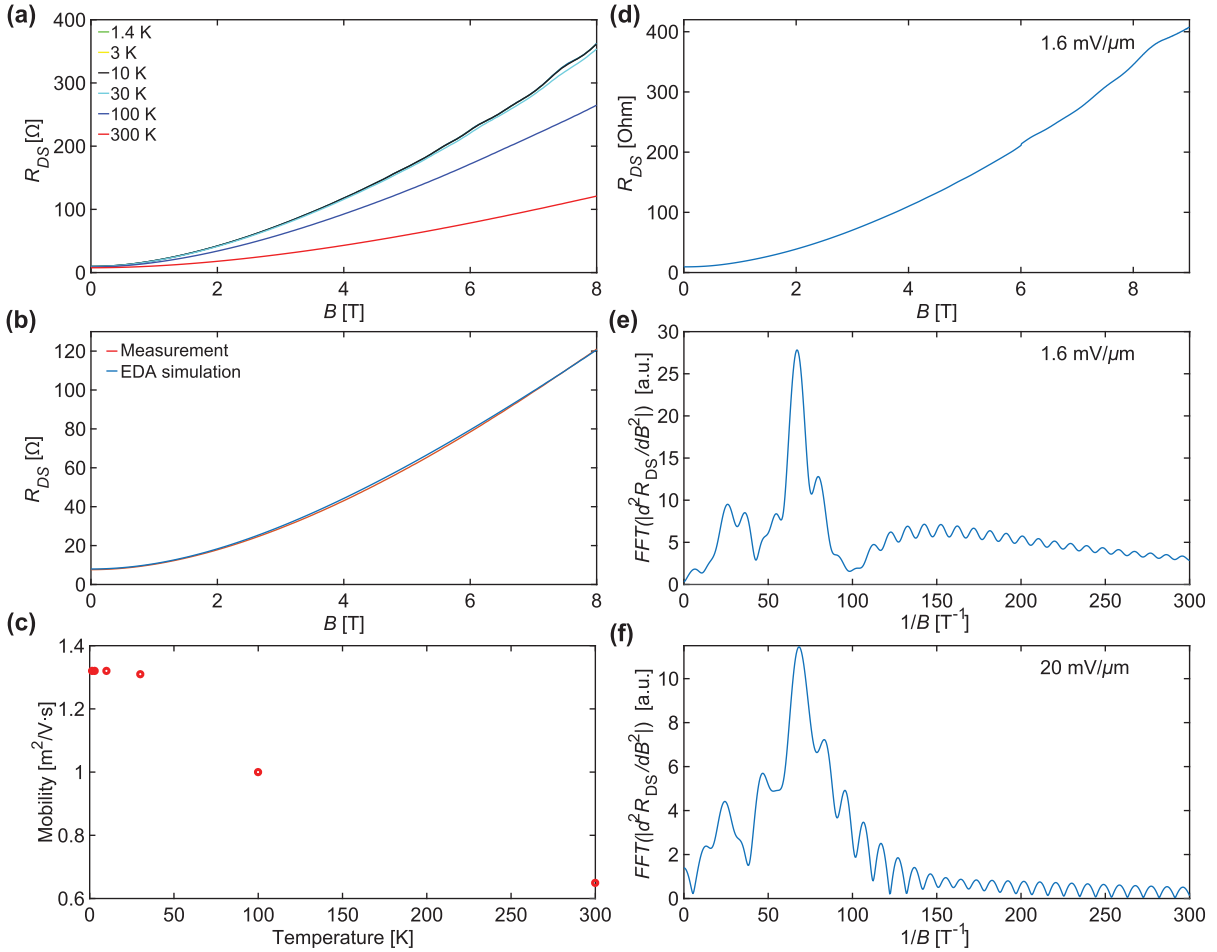
Fig. 3. Magnetoresistance, mobility, and SdH oscillations of the stand-alone HEMT transistor. (a) Source–drain resistance R_{DS} as a function of the applied static magnetic field (from 0 to 8 T, orthogonal to the 2DEG) from 1.4 to 300 K. The curves from 1.4 to 30 K overlap. The transistor is biased with $V_{GS} = 0.2$ V and $V_{DS} = 50$ mV. (b) Comparison between the measured and the EDA simulated R_{DS} values as a function of the applied static magnetic field (see the details of the EDA simulation in the text). (c) Extracted effective carrier mobility as a function of the temperature. The magnitude of carrier mobility has no significant variation from 1.4 to 30 K and decreases by a factor of two from 30 to 300 K. (d) Source–drain resistance R_{DS} as a function of the magnetic field for $V_{GS} = 0.2$ V and $V_{DS} = 4$ mV (i.e., electric field of 16×10^{-4} V/μm). Small SdH oscillations are visible above 5 T. (e) FFT of $d^2 R_{DS}/dB^2$ plotted as a function of $1/B$. The source–drain resistance R_{DS} is the one plotted in (d). The main periodicity of the SdH oscillations is at 70 T^{-1}. (f) FFT of $d^2 R_{DS}/dB^2$ plotted as a function of $1/B$. The source–drain resistance R_{DS} is measured at $V_{DS} = 50$ mV (i.e., electric field of 2×10^{-2} V/μm). The periodicity is the same as in (e), but with a much smaller amplitude, presumably due to the larger electric field applied.

As reported earlier, the realized oscillator shows a lower power consumption at cryogenic temperature than at 300 K. This is presumably due to the following reasons. The decrease of the threshold voltage from -0.22 to -0.07 V allows to reduce V_{DD} to obtain the same overdrive voltage $V_{GS} - V_{th}$. The decrease of the coil resistance results in a lower g_m^{min} value (and, hence, in a lower minimum V_{DD}), whereas the increase of β results in a larger g_m value (see the Appendix).

It is worthy to note that the topology of the LC oscillator reported here [see Fig. 1(d)] is optimized for low parasitics and area occupation. Only a few components are required, and the bias point of the oscillator is set through a single supply voltage V_{DD} (i.e., no extra pads are required). However, as we will discuss in detail in the Appendix, this architecture can be further optimized to achieve even lower power consumption. Indeed, the bias resistance R_B is large with respect to R_{DS} and R, so the majority of the power provided by the generator

is dissipated across R_B, which has the only aim to produce a suitable V_{GS} bias. In addition, since the threshold voltage of the transistor varies as a function of the temperature, it would be beneficial to optimize V_{GS} independently (e.g., by adjusting the gate voltage), whereas in the proposed architecture, it results intrinsically defined by V_{DD}. As discussed in the Appendix, a slightly more complex topology, where R_B is replaced by an inductor L_B and the gate–source voltage V_{GS} is freely adjustable, should allow to obtain a further significant reduction of the start-up power consumption.

In Fig. 4(a), we report the experimentally measured phase noise at 1.4, 100, and 300 K as well as the noise of the measuring apparatus, which is lower than the oscillator noise (6 dB in the worst case, i.e., at low temperature and large-frequency offset from the carrier). The voltage noise spectral density at the output of the DLD is measured using a lock-in amplifier. The phase noise spectral density is computed from the

TABLE I
KEY FEATURES OF THE HEMT OSCILLATOR

Oscillation frequency [GHz] @ 300 K	11.2
Oscillation frequency [GHz] @ 1.4 K	11.3
Coil size [μm]	400 x 480
Approx. coil resistance [Ω] @ 11.2 GHz, 300 K	3
Approx. coil inductance [nH] @ 11.2 GHz, 300 K	1.2
Approx. coil Q-factor @ 11.2 GHz, 300 K	27
$I_{DD}^{\min}$ [μA]	410
$V_{DD}^{\min}$ [mV]	220
$P^{\min}$ [μW] @300 K	90
$I_{DD}^{\min}$ [μA]	110
$V_{DD}^{\min}$ [mV]	40
$P^{\min}$ [μW] @1.4 K	4
Figure-of-merit (FOM) [dBc/Hz]* @ 1 MHz frequency offset from the carrier, 300 K	188
Figure-of-merit (FOM) [dBc/Hz] @ 1 MHz frequency offset from the carrier, 1.4 K	217

* The oscillator figure-of-merit (FOM) is computed as $(20 \log(f_{LC}/f_{OS}) - L(f_{OS}) - 10 \log(P^{\min}))$, where $\mathcal{L}(f_{OS})$ is the phase noise (in dBc/Hz) at the frequency offset f_{OS} (in Hz), f_{LC} is the oscillator working frequency (in Hz), and $P^{\min}$ is the minimum power consumption (in mW) [42], [69].
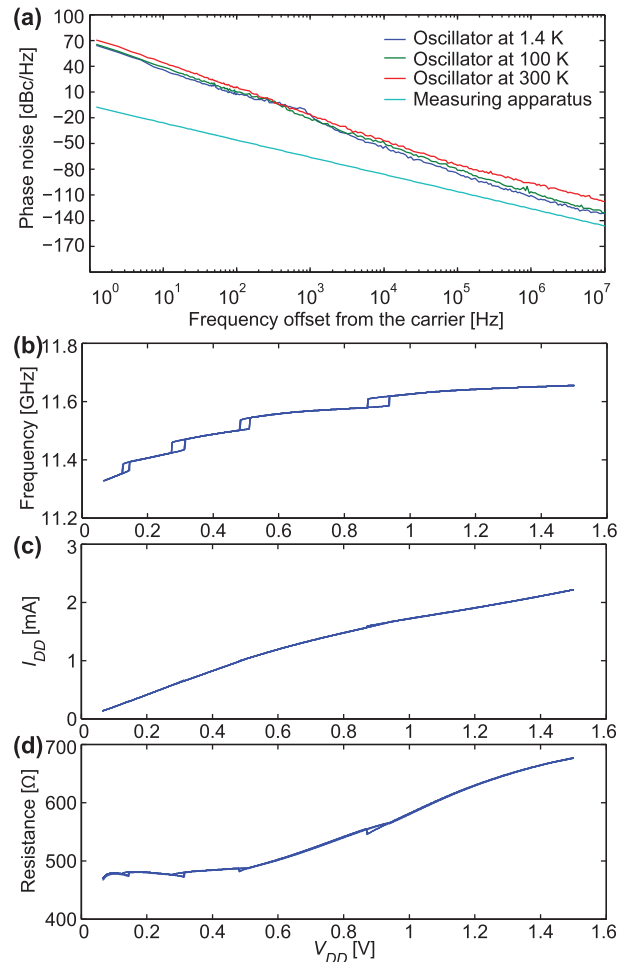

Fig. 4. Characterization of the HEMT *LC* Colpitts oscillator. (a) Measured phase noise spectral density of the HEMT *LC* Colpitts oscillator at 1.4, 100, and 300 K, at the minimum bias voltage for stable oscillations. At all temperatures, the minimum noise is measured at the minimum bias. The phase noise of the measuring apparatus [see Fig.1(c)] is also reported. Plots of (b) working frequency, (c) bias current, and (d) resistance of the oscillator as a function of its bias voltage. The latter is swept up and down for ten times from 0.065 to 1.5 V. Jumps and hysteresis phenomena are clearly visible and reproducible for both frequency and resistance. The frequency jumps are approximately equal to 35 MHz for all transitions.

measured voltage noise spectral density and the frequency-to-voltage conversion factor of the DLD. The measured phase noise floor (i.e., the phase noise at offset frequencies above the $1/f$ noise corner frequency, which is of about 1 MHz for our oscillator) corresponds, within a factor of two, to the thermal phase noise originating from the coil resistance given by $10 \log(kTR(f_{LC}/f_{OS}V_{LC,0})^2)$, where $V_{LC,0}$ is the oscillation amplitude (in V), R is the coil resistance at the operating frequency (in Ω), and f_{OS} is the frequency offset from the carrier (in Hz) [70].

Fig. 4 reports also the measurements of the oscillator operating frequency, dc current I_{DD}, and resistance R_{DD} as a function of the bias voltage V_{DD} at 1.4 K. The bias voltage is swept up and down from 65 mV (i.e., close to the start-up condition of 40 mV) to 1.5 V. As shown in Fig. 4(b)–(d), the oscillation frequency (as well as the current and the resistance) shows discontinuities as a function of the bias voltage. The frequency jumps are of approximately 35 MHz. The position of the transitions and their amplitude change as a function of the applied magnetic field and the temperature. The density of transitions increases close to the start-up bias point. The transitions get smoother above 30 K and disappear above 70 K. In contrast to the CMOS-based oscillators [71], no random telegraph signals (RTSs) are present. We also observed that it is possible to induce frequency jumps at fixed bias voltage V_{DD} by changing the applied magnetic field (both parallel and orthogonal to the 2DEG). We performed the previous characterization on four nominally identical oscillators, obtaining similar although not identical results. The number of sharp transitions, for a bias V_{DD} in the range from 65 mV to 1.5 V,

changes from three to five and their amplitude from 20 to 200 MHz. As for the CMOS oscillators reported before [71], the physical origin of the measured frequency jumps is still unclear to us.

V. CONCLUSION AND OUTLOOK

In this paper, we reported about the design and characterization of a low-power HEMT *LC* Colpitts oscillator operating at 11 GHz. In particular, we investigated the minimum power consumption to sustain stable oscillations and the phase noise in the temperature range from 1.4 to 300 K. The realized oscillator shows the lowest power consumption reported in the literature for an *LC* oscillator working in this frequency range. A comparison with the state of the art is shown in Table II. Our oscillator shows comparable FOM at 300 K and the best FOM at low temperatures. To sum up the key points, we manage to get the reported low-power consumption thanks to: 1) the

TABLE II
OSCILLATOR STATE-OF-THE-ART COMPARISON

	Temperature [K]	Technology	Frequency [GHz]	Power Consumption [mW]	Phase Noise @ 1 MHz frequency offset [dBc/Hz]	FOM
[72]	300	CMOS 180 nm	15	3	-109.3	188
[73]	300	CMOS 180 nm	10.3 - 11.1	15.1	-115.9	184
[74]	300	CMOS 130 nm	10	4.2	-110 , -107	183
[75]	300	SiGe 130 nm	6.5 - 15.1	19	-110	177
[32]	300	GaN HEMT 250 nm	4.7	2.7	-121.7	190
[23]	300	CMOS 65 nm	40	0.28	-98 , -70[*]	196 , 178[*]
[26]	300	CMOS 65 nm	57.4	0.13	-[**]	197[**]
[13]	300	CMOS 40 nm	6.3	4 , 13[***]	-125	194 , 189[***]
[13]	4.2	CMOS 40 nm	6.7	7 , 18[***]	-120	192 , 188[***]
[33]	300	SiGe 130 nm	29.8	37	-115	188
[33]	4	SiGe 130 nm	30.8	47	-112	185
This work	300	HEMT 70 nm	11.2	0.09	-97	188
This work	1.4	HEMT 70 nm	11.3	0.004	-112	217

[*] This is a self-oscillating mixer, so the phase noise depends on the injected power. We selected the best and worst cases.
[**] Phase noise measurement is not shown in this paper. Only FOM is shown in a graph.
[***] Power consumption depends on the current setting. We selected the best and worst cases.

high mobility of the HEMT transistor (with respect to standard CMOS); 2) the reduced threshold voltage at low temperature; and 3) a design optimization aimed at this specific goal. We also report on the results of simulations, which indicate that the power consumption can be further reduced by using a slightly different topology. A reduced power consumption is of crucial importance for measurements at low temperatures. At temperatures below 1 K, the limited effective cooling power of ^{3}He and ^{3}He^{4}He dilution refrigerator systems demands for devices operating with power in the μW range and below, especially if the power has to be dissipated in a very small volume, such as the channel of an HEMT transistor suitable to operate at microwave frequencies above 10 GHz. Particularly interesting is the possibility to reach the condition $\hbar\omega > kT$, where we expect to observe the reduction of the thermal noise and, possibly, also an observable quantum behavior related to the oscillator energy quantization coupled with the nonlinear behavior of the transistor. LC resonators operating in the condition $\hbar\omega > k_B T$ are, in principle, possible candidates to show a macroscopic quantum behavior. However, due to their linear behavior, the energy (frequency) quantization is not observable [76]. The LC oscillators described in this paper show a relatively strong dependence of the oscillator frequency on the applied bias voltage, which makes these oscillators highly anharmonic. This condition might be sufficient to observe interesting unexplored phenomena, which might include their behavior as artificial atoms, as reported before for superconducting quantum circuits (SQCs) based on Josephson junctions [76], [77].

APPENDIX

The HEMT LC oscillator topology shown in Fig. 1(a) and described in Section III has a limited versatility since the dc gate voltage is tied to ground and the dc source voltage is intrinsically determined by the voltage drop across R_B. As a consequence, V_{GS} cannot be independently adjusted with respect to V_{DS}.

Fig. 5(b) shows an improved topology, which would allow: 1) to decouple V_{GS} from V_{DD} and 2) to avoid the power dissipated across the bias resistor R_B. In this more versatile topology, V_{GS} can be independently adjusted with respect to V_{DS}, and the series resistance of the bias inductor R_{LB} is much smaller than the bias resistor R_B used in the topology, as shown in Fig. 5(a). As a consequence, we expect that this topology should allow to reduce the oscillator power consumption at the start-up (i.e., the minimum power consumption required by the LC Colpitts oscillator to produce stable oscillations).

In this topology, the bias inductance L_B is chosen sufficiently large, such that $\omega_{LC}L_B \gg 1/\omega_{LC}C_2$. Hence, the oscillator frequency is, also for this topology, given by $\omega_{LC} = 1/\sqrt{LC}$, where $C = C_1 C_2/(C_1 + C_2)$ is the effective capacitance. In order to compute the start-up condition for this oscillator, we can use the small-signal ac model shown in Fig. 5(c), which is valid regardless of: 1) the type of the FET transistor (MOSFET or HEMT) and 2) its polarization (triode or saturation). The transistor is modeled by its transconductance ($g_m = \partial I_{DS}/\partial V_{GS}$) and its output resistance ($r_O = \partial V_{DS}/\partial I_{DS}$). Stable oscillations are obtained when the negative resistance created by the transistor compensates for the overall losses in the system. In order to analyze the circuit, we separate the tank inductor from the energy restoring system at the level of the dashed line [see Fig. 5(c)]. Since the reactance of the compensation system affects only the operating frequency, we consider only the resistive part of the overall impedance. The condition required for the total resistance to be zero (i.e., for the compensation of the losses) is

$$R = -g_m \frac{C_2}{C_1} \frac{r_O^2}{\omega_{LC}^2 r_O^2 C_2^2 + 1} + \frac{r_O}{1 + \omega_{LC}^2 r_O^2 C_2^2}. \qquad (1)$$

Consequently, the minimum transconductance for stable oscillation is

$$g_m^{\min} = \left(R + \frac{r_O}{1 + \omega_{LC}^2 r_O^2 C_2^2} \right) \frac{C_1}{C_2} \frac{1 + \omega_{LC}^2 r_O^2 C_2^2}{r_O^2}. \qquad (2)$$
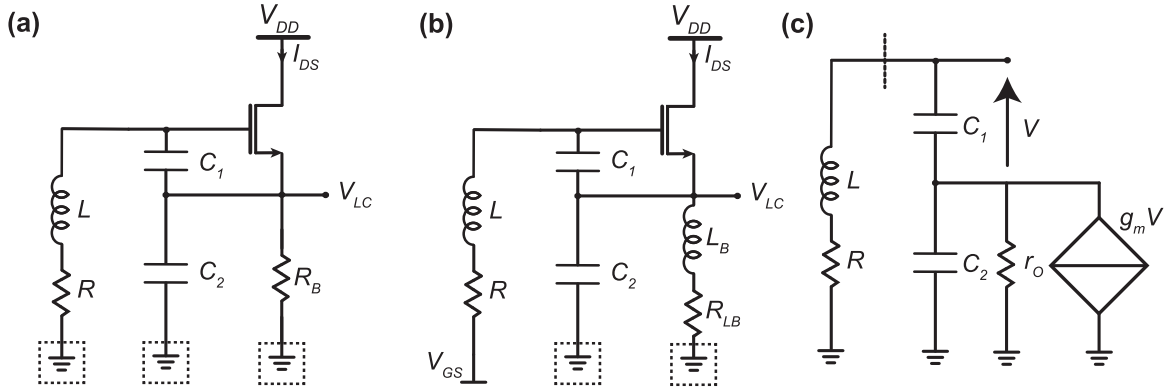
Fig. 5. Schematic of the HEMT *LC* Colpitts oscillators. (a) Schematic of the HEMT *LC* Colpitts oscillator designed and characterized in this paper. It consists of a single HEMT transistor, a tank inductor (inductance L and series resistance R), two tank capacitors (C_1 and C_2), and a bias resistor (R_B). The value of the components used in simulations at 300 and 1.4 K is: $L = 1.15$ nH, $R = 3$ Ω at 300 K (1 Ω at 1.4 K), $C_1 = 150$ fF, $C_2 = 500$ fF, and $R_B = 500$ Ω (350 Ω at 1.4 K). (b) Schematic of the low-power optimized HEMT *LC* Colpitts oscillator. It consists of a single HEMT transistor, a tank inductor (inductance L and series resistance R), two tank capacitors (C_1 and C_2), and a bias inductor (inductance L_B and series resistance R_{LB}). The value of the components used in simulations at 300 and 1.4 K are: $L = 1.15$ nH, $R = 3$ Ω (1 Ω at 1.4 K), $C_1 = 150$ fF, $C_2 = 500$ fF, $L_B = 15$ nH, and $R_{LB} = 3$ Ω (1 Ω at 1.4 K). The oscillator is powered with a dc source (voltage: V_{DD}, current: I_{DS}). (c) Detailed schematic of the ac small-signal model of the low-power optimized HEMT *LC* Colpitts oscillator shown in (b). The HEMT transistor is modeled by voltage-controlled-current source and an r_O resistor.

According to a level 1 model, the transistor is characterized by three parameters (V_{th}, β, and λ), and its transconductance in the triode and saturation regions is

$$g_m^{tri} = \frac{2I_{DS}}{2(V_{GS} - V_{th}) - V_{DS}} \qquad g_m^{sat} = \frac{2I_{DS}}{V_{GS} - V_{th}}. \qquad (3)$$

Numerical computations, based on the previous equations implemented in Mathematica (Wolfram Research, USA), reveal that the minimum power consumption $P^{min} = V_{DS}^{min} I_{DS}^{min}$ is weakly dependent on r_0, which can be assumed to be ∞ (i.e., $\lambda = 0$). Moreover, since the gate–source voltage V_{GS} is adjustable, we can consider the overdrive voltage ($V_{GS} - V_{th}$) as a single variable. The numerical computations also show that the optimal bias for minimum power consumption is at the transition between the saturation and quadratic regions, where $V_{DS} \cong (V_{GS} - V_{th})$ and $I_{DS} \cong (\beta/2)(V_{GS} - V_{th})^2$. Introducing these assumptions, we obtain the following simplified equations:

$$\begin{cases} I_{DS}^{min} \cong \dfrac{(g_m^{min})^2}{2\beta} \\ V_{DS}^{min} \cong V_{GS}^{min} - V_{th} = \dfrac{g_m^{min}}{\beta} \\ g_m^{min} \cong RC_1C_2\omega_{LC}^2 \end{cases} \qquad (4)$$

and, hence, the minimum power consumption for an *LC* Colpitts oscillator having the topology shown in Fig. 5(b) is

$$P^{min} = \frac{(g_m^{min})^3}{2\beta^2} = \frac{\left(RC_1C_2\omega_{LC}^2\right)^3}{2\beta^2} = \frac{(R(C_1 + C_2)/L)^3}{2\beta^2}. \qquad (5)$$

As intuitively expected, the power consumption is reduced for a smaller coil resistance R and for a larger β value. From (5), the use of a transistor with a larger width (and hence with a larger β value) would allow to obtain a lower power consumption. However, a larger transistor would have larger parasitic capacitances, de facto limiting the maximum achievable oscillation frequency.

For an oscillator based on the topology optimized for power consumption [see Fig. 5(b)] and having the same parameters as those reported in this paper [see Fig. 5(a)] (i.e., $L = 1.15$ nH, $R = 3$ Ω, $C_1 = 150$ fF, $C_2 = 500$ fF, $\beta = 0.28$ A/V^2, and $\omega_{LC} = 2\pi \times 11$ GHz), the theoretical minimum power consumption expected from (5) would be of about 50 nW. It is important to note that a moderate error in the estimation of the parameters in (5) would result in a very large variation of the power consumption. For example, the combined effect of a two times larger R value with a two times smaller β value would result in a minimum power consumption increase by a factor of 32, thus resulting in a power consumption of about 2 μW.

In order to test the validity of the simple analytical result given by (5) for the oscillator topology in Fig. 5(b), we performed simulations with different transistor models. The results of these simulations are reported in Table I, which also includes simulations and experimental results obtained with the oscillator topology shown in Fig. 5(a) (i.e., the one designed, experimentally characterized, and reported in this paper). The simulated results are obtained, respectively, using a level 1 model [54], [55], a level 1 model with parasitics, and the foundry model. The level 1 parameters are extracted from the stand-alone HEMT transistor experimental characterization reported in Section II. The parasitics of the transistor are obtained from the foundry model. The approximate values for the capacitances between the transistor terminals (C_{GS}, C_{DS}, and C_{gd}) are of 15 fF, the capacitances terminals to ground (C_d and C_s) are of 25 fF, the series resistances of the terminals (R_g, R_s, and R_d) are of 3–5 Ω, and the series inductances of the terminals (L_g, L_d, and L_s) are of 3–5 pH.

The topology in Fig. 5(a) has a start-up condition where the minimum supply voltage V_{DD}^{min} is approximately given by V_{th} and the minimum current I_{DS}^{min} is approximately given by $V_{DD}^{min}/R_B \cong V_{th}/R_B$. Hence, the minimum power consumption is $P^{min} = V_{DD}^{min}I_{DS}^{min} \cong V_{th}^2/R_B$. For this topology, an accurate transistor modeling is not critical for the power consumption.

TABLE III
OSCILLATOR START-UP CONDITION

Oscillator type[*]		Fig.5(a)	Fig.5(b)
$V_{DD}^{\min}$ [mV] @300 K	experimental	220	-
	foundry	255	34
	level 1	188	7
	level 1 with parasitics	191	19
$I_{DS}^{\min}$ [μA] @300 K	experimental	410	-
	foundry	420	450
	level 1	500	6
	level 1 with parasitics	450	94
$P^{\min}$ [μW] @300 K	experimental	90	-
	foundry	107	16
	level 1	94	0.05
	level 1 with parasitics	85	2
$V_{DD}^{\min}$ [mV] @1.4 K	experimental	40	-
	level 1	51	2
	level 1 with parasitics	57	6
$I_{DS}^{\min}$ [μA] @1.4 K	experimental	110	-
	level 1	130	2
	level 1 with parasitics	150	20
$P^{\min}$ [μW] @1.4 K	experimental	4	-
	level 1	7	0.004
	level 1 with parasitics	8	0.120

[*] Experimental and simulated start-up conditions for the two *LC* Colpitts oscillator topologies shown in Fig. 5, both implemented using an HEMT technology (D007IH mHEMT 70 nm, OM-MIC, France). The simulations are performed using the level 1 model of the HEMT transistor, with parameter values extracted from the standalone HEMT transistor characterization reported in Section III, and the foundry model supplied by OMMIC. The simulations are performed using Quite Universal Circuit Simulator (QUCS) for level 1 model and Advanced Design System (ADS) (Keysight, USA) for the foundry model. The value of the level 1 parameters at 300 K are: $V_{th} = -220$ mV, $K_P = 3.4 \times 10^{-3}$ A/V^2, $W = 52$ μm, $L = 0.07$ μm, $\lambda = 10$ V^{-1}, $\gamma = 0$. The values of the parameters at 1.4 K are: $V_{th} = -70$ mV, $K_P = 6.5 \times 10^{-3}$ A/V^2, $W = 52$ μm, $L = 0.07$ μm, $\lambda = 2$ V^{-1}, $\gamma = 0$. K_P is obtained from the extracted value of β as $K_P = \beta(L/W)$.

Hence, it is not surprising that the simulations performed using a level 1 model for the transistor can predict quite accurately the minimum power consumption required for the oscillation. As shown in Table III, for this oscillator topology, the experimentally obtained minimum power consumption is in agreement, within a factor of two, with the simulations performed using the level 1 model.

For the topology sketched in Fig. 5(b), the minimum power consumption obtained from level 1 simulations is in agreement, within a few percents, with the analytical expression given in (5). However, this only means that (5) is properly derived from the basic equations of the level 1 model. If we use the model given by the foundry, the power consumption at 300 K is two orders of magnitude larger with respect to the level 1 model without parasitics. If the above-described parasitics are introduced in the level 1 model, the agreement improves significantly, but the difference in power consumption is still of about one order of magnitude. The causes of this large discrepancy are unclear. Despite the relatively poor modeling agreement, the simulations (and the intuitive arguments related to the biasing freedom) indicate that the oscillator topology shown in Fig. 5(b) should achieve a significantly lower power consumption with respect to the one in Fig. 5(a).

In the near future, we plan to implement and experimentally characterize this oscillator topology, with the aim of obtaining a power consumption below 1 μW at low temperature and as a means to give more robust guidelines for the modeling of ultralow-power HEMT oscillators, in particular for deep cryogenic applications.

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