Analysis on Noise Requirements of RF Front-End Circuits for Spin Qubit Readout

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Abstract — **Currently, radio frequency (RF) measurement setups for semiconductor qubits are implemented with high performance discrete devices operating at cryogenic temperatures, and the output signals are detected by room temperature instruments. This is impractical for a real quantum processor, and integrated circuits (ICs) should be designed for spin qubit readout in a practical quantum computer, to ensure system reliability and compactness. To guide the system-level IC design, we analyze in this work noise specifications of RF front-end circuits for qubit readout, mainly focusing on noise figure (NF) of the low-noise-amplifier (LNA) and phase noise (PN) of the voltage-controlled-oscillator (VCO). RF reflectometry and RF dispersive gate sensing (DGS) are two main spin qubit readout techniques, both of which should detect weak reflected signals as low as -135 dBm and distinguish <1% amplitude or phase variation, which results in high sensitivity and low noise requirements for the readout circuits, to achieve the high measurement fidelity. For the analysis, we model the RF reflectometry and RF-DGS as demodulators respectively of the on-off keying (OOK) signal and phase modulated (PM) signal from qubits. From this, we provide a first estimation of the required NF and PN for a given fidelity and readout bandwidth, as well as an insight into the relationship between phase resolution of RF-DGS and performance degradation due to PN of the VCO. We then review some state-of-the-art CMOS LNA and VCO topologies, which can be utilized in the spin qubit readout ICs to satisfy the specifications.**

Keywords — Cryo-CMOS, qubit, spin qubit, quantum computer, noise, phase noise, LNA, VCO.

Fig. 1. Two techniques for readout of semiconductor quantum dots: (a) RF reflectometry [6], (b) dispersive gate sensing [8].

I. INTRODUCTION

Quantum computing is a fast growing field addressing the constant request for increased computational power [1]. Quantum computers require classical electronics to read out and control the state of quantum bits, to perform quantum error corrected computation. In particular, solid-state quantum processors are typically realized by semiconductor or superconductor quantum devices operated at cryogenic temperatures below 0.5 K [2]. The required radio-frequency control electronics is currently implemented by discrete commercial devices wired to the quantum devices on one end and to room-temperature instruments on the other end [3].

This is however only feasible for the limited number of qubits available today and cannot be scaled to the million qubits required to realize a practical quantum computer [4]. Therefore, to address compactness and scalability, CMOS electronic circuits have been proposed to be designed and operated directly at cryogenic temperatures around 4.2 K and to realize custom integrated circuits for qubit control and readout. Such an approach can also lead to the possible integration with the quantum devices directly.

In the case of semiconductor qubits, the quantum devices are typically realized by transistor-like structures with high electrostatic gate control, s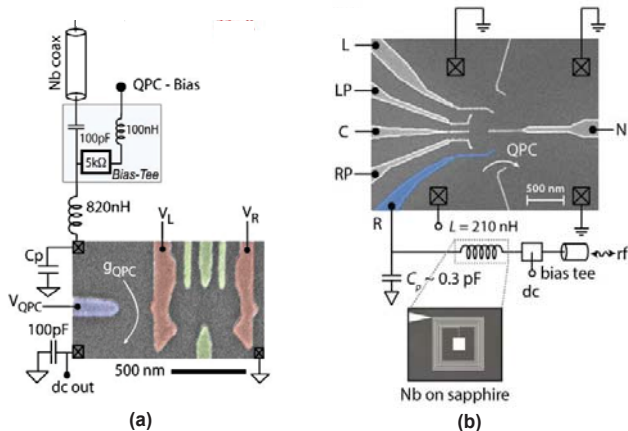o to be able to create a quantum dot capable of trapping single electrons in the transistor channel. Such quantum devices are typically read out by radio-frequency techniques employing readout front-ends very similar to RF receivers for wireless communication systems [5].

There are several functional blocks in RF readout architectures for semiconductor qubits. The LC impedance matching network (LC-IMN), the low noise amplifier (LNA), the directional coupler (used to decouple the incident RF signal from the reflected signal carrying the readout information), the LNA, the mixer and the voltage-controlled oscillator (VCO). In this paper, we will introduce the two main techniques for semiconductor qubit readout and analyze the noise specification for the readout circuits. CMOS circuit topologies for front-ends are also reviewed briefly.

II. RF READOUT TECHNIQUES AND NOISE SPECIFICATIONS

For the readout of semiconductor quantum dots, two main techniques have been developed in the context of radio-frequency probing. The first one is radio-frequency reflectometry [6][7], the second one is dispersive gate sensing [8]. In radio-frequency reflectometry, an intermediate charge sensor such as a single-electron transistor (SET) or a quantum point contact (QPC), as shown in Fig.1 (a), is used as an electrometer to sense the state of the qubit and convert it into an electrical quantity, which is then read out. For an RF-QPC, the resistance of the sensor will change according to state of the quantum device. The impedance matching network used to convert the high impedance of the QPC into 50 Ω is tuned to have optimal match at the readout frequency, but changes in the resistance of the QPC will lead to a change in the portion
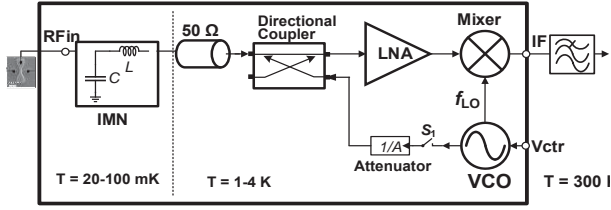
Fig. 2. Schematic diagram of a RF reflectometry readout for spin qubits.

of the radio-frequency carrier power reflected from the RF-QPC. Therefore, such a readout technique is called radio frequency reflectometry and one can relate the state of the quantum device to a change in the amplitude of the reflected signal.

More recently, direct connection to the gate of the quantum device has been proposed in order to reduce the complexity of the readout scheme as shown in Fig.1 (b) [8], providing direct in *situ* access to the quantum device without the need of an external electrometer. In such a technique, the semiconductor quantum device is addressed at its gate with an RF carrier signal and the phase of the reflected signal is read out. According to the state of the quantum device, the capacitance at the gate will be different, due to the presence in the $|1\rangle$ state of an additional quantum capacitance ΔC. This contributes to a phase shift $\Delta\varphi$ in the response of the resonant matching network, which carries the quantum information about the qubit state. For this reason, such a technique is called dispersive gate sensing.

The cryogenic readout circuit is shown in Fig. 2: the qubit readout circuit mainly consist of LC-IMN working at mK, the directional coupler (DC), low noise amplifier (LNA), mixer and voltage controlled oscillator (VCO) working at 4.2 K. Differently from the current measurement setup of semiconductor qubit for theoretical demonstration and verification [3], the demodulator and the VCO are moved to 4.2 K to simplify the electrical connection between cryogenic and room temperature circuits. The VCO generates incident RF signal (attenuated not to affect the spin state of the quantum dot) and guided down to the QPC or SET through the DC and LC-IMN. Then, the signal is reflected by the quantum devices. The reflected signal travels through the direct path of DC and is amplified by LNA. Finally, the high-frequency signals are mixed with local oscillating (LO) signals and down-convert the signals in a low-IF (or zero-IF) detection scheme, to be then digitized by an ADC.

The RF reflectometry readout of SET is shown Fig. 3 (a), and the LC resonator is used to match the output impedance of the SET to 50 Ω at the operating frequency f_0. As the spin status of the electron trapped in the quantum dot changes, the conductance of the SET or QPC (g_o) changes accordingly (by ~ 10%). The changes of the g_o then modulate the RF carrier power reflected from the matching network at resonance [3]. Here, we model it as a variable resistor.

Similarly, the gate dispersive readout is illustrated in Fig. 3(b), where the change of the loaded capacitance is modeled as a varactor, where capacitance changes according to the spin state of the electron. Here, we must clarify that for the RF reflectometry readout of SET or QPC, the detected signal is amplitude variation, while the gate dispersive readout only the phase change of the reflected signals is detected.

The reflection of a microwave signal depends on change of the load impedance, according to:
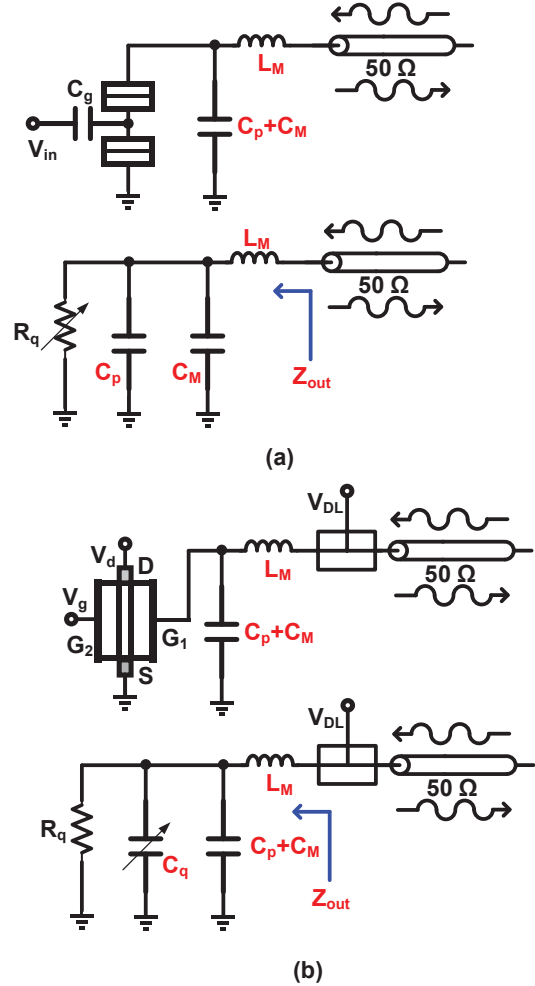

Fig. 3. RF readout techniques of quantum dot and its equivalent circuit for readout: (a) RF reflectometry (b) gate dispersive readout.

$$A_r = A_{in} \cdot \Gamma = A_{in} \frac{Z_{out} - Z_0}{Z_{out} + Z_0}, \tag{1}$$

where Z_0 is the character impedance of the transmission line, Γ is the reflection coefficient and Z_{out} is the output impedance of the quantum device with LC- IMN. i.e.:

$$Z_{out} = \frac{R_q}{1 + j\omega R_q(C_M + C_p)} + j\omega L_M. \tag{2}$$

For the change of the spin status for an electron, the variation for the amplitude and the phase of the reflected signals can be deduced as,

$$\Delta A = \frac{|A_{in}|\Delta R_s}{2 Q R_s} \tag{3}$$

$$\Delta\varphi \approx -\frac{\pi Q \Delta C_q}{C_p}, \tag{4}$$

where Q is the quality factor of the matching network, $R_s = 50$ Ω is the real part of Z_0, and ΔR_s is the change of the real part of the impedance of Z_{out}.

Assuming P_{in} is incident power to the quantum device, to prevent incident signal from coupling to quantum dot, P_{in}
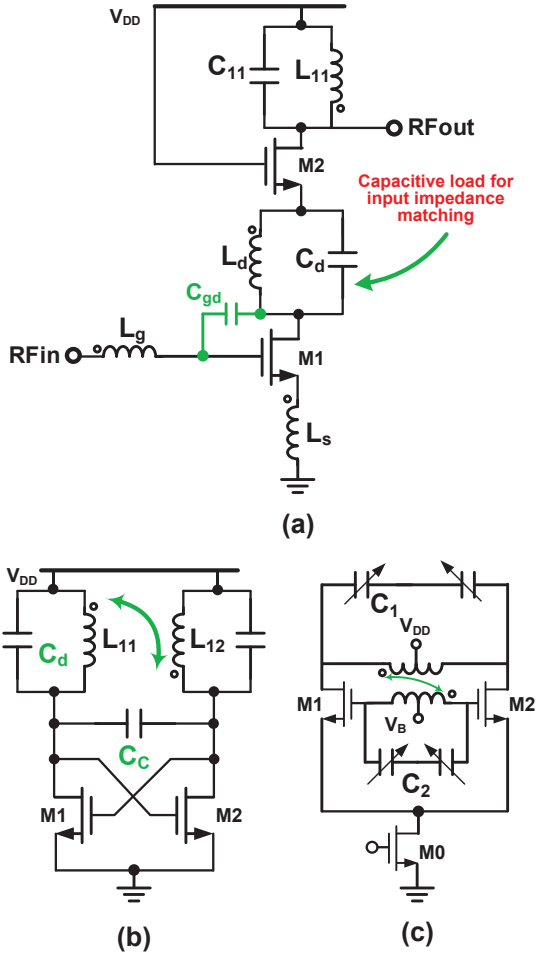
Fig. 4. CMOS circuit topologies to achieve low noise performance

To demodulate, the reflected signals are mixed with the LO signal provide by the VCO. The calculated PN requirement of the VCO in the thermal noise should be better than -147 dBc/Hz at 10 MHz offset from the carrier and -115 dBc/Hz in the sub flicker noise corner region [5].

III. CIRCUIT IMPLEMENTATION ON CMOS TECHNOLOGIES

The CMOS process are proposed to design the qubit readout controller system on chip (SOC) [5]. Deep submicron CMOS devices work well and show accpetable noise performance at 4.2 K [11] [12], and low power consumption of the devices also alleviates the cool down requirements to reach cryogenic temperature.

Three typical topologies are applied to fulfil CMOS LNAs at room temperature, i.e. common gate amplifier with Feedback (CGAF) [13][14], inductively degenerated common source (IDCSA) [15], and the noise cancellation amplifier (NCA) [16]. The CGAFs are broadband and the input impedance match can be easily achieved by the intrinsic input impedance of the active devices, while these structures suffer from inferior noise performance (>2 dB) since theoretical optimum achievable noise ($1+\gamma/\alpha \approx 2\sim3$) is heavily deviated from device minimum noise figure $F_{min} < 0.5$ dB at sub-10 GHz. The NCA utilizes an auxiliary amplifier path to create out-of-phase noise signal at the output node. In principle, the noise of the main amplifier will be nullified, while the auxiliary amplifier can still contribute considerable noise. Given the power consumption is nearly doubled due to dual-path, these structures are not attractive for qubit readout application, especially when the qubit readout frequency is set to higher than 6 GHz to make matching inductors small enough to be integrated on chip [17].

The IDCSAs are widely used in narrowband LNAs design, and F_{min} can be achieved by optimum noise impedance (Z_{opt}) matching. However optimum noise impedance can be only matched at single frequency and, as CMOS processes advance, the effect of gate-drain capacitor (C_{gd}) becomes influent, which leads to the input impedance of transistor $Z_{in} \neq Z_{opt}^*$. Thus the input impedance matching and the noise matching cannot be achieved simultaneously. As shown in Fig.4 (a), a capacitive load is introduced to adjust Z_{in} of the amplifier while keep Z_{opt} unchanged [18]. This structure was used to design LNAs in 90 nm CMOS process with NF smaller than 0.5 dB at 1 GHz, which satisfies NF specifications for qubit readout, while the broadband design at higher frequency is still open to be investigated.

Since the flicker noise of the transistors goes higher at cryogenic temperature and the bandwidth of the phase-locked-loop is limited, when designing VCOs at 4.2 K for qubit readout both the thermal noise region ($1/f^2$) and the flicker noise ($1/f^3$) region should be treated seriously. Recently, harmonic oscillator techniques were proposed to optimize phase noise of the VCO [19], where the second harmonic is used to lower the flicker noise corner and the third harmonic is applied to reduce impulse sensitivity function (ISF) and thus PN, due to thermal noise. A typical VCO structure with second harmonic optimization is illustrated in Fig.4 (b) [20], where LC tank resonates at both operating frequency and second harmonic. The PN of the VCO is -139.7 dBc/Hz at $\Delta f = 3$ MHz from 3 GHz, and the flicker noise corner is

should be set <-99 dBm for both readout techniques [5]. For the amplitude based radio-frequency reflectometry, given the variation of the resistance is around 10% and $Q = 15$, based on (3), the reflected signal power can be calculated as -124 dBm. The readout fidelity F_R is determined by the SNR of the front-end circuit [9] according to:

$$F_R = \frac{1}{2} Erfc\left(\frac{1}{2\sqrt{2}}\sqrt{SNR}\right) \qquad (5)$$

The noise temperature specification of the LNA for $Q = 15$ can be calculated as 6.3 K for readout frequency of 1 GHz.

For the RF gate dispersive readout, the reflected signal at input port of the LNA is determined by the performance of LC-IMN. Assuming the reflected scatter parameter $S_{11} = -10$ dB, the sensed power at the input port of the LNA can be estimated as -110 dBm. Since the phase change of reflected signal is smaller than 1° [8], the demodulation of the reflected signal should be modeled as high order phase shift keying (PSK) signals, such as 512-PSK and 1024-PSK, depending on the Q-factor of the matching network. Based on the results in [10], the required SNR for 512- and 1024-PSK under BER=0.1% are approximately 35 dB and 40 dB, with some margin respectively. Then we can calculated the noise temperature requirements of the LNA are around 22 K and 4.2 K respectively.

around 200 kHz. Fig.4 (c) depicts a class F VCO implemented by transformer where the tank shows high impedance at fundamental frequency and 3rd harmonic [21], and the VCO endows extremely low PN of -142.5 dBc/Hz, with $\Delta f = 3$ MHz at 3.7 GHz, and $1/f^3$ corner is around 300 kHz. Therefore, a low PN and flicker noise corner VCO can be achieved for qubit readout when both 2nd and 3rd harmonics are considered for the tank design.

IV. CONCLUSION

In this paper, we analyzed the operation of semiconductor qubit readout techniques. From this, we deduced the noise performance requirement of RF front-end circuits for qubit readout. The noise figure requirement of the dispersive readout is higher than the RF reflectometry due to the high resolution of the phase variation. The phase noise requirements are also extremely strict comparing to the existing RF wireless communication systems. We also reviewed some typical circuit topologies for LNA and VCO on advanced CMOS process, to show that new circuit techniques should be proposed to satisfy the specifications of the qubit readout application.

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