Low-frequency Noise and Random Telegraph Noise in Nanoscale Devices: Modeling and Impact on Circuit Operation

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***Abstract*—In this work, we present our latest modeling approaches regarding low-frequency noise (LFN) and random telegraph noise (RTN) in advanced MOSFETs, with a special focus on the fully depleted (FD) SOI CMOS technology. Concerning the channel mobility fluctuations, the Hooge parameter is shown to be inversion charge dependent, thus not constant with bias. Furthermore, we present a method that accounts for the impact of quantum mechanical effects on the RTN trap kinetics and a complete 1/f carrier number with correlated mobility fluctuations noise model for FDSOI MOSFETs. Finally, various methods of model implementation are shown, allowing for accurate defect-aware circuit noise and reliability studies. Oscillators and SRAM circuits are taken as examples.**

Keywords—Low frequency noise, Random Telegraph Noise, Modeling, Verilog-A, FDSOI, MOSFET

I. Introduction

As the intensity of Low frequency noise (LFN) and Random Telegraph Noise (RTN) fluctuations increases with the reciprocal device area [1]-[2], they can therefore jeopardize the functionality of both analog [3] and digital [4] circuits. They could even appear as an ultimate variability source [5] due to carrier dynamic trapping in undoped channel devices. For these reasons, the proper modeling and simulation of LFN and RTN phenomena in nano-scale devices is a key requirement for the technology evaluation and evolution.

In Ultra-Thin Body and Box (UTBB) Fully Depleted Silicon-On-Insulator (FDSOI) MOSFETs [6] in particular, LFN and RTN can be further influenced by coupling effects. Due to this coupling, it is difficult to predict precisely the contribution of each interface on the measured noise. Moreover, application of a positive or negative bias voltage on the buried oxide can possibly lead to the appearance of either Lorentzian-type noise [7], or significant increase of the flicker noise level [8], [9]. Thus, analytical study of the noise sources and their dependence on the bias conditions is crucial for both device characterization and noise modeling.

In this work, we present some important aspects concerning the LFN/RTN modeling in advanced devices, as well as the development of circuit noise simulation methods. In Section II, some new noise modeling approaches are presented regarding the Hooge channel mobility fluctuations, the impact of quantum mechanical effects on the trap kinetics and the flicker noise of FDSOI MOSFETs. In Section III, we demonstrate a series of different model implementation methods that can provide realistic defect-aware circuit noise simulations of high accuracy.

II. Revision of Noise Model Approaches

A. Dependence of Hooge parameter on inversion charge

According to the Hooge mobility fluctuations (HMF) noise model [10], the drain current noise is the result of carrier mobility fluctuations stemming from variations in the scattering probability due to phonon number fluctuations. This results in a flicker noise with amplitude inversely proportional to the total number of carriers in the device. The normalized drain current noise in linear operation then reads [11]:

$$\frac{S_{Id}}{I_d^2} = \frac{q\alpha_H}{WLQ_i f} \tag{1}$$

where Q_i is the inversion charge and α_H is the Hooge parameter ($\approx 10^{-7}$-10^{-4}). In (1) it is implied that α_H is independent of voltage bias or inversion charge. However, as the Hooge mobility fluctuations depend only on the phonon scattering rate [12], α_H should be modulated by its contribution among other scattering mechanisms limiting the carrier mobility. Therefore, in the case of a MOSFET, the Hooge parameter should be expressed as:

$$\alpha_H = \alpha_{H0}\left(\frac{\frac{1}{\mu_{ph}}}{\frac{1}{\mu_{ph}}+\frac{1}{\mu_{Cs}}+\frac{1}{\mu_{SR}}}\right)^2 \tag{2}$$

where α_{H0} refers to the intrinsic Hooge parameter and μ_{ph}, μ_{Cs} and μ_{SR} are respectively the phonon, Coulomb and surface roughness scattering limited mobility in the inversion layer [13]. If we also account for the universal mobility law [33], against effective electric field as plotted in Fig. 1(a), the dependence of α_H can be evaluated theoretically versus the inversion charge from weak to strong inversion. As shown in Fig. 1(b), α_H is far from being independent of the inversion charge, and is maximized when

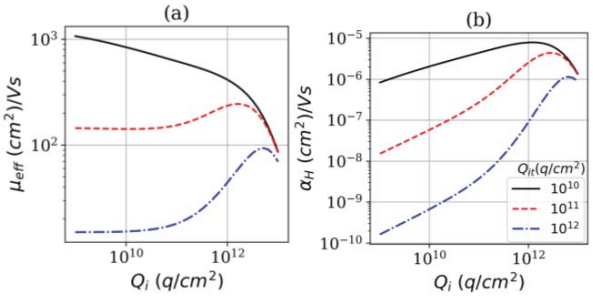

Fig. 1. Theoretical variations of μ_{eff} (a) and Hooge parameter α_H (b) with MOSFET inversion charge Qi for various interface charge Q_{it} levels modulating the Coulomb scattering rate (α_{H0}=10^{-5}).

the PH contribution prevails with respect to CS and SR rates.

Fig. 2 shows the impact of the Hooge parameter dependence with inversion charge (2) on the associated normalized drain current noise. In this situation, S_{Id}/I_d^2 is no longer simply inversely proportional to the inversion charge as it were the case for HMF model with constant mobility.

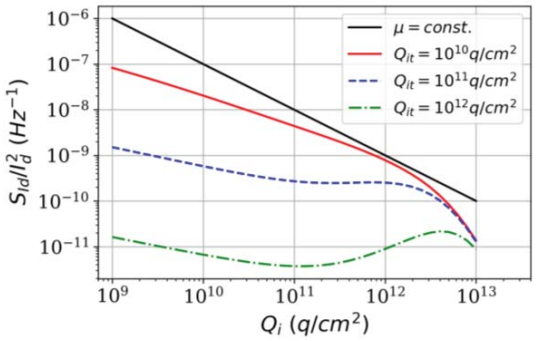

Fig. 2. Variation of normalized drain current noise S_{Id}/I_d^2 with inversion charge for HMF model with Hooge parameter of Fig. 1b.

B. Impact of QMEs on Random Telegraph Noise

Regarding the trap kinetics, in general, the RTN capture and emission times are governed by the Shockley-Read-Hall statistics [14] and read:

$$\bar{\tau}_c = \frac{1}{\sigma n_s v_{th}}\ (a)\ ,\ \ \bar{\tau}_e = \frac{1}{\sigma n_t v_{th}}\ (b) \tag{3}$$

where v_{th} is the thermal velocity, σ is the trap cross section, n_s is the surface carrier concentration and n_t is the surface carrier concentration when the Fermi level E_f crosses the trap energy E_t. The trap cross section might depend on the trap depth into the oxide and on the temperature as $\sigma=\sigma_0 \exp(-E_a/kT).\exp(-x_t/\lambda)$ [14].

However, when the trap is not located right at the oxide-channel interface, but at a depth x_t in the oxide, the apparent trap energy E_t depends on the band bending in the gate dielectric as:

$$E_t = E_{t0} - q\frac{x_t}{t_{ox}}\left(V_g - V_{fb} - \psi_s\right) \tag{4}$$

where ψ_s is the surface potential and V_g is the gate voltage. Another way to express this difference is through n_t in 3(b), if we replace it with:

$$n_t = n_0 e^{\frac{\psi_{st}}{kT}} = n_0 e^{\frac{\psi_{st,0} - \Delta\psi_t}{kT}} \tag{5}$$

where ψ_{st} is the surface potential for which E_t coincides with E_f, and $\Delta\psi_t = x_t.Q_i/\varepsilon_{ox}$ corresponds to the potential drop across the oxide, from the interface to the trap depth.

It should also be noted that the capture and emission times of (3) are evaluated within the classical statistics i.e. using carrier volumetric concentration at the surface. They have to be updated when quantum mechanical effects become important in the MOSFET inversion layer, since n_s is cancelled out at the surface. Indeed, the capture probability is proportional to the escape frequency, f_e (≈2.10^{13} Hz), of the electrons in the quantized sub-band and to the barrier tunnelling transparency to reach the trap in the oxide. If in addition we take into consideration (5), the capture and emission time can be expressed in a way that accounts for the trap depth x_t within the single sub-band approximation as:

$$\bar{\tau}_c = \frac{q}{\sigma f_e Q_i}\ (a)\ ,\ \ \bar{\tau}_e = \frac{q.e^{\frac{x_t(Q_i+Q_d)}{kT\varepsilon_{ox}}}}{\sigma f_e Q_{it}}\ (b) \tag{6}$$

where, ε_{ox} is the oxide permittivity, Q_{it} the inversion charge when the Fermi level E_f crosses the trap energy E_t and Q_d is the depletion charge. It should be emphasized that this formulation (6) of the capture and emission times can also be of great interest for compact modelling applied to circuit simulation (see section III).

C. Flicker noise (1/f) modeling in FDSOI MOSFETs

A very useful quantity for noise model implementation in circuit simulations is the input-referred gate voltage noise $S_{Vg}=S_{Id}/g_m^2$, because it can be inserted as a voltage noise source at the transistor gate. Following this conversion, the Carrier Number Fluctuations (CNF) with Correlated Mobility Fluctuations (CMF) model [15] is expressed as [16]:

$$S_{Vg} = S_{Vfb}\left(1 + \Omega\frac{I_d}{g_m}\right)^2 \tag{7}$$

where S_{Vfb} is the flat band voltage power spectral density given by (8) and $\Omega=\alpha_{sc}\mu_{eff}C_{ox}$ is the CMF factor with α_{sc} being the remote Coulomb scattering coefficient.

$$S_{Vfb} = \frac{q^2\lambda kTN_t}{WLC_{ox}^2 f} \tag{8}$$

Now if we consider that in SOI devices, there are two interfaces present -the channel/gate oxide and the channel/buried oxide, (8) shall be rewritten as [17]:

$$S_{Vg} = S_{Vfb1}\left(1 + \Omega_1\frac{I_d}{g_{m1}}\right)^2 + S_{Vfb2}\left(1 + \Omega_2\frac{I_d}{g_{m2}}\right)^2 \tag{9}$$

where index 1 refers to the front and 2 to the back interface. Combining (8) and (9) and accounting for the fact that in front-gate mode, Ω_2 can be considered negligible (shown in [17]), we obtain:

$$S_{Vg1_{(SOI)}} = S_{Vfb1}\left[\left(1 + \Omega_1\frac{I_d}{g_{m1}}\right)^2 + C_{21}^2\frac{N_{t2}}{N_{t1}}\left(\frac{C_{ox1}}{C_{ox2}}\right)^2\right] \tag{10}$$

with $C_{21}= g_{m2}/g_{m1}$ being the coupling factor. Equation (10) reveals that in the simplest case where $\Omega_i=0$ and $g_{m2}/g_{m1}= C_{ox1}/C_{ox2}$ (subthreshold region), the total noise level is equal to the front interface noise multiplied by $(1+N_{t2}/N_{t1})$. Thus, in the case of same quality oxide interfaces, the total 1/f noise would be two times higher in amplitude than the typical bulk MOSFET 1/f noise. If we further consider the FDSOI case where the channel is depleted when no significant back-bias is applied and add the access resistance noise term, we can create a generic model approach as below:

$$S_{Vg,i} = S_{Vfb,i}\left[\left(1 + \Omega_i\frac{I_d}{g_{m,i}}\right)^2 + \frac{N_{t,j}}{N_{t,i}}\left(\frac{1}{1 + C_{ox,j}/C_{Si}}\right)^2\right] + \left(\frac{g_d}{g_{m,i}} + \frac{1}{2}\right)^2 S_{Rsd} \tag{11}$$

where the index "i" corresponds to the operating gate interface, i.e. 1 for front-gate (FG) mode and 2 for back-gate (BG) mode, and index "j" to the opposite side interface. This equation reveals that the contribution of the opposite interface to the total 1/f level depends on both the trap density ratio and its oxide to channel capacitance ratio.

It should be noted that the last term in (11) is obtained by considering that the drain current sensitivity with respect to the access resistance R_{sd} variation is given by:

$$\frac{\partial I_d}{\partial R_{sd}} = g_d + \frac{g_m}{2} \tag{12}$$

III. From Noise Modeling to Circuit Simulations

For our noise model implementations, we used the Verilog-A [18] behavioral description language, since it provides the capacity of both frequency and time domain simulation approaches, while allowing for full description of the device behavior and its interface connections.

A. Frequency vs time domain modeling

Provided that there is a compact flicker noise model expression, one can easily include a noise source in the Verilog-A code. The CNF/CMF model (8) for example can be implemented by adding two voltage noise sources at the transistor gates, as follows:

V(g) <+ flicker_noise(Svg1, 1, "CNFCMF1");

V(b) <+ flicker_noise(Svg2, 1, "CNFCMF2");

where *Svg1-2* are the power spectral density (PSD) values at 1 Hz and can be given through (9) in the Verilog-A code, accounting for both front/back transconductances g_{m1} and g_{m2}. The number 1 represents the value of the exponent γ and "CNFCMF1-2" are the names of the noise sources. These voltage sources will automatically induce a drain current PSD equal to $S_{Vg1}.g_{m1}^2 + S_{Vg2}.g_{m2}^2$.

The above method is very efficient for circuit simulations in the frequency domain accounting for 1/f noise. A good example of such case is the phase noise, because in frequencies close to the oscillation frequency it is directly proportional to the LFN amplitude [19]. In order to demonstrate the importance of accurate LFN modelling in FDSOI circuits, we took the example of a 3-stage ring oscillator circuit. Fig. 3 shows three examples: one case where only the front interface noise is considered (N_{t2}=0), one where N_{t2}=N_{t1}/2 and finally a case with equally defective front and back oxides (N_{t2} = N_{t1}). From the figure becomes clear that if the N_{t2} contribution is not taken into account,

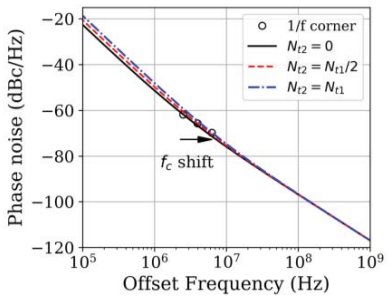

Fig. 3. Simulated 3-stage oscillator (W=10μm, L=30nm) phase noise versus frequency for three different N_{t2}/N_{t1} ratios, using the model of (9). The flicker/thermal corner frequency points are noted with a circle.

both the phase noise level and the 1/f corner frequency are underestimated by 2-3 times, which may lead to false design decisions.

Regarding the time domain, even only with 1/f noise modules, realistic fluctuation-aware transient results can be obtained by using the "Transient Noise" option in Spectre (Cadence) or ELDO (Mentor Graphics) simulators with proper time constraints (speed and duration) as we have shown in [20] and [5]. Fig. 4 shows such an example, where we simulated the measured Supply Read Retention Voltage dynamic variability of a 6T SRAM cell, using the Periodic Transient Noise approach [5].

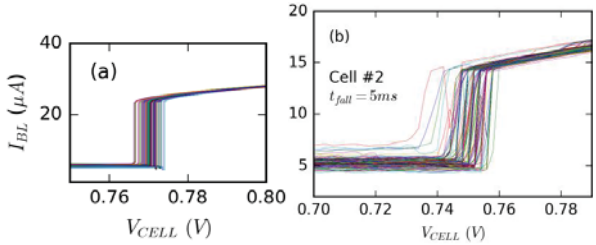

Fig. 4. Noise-induced dynamic variability of 6T SRAM cell SRRV (after [5]): periodic transient noise simulations with 1/f Verilog-A noise module (a) and I-V measurements with Agilent B1530A (b).

However, 1/f noise is rarely the dominant LFN source in advanced nano-scale area MOSFETs like FDSOI [17], FinFETs [21] or Nanowire FETs [22] where g-r or RTN related Lorentzian noise often prevail. Thus, the non-1/f frequency dependencies cannot be taken into account by applying the "flicker_noise" method, making it unsuitable for reliable sub-μm circuit noise simulations. A compromising way would be to use the "noise_table" function in Verilog-A and insert Lorentzian PSD table values for each voltage bias. Nonetheless, apart from this method's complexity, the corresponding "Transient Noise" results cannot reproduce the RTN abrupt current shifts which can cause digital circuit errors [4]. Fortunately, Verilog-A can be also used to create time-dependent modules, since it gives access to the running time value of a transient simulation, as well as control over parameters such as the permitted time-step etc. This proves very useful for defect-aware transient simulations, from RTN and LFN to BTI (time-dependent degradation).

An example of such defect-aware module can be found in [23]: the trap occupancy is checked in every time-step and/or bias modification, resulting in realistic transient and PSD results, as shown in Fig. 5. Using the same module, we showed that the RTN-induced static-noise margin (SNM) dynamic reduction reaches 20% (Fig. 6), which corresponds

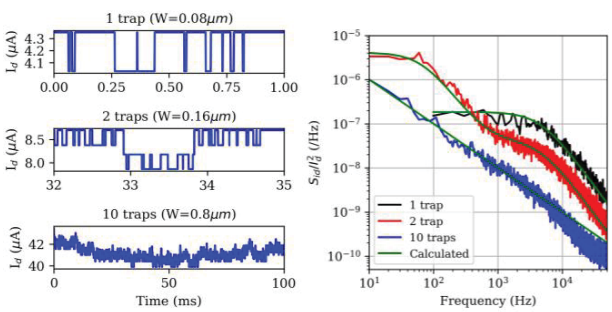

Fig. 5. Simulated RTN signal examples for N_T = 1, 2 and 10 traps (left) and corresponding normalized FFT spectra (right) (after [23]).

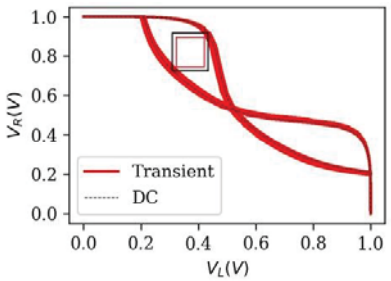

Fig. 6. Right versus left node voltage plot to extract Read Static Noise Margin with and without the impact of defect activity (after [23]).

to 1/3 of the mismatch-induced SNM reduction. This means that the total (static+dynamic) variability in nano-scale circuits can be increased by 30%.

B. *Implementing defect-aware models in existing PDKs*

In one of our recent works [23], we integrated the aforementioned Verilog-A defect-aware module in an open FDSOI compact drain current model, achieving one-step bias-dependent transient simulations. However, in order to make the use of our module completely generic and current model independent, it needs to be implemented using already existing PDK device instances. To this end, the simplest way would be to create a sub-circuit instance that contains the PDK transistor, along with a RTN voltage source in series with the gate, as shown in Fig. 7(a), so that $V_g' = V_g + \Delta Vg$, where $\Delta V_g = -\Delta V_{t\_RTN}$. Because the PDK device models usually don't provide access to the inversion charge values, obtaining the drain current, I_d, values during a transient is needed for the calculation of τ_c and τ_e for each trap. If the mobility degradation effects are neglected for simplicity, one can express the inversion charge as:

$$Q_i(t) = \frac{L}{W}\frac{I_d(t)}{\mu_0 V_d} \ (a) \quad , \quad Q_{it} = \frac{L}{W}\frac{I_{dt}}{\mu_0 V_d} \ (b) \qquad (13)$$

However, this implementation method has a serious issue: $I_d(t)$ is the device current that contains the defect activity induced through ΔV_t that causes a ΔI_d shift. Thus, the capture time calculation during a transient simulation is sensitive to the trap occupancy itself, creating continuity errors. The solution we propose is to use an ideal defect-less "dummy" transistor inside the sub-circuit, which will always provide the $I_d(t)$ values without accounting for the trap activity. This method is illustrated schematically in Fig. 7(b).

Finally, regarding the energetic position of the traps, since we cannot express a charge-voltage relation as in [23], the trap energy level can be declared through a characteristic I_{dt}, for which E_t coincides with E_f and calculate Q_{it} through 13(b), to use it in 6(b) for the calculation of τ_e.

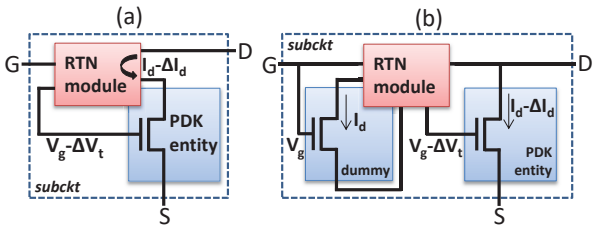

Fig. 7. Module implementation methods in existing PDKs: without (a) and with (b) noise-less dummy transistor.

REFERENCES

[1] G. Ghibaudo, O. Roux-dit-Buisson, and J. Brini, "Impact of Scaling Down on Low Frequency Noise in Silicon MOS Transistors," *Phys. Status Solidi*, vol. 132, no. 2, pp. 501–507, Aug. 1992.

[2] K. K. Hung, P. K. Ko, C. Hu, and Y. C. Cheng, "Random telegraph noise of deep-submicrometer MOSFETs," *IEEE Electron Device Lett.*, vol. 11, no. 2, pp. 90–92, 1990.

[3] G. Wirth, D. Vasileska, N. Ashraf, L. Brusamarello, R. Della Giustina, and P. Srinivasan, "Compact modeling and simulation of Random Telegraph Noise under non-stationary conditions in the presence of random dopants," *Microelectron. Reliab.*, vol. 52, no. 12, pp. 2955–2961, 2012.

[4] K. Takeuchi *et al.*, "Direct observation of RTN-induced SRAM failure by accelerated testing and its application to product reliability assessment," *Dig. Tech. Pap. - Symp. VLSI Technol.*, pp. 189–190, 2010.

[5] C. G. Theodorou, M. Fadlallah, X. Garros, C. Dimitriadis, and G. Ghibaudo, "Noise-induced dynamic variability in nano-scale CMOS SRAM cells," in *European Solid-State Device Research Conference*, 2016, vol. 2016–Octob, pp. 256–259.

[6] N. Planes *et al.*, "28nm FDSOI technology platform for high-speed low-voltage digital applications," *Dig. Tech. Pap. - Symp. VLSI Technol.*, vol. 33, no. 4, pp. 133–134, 2012.

[7] E. Simoen, A. Mercha, C. Claeys, N. Lukyanchikova, and N. Garbar, "Critical discussion of the front-back gate coupling effect on the low-frequency noise in fully depleted SOI MOSFETs," *IEEE Trans. Electron Devices*, vol. 51, no. 6, pp. 1008–1016, 2004.

[8] L. Zafari, J. Jomaah, and G. Ghibaudo, "Low frequency noise in multi-gate SOI CMOS devices," *Solid. State. Electron.*, vol. 51, no. 2, pp. 292–298, 2007.

[9] C. G. Theodorou *et al.*, "Impact of front-back gate coupling on low frequency noise in 28 nm FDSOI MOSFETs," *Eur. Solid-State Device Res. Conf.*, vol. 2, no. 2, pp. 334–337, 2012.

[10] F. N. Hooge, "1/f noise," *Phys. B+C*, 1976.

[11] I. M. Hafez, G. Ghibaudo, and F. Balestra, "A study of flicker noise in MOS transistors operated at room and liquid helium temperatures," *Solid State Electron.*, 1990.

[12] F. N. Hooge, "1/F Noise Sources," *IEEE Trans. Electron Devices*, vol. 41, no. 11, pp. 1926–1935, 1994.

[13] K. Takagi, T. Mizunami, T. Shiraishi, and M. Wada, "Excess noise generation by carrier fluctuation in semiconductor devices," in *IEEE International Symposium on Electromagnetic Compatibility*, 1994.

[14] M. J. Kirton, M. J. Uren, S. Collins, and M. Schulz, "Individual defects at the Si:SiO2 interface," *Semicond. Sci. Technol.*, vol. 4, pp. 1116–1126, 1989.

[15] G. Ghibaudo, O. Roux, C. Nguyen-Duc, F. Balestra, and J. Brini, "Improved Analysis of Low Frequency Noise in Field-Effect MOS Transistors," *Phys. Status Solidi*, vol. 124, no. 2, pp. 571–581, 1991.

[16] E. G. Ioannidis, C. A. Dimitriadis, S. Haendler, R. A. Bianchi, J. Jomaah, and G. Ghibaudo, "Improved analysis and modeling of low-frequency noise in nanoscale MOSFETs," *Solid. State. Electron.*, vol. 76, pp. 54–59, 2012.

[17] C. G. Theodorou *et al.*, "Low-Frequency Noise Sources in Advanced UTBB FD-SOI MOSFETs," *IEEE Trans. Electron Devices*, vol. 61, no. 4, pp. 1161–1167, 2014.

[18] G. Depeyrot, "Verilog-A Compact Model Coding Whitepaper," *Memory*, vol. 2, no. June, pp. 821–824, 2010.

[19] A. Hajimiri and T. H. T. H. T. H. Lee, "A general theory of phase noise in electrical oscillators," *IEEE J. Solid-State Circuits*, vol. 33, no. 2, pp. 179–194, 1998.

[20] C. G. Theodorou, E. G. Ioannidis, S. Haendler, C. A. Dimitriadis, and G. Ghibaudo, "Dynamic variability in 14nm FD-SOI MOSFETs and transient simulation methodology," *Solid. State. Electron.*, vol. 111, no. September, pp. 100–103, 2015.

[21] C. G. Theodorou, N. Fasarakis, T. Hoffman, T. Chiarella, G. Ghibaudo, and C. A. Dimitriadis, "Origin of the low-frequency noise in n-channel FinFETs," *Solid. State. Electron.*, vol. 82, pp. 21–24, Apr. 2013.

[22] S. Yang *et al.*, "Random Telegraph Noise in n-type and p-type silicon nanowire transistors," *2008 IEEE Int. Electron Devices Meet.*, pp. 1–4, 2008.

[23] C. G. Theodorou and G. Ghibaudo, "A Self-contained Defect-aware Module for Realistic Simulations of LFN, RTN and Time-dependent Variability in FD-SOI Devices and Circuits," in *IEEE S3S Conference*, 2018.