Nanoimprint Technology for Liquid-Gated Si Nanowire FET Biosensors: Noise Spectroscopy Analysis

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***Abstract*—Silicon nanowire (Si NW) field-effect transistors (FETs) are currently attracting considerable attention in both theoretical and practical studies. Their remarkable properties, in particular their high sensitivity to surface charges, open up prospects for various sensing applications. Devices based on Si NW FETs are usually fabricated by relatively expensive electron-beam lithography (EBL). Here, we report on the results of studies involving accumulation mode *p*-type liquid-gated Si NW FETs fabricated making use of optimized, cost-efficient, and CMOS-compatible nanoimprint technology. Electrical transport in the fabricated structures is investigated using DC current-voltage measurements and low-frequency noise spectroscopy. The results obtained indicate the high quality of the Si NW FET structures and their stable operation in the electrolyte liquid environment without leakage currents. Noise studies reveal that the main origin of noise is the mobility fluctuation of the charge carriers in the nanowire channel. The nanowire FET performance parameters are extracted by data analysis and compared to those reported in the literature.**

***Index Terms*—Silicon nanowires, nanoimprint technology, noise spectroscopy, biosensors.**

I. Introduction

Continuous quality monitoring of silicon nanowire field-effect transistor (FET) structures is an essential prerequisite for the successful development of robust and reliable biosensors based on silicon nanowires (Si NWs). Thus, appropriate performance characterization tests have to be performed at every development stage from device fabrication up to encapsulation and calibration.

Fabrication is usually performed on the basis of commercially available silicon-on-insulator (SOI) wafers. Choosing either *p*- or *n*-type SOI wafers with the defined level of impurities determines the doping level of nanowires and their further performance as FET biosensors. The source and drain areas should have small resistances to be able to form ohmic contacts. They are usually defined by photolithography and a subsequent heavy doping procedure. Then the mesa structure, including the pattern for the source and drain areas as well as for the areas reserved for nanowires, is defined using reactive ion etching (RIE). Nanosized nanowire structures are patterned by means of electron-beam lithography (EBL), followed either by RIE or wet chemical etching procedures. Finally, passivation and surface modification steps are performed to make the fabricated Si NW FET devices suitable for selective and sensitive measurements of bioliquids.

One of the key advantages of the "top-down" fabrication technology is its high complementary metal oxide semiconductor (CMOS) compatibility. It also provides precise control over the orientation of nanowires. State-of-the-art electron beam and focused ion beam lithographies allow patterning of nanoscale objects less than $10\,\mathrm{nm}$ in size. However, such techniques are relatively expensive and not well suited for large-scale serial production. Recent advances in fabrication techniques, such as nanoimprint lithography (NIL) permit reliable and cost-efficient nanostructure patterning, which facilitates rapid large-scale fabrication of nanowires with a high yield rate.

The fabrication of nanowire biosensors using nanoimprint lithography consists of two main steps: fabrication of the mold (a reusable master for patterning the nanowire structures) and subsequent fabrication of Si NW FETs – active transducers of the sensor. Optimization of the technological processes involved in fabrication is crucial for the performance of the devices, and thus has to be performed carefully. The master structure should allow low-roughness high-resolution nanopatterning. It should also have good mechanical properties, e.g., stiffness, to be suitable for multiple use. In this respect, silicon can be considered a perfect substrate material for mold fabrication. It possesses high mechanical stability, and it can be processed using well-developed CMOS-compatible technologies. Anisotropic wet etching techniques allow very smooth etching profiles to be achieved, which is crucial for device performance.

Despite the tremendous sensitivity of biosensors based on Si NW FETs, they still have certain disadvantages. One of the most fundamental problems is the degeneration of their electrical characteristics while working in electrolyte liquid environments [1]. This unwanted effect is most often caused by the degradation of the gate insulator, which is exposed to the bioliquids under study in the sensing experiments.

Therefore, the quality of the gate dielectric often defines the performance of Si NW FET sensors [2]. In this regard, using techniques to constantly control device performance and establishing novel nondestructive sensing approaches is crucial for the development of reliable Si NW biosensors.

Ultimate downscaling of the electronic devices substantially restricts the use of traditional characterization techniques, e.g., capacitance-voltage measurements. Thus, an alternative approach has to be utilized to investigate the conducting channel/insulator and insulator/electrolyte interfaces in nanoscale liquid-gated Si NW FETs. Low-frequency noise spectroscopy can therefore provide information about the quality, electrical performance, and operating regimes of silicon nanowire structures [3]. This is a powerful, highly sensitive, and nondestructive characterization approach. Thus, it can replace capacitance-voltage measurements and complement DC current-voltage characterization.

In this contribution, we report on studies of transport and low-frequency noise behavior of accumulation mode p-type liquid-gated silicon nanowire field-effect transistors, fabricated using advanced CMOS-compatible nanoimprint technology. We estimated the important characteristics of our NW FET devices, i.e., the threshold voltage V_{Th}, the subthreshold swing SS, and the carrier mobility μ. Investigation of the noise behavior revealed that the excess noise originates from the mobility fluctuations in the NW channel. We also estimated the dimensionless Hooge parameter, the measure of device "noisiness", and compared it with the values reported in the literature. Our findings indicate the high quality of the fabricated Si NW FET devices, and they are important for the development of highly-sensitive Si NW-based biosensors.

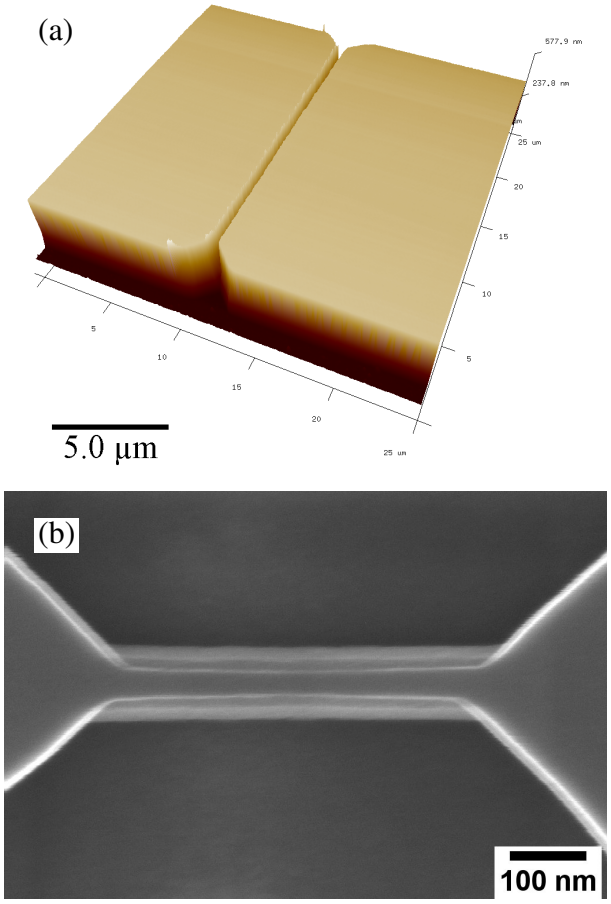

Fig. 1: (a) AFM micrograph of a typical fabricated mold, etched in the Si$\langle 110 \rangle$. (b) Scanning electron microscopy (SEM) image of a typical single Si NW structure after wet etching.

II. Results and Discussion

A. Device fabrication

We designed and fabricated the nanoimprint mold with decreased roughness on the basis of Si$\langle 110 \rangle$ substrates using electron-beam lithography and wet KOH etching. It was utilized as a reusable mask to pattern the nanowires. The high quality of the mold for NW structures was confirmed by atomic force microscopy (AFM) imaging (see Fig. 1 (a)). It should be noted that the fabricated mold allows simultaneous patterning of the tiny nanowire structures as well as the large feed lines and contact pads.

The silicon nanowire biosensors were fabricated on the basis of $100\,\mathrm{mm}$ p-type SOI wafers, purchased from Soitec. The substrates had $70\,\mathrm{nm}$ of a p-type active Si$\langle 100 \rangle$ layer, separated from the highly doped base silicon by a $145\,\mathrm{nm}$ thick buried oxide (BOX) layer. To transfer the pattern from the mold to the SOI substrate, the latter was coated with mr-I 7020R resist and thermal nanoimprint lithography was performed. After the nanowires had been defined in the resist, dry and wet etching procedures were used to transfer the pattern first to the hard mask and then to the active silicon layer. Wet etching was performed in $5\,\%$ tetramethylammonium hydroxide (TMAH) solution at $60\,^{\circ}\mathrm{C}$ in order to implement a smooth etching profile of the nanowire sidewalls. The SEM micrograph of a typical single silicon nanowire structure after TMAH etching is shown in Fig. 1 (b). This approach allowed a significant reduction of the NW surface roughness, and therefore a considerable improvement of the performance of the devices. Nanowire etching was followed by ion implantation, metallization, and thermal annealing of the feed lines to implement ohmic contacts to NW structures. The uniform $8\,\mathrm{nm}$ thin gate dielectric was formed using a dry thermal oxidation process. Lastly, passivation and encapsulation were performed to make the devices suitable for measurements in electrolyte liquid environments.

B. Transport characterization

DC electrical transport in the fabricated Si NW FET devices was investigated using the current-voltage (I-V) approach. The NW structures, covered by silicon dioxide, were exposed to $10\,\mathrm{mM}$ PBS pH = 7.4 solution. An external Ag/AgCl reference electrode was used to apply the gate potential while the drain–source bias V_{DS} was applied to the highly doped contact regions of the nanowire FETs. The V_{DS} was set at $100\,\mathrm{mV}$ in all the measurements performed, thus implementing the linear operation regime for the transistor structures. The current-

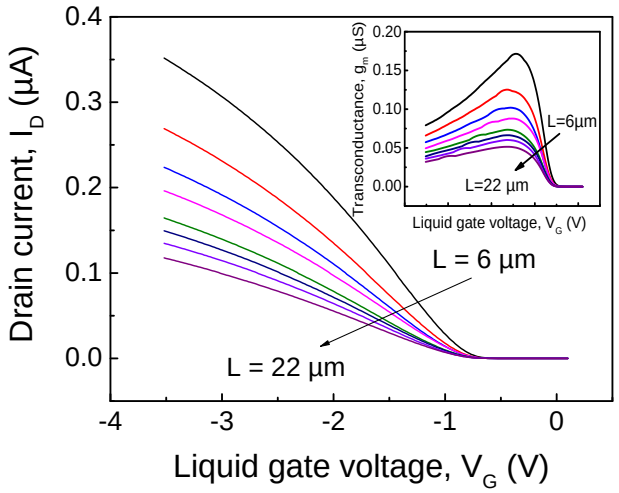

Fig. 2: Set of transfer curves, measured on the accumulation mode p-type single Si NW FET structures with a width of $250\,\mathrm{nm}$ and lengths in the range of $6\,\mu\mathrm{m}$ to $22\,\mu\mathrm{m}$. The corresponding transconductance curves are shown in the inset.

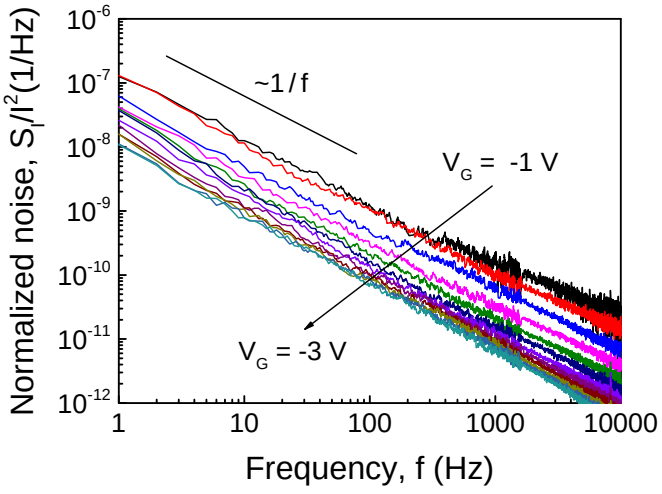

Fig. 3: Typical normalized current noise spectra, measured on the single Si NW structure with a width of $250\,\mathrm{nm}$ and length of $6\,\mu\mathrm{m}$ at different values of the liquid gate voltage in the range from $V_G = -1$ V to $V_G = -3$ V.

voltage characteristics were measured using a Keithley 2602A two-channel source-measurement unit. Typical transfer curves measured on the accumulation mode p-type single silicon nanowire FETs with a width of $250\,\mathrm{nm}$ and lengths in the range of $6\,\mu\mathrm{m}$ to $22\,\mu\mathrm{m}$ are shown in Fig. 2. The fabricated devices show typical transistor-type behavior of the electrical characteristics and stable operation in the electrolyte-liquid environment. It should be noted that the registered leakage current $I_G \leq 1$ nA was at least three orders of magnitude lower than the drain current I_D in the entire range of the liquid gate voltages applied. This confirms the high quality of the fabricated nanowire FET structures. Analysis of the NW FET transfer curves allows the quantitative determination of such important parameters as threshold voltage V_{Th}, subthreshold swing SS, and carrier mobility μ. The first two parameters can be extracted directly from the transfer curves while the remaining parameter can be estimated using the following expression [4]:

$$\mu = \frac{g_m L}{W C_{ox} V_{DS}}. \tag{1}$$

Here, C_{ox} is the gate oxide capacitance per unit area, $g_m = \partial I_D / \partial V_G|_{V_{DS}=const.}$ is the transconductance, W and L are the width and length of the NW channel, respectively. In the first approximation, the C_{ox} value can be estimated using the expression for the parallel plate capacitor:

$$C_{ox} = \frac{\varepsilon_0 \varepsilon}{t_{ox}}, \tag{2}$$

where $\varepsilon_0 \simeq 8.85\times10^{-12}\,\mathrm{F\,m^{-1}}$ is the dielectric permittivity of vacuum, $\varepsilon = 3.9$ is the relative permittivity of the gate oxide, and $t_{ox} = 8$ nm is the gate oxide thickness. The parameters of the studied Si NW FET structure, extracted from the transfer curves, are summarized in Table I. The obtained values are in good agreement with the data reported in the literature [5].

C. Nose studies

The low-frequency noise spectra (from $1\,\mathrm{Hz}$ to $10\,\mathrm{kHz}$) were measured using our advanced noise measurement setup developed in house [6]. Typical normalized current noise spectra, measured on the single silicon nanowire FET structure with a width of $250\,\mathrm{nm}$ and length of $6\,\mu\mathrm{m}$, acquired at different values of the liquid gate voltage are shown in Fig. 3. The measured spectra demonstrate a clear $1/f$ dependence in the entire range of the gate voltages applied.

To analyze the origin of the noise, we calculated the input-referred noise S_U using the current noise spectral density S_I and the transconductance value g_m, obtained as the first derivative of the NW transfer curve:

$$S_U = \frac{S_I}{g_m^2} \tag{3}$$

The input-referred noise level, taken at the frequency of $100\,\mathrm{Hz}$, is plotted vs. the overdrive gate voltage $V_{OV} = V_G - V_{Th}$ in Fig. 4. At increased gate voltages $V_{OV} > -0.5$ V, the S_U increases with increasing liquid gate overdrive. Such noise behavior indicates that the main noise source is the mobility fluctuation of the charge carriers in the nanowire channel, which can be described by the Hooge model [7].

To compare the noise level of the fabricated devices with that reported in the literature we estimated the dimensionless

TABLE I: Parameters of NW FETs

Parameter name		Value	
Threshold voltage	V_{Th}	-0.8	V
Subthreshold swing	SS	130	$\mathrm{mV\,dec^{-1}}$
Carrier mobility	μ	95	$\mathrm{cm^2\,V^{-1}\,s^{-1}}$

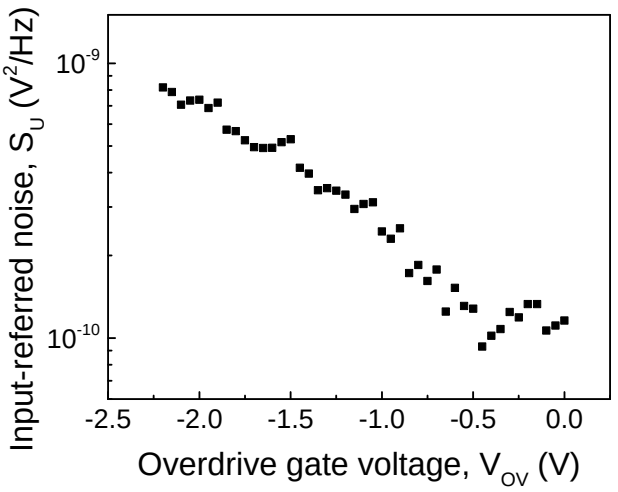

Fig. 4: Input referred noise taken at the frequency of 100 Hz as a function of the overdrive liquid gate voltage.

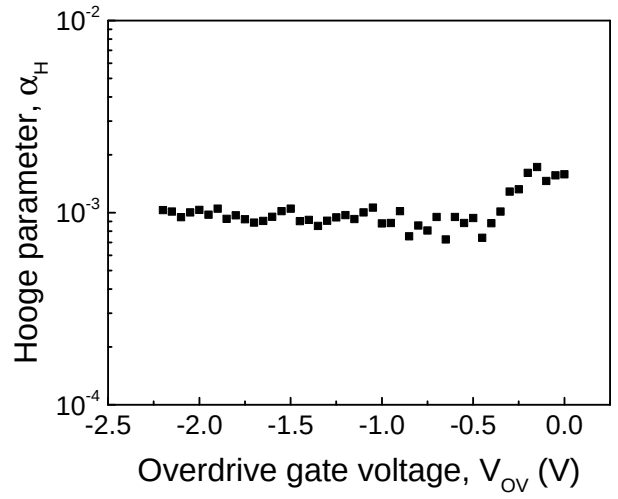

Fig. 5: Hooge parameter as a function of the liquid gate overdrive voltage.

Hooge parameter using the following expression [8], [9]:

$$\alpha_H = \frac{fS_I}{I_D}\frac{L^2}{q\mu V_{DS}}. \tag{4}$$

Here, $q = 1.602 \times 10^{-19}$ C is the electron charge. The Hooge parameter obtained vs. the overdrive gate voltage dependence is shown in Fig. 5. The S_U and α_H values in the liquid-gated NW structures fabricated using the optimized nanoimprint technology are comparable with those obtained for structures fabricated using electron-beam lithography [10] for the same range of overdrive gate voltages. The results demonstrate the high quality of the liquid-gated NW FET structures, which can be used for biosensing and the biomedical monitoring of biological liquids.

III. Conclusions

To conclude, we fabricated silicon nanowire field-effect transistor devices with enhanced characteristics using cost-efficient nanoimprint technology. The high quality of the Si NW structures was confirmed by AFM and SEM imaging. The fabricated nanowire FETs were characterized using the DC current-voltage approach and low-frequency noise spectroscopy. Important performance characteristics including the threshold voltage, subthreshold swing, and carrier mobility were estimated by analyzing the NW FET transfer curves and summarized in Table I. The obtained values are in good agreement with those reported in the literature. Analysis of the noise spectra revealed that the main noise source in the fabricated Si NW FET structures is related to the mobility fluctuations of the charge carriers in the nanowire channel. The estimated values of the Hooge parameter were close to $\alpha_H \approx 1 \times 10^{-3}$, which is comparable with or even lower than those reported for most traditional fabrication technologies including electron-beam lithography.

Acknowledgment

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