Processing Impact on the Low-Frequency Noise of 1.8 V Input-Output Bulk FinFETs

Cor Claeys
ESAT Dept.
KU Leuven
Leuven, Belgium
cor.claeys@kuleuven.be

Geert Hellings, Hiroaki Arimura, Bertrand Parvais, Lars-Åke Ragnarsson, Harold Dekkers, Tom Schram, Dimitri Linten, Naoto Horiguchi and Eddy Simoen
imec
Leuven, Belgium

Dimitri Boudier and Bogdan Cretu
ENSICAEN, UNICAEN, CNRS, GREYC
University of Caen
Caen, France
Bogdan.Cretu@ensicaen.fr

***Abstract*—The low-frequency noise of input-output (I/O) FinFETs with 3.5 nm SiO_2 gate dielectric is studied for different processing conditions. It is shown that a high-pressure (HP) deuterium anneal can improve the noise Power Spectral Density (PSD). There is no significant impact on n-channel devices, while a pronounced effect is observed for p-channel devices, especially for a HP anneal at 400 ºC and 20 atm. Results are also presented on the use of a Si/SiGe superlattice architecture and it is shown that the same gate stack quality as for standard devices can be maintained.**

Keywords—Flicker noise, number fluctuations, oxide trap density, deuterium annealing, input/output FinFETs, superlattice

I. Introduction

System-on-a-chip (SoC) applications of CMOS technology require the presence of different flavors of transistors. Besides devices for high speed and low power logic, high-voltage Input-Output (I/O) transistors, which are able to operate at higher supply voltage, have to be implemented [1]. The corresponding gate oxide thickness (t_{ox}) is currently in the range of 3 nm, so that standard SiO_2 can serve as a high-reliability gate dielectric for I/O MOSFETs. In order to be compatible with a bulk FinFET process flow, alternatives to standard high-temperature thermal oxidation are being explored. An attractive option in this context could be the Atomic Layer Deposition (ALD) of SiO_2 yielding high-quality and highly reliable I/O transistors [2]. It has also been demonstrated that a high-pressure post-deposition annealing (PDA) in deuterium (D_2) can improve the interface properties, i.e., the subthreshold slope *SS* and the density of interface states (D_{it}) of Si-cap-free SiGe p-channel FinFETs and the overall device performance [3].

Further along the roadmap, vertically stacked horizontal gate-all-around nanowire FETs are promising candidates because they allow a more aggressive gate length scaling [4]. However, the spacing between stacked nanowire devices does not accommodate the thick oxide for I/O FETs. Alternatively, one can consider a Si/SiGe/Si/SiGe/Si superlattice FinFET for I/O applications.

In this work, the impact of high-pressure (HP) PDA on the low-frequency (LF) noise performance of 1.8-V compatible I/O bulk FinFETs, with 3.5 nm ALD SiO_2 and metal gate is reported. It is well-known that LF noise is a good quality and reliability indicator for the gate stack [5],[6], which has recently also been applied to planar I/O transistors for DRAM peripheral applications [7],[8]. It is shown here that while the HP annealing has little impact on the 1/*f* noise Power Spectral Density (PSD) of the nMOSFETs, a significant reduction can be observed for the p-channel counterparts, especially, for an anneal at 400 ºC. The responsible mechanism for the 1/*f* noise reduction is investigated, showing that the main contribution comes from the lowering of the access resistance noise. A secondary effect may be the result of a lowering of the density of traps in the SiO_2, with energy close to the silicon valence band edge.

Furthermore, the noise spectra of Si/SiGe superlattice I/O n-channel FinFETs are investigated, pointing out that the spectra contain 1/*f* and generation-recombination (GR) noise components. The flicker noise is related to remote Coulomb scattering impacting the carrier mobility, while traps in the depletion later cause the second component [9].

II. Experimental Details

I/O FinFETs with a supply voltage of 1.8 V have been processed in a 16 nm technology with an Equivalent Oxide Thickness (EOT) of 3.5 nm. The gate stack consists of a SiO_2 gate dielectric processed by Atomic Layer Deposition and a TiN metal gate. One quarter of a 300 mm wafer received a 20 atm H_2 anneal at 450 ºC for 20 min (devices are labeled HP1), while another quarter underwent a 20 atm H_2 anneal at 400 ºC for 20 min (HP2).

Noise measurements have been executed on 1 µm long FinFETs with 4 fins, with a height of 35 nm and a width of 10 nm. The noise was measured on at least four devices per wafer in linear operation ($|V_{DS}|$=50 mV) by stepping the front gate voltage V_{GS} from weak to strong inversion. The input-referred voltage noise PSD was calculated from $S_{V_G} = S_I/g_m^2$, with g_m the measured transconductance in each operation point and S_I the measured drain current noise PSD.

The $Si/Si_{0.70}Ge_{0.30}$ superlattice I/O FinFETs operating at 1.8 V have a gate stack of 2 nm ALD high-κ dielectric (HfSiO) on top of 3 nm interfacial SiO_2. In the case of 2.5 V operation the thickness on the interfacial SiO_2 is increased to 5 nm, resulting in an equivalent oxide thickness (EOT) of 5.6 nm. Full process details are described in [4].

III. Results and Discussion

A. I/O Bulk FinFETs

The input I_D-V_{GS} characteristics in linear operation corresponding with the noise measurements are represented in Fig. 1, together with the transconductance. For the n-channel FinFETs in Fig. 1a, rather similar g_m and I_D are found, the main impact being an increase of the threshold voltage V_T upon application of a HP anneal. No systematic trend is found for the pFinFETs in Fig. 1b, whereby it should be remarked that the observed changes fall within the variability range of the device performance.

Typical LF noise spectra are shown in Fig. 2, in linear operation and at a current of about 1.1 µA for n- (Fig. 2a) and 1 µA for pFinFETs (Fig. 2b) for a reference (no HP anneal), a HP1 and a HP2 device, respectively. As can be seen, the spectra are predominantly $1/f^{\gamma}$-like with the frequency exponent γ close to 1. It is clear from Fig. 2a that there is little difference in the current noise PSD (and also in the normalized PSD given by S_I/I_D^2) for the n-channel transistors. For the pFinFETs, on the other hand, there is a clear reduction of S_I for HP2, while the spectrum for HP1 coincides with the reference non-annealed device.

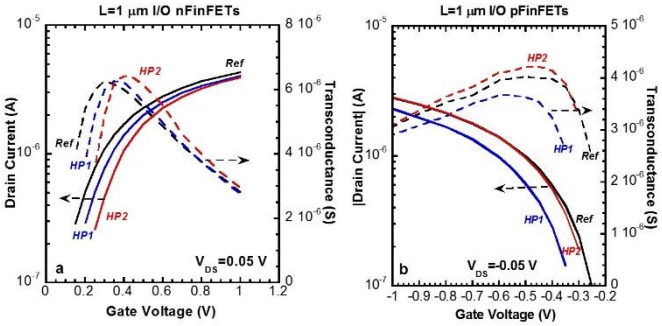

Fig. 1. Input I_D-V_{GS} characteristics in linear operation at $|V_{DS}|$=0.05 V and corresponding transconductance of 1 µm long n- (a) and p-channel (b) FinFETs, without HP annealing (ref), HP1 and HP2.

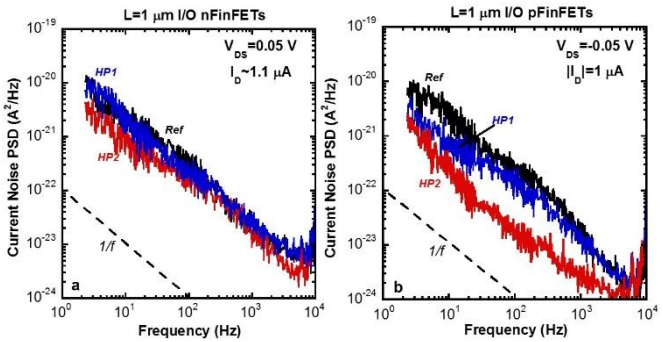

Fig. 2. LF noise spectra in linear operation at $|V_{DS}|$=0.05 V and $|I_D|$~ 1 µA for 1 µm long n- (a) and p-channel (b) FinFETs, without HP annealing (ref), HP1 and HP2. The dashed line is a guide to the eye, representing a $1/f$ slope.

The normalized noise at a frequency f=10 Hz is shown for each type of device as a function of the drain current in Fig. 3. The data for the three types of I/O nFinFETs are rather similar (within the dispersion of the noise data). Moreover, from the proportionality of S_I/I_D^2 with g_m^2/I_D^2, one can conclude that the $1/f$ noise is determined by number fluctuations [5],[6],[10], i.e., by trapping into so-called border traps in the SiO_2. Moreover, for the nFinFETs, within the variability of the data, no change in the oxide trap density is observed at energies close to the conduction band in silicon, following the application of a HP PDA.

The case is different for the pFinFETs in Fig. 3b. A reduction of the normalized current noise PSD is found for the devices with HP1 and HP2, compared with the reference. This occurs mainly for larger $|I_D|$, while in weak-to-moderate inversion, the normalized noise runs parallel with g_m^2/I_D^2. This points to predominant gate oxide trapping as origin for the $1/f$ noise at low currents, while in strong inversion, another mechanism becomes more prominent.

The input-referred voltage noise PSD represented in Fig. 4a for the nFinFETs is constant for most of the gate voltage overdrive V_{GT}=V_{GS}-V_T range studied and corresponds with the value at flat-band voltage, i.e., $S_{V_{FB}}$, with negligible correlated mobility fluctuations. It is rather similar for the three nFinFETs studied. According to the number fluctuations theory, the oxide trap density N_{ot} can be extracted from [5],[10]:

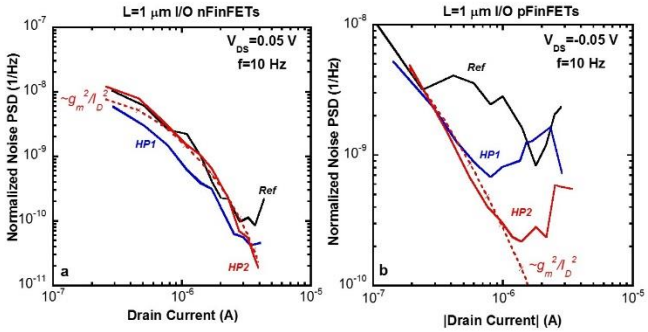

Fig. 3. Normalized current noise PSD, S_I/I_D^2, at f=10 Hz and in linear operation at $|V_{DS}|$=0.05 V of 1 µm long n- (a) and p-channel (b) FinFETs, without HP annealing (ref); HP1 and HP2. The dotted lines correspond with g_m^2/I_D^2.

$$S_{V_{FB}} = \frac{q^2 k_B T \lambda N_{ot}}{f W L C_{ox}} \quad (1)$$

with C_{ox} the oxide capacitance per unit area, q the electron charge; k_B Boltzmann's constant, T the temperature, WL the effective transistor area and λ the attenuation length of the electron (hole) wave function in SiO_2.

The pFinFETs exhibit a much stronger dependence of S_{VG} on the gate voltage overdrive in Fig. 4b. This indicates that besides the number fluctuations and associated correlated mobility fluctuations (CMF) another mechanism becomes important in strong inversion. In fact, it has been shown in the past that at larger currents, there could be a strong impact of the series or access resistance (r_{acc}) on the noise PSD [11], which can be represented by [12]:

$$S_{V_G} = \frac{(r_{tot}-r_{acc})^2}{r_{tot}^2} S_{V_{FB}} (1 \pm \alpha_C \mu_{eff} C_{ox} V_{GT})^2 + \frac{K_r}{f} \frac{r_{acc}^2}{2 r_{tot}^2} \frac{I_D^2}{g_m} \quad (2)$$

with r_{tot} is the total channel resistance (=V_{DS}/I_D in linear operation), r_{acc} the access resistance, K_r the strength of the access resistance noise source, μ_{eff} the effective mobility and α_C the Coulomb scattering factor. The + or – sign in Eq. (2) depends on the donor or acceptor character of the oxide traps. Narrow-fin architectures are particularly prone to a high access resistance and associated increase in input-referred voltage noise PSD [12],[13].

According to the second term in Eq. (2), the access resistance noise S_r increases proportionally with I_D^4, which is represented by the dashed curves in Fig. 4b and well fits the experimental data at more negative gate voltage overdrives. It is also evident that the main effect of the HP anneal is to reduce this S_r contribution to the total noise PSD by approximately 20 % going from the reference to HP2. Note that the increase with V_{GT} in Fig. 4a for the nFinFETs of S_{VG} could also be related to the series resistance noise, although in this case there is no systematic trend between annealed and reference nFinFETs.

Besides the clear reduction of S_r at larger V_{GT} for the pFinFETs, there is also a tendency for lower noise PSD around V_T (the flat-band value) in Fig. 4b, suggesting a reduction in N_{ot} around the valence band energy of silicon. However, considering that three different devices are being measured - and not the same device after different HP PDA – some caution in this interpretation is required, in view of the significant noise dispersion or variability which exists for scaled technologies [6],[13]. Therefore, in Fig. 5 the average flat-band noise PSD at 10 Hz is represented for all n- and p-channel FinFETs studied, showing little change for the n-channel devices and a marked reduction for the pFinFETs after a HP2 anneal at 400 ºC.

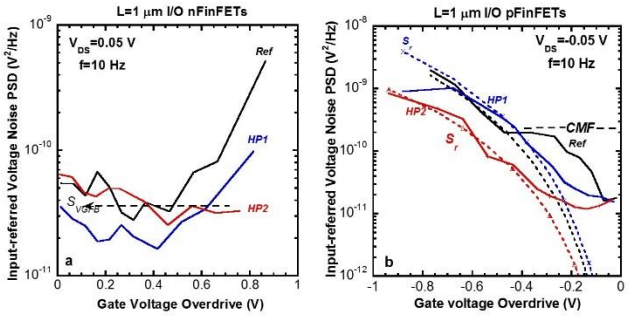

Fig. 4. Input-referred voltage noise PSD at f=10 Hz and in linear operation at $|V_{DS}|$=0.05 V of 1 µm long n- (a) and p-channel (b) FinFETs, without HP annealing (ref), HP1 and HP2. The dashed lines in (b) represent the series resistance related noise PSD.

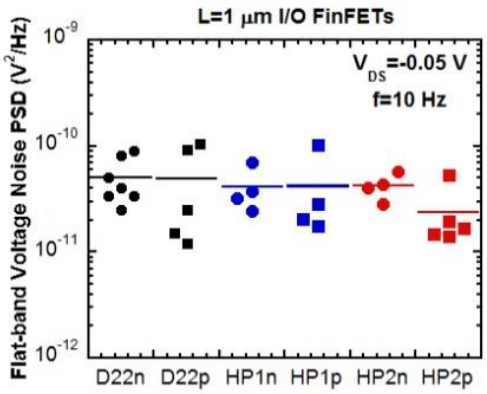

Fig. 5. Flat-band voltage noise PSD at 10 Hz and linear operation for 1 µm I/O n- and pFinFETs without annealing, after HP1 at 450˚C and HP2 at 400˚C.

B. I/O Si/Si$_{0.70}$Ge$_{0.30}$ superlattice FinFETs

The input I_D-V_{GS} characteristics of 1.8 V superlattice I/O FinFETs are shown in Fig. 6a for n- and p-channel devices [4]. There is a good electrostatic control with I_{on} >1200 µA/um and for the pFETs the SS = 69 mV/dec and DIBL = 30 mV/V [4]. The gate voltage noise PSD (experimental and model) is shown in Fig. 6b. for two devices [9]. The developed noise model is based on [14]

$$S_{v_g}(f) = B_w + \frac{K_f}{f^{\gamma}} + \sum_{i=0}^{N} \frac{A_i}{1+\left(\frac{f}{f_{0i}}\right)^2} \qquad (3)$$

with as noise components the 1/f noise (noted K_f), the generation-recombination Lorentzians with corner frequency (f_{oi}) and plateau value (A_{oi}) and the white noise B_w.

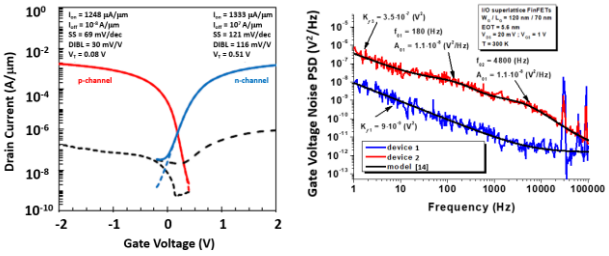

Fig. 6. Input I_D-V_{GS} characteristics for 1.8 V superlattice I/O n- and p-channel FinFETs (3 nm SiO_2 and 70 nm gate length) (a) [4], and gate voltage noise PSD for two devices (b). For device 1 the noise modeling only requires white noise and flicker noise, while device 2 also requires a Lorentzian generation-recombination noise component [9].

The trap density can be calculated using Eq. (1). It is important to remark that for the studied devices there is a correlation between the trap density and the inverse mobility of the devices as illustrated in Fig. 7 [9]. A similar trend has been reported before for e.g. HfO_2 nMOSFETs [15] and TiN/TaN/ HfO_2 Ge pMOSFETs [16] and was associated with the impact of the remote Coulomb scattering. Shorter devices lead to a more pronounced reduction of the mobility.

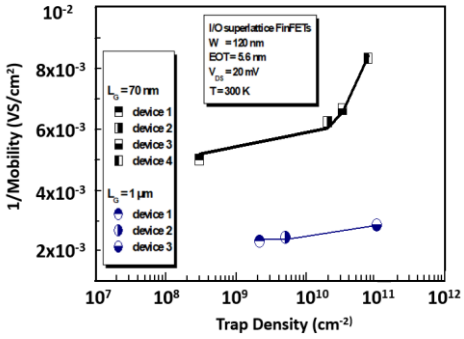

Fig. 7. Correlation between the trap density and the inverse of the carrier mobility for 70 nm superlattice I/O devices.

Using noise spectroscopy whereby the low frequency noise at a fixed polarization is studied as a function of the temperature enables to obtain more information on the nature of the traps by determining for each trap the energy level, the concentration and the capture cross section. The analysis includes the evolution of both the corner frequencies and the plateau values. Some typical results are illustrated in Fig. 8 resulting in four trapping levels, i.e., E_C-E_T = 0.45 eV (T1), E_C-E_T = 0.44 eV (T3), E_C-E_T = 0.42 eV (T2) and E_C-E_T = 0.17 eV (T4) [9]. These levels can be associated with V_2H, VP, $V_2^{(0/-)}$ and C_iC_S complexes, respectively. Further investigations are ongoing.

Similar as for the standard I/O bulk FinFETs discussed in the previous section it is interesting to analyze the flat-band noise PSD at 10 Hz as shown in Fig. 9. It can clearly be seen that the median value of the noise is only slightly increased for the superlattice FinFETs compared to the reference device architecture, although there is a higher spread in the data.

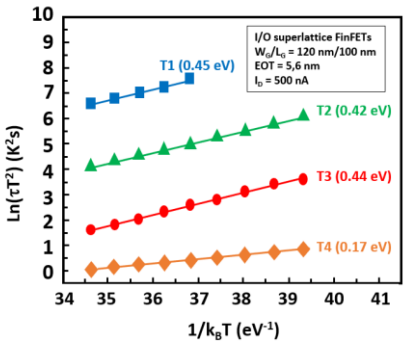

Fig. 8. Arrhenius diagram for the time constants of the GR noise component used to determine the activation energy of the trapping levels in superlattice devices [9].

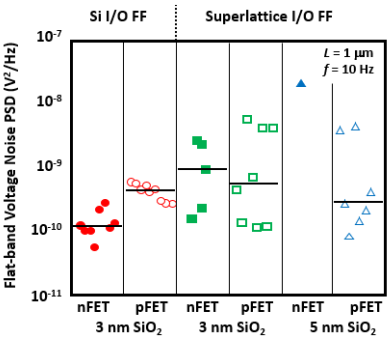

Fig. 9. Flat-band voltage noise PSD at 10 Hz and linear operation for standard and superlattice 1 µm I/O n- and pFinFETs. The horizontal solid lines are median values.

IV. Conclusions

It has been shown that the 1/*f* noise PSD of I/O pFinFETs with 3.5 nm ALD SiO_2 is significantly reduced after a post-deposition high-pressure deuterium anneal at 400 ºC. This is mainly related to the reduction of the series resistance noise. The n-channel counterparts show little impact of the HP annealing on the flat-band voltage noise PSD, while in strong inversion suppression of the access resistance noise could be found for some devices. For Si/SiGe superlattice devices the presence of traps in the depletion layer impacts the low frequency noise of Si/SiGe superlattice devices. Although there is a higher spread in the noise from device to device compared to standard I/O devices, there is only a limited impact on the median low-frequency noise values.

Acknowledgement

This work has been performed in the frame of the imec Core Partner program on Logic FinFET devices.

References

[1] C.-H. Jan, U. Bhattacharya, R. Brain, S.-J. Choi, G. Curello, G. Gupta, W. Hafez, M. Jang, M. Kang, K. Komeyli, T. Leo, N. Nidhi, L. Pan, J. Park, K. Phoa, A. Rahman, C. Staus, H. Tashiro, C. Tasi, P. Vandervoorn, L. Yang, J.-Y. Yeh, and P. Bai, "A 22nm SoC platform technology featuring 3-D tri-gate and high-*k*/metal gate, optimized for ultra low power, high performance and high density SoC applications," in *Tech. Dig. IEEE Int. Electron Devices Meeting – IEDM12*, pp. 44-47, Dec. 2012 DOI: 10.1109/IEDM.2012.6478969

[2] E. Simoen, G. hellings, B. Parvais, L.-A. Ragnarsson, H. Dekkers, T. Schram, D. Linten and N. Horiguchi, "Low-frequency noise assessment of 1.8 V input-output bulk FinFETs with ALD SiO_2," presented at *CSTIC 2018*, March 2018.

[3] H. Mertens, R. Ritzenthaler, H. Arimura, J. Franco, F. Sebaai, A. Hikavyy, B.J. Pawlak, V. Machkaoutsan, K. Devriendt, D. Tsvetanovam A.P. Milenin, L. Witters, A. Dangol, E. Vancoillie, H Bender, M. Baradoglu, F. Holsteyns, K. Barla, D. Mocuta, N. Horiguchi, and A.V-Y. Thean, "Si-cap-free SiGe p-channel FinFETs and gate-all-around transistors in a replacement metal gate process: Interface trap density reduction and performance improvement by high-pressure deuterium anneal," in *Tech. Dig. Symp. on VLSI Technology*, The IEEE New York, p. T142, 2017 DOI: 10.1109/VLSIT.7223654

[4] G. Hellings, H. Mertens, A. Subirats, E. Simoen, T. Schram, L.-A. Ragnarsson, M. Simicic, S.-H. Chen, B. Parvais, D. Boudier, B. Cretu, J. Machillot, V. Pena, S. Sun, N. Yoshida, N. Kim, A. Mocuta, D. Linten, and N. Horiguchi, "Si/SiGe superlattice I/O FinFETS in a vertically-stacked Gate-All-Around horizontal nanowire technology", in *Tech. Dig. Symp. on VLSI Technology*, The IEEE New York, p.p. 85-86, 2018, DOI: 10.1109/VLSIT.2018.8510654

[5] G. Ghibaudo and T. Boutchacha, "Electrical noise and RTS fluctuations in advanced CMOS devices," *Microelectron. Reliab.*, vol. 42, no. 4-5, pp. 573-582, May 2002. DOI: 10.1016/S0026-2714(02)00025-2

[6] E. Simoen, H.-C. Lin, A. Alian, G. Brammertz, C. Merckling, J. Mitard, and C. Claeys, "Border traps in Ge/III-V channel devices: Analysis and reliability aspects," *IEEE Trans. Device and Mater. Reliability*, vol. 13, no. 4, pp. 444-455, Dec. 2014 DOI: 10.1109/TDMR.2013.2275917

[7] R. Ritzenthaler, T. Schram, A. Spessot, C. Caillat, M. Cho, E. Simoen, M. Aoulaiche, J. Albert, S. Chew, K. Noh, Y. Son, P. Fazan, N. Horiguchi, and A. Thean, "Diffusion and gate replacement: A new gate first high-*k*/metal gate CMOS integration scheme for DRAM peripheral applications," *IEEE Trans. Electron Devices*, vol. 63, no. 1, pp. 265-271, Jan. 2016 DOI: 10.1109/TED.2015.2501721

[8] E. Simoen, R. Ritzenthaler, M.-J. Cho, T. Schram, N. Horiguchi, M. Aoulaiche, A. Spessot, P. Fazan, and C. Claeys, "Increase in oxide trap density due to the implementation of high-κ and Al_2O_3 cap layers in thick-oxide input-output transistors for DRAM applications," *ECS J Solid-St. Science and Technol.*, vol. 5, no. 6, pp. N27-N31, June 2016 DOI: 10.1149/2.0051606jss

[9] D. Boudier, B. Cretu, E. Simoen, G. Hellings, T. Schram, H. Mertens, and D. Linten, "Low frequency noise analysis on Si/SiGe superlattice I/O n-channel FinFETs", in *Proc. ULIS-EUROSOI 2019* (in press).

[10] G. Ghibaudo, O. Roux, Ch. Nguyen-Duc, F. Balestra, and J. Brini, "Improved analysis of low frequency noise in field-effect MOS transistors," *Phys. Status Solidi A*, vol. 174, no. 2, pp. 571-581, Apr. 1991 DOI: 10.1002/pssa.2211240225

[11] E. Vandamme, L.K.J. Vandamme, E. Simoen, R. Schreutelkamp, and C. Claeys, "The noise behaviour of silicided and non-silicided MOSFETs," *Solid-State Electron.*, vol. 38, no. 11, pp. 1893-1897, Dec. 1995 DOI: 10.1016/0038-1101(95)00011-H

[12] D. Boudier, B. Cretu, E. Simoen, R. Carin, A. Veloso, N. Collaert, and A. Thean, "Low frequency noise assessment in n- and p-channel sub-10 nm triple-gate FinFETs: Part II: Measurements and results," *Solid-State Electron.*, vol. 128, pp. 109-114, Feb. 2017 DOI: 10.1016/j.sse.2016.10.013.

[13] J.W. Lee, M.J. Cho, E. Simoen, R. Ritzenthaler, M. Togo, G. Boccardi, J. Mitard, L-Å. Ragnarsson, T. Chiarella, A. Veloso, N. Horiguchi, A. Thean, and G. Groeseneken, "1/*f* noise analysis of replacement metal gate bulk p-type fin field effect transistor," *Appl. Phys. Lett.*, vol. 102, p. 073503/1-3, Feb. 2013 DOI: 10.1063/1.4793306

[14] H. Achour, B. Cretu, E. Simoen, J.-M. Routoure, R. Carin, A. Benfdila, M. Aoulaiche, and C. Claeys, "Identification of Si film traps in p-channel SOI FinFETs using low temperature noise spectroscopy," *Solid-State Electron.*, vol. 112, no. 11, pp 1-6, 2015 DOI: 10.1016/j.sse.2015.02.014.

[15] E. Simoen, A. Mercha, C. Claeys, and E. Young, "Correlation between the 1/*f* noise parameters and the low-field mobility in HfO_2 gate dielectric n-channel metal–oxide–semiconductor field-effect transistors," *Appl. Phys. Lett.*, 2004, vol, 85, pp 1057-1059, 2004 DOI: 10.1063/1.1779967

[16] W. Guo, G. Nicholas, B. Kaczer, R.M. Todi, B. De Jaegger, C. Claeys. A. Mercha, E. Simoen, B. Cretu, J.-M. Routoure, and R. Carin, "Low-frequency noise assessment of silicon passivated Ge pMOSFETs with TiN/TaN/ HfO_2 gate stack," *IEEE Electron Device Lett.*, vol. 28, no. 4, pp 288-291, April 2017 DOI: 10.1109/LED.2007.891797