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**Master Thesis**

**(Confidential)**

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# **Development of a Monolithic Fiber- Based Electric Field Sensor**

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# Abstract

This project has been done on the development of a monolithic fiber-based electric field sensor, with a focus on establishing a reliable, cost-effective, and scalable production cycle to be implemented initially at a pilot and consequently at an industrial scale. The small scale and the low cost of these electrically passive sensors would enable their application where applying an external electric current is either forbidden (e.g. by the ATEX directive), or would distort the electric field and thus limit the possibility of monitoring sensitive assets. This electric field sensor works on the principles of electrostatic induction and translates the electric field to the displacement of an array of mirrors and holes suspended over a second array of mirrors. By shining the rays of light onto the suspended array, it would be possible to monitor the variations of the reflected light due to the displacement of the suspended array over the second array which is deposited on a transparent substrate.

At the first phase of the project, by utilizing the COMSOL Multiphysics simulation software, the optimal parameters of the electric sensor were simulated. Based on the results of the simulations, a general process flow was drafted and received the approval from the experts at the EPFL Center of Micro/Nano Technology (CMi). Based on the finite element simulations, in order to maximize the displacement of the sensor along the electric field, it has been shown that reducing the thickness of the sensor would significantly increase the longitudinal displacement of the sensor. Additionally, in order to further decrease the stiffness of the springs connecting the suspended mass to the frames, the structural material of the sensor was selected to be Copper, which also has a high electrical permittivity and low fabrication cost.

Next, the micro fabrications based on the optimized design and the process flow were carried out at the CMi ISO 5 cleanroom facilities. In order to adapt the process flows to the capabilities and the availability of the machines, several process flows have been tested and the result of which have all been documented in this report. Moreover, regarding the limited range of the available choices for having a process flow which is compatible with the CMi facilities, the recommendations for further simplifying the process and decreasing the final production costs are mentioned in this report.

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# Chapter 1 Introduction

In the everyday life, there are various machines valuable assets which are continuously monitored and protected by means of electric field sensors(1). Several industries benefit from the advantages of utilizing electric field sensors to regulate the adverse effects of accumulated charges, or to analyze the sensed signals and extract valuable information from the generated data. Some of the most important applications of the electric field sensors are in the measurement of(1–3):

- The surface charge on the sensitive assets at the vicinity of electronic equipment to avoid accidental arcing (1)
- The possibility and potential of lightning which would hit vital assets or buildings(4)
- Electric fields under the high-voltage power lines and the evaluation of their electromagnetic effects on the humans and nearby living entities (3)
- Electric fields originating from the brain activity by means of electrocardiogram (ECG) and electroencephalogram (EEG) sensors (3)

Devices which function as electrometers work either by reporting the voltage measured compared to a ground reference, or by expressing it in volts per distance(2).

In order to evaluate the current technologies behind the different types of electric field sensors, a market research has been done for this project.

## 1.1 Market Research

For the measurement of the electric field for different applications such as the examples mentioned in the previous part, there are in general three main types of electric field sensors; Induction Probes, Field Mills (and other oscillating plate sensors), and Optical Probes which function based on the Pockel's effect.

In the following section, the general overview of these sensors and their attributes are explained.

### 1.1.1 Induction Probes:

When utilizing an induction probe, the principal mechanism of sensing is by putting a conductive probe at the vicinity of an electric field and allowing it to equilibrate with the local field and then measuring the potential in the manner shown in Figure 1.a.

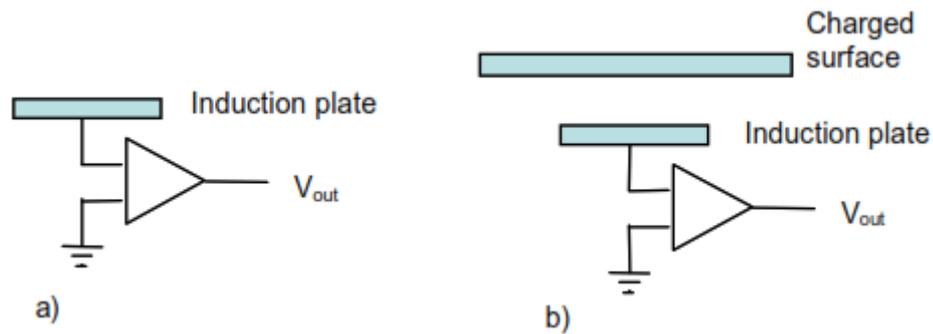


Figure 1: Schematic representation of a) an induction plate sensor for the detection of an electric field and b) a surface charge meter (2).

Moreover, induction probes are sometimes used as surface charge meters. As can be seen in Figure 1.b, in these sensors, there are two plates which function as the two parallel plates of a capacitance. By measuring the potential of the induction plate and the surface charge for a given distance, the potential of the charged surface would be deduced. In different values for the distance, the capacitance of this scheme would vary according to the formula  $C = \epsilon \cdot A / d$  where  $\epsilon$  would be the permittivity of air,  $A$  the surface area of the induction plate, and  $d$  the distance between the charged surface of interest and the induction plate. By calibrating the sensor for different distances, it would be possible to measure the surface charges by simply adjusting the sensor for the measurement (2).

Although Induction Probe sensors are cheap, there are several drawbacks which highly limit their application in the measurement of the electric fields in the industry. The main issues are the requirement to be re-zeroed after each measurement which completely shadows the possibility of using them as an electric field “monitoring” device. Second, they are highly susceptible to the ambient space charges which skew the results of the sensing. And third, being grounded for the measurement of the electric field leads to the distortion of the field and hence highly limits its application for measuring the strength of the electric fields with low value without distorting them(2,5).

### 1.1.2 Field Mills and Sensors with Oscillating Plates:

The second technique for measuring the direct current (DC) electric fields is by creating a pseudo-alternative current (AC) by means of either spinning a shutter over the plate of a measuring capacitor similar to the induction probes, or by oscillating one of the two parallel plates of a capacitor, either in MEMS scale or larger scales. The schematic of such shuttered electric field sensors is presented in Figure 2. The DC to AC conversion in the field mills considerably reduces the effects of the ambient space charges(2).

Despite the fact that field mills are more sensitive than induction probes and do not require frequent re-zeroing, the issue with these type of sensor is that they are more complex, more expensive, and bulkier than the induction probes(2). Furthermore, they have a grounded shutter which would distort the electric field.

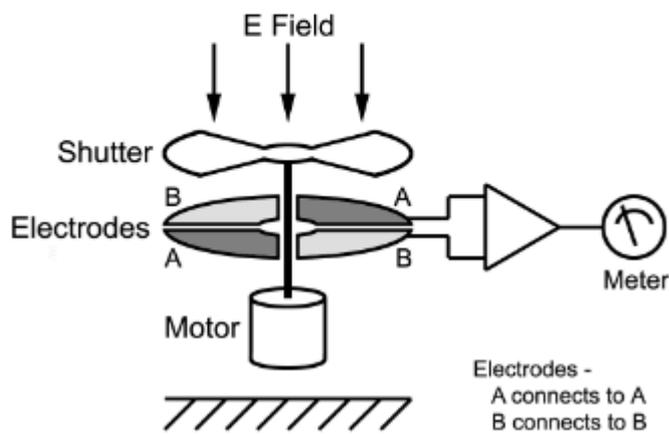


Figure 2: Representation of the shuttered field mill sensors (6,7)

Concerning the size of these sensors which usually exceeds a diameter of 10 centimeters, most of the field mill sensors are used for the detection of the possibility of lightning nearby the vital assets or for measuring the electric field at the vicinity of power lines to study their effects on the humans(1,2).

Nonetheless, by utilizing the concept of these sensors and translating them to the MEMS scale through utilizing oscillating plates which convert DC to pseudo AC, it has been possible to achieve functional electric field sensors. However, the transduction and readout mechanism used in these commercially available sensors leads to a low resolution of 200 V/m. By utilizing more efficient readout methods such as optical displacement measurement, it would be possible to not only avoid the distortion of the field due to the connection of the sensor to the ground, but also to have considerably higher resolutions for field detection(5).

### 1.1.3 Optical Probes (Pockel's effect)

As mentioned for the Induction Probes and the Field Mills, having a grounded metallic sensor plate distorts the electric field and limits their application where it is of importance not to disturb the field. However, what makes optical probes an interesting alternative is that these sensors do not distort the electric field (2,5). Most often these sensors work based on the Pockel's effect, by which the birefringent properties of a crystal change in the presence of an electric field and these changes in the optical properties of the material can be monitored. It has been shown that crystals based on Bismuth germanate ( $\text{Bi}_4\text{Ge}_3\text{O}_{12}$ ) and Lithium niobate ( $\text{LiNbO}_3$ ) can detect DC fields down to 10kV/m with a resolution of 100V/m (8,9). A schematic of the Optical Probes based on Pockel's effect is depicted in Figure 3.

Although these sensors do not suffer from the drawback of affecting the electric field, they are limited to detecting electric fields stronger than 10,000 V/m. Moreover, the resolution for these sensors deteriorates in low frequencies and they only perform well in AC fields. Furthermore, this kind of electro-optical field measurement sensors is prone to temperature instabilities caused by pyro-electric phenomena which lead to the thermal expansion of the crystal(5).

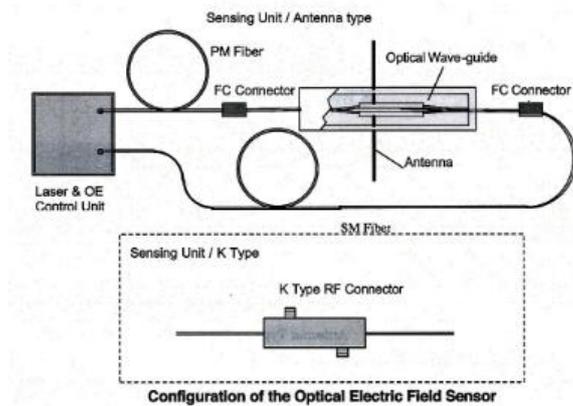


Figure 3: Schematic representation of optical probes based on Pockel's effect(2).

Based on the above market research, it has been realized that currently there is a gap in the market for MEMS scale electric sensors which do not distort the electric field while being able to measure fields of 1kV/m.

## 1.2 Objectives and Structure of this Thesis

The objective of this thesis has been to design, simulate, and fabricate a monolithic fiber-based electric field sensor at the MEMS scale. This has been an endeavor to fill in the gap among the commercially available electric field sensors, which cannot currently measure electric fields below 10kV/m without distorting the field (2). In this regard, an electrically passive sensor with a fiber-based readout has been designed which works on the principles of electrostatic induction. Such an optical sensor would enable achieving important criteria which are key to providing the final product with a competitive advantage in the market:

- Distortion-free measurement of electric field
- EMI<sup>1</sup>/RFI<sup>2</sup>, and ATEX<sup>3</sup> compatible (for the explosive environment)
- Low loss over long-distance monitoring
- Electrically passive sensor
- MEMS-scale
- Low-cost and mass-producible

In this project, after drawing the 3D CAD model of the sensor, the first phase of Multi-physics simulations have been run before starting the fabrications. Next, after designing the general process flow and starting the fabrications, the second phase of the simulations was also run in order to reiterate on the design and optimize the parameters. Thus, this thesis is organized as follows:

<sup>1</sup> Electromagnetic Interference

<sup>2</sup> Radio-Frequency Interference

<sup>3</sup> Appareils destinés à être utilisés en **AT**mosphères **EX**plosible

In chapter 2, the physics behind the proposed electric field sensor will be described, in order to show how the transduction scheme would work in practice and what are the main elements of such a sensor. Then, the 3D CAD model which has been designed based on the physics involved is explained.

Next, in chapter 3 the simulations know-how and the effect of different parameters on the displacement of the sensing mass is clarified. It should be noted that this information have been simultaneously used alongside the fabrication step in this project.

In chapter 4, the general process flow and the fabrication steps are described step-by-step and in details in order to render this work reproducible. The descriptions of the steps and trials are in chronologic order in the same way as they evolved throughout the project so that readers can understand the rationale behind the technical decisions which have been made.

In the last chapter, the achievements, conclusions and the next steps are provided for the continuation of this project and increasing the production efficiency while decreasing the fabrication costs.



# Chapter 2 Transduction Scheme and Design

In this chapter, first the physics behind the proposed electric field sensor is described, in order to show how the transduction scheme would work in practice and what are the main elements of such a sensor. Then, the 3D CAD model which has been designed based on the physics involved, is explained.

## 2.1 Transduction Scheme

The chosen transduction scheme inspired by the work of A. Kainz et. al. (5), is a solution to the aforementioned shortcomings of electric field sensors, in terms of size, price, detection range, and resolution. This method utilizes the electrostatic induction caused by the mobility of the electrostatic charges inside conductive materials situated in an electric field. Considering a conductive sphere in an electric field, such as the one depicted in Figure 4, the electrostatic induction leads to the decoupling of the charges in the sphere. This decoupling and accumulation of the charges on opposing sides of the surface of the sphere lead to the generation of equal but opposing attractive electrostatic forces applied by the electric field which render the total force on the sphere to be zero.

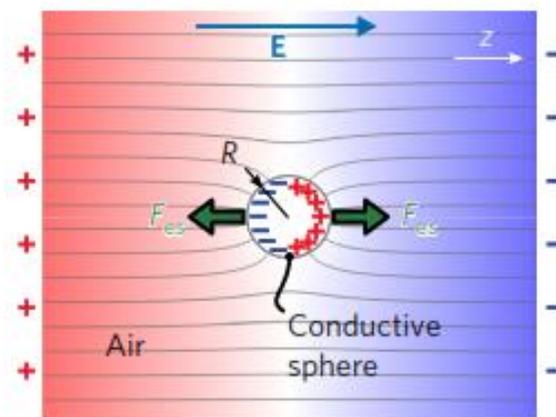


Figure 4: Schematic of a conductive sphere with the radius  $R$  placed inside an electric field  $E$  (5). The decoupling of the charges on the sphere lead to the generation of equal but opposing attractive electrostatic forces  $F_{es}$  applied to them by the electric field.

Now, considering that the material can stretch along the direction of the electric field ( $z$  direction in Figure 4), the variations of the electric field would be translated into displacement and elongation of the matter. This phenomenon can be also modeled by having two conductive plates as shown in Figure 5, which are connected together through a conductive spring. In this scenario, the conductive spring would elongate due to the electrostatic forces which are stretching it at opposing directions along the electric field.

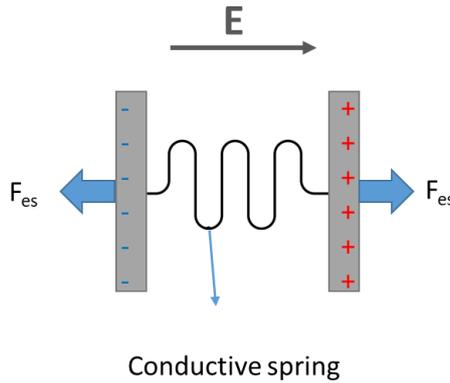


Figure 5: Schematic of a conductive object inside an electric field wherein the two oppositely charged surfaces are represented by two parallel plates connected together through a conductive spring. This setup allows the decoupling of the charges and their accumulation on two different plates enabling the spring to be stretched by the opposing two  $F_{es}$  forces applied to its ends.

Through such setup, one can measure the elongation of the spring and observe the correlation that exists between the changes in the length of the conductive spring and the strength of the electric field.

Based on the analytical solutions, the electrostatic force applied to each of these plates can be obtained through the following equation(10):

$$F_{es} = \epsilon \frac{A}{2} \cdot E^2$$

Where  $\epsilon$  is the relative permittivity of air,  $A$  is the surface area onto which the force is being applied, and  $E$  is the electric field.

In the next section, the 3D design based on this physical phenomenon is explained.

## 2.2 Design

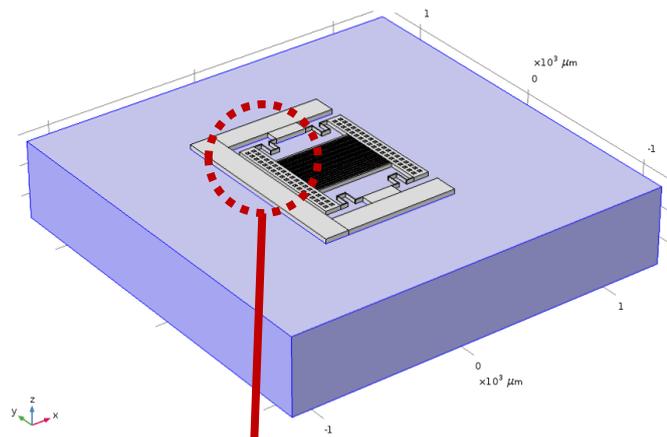
The initial design based on the transduction scheme introduced in the previous section is depicted in Figure 6 which is obtained via the internal CAD feature of COMSOL. What is shown, is the 3D design of the electric field sensor which is situated on top of a glass substrate. Figure 6..a shows that the sensor with a thickness of 25um is situated on a glass substrate with a thickness of 500um. Figure 6..b shows a higher magnification of the device, depicting how the springs and the array of the mirrors and holes would be suspended above the substrate while being connected to the frames. Figure 6..c shows an imaginary representation of how charges would redistribute in such a device.

This design enables the sensor to be electrically isolated and not connected to the ground. Furthermore, the left and right-hand sides of the device function as though they are the two parallel plates shown in Figure 5 over which the charges would accumulate. These two regions are connected together through the 4 meanders that hold the freely oscillating central mass suspended above the substrate.

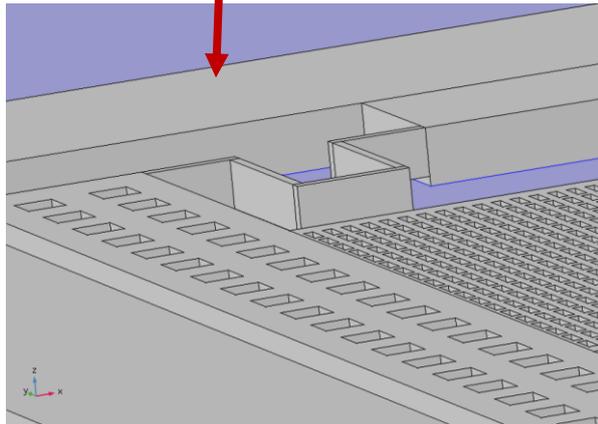
The larger holes on the sides of the central mass are designed to reduce the time for the release process, as they decrease the total undercut required to etch the sacrificial layer underneath the oscillating mass.

The array of the small holes are designed to let Aluminum be deposited at the last fabrication step on the surface of the substrate and hence lead to the formation of another array of mirrors. Hence, when the suspended array is not displaced by the presence of the electric field, all of the light which is shed on the sensor from the top along the z-axis would reflect back; as rays of light which go inside the holes hit the array of mirrors which are deposited on the surface, and the rays of light which do not go through the holes, get reflected back by the suspended mirror.

a)



b)



c)

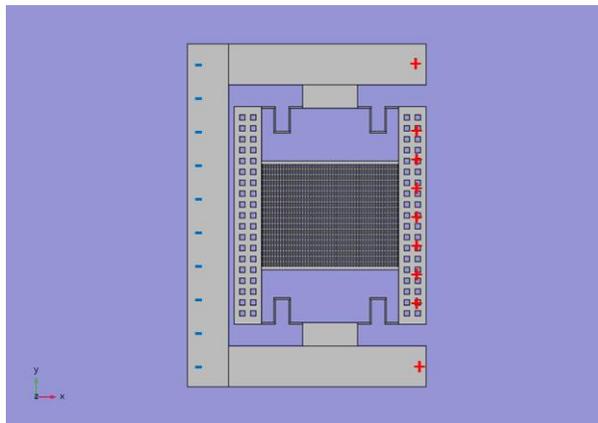


Figure 6: 3D design of the electric field sensor. a) The sensor in this picture is 5μm on a glass substrate with a thickness of 500μm. b) Higher magnification shows how the springs and the array of the mirrors and holes would be suspended above the substrate while being connected to the frames. c) Top view of the sensor and the imaginary redistribution of the charges on the different parts of the sensor



# Chapter 3 Simulations and the Refined Design

For the simulations of this project, COMSOL Multi-Physics software has been used. In this chapter, first the steps and challenges of building such a model are described, and next, the results and effects of modifying various parameters are presented.

Furthermore, the simulations throughout this project have been done in two different phases. The first phase which took place at the beginning of the project, was completely prior to starting any fabrication and mainly to give an understanding of the phenomena which would happen in such a setup. At this phase, the simulations were done in separate physics of the software and not in Multi-physics mode due to the complexity of a multi-physics model and the required time to tackle the corresponding challenges. The most important result of this series of simulations was to show effect of adding an extra antenna (called Bar in this report) in substantially amplifying the electric field in the distance (called Gap in this report) between the antenna and the initially designed sensor.

## 3.1 COMSOL Simulation Software

COMSOL Multi-Physics software is one of the most power simulation tools for modeling scenarios wherein different physics affect the model of interest at the same time. For this software, regardless of the type of the problem which should be solved, the order of building the model stays the same. In the following section, each of these steps and the difficulties faced for each during the simulations are explained.

### 3.1.1 Geometry

The first step for the COMSOL simulations is to have the CAD file of the design, which can be imported or be built by COMSOL itself. Regarding the need for having a parameterized design which can automatically update the dependent structural variable in the case of running sweeps on independent variables, it was decided to make the model with COMSOL's own CAD feature.

Regarding the presence of approximately 3,000 structural features in the CAD design which was presented in Figure 6, the first step in inputting the geometry of the model inside COMSOL was to simplify the CAD file by applying the following modifications on the design:

- Replacing the array of holes on the suspended mass by the same volume of a hole at the center of the model
- Replacing the meanders by the beams with relatively equal stiffness values
- Removing the substrate from the model
- Adding a cuboid of air around the sensor which would, later on, have the ground and an electric potential applied to two of its parallel faces

Without simplifying the model, it would have been impossible to run the multi-physics simulation with the available amount of resources, both in terms of the computational power and time.

Moreover, for the parameters of the Geometry, all of those parameters which were of interest to be studied and especially to be swept, were defined as independent, and all of the other parameters are automatically updated in case the independent values change.

In addition, for the simplicity of referring to the different parts of the model, each section is named to help the audience understand the utilized terms. The legend of these terms can be found in Figure 7.

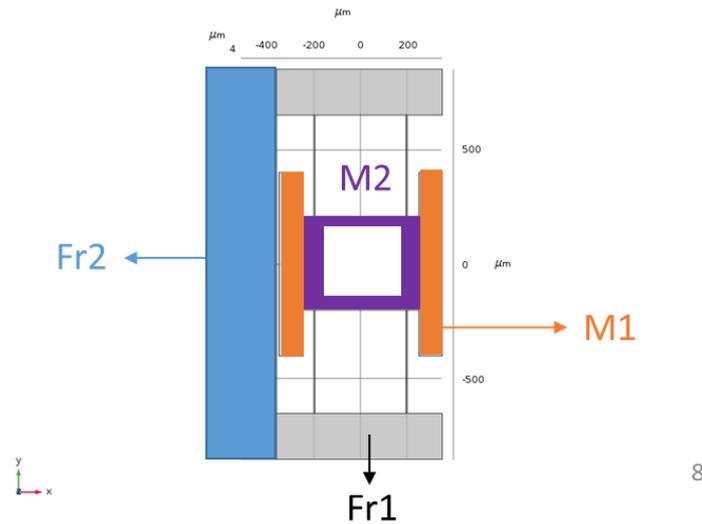


Figure 7: The legend for the utilized terms for different sections of the structure.

### 3.1.2 Materials

In order to simulate the presence of an electric field around the sensor, its structure should be surrounded by a cuboid of air, on sides of which the ground and an electric potential would be applied as can be seen in Figure 8. The material of the cuboid is chosen to be air, and the materials of the sensor is chosen to be Copper. It should be noted that the software requires the value for the relative permittivity of Copper and since it is a conductive material, it is best to define the copper parts as no conduction loss.

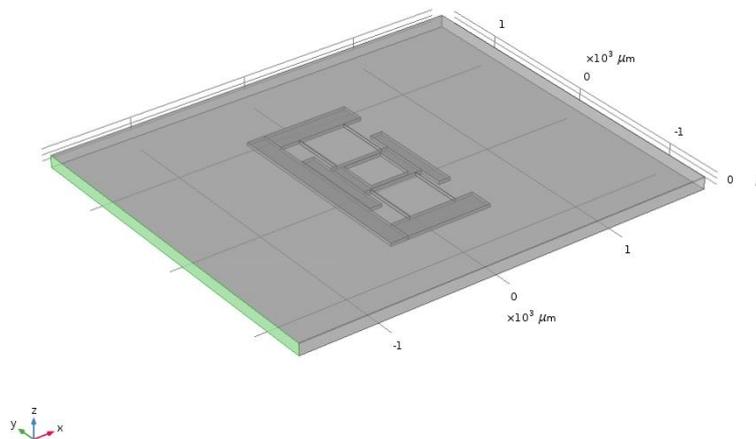


Figure 8: Representation of how a cuboid of air is surrounding the sensor. The green side of the cuboid is where the electric potential would be applied and the other side of the cube parallel this one would be grounded.

### 3.1.3 Meshing

One of the most important and challenging parts of simulating complex geometries with high aspect ratios is the meshing step. There are two approaches that can be taken in order to mesh the design; using COMSOL built-in physics-controlled meshing, or having a user-defined meshing. In most of the cases where the model is not complex or does not have very high aspect ratios, the physics-controlled meshing is the fastest and easiest option to take which by using the error estimation and mesh re-initialization feature of COMSOL leads to very good results. However, choosing this option for the model made in this project did not lead to successful results. The reason for this issue has been the default size of the meshing elements which should be chosen. If the chosen element size is large to match the large volume of the cuboid, then it would not match the thin structure of the sensor. On the other hand, if the chosen element size is very fine to successfully cover the structure of the sensor, then filling the cuboid would require a highly large number of elements and the multi-physics simulations would not lead to results with the available amount of resources in terms of the computational power and time. In fig the physics-controlled meshing and a user-defined mapped mesh is shown.

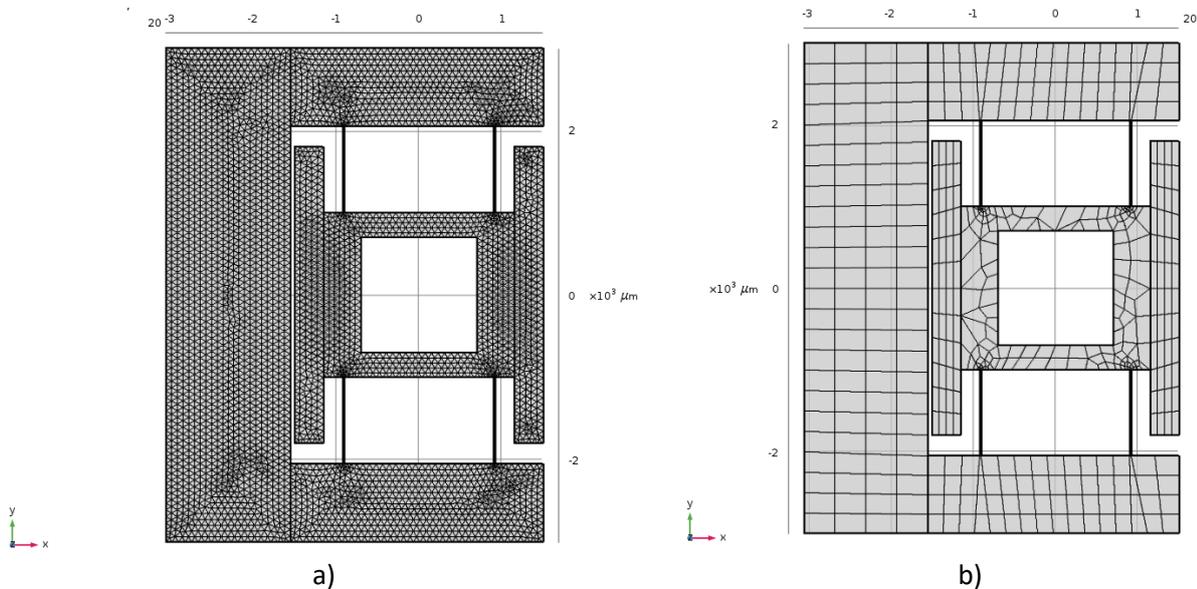


Figure 9: Meshing of the sensor (cuboid is hidden for the purpose of visibility) in COMSOL. a) physics-controlled mesh versus b) an example of a user-defined mesh.

Hence, the meshing should have been user-defined in this project. Moreover, by choosing different element sizes, for different parts, if the size difference is large, then the software would not be able to match the interfaces. Furthermore, in the case of having low quality meshing, the result of the simulations especially after running sweeps on a certain parameter would have a great deal of variations and do not show a clear trend.

In addition, after the first phase of running the simulations, as mentioned earlier in this report, a redefinition of the design took place which led to the addition of an antenna on the right-hand side of the sensor to amplify the electric field. For the region between this added antenna in the redefined design, and the central mass of the sensor which stays untouched from the initial design (this region is called Gap in this report), the meshing should have been different. Due to the size of this Gap which was chosen to be 5 microns for the

second phase of the simulations as well as the fabrications, the only element size that could fit the gap was the “Extremely fine” option, while it was previously filled up by the elements of the air region, which were defined by the cuboid. In order to solve this issue of the mismatch between the element sizes, an additional air volume was designed to fill in the Gap with the finest element size, and to allow the other regions in its vicinity to adapt their meshing to the Gap, by only choosing one or maximum two degrees of larger elements. The results of this redefined design and the meshing are presented in the next section.

### 3.1.4 Electromechanical Module

In order to assign the physics to this model in COMSOL, the two physics of Electrostatics and Solid Mechanics should be utilized, alongside the Electromechanical module which connects these two physics together. The main options which have been chosen for the physics of this model are listed below:

- Electric potential and the ground are applied onto the sidewalls of the cuboid
- The frames of the sensor are fixed from the bottom as the substrate is excluded from the model for the sake of simplification
- Floating potentials on the regions where the charges are supposed to freely move and decouple, being the sensor and the antenna which has been added at the next steps throughout the project
- Assigning the air volumes to be deforming domains, so that their meshing can deform as the suspended mass of the sensor moves

By implementing these choices, the model would be ready to be simulated. The results of the simulations are explained in the next two sections of this report.

## 3.2 Simulations of the First Design

At the beginning of the project, considering the difficulties in running the multi-physics simulations successfully, the electrostatics module was analyzed first to troubleshoot and refine the design. Running the simulations with the aforementioned settings and parameters, the potential distribution and electric field in different regions of the model were analyzed. Based on the findings at this stage

For the distribution of the electric potential in the model, as can be seen in Figure 10 the electric potential inside the cuboid and the sensor is plotted.

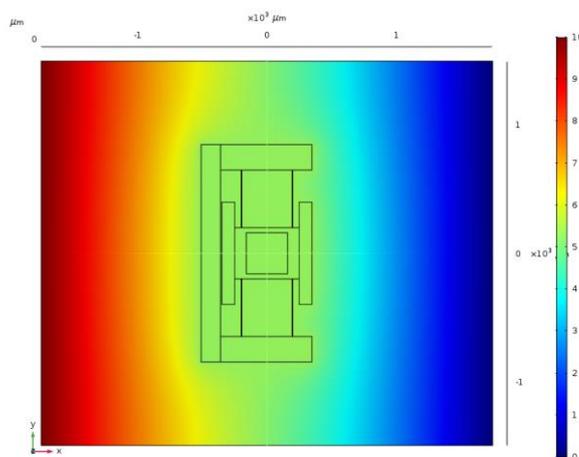


Figure 10: The plot of the electric potential inside the cuboid and the sensor. The sensor has a constant voltage in its entirety as the material is conductive and free movement of charges equilibrates the difference in potentials.

What is shown is that by putting the sensor inside an electric field, which is generated by applying a 10V potential to one side of the cuboid and the ground terminal to the other parallel side, the sensor has a constant voltage in its entirety. This is due to the fact that as the material is Copper and is conductive, the free movement of charges equilibrates the differences in the potential inside of it.

Additionally, in order to completely visualize the physics behind the transduction scheme, the surface charge density distribution plot has been presented in Figure 11.

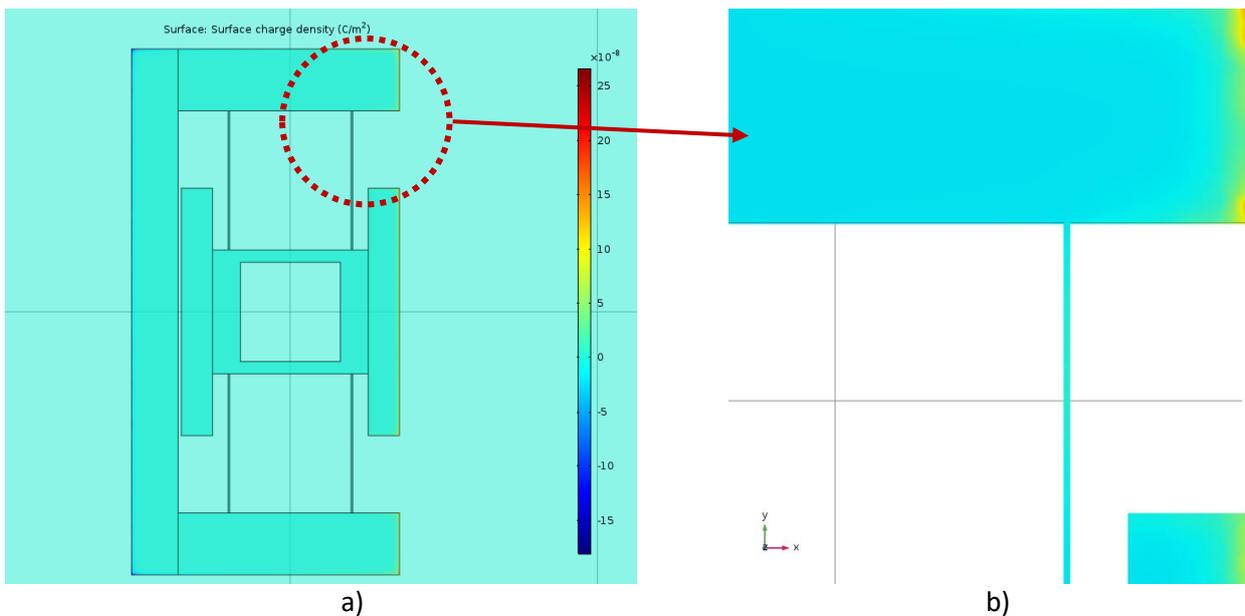


Figure 11: a) The surface charge density distribution plot which confirms the theory behind the previously introduced transduction scheme b) higher magnification of the edges and the beam showcasing the edge effects

As can be seen in Figure 11, the charges are distributed exactly as predicted by theory except the fact that at the corners due to the edge effect the charge density is higher.

Moreover, in order to visualize the electric field and its interaction with the sensor, by defining an XY-Cut Plane through the middle of the thickness of the model, it has been possible to successfully plot the electric field in these regions as it has been shown in Figure 12.

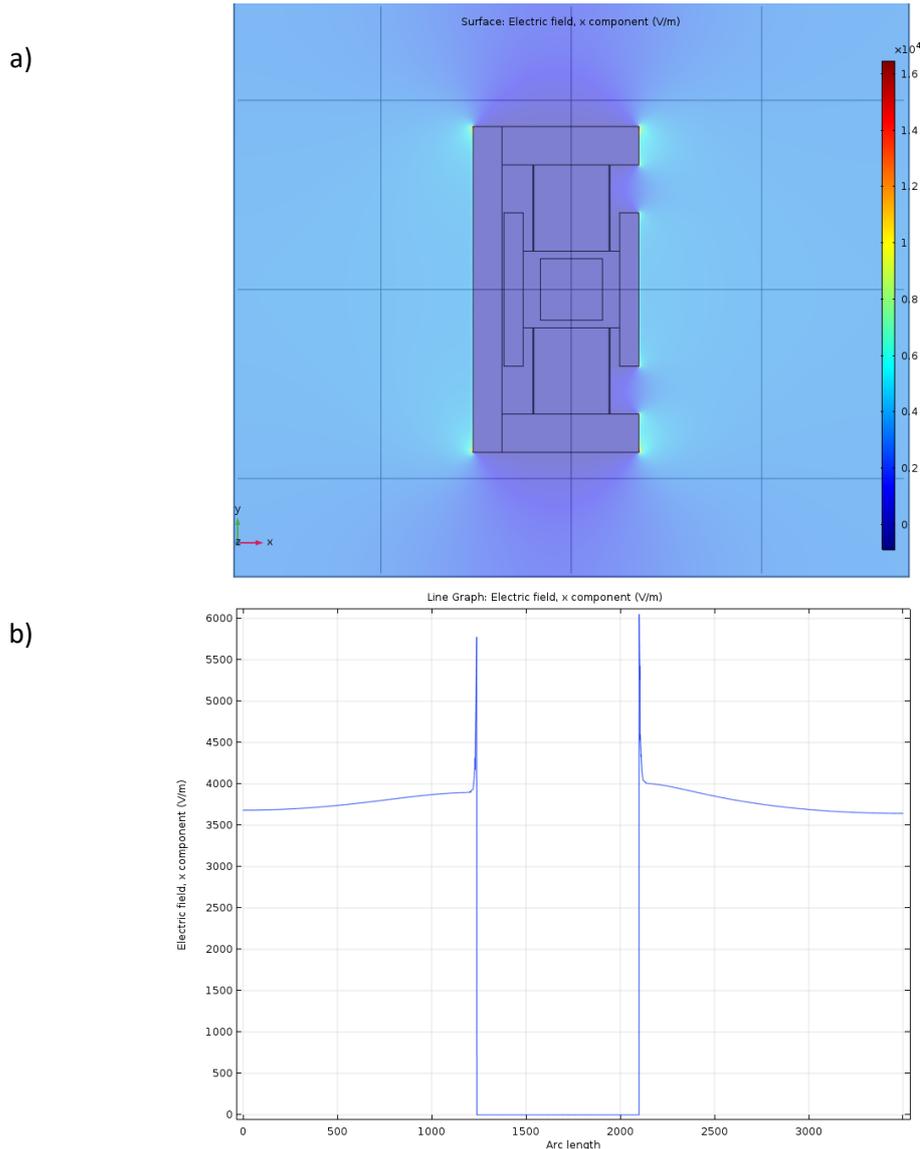


Figure 12: Electrostatic simulation of the model showing: a) the surface electric field on an imaginary XY-Cut Plane which goes through the middle of the thickness of the model b) The electric field on an imaginary x-axis Cut Line in XY plane going through the middle of the model.

As was previously predicted, inside the sensor due to its conductivity the electric field is zero, while on the left and right-hand side of the sensor, and especially at the corners, the charges have the highest density and hence the maximum electric field is observed. By applying a  $\Delta V=10V$  potential difference between the two sides of the cuboid, the electric field inside the cuboid calculated from  $E=\Delta V/d$  where  $d$  is the distance between the two sides, gives a leads to a value of  $2.8kV/m$ . However, looking at the values of the electric field, one observes that outside of the sensor, the average value is more than  $3,600 V/m$  which is clearly more than the value calculated in the absence of a metallic structure. The reason for this difference is merely the same as the scenario where a metallic plate is put between the plates of a capacitance. What happens in that case, is that if the plates are infinite in surface area, the model behaves as though the plates of the capacitance are brought closer together by an amount equal to the thickness of the intermediary plate. Hence, in this case, only an increase in the electric field at the vicinity of the sensor is observed and further from the sensor the electric field looks intact.

The second crucial point about these observations is the peak in the value of the electric field on the two surfaces of the sensor. This sharp increase is supposed to be caused by the edge effect at these positions. However, this would potentially describe the reason why placing an extra conductive plate closely on the right-hand side of the sensor (5) would amplify the electric field in this region.

Furthermore, in order to compute the relationship between the electrostatic force that is applied to the sensor and the strength of the electric field, the Force Calculation module in COMSOL was added and the results of this simulation are presented in Figure 13. As can be seen, the relationship is perfectly in accordance with the theory mentioned in the transduction scheme that  $F_{es} \propto E^2$ .

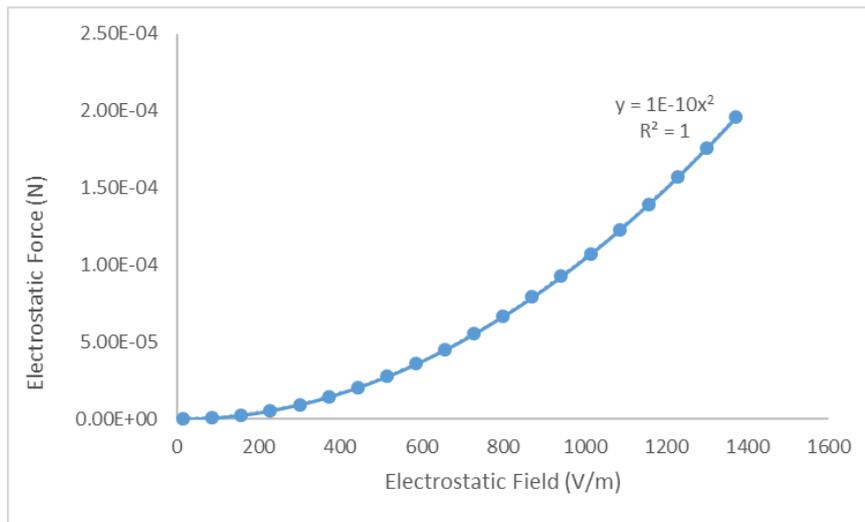


Figure 13: The applied electrostatic force to the sensor versus the electric field which confirms the quadratic relationship between  $F_{es}$  and  $E$ .

After the successful simulations utilizing only the electrostatic module, the multi-physics simulations for having both the electrostatic and solid mechanics modules were made possible. The first simulation which provided one of the most important pieces of information on the design, was the simulation of the thickness of the device and its effect on the displacement of the suspended mass. The result of such simulation for the model shown in Figure 12, are presented here in Figure 14.

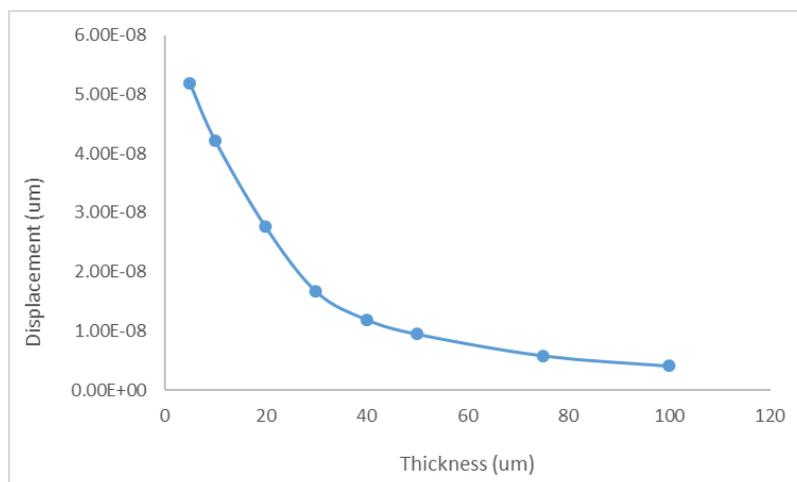


Figure 14: The changes in the displacement versus different values of the thickness of the device.

### 3.2.1 Conclusions of the Simulations on the First Design

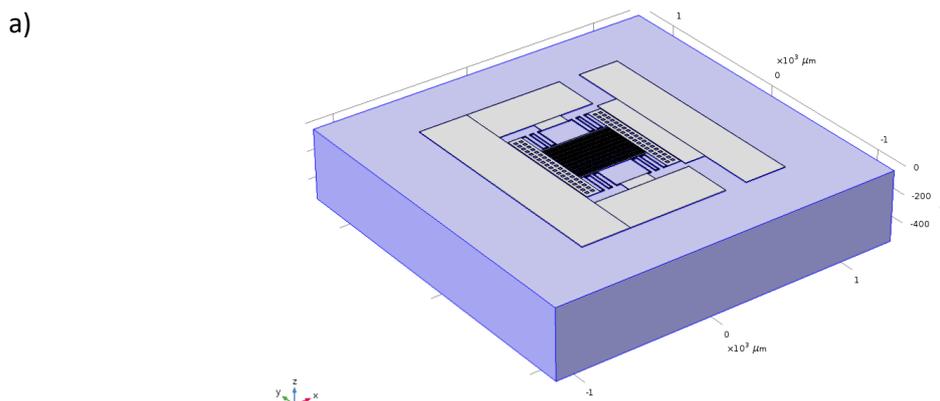
Based on the results obtained from the simulations on the first design, the following modifications were decided to be applied on the design and the model for simulations:

- The initial thoughts on the thickness of the sensor were influenced by the results presented in Figure 14 and hence the target thickness for the device was set to be below 5 $\mu\text{m}$ .
- It was decided to redo the simulations by adding an extra antenna on the right-hand side of the sensor which could potentially concentrate and amplify the electric field in the Gap between the sensor and the antenna.
- Although the simulations are run with beam instead of meanders, the number of meanders were doubled in series in order to decrease their stiffness for the main design.
- As mentioned previously for Figure 12, in order to have a higher electric field at the vicinity of the device, it was decided to test the simulations with the Frames and Bar (antenna) that increase the length of the device along the x-axis.

### 3.2.2 The Refined Design

Based on the above mentioned decisions, the model was modified for the second phase of the simulations and for the fabrication, in order to have a higher displacement when placed in an electric field. The model based on these changes can be seen in Figure 15.

As can be observed, the range of the thickness is considerably less than the previous model. Furthermore, the presence of two meanders at each side instead of only one can be seen. Moreover, the addition of the antenna and the formation of the Gap are visible in this Refined design. The model is also built in a way that the sweeping along the x-axis would be dynamically modifying the position of the other parts, which allows having the sweeps on the parameters along the electric field.



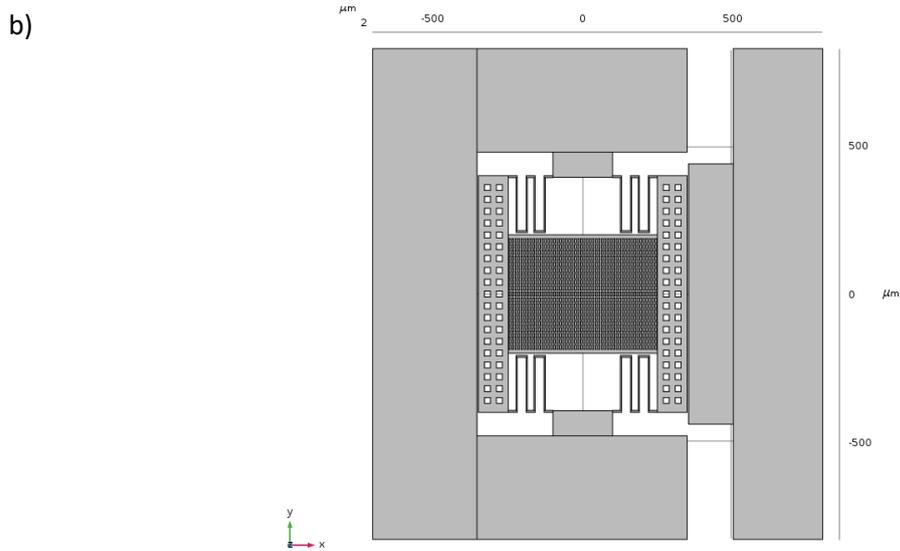


Figure 15: The refined design based on the conclusions from the first model. a) 3D view b) Top view. Addition of the Bar on the right and the formation of a Gap between it and the sensor, reduction of the thickness, widening of the frames along the x-axis, and increasing the number of meanders in series are new in this model.

### 3.3 Simulations of the Refined Design

There have been two main differences between the simulations of this Refined model and the previous model. First, the added antenna should have a fixed constraint from bottom as the boundary condition, as well as having the floating potential setting for the electrostatics module. Second, the meshing will no more be successfully done with the previous approach, as the meshed elements of air would only fill inside the Gap if the finest element size is chosen which would not be practical to assign to the whole cuboid due to the significant increase in the simulation time.

To solve the meshing issue, several user-defined mappings were tested. However, in order to have a mesh which can meet the needs of different aspect ratios while sweeping over the parameters, lacked the suitable matching of the interfaces. As explained in section 3.1.3 for the meshing, the solution for this problem proved to be adding an extra volume of air with the finest mesh element size inside this Gap, and to mesh the rest of the model as before. As can be seen in Figure 16 this meshing was successfully done with a high quality of elements.

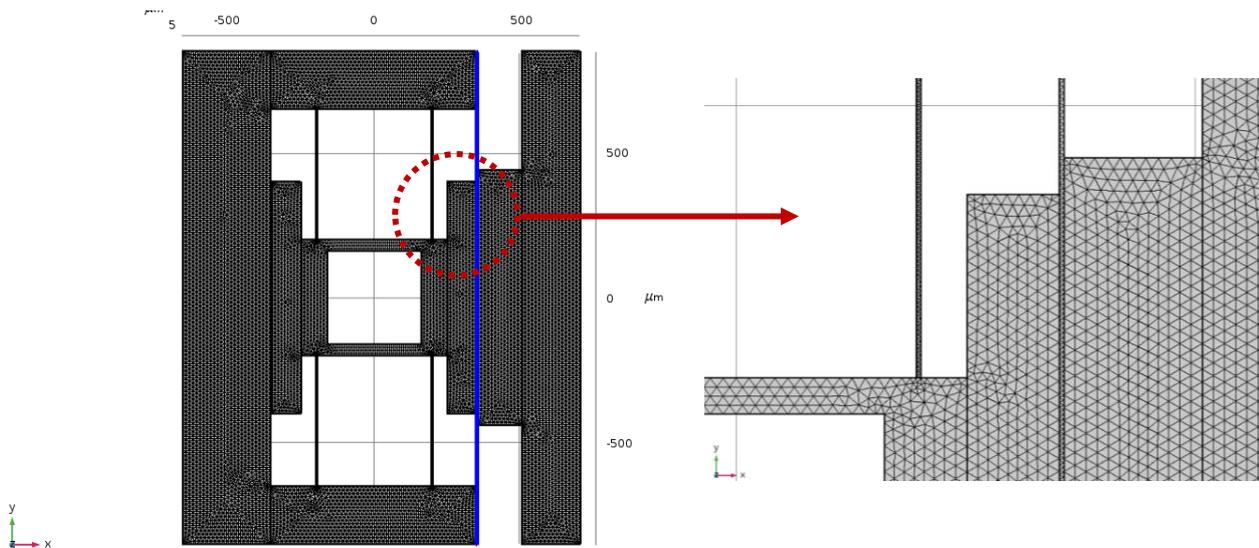


Figure 16: a) Top view of the solution to the meshing problem for the Refined model with a Gap area (blue) between the newly-added bar and the sensor. b) higher magnification of the Gap area which shows the difference in the size of the elements.

By having a reliable meshing which allowed running the swept simulations without errors, the effect of various parameters on this model were studied which are explained in the next section.

Furthermore, by running the simulations again for the visualization of the electric field and the surface charge density, the results presented in Figure 17 and Figure 18 can be observed.

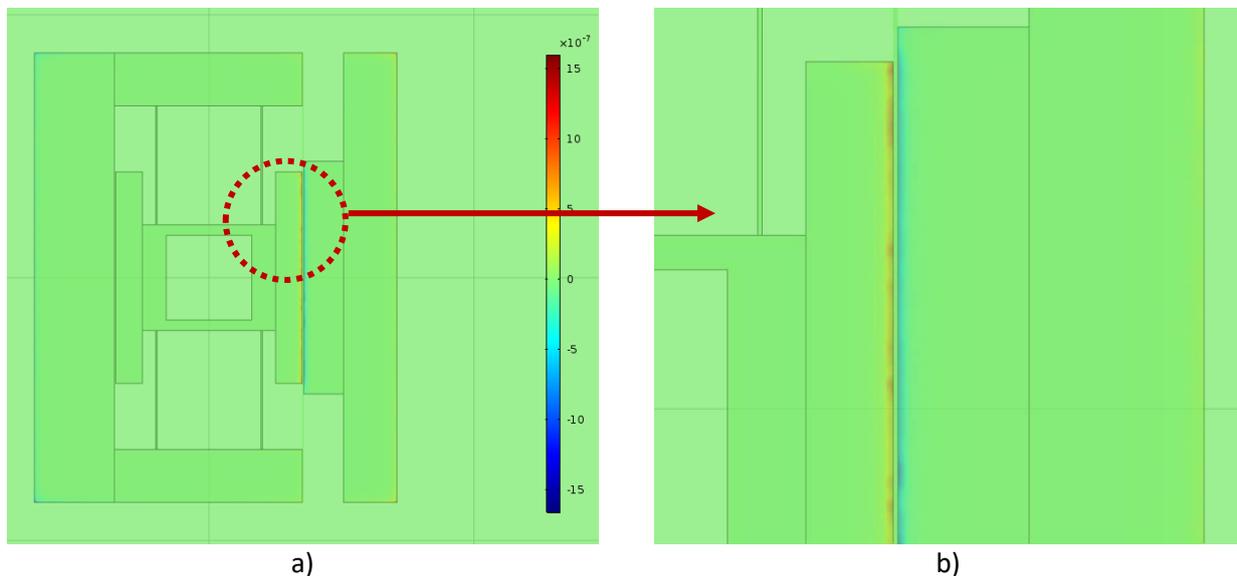


Figure 17: a) The surface charge density distribution plot which confirms the theory behind the previously introduced transduction scheme b) higher magnification of the edges and the beam showcasing the edge effects and the regions on the both sides of the gap which have a high density of accumulated charges

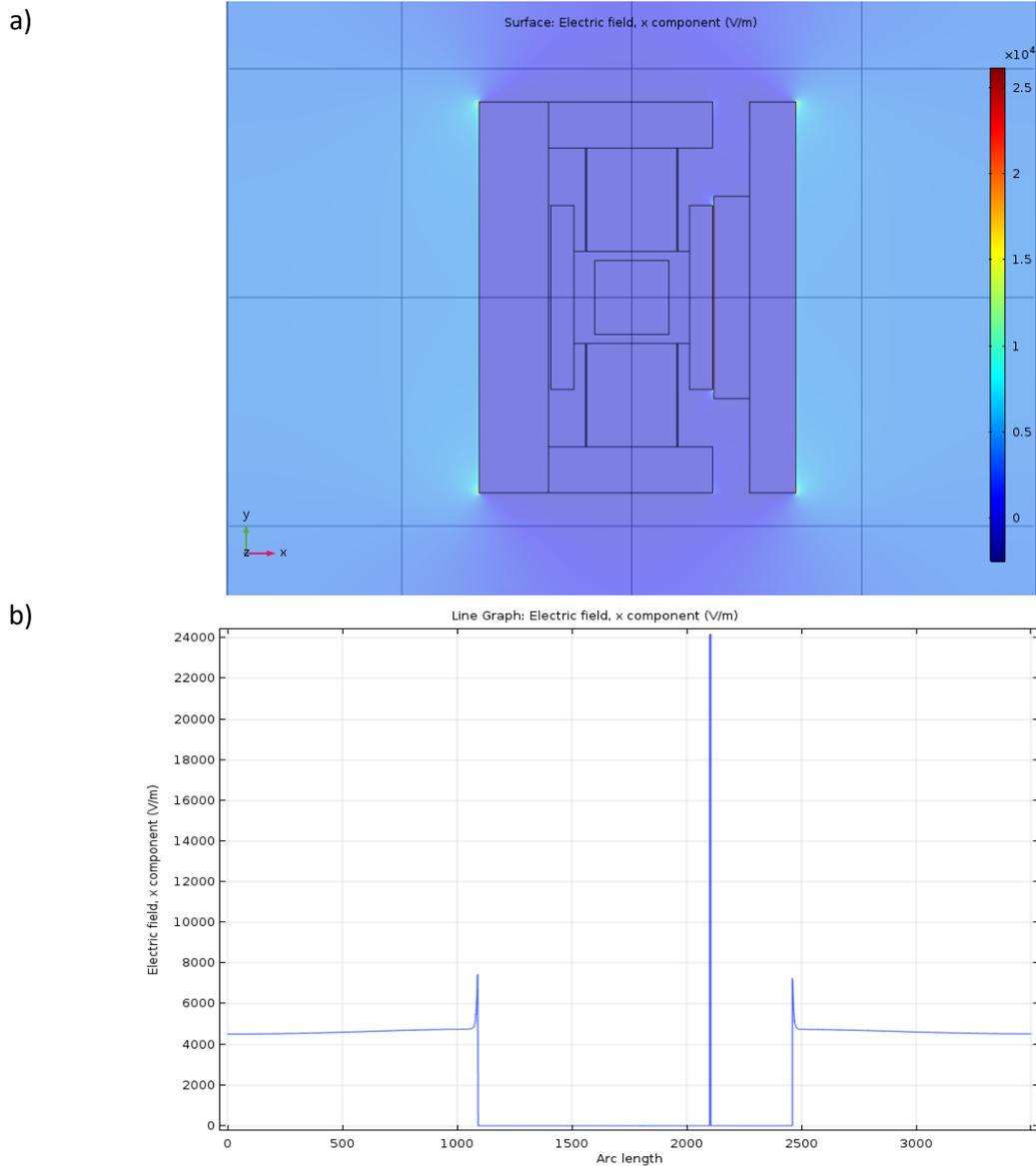


Figure 18: Electrostatic simulation of the refined model showing: a) the surface electric field on an imaginary XY-Cut Plane which goes through the middle of the thickness of the model b) The electric field on an imaginary X-axis Cut Line in XY plane going through the middle of the model

### 3.3.1 Effect of Various Parameters

In this section, the effect of various parameters on the displacement of the suspended mass are explained. In order to facilitate the navigation through the abbreviations used for each parameter, the top views of the device with the respective chosen names for each part are shown in Figure 19.

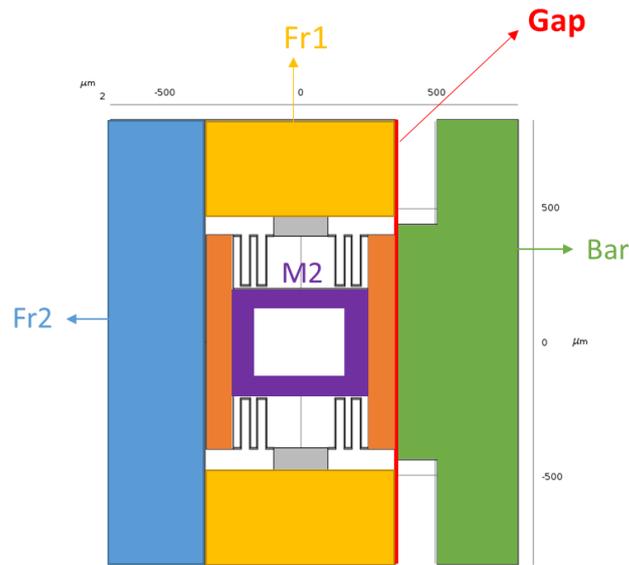


Figure 19: The legend for the utilized terms for different sections of the refined structure.

For the effect of the different parameters are all presented in Figure 20. In these graphs, the displacement in analyzing each parameter is normalized upon the values of an initial design which has a Gap of 30um, Thickness of 10um, Fr2X of 300um, M2X of 400um, Barx of 50um, and M2Y of 400um.

As can be seen in Figure 20.a by increasing the Gap size, the displacement drastically reduces. Hence, for all of the designs, the lowest amount of the Gap size should be considered, while considering the lower limit which comes from the electrostatic pull-in reported to be 1/3 of the gap size(5).

In Figure 20.b, it is shown that by decreasing the thickness of the device, the displacement and indeed the sensitivity of the sensor increases. However, it should be noted that the thickness should always be higher than the width of the meanders, otherwise the deflection in the z-direction would be prevalent as the stiffness in this direction would be less than the x-direction.

Figure 20.c, d and e all show that by increasing the length of the device along the axis of the electric field, the displacement of the suspended mass will increase linearly. As mentioned before for Figure 12, this is phenomenon happens in the same way as putting a conductive slab between the two plates of a capacitance.

And for the final graph in Figure 20.f, it can be seen that any increase along the Y-axis will not lead to any significant change in the displacement.

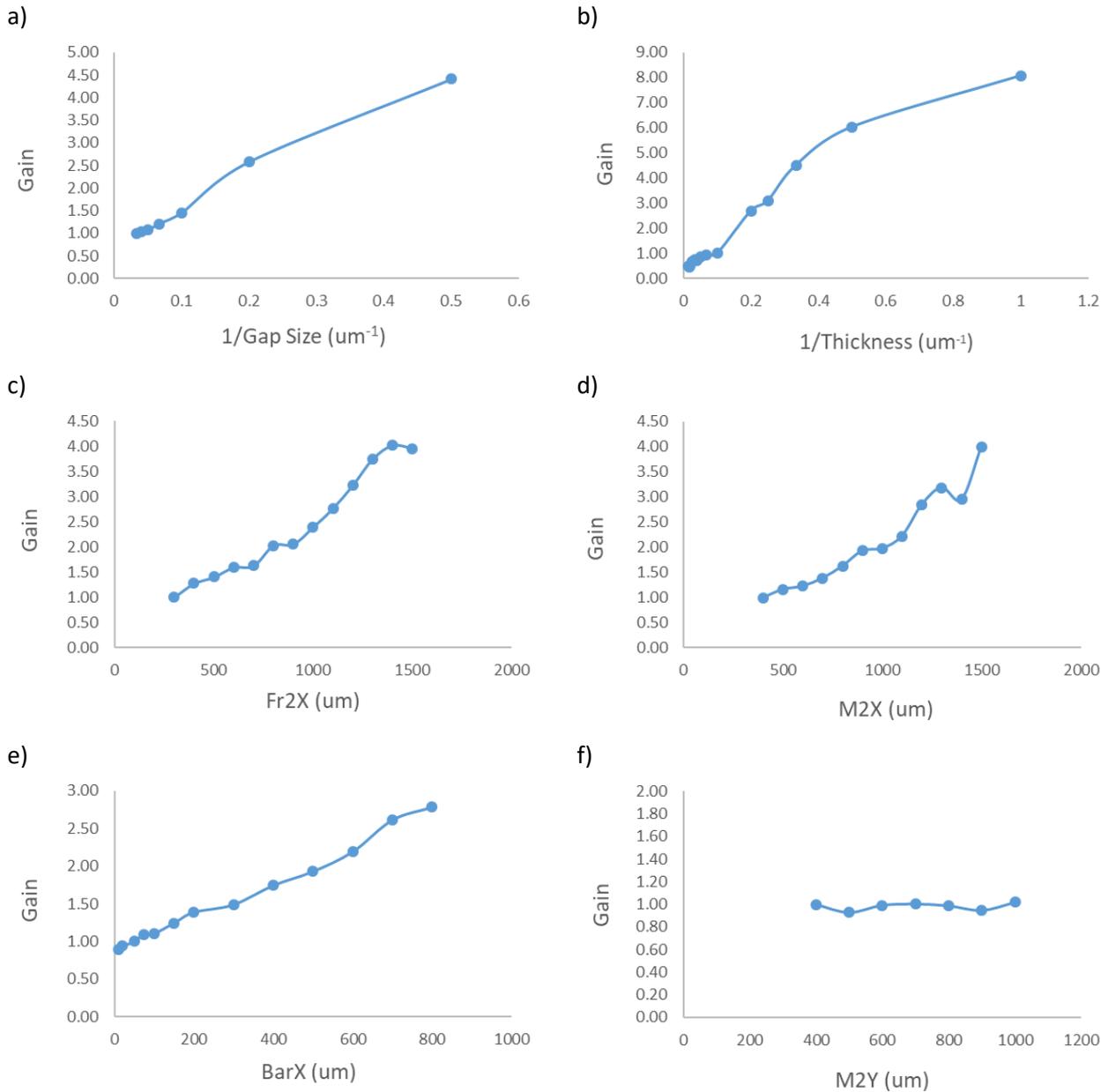


Figure 20: Effect of various parameters on the gain over the displacement of the suspended mass in the initial design with Gap 30um, Thickness 10um, Fr2X 300um, M2X 400um, Barx 50um, M2Y 400um. a) Effect of the Gap size, the distance between the added antenna on the right and the suspended mass b) effect of the thickness of the device c) effect of M2Y, the height of the suspended mass d) effect of M2X, the length of the suspended mass e) effect of BarX, the width of the added antenna on the right f) effect of Fr2X, the width of the frame on the left hand-side

### 3.3.2 Conclusions of the Simulations on the Refined Design

By looking at the results represented in Figure 20, it has been made clear the final parameters of the device for the fabrication should be as the following:

- The least possible Gap size that would not lead to the electrostatic pull-in and would still be possible to fabricate
- The least amount of thickness which does not go below the width of the meanders
- The longer the device becomes along the direction of the electric field, the higher would be the displacement. However, it should be noted that a final product consists of three unidirectional sensors

each along an axis perpendicular to the other two, to cover the electric fields in 3D. Thus, even though the devices become longer in one direction, the total size of the device would increase in the same amount as having the device longer in both of the directions in its plane.

## Chapter 4 Fabrication

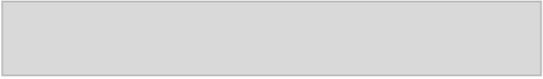
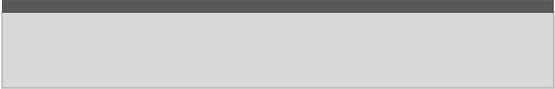
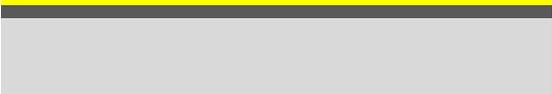
As mentioned in Chapter 3, based on the results of the simulations, the design of the sensor was finalized. Hence, in order to obtain an array of mirrors and holes suspended over another array of mirrors which are deposited on the substrate, the release process of a sacrificial layer would have been necessary. Thus, the process flow required the deposition of a sacrificial layer, which would be etched away at the end of the fabrication.

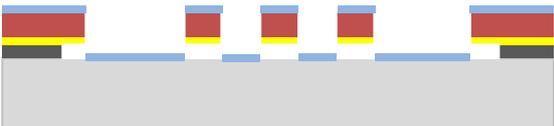
Additionally, regarding the results derived from the simulations, in order to be able to have various values for the stiffness by changing the cross-section of the springs, it would have been necessary to be able to modify the thickness of the device (which is the same as the height of the springs). Consequently, the process flow should have been flexible enough to cover this range for the different thicknesses of the device which would range from 1 $\mu$ m to 5 $\mu$ m. This process would be easily accessible by the electroplating of Copper with optimized current and processing time. As a result, on top of the sacrificial layer, a thin seed layer for the subsequent electrodeposition of Copper needed to be deposited.

As the next step, to be able to pattern the parts of the wafer which should have been plated with Copper, a layer of photoresist with a thickness slightly more than the required thickness of the device (Copper) was needed to be coated onto the seed layer. Then, by exposing the photoresist with the designed CAD file through a mask-less laser writer, or through a hard mask, it would be possible to dissolve the exposed parts of the photoresist in the developer solution. After developing the photoresist, the Cu plating is done which makes it possible to remove the photoresist which was previously forming the molds for Cu. As the last step before releasing the device, it would be essential to remove the seed layer either by wet or dry etching processes. In the end, by etching the sacrificial layer, the array of mirrors and holes would become suspended, as can be seen in Table 1, and the chips would be ready to be diced out of the wafer.

The schematics of the different steps of the process flow for the fabrication of the electric field sensors are depicted in Table 1. The choice of the processes is adapted to the availability of the equipment of the CMI facilities at EPFL. Furthermore, for each step, there have been several possibilities in terms of the machines and recipes which were tried out during this project in order to optimize the final process flow.

Table 1: The designed general process flow for the fabrication of the electric field sensors. A description and the schematic cross-section of the wafer after each step is presented. For several steps, different alternatives have been tried out and the choice of the machines and recipes are adapted to the availability of the equipment of the CMI facilities at EPFL.

Step	Process description	Cross-Section After Process
01	<b>Substrate Retrieval and Cleaning</b>	
02	<b>Deposition of the Sacrificial Layer</b> Thickness: 2um	
03	<b>Deposition of the Seed Layer</b>	
04	<b>Coating of the Photoresist</b>	
05/06	<b>Photolithography and Development</b>	

<p>07</p>	<p><b>Cu Electrodeposition</b></p>	
<p>08</p>	<p><b>Photoresist Removal</b></p>	
<p>09</p>	<p><b>Opening (Removal of the Seed Layer)</b></p>	
<p>10</p>	<p><b>Release Process (Removal of the Sacrificial Layer)</b></p>	
<p>11</p>	<p><b>Deposition of the Reflective Layer to Form Mirrors</b></p>	

Due to the fact that in several steps, such as the choice of the substrate, sacrificial layer, seed layer, photoresist, exposure method, and wet etching, there have been different possibilities, in the following sections, each step and its variant methods have been described in detail.

#### 4.1 Substrate

Considering the readout mechanism of this sensor, it is necessary to have a transparent substrate, so that the light which does not get reflected from the sensor, passes through the device and gets absorbed by the surrounding environment. In this regard, three main features were taken into consideration to choose the optimal substrate; Optical Characteristics, Mechanical Characteristics, and the cost. Based on these criteria, four options have been considered which are analyzed in Table 2. The

chosen wavelength for the optical characteristics is 1.5 $\mu$ m which is the widely-used in the telecommunication industry.

Table 2: Comparison of the cost, versus the optical and mechanical characteristics of different alternatives for the substrate of the electric field sensor(11). The chosen wavelength for the optical characteristics is 1.5 $\mu$ m which is the widely-used telecom window.

Material	Optical Transmission at 1.5 $\mu$ m Wavelength (11,12)	Thermal Shock Resistance (11)	Approximate Cost of a 10mm wafer (CHF)(13,14)
Float Glass	90% (400nm to 2 $\mu$ m)	Low	9.60*
BoroFloat Glass	90% (250nm to 3 $\mu$ m)	Medium (up to 450°C)	27.80*
Full Spectrum Fused Silica	90% in (250nm to 2 $\mu$ m range)	High (Up to 1,000 °C)	68.30*
Sapphire	85% (300nm to 4 $\mu$ m)	Very High (up to 2,000°C)	400**

\* Supplied by CMi at EPFL

\*\* Supplied by MTI Corp.

Based on the data from Table 2, for the process flow which required processing temperatures higher than 450°C, Full Spectrum Fused Silica was chosen and for the process flows which did not require thermal stability at these higher temperatures, Borofloat 33 was utilized.

Based on the choice of the sacrificial layer which would be deposited on the substrate, it might be necessary that substrates go through a cleaning step such as O<sub>2</sub> plasma cleaning, Piranha Bath cleaning, and RCA cleaning.

## 4.2 Sacrificial Layer

In order to deposit the sacrificial layer, which is destined to be removed in order to release the middle part of the device and lead to the suspension of the central mass, two different materials were tried out; Amorphous Silicon and Aluminum.

### 4.2.1 Amorphous Silicon as the Sacrificial Layer

Amorphous Silicon deposited through Low-Pressure Chemical Vapor Deposition (LPCVD) process has the advantage of having an extremely homogenous thickness, very low surface roughness, as well having different etching chemistry compared to the utilized seed layer and Copper. This process is done by the CMi directly and the LPCVD used for depositing a-Si is depicted in Figure 21.

However, despite the advantages of the a-Si, this process is highly time-consuming and hence the processing cost of this furnace is quite high. For the deposition of 2 $\mu$ m of a-Si on 5 fused silica substrates, the processing fee reached 2,830 CHF for 44 hours of deposition.



Figure 21: Representation of LPCVD furnaces at CMi for the deposition of Poly-Si and Amorphous Si (15)

Due to the high cost of this process, it was decided to find an alternative for the amorphous Silicon sacrificial layer. In this regard, Aluminum was chosen for which the deposition step is explained in the next section.

#### 4.2.2 Aluminum as the Sacrificial Layer

In order to cut the steep cost of the long LPCVD process, an alternative for the a-Si was suggested to be Aluminum, due to its low surface tension at the thickness of 2 $\mu$ m compared to other materials such as Chromium, the possibility of having a selective etching vis-a-vis the seed layer and Copper, as well as its relatively low processing cost and the availability of processing through evaporation and sputtering machines in CMi. Furthermore, regarding the native oxide layer that forms on Aluminum, the deposition of the seed layer had to be done with the same machine without breaking the vacuum. This in fact, not only improves the adhesion between the Aluminum and the seed layer (Cr-Au), but also reduces the processing time and the cost in general as there would have been no need for an extra machine or processing step for separately depositing the seed layer.

Moreover, in order to deposit the Aluminum sacrificial layer, since the temperature of the substrate was supposed to not increase considerably, instead of expensive fused silica wafers mentioned in Table 2, borofloat wafers were chosen.

In general, the deposition of Aluminum in CMi is done through two different methods, Evaporation and Sputtering. Below, the details of the trials with each technique are presented in the chronological order:

- **Evaporation:** Initially, it was decided to choose the evaporation technique due to its better surface quality compared to sputtering and availability of two machines at CMi, Lab600, and EVA760 (shown in Figure 22)



Figure 22: Presentation of a) EVA760 (16) and b) Lab600 evaporation machines (17)

However, on the one hand, due to the large chamber size of the Lab600 machine and the high thickness of the required Al layer (2 $\mu$ m), the utilization of Lab600 for this purpose was rejected by the CMi staff (8<sup>th</sup> of June, 2018). On the other hand, 4 days after having received the access to the EVA760 machine, the cryogenic piping of the machine started to have a leak and the machine underwent a maintenance of at least 4 months, which was well beyond the timeline of this project.

As a result, at this stage of the project, the only option to process the 2 $\mu$ m of Aluminum in CMi was to use the sputtering technique.

- **Sputtering:** The only sputtering machine at CMi with all of the three targets of Al, Cr, and Au, is the DP650 machine which is presented in Figure 23.

However, there have been two main issues to start with DP650 sputtering machine:

1. The absence of the Al-Cr-Au recipe in the database of the machine
2. Limitation of the Al deposition to 1.5 $\mu$ m

With the assistance from the supportive staff at the CMi, the two aforementioned issues were solved in a matter of a few days and the first test with for Al(2 $\mu$ m)-Cr(15nm)-Au(150nm) with deposition at room temperature was done. As can be seen in Figure 24.a, the surface of this wafer is matt and rough, in complete contrast to how it should look like.



Figure 23: Representation of the DP650 sputtering machine at CMi, which is the only sputtering machine with all of the three required targets of Al, Cr, and Au (18)

After studying the potential reasons underlying the deterioration of the quality of this wafer, and by consulting Dr. Philippe Langlet from CMi, it was found out that the issue arises from the low heat conductivity of the glass substrate. During the sputtering of Aluminum, considering the long deposition time of 66 minutes, as the highly energetic atoms of Aluminum hit the surface, the temperature of the substrate increases locally by several hundreds of Celsius degrees. Moreover, as the glass substrate does not conduct the heat efficiently, the substrate stays at elevated temperatures during the deposition of the next thin films, Chromium, and Gold. This issue results in the inter-diffusion of the hot and energetic Aluminum atoms to the Cr and Au layers and deteriorates the surface quality.

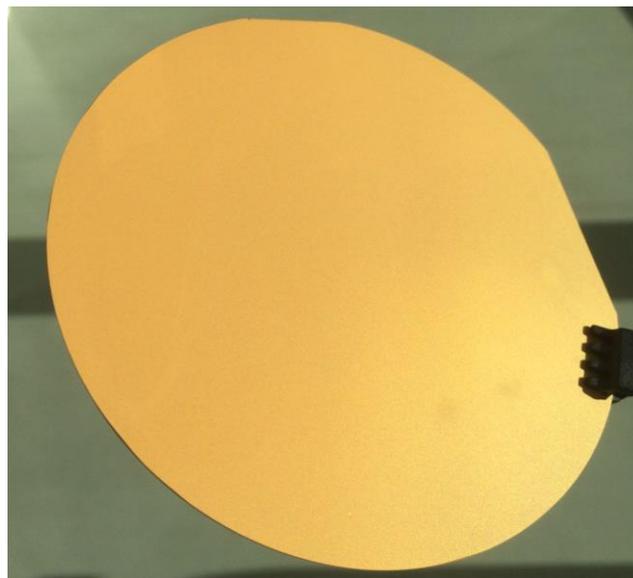


Figure 24: The first wafer with Al(2um)-Cr(15nm)-Au(150nm) layers obtained from DP650 sputtering machine. The matte and rough surface is caused by the diffusion of Al atoms to the Gold layer.

In order to solve this issue, a new recipe was made with a duration of 8 hours of cool down after the deposition of Aluminum, in order to avoid the previous issues. However, due to the absence of the convective heat transfer inside the vacuum and the low heat conductivity of the glass substrate, it can be seen in Figure 25.

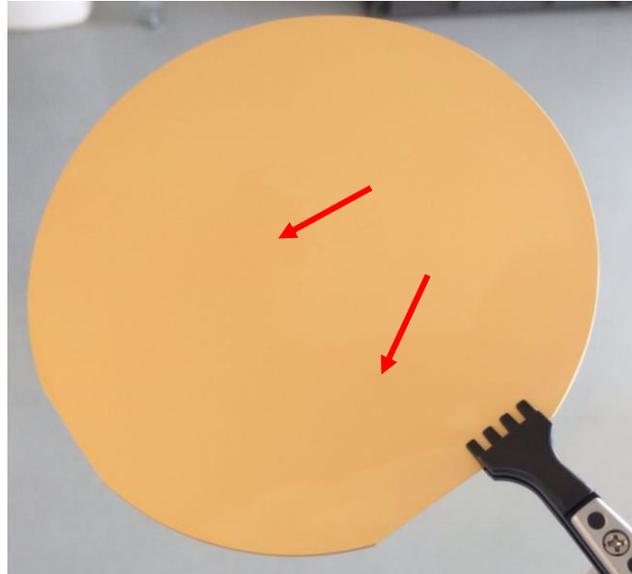


Figure 25: The second wafer with Al(2um)-Cr(15nm)-Au(150nm) layers obtained from DP650 sputtering machine. Due to the absence of convective heat transfer mechanism in the vacuum and the low heat conductivity of the substrate, even after 8 hours of cool down step, some matte regions (marked by red arrows) can be seen on the surface of the wafer.

Being limited to the sputtering machine at CMI which does not provide satisfactory results, and not having the possibility to run the tests with the evaporation machines, EVA760 (down due to maintenance) and Lab600 (not permitted by CMI due to the high thickness of Aluminum), it was decided to contact the other institutes and department at EPFL in search of evaporation machines. As a result, the operator of the single-chamber evaporation machine at the Physics Department at EPFL accepted to run a test which leads to the layer shown in Figure 26. As can be seen, the surface quality is considerably better than the previously obtained layers through sputtering.

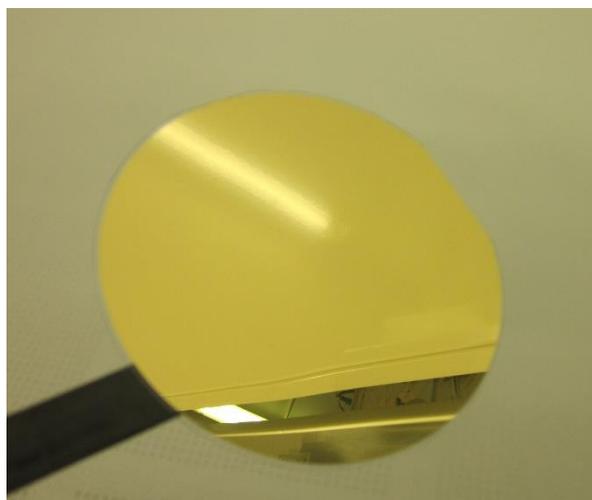


Figure 26: The coated borofloat wafer from the Physics Department at EPFL with a high quality (superior to the wafers coated through sputtering) and reflective surface.

After obtaining an acceptable result and pursuing the further steps in the process flow with this wafer, the CMi staff were also convinced to allow a run with the Lab600 machine. In this process, 8 wafers were put on the tray which is fixed to the ceiling of the machine with a distance of 1 meter from the targets. As Lab600 is also an evaporation machine, the obtained surface quality looked very similar to the one from the Physics Department.

In Table 3, one can find the summary of the different utilized substrates, deposition techniques, their results, and the reference number of their Test wafers. The detailed Run card for each Test wafer is written in the Annex of this report. In contrast to the wafer with the amorphous Silicon as the sacrificial layer, for the wafers with Aluminum, the sacrificial layer and the seed layer are deposited at once under the same vacuum.

Table 3: the summary of the different utilized substrates, deposition techniques, their results, and the reference number of their Test wafers. Contrary to the wafer with the a-Si sacrificial layer, for Al, the sacrificial layer and the Cr-Au seed layer are deposited at once under the same vacuum.

Ref. Number	Substrate Material	Sacrificial Layer	Machine	Recipe	Surface Quality
Test 1,3,4	Fused Silica	a-Si	DP650	Cr(15nm)-Au(150nm)	High
Test 2	Borofloat	Al	DP650	Al(2um)-Cr(15nm)-Au(150nm)	Low
Test 5	Fused Silica	Al	EVA (Physics Dept.)	Al(2um)-Cr(15nm)-Au(150nm)	High
Test 6	Borofloat	Al	DP650	Al(2um)-8hr Wait-Cr(15nm)-Au(150nm)	Low-High
Test 7-15	Borofloat	Al	Lab600	Al(2um)-Cr(15nm)-Au(150nm)	High

### 4.3 Seed Layer

In order to grow the device layer which would be made out of Copper on the substrate, it would be obvious that amorphous Silicon would not work as the seed layer. However, in the case of Aluminum, there is a myriad of companies who electroplate Copper on Aluminum, in applications such as chrome plating Aluminum rims for in automotive industry where a Zincating step is done to protect the surface of the active Aluminum from oxidizing (19). However, considering the limitations in the modification of the contents of the Cu plating bath in CMi, there would be a need for the intermediary seed layer to facilitate the growth of Copper on top of Aluminum. The seed layer chosen in this project has been kept the same, being Cr(15nm)-Au(150nm). The reason for the presence of Chromium is due to its good adhesion to Aluminum and Gold, as well as its small atom size which enables filling the defects at the interface.

The seed layer in this project has been deposited either through sputtering or evaporation. As already mentioned for Table 3, the a-Si substrates are all followed by sputtering of the seed layer onto the sacrificial layer. However, for the wafers with the Aluminum sacrificial layer, regardless of the deposition technique (which has been both evaporation and sputtering), the deposition of the seed layer

and the sacrificial layer have been happening in a single machine at once and under the same vacuum to prohibit the formation of the Al native oxide layer.

#### 4.4 Coating the Photoresist and Photolithography

As can be seen in the general process flow in Table 1, in order to make the molds for the Copper plating step, a photolithography process should have been utilized. The wafer-scale design made by the K-Layout software based on the parameters of interest which were derived in Chapter 4 is presented in Figure 27.

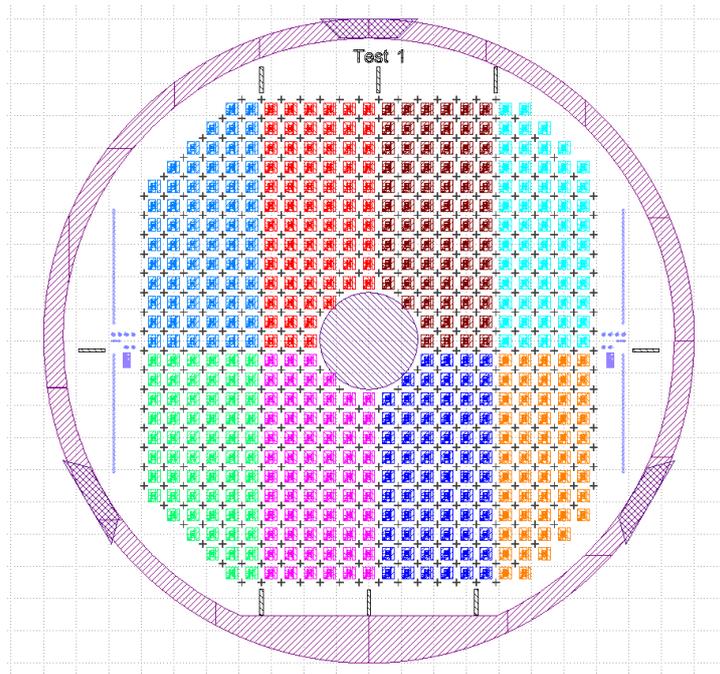


Figure 27: The wafer-scale design of the chips for the exposure generated by K-Layout software.

For the eight blocks of design which are color coded in Figure 27, three different parameters are checked, each with two different values that can be seen in Table 4.

Table 4: Parameters which have been checked with the 8 designs on the wafer.

Parameter of Interest	Values
Gap Size	5um
	10 um
Meanders Length (M2Y)	85 um
	180 um
Number of Meanders	1
	2

Before starting the exposure, it is required to coat the photoresist on the wafer. The only positive photoresists provided by CMI that could be coated with 5um were the AZ9260 and ECI3027 resists. As a result, the first trials were done with AZ9260 photoresists.

In order to organize the results which were obtained from the photoresists, the tests are split into two categories based on the materials of the sacrificial layer, amorphous Silicon and Aluminum.

- **Amorphous Silicon:** For the wafers with amorphous Silicon as their sacrificial layer, the deposition of the seed layer, Cr(15nm)-Au(150nm), was done through the sputtering machine (DP650). Hence, the roughness is in general higher than the evaporation technique which results in a better adhesion of the photoresists to the surface of the seed layer. All of the wafers with the a-Si as their sacrificial layer in this project were coated with 5.5um of AZ9260 positive photoresist and the result of the photolithography, meaning the coating, exposure, and development were all successfully done. The importance of the quality of the seed layer was in fact realized after seeing the failure of the photolithography step for Aluminum wafers and comparing them with the a-Si ones.
- **Aluminum:** For the wafers with Aluminum as their sacrificial layer, as mentioned in Table 3, the surface quality after the deposition of the seed layer has been quite diverse. With the first wafer with Aluminum (Wafer Test 2) which was coated with the Al-Cr-Au recipe in DP650 sputtering machine, after depositing the AZ9260 5.5um and exposing the wafer, the pattern of the structures could be perfectly recognized. However, after the development, as can be seen in Figure 28, the photoresist was completely detached in the exposed areas and their surroundings.

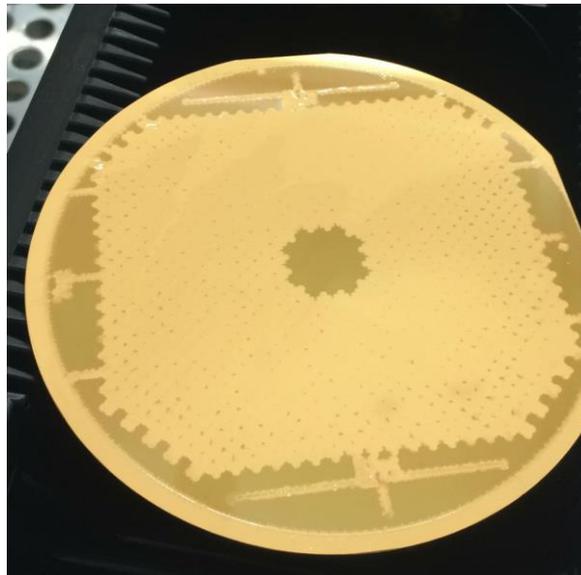


Figure 28: Wafer Test 2 after development of the exposed photoresist. The resist is completely detached and flaked off.

After discussing with the CMI photolithography expert, Dr. Julien Dorsaz, the following reasons for this failure were suggested:

- The Aluminum layer with the alloying which has happened by the inter-diffusion of Al atoms into the Gold layer has decreased the heat conductivity of the wafer compared to the a-Si wafers and hence the low heat conductivity of the wafer has led to the overheating of the wafer during the exposure and has formed bubbles inside the photoresist which result in the detachment of the resist after development. The suggested solution has been to use step exposure by using a mask.
- The low heat conductivity of Aluminum results in an insufficient baking of the photoresist. For this purpose, the baking temperature should be increased by 10°C
- The AZ9260 resist does not provide a high adhesion to noble metals and hence either the resist should be changed, or an intermediary layer should be added to enhance the adhesion

As the next step, in order to solve the potential problems seen before, the Test Wafer 5, which was coated in the evaporator machine of the physics department at EPFL was put into test. For this wafer, instead of exposing through the Mask-Less Aligner (MLA150) machine, a hard mask which is shown in Figure 29, was fabricated to be used in the MA6 Gen3 machine shown in Figure 29.

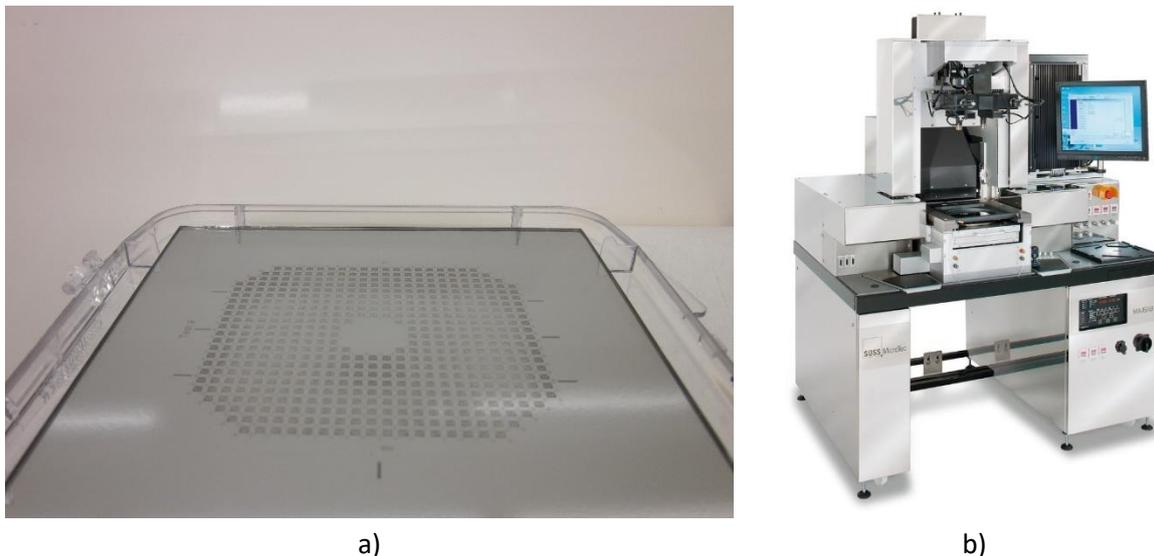


Figure 29: a) The hard mask fabricated for the step exposure via b) SUSS Microtec MA6 Gen3 Mask Aligner machine in CMI (20).

However, the result after the development of this wafer (Test 5), was not successful. As can be seen in Figure 30, a side-by-side comparison of Test Wafers 2 (right) and 5 (left) is presented. For Test Wafer 5, it is obvious that it has a more reflective and brighter surface, as it is coated through evaporation opposed to Test Wafer 2 which is sputtered and rough. Moreover, the remainder resist spots on Test2 indicate the overheating of the resist which is solved by utilizing step exposure, having 5 seconds of exposure and 20 seconds of cool down, all repeated for 5.5 cycles which takes 27.5 seconds (equal to 550 mJ/cm<sup>2</sup>). Furthermore, the overall detachment of the resist on both wafers is now an indicator of poor adhesion of the photoresist to the substrate. It should also be noted that the grey area on Test Wafer 2 emerged after an O<sub>2</sub> plasma treatment of 5 minutes to strip the resist, which apparently led to the diffusion of Al atoms to the Gold thin film on surface.

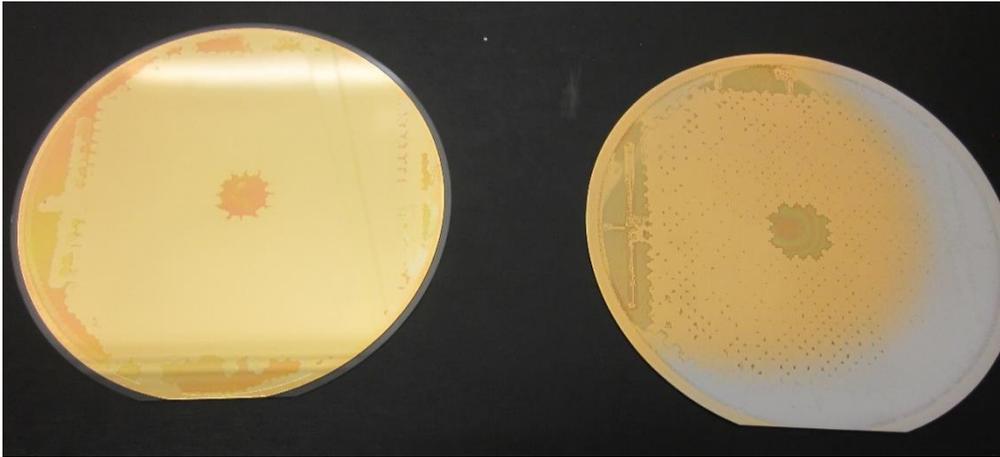


Figure 30: Side-by-side comparison of Test Wafers 2 (right) and 5 (left). Test5 has a more reflective and brighter surface as it is coated through evaporation opposed to Test2 which is sputtered and rough. The remainder resist spots on Test2 indicate the overheating of the resist which is solved by utilizing step exposure. The overall detachment of the resist on both wafers is now an indicator of poor adhesion of PR to substrate. The grey area on Test Wafer 2 emerged after an O<sub>2</sub> plasma treatment of 5 minutes to strip the resist, which apparently led to the diffusion of Al atoms to the Gold thin film on surface.

Having narrowed down the origin of the issue to the lack of adhesion between the resist and the substrate, 3 alternatives could be tested:

- Increasing the baking temperature
- Changing the resist type
- Utilizing Titanium as an intermediary layer

After cleaning Test Wafer 5 which was shown in Figure 30, a new recipe with an elevated (+10°C) baking temperature was tested which led to good adhesion. However, this result could not be reproduced with the next wafers. Contrary to Test Wafer 5 which was coated by the EVA evaporation machine in Physics department, all of the next wafers were coated in the Lab600 evaporation machine at CMi. One potential explanation for this unrepeatability might be the difference between the surface roughness of the wafers. Meaning that Test Wafer 5 has had a higher roughness which interlocks the photoresist better than the Test Wafers 7-14 which were tested after 5. Moreover, another explanation would be the presence of nanometers-thin residues of the burnt resist which improved the adhesion of the next photoresist deposition.

In order solve the remaining issue for the next wafers, the baking temperature was further increased by 5°C but the result did not change. Thus, the next remaining option was to opt for the resists and/or intermediary layers that increase the adhesion. In this regard, for the Test Wafer 8, instead of AZ9260 photoresist, the ECI3027 resist was used. However, as can be seen in Figure 31, although the structures are formed and the detachment issue is not as serious as before, still the structures seem to be peeled of and deformed due to the detachment of the photoresist. Moreover, the exposure test pattern which is placed on all of the corners (Figure 31) shows that there is also an underexposure issue with this wafer.

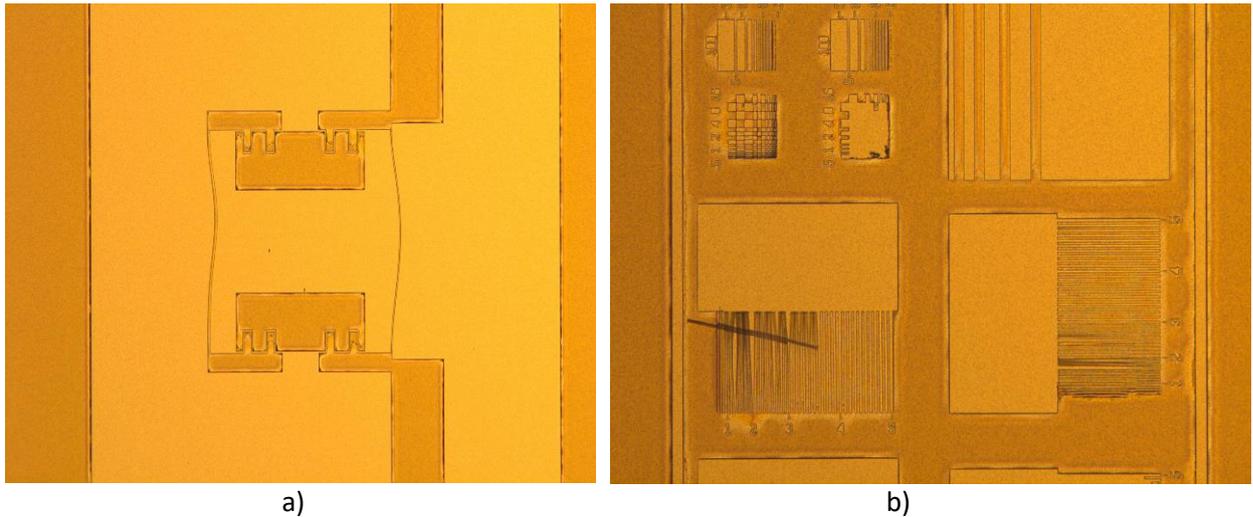


Figure 31: The optical microscope pictures of Test Wafer 8, showing the detachment of the ECI3027 photoresist and an underexposure

In order to solve these issues, for the next test a 10nm-layer of Titanium was coated on the wafers and then after activating their surface with a short (30 s) oxygen plasma treatment, they were coated with the ECI3027 which has a higher adhesion to the surface. For this batch of wafers, the adhesion has been perfect, however, the quality of the ECI3027 photoresist on glass substrates is slightly low as can be seen in Figure 32. The small circles with the 120° angle are in fact the positions of the pins on the backside of the wafer in the ACS200 machine, which emerge on the wafer due to the different cooling rate of these regions (as well as the corners of the wafers) compared to the other parts of the wafer.

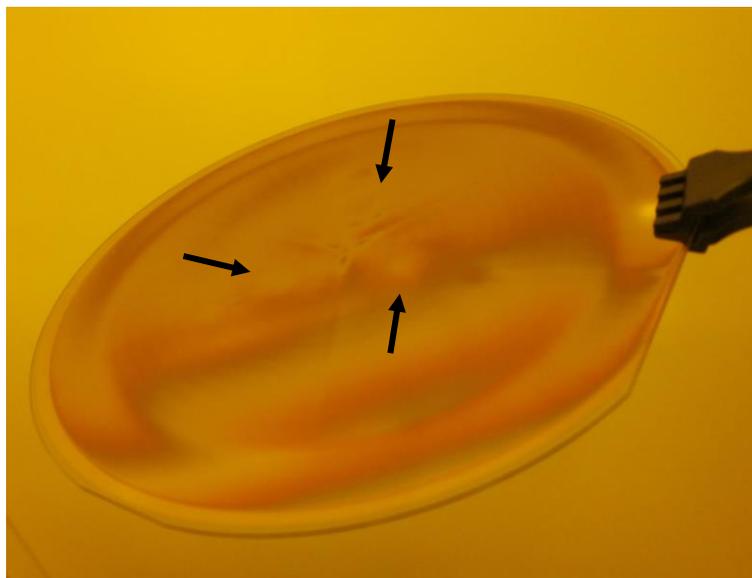


Figure 32: Test Wafer 9 after the deposition of a 10nm-layer of Titanium followed by oxygen plasma surface activation and coating 5um of ECI3027 resist. The small circles (shown with arrow) at the 120°C show the position of the handling pins in ACS200 machine which lead to a faster cooling down in these regions compared to the other parts of the wafer.

## 4.5 Cu Plating

After forming the molds by developing the exposed photoresists, the wafer is ready to be copper plated. However, as the electrodeposition bath at CMI is not frequently used, the quality of the bath and the rate of deposition can considerably fluctuate. In order to calculate the current and the duration of the deposition, the surface area that needs to be electroplated should be calculated. This was done through CleWin software and for the design shown in Figure 27, it was 20% of the active surface area when the wafer is clamped. Multiplying the 20% by the 2A of current which should be used for a blank wafer, the required current for this design should have been 0.4A, and the deposition rate would be 0.5um per minute. However, as mentioned before, regarding the instability of the bath, the deposition rate and the surface quality vary considerably. In Figure 33, some examples of the copper plated structures which are all fabricated with a current of 0.4A can be seen.

As it can be noted in these pictures, although the utilized current has been the same for all of the three wafers, the roughness and quality of the obtained structure varies significantly. This issue indicates the instability of the copper plating bath and the difficulties for achieving a reliable and reproducible result. The main problem that leads to this issue is the limited number of users for this bath in CMI and hence a long renewal cycle for the bath. As the additives and ions inside the bath are used by depositions, the quality gradually degrades and makes it very difficult to obtain reliable results, even by using a dummy before the main run.

In this regard, although obtaining reliable results is difficult in CMI, having a dedicated bath for this purpose and renewing it on time, not only would lead to a reliable and low cost process, but also enables electroplating copper directly onto aluminum by using a Zincating step. This step hinders the formation of the native Aluminum Oxide layer which enables excluding the seed layer deposition step. Furthermore, not having the seed layer and the Gold on the surface of the wafer before coating the photoresist, would improve the adhesion between the resist and the top surface (Aluminum), which would omit the need for the intermediary Titanium layer previously used for increasing the adhesion.

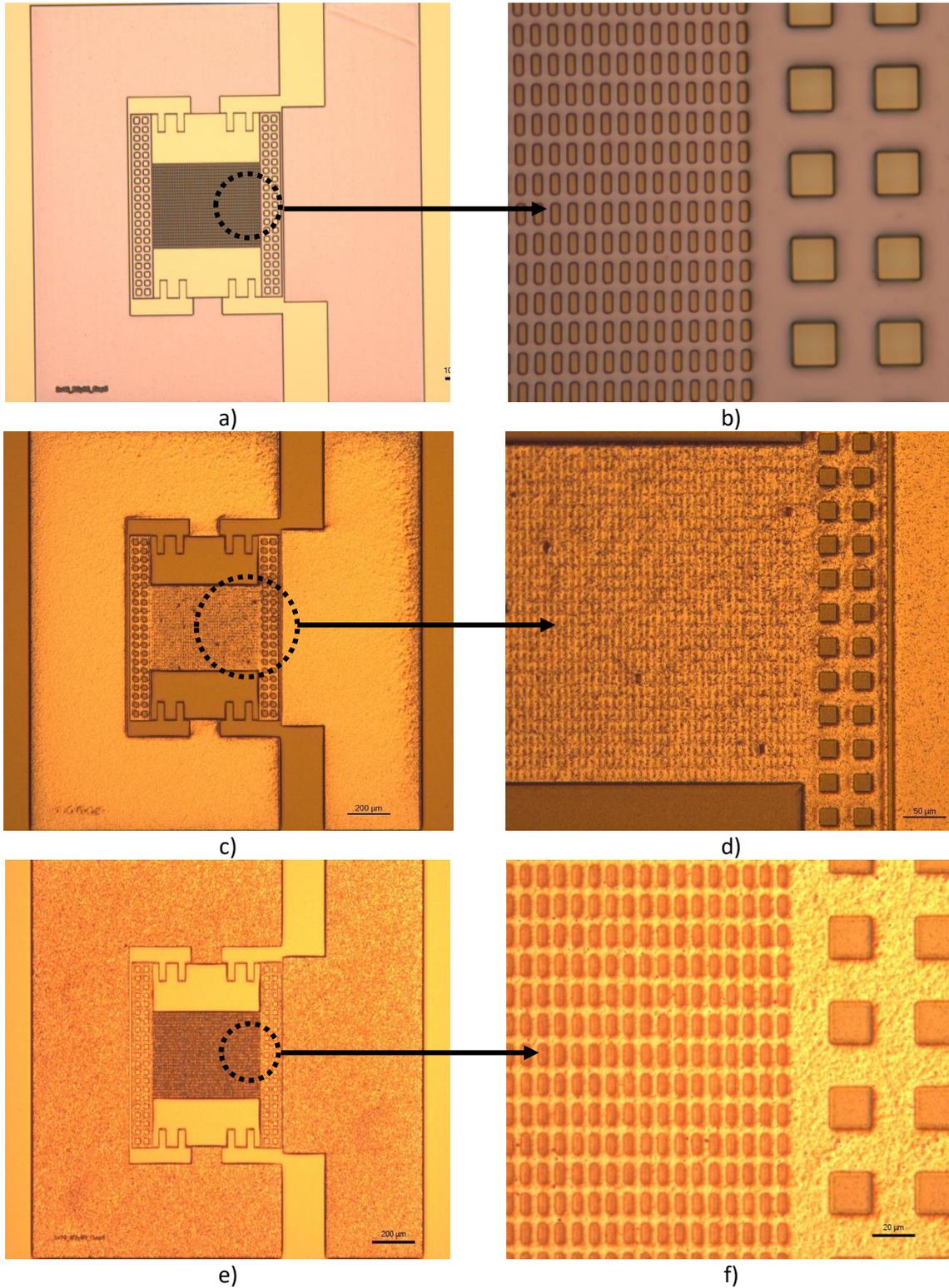


Figure 33: Optical micrographs of the structure of the devices after copper electroplating and removal of the photoresist. All of the depositions have happened at the same 0.4 A current, while the difference in the pictures shows the instability of the bath and the differences in the roughness that can be obtained. a & b) Test Wafer 1, c & d) Test Wafer 9, e & f) Test Wafer 12.

### 4.6 Resist Stripping and Opening (Seed Layer Removal)

Considering the presence of copper on the surface, in order to remove the photoresist, instead of the oxygen plasma, the UFT Resist Remover 1165 should be used. After removing the resist, parts of the wafer which were protected by the removed photoresist will be accessible. At this stage, according to the general process flow, an Ion Beam Etching (IBE) step should be done to remove the thin layer of the seed layer and open the access to the sacrificial layer. In the IBE process, as is shown in Figure 34, the wafer will be put on a rotating substrate and then energetic atoms of Argon will hit the surface which can be tilted. This tilting of the substrate hinders the formation of residues and products of etching on the sidewalls (a phenomenon also known as fencing) (21,22).

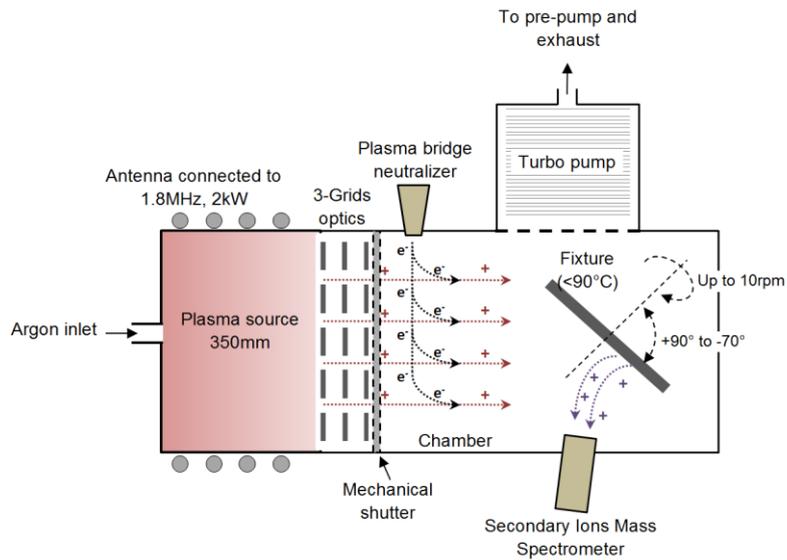


Figure 34: Schematic of the internal working mechanisms of Veeco Ion Beam Etching machine (IBE350) (22)

Optical microscope images of the structures after the IBE process are provided in Figure 35.

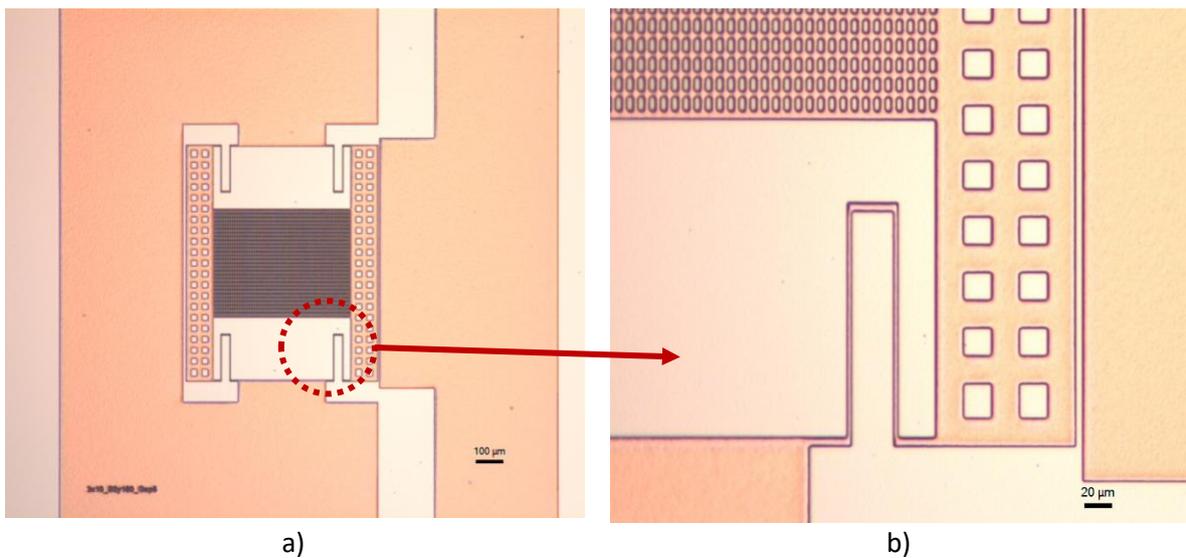


Figure 35: Optical micrographs of the structure of a device after the IBE process. A) 5X magnification b) 20X magnification

The duration of the IBE process depends on the energy of the Argon atoms, which is defined by the type of recipe, and the material that would be etched. Based on the different etch rates reported for each material, the duration required for etching of each thin film would be calculated.

Furthermore, through Secondary Ion Mass Spectroscopy (SIMS) attached to this IBE machine, it is possible to monitor when each material is being etched by showing the real-time mass spectroscopy of the chosen elements.

#### 4.7 Release Process (Removal of the Sacrificial Layer) and Al Coating

After removing the seed layer and providing the access to the sacrificial layer, a release process should take place to remove the sacrificial layer and render the central mass suspended. The amount of the undercut required for releasing the structures is dictated by the largest distance which is required for the etchant to travel until it reaches another front-line of etchant. As can be seen in Figure 35, in this design, the largest value for such a distance is defined by the distance between the large holes on the sides of the suspended mass which is 20 $\mu$ m.

The etchants used for the release process can be categorized based on the material of the sacrificial layer as the following:

- **Amorphous Silicon Sacrificial Layer:** For removing the a-Si layer, the etchant of choice is KOH 40% in 60°C. The setup for such processing can be seen in Figure 36, which depicts a beaker filled with KOH40% placed on top of a hotplate set to 60°C, with a magnet for the agitation of the fluid.



Figure 36: Setup of the release process, having the beaker filled with KOH40% over a hotplate set to 60°C, with a magnet for the agitation of the fluid.

However, regarding the duration of the process, as it was found in the literature that the average etch rate for a-Si would be 300nm/min. However, for Test Wafer1, even after 120min, some parts of the surface of the wafer looked gray, meaning that the amorphous silicon is not still etched away. Nevertheless, for this wafer, after utilizing HCl for the neutralization, unexpectedly it attached the Chromium layer and led to the releasing of the structure.

After studying the reason behind the low etch rate of the a-Si, it was found out that the content of Hydrogen inside the a-Si layer the temperature at which it is deposited in the LPCVD furnace can considerably affect the etch rate of a-Si in KOH (23). Nonetheless, as the content of Hydrogen has been unknown, in order to assure about the exact etch rate, utilizing a test wafer with the pattern presented in Figure 37 was proposed. In this design, 16 squares of  $1\text{cm}^2$  are filled with the squares with different edge sizes of 4, 8, 12, 20, ..., 100  $\mu\text{m}$ . By putting this kind of wafer inside the etchant, it would be possible to visually observe when each of the  $1\text{cm}^2$ -squares disappears. As an example magnified in Figure 37.b, the amount of time that takes to visually observe the 50 $\mu\text{m}$ -slot has disappeared, is the required etch time for removing 25 $\mu\text{m}$  ( $0.5 \times 50\mu\text{m}$ ) of a-Si. Although the wafer for this purpose (Test Wafer 3) had been fabricated for this purpose, it was not possible to finalize this etch rate test due to the lack of time.

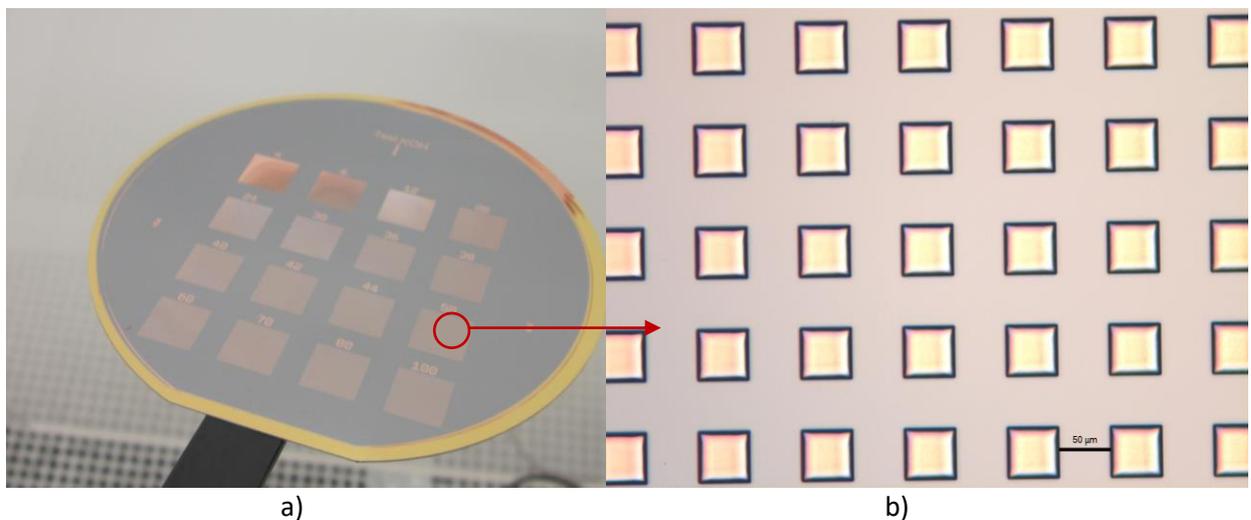


Figure 37: a) Test Wafer 3 for KOH etch rate test. Each of the sixteen  $1\text{cm}^2$  squares is filled with squares of different edge sizes as written on the wafer. b) the 50 $\mu\text{m}$ -squares filling up the 12<sup>th</sup> big square on the wafer. As an example, the amount of time that takes to visually observe the 50 $\mu\text{m}$ -slot has disappeared, is the required etch time for removing 25 $\mu\text{m}$  ( $0.5 \times 50\mu\text{m}$ ) of a-Si.

## 4.8 Dicing and Final Chips

As mentioned for the previous steps and considering the logs for all the test wafers which are presented in the Annex of this report, only one of the wafers became ready to be diced. This step which is a service done by CMi is performed by coating the top-side of the wafer with a photoresist to hold the structure together throughout dicing, and then giving the wafer to the staff by providing the information about the wafer's top and bottom sides. In the end, the diced wafer will be delivered by CMi with a UV-cured film which should be adhered to the back-side of the wafer to hold the chips together.

However, in our case, although the details about the wafer were provided to the staff member responsible for this service, as the operator changed for this dicing, the person who diced the chips attached the UV-tape to the top-side of the chips instead of the back-side, posing a crucial threat to the suspended structures. The picture of 4 chips which are detached from the UV-cured film and cleaned in Acetone and Isopropyl Alcohol (IPA) is presented in Figure 38.

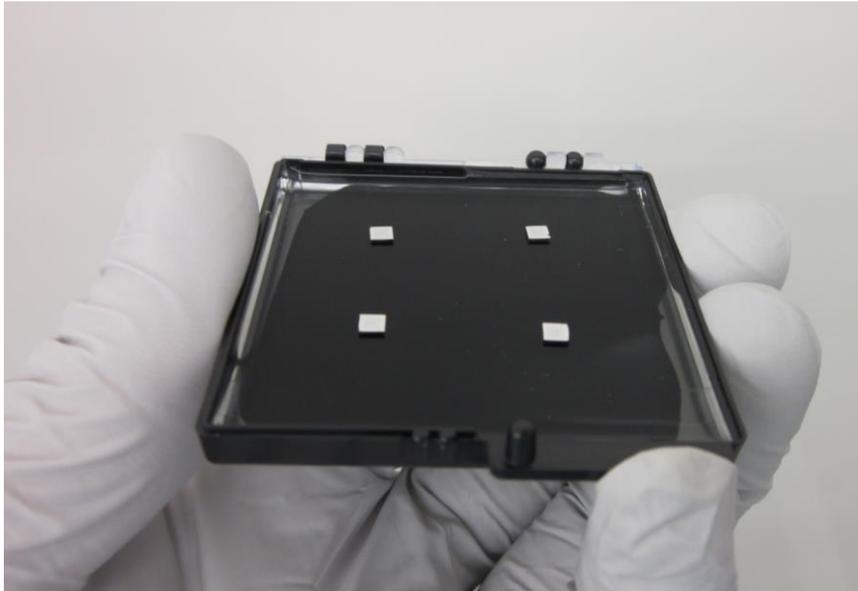


Figure 38: Picture of 4 chips from Test Wafer 1 which are detached from the UV-cured film and cleaned in Acetone and Isopropyl Alcohol (IPA).

Moreover, to see the structure of the device and if the central mass is suspended, several Scanning Electron Microscopy (SEM) images are captured which are presented in Figure 39.

As it can be seen in Figure 39.a and b, the whole device has been perfectly shaped. In Figure 39.c, suspension of the big mass and the remaining seed layer is visible. This remaining amount of the seed layer is supposed to be caused by the shadowing from the nearby vertical sidewalls in the IBE process. For the future trials, it is suggested to add a  $0^\circ$  followed by the  $-10^\circ$  tilting to remove both the potential fencing from  $0^\circ$  etching, and remove this visible remainder of the seed layer through  $-10^\circ$  tilting.

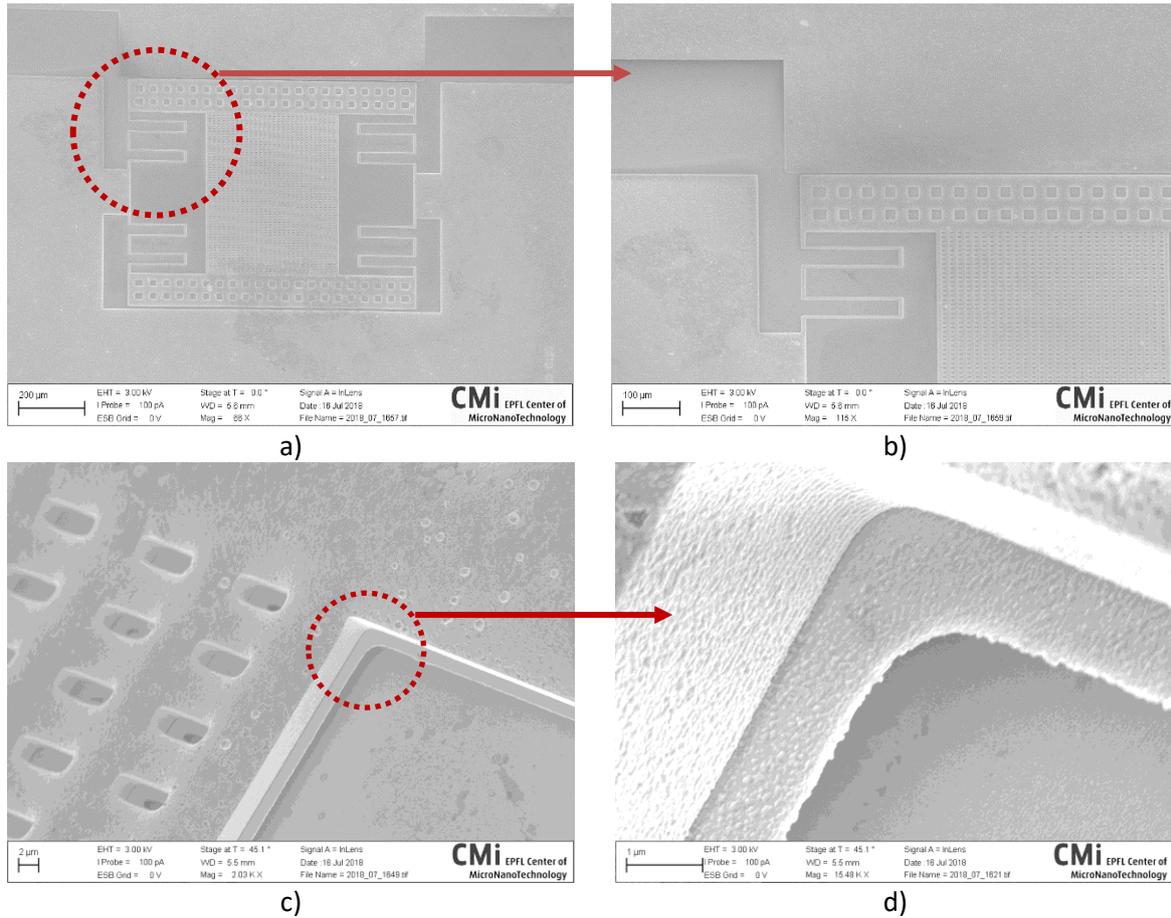


Figure 39: SEM images of a diced chip showing a) the whole device, b) magnified view of the meanders and large holes, c) suspension of the big mass and the remaining seed layer, d) magnified view of the remaining seed layer due to the limitations of IBE process.

However, despite the very promising results obtained for the suspended parts of the structure, it seems that for the long meanders, the tip of the meander in some devices touches the substrate. This is partial failure might be due to the wrong adhesion of the UV-cured film on the top-side of the wafer which has pushed the structure to collapse. The SEM image of such a collapse of meanders is presented in Figure 40.

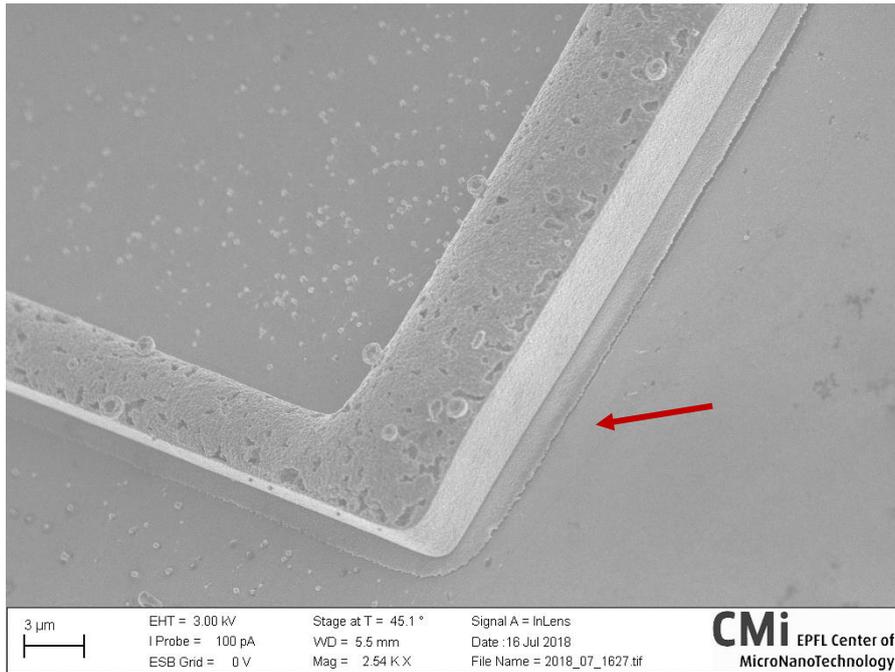


Figure 40: SEM image showing the tip of the meander at which it touches the substrate. This collapse might be due to the compressive tension from adhering the UV-cured film on the wrong side of the wafer.

# Chapter 5 Conclusion

In order to conclude this report, two main aspects are emphasized; Achieved Results, and the suggested Next Steps for the continuation of this project.

## 5.1 Achieved Results

Throughout this project, several important achievements have been reached despite some unfortunate problems, such as breaking down of some key equipment in CMi, as well as an accident which lead to a bone fracture of the author of this report resulting in a delay of one month in starting the fabrications.

To briefly explain the achievements of this project, the following checklist can be made:

- **Simulations:** Without having any prior knowledge to COMSOL Multi-Physics software, it was made possible to simulate a complex model and extract the required information which were used in the fabrication and reduced the cost through omitting a trial-and-error phase for designing the structure.
- **Process Flow:** Not only the general process flow was made for these fabrications, but also each step was troubleshoot to facilitate the fabrication of the sensors through two different approaches based on the material of the sacrificial layer.
- **Fabrication:** Despite the fact that one of the wafers resulted in obtaining the chips, the feasibility study of the selected process flow has proved that if some machines have a stable outcome, such as the copper plating bath, finishing the process flow for a wafer and obtaining the chips would happen without any major issue.
- **Debugging and Troubleshooting:** Throughout this project, several alternative steps for both the simulations and different parts of the process flow were studied or put into practice. Hence, the developed design and process flow are the essence of these efforts and both can be run without errors.

## 5.2 Next Steps

The suggestions for the continuation of this project can be organized into three categories for the design, simulations, and the fabrication.

- **Design:** One of the important mechanisms that seems to considerably affect the displacement is the edge effect. The suggestion for the next trials of the design is to further utilize this phenomenon to increase the displacement of the suspended mass. One suggested approach for this purpose is to have corrugated designs on the left hand-side of the bar and the right-hand side of the M1 mass, so that they can form interdigitated fingers such as the MEMS capacitors. In such setup it would be possible that by forming shorter edges, the edge effect happens in several positions and hence further increase the electrostatic force and thus the displacement of the suspended mass.

- **Simulations:** Although the simulations which have been already done provide the results for most of the parts of the design which could potentially have an effect on the performance of the device, still there is room for trying out simulations for new elements or designs such as the one mentioned above.
- **Fabrication:** Most of the challenges during the project were faced during the fabrications. The future steps and suggestions for the fabrication are organized in categories:
  - **The seed layer:** Although Copper plating bath in CMi cannot be modified to allow the direct deposition of Copper on Aluminum, by having a dedicated plating bath and with the suitable additives such as the ones for zincating to hinder the formation of the native Aluminum oxide, it would be possible to in fact skip the step for deposition of the seed layer.
  - **Choice of the photoresist:** After testing two positive photoresist, AZ9260 and ECI3027, each showed to have their own limitations. A new negative resist, AZ® 15nXT (115 CPS)(24), which would be soon added to the recipes in ACS200 machine in CMi, seems to have the required properties for this project. It has an excellent adhesion to the substrate and has a high resistance towards over-exposure.
  - **Opening (seed layer removal):** As could be observed in the SEM images, the opening step does not completely etch the seed layer next to the structures. One immediate potential solution to this issue is performing the IBE etching twice, once with 0° and the second time with -10°. The latter would result in some fencing which would be later on cleared by the former process.
  - **Release process:** The test wafer for the KOH etch rate test on a-Si is already made during this project, however, due to the lack of it has not been used. It is suggested to run this test and measure the time required for the release of the steps with different feature sizes. Moreover, the same wafer test needs to be fabricated for the Aluminum seed layer in order to provide the maximum control over the etching process.

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# Annex

■ Successful 
 ■ Partial Damage 
 ■ Failed 
 ■ In progress 
 ■ To be done

<b>WAFER TEST 1</b> <b>Substrates: Fused Silica, Amorphous Silicon 2um, Cr (10nm)-Au (150nm)</b>							
Date	Process Description	Machine	Recipe	Parameters	Duration	Result	Notes
19.06.2018	Seed layers	DP650	RTU_Cr_Au	Cr: 6.4 , 5.8 A°/s Au: 12.3 , 13.8 A°/s	Cr: 26 s Au: 115 s	--	--
19.06.2018	Photoresist Coating	ACS	0449	AZ9260_5_5um De-hydration with EBR	15 min/wafer	--	--
19.06.2018	Exposure_CuPlating Structure	MLA	standard	Dose: 275 Def: +1	50 min/wafer	--	--
19.06.2018	Developing	ACS	0949	AZ92605_5um	10 min/wafer	--	--
21.06.2018	Plasma Activation	Tepla +1	2	500 Watts	10 sec	--	--
21.06.2018	Cu Plating	Desaules		Exposed Surface: 20% (CleWin) Current (20% $\times$ 2A): 0.4 A (oscillating up to 0.5)	10 min	7um (DekTak), Meaning the deposition rate has been 0.7 um/min	Preferably test on a dummy first, the bath was down last week and not stable now
21.06.2018	Resist Removal	UFT Resist		Temperature had gone to 88°C	5min+5min		
21.06.2018	Seed Layer Removal	IBE Zone 11	High-IBE.Prc	Angle -10°	47 (40Au+7Cr) sec	SIMS file saved mtamizifar	Flash memory not found in Z11
21.06.2018	Amorphous Silicon Removal with KOH	Base Bench +1	KOH 40%	at 60°C	2hours		- For the next time, use the horizontal holder
21.06.2018	HCl Neutralization	Acid Bench	HCl Neutralization	Room Temperature	few seconds	Cr was attacked and alignment marks were released	Cyrille: Neutralization can be done in Hot water (90°C)
29.06.2018	Al deposition	DP650	RTU_Al	5.8 A°/s, 5.3A°/s	100		
03.07.2018	Photoresist Coating for Dicing	ACS	0449	AZ92605_5um De-hydration with EBR	15 min/wafer		
05.07.2018	Dicing	N/A	N/A	N/A	N/A	The wrong side of the wafer is taped by the CMi operator!!!	

■ Successful  
 ■ Partial Damage  
 ■ Failed  
 ■ In progress  
 ■ To be done

<b>WAFER TEST 2</b> <b>Substrates: Fused Silica, Alu 2um, Cr (15nm)-Au (150nm), simplified alignment marks</b>							
Date	Process Description	Machine	Recipe	Parameters	Duration	Result	Notes
28.06.2018	Plasma Cleaning	Tepla 300	3	500 Watts	1:00 min		
28.06.2018	Sacrificial+Seed layers	DP650	RTU_Al_Cr_Au	Al: 5.8 , 5.3A°/s Cr: 6.4 , 5.8 A°/s Au: 12.3 , 13.8 A°/s	Al: 3700 s Cr: 26 s Au: 115 s	Should be: Al: 2.053um Cr: 15.8 nm Au: 150 nm	rough surface Conclusion:
29.06.2018	Photoresist Coating	ACS	0449	AZ92605_5um Dehydration with EBR	15 min/wafer		
29.06.2018	Exposure_CuPlating Structure	MLA	standard	Dose: 275 Def: +1	40 min/wafer	seemed ok after after the exposure before development	simplified alignment marks as suggested by the dicing CMI page results in lower exposure time
29.06.2018	Developing	ACS	949	AZ92605_5um	10 min/wafer	totally flaked off and ruined resist	Julien says PR is overheated, suggests step exposure
29.06.2018	Resist Removal	Tepla 300	7	500 watts	7mins	decolorized substrate	The heat results in the diffusion of Al atoms -Burnt resist will not go away with plasma easily

"Take-Away Conclusions:

1. Al cannot be sputtered on glass due to low heat conductivity of the substrate
2. Resist overheats and flakes of after development due to low heat conductivity of substrate
3. Al atoms diffuse to gold in 5min O2 plasma due to high temperature "

<b>WAFER TEST 3</b> <b>Substrates: Fused Silica, Amorphous Silicon 2um, Cr (15nm)-Au (150nm), KOH Etch Rate Test of a-Si</b>							
Date	Process Description	Machine	Recipe	Parameters	Duration	Result	Notes
03.07.2018	a-Si thin film measurement	Nanospec	186	5 points		Mean: 20000 nm	
03.07.2018	O2 Plasma for cleaning surface	Tepla 300	3	500 Watts	1min		
04.07.2018	Seed layers	DP650	RTU_Cr_Au	Cr: 6.4 , 5.8 A°/s Au: 12.3 , 13.8 A°/s	Cr: 26 s Au: 115 s		
09.07.2018	Photoresist Coating	ACS	2449	MTAM_AZ92605_5um Dehydration with EBR	15 min/wafer		this recipe has +10°C higher baking temperature
09.07.2018	Exposure_KO-HEtchRate	MLA	standard	Dose: 275 Def: +1	21min/wafer	Design is not centered	
09.07.2018	Developing	ACS	0949	AZ92605_5um	10 min/wafer		
10.07.2018	Plasma Activation	Tepla +1	2	500 Watts	10 sec		
10.07.2018	Cu Plating	Desaules	--	Exposed Surface: 6% (manual calc) Current: 0.200 A (oscillating up to 0.350)	8 min		
10.07.2018	Resist Removal	UFT Resist	--	Temperature had gone to 80°C	5min+5min		
10.07.2018	Seed Layer Removal	IBE Zone 11	High-IBE.Prc	Angle -10°	60 (40Au+7Cr+13) sec	SIMS did not give correct results!	Check with Jofrey next time
	KOH Etch Rate Test of a-Si	Base Bench +1	KOH 40%	at 60°C	10min		
	Neutralization of KOH		H2O 90°C Neutralization	H2O 90°C	10min		
	a-Si thin film measurement	Nanospec	186	5 points			

■ Successful  
 ■ Partial Damage  
 ■ Failed  
 ■ In progress  
 ■ To be done

**WAFER TEST 4**

**Substrates: Fused Silica, Amorphous Silicon 2um, Cr (15nm)-Au (150nm), Will be exposed after the KOH Etch Rate test with wafer 3**

Date	Process Description	Machine	Recipe	Parameters	Duration	Result	Notes
03.07.2018	Plasma Cleaning	Tepla 300	3	500 Watts	1:00 min		
03.07.2018	Seed layers	DP650	RTU_Cr_Au	Cr: 6.4 , 5.8 A°/s Au: 12.3 , 13.8 A°/s	Cr: 26 s Au: 115 s	Should be: Cr: 15.8 nm Au: 150 nm	Shiny as it should be, not like Test 2 wafer
04.07.2018	Photoresist Coating	ACS	0449	AZ92605_5um Dehy- dration with EBR	15 min/wafer		
04.07.2018	Exposure_CuPlating Structure	MLA	standard	Dose: 275 Def: +1	50 min/wafer		
04.07.2018	Developing	ACS	0949	AZ92605_5um	10 min/wafer		
	Plasma Activation	Tepla +1	2	500 Watts	10 sec		
	Cu Plating	Desaules		Exposed Surface: 20% (CleWin) Current: 0.4 A (oscil- lating up to 0.5)	10 min	7um (DekTak), Mean- ing the deposition rate has been 0.7 um/min	Preferably test on a dummy first, the bath was down last week and not stable now
	Resist Removal	UFT Re- sist		Temperature had gone to 88°C	5min+5min		
	Seed Layer Removal	IBE Zone 11	High-IBE.Prc	Angle -10°	47 (40Au+7Cr) sec	SIMS file saved	Flash memory not found in Z11
	Amorphous Silicon Removal with KOH	Base Bench +1	KOH 40%	at 60°C	to be defined by Wafer 3		- For the next time, use the horizontal holder
	Neutralization of KOH		H2O 90°C Neutralization	H2O 90°C	10min		
	Photoresist Coating for Dicing	ACS	0449	AZ92605_5um Dehy- dration with EBR	15 min/wafer		
	Dicing						

WAFER TEST 5 Substrates: Fused Silica, Al 2um (Phys. EVA), Cr (15nm)-Au (150nm)							
Date	Process Description	Machine	Recipe	Parameters	Duration	Result	Notes
03.07.2018	Sacrificial+Seed layers	EVA Physics Dept.	Al_Cr_Au	Should be: Al: 2 um Cr: 15 nm Au: 150 nm	N/A		Looks fine and shiny, Only a small ~500um Golden flake at the corner which was blown away with N2
05.07.2018	Photoresist Coating	ACS	0449	AZ92605_5um Dehydration with EBR	15 min/wafer		
05.07.2018	step exposure	MA6	mtamizifa.test2	550 mj/cm2 , 5 exp, 15 wait	27.5 s		
05.07.2018	Developing	ACS	0949	AZ92605_5um	10 min/wafer	very bad. Julien says it is due to bad adhesion of PR and suggests baking of PR at +10°C higher temperature	
09.07.2018	Resist Stripping	UFT Resist	--	70°C	10min+10min		
09.07.2018	Photoresist Coating	ACS	2449	AZ92605_5um Dehydration with EBR	15 min/wafer		Julien increased the baking temperature
09.07.2018	step exposure	MA6	mtamizifa.test2	550 mj/cm2 , 5 exp, 25 wait	27.5 s		
09.07.2018	Developing	ACS	0949	AZ92605_5um	10 min/wafer	Perfect!	
10.07.2018	Plasma Activation	Tepla +1	2	500 Watts	10 sec		
10.07.2018	Cu Plating	Desaules	--	Exposed Surface: 20% (CleWin calc) Current: 0.400 A (oscillating up to 0.417)	5 min	Dektak: thickness is 2.5um (PR - 3.0um=2.5um)	mildly hit the voltage supply to stabilize the current
10.07.2018	Resist Removal	UFT Resist	--	Temperature had gone to 80°C	5min+5min		
10.07.2018	Seed Layer Removal	IBE Zone 11	High-IBE.Prc	Angle -10°	60 (40Au+7Cr+13) sec	SIMS did not give correct results!	Check with Jofrey next time
11.07.2018	Release	Al Etch Zone 2	H3P04+HNO3	35°C	10min + 30min	HNO3 attacks Cu !	Double check the advice from CMi as it can go very wrong!

■ Successful  
 ■ Partial Damage  
 ■ Failed  
 ■ In progress  
 ■ To be done

<b>WAFER TEST 6</b> <b>Substrates: Borofloat, Al 2um, Cr (15nm)-Au (150nm)</b>							
Date	Process Description	Machine	Recipe	Parameters	Duration	Result	Notes
04.07.2018	Plasma Cleaning	Tepla 300	3	500 Watts	1:00 min		
06.07.2018	Sacrificial+Seed layers	DP650	RTU_Al-8H_Cr_Au	Al: 5.8 , 5.3A°/s Cr: 6.4 , 5.8 A°/s Au: 12.3 , 13.8 A°/s	Al: 3700 s Cr: 26 s Au: 115 s	Should be: Al: 2.053um Cr: 15.8 nm Au: 150 nm	Some parts are shiny and some parts (~40%) are matte Despite the very long waiting time, sputtering does not seem a good option. Request for Lab600 new 441 recipe is sent

■ Successful  
 ■ Partial Damage  
 ■ Failed  
 ■ In progress  
 ■ To be done

**WAFER TEST 7**  
**Substrates: Borofloat, Al 2um (CMi. Lab600), Cr (15nm)-Au (150nm)**

Date	Process Description	Machine	Recipe	Parameters	Duration	Result	Notes
16.07.2018	Plasma Cleaning	Tepla 300	3	500 Watts	1:00 min		
16.07.2018	Sacrificial+Seed layers	Lab600	410) HRN_Al_Cr_Au	Al: 20 kA Cr: 0.150 kA Au: 1,500 kA	180 min total		Perfect shiny surface
17.07.2018	Photoresist Coating	ACS	2449	MTAM_AZ92605_5um Dehydration with EBR	15 min/wafer		
17.07.2018	Exposure_KO-HEtchRate	MLA	standard	Dose: 275 Def: +1	21min/wafer	Design was centered	
17.07.2018	Developing	ACS	0949	AZ92605_5um	10 min/wafer		Let's see what happens with MA6
18.07.2018	Resist Stripping	UFT Resist	--	70°C	10min+10min		
18.07.2018	Photoresist Coating	ACS	2449 (higher bake temperature)	AZ92605_5um Dehydration with EBR	15 min/wafer		Julien increased the bake temperature again
18.07.2018	Developing	ACS	0949	AZ92605_5um	10 min/wafer	Perfect!	
18.07.2018	Surface cleaning+resist removal for 7&8	UFT Resist	--	70°C	5min+5min		
20.07.2018	Plasma Cleaning	Tepla 300	2	500 Watts	0:30 s		

■ Successful  
 ■ Partial Damage  
 ■ Failed  
 ■ In progress  
 ■ To be done

<b>WAFER TEST 8</b> <b>Substrates: Borofloat, Al 2um (CMi. Lab600), Cr (15nm)-Au (150nm)</b>							
Date	Process Description	Machine	Recipe	Parameters	Duration	Result	Notes
16.07.2018	Plasma Cleaning	Tepla 300	3	500 Watts	1:00 min		
16.07.2018	Sacrificial+Seed layers	Lab600	410) HRN_Al_Cr_Au	Al: 20 kA Cr: 0.150 kA Au: 1,500 kA	180 min total		Perfect shiny surface
18.07.2018	Surface Cleaning	UFT Resist	--	70°C	5min+5min		
19.07.2018	Photoresist Coating	ACS	429	ECl 5um_Dehy_EBR	10 min/wafer		
19.07.2018	step exposure	MA6	mtamizifa.test8	450 mj/cm2 , 5 exp, 25 wait	25 s		
19.07.2018	Developing	ACS		ECl3027_5um	10 min/wafer	slightly underexposed PR is detached	
18.07.2018	Resist Cleaning	UFT Resist	--	70°C	5min+5min		
20.07.2018	Plasma Cleaning	Tepla 300	2	500 Watts	0:30 s		
20.07.2018	Ti coating for PR adhesion	DP650	RTU_Ti	Ti: 3.4-3.1 °A/s	40s		shades of a previous mask exposure are visible on the surface, despite having gone through UFT and plasma cleaning

■ Successful  
 ■ Partial Damage  
 ■ Failed  
 ■ In progress  
 ■ To be done

<b>WAFER TEST 9</b> <b>Substrates: Borofloat, Al 2um (CMi. Lab600), Cr (15nm)-Au (150nm)</b>							
Date	Process Description	Machine	Recipe	Parameters	Duration	Result	Notes
16.07.2018	Plasma Cleaning	Tepla 300	3	500 Watts	1:00 min	Plasma Cleaning	Tepla 300
16.07.2018	Sacrificial+Seed layers	Lab600	410) HRN_Al_Cr_Au	Al: 20 kA Cr: 0.150 kA Au: 1,500 kA	180 min total	Sacrificial+Seed layers	Lab600
18.07.2018	Surface cleaning+resist removal for 7&8	UFT Resist	--	70°C	5min+5min	Surface cleaning+resist removal for 7&8	UFT Resist
20.07.2018	Plasma Cleaning	Tepla 300	2	500 Watts	0:30 s	Plasma Cleaning	Tepla 300
20.07.2018	Ti coating for PR adhesion	DP650	RTU_Ti	Ti: 3.4-3.1 °A/s	40s	Ti coating for PR adhesion	DP650
20.07.2018	Surface Activation	Tepla 300	3	500 Watts	1 min	Surface Activation	Tepla 300
20.07.2018	Photoresist Coating	ACS	429	ECl 5um_Dehy_EBR	10 min/wafer	Photoresist Coating	ACS

■ Successful  
 ■ Partial Damage  
 ■ Failed  
 ■ In progress  
 ■ To be done

**WAFER TEST 10**

**Substrates: Borofloat, Al 2um (CMi. Lab600), Cr (15nm)-Au (150nm)**

Date	Process Description	Machine	Recipe	Parameters	Duration	Result	Notes
16.07.2018	Plasma Cleaning	Tepla 300	3	500 Watts	1:00 min		
16.07.2018	Sacrificial+Seed layers	Lab600	410) HRN_Al_Cr_Au	Al: 20 kA Cr: 0.150 kA Au: 1,500 kA	180 min total		Perfect shiny surface
20.07.2018	Plasma Cleaning	Tepla 300	2	500 Watts	0:30 s		
20.07.2018	Ti coating for PR adhesion	DP650	RTU_Ti	Ti: 3.4-3.1 °A/s	40s		
20.07.2018	Surface Activation	Tepla 300	3	500 Watts	1 min		
20.07.2018	Photoresist Coating	ACS	429	ECl 5um_Dehy_EBR	10 min/wafer		

■ Successful  
 ■ Partial Damage  
 ■ Failed  
 ■ In progress  
 ■ To be done

**WAFER TEST 11**

**Substrates: Borofloat, Al 2um (CMi. Lab600), Cr (15nm)-Au (150nm)**

Date	Process Description	Machine	Recipe	Parameters	Duration	Result	Notes
16.07.2018	Plasma Cleaning	Tepla 300	3	500 Watts	1:00 min		
16.07.2018	Sacrificial+Seed layers	Lab600	410) HRN_Al_Cr_Au	Al: 20 kA Cr: 0.150 kA Au: 1,500 kA	180 min total		Perfect shiny surface
20.07.2018	Plasma Cleaning	Tepla 300	2	500 Watts	0:30 s		
20.07.2018	Ti coating for PR adhesion	DP650	RTU_Ti	Ti: 3.4-3.1 °A/s	40s		
20.07.2018	Surface Activation	Tepla 300	3	500 Watts	1 min		
20.07.2018	Photoresist Coating	ACS	429	ECl 5um_Dehy_EBR	10 min/wafer		

■ Successful   
 ■ Partial Damage   
 ■ Failed   
 ■ In progress   
 ■ To be done

<b>WAFER TEST 12</b> <b>Substrates: Borofloat, Al 2um (CMi. Lab600), Cr (15nm)-Au (150nm)</b>							
Date	Process Description	Machine	Recipe	Parameters	Duration	Result	Notes
16.07.2018	Plasma Cleaning	Tepla 300	3	500 Watts	1:00 min		
16.07.2018	Sacrificial+Seed layers	Lab600	410) HRN_Al_Cr_Au	Al: 20 kA Cr: 0.150 kA Au: 1,500 kA	180 min total		Perfect shiny surface
18.07.2018	Surface cleaning	UFT Resist	--	70°C	5min+5min		
18.07.2018	Ti coating for PR adhesion	DP650	RTU_Ti	Ti: 3.4-3.1 °A/s	40s		
19.07.2018	Photoresist Coating	ACS		ECI3027_5um Dehydration with EBR	15 min/wafer		
19.07.2018	step exposure	MA6	mtamizifa.test8	500 mj/cm <sup>2</sup> , 5 exp, 25 wait	25 s		slightly underexposed
19.07.2018	Developing	ACS		ECI3027_5um	10 min/wafer	Perfect!	
19.07.2018	Ti layer removal	Plade Wetbench Zone 2	Ti Etch	RT	30s		
19.07.2018	Cu Plating	Desaules	--	Exposed Surface: 20% (CleWin calc) Current: 0.400 A (oscillating up to 0.430)	8 min	Dektak: thickness is 4um (PR - 2.0um=4um) with very high roughness	mildly hit the voltage supply to stabilize the current
19.07.2018	Resist Removal	UFT Resist	--	Temperature had gone to 80°C	5min+5min		
19.07.2018	Ti layer removal	Plade Wetbench Zone 2	Ti Etch	RT	1min		

19.07.2018	Seed Layer Removal_Au Etch	Acid Bench	KI+I <sub>2</sub>	RT	5min+5min	Attacks Copper faster, opposed to Cyril's assumption	The copper through bad plating is highly porous and etches away very quickly
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