Tri-gate technologies for high-performance power GaN devices

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Abstract

GaN-based electronic devices have great potential for future power applications, thanks to their wide band-gap, high breakdown electric field, and high electron mobility. In addition, these devices can be integrated on large-size Si substrates and enable novel monolithic power integrated circuits (ICs), providing an exceptional cost-effective GaN-on-Si platform to revolutionize current power conversion systems with much higher power density and greater energy efficiency.

Despite all these remarkable advantages, the performance of current GaN-on-Si power devices is still far away from the prospect promised by this material, and further enhancement requires a significant reduction in the ON-resistance of a unit area ($R_{ON}{\cdot}A$) and an increase in the breakdown voltage (V_{BR}) of the device. Moreover, the family of GaN-on-Si power devices is not yet complete, as high-voltage power GaN-on-Si Schottky barrier diodes (SBDs) are still missing on the market in spite of the great demand, restricting the full functionality of GaN-on-Si power solutions.

This thesis proposes tri-gate technologies to overcome these challenges. The common drawback of increased R_{ON} in tri-gate GaN high electron mobility transistors (HEMTs) is resolved, and the exceptional merit of the tri-gate for high V_{BR} is discovered. A novel slanted tri-gate structure is invented to improve the V_{BR} for GaN-on-Si metal-oxide-semiconductor HEMTs (MOSHEMTs) at a fixed A, resulting in a much reduced $R_{ON}{\cdot}A$ product and a record high-power figure-or-merit among GaN-on-Si power transistors. High-voltage power GaN-on-Si SBDs are also achieved based on a judicious design of the tri-gated anode region, demonstrating unprecedented reverse-blocking performance that is dramatically improved from existing technologies, along with excellent integratability with GaN transistors, which is demonstrated in reverse-blocking GaN MOSHEMTs with record voltage-blocking capabilities. Furthermore, a novel multi-channel tri-gate structure is developed in this thesis, deploying multiple 2DEG channels to dramatically reduce the $R_{ON}{\cdot}A$ value while maintaining a high V_{BR} thanks to the tri-gate, resulting in novel multi-channel tri-gate power GaN-on-Si normally-ON/OFF MOSHEMTs and SBDs with state-of the-art performance.

The results in this thesis reveal the extraordinary value of the tri-gate in enhancing the V_{BR} for high-voltage GaN power devices, demonstrate high-performance power GaN-on-Si SBDs that can be rated for 650 V, and unleash the enormous potential of the multi-channel tri-gate approach to dramatically

improve the performance of power GaN devices, offering a complete and effective platform towards the full capabilities of GaN for future efficient power conversion.

Keywords

GaN, power, HEMTs, SBDs, tri-gate, tri-anode, slanted tri-gate, multi-channel tri-gate, breakdown voltage, on-resistance, leakage current.

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Chapter 1 Introduction

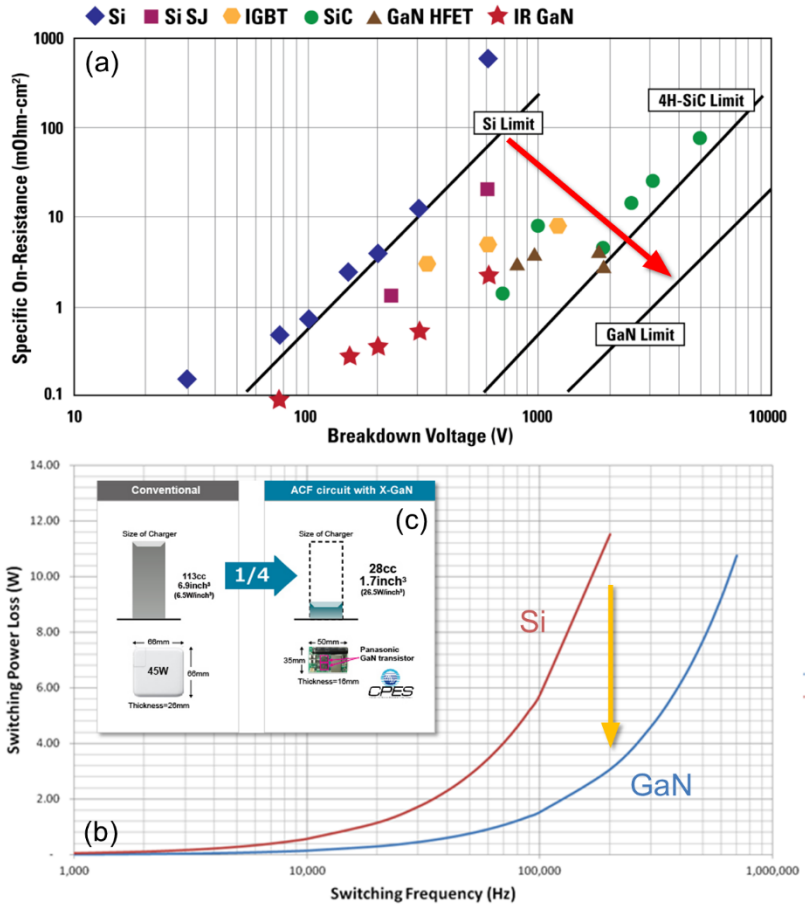
1.1 Advantages of GaN for efficient power conversion

Figure 1.1: Applications of power electronics.

Power conversion is to control and convert electrical energy from one form to another, by modifying the current flow, voltage, frequency and other components of the power based on solid-state electronic devices and circuits. Power electronics is one of the key technologies that have cast the modern electronic era that we enjoy today, and is indispensable in our daily lives, modern industries, and among many others (Fig. 1.1), powering around 40% of the world's energy needs [1].

The key components of a power conversion system are power semiconductor devices, which can include transistors, diodes and thyristors according to different conversion topologies. While conventional Si-based power devices have steadily improved the efficiency and cost of power management in the past a few decades, the rate of such improvement is asymptotically approaching a limit, as a result of the fundamental constriction in the material capabilities of Si [2]. Now it has become a challenge to achieve new power Si devices with higher energy efficiency and power density to meet the growing demands in diminishing carbon emission and shifting to renewable energy.

On the other hand, Gallium nitride (GaN) has emerged as the front-running solution to these issues [3]–[8]. As an extraordinary representative of wide band-gap semiconductors, GaN offers the wide



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band-gap, high electron mobility, high electron saturation velocity, and high breakdown field, yielding much higher Baliga Figure of Merit (BFM), Baliga High Frequency Figure of Merit (BHHFM) and Johnson's Figure of Merit (JFM) over Si (Tab. 1). The unique combination of these remarkable properties in GaN enables novel power devices with low resistive loss (Fig. 1.2(a)), low switching loss (Fig. 1.2(b)) and small switching delay, which are highly desirable to improve the energy efficiency, operation frequency (Fig. 1.2(b)) and power density (Fig. 1.2(c)) for the next generation of power converters.

Table 1.1: Comparison of Si and GaN for power applications.

	Electron mobility ($cm^2/V{\cdot}s$)	**Electron Saturation velocity ($\times 10^7$ cm/s)**	**Band-gap (eV)**	**Breakdown field (10^6 V/cm)**	**BFM**	**BHFFM**	**JFM**
Si	1350	1	1.12	0.3	1	1	1
GaN	2200 (2DEG)	2.2	3.39	3.3	850	98	1090

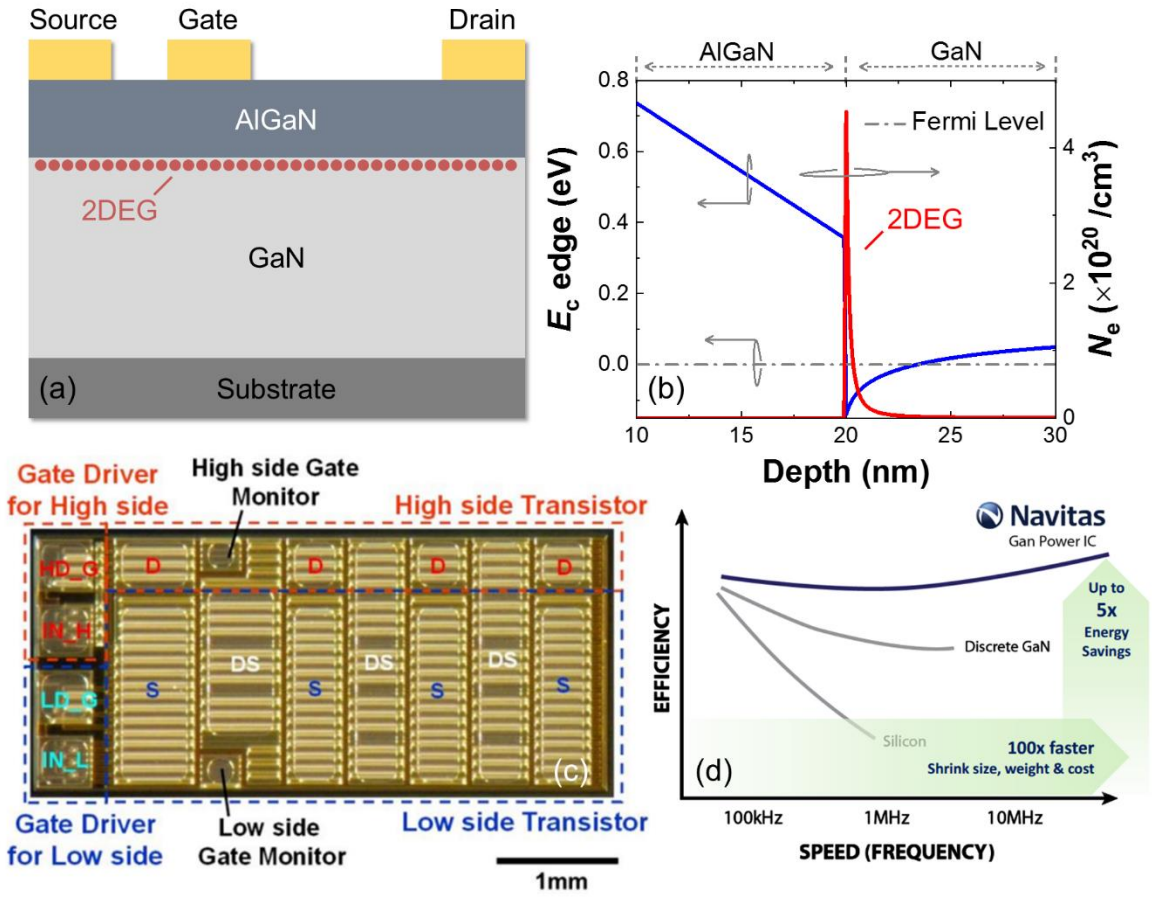
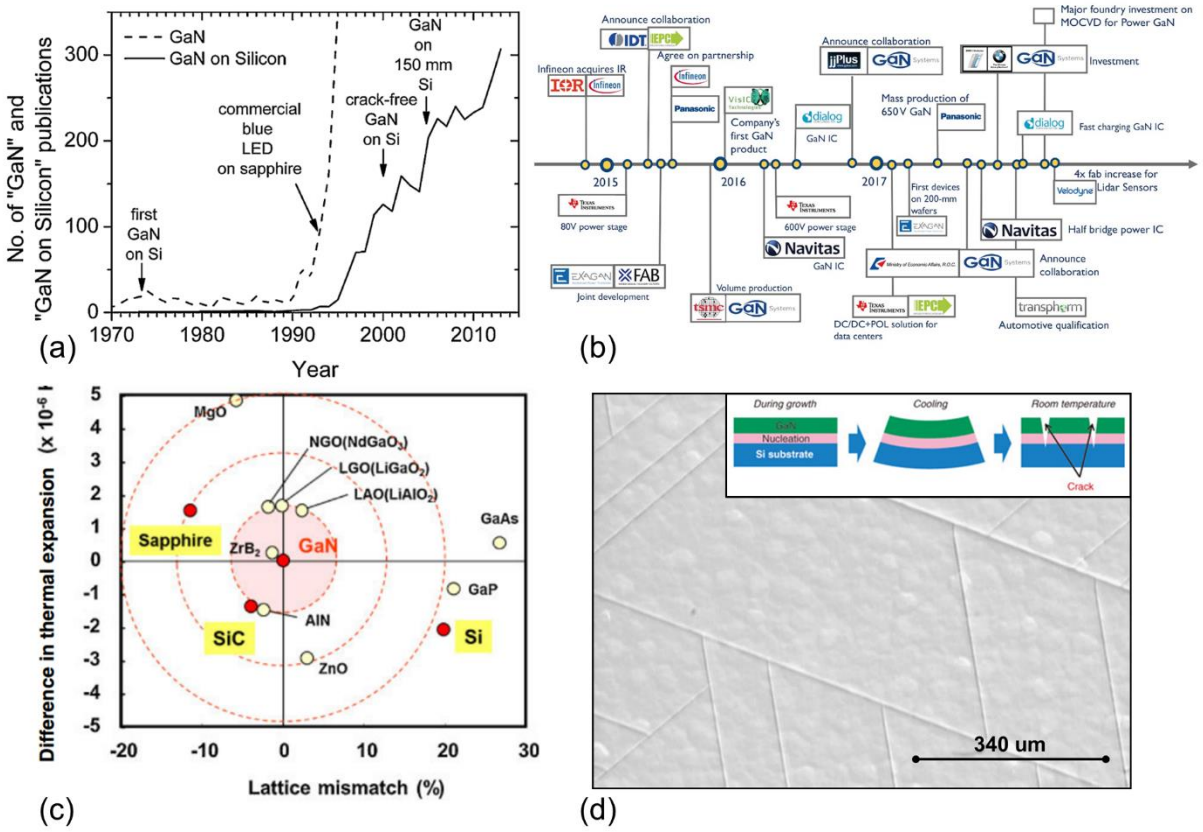


Figure 1.3: (a) Cross-sectional schematic of an AlGaN/GaN high electron mobility transistor (HEMT). (b) Simulated energy band structure of the AlGaN/GaN heterostructure, showing the 2DEG channel at the AlGaN/GaN interface. (c) A monolithic power integrated circuits (ICs) based on the AlGaN/GaN heterostructure. The circuit was demonstrated by Panasonic, and the image was obtained from https://www.psma.com/sites/default/files/uploads/tech-forums-semiconductor/presentations/is164-unlocking-power-gan.pdf. (d) The significant advantages of all-in-GaN power ICs presented by Navitas, which was obtained from https://www.psma.com/sites/default/files/uploads/tech-forums-semiconductor/presentations/is94-gan-power-ics-1-mhz-topologies-technologies-and-performance.pdf.

In addition to the superior material properties, GaN further enables novel high-voltage monolithic power integrated circuits (ICs) that could potentially revolutionize many power applications, thanks to the AlGaN/GaN HEMT technology. Different from conventional Si-based power devices, mainstream GaN power devices are based on a lateral AlGaN/GaN heterostructure, relying on the 2-dimensional electron gas (2DEG) at the AlGaN/GaN interface (Fig. 1.3(a)), generated by spontaneous and piezoelectric polarization effects of the AlGaN barrier layer (Fig. 1.3(b)) [9]. Such 2DEG channel presents excellent electric conductivity due to its high concentration (N_e) and high mobility (μ), which is crucial to enhance the efficiency of a power device. In addition, the lateral current flow along the 2DEG channel results in a lateral scheme for GaN power devices, which greatly facilitates the monolithic integration of different devices and enables novel high-frequency power ICs with dramatically improved performance (Fig. 1.3(c)). As shown in Fig. 1.3(d), all-in-GaN power ICs can significantly



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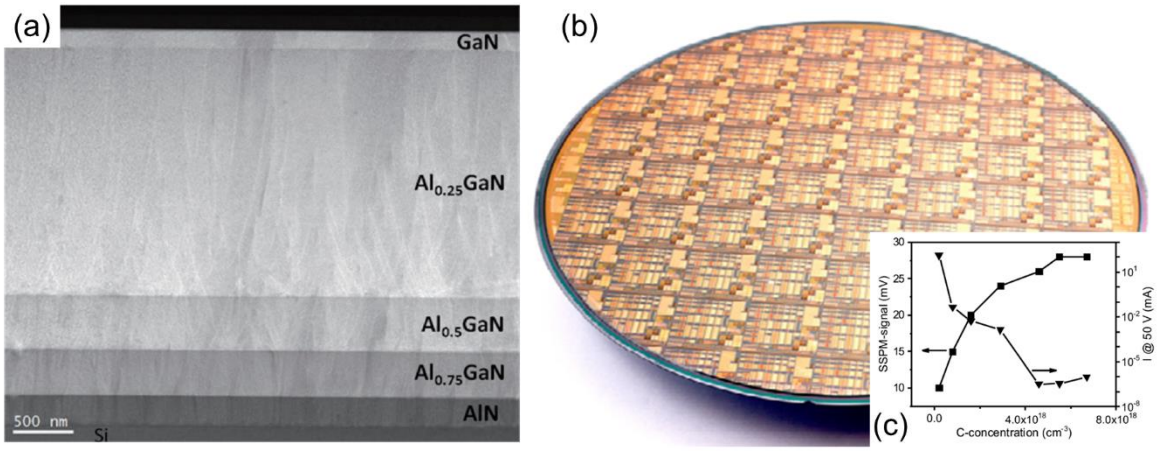
increase the operation frequency and dramatically enhance the efficiency of power converters from conventional technologies based on discrete devices, which are highly demanded for future compact and efficient power conversion.

1.2 Cost-effective GaN-on-Si platform

GaN-on-Si technology is a key enabler for real-world GaN power solutions (Figs. 1.4(a) and (b)). While GaN devices have demonstrated tremendous prospects, they must be cost effective for commercialization, as many power applications are cost-sensitive. A major approach for the cost reduction is to construct GaN power devices on Si substrates based on a mature thin film process. GaN power devices are usually grown on foreign substrates using metalorganic chemical vapor deposition (MOCVD). Among the available substrates, Si is at present the most suited one for GaN power devices, offering low price (0.1 €/cm^2), large sizes (up to 12 inch) and reasonable thermal conductivity,



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while other substrates like SiC (10 €/cm^2, ≤ 6 inch) or sapphire (1 €/cm^2, ≤ 8 inch) are costly and small, and can be even thermally insulating as in sapphire [10].

However, the mismatch in thermal expansion coefficients between GaN and Si (Fig. 1.4(c)) results in huge thermal stress during the post-growth cooling process (inset in Fig. 1.4(d)), and constricts the maximum thickness of GaN-on-Si epi layers by generating cracks (Fig. 1.4(d)), limiting the voltage rating, the curvature, and the yield of the epi layers. This issue is mainly addressed by graded AlGaN [11], [12] or superlattice buffer layers [13] to provide compressive stress to the upper GaN layer during the cooling, thanks to the lattice mismatch between GaN and Al(Ga)N (Fig. 1.4(c)). These approaches have been widely used in the industry and successfully led to thick crack-free GaN-based epi layers on 8 inch Si substrates, as shown in Figs. 1.5(a) and (b). There are also other techniques that could diminish the thermal stress, such as different interlayers, yet they may feature either obvious disadvantages or complicated growth process, which are less approved for mass production.

The second challenge for growing GaN-on-Si power devices is the large buffer leakage current, which increases the OFF-state current (I_{OFF}) and degrades the breakdown voltage of the device (usually defined at the voltage when I_{OFF} reaches 1 µA/mm). This issue is firstly due to the n-type conductivity in unintentionally doped GaN, which is presumably caused by native defects and residual impurities, and degrades the resistivity of the GaN buffer layer. To address this problem, one approach is to dope the GaN layer with carbon atoms, by either methyl radicals or extrinsic precursors, which can introduce acceptor states and compensate the background carriers and impurities, resulting in an enhanced resistivity and a diminished leakage current (Fig. 1.5(c)) [14]. The carbon doping profile should be carefully optimized to minimize its impact on the dynamic performance of the device [15], [16].

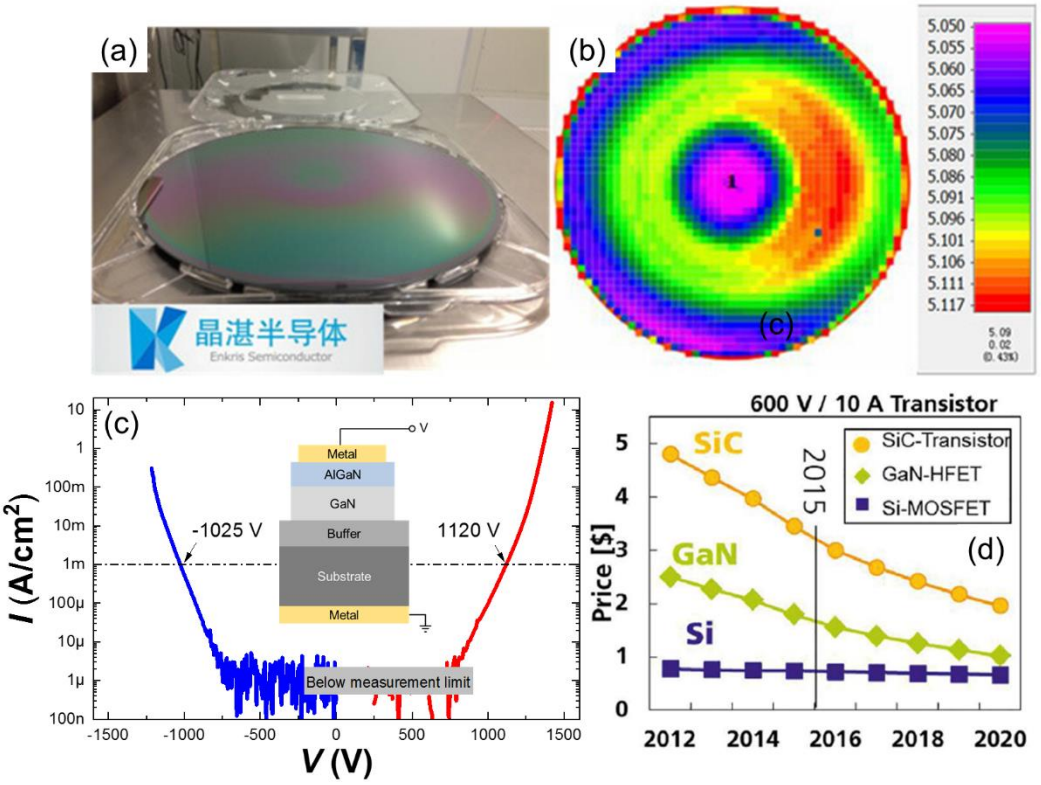


Figure 1.6: (a) A 8 inch creack-free GaN-on-Si wafer with 5 µm thick epi layers for 650 V-rated power devices, and (b) the measured total thickness of the epi layers across the entire wafer, which were grown by Enkris and obtained from https://www.pntpower.com/enkris-semiconductor-shows-1600v-breakdown-gan-hemt-on-200mm-si-wafer/. (c) Room-temperature vertical breakdown characteristics of a 5 µm-thick AlGaN/GaN-on-Si wafer. (d) Expected selling price of a single 600V/10A transistor based on Si, SiC and GaN, obtained from https://www.led-professional.com/resources-1/articles/led-retrofit-based-on-algan-gan-on-si-field-effect-transistor-drivers.

The large buffer leakage current for GaN-on-Si is also limited by the defective AlN nucleation layer, along with the out diffusion of Si atoms from the substrate. So it is very important to improve the crystalline quality of the AlN nucleation layer to better isolate the 2DEG channel from the Si substrate. This is usually tackled by a careful optimization of the AlN nucleation layer, i.e. growth temperature, pressure, III/V ratio and so on.

Nowadays GaN-on-Si has been proven an excellent platform for power devices rated for up to 650 V, thanks to the great efforts of many researchers and the techniques mentioned above. Figure 1.6(a) shows an 8 inch crack-free AlGaN/GaN-on-Si wafer grown by Enkris Inc. for power applications, featuring uniform 5 µm-thick epi layers (Fig. 1.6(b)) and high breakdown voltage over 1000 V at 1 mA/cm^2 (Fig. 1.6(c)), along with small leakage currents and low wafer bow, well fitting the requirements in voltage blocking for 600 V/650 V-rated devices.

The GaN-on-Si technique combines the high-performance of GaN devices and the low cost of mature Si platform, providing a unique platform to enable real-world GaN power solutions. As shown in Fig. 1.6(d), the price of 600 V GaN-on-Si devices is quickly approaching that of counterpart Si devices

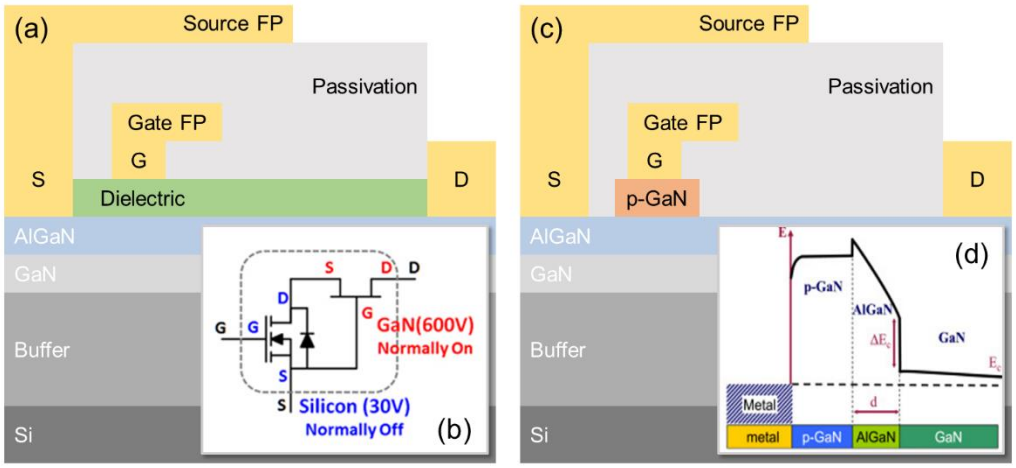


Figure 1.7: (a) Schematic of a normally-ON GaN-on-Si MISHEMT. (b) Schematic of the cascode configuration, which was obtained from https://cpes.vt.edu/library/viewnugget/329. (c) Schematic of a normally-OFF GaN-on-Si HEMT using the p-GaN cap technology. (d) The energy band structure of the p-GaN/AlGaN/GaN heterostructure, which was obtained from https://www.sciencedirect.com/science/article/pii/S1369800117316554#f0005.

and far below that of SiC devices, even though they are not yet in the mass production phase, which can be highly competitive for the market.

1.3 Current GaN-on-Si power device technologies

Up to date, numerous power GaN devices have been demonstrated based on the cost-effective GaN-on-Si platform, among which power HEMTs were first commercialized for power switching applications. In addition to the common field plate (FP) technologies that are widely used for power devices based on various semiconductors, GaN-on-Si HEMTs particularly feature two series of technologies for normally-OFF operation and low dynamic ON-resistance (R_{ON}).

While power switches usually need normally-OFF characteristics for safety reasons, GaN HEMTs are natively normally-ON, limited by the 2DEG beneath the gate electrode. Currently there are two mainstream approaches to address this issue. The first is the cascode configuration [17], which realizes the normally-OFF operation at a circuit level, by matching and connecting a high-voltage normally-ON GaN MISHEMT (Fig. 1.7(a)) to a low-voltage normally-OFF Si MOSFET (Fig. 1.7(b)). The second way is to obtain the normally-OFF operation at the device level, by engineering the gate region of the HEMT using a p-GaN cap layer beneath the gate to deplete the 2DEG and achieve positive threshold voltages (V_{TH}) (Figs. 1.7(c) and (d)) [18], [19]. Each of the methods has its own merits and flaws. The cascode approach sidesteps the complex engineering of the gate region, providing a robust MOS gate that has large positive V_{TH} and can be controlled as in conventional Si MOSFETs. But the GaN MISHEMT in this approach is indirectly controlled by the Si MOSFET, which is not favored for safe operation and reduction of ringing noises [7]. The p-GaN technology enables true normally-OFF devices, offering better control for the slew rate and more flexibility for

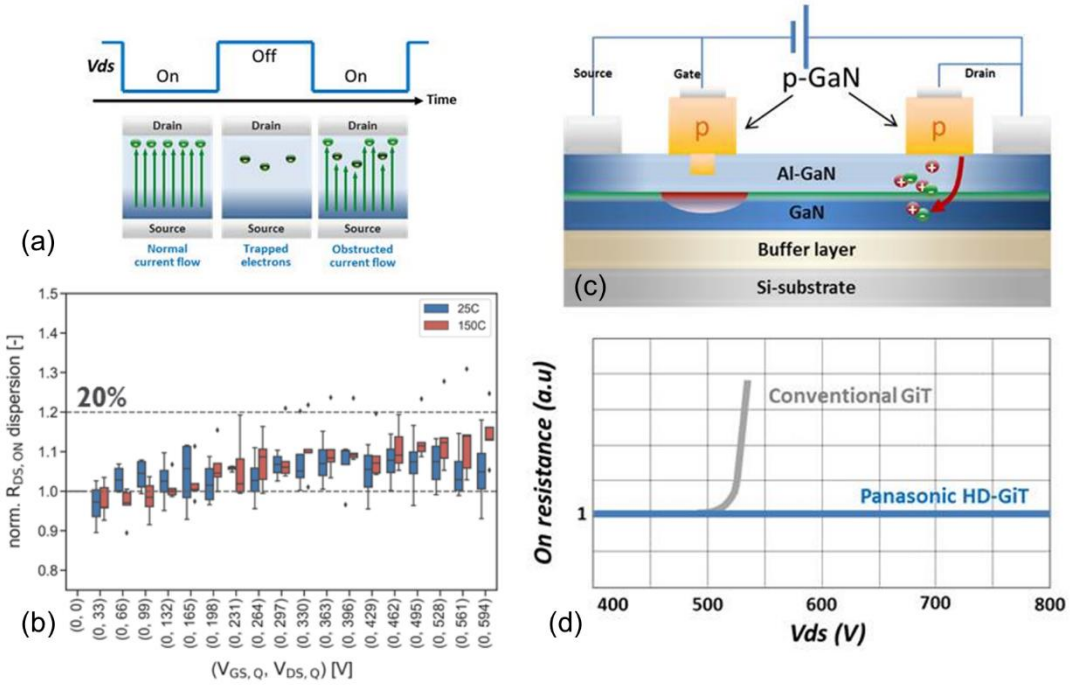
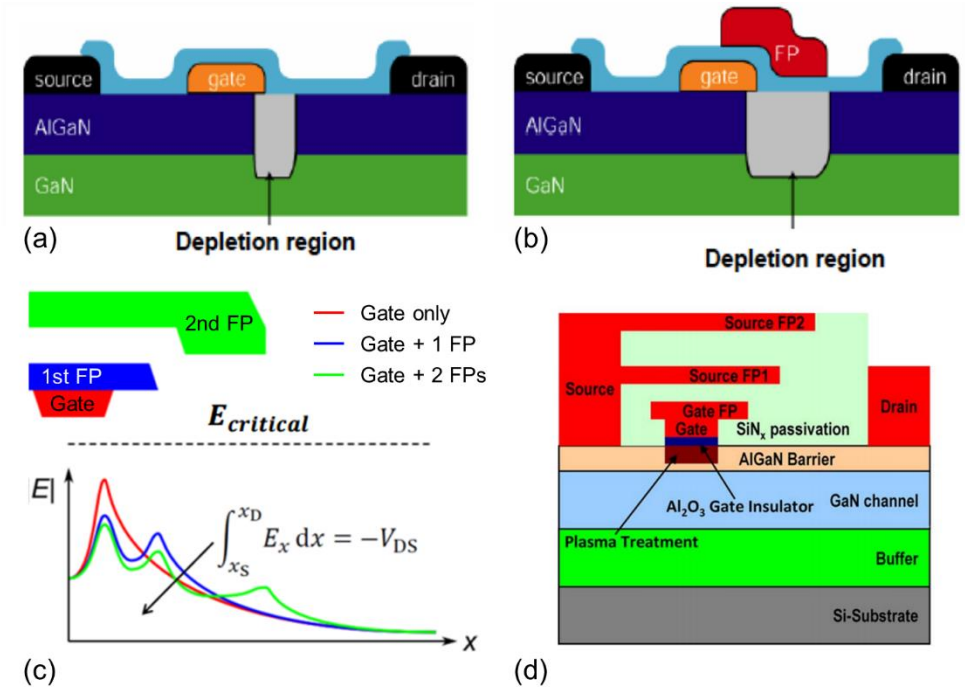


Figure 1.8: (a) Schematic showing the physical origin of the current collapse. (b) Dynamic R_{ON} dispersion of 600 V-rated GaN-on-Si HEMTs versus OFF-state drain voltage, demonstrated by IMEC. (c) Schematic of a normally-OFF GaN-on-Si HEMT with hybrid hole-injection drain electrode, invented by Panasonic. (d) The enhancement in dynamic performance of the device using the hybrid drain electrode. (a), (c) and (d) are obtained from https://na.industrial.panasonic.com/products/semiconductors/x-gan-power/power-devices, and (b) was obtained from https://www.electronicsweekly.com/news/business/imec-offers-gan-si-fab-technology-transfer-2017-06/.

the users [7], yet the maximum gate voltage for such devices is limited to ~6 V due to the absence of the gate insulator, which makes the device quite vulnerable and requires complicated driving circuits for gate protection, degrading the reliability of the conversion system. Current commercial GaN-on-Si power switches are mostly based on these two methods, rated for 650 V and below, and their flaws are addressed by better designing and integrating the peripheral circuits in the converter.

In addition to the techniques for normally-OFF operation, GaN-on-Si power devices also demand effective technologies to reduce their dynamic ON-resistance (R_{ON}). Different from typical Si and SiC power devices, the current flow in GaN-on-Si power devices is lateral and very close to the surface, thus electrons can be trapped by surface states in OFF state and degrading the ON-state current (Fig. 1.8(a)) [7], as the time required for the de-trapping is usually orders of magnitude longer than the typical switching period of the device, resulting in the much higher dynamic R_{ON} than the static R_{ON}. The dynamic R_{ON} can be further degraded with inappropriate carbon doping in the buffer layers, because the carbon doping introduces deep acceptor states which can trap the electrons in the buffer layers at high blocked voltages. Nowadays the issue of dynamic R_{ON} is mainly addressed by diminishing the trap density with surface passivation [20], [21] and optimized carbon doping profile [7], and distributing the electric field using field plates [22], which has resulted in high-performance



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GaN-on-Si power HEMTs with little increase in dynamic R_{ON} (Fig. 1.8(b)). Recently a new approach of a hybrid drain electrode with a hold-injection layer has been demonstrated by Panasonic, as shown in Fig. 1.8(c). This technology can maintain low dynamic R_{ON} even until even 800 V (Fig. 1.8(d)), which is very promising to further push GaN-on-Si power devices for voltage ratings even higher than 650 V.

The FPs in GaN-on-Si devices are not only for low dynamic R_{ON} but also for high V_{BR}. FPs are a common technology used for many power devices to distribute the electric field and enhance the V_{BR}. In GaN power devices, the electric field concentrates at the edge of the gate electrode (or of the anode in case of diodes) in OFF state, as a result of the lateral architecture of the device, resulting the early breakdown and the limited voltage rating for the device [23]–[25]. FPs are necessary to address this issue in current GaN-on-Si power devices. As shown in Figs. 1.9(a) and (b), the FP extends the depletion region towards the high-potential electrode (the drain or the cathode) in OFF state, alleviating the electric field at the edge of the low-potential electrode (the gate or the anode) (Figs. 1.9(c)) and enhancing the breakdown voltage. For high voltage ratings like 650 V, usually a complicated design of multiple FPs [26] are necessary to effective distribute the high electric field, as shown in Figs. 1.9(c) and (d) [27].

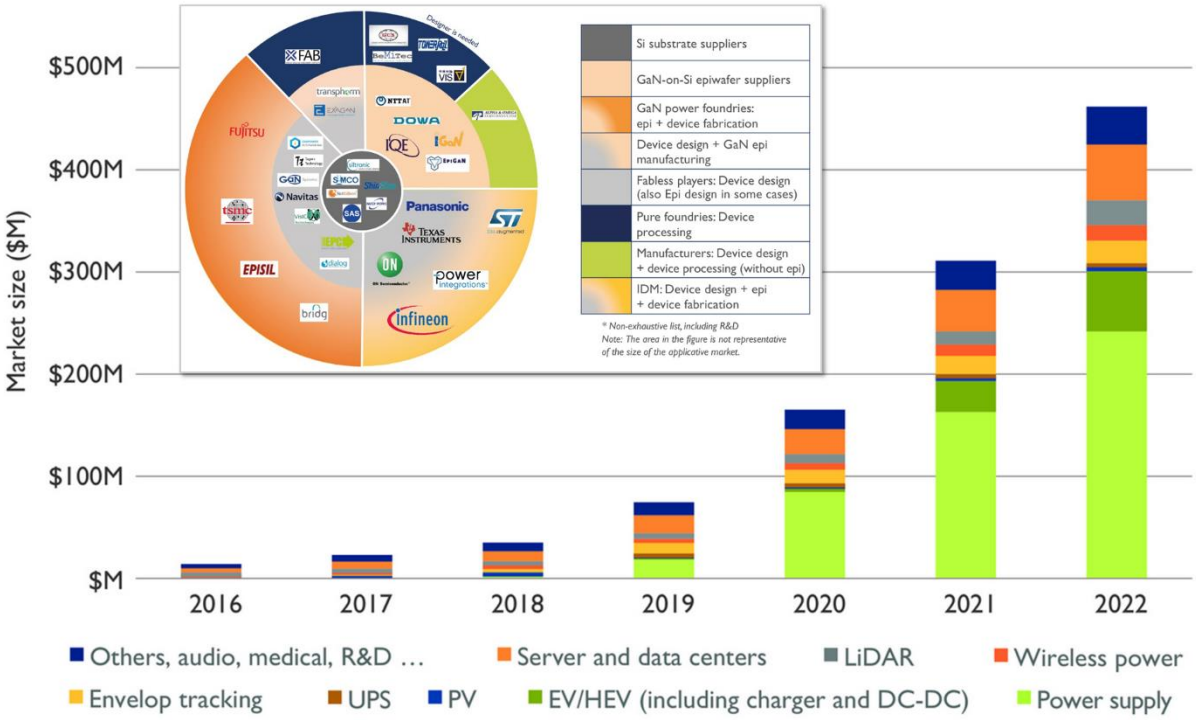

Figure 1.10: The market size of GaN power devices, split by applications. The inset shows an overview of the power GaN industry in 2019. Both figures were obtained from http://www.yole.fr/2014-galery-CS.aspx#I0007a5e9.

1.4 Major challenges

The epitaxy and device technologies presented in Sections 1.2 and 1.3 have successfully led to high-performance power GaN-on-Si devices with competitive cost, presenting magnificent prospects for the future power electronics market (Fig. 1.10), and attracting numerous key players in the semiconductor industry, including Infineon and TSMC (inset in Fig. 1.10). However, the performance of current power GaN devices are still away from the prospect promised by this material (Fig. 1.2(a)), and their future advance will be along the following aspects.

Reduction of R_{ON}·*Area* (R_{ON}·*A*). The R_{ON}·*A* product is a key figure of merit for power devices, which refers to the product of the R_{ON} and the *A* of the device. A smaller R_{ON}·*A* value indicates less resistive loss and more dies per wafer for a given voltage rating, therefore it is essential to enhance the efficiency and reduce the cost of power conversion. However, the reduction of R_{ON}·*A* in GaN power devices is very challenging. As conventional FPs are insufficient to spread the crowded electric field, a large gate-to-drain separation (L_{GD}) is required for the high breakdown voltage, which deteriorates both the R_{ON} and the *A*. For instance, a L_{GD} of 15 μm is typically needed for 650 V-rated GaN power transistors, which increases in the R_{ON} and *A* by 19 % and 36 %, respectively, as compared with the 10 μm-L_{GD} device (Fig. 1.11(a)). To reduce the R_{ON}·*A* in GaN power devices, the high V_{BR} required for a certain voltage rating must be achieved at a smaller L_{GD}, so it is absolutely necessary to develop novel FPs that can better distribute the electric field and enhance the V_{BR} at a fixed L_{GD}.

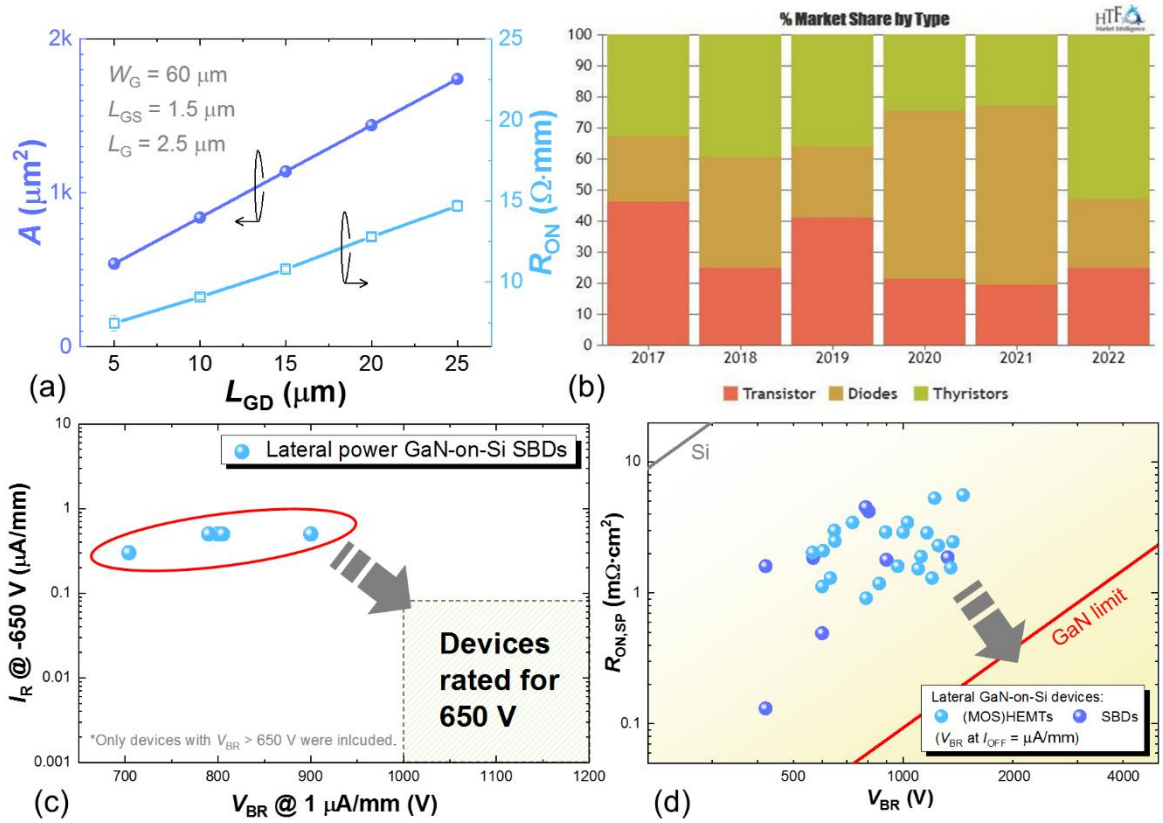

Figure 1.11: (a) Dependence of area (A) and ON-resistance (R_{ON}) of GaN-on-Si MOSHEMTs on the gate-to-drain distance (L_{GD}). (b) Market share of power semiconductor devices by device type, obtained from https://www.openpr.com/news/1001380/Latest-Report-of-Discrete-Power-Device-Market-Size-Share-Growth-Trends-and-Forecast-2018-2022.html. (c) Reverse leakage current (I_R) and V_{BR} of current lateral power GaN-on-Si SBDs. (d) Specific R_{ON} ($R_{ON,SP}$) versus breakdown voltage (V_{BR}) of current power GaN-on-Si devices, in which the V_{BR} was defined at a OFF-state leakage current (I_{OFF}) of 1 µA/mm.

High-performance GaN-on-Si power SBDs. Power diodes are indispensable in nearly every topology of power converters, thus holding a great share of the power device market (Fig. 1.11(b)). While GaN-on-Si SBDs are highly promising as power diodes, thanks to the small turn-on voltage, the zero reverse recovery time, and the low cost, they are not yet available on the market, leaving the family of GaN-on-Si power devices incomplete. This issue is mainly limited by the poor V_{BR} and large leakage current in GaN-on-Si SBDs (Fig. 1.11(c)), which are far away from the requirements of 650 V-rated devices, i.e. $I_R \leq 0.1$ µA/mm at -650 V and $V_{BR} \geq 1000$ V at 1 µA/mm (preferably with grounded substrate). Such poor voltage-blocking capability is neither well understood nor resolved, and fundamentally restricts the voltage rating and energy efficiency of the SBDs. Consequently, it is crucial to resolve the voltage-blocking issue for GaN-on-Si SBDs to enable high-voltage GaN-on-Si SBDs and unleash the full functionality of the GaN-on-Si power solutions.

To unleash the full potential of GaN. The exceptional properties of GaN have led to excellent devices for power applications. Nevertheless, the performance of current GaN devices is still far below the prospect promised by this material (Fig. 1.11(d)). To enhance the power conversion systems for

a greener and more sustainable future, further improvements in the energy efficiency and power density of GaN power devices are essential, which requires a significant reduction in R_{ON}, increase in V_{BR}, while maintaining high switching speed at high frequencies. Therefore it is crucial to develop novel device technologies based on both material and device engineering to unleash and even outperform the full potential of GaN.

1.5 Thesis outline

This thesis aims to overcome the challenges outlined above by developing unconventional tri-gate technologies. The remainder of this thesis is organized as follows:

Chapter 2 elucidates the impact of tri-gates on the characteristics of GaN transistors, including V_{TH}, R_{ON}, transconductance (g_m), current capability, trench conduction, thermal resistance and gate charge. The common issue of large R_{ON} resistance in tri-gate GaN devices is resolved, and the core values of the tri-gate in modulating the V_{TH} and providing a superior 3-dimensional gate control are revealed, along with other advantages in normally-OFF operation and reduced thermal resistance. This chapter is based on the published results of this thesis work in Refs. [28]–[30].

Chapter 3 discloses the concept of novel field plates based on the slanted tri-gate structure for high-voltage lateral GaN power devices, and demonstrates high-performance slanted tri-gate GaN-on-Si MOSHEMTs with high breakdown voltage and record high-power figure of merit. This chapter is based on the published results of this thesis work in Refs. [31], [32].

Chapter 4 reveals the unique value of the tri-gate technology in diminishing the leakage current for lateral GaN SBDs, demonstrates GaN-on-Si slanted tri-gate SBDs with unprecedented voltage blocking performance, and presents high-voltage reverse-blocking GaN-on-Si power transistors based on a monolithic integration of GaN-on-Si power transistors and slanted tri-gate SBDs. This chapter is based on the published results of this thesis work in Refs. [33]–[37].

Chapter 5 demonstrates a novel multi-channel tri-gate technology as a promising platform to unleash the full potential of GaN, based on an intensive and coupled material research and device engineering, which opens tremendous opportunities for future efficient electronics even in many other applications. This chapter is based on the published results of this thesis work in Refs.[38], [39].

Chapter 6 concludes the thesis and presents some future works.

Chapter 2 Tri-gate technologies for GaN devices

2.1 Introduction

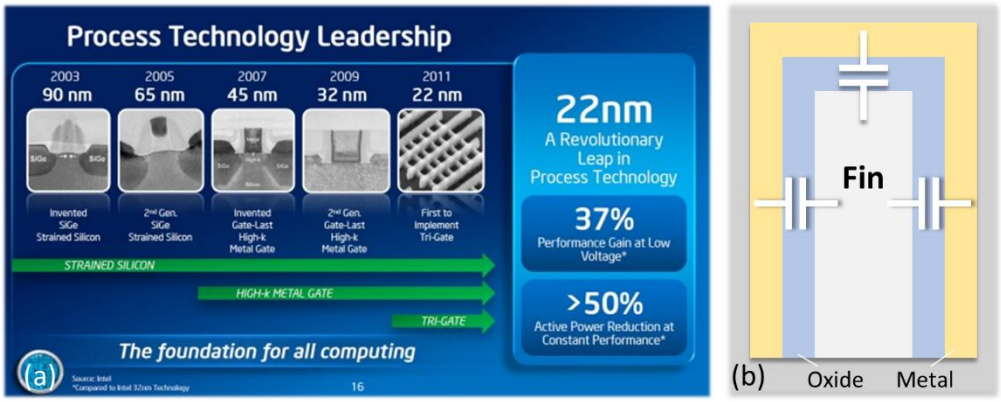

Figure 2.1: (a) Roadmap of logic transistor technologies for processors, obtained at https://www.extremetech.com/. (b) Cross-sectional schematic of a tri-gate FinFET.

The tri-gate architecture was firstly invented by Intel research scientists in 2002 to address the short channel effect in ultra-scaled Si MOSFETs [40], which has been a significant success for nodes below 32 nm (Fig. 2.1(a)). Compared to conventional planar MOSFETs, tri-gate transistors feature 3D gate electrodes warped around semiconductor fins, offering increased on-state current (I_{ON}) and far reduced off-state leakage current (I_{OFF}), thanks to the wider conductive channel and larger gate capacitance (C_G) in a given device footprint, respectively (Fig. 2.1(b)). These remarkable advantages of the tri-gate enable processors to operate at a lower supply voltage along with a lower power consumption, resulting in substantial enhancement in processor performance, and rendering the tri-gate as the key technology to continue Moore's Law.

Soon after its first demonstration in Si, the tri-gate attracted great attention for the nitride community to enhance the performance of GaN power and RF devices. In 2008, K. Ohi *et al.* demonstrated the first tri-gate GaN HEMT using a AlGaN/GaN-on-sapphire heterostructure, revealing the excellent current stabilities in this device [41]. Later in 2009, the same author presented that the V_{TH} in tri-gate GaN HEMTs can be modulated by the fin width (w_{fin}) in the tri-gate region, along with reduced I_{OFF} and *SS* [42]. M. Azize *et al.* shed some light the dependence of V_{TH} on w_{fin} by the strain relaxation of the AlGaN/GaN fins [43] and then demonstrated tri-gate GaN MOSHEMTs using Al_2O_3 as the gate

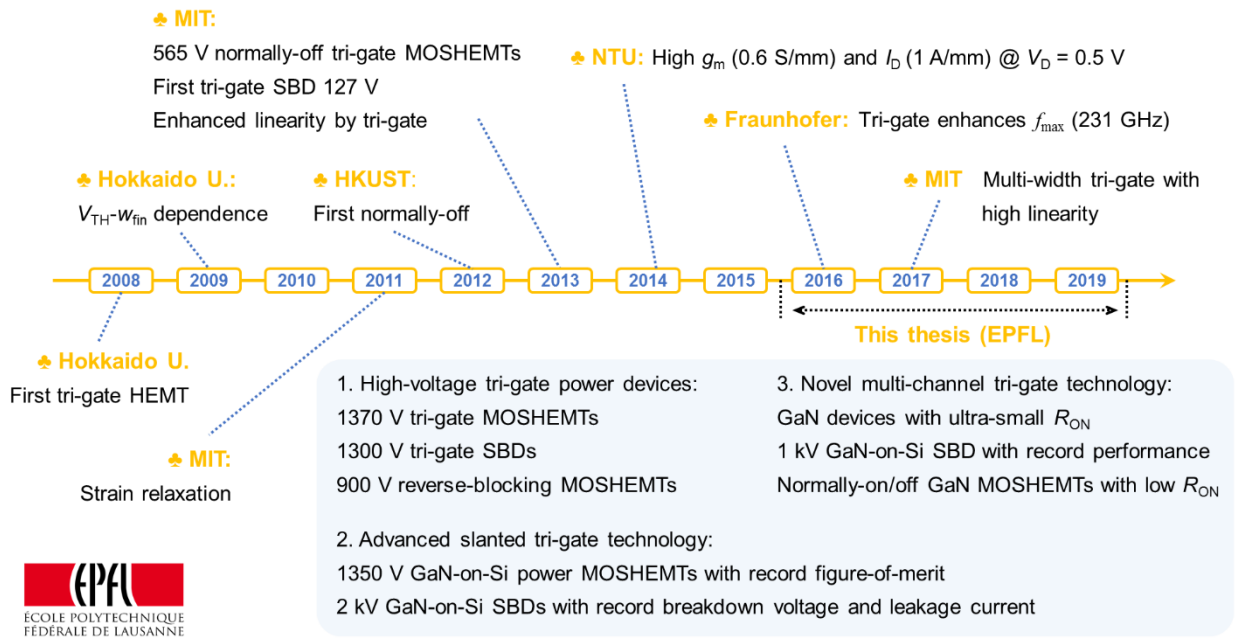

Figure 2.2: Roadmap for tri-gate GaN electronics devices.

dielectric [44]. The dependence of V_{TH} on w_{fin} was then used to obtain normally-off operation, which is highly desirable for power switching applications for safety reasons, as demonstrated in 2012 by S. Liu *et al.* [45], presenting the first normally-off tri-gate GaN HEMT by narrowing the fins to 90 nm (V_{TH} determined by extrapolation of the transfer curve in linear scale). Later in the same year, B. Lu *et al.* [46] showed that the V_{TH} in tri-gate GaN MOSFETs can be further pushed to 0.78 V using a recessed tri-gate structure (V_{TH} determined from extrapolation of the transfer curve in logarithmic scale), along with a high breakdown voltage of 565 V at 0.6 µA/mm. In 2013, E. Matioli *et al.* [47] discovered the unique value of the tri-gate in diminishing the I_{OFF} in lateral GaN SBDs. Based on these milestones, more remarkable progresses have been made for tri-gate GaN devices since 2013, revealing more advantages of tri-gate GaN devices, such as excellent linearity, small *SS*, high trans-conductance, and good current stability, which have been reported in Refs. [48]–[87], as summarized in Fig. 2.2.

While the tri-gate has demonstrated plenty of advantages for GaN electronic devices, its application for GaN power devices has halted since 2013 due to the following reasons. Firstly, the V_{BR} of tri-gate GaN devices are limited to 565 V [46] in MOSHEMTs and 127 V and SBDs [47], which are insuffi-cient for high-voltage power applications. For instance, typical 650 V-rated GaN-on-Si power devices require V_{BR} over 1000 V, which is far beyond these values. In addition, the true merits of the tri-gate for high-voltage power devices have not yet been discovered, while other advantages such as reduced *SS* and enhanced linearity are more for low operating voltages and less attractive for power devices. Moreover, the tri-gate technology has an essential drawback, as it degrades the R_{ON} and $I_{D,max}$ of the

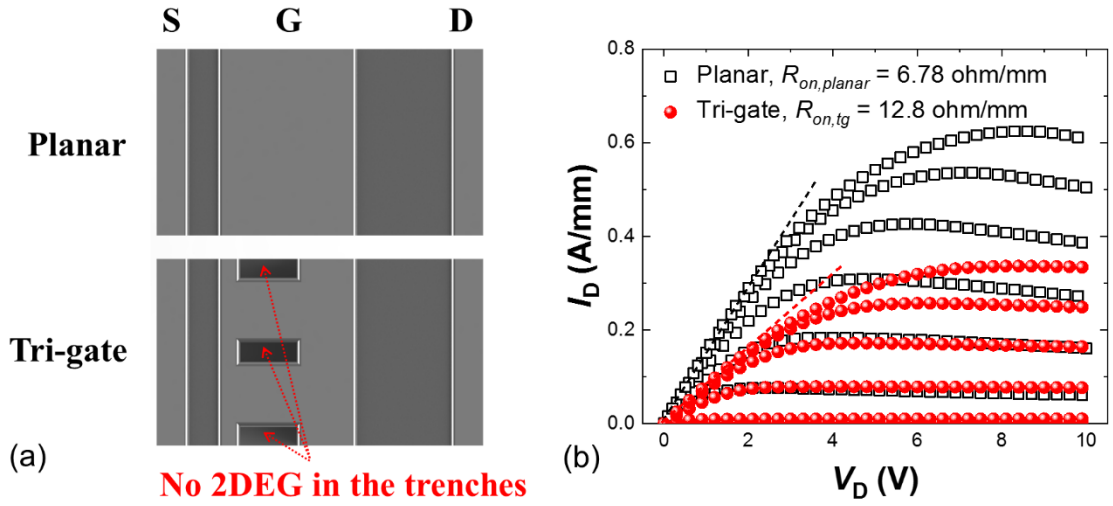

Figure 2.3: (a) Top-view schematics of planar and tri-gate MOSHEMTs. (b) Output characteristics of a planar and tri-gate AlGaN/GaN MOS-HEMT, measured using V_G from -4 to 6 V with a step of 2 V and normalized by the width of device footprint of 150 µm.

device. To construct the tri-gate, a portion of the 2DEG has to be selectively removed by etching to form the fins, which narrows the effective channel in the tri-gate region and degrades total conductance of the device, resulting in a smaller $I_{D,max}$ and a larger R_{ON} (as shown in Fig. 2.3). Such degradation deteriorates the current capability and the energy efficiency of the device, leaving the tri-gate structure less promising for power applications.

To enhance GaN power devices using tri-gate technologies, these issues must be resolved, which are among the main goals of this thesis. In this chapter, we thoroughly investigate tri-gate GaN devices to understand the impact of tri-gate on device characteristics, resolve the degradation in R_{ON} and $I_{D,max}$ caused by the tri-gate by optimizing its geometries, and reveal more advantages of the tri-gate in reducing the thermal resistance and gate charge.

2.2 Impact of fin width on transfer characteristics

To understand the impact of tri-gate on transfer characteristics of the devices, we fabricated tri-gate AlGaN/GaN-on MOSHEMTs on Si with different w_{fin} (Figs. 2.4(a) and (b)). The AlGaN/GaN epitaxy consisted of 3.75 µm of buffer, 0.3 µm of un-doped GaN (u-GaN) channel, 23.5 nm of AlGaN barrier and 2 nm of u-GaN cap layers. The tri-gate MOSHEMTs had different w_{fin} but the same nominal filling factor ($FF = w_{fin}/(w_{fin} + s)$) of 50% ($s$ and w_{fin} in Fig. 2.4 were about the same), along with the same width of the device footprint ($w_{footprint}$ = 60 µm). The fins were 700 nm-long (l_{fin}), and 2 µm and 11.3 µm apart from the source and drain electrodes, respectively. The gate metal was 2.5 µm-long, covering the entire length of the fins and extending 0.5 µm and 1.3 µm towards the source and drain electrodes, respectively.

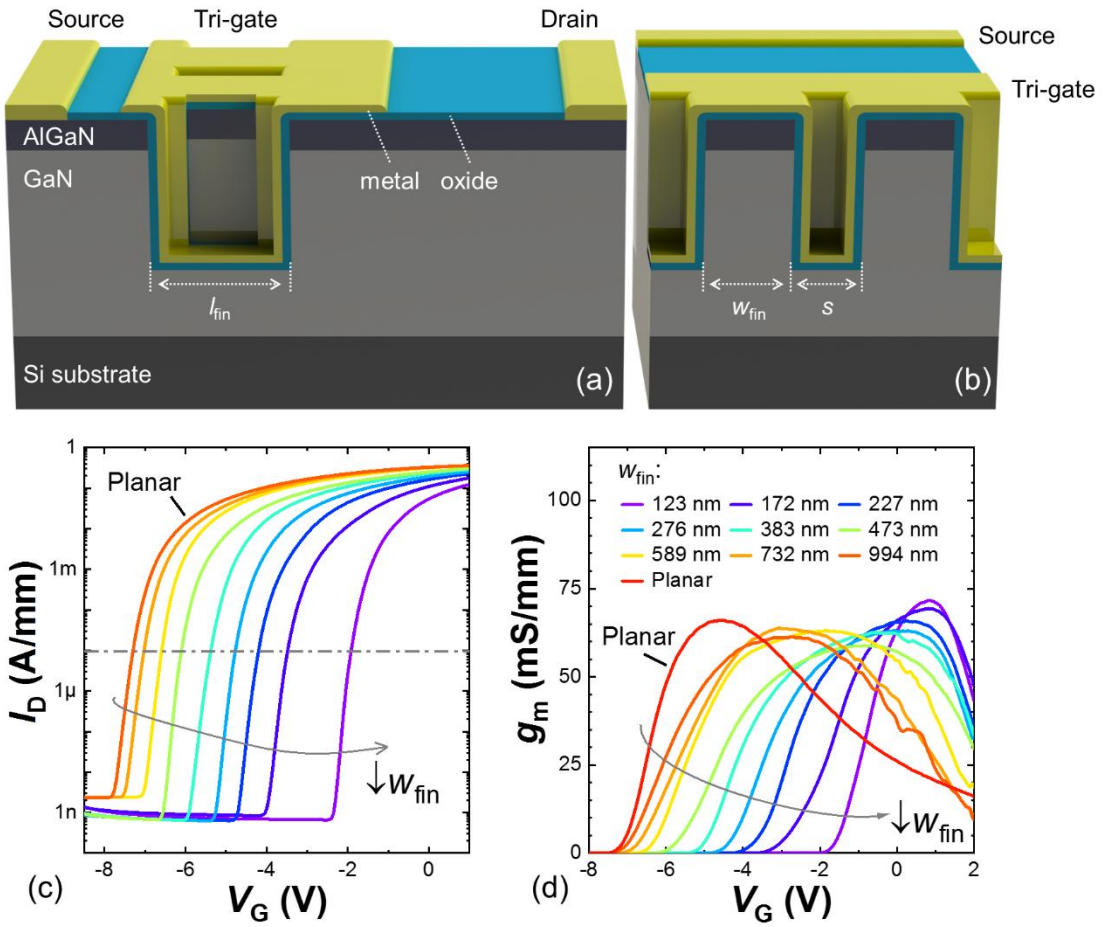

Figure 2.4: Schematics of (a) the tri-gate MOSHEMTs and (b) its tri-gate region. The AlGaN/GaN epitaxy consisted of 3.75 µm of buffer, 0.3 µm of un-doped GaN (u-GaN) channel, 23.5 nm of AlGaN barrier and 2 nm of u-GaN cap layers. Average (a) I_D-V_G and (b) g_m-V_G characteristics in the tri-gate AlGaN/GaN MOSHEMTs with different w_{fin}, measured at V_D = 5 V and normalized by the width of the device footprint. Published in Ref. [30].

The device fabrication started with e-beam lithography to define the fins and mesa, which were etched with a depth of 166 nm using Ar/Cl_2-based inductively coupled plasma (ICP). Ohmic metals (Ti/Al/Ni/Au) were then formed by lift-off and annealing processes, followed by 20 nm Al_2O_3 as the dielectric and Ni/Au as the gate metals. All measured current values were normalized by $w_{footprint}$, and the standard deviation was determined from about 10 devices of each type.

Transfer characteristics of tri-gate GaN MOSHEMTs are significantly impacted by w_{fin}. As shown in Fig. 2.4(c), V_{TH} increased and *SS* decreased with narrower fins. In planar MOSHEMTs, V_{TH} was -7.43 ± 0.07 V and *SS* was 98 ± 14 mV/dec, which were improved by the tri-gate with w_{fin} of 123 nm to -1.68 ± 0.26 V and 83 ± 5 mV/dec, respectively. These results are consistent with other works in the literature [46], [86] and indicate a better electrostatic control using the tri-gate.

The enhanced control in tri-gate GaN transistors however does not necessarily improve the g_m as usually expected. As shown in Fig. 2.4(d), g_m firstly reduced to 59.1 ± 2 mS/mm when w_{fin} was decreased to 473 nm, which is smaller than in planar devices (66.1 ± 2 mS/mm), but then increased

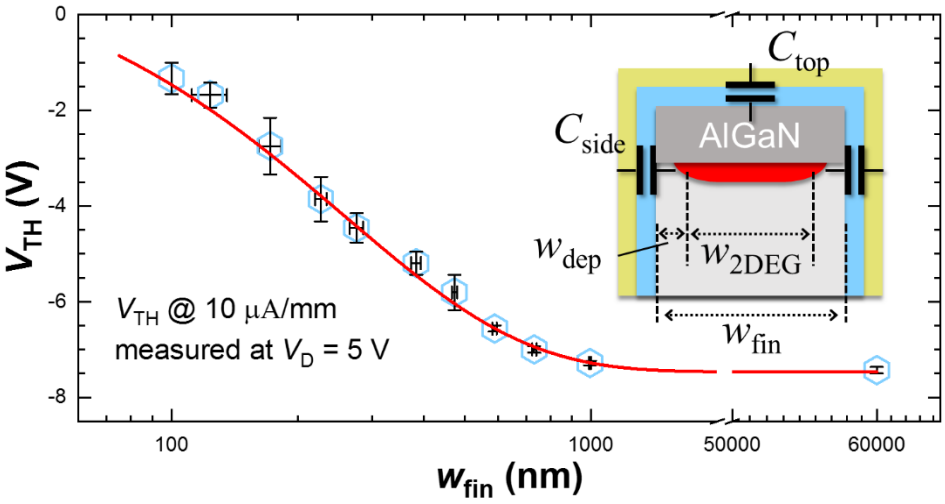

Figure 2.5: Summarized dependence of V_{TH} on w_{fin}, in which w_{fin} was measured by scanning electron microscopy (SEM) and the V_{TH} was defined at 10 μA/mm. The inset illustrates the effect of sidewall depletion in distributing the 2DEG across a fin. Published in Ref. [30].

to 71.9 ± 2 mS/mm at w_{fin} of 123 nm. This phenomenon is mainly determined by the trade-off between electric conductivity and electrostatic control of the channel. By replacing the planar gate with wide tri-gates, the electrical conductivity of the device was degraded due to the fin etching, with limited enhancement in electrostatic control, resulting in a decreased g_m. By narrowing further the fins, the tri-gate control was greatly enhanced, overcoming the degradation in conductivity and resulting in a higher g_m.

The tri-gates can also reduce the source resistance and improve the linearity of g_m, as suggested in the literature [67], however it depends on w_{fin}, as shown in Fig. 2.4(d). While devices with wider tri-gates did exhibit flatter g_m peaks than in planar devices, the full width at half maximum (FWHM) of the g_m was only about 2.9 V at w_{fin} = 123 nm, which was much smaller than that of the planar device (5.5 V). Although the underlying mechanism for this observation is not yet clear, it is likely due to the significant increase in capacitance per fin area (C_{fin}) with narrowing fins (which will be discussed later). An alternative approach to enhance the linearity is to integrate parallel fins with different w_{fin} in a single tri-gate device [87]. Such multi-w_{fin} tri-gate transistors function as parallel transistors with different V_{TH}, which can greatly enhance the linearity thanks to the smooth dependence of V_{TH} on wfin in tri-gate GaN transistors (Fig. 2.5).

2.3 Dependence of threshold voltage on the fin width

The smooth dependence of V_{TH} on w_{fin} (Fig. 2.5) is one of the most important features of tri-gate GaN devices, which can be used to control the breakdown voltage, leakage current, as well as the linearity, and can be further adapted to form lateral AlGaN/GaN field effect rectifiers [88] or current limiting diodes [89]. This dependence of V_{TH} on w_{fin} is determined by several reasons, including the increased

C_{fin} and the reduced N_s in narrower fins caused by strain relaxation and sidewall depletion, which can be described in more details as follows:

1) Increased capacitance: a simplified model of a tri-gated fin includes three capacitors (inset of Fig. 2.6). The top capacitor (C_{top}) is formed by the gate dielectric and the barrier layer, and the two sidewall capacitors ($2 \cdot C_{side}$) are formed by the oxide and parts of the fin body. C_{side} is a dynamic value that depends on both w_{fin} and V_G, and increases as w_{fin} reduces, similarly to double-gate junctionless transistors. It should be noted that the C_{top} can also increase as w_{fin} decreases due to the fringing electric field, especially when w_{fin} approaches the thickness of the barrier and the dielectric layers.
2) Strain relaxation: The strained AlGaN/GaN heterostructure starts to relax after the fin etching by elastic deformation, which partially relieves the strain and reduces the N_s. Such relaxation highly depends on the dimension of the fins [43], [90], and can diminish the charges from both piezoelectric and spontaneous polarization effects.
3) Sidewall depletion: Carriers within the fins are depleted within a certain width (w_{dep}) from the sidewalls towards the fin center (inset in Fig. 2.6). Thus N_s, even at the center of the fin, can be affected by sidewall depletion, which is a crucial factor that allows to achieve normally-off tri-gate GaN transistors. In addition, w_{dep} is also important to determine the equivalent width of the 2DEG (w_{2DEG}) within each fin and extract an equivalent N_s.

2.3.1 Effect of the increased gate capacitance

We investigated these three factors to understand the V_{TH}-w_{fin} dependence in tri-gate GaN transistors. Tri-gate AlGaN/GaN MOS capacitors were fabricated (Figs. 2.6(a) and (b)) and their *C*-*V* characteristics were measured (Fig. 2.6(c)), in which the C_{fin} was normalized by top surface area of the fins, namely $w_{fin} \times l_{MOS} \times N_{fin}$, in order to represent the control of the 2DEG, which is only present within the fins. The planar capacitor presented a nearly constant capacitance, which dropped sharply when V reached $V_{TH.}$ In contrast, the depletion of tri-gate capacitors was progressive with applied V. C_{fin} reduced gradually as V approached V_{TH}, with a steeper slope for smaller w_{fin}, since the sidewall gates progressively depleted the 2DEG from the sides to the center of the fin. Considering that C_{fin} of the tri-gate varies with the voltage and is difficult to quantify, here we propose an effective $C_{fin,eq} = Q/|V_{TH}|$, in which Q was the charge determined from the integration of C_{fin}, to explore the dependence of tri-gate control on w_{fin}. As shown in Fig. 2.6(d), the $C_{fin,eq}$ increased with narrowing fins, especially for $w_{fin} < 200$ nm. When $w_{fin} = 123$ nm, the $C_{fin,eq}$ was as high as 342 ± 34 nF/cm^2, which is about

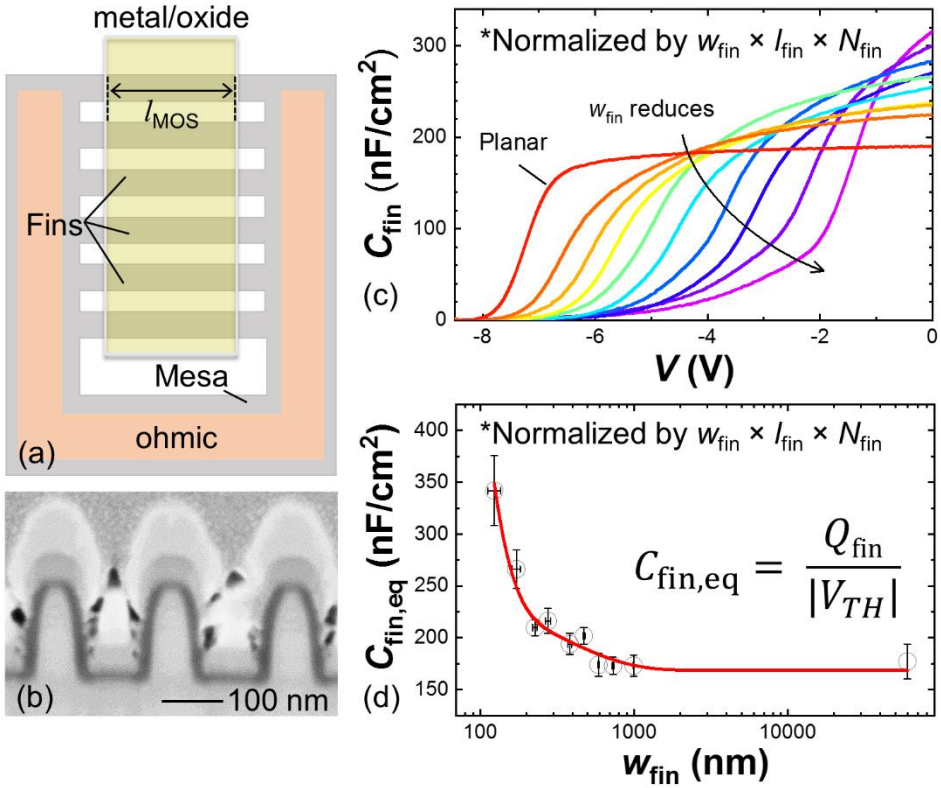

Figure 2.6: (a) Schematic of the fabricated tri-gate MOS capacitor. (b) Cross-sectional SEM image of a tri-gate MOS structure fabricated on a dummy sample, tilted by 52°. (c) Average capacitance per fin area (C_{fin}) with different wfin, measured at 1 MHz. (d) Calculated effective capacitance per fin area ($C_{fin,eq}$) versus w_{fin}. All capacitors had the same wfootprint of 60 µm and *FF* of 0.25. The length of the anode (l_{MOS}) metal was 3 µm and l_{fin} was 4 µm. Capacitance values here were normalized by the top surface area of the fins (w_{fin} × l_{MOS} × N_{fin}) to understand the control of the 2DEG, in which N_{fin} refers to the number of fins in a single device. Published in Ref. [30].

twice the value of the planar capacitor (177 ± 17 nF/cm^2). This effect reflects the enhanced electro-static control that contributed to the positive shift in V_{TH} with reduced w_{fin}. Figure 2.6(d) offers general guidelines for the application of tri-gate structures: the large $C_{fin,eq}$ for w_{fin} < 200 nm is suited for addressing the short channel effect, while w_{fin} around 200 nm is more favorable for power and RF devices, offering the benefits of the tri-gate, such as in tuning the V_{TH}, the g_m and the linearity in a wide range (Figs. 2.6(c) and (d)), but without the significant increase in $C_{fin,eq}$.

2.3.2 Effect of the strain relaxation and sidewall depletion

Strain relaxation and sidewall depletion also cause a positive shift of V_{TH} by reducing the N_s in the fins. To extract N_s it is crucial to precisely determine w_{2DEG}, which was extracted from AlGaN/GaN fin-based Hall crosses (Fig. 2.7(a)) [91], [92]. R_{xx} between two opposite electrodes was measured as a function of the applied magnetic field *B*, which shows two shoulders at *B* = ± 3.34 T (Fig. 2.7(b)). This is due to electron back-scattering effect, which is a geometrical phenomenon that results in the observed peaks in R_{xx} when $w_{2DEG} \approx 0.55 \cdot l_c$ [92]. Here the l_c refers to the cyclotron radius of the circular orbit of electrons in magnetic fields, which is equal to m^*v/qB. w_{2DEG} was calculated to be 48

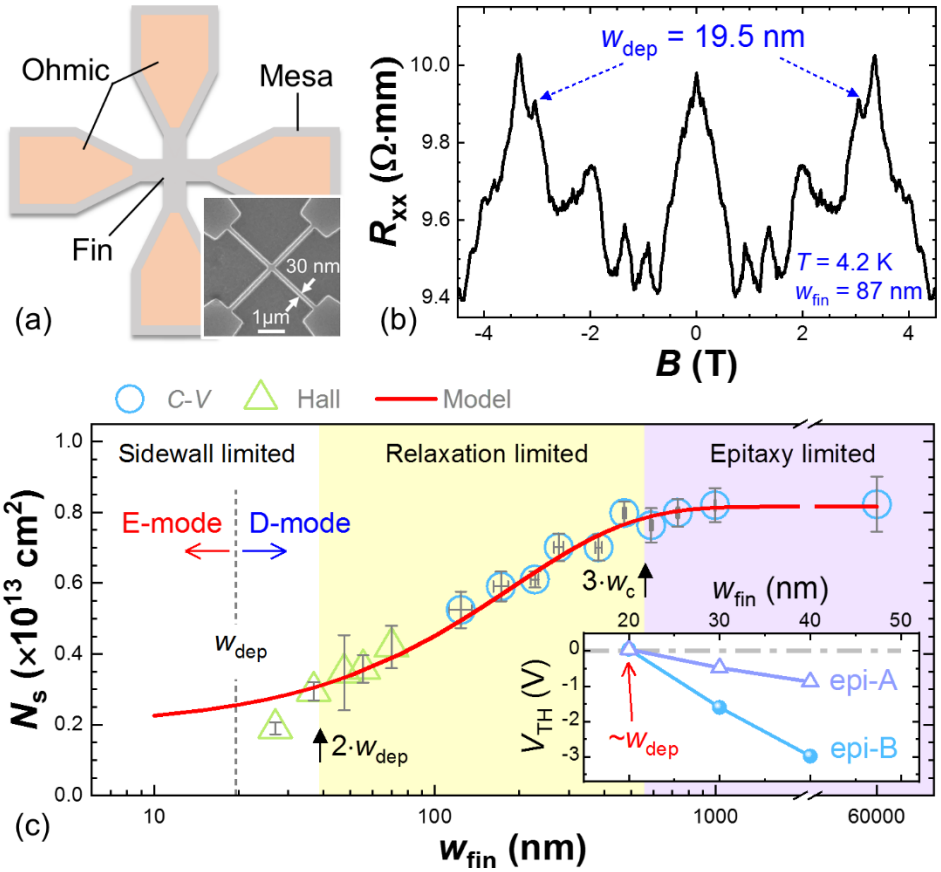

Figure 2.7: (a) Schematic and SEM image of the fabricated hall crosses. (b) R_{xx} versus magnetic field measured at 4.2 K. (c) N_s versus w_{fin}, extracted from both MOS capacitors as well as Hall crosses, in which the N_s from C-V measurements was normalized by $w_{2DEG} \times l_{MOS} \times N_{fin}$, in which the w_{2DEG} was equal to (w_{fin} - 2·w_{dep}). The inset shows the V_{TH} at 1 μA/mm in tri-gate GaN MOSHEMTs with wfin from 20 nm to 40 nm using different epi structures, in which epi-A and epi-B had N_s of 1 × 10^{13} cm^{-2} and 1.5 × 10^{13} cm^{-2}, respectively. Published in Ref. [30].

nm using $w_{2DEG} = \hbar k_F/qB$, and w_{dep} was found to be 19.5 nm using $w_{dep} = (w_{fin} - w_{2DEG})/2$.

After knowing w_{2DEG}, we integrated the *C-V* results from the capacitors, normalized the number of carriers by $w_{2DEG} \times l_{MOS} \times N_{fin}$, and extracted the N_s as a function of w_{fin}, as shown in Fig. 2.7(c). The N_s extracted from the measured Hall crosses were also included in the same plot for comparison, showing consistency with the *C-V* results, which supports the determined w_{dep}.

The reduction in N_s from planar to narrow tri-gates can be analytically modeled as:

$$N_{s,fin} = (1 - \beta) \cdot N_{s,p},$$

in which $N_{s,fin}$ and $N_{s,p}$ are the carrier densities in AlGaN/GaN fin and planar structures, respectively. $\beta(w_{fin})$ describes the strain relaxation with reducing w_{fin}, and can be written as:

$$\beta = \alpha \cdot e^{-w_{fin}/w_c},$$

which resulted in α = 0.623 and w_c = 187 nm from fitting this model with the experimental data in Fig. 2.7(c).

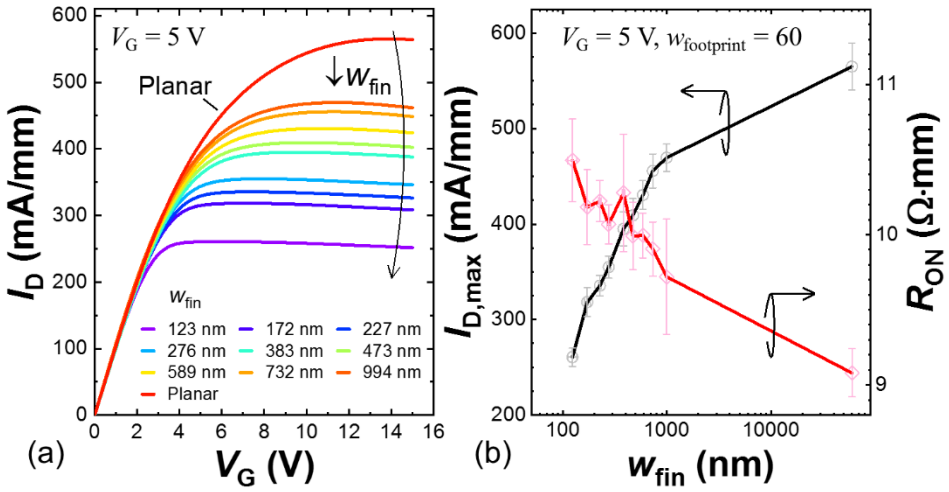

Figure 2.8: (a) Average output characteristics of tri-gate and planar MOSHEMTs, measured at V_G = 5 V and normalized by $w_{footprint}$. (b) Summarized dependences of $I_{D,max}$ and R_{ON} on w_{fin}. Published in Ref. [30].

The quantity w_c represents a characteristic width for relaxation, such that the N_s-w_{fin} dependence is relaxation-limited when w_{fin} is below $3 \cdot w_c$ (Fig. 2.7(c)). When w_{fin} is greater than $3 \cdot w_c$, the effect of relaxation is minor, thus N_s is limited by the design and growth of the AlGaN/GaN heterostructure, varying little with w_{fin}. When w_{fin} is smaller than $2 \cdot w_{dep}$, N_s is limited by the sidewall depletion, and reduces much faster than the model prediction, as the fins get narrow enough so that the sidewall depletion affects the 2DEG even at the center of the fin. This defines three main regions of the N_s-w_{fin} characteristics: sidewall-limited, relaxation-limited and epitaxy-limited regions (Fig. 2.7(c)). The sidewall depletion is a crucial factor to achieve normally-off operation, as it can even remove most of the 2DEG in the fins when w_{fin} is sufficiently small ($\leq w_{dep}$). As shown in the inset in Fig. 2.7(c), normally-off operation could be achieved for w_{fin} = 20 nm ($\approx w_{dep}$) with V_{TH} of 0.04 V at 1 μA/mm, regardless of different epi structures with different N_s, indicating the effective depletion of the 2DEG by the sidewalls. This value of w_{fin} agrees well with previous reports showing that the effective non-conductive width in GaN fins was between 19 nm and 26 nm [92].

2.4 Eliminating degradation in on-resistance and output current

As introduced in Section 2.1, the tri-gate can increase the R_{ON} and reduce the $I_{D,max}$ in GaN electronic devices due to the fin etching, which is an important issue that must be resolved. In this section, we address this issue by optimizing the width (w_{fin}), length (l_{fin}) and filling factors (FF) of the fins in the tri-gate region and present tri-gate GaN MOSHEMTs with about zero degradation in R_{ON} and $I_{D,max}$.

2.4.1 Effect of the fin width

The on-state performance of the device is greatly impacted by w_{fin}, as narrowing the fins degrades the $I_{D,max}$ and R_{ON} (Figs. 2.8(a) and (b)). $I_{D,max}$ reduced from 565 ± 25 mA/mm in the planar device to 261

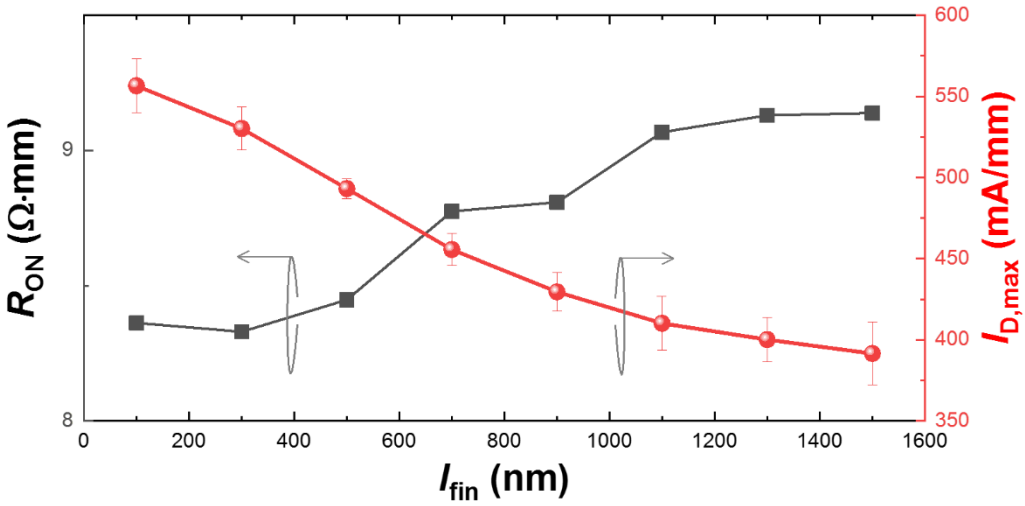

Figure 2.9: Average R_{ON} and $I_{D,max}$ of tri-gate GaN MOSHEMTs versus the length of the fins (l_{fin}), with a fixed w_{fin}, measured at V_G = 5 V and normalized by the width of the device footprint.

± 10 mA/mm in tri-gate devices with w_{fin} of 123 nm, corresponding to a significant reduction of 53.9 %. This is due to the narrower effective channel width ($w_{channel} = w_{fin} \times N_{fin}$) in tri-gate devices and also the increased sidewall scattering in narrow fins, which diminishes the velocity of electrons in the tri-gate region and results in smaller $I_{D,max}$. From planar to w_{fin} = 123 nm, the R_{ON} increased by 15.5%, which is likely due to the degraded electron mobility and larger spreading resistance in narrower fins [43], [93]. The degradation in R_{ON} was much less pronounced than in $I_{D,max}$, as the length of the etched region (the trenches) was small with respect to the length of the entire active region of the device, but I_D was greatly affected by the bottleneck on the current path from the narrow fins which were more impacted by sidewall scattering. The different V_{TH} in the devices was not considered here, since the devices were all normally-on and V_G = 5 V was sufficiently large to nearly saturate their R_{ON}. To reduce the R_{ON} and increase the $I_{D,max}$, a larger w_{fin} is desirable.

2.4.2 Effect of the fin length

The l_{fin} also has great impact on R_{ON} and $I_{D,max}$ in tri-gate MOSHEMTs (Fig. 2.9). As l_{fin} was increased, the R_{ON} increased and the $I_{D,max}$ reduced accordingly. This phenomenon is caused by the lower conductance in the tri-gate region as compared with the planar region in the devices, because of the fin etching which reduces the effective channel width and creates defective sidewalls that degrades the electron velocity in the tri-gate region. Consequently, a small l_{fin} is favored to reduce the R_{ON} and increase the $I_{D,max}$ in tri-gate GaN devices.

2.4.3 Effect of the filling factor

The *FF* is crucial to achieve tri-gate GaN devices with small R_{ON} and high $I_{D,max}$, since it determines the effect channel width ($w_{channel} = w_{fin} \times N_{fin}$), the effective source width, as well as the trench conduction. To illustrate the effect of effective source injection and trench conduction, we compared four

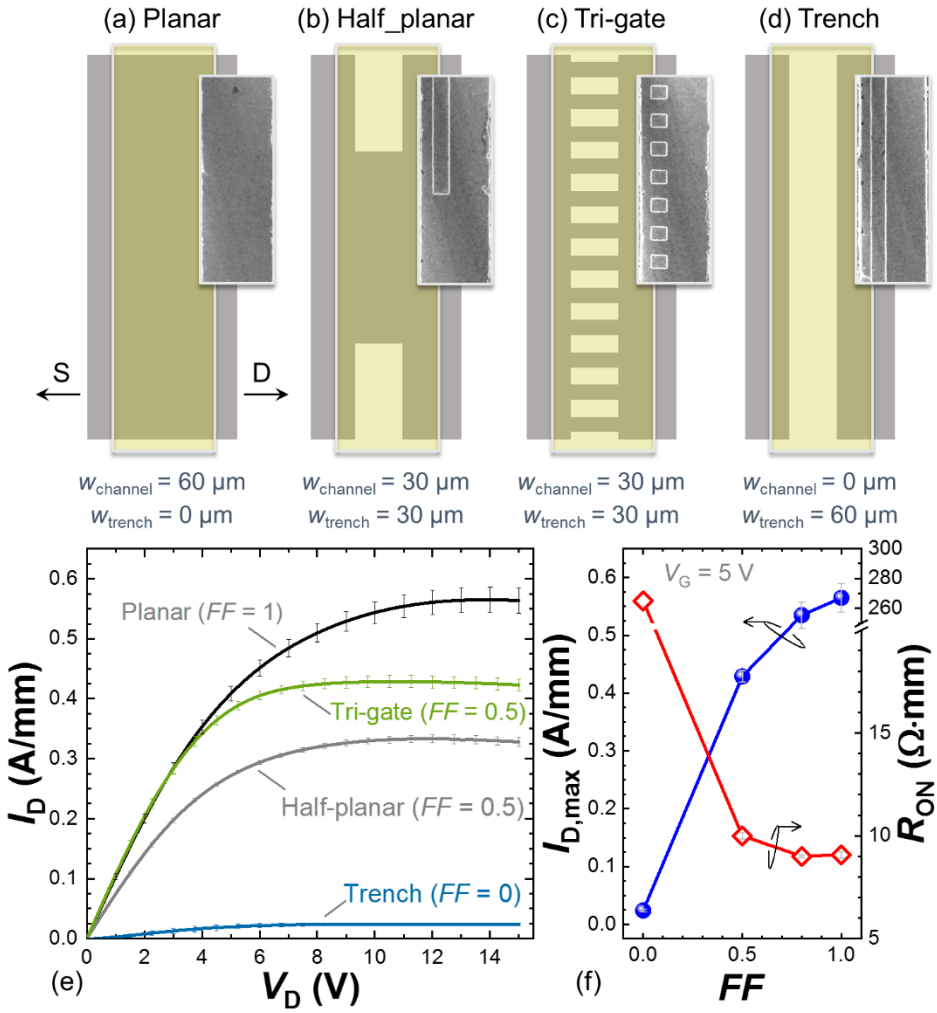

Figure 2.10: (a)-(d) Top-view schematcs of the four types of transistors with similar dimensions but different gate regions. (e) Output characteristics at V_G = 5 V. (f) Dependences of $I_{D,max}$ and R_{ON} on *FF* at V_G = 5 V with w_{fin} = 600 nm and l_{fin} = 700 nm. All current values are normalized by the width of device footprint ($w_{footprint}$ = 60 µm). Published in Ref. [30].

types of transistors with similar dimensions but different gate regions.

1) The Planar (Fig. 2.10(a)) was a planar-gate MOSHEMT with $w_{channel}$ = $w_{footprint}$ of 60 µm.
2) The Half-planar (Fig. 2.10(b)) had one 30 µm-wide "fin" ($w_{channel}$) and two 15 µm-wide trenches (w_{trench} = 30 µm) in its gate region, corresponding a *FF* of 0.5.
3) The Tri-gate (Fig. 2.10(c)) was a tri-gate MOSHEMT with *FF* also of 0.5, in which 600 nm-wide fins were evenly distributed in the tri-gate region, resulting in $w_{channel}$ and w_{trench} of both 30 µm, the same as the Half-planar.
4) The Trench (Fig. 2.10(d)) was similar to other devices except for its fully recessed gate region, resulting $w_{channel}$ and w_{trench} of 0 µm and 60 µm, respectively, corresponding to a *FF* of 0. The recess depth was the same as the fin height in the Tri-gate.

The output characteristics of these devices at V_G = 5 V were measured and compared in Fig. 2.10(e), all normalized by $w_{footprint}$ of 60 µm. While the Half-planar had a $w_{channel}$ of 30 µm (e.g. half of the

channel width of the Planar), it exhibited $I_{D,max}$ of 333 ± 6 mA/mm, which is larger than half of the $I_{D,max}$ in Planar (565 ± 21 mA/mm). This is because the width of effective source injection (w_{source}) in the Half-planar was greater than its $w_{channel}$. Assuming a uniform injection from the source and ignoring the crowding effect, w_{source} in Half-planar can be estimated using:

$$w_{source} = \frac{\left(I_{D,max}^{Half-planar} - 0.5 \times I_{D,max}^{Planar}\right) \times w_{footprint}}{I_{D,max}^{Planar}},$$

which is 35.4 μm, indicating that the effective source extended 2.7 μm from each side of the channel towards the mesa edge. This results in a larger $I_{D,max}$ ratio between the Half-planar and Planar (58.9%) than the *FF* of 50% of the Half-planar.

The $I_{D,max}$ can be further enhanced by increasing the w_{source} for a fixed *FF*, by dividing the 30 μm-wide "fin" (Half-planar) into many narrower fins and distributing them evenly in the device (Tri-gate). As shown in Fig. 2.10(e), the Tri-gate presented much larger $I_{D,max}$ (429 ± 10 mA/mm) than the Half-planar, although they had the same $w_{channel}$ and *FF*. This is thanks to the much larger w_{source} in the Tri-gate, which can be comparable to that in the Planar as the spacing between the fins was 0.6 μm, which is much smaller than the extension length (2.7 μm) of the effect source injection (here we assumed that w_{fin} did not significantly change the extension length of the effective source).

Considering that each trench is shared by two fins, the width of a single trench should be smaller than 1.35 μm in a tri-gate device to assure the full use of the source injection in a given $w_{footprint}$ (1.35 μm = 0.5 × 2.7 μm,). Then the degradation in R_{ON} and $I_{D,max}$ can be fully recovered by increasing the *FF* to achieve channels, which is based on a large w_{fin} of 600 nm and a small l_{fin} of 700 nm as discussed in sections 2.4.1 and 2.4.2. From the *FF* = 0 in the Trench to a large *FF* of 0.8 (Fig. 2.10(f)), the difference in $I_{D,max}$ and R_{ON} between the planar and tri-gate devices became very small, within the error bars, revealing that the degradation caused by the etching of the 2DEG in tri-gate devices was completely eliminated. Meanwhile, it is noteworthy that the trenches also contributed to the on-state conduction of the transistors, as they function as trench MOSFETs in parallel with the fin-MOSHEMTs, which can be seen form the I_D-V_D characteristics of Trench in Fig. 2.10(e) and will be discussed in the following section.

2.5 Additional trench-conduction channels

Trench conduction is another important feature of tri-gate GaN devices, which refers to the additional conductive channels formed at the sidewall and bottom oxide/GaN interface in the trench region, functioning as MOSHEMTs in parallel with the Fin-MOSHEMTs and reducing the resistance of the tri-gate region. The sidewall conduction was also suggested by previous studies [57], [70], [70], [75],

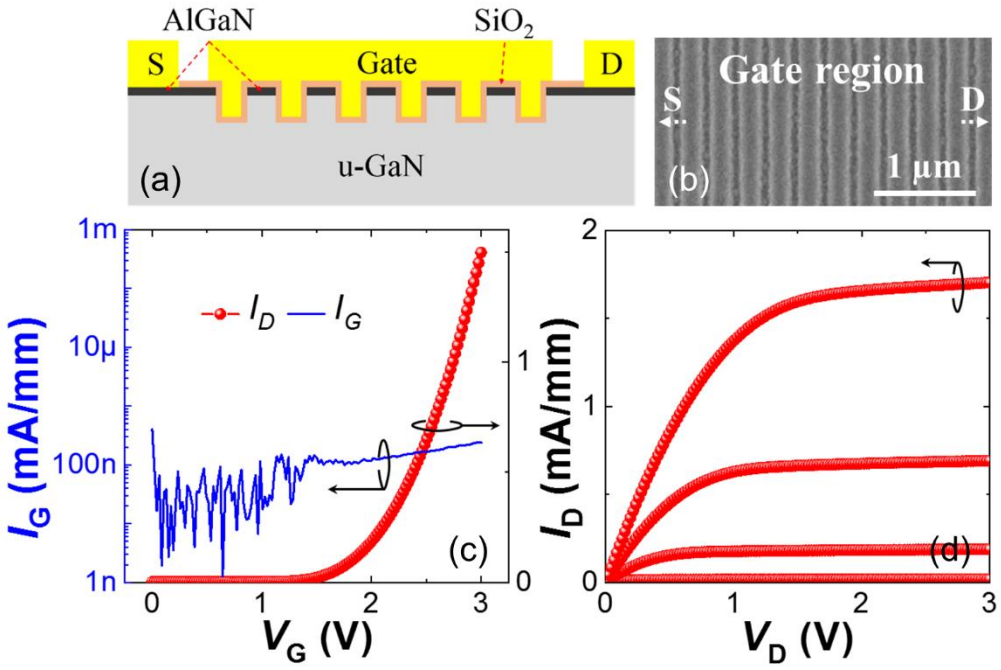

Figure 2.11: (a) Cross-sectional schematic and (b) top-view SEM observations in gate region of the periodically gate-recessed transistors; (c) transfer and (d) output characteristics of the transistors. Published in Ref. [28].

[81], [83] but has not been investigated, in addition carrier accumulation at the oxide/GaN interface at trench bottom of the fins was neglected. To investigate this effect, periodically gate-recessed MOS transistors were fabricated (Figs. 2.11(a) and (b)) using 18 nm of SiO_2 as the gate dielectric. Gate length of these transistors was 132 μm and the gate-to-source/gate-to-drain distance was 4 μm. The gate region of the transistors was periodically recessed with a depth of 114 nm and a length of 165 nm (period was 300 nm). Transfer characteristics of the transistor (Fig. 2.11(c)) reveal current flows perpendicularly to the fins with normally-off behavior, indicating that carriers accumulated at the sidewalls as well as the bottom of each trench, and the two accumulation regions overlapped with each other with a threshold voltage of ~2 V. I_D-V_D plots of the transistors are presented in Fig. 2.11(d), showing that accumulation-induced channels were well modulated by the gate. These results clearly show that carrier accumulation at oxide/GaN interface forms additional conduction channels in the trenches, which contributes to the output current of tri-gate GaN devices when V_G is greater than its V_{TH}.

2.5.1 Trench conduction in normally-on devices

The trench conduction is typically small in normally-on tri-gate GaN transistors, because of the large difference in V_{TH} of trench MOSFETs and the Fin MOHEMTs and the poor electron mobility in the trench MOSFETs, which is caused by etch damages during the fin etching.

Firstly we illustrate the effect of large difference in V_{TH} by exploring the gate-source capacitance

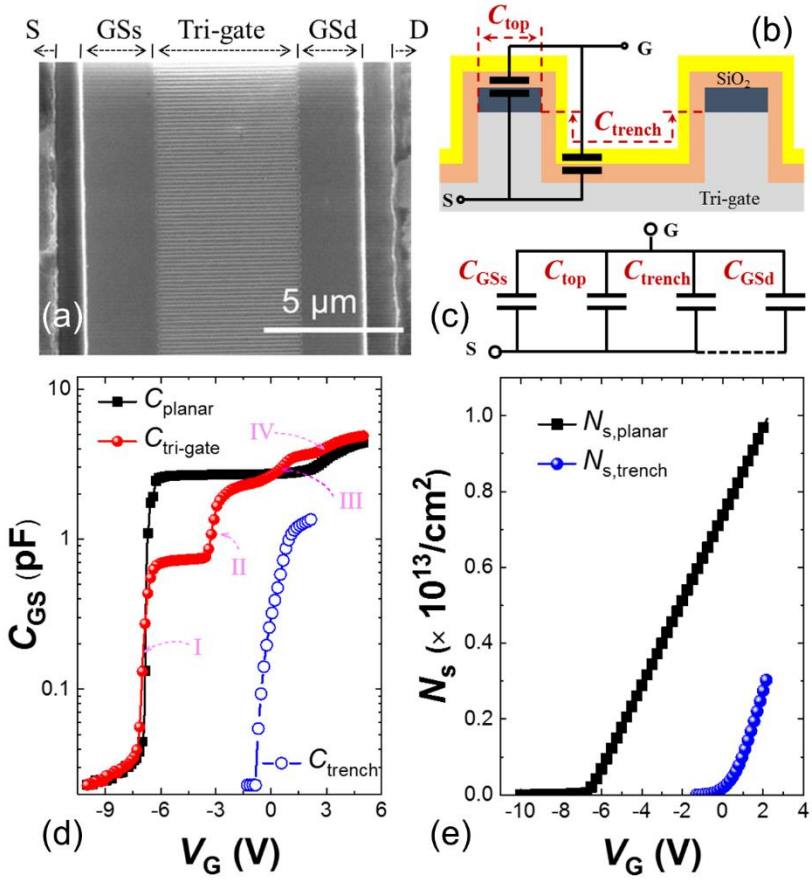

Figure 2.12: (a) Top-view SEM image of the tri-gate MOSHETMs used for *C-V* measurements. (b) Equivalent circuit of C_{GS} for the tri-gate MOSHEMT. (c) Schematic of C_{top} and C_{trench} in the tri-gate region. (d) Measured *C-V* characteristics of the MOSHEMTs and extracted C_{trench}; (e) V_G-dependent sheet carrier density (N_s) of the planar MOSHEMT and the trench MOSFET. Published in Ref. [28].

(C_{GS}) of the tri-gate and planar MOSHEMTs (Fig. 2.12(a)), which were denoted as $C_{tri\text{-}gate}$ and C_{planar}, respectively. These MOSHEMT had w_{fin} of 114 nm with a *FF* of ~0.45, in which the direction of the current was parallel to the fins. Gate lengths of the MOSHEMTs were both 10 μm. $C_{tri\text{-}gate}$ is composed of four capacitors in parallel as shown in Fig. 2.12(b). The first capacitor is the SiO_2/AlGaN/GaN top gates in the fin region (C_{top}), and the second is the SiO_2/GaN in the trenches (C_{trench}), which acted similarly to MOSFETs, as shown in Fig. 2.12(c). The other two capacitors are the planar SiO_2/AlGaN/GaN potions of the gate, one close to the source (C_{GSs}) and the other close to the drain (C_{GSd}), corresponding to the GSs and GSd regions in Fig. 2.12(a). Figure. 2.12(d) shows the *C-V* characteristics of the tri-gate and planar HEMTs. The steps I-IV observed for the *C-V* characteristics of the tri-gate MOSHEMT corresponded to carrier accumulation in C_{GSs}, C_{top} + C_{GSd}, C_{trench} and at the SiO_2/AlGaN interface, respectively. C_{top} showed a less negative V_{TH} with respect to C_{GSs} due to sidewall gate depletion and partial relaxation of AlGaN/GaN fins [43]. Before step IV, $C_{tri\text{-}gate}$ is simply the sum of C_{GSs}, $C_{top+GSd}$ and C_{trench}. Assuming that these capacitors shared similar values of capacitance in depletion, C_{trench} was extracted using $C_{trench} = C_{tri\text{-}gate} - [C_{GSs} + (C_{top} + C_{GSd})]$ when V_G was below 2 V since i. there was no spillover; ii. these capacitors were in parallel; iii C_{GSs} + (C_{top} +

C_{GSd}) was saturated and its value was close to the value of $C_{tri\text{-}gate}$ before the V_{TH} of C_{trench}, as shown in Fig. 2.12(c). Figure 2.12(e) presents the comparison between the sheet carrier density of the planar MOSHEMT ($N_{s,planar}$) and the trench ($N_{s,trench}$), extracted from the *C-V* measurements. $N_{s,trench}$ is the equivalent carrier density obtained by normalizing the number of carriers with the product of trench length and width (not considering the four sidewalls of the trench) for a fair comparison with the planar MOSHEMT. At a V_G of 2 V, the $N_{s,trench}$ was only about 28.4% of the $N_{s,planar}$, which is not an significant portion.

The other reason for the negligible trench conduction in normally-on tri-gate GaN transistors is the poor mobility in the trench region. According to Refs. [94], [95], the voltage-dependent effective mobility (μ_{eff}) of SiO_2/etched GaN channel is only about 16 $cm^2/V{\cdot}s$. This value is much lower than the low-field electron mobility (μ_0) and μ_{eff} of the planar MOSHEMT equal to 1560 and 700 $cm^2/V{\cdot}s$ at V_G = 2 V, respectively, extracted using a mobility-degradation model [96], [97]. The μ_0 was close to the Hall mobility, which was about 1660 $cm^2/V{\cdot}s$. Since I_D of a transistor is proportional to the product of N_s and μ, the I_D of the MOSFET was only about 6.5 % of the counterpart planar MOSHEMT at V_G = 2 V. As typical normally-on devices do not operate at very high V_G, the contribution of trench conduction to the total conductance of these devices can be estimated to be small.

2.5.2 Trench conduction in normally-off devices

While the trench conduction is insignificant in normally-on devices, it is very important for tri-gate GaN normally-off devices. In a normally-off device, the V_{TH} of the Fin MOSHEMTs and trench MOSFETs become very close to each other, thus the MOSFETs may contribute a significant portion to the total carriers and hence the conductance of the device.

To illustrate such effect, we investigated normally-off tri-gate GaN MOSHEMTs, as shown in Figs. 13(a)-(c). The AlGaN/GaN epitaxial structure here consisted of, from bottom to up, 3.3-μm buffer, 1.2-μm un-doped GaN (u-GaN), 18-nm $Al_{0.26}Ga_{0.74}N$ barrier and 2-nm u-GaN cap layers. The device fabrication started with Cl_2-based inductively coupled plasma (ICP) etching for device isolation, followed by ohmic metal deposition of Tip/Al/Ni/Au and rapid thermal annealing in N_2 atmosphere at 870 ºC to form ohmic contacts. The 114 nm-high AlGaN/GaN fins were fabricated by combining interference lithography, photolithography and ICP etching. The w_{fin} was about 300 nm and the *FF* was ~0.5. Then gate recess region was defined by e-beam lithography with a length of about 340 nm and recessed using ICP etching with a depth of about 15 nm (the AlGaN barrier layer was not complete recessed). Then 18 nm SiO_2 was deposited by atomic layer deposition (ALD) as the gate dielectric and selectively removed in ohmic contact regions. Finally the gate was formed by deposition

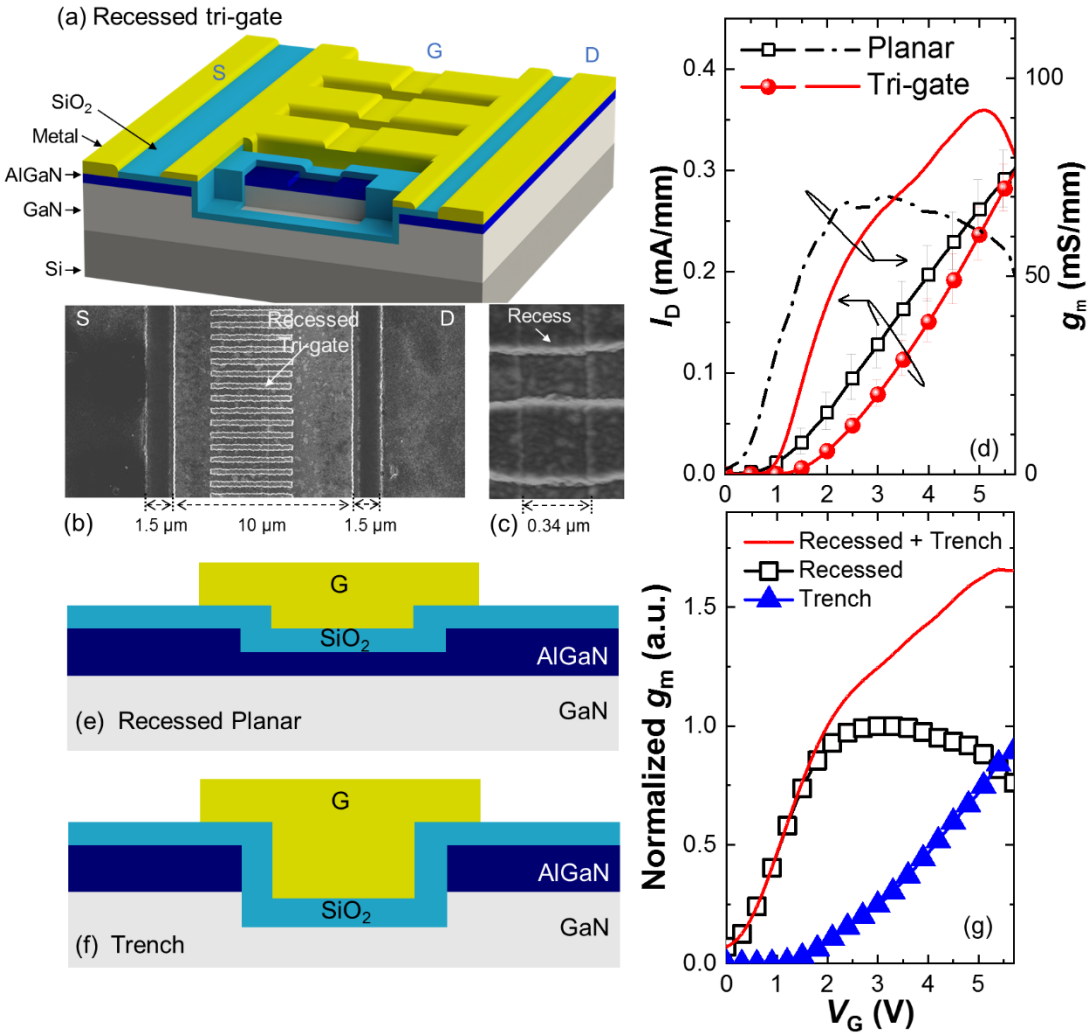

Figure 2.13: (a) Schematics of the recessed tri-gate MOSHEMT. (b) and (c) Top-view SEM observation of (b) the entire MOSHEMTs and (c) the recessed tri-gate. (d) Transfer characteristics of the recessed planar and tri-gate MOSHEMTs, measured at V_D = 5 V and normalized by the width of the device footprint. Cross-sectional schematics of planar-MOSHEMTs with (e) recessed and (f) trenches in the gate region and (g) the comparison of their normalized g_m versus V_G.

and lift-off of Ni/Au. Figure 2.14(c) presents a zoomed-in SEM observation of the recessed tri-gate in which good step coverage of the gate metal can be observed. Planar gate-recessed AlGaN/GaN HEMTs with similar dimensions were taken as reference. All device characteristics such as I_D and g_m were normalized by the width of the device footprint (150 μm).

Figure 2.13(d) shows the transfer characteristics of the recessed planar and tri-gate MOSHEMTs, revealing normally-off operation for both devices. The V_{TH} in recessed planar and tri-gate devices was about 1 V and 2 V, respectively, extracted by extrapolation of the I_D-V_G curve in linear scale. Compared with the recessed planar device, the recessed tri-gate devices exhibited a higher g_m 87 mS/mm. Such enhancement in g_m is due to the trench conduction rather than a better tri-gate control as usually expected, since the increase in the gate control at w_{fin} = 300 nm is insufficient to overcome

the loss in device conductance at FF = 0.5 to enhance the g_m, as shown in Fig. 2.4(b). When V_G was beyond 2 V, the trench MOSFETs e turned on and offered additional conduction channels, resulting in the g_m. To further support this explanation, we further fabricated MOSHEMTs with trenches (Fig. 2.13(e)) in the gate region and then compared them with the recessed planar MOSHEMTs (Fig. 2.13(f)). The g_m-V_G curves of both structures were normalized and summed together (Fig. 2.13(g)), which agreed very well with the double-peak g_m-V_G behavior of the recessed tri-gate MOSHEMTs presented in Fig. 2.13(d). This indicates that the trench conduction contributed a significant portion to the total conductance of the device at high V_G, thus it needs to be carefully optimized for tri-gate normally-off GaN devices.

2.6 Improving thermal performance

In addition to offering the additional trench conduction channels, the 3D nature of the tri-gate also reduces the thermal resistance (R_{TH}) of tri-gate GaN devices (Fig. 2.14), which is a very important advantage for power and RF devices since they usually operate at a high channel temperature and require effective cooling. To explore this advantage, AlGaN/GaN tri-gate MOSHEMTs with a w_{fin} of 300 nm and a FF of ~0.5 were investigated in comparison with counterpart planar MOSHEMTs. The drain current-voltage (I_D - V_D) characteristics of the two devices are shown in Fig. 2.14(a), both normalized by the width of the device footprint. Using the thermoelectric technique proposed in Ref. [98], we measured the temperature dependence of the extrapolated drain saturation current ($I_{DS,0}$) of the two devices and estimated the average temperature over the entire device active area (T_{avg}) as shown in Fig. 2.14(b) (as justified in Ref. [99], the T_{avg} obtained by this method is close to the T_{avg} measured by micro-Raman thermography at low power levels although it may neglect the effect of traps). With the same applied power (P_a), the tri-gate MOSHEMT exhibited a much reduced T_{avg} compared to the planar, which is comparable or greater than other technologies proposed for thermal management of GaN electronics such as graphene-graphite quilts [100], Cu-filled backside via [101], substrate transfer using h-BN [102] and nanocrystalline diamond thin film [103]. Figure 2.14(b) also suggests a smaller R_{TH} for the tri-gate MOSHEMT, which is consistent with a recent report in the literature [78]. From the slope of the linear region of the T_{avg} versus P_a curves, R_{TH} of the planar and tri-gate MOSHEMTs were estimated to be about 34.2 and 17.0 K·mm/W, respectively, normalized by device width. The reduction in R_{TH} of about 50% in the tri-gate MOSHEMT is very close to the reduction (55%) by replacing the Si substrate with SiC [104], indicating the great potential of the tri-gate technology in thermal engineering of GaN transistors. The reduced R_{TH} in the tri-gate MOSHEMT can be attributed to mainly two reasons: i. the increased surface area with nanowire architecture and ii. the absence of the AlGaN barrier at the sidewalls, since AlGaN has much lower

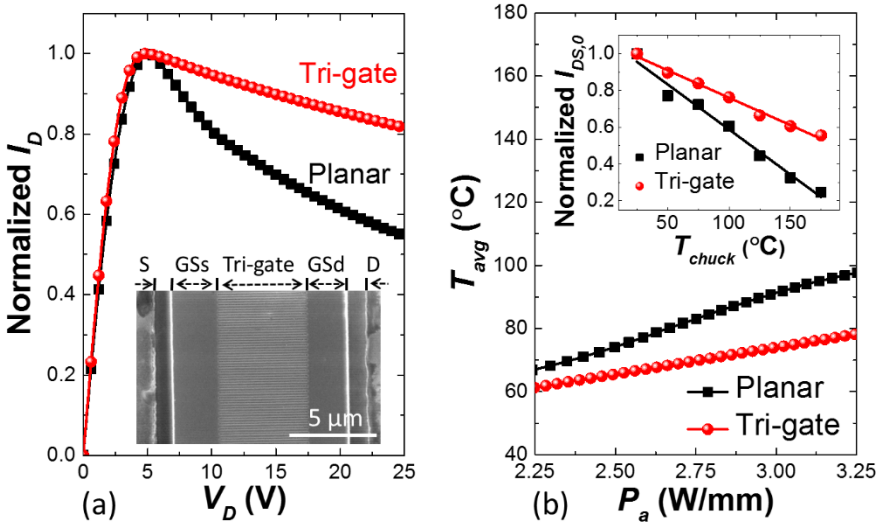

Figure 2.14: (a) Normalized I_D-V_D characteristics of planar and tri-gate AlGaN/GaN MOSHEMT measured with similar V_G - V_{TH} (~5 V) and (b) extracted average temperature of the 150-µm-wide transistors versus applied power normalized by device width; the insets of (a) and (b) show the SEM observation of the tri-gate transistor and the linear dependences of the extrapolated saturation drain current on the chuck temperature, respectively. Published in Ref. [28].

thermal conductivity with respect to GaN [105], which improves heat dissipation through the surface when the device features a large surface area, high surface temperature, or a suface heat sink.

2.7 Reducing gate charge

The tri-gate architecture can be an effective way to reduce C_G and Q_G in normally-on GaN (MOS)HEMTs, depending on its design and V_G (Fig. 2.15). It is often considered that the tri-gate geometry increases the C_G due to its 3D nature, as it is the case in FinFETs. This is true when C_G is evaluated for a single fin with small w_{fin}, since in this case the gate capacitance per area of 2DEG is indeed increased, as discussed in Fig. 7(d). However, it is usually more important to understand how the tri-gate impacts C_G and Q_G in entire device footprint consisting of multiple parallel fins, especially for device designers on power and RF electronics. In this scenario, C_G and Q_G can be both greatly diminished in tri-gate compared to planar transistors, because a portion of the 2DEG carriers is removed during the fin etching, which is determined by *FF*, and only the carriers present at the 2D channels in the fins contribute to C_G and Q_G (before the sidewall channels turn on). This is very different to FinFETs, in which the entire 3D periphery of the fins contributes to C_G and Q_G.

As shown in Fig. 2.15(a), the C_G of the tri-gate devices varied from 0.79 to 0.91 pC/mm, depending on w_{fin}, which were between 58.6% and 68.4% of the planar device (at *FF* = 0.5 and V_G = 0 V). The Q_G was also reduced by over 50%, resulting in a decreasing R_{ON}·Q_G product (Fig. 2.15(b)) and hence a higher figure-of-merit for high-frequency switching. These results indicate that, depending on its

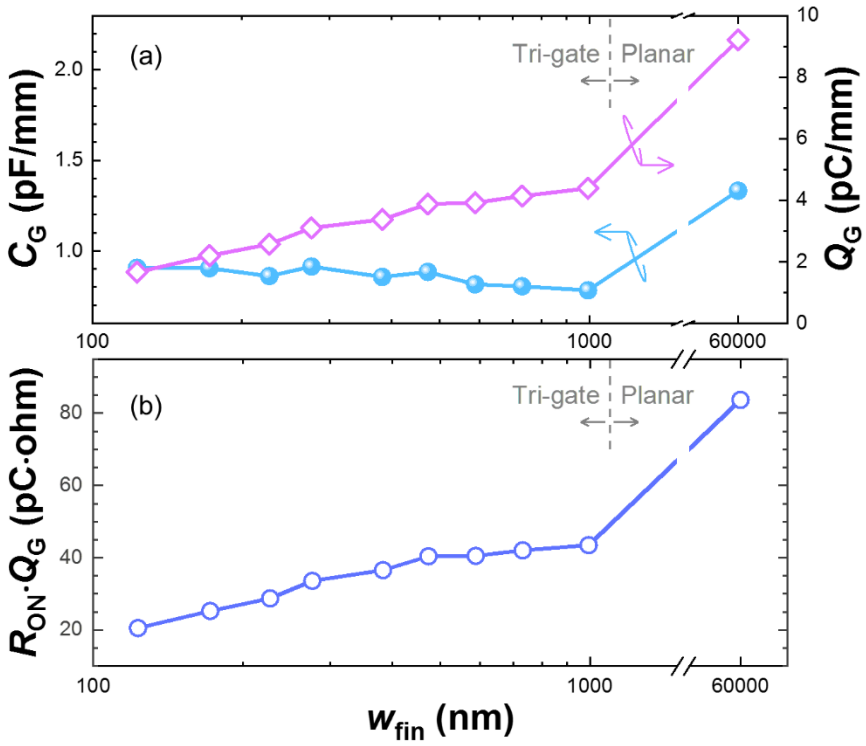

Figure 2.15: (a) Dependence of C_G and Q_G on w_{fin} normalized by $w_{footprint}$, extracted at V_G = 0 V. (b) The dependence of R_{ON}·Q_G on w_{fin}. All results were extract at V_G = 0 V and FF = 0.5. Published in Ref. [30].

geometry and V_G, the tri-gate can reduce C_G, Q_G, and R_{ON}·Q_G in GaN (MOS)HEMTs, which can be highly valuable for many applications.

2.8 Conclusion

In this chapter we presented a detailed investigation of the impact of the tri-gate structure on GaN metal- MOSHEMTs. The transfer characteristics of the devices are greatly influenced by w_{fin}, as small w_{fin} enhances the g_m, at the expense of degraded linearity. The V_{TH} can also be increased as w_{fin} is reduced, due to enhanced tri-gate control and reduced N_s. The smaller N_s in narrower fins is caused by more pronounced strain relaxation as well as sidewall depletion, which was quantified using both Hall and *C-V* measurements. Normally-off operation was achieved for w_{fin} close to the w_{dep} of 19.5 nm, since the fin is depleted from its two sidewalls. The impact of w_{fin} on R_{ON} and current capability on w_{fin} were also investigated, along with the influence of the effective source injection, the trench conduction and the *FFs* on these key characteristics. The degradation caused by the tri-gate fin etching could be fully recovered by increasing the *FF*. Finally, we show that the tri-gate can reduce the thermal resistance in the devices as well as and diminish Q_G in tri-gate normally-on MOSHEMTs, depending on design of the tri-gate and the V_G, leading to a smaller R_{ON}·Q_G product that is beneficial for high-frequency switching applications.

Chapter 3 Novel tri-gate field plates for high-voltage applications

3.1 Introduction

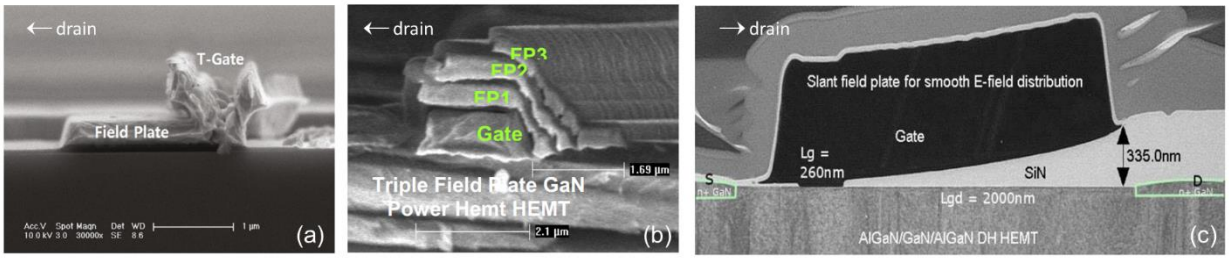

Figure 3.1: Cross-sectional SEM images of (a) a single FP [73], (b) multiple FPs [74] and (c) a slant FP [75] in GaN HEMTs.

GaN power devices are usually based on a lateral AlGaN/GaN-on-Si heterostructure. Such lateral scheme enables monolithic power integrated circuits (Power ICs) composed of various GaN devices and even Si devices, and can innovate current power conversion systems with much smaller module size and higher efficiency. However, a current major challenge is the limited voltage-blocking performance in these lateral devices, which is still far from the GaN materials capabilities. An important reason for such early breakdown is the inhomogeneous distribution of the electric field. When a high voltage is blocked in OFF state, the electric field concentrates at the edge of the gate electrode, leading to the early breakdown of the device [23]–[25], [106], [107]. To spread more homogeneously the electric field, various designs of field plates (FPs) have been developed [106]–[108], including the single FP (Fig. 3.1(a)) [109], multiple FPs (Fig. 3.1(b)) [26], and the slant field plate (Fig. 3.1(c))[110], among which the slant FP has been proven more effective [110]–[117]. These conventional FPs are achieved based on a vertical scheme, through a precise control over the thickness (as in single and multiple FPs) and angle of the sloped oxide (as in slant FPs) in the vertical direction, which is however extremely challenging and difficult to fabricate and control, and limits the design flexibility of the FPs. More importantly, a large gate-to-drain separation (L_{GD}) is still needed for high-voltage blocking, which degrades significantly the on-resistance (R_{ON}) and the efficiency of the device [118].

In this chapter, we present a novel lateral scheme based on the tri-gate technology to enhance these FPs. We firstly demonstrate the high-voltage capabilities of tri-gate GaN devices by presenting high-

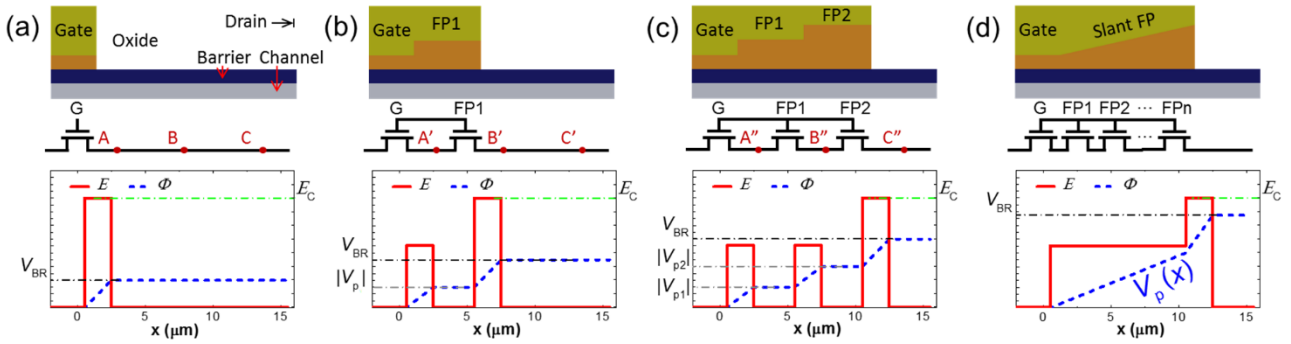

Figure 3.2: Schematics, equivalent circuits and distributions of potential (Φ) and electric field (E) in lateral GaN transistors in OFF state with (a) no FPs, (b) a single FP, (c) two FPs and (d) a slant FP. Published in Ref. [31].

performance tri-gate GaN MOSHEMTs with greatly enhanced breakdown voltage (V_{BR}) and improved high-power figure-of-merit (FOM), as compared to conventional planar-gate MOSHEMTs, by converting a portion of the planar gate into a FP without additional fabrication processes using the tri-gate technology. In addition, we demonstrate a novel slanted tri-gate architecture which, similarly to vertical slant FPs, spreads more effectively the electric field and further improves the V_{BR}. Different from vertical slant FPs, slanted tri-gate can be easily and accurately engineered with a lateral approach, by varying lithographically the width of the tri-gate nanowires, which resulted in a significant enhancement in V_{BR} (~500 V) and a state-of-the-art FOM up to 1.2 GW/cm^2.

3.2 Principle and Concept

To explain our concept, let us first present the general working principle of FPs. The most important design variable for FPs is their pinch-off voltage (V_p), which effectively controls the distribution of the potential (Φ) and the electric field (E) in a lateral device. Figure 3.1 shows a simplified model on the effect of the V_p in spreading the electric field within different FP designs [23]–[25]. For devices without the FP (Fig. 3.1(a)), Φ in the channel increases sharply to the drain voltage V_D at the edge of the gate, where the E peaks. There is nearly no voltage drop between the gate and the drain due to the high-conductivity 2DEG channel, thus E ~ 0. When E reaches the critical breakdown field (E_C), the devices breaks and the V_{BR} is determined from the integral of the $E(x)$. A FP operates as a transistor in series with the gate (Fig. 3.2(b)), with a more negative V_p due to the thicker oxide in the FP region. When the FP pinches off the channel underneath, the Φ at A' is fixed at a certain value (about $|V_p|$ in a simplified model according to Refs. [23] and [25]). This creates a two-step distribution of Φ, thus the total E is shared between two peaks at the edges of both the gate and the FP. The device breaks when either of the two peaks reaches E_C, which results in a larger voltage as compared to the device without the FP due to the larger integral of $E(x)$ spread in two peaks. Since a single FP is insufficient to block large voltages, multiple FPs are usually adopted to distribute better the field. As shown in Fig. 3.2(c), multiple FPs introduce more equivalent transistors with different V_p, creating more steps

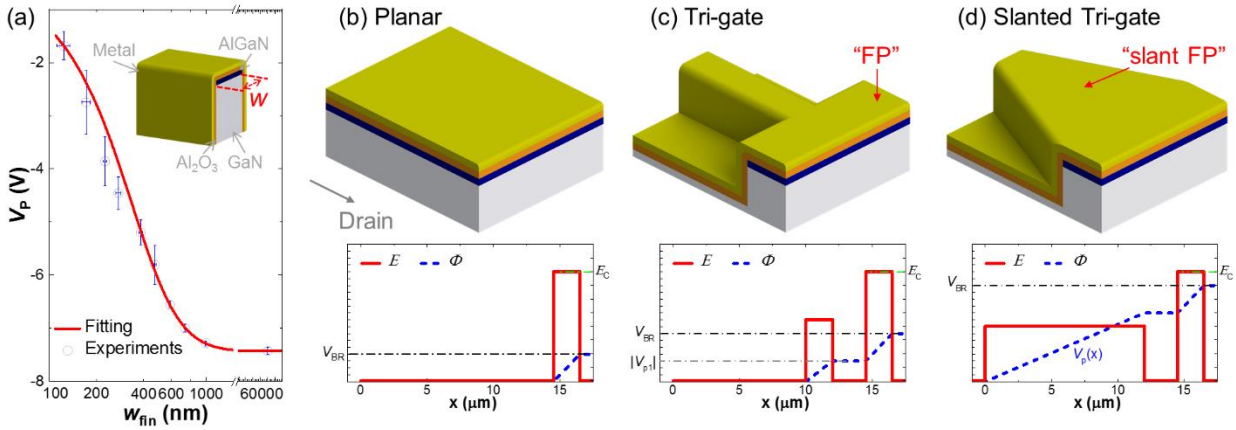

Figure 3.3: (a) Dependence of V_p on w_{fin} in tri-gate AlGaN/GaN MOS structures, in which the error bars were determined from about eight devices of each kind. The inset shows a schematic of the tri-gate structure. Schematics of structures of (b) a planar gate, (c) a single tri-gate, and (d) multiple tri-gates, along with the distribution of channel potential and electric field in them.

in Φ and hence more distributed peaks in E. The ultimate outcome of increasing the number of FPs is a slant FP (Fig. 3.2(d)), which functions as many incrementally-stepped FPs, offering a continuous gradient of V_p towards the drain. This distributes Φ across the FP as a function of x, spreads continuously the E along the entire FP region and thus improves the V_{BR}.

Therefore, V_p is the most important variable to manipulate the electric field and enhance the V_{BR}. In conventional FPs based on the vertical scheme, the V_p is manipulated through either the thickness of the oxide or the AlGaN barrier layer, which is complicated as it requires additional fabrication processes. It is even far more challenging to even fabricate the slant FP due the significant difficulties in a sloped etching of the oxide, restricting the realization of optimized FP designs. In contrast, these FP designs can be easily realized using the tri-gate technology by simply tuning the V_p with the width of the fins (w_{fin}) in a facilitated fabrication process without laborious engineering of the thickness or slope of the oxide. As shown in Fig. 3.3(a), the V_p increases smoothly with narrowing fins as explained in Section 2.3, which offers a highly controllable and very convenient lateral scheme to obtain different V_p profiles to spread the electric field. As shown in Figs. 3.3 (b) and (c), a portion of the planar gate can be easily converted into a FP to enhance the V_{BR}, by simply including a tri-gate region during the mesa etching. In addition, the optimal design of slant FP can be easily achieved by a slanted tri-gate structure (Fig. 3(d)), by simply pattering a slanted fin with increasing w_{fin} towards the drain electrode, which is very convenient and highly promising for high-voltage lateral power devices.

3.3 High-voltage tri-gate GaN-on-Si MOSHEMTs

In this section we present the first high-voltage tri-gate GaN MOSHEMTs using the structure illustrated in Fig. 3.3(c), which resulted in a high hard V_{BR} of 1755 V at I_{OFF} of 45 μA/mm, along with a

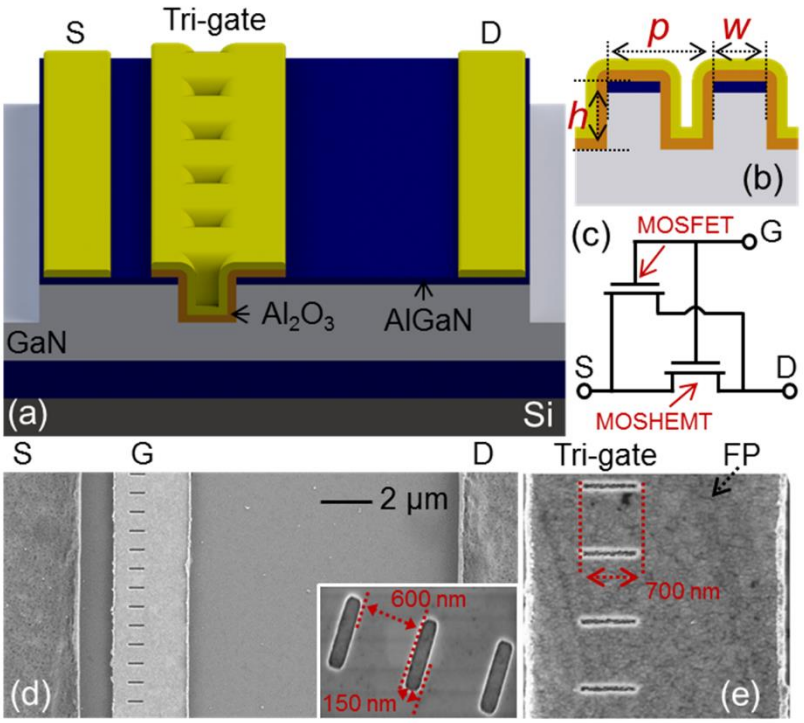

Figure 3.4: (a) Schematic of the tri-gate MOSHEMTs. (b) Cross-sectional schematic of the tri-gate region. (c) Equivalent circuit of the tri-gate MOSHEMTs. (d)-(e) Top-view SEM images of the tri-gate MOSHEMTs. The inset shows a SEM image of the fins without the dielectric and gate metal layers. Published in Ref. [32].

high soft V_{BR} of 1370 V at I_{OFF} = 1 μA/mm for devices with L_{GD} of 15 μm, yielding excellent high-power FOMs up to 1.25 GW/cm^2 and rendering the first tri-gate GaN device for high-voltage applications.

The devices were fabricated on a AlGaN/GaN-on-Si epitaxy grown by MOCVD, which consisted of 3.75 μm of buffer, 0.3 μm of un-doped GaN (u-GaN) channel, 23.5 nm of AlGaN barrier and 2 nm of u-GaN cap layers. The schematics, an equivalent circuit and scanning electron microscopy (SEM) images of the tri-gate MOSHEMTs are shown in Fig. 3.4. The device fabrication started with e-beam lithography to define the mesa and fins, which were then etched by Cl_2-based inductively coupled plasma and followed by ohmic metal deposition and rapid thermal annealing. The height of the fins was about 166 nm. The w_{fin} was 600 nm and the filling factor (FF) as 0.8. Then 20 nm of Al_2O_3 was deposited by atomic layer deposition as the gate dielectric. Finally the gate was formed using Ni/Au, which was later used as the mask for removal of the Al_2O_3 in access/ohmic regions. AlGaN/GaN MOSHEMTs with similar dimensions but planar gates fabricated on the same chip were taken as reference, for which the Al_2O_3 was also removed in their access regions. Device characteristics such as I_D, I_{OFF} and transconductance (g_m) were all normalized by the width of device footprint (60 μm) in both planar and tri-gate devices, and their error bars were determined from measurements on about 10 separate devices of the same kind.

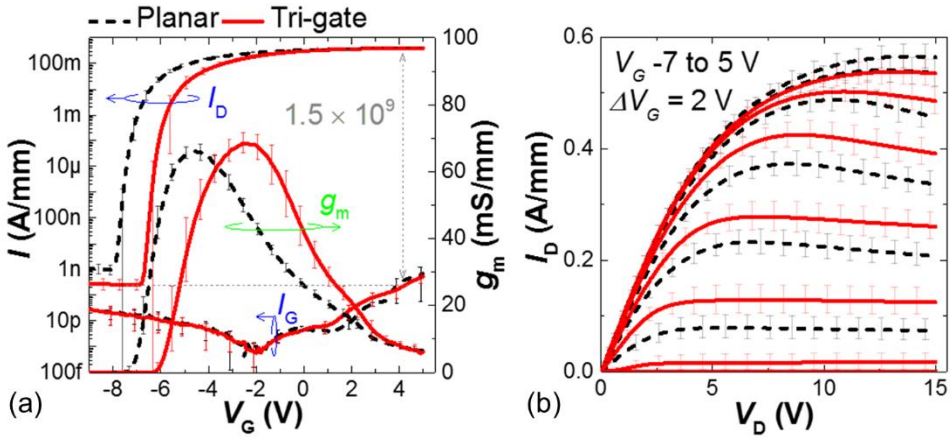

Figure 3.5: (a) Transfer (at V_D = 5 V) and (b) output characteristics of the devices, normalized by the width of device footprint. The $L_{GS}/L_G/L_{GD}$ were 1.5/2.5/10 μm, respectively. Published in Ref. [32].

As shown in Fig. 3.5(a), the planar (Planar) and tri-gate (Tri-gate) MOSHEMTs presented similar g_m of 66.1 ± 2 and 68.5 ± 3 mS/mm, respectively, and similar I_D at V_G = 5 V but different V_{TH}, which has been explained in details in Section 2.3. I_{OFF} was reduced from 1.4 ± 0.7 to 0.28 ± 0.12 nA/mm and *SS* was improved from 98 ± 14 to 93 ± 7 mV/dec due to the better gate control of the tri-gate. The Planar and Tri-gate showed similar maximum I_D of 565 ± 24.5 and 535 ± 23.4 mA/mm at V_G = 5 V (Fig. 3.5(b)), which is a small difference considering the error bars. Furthermore, considering the difference of 1.5 V in V_{TH}, the Tri-gate actually exhibited the same I_D as the Planar at the same gate driving voltage (V_G - V_{TH}). R_{ON} of the Planar and Tri-gate was 9.08 ± 0.16 and 9.01 ± 0.07 Ω·mm, respectively, extracted from I_D-V_D sweeps in linear region. The similar on-state conductance presented by the Tri-gate compared to the Planar suggests that the degradation due to the partial removal of 2DEG by nanowire etching was resolved thanks to the tri-gate geometry optimized in Section 2.4. Another two minor factors that can help compensate the effect of fin etching are the trench conduction (Fig. 3.4(c)) and reduced self-heating, as discussed in Sections 2.5 and 2.6, respectively.

Three-terminal breakdown voltages of the MOSHEMTs were measured with floating substrate (Fig. 3.6), where two types of breakdown are discussed: hard (when device breaks) and soft (when I_{OFF} reaches 1 μA/mm) breakdowns. As shown in Fig. 3.6(a), the hard V_{BR} of the Tri-gate with L_{GD} of 5, 10 and 15 μm were 792, 1100 and 1755 V at I_{OFF} of 0.3, 0.3 and 45 μA/mm, respectively. Compared with the Planar, the tri-gate presented larger V_{BR} when L_{GD} < 10 μm, which is mainly due to the increased effective L_{GD} and the integrated FP in the Tri-gate (Fig. 3.4(e)) as explained in Section 3.2. The effective gate control in the Tri-gate happens mainly within the nanowires, therefore the planar portion of the gate overhang close to the drain side functioned as a gate-connected FP due to its more negative pinch-off voltage as compared to the tri-gate region (Fig. 3.5(a)). With increasing V_D, the heterostructure under the FP is depleted, reducing the electric field in the tri-gate region and leading to the enhanced V_{BR} [25], [116], [119]. Although other factors in the Tri-gate may also improve the

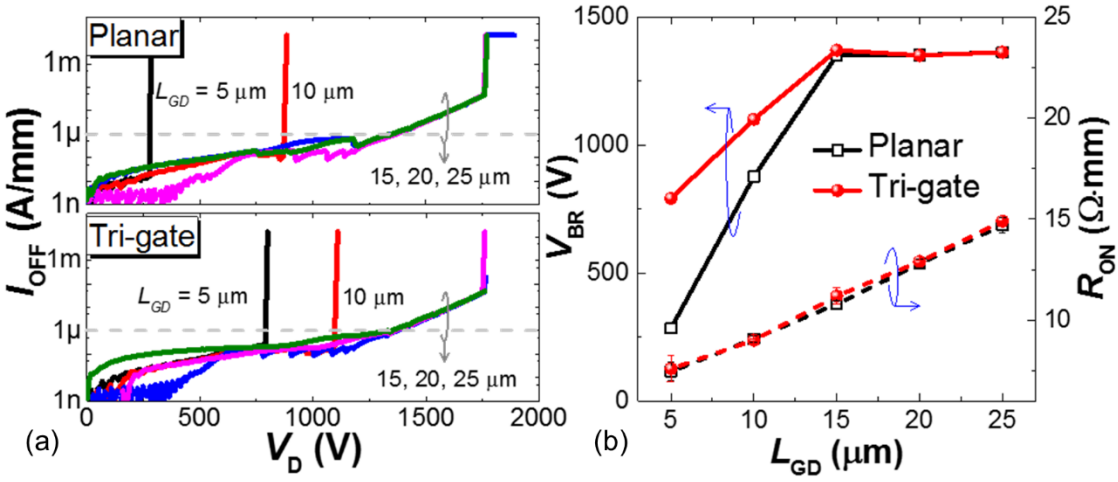

Figure 3.6: (a) OFF-state breakdown characteristics of the planar and tri-gate (*FF* = 0.8) MOSHEMTs with different L_{GD}, measured with floating substrate. (b) Extracted L_{GD}-dependent R_{ON} and V_{BR} of the MOSHEMTs. The breakdown was defined at $I_{OFF} \leq 1$ µA/mm. Published in Ref. [32].

V_{BR} due to 3-D geometry of the tri-gate, we consider these effects to be minor, since tri-gate transistors without the integrated FP in the literature exhibited similar V_{BR} to their counterpart planar transistors [50], [59]. In addition, the effective L_{GD} was increased by 1.3 µm in the Tri-gate, as the gate edge shifted from the drain-side edge of the gate metal (in the Planar) to the drain-side edge for the fins. The critical field strength, extracted from the V_{BR}-L_{GD} curve of the Planar, was about 107 V/µm, thus the increase in effective L_{GD} led to an increase of 140 V in V_{BR}. For $L_{GD} \geq 15$ µm, hard V_{BR} of all devices saturated at ~1760 V, indicating that V_{BR} was limited by the buffer and silicon substrate, in agreement with Refs. [120]–[122]. Figure 3.6(b) shows the R_{ON} and soft V_{BR} of the devices versus L_{GD}. The Planar and Tri-gate exhibited similar R_{ON}, which were linearly dependent on L_{GD}. For $L_{GD} \leq 10$ µm, there was no difference between soft and hard breakdown since I_{OFF} was always below 1 µA/mm. With $L_{GD} \geq 15$ µm, the soft V_{BR} also saturated, which was limited again by the buffer layers.

The Tri-gate was benchmarked against state-of-the-art GaN (MOS)HEMTs on silicon using two commonly-used definitions of V_{BR} ($I_{OFF} \leq 1$ mA/mm and ≤ 1 µA/mm). For calculation of the specific R_{ON} ($R_{ON,SP}$), 1.5 µm of transfer length for each ohmic contact was taken into account. Benchmark for V_{BR} at $I_{OFF} \leq 1$ mA/mm is shown in Fig. 3.7(a). The Tri-gate with L_{GD} of 5, 10 and 15 µm exhibited high power FOM of 688, 791 and 1252 MW/cm^2, respectively, indicating their excellent capabilities as power transistors. However, 1 mA/mm is a large leakage level to determine V_{BR} for power devices, as devices with V_{BR} > 1000 V would present prohibitively large off-state dissipated power over 1 W/mm. 1 µA/mm is now becoming more common in the literature as it represents a fairer comparison of voltage-blocking performance of power devices. Figure 3.7(b) presents the benchmark with V_{BR} at

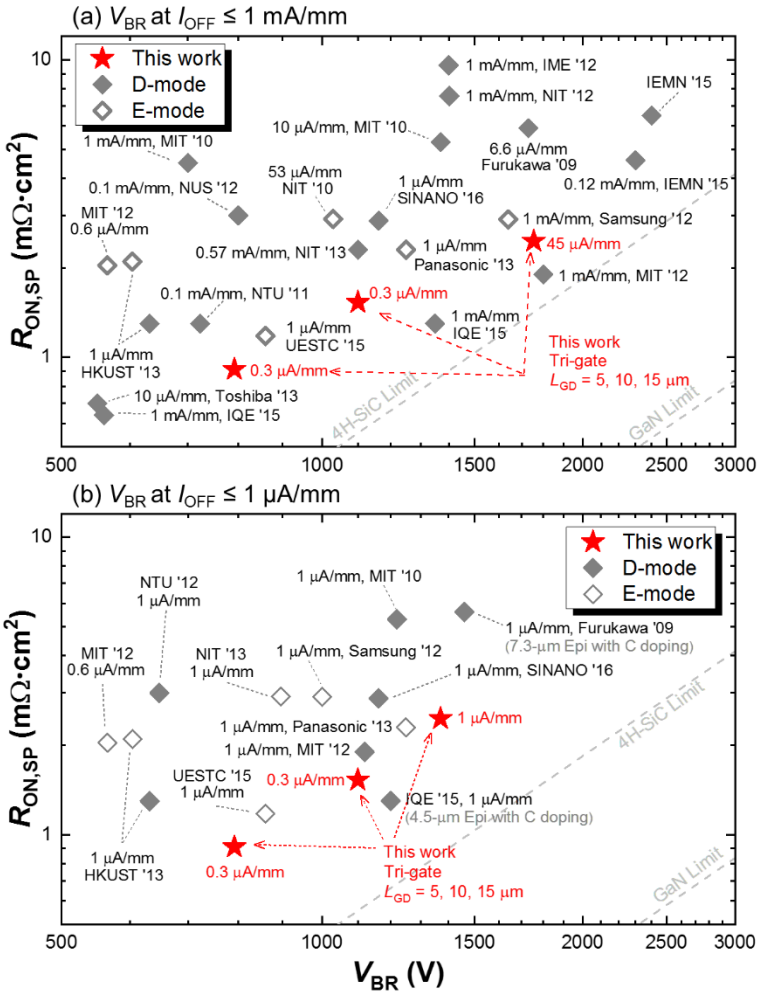

Figure 3.7: $R_{ON,SP}$ versus V_{BR} benchmarks of the tri-gate MOSHEMTs in this work against state-of-the-art GaN E/D-mode (MOS)HEMTs on Si by defining V_{BR} at I_{OFF} (a) ≤ 1 mA/mm and (b) ≤ 1 μA/mm. For fair comparison, literature results with unspecified R_{ON} or I_R were not included. Published in Ref. [32].

I_{OFF} ≤ 1 μA/mm. The V_{BR} for all reference devices was re-calculated based on the reported data following the definition of V_{BR} at I_{OFF} of 1 μA/mm. The 5-μm- L_{GD} Tri-gate exhibited high V_{BR} of 792 V at small I_{OFF} of 0.3 μA/mm, along with small $R_{ON,SP}$ of 0.91 ± 0.08 mΩ·cm^2, which is, to the best of our knowledge, the smallest $R_{ON,SP}$ among GaN (MOS)HEMTs on silicon with V_{BR} > 700 V. The 15-μm- L_{GD} Tri-gate presented high V_{BR} of 1370 V at 1 μA/mm, very close to the best value obtained by 7.3 μm of carbon-doped buffer layers [118], despite its much thinner buffer of 3.75 μm.

In summary, the high performance tri-gate GaN-on-Si MOSHEMTs demonstrated reduced the *SS* and I_{OFF}, enhanced on/off ratio, low R_{ON}, and improved V_{BR}, along with excellent high power FOMs comparable to the state-of-the-art results of planar GaN-on-Si (MOS)HEMTs, revealing the enormous value of nanostructured GaN transistors for the future power conversion.

3.4 High-performance slanted tri-gate GaN-on-Si power MOSHEMTs

In this section we present the unique value of the slanted tri-gate structure (Fig. 3.3(d)) in enhancing the V_{BR} of GaN power MOSHEMTs. While conventional slant FPs (Fig. 3.1(c)) rely on a vertical approach to tailor the V_p is via the thickness of the oxide, the slanted tri-gate relies on a lateral design to tailor its V_p, by simply changing the w_{fin} lithographically, which significantly facilitates the design and fabrication of such slant FPs. We demonstrate this concept for AlGaN/GaN-on-Si MOSHEMTs (Figs. 3.8(a) and (b)) resulting in an large increase of ~500 V in V_{BR} compared to the counterpart planar devices, a high V_{BR} of 1350 V at a small L_{GD} of 10 μm, and a record high-power FOM of 1.2 GW/cm^2 among GaN-on-Si lateral transistors.

The slanted tri-gate AlGaN/GaN-on-Si MOSHEMTs were fabricated using a typical gate-last process. The AlGaN/GaN fins in the slanted tri-gate region were defined with a slanted width and etched with a depth of ~160 nm. The w_{fin} of the slanted nanowire varied from 350 nm at its source side to 700 nm at its drain side (Fig. 3.8(b)). The source-side and drain-side planar portions of the gate metal were 0.5 μm- and 1.5 μm-long, respectively. We also fabricated MOSHEMTs with conventional planar gates and tri-gates on the same chip for comparison. They shared the same design and dimensions as the slanted tri-gate device, except for the nanowires. The planar device had no fins, while the tri-gate device had a constant w_{fin} of 600 nm, instead of slanted. The drain-side planar portion of the gate metal in the tri-gate device was 1.3 μm-long, which is slightly smaller than in the slanted tri-gate device but does not cause any significant changes in the V_{BR} according to our observation. All device characteristics in this work, such as I_D, g_m and I_{OFF}, were normalized by the width of the device footprint (60 μm). To understand the isolated effect of slanted tri-gate in enhancing the V_{BR}, we did not adopt conventional FPs or passivation in these devices.

Figure 3.9 shows the OFF-state breakdown characteristics of the three transistors. An improvement in V_{BR} from 877 to 1100 V at 1 μA/mm was observed with the introduction of the tri-gate region in a portion of the gate (as shown in the insets of Fig. 3.9(a)), which creates a region of a smaller $|V_p|$ within the gate and converts the planar part of the gate towards the drain side into an effective FP, spreading more effectively the electric field as discussed previously in Section 3.2. The V_{BR} was further improved with the slanted tri-gate to 1350 V at 1 μA/mm. Figure 3.9(b) shows the large improvement in V_{BR} reaching the limit of our buffer layers with a L_{GD} as small as 10 μm due to the more effective spreading of the electric field by the slanted tri-gate. More importantly, the significant enhancement observed from the planar to the tri-gate and slanted tri-gate transistors was achieved by simply patterning the tri-gate and slanted tri-gate regions during the mesa etching to engineer the

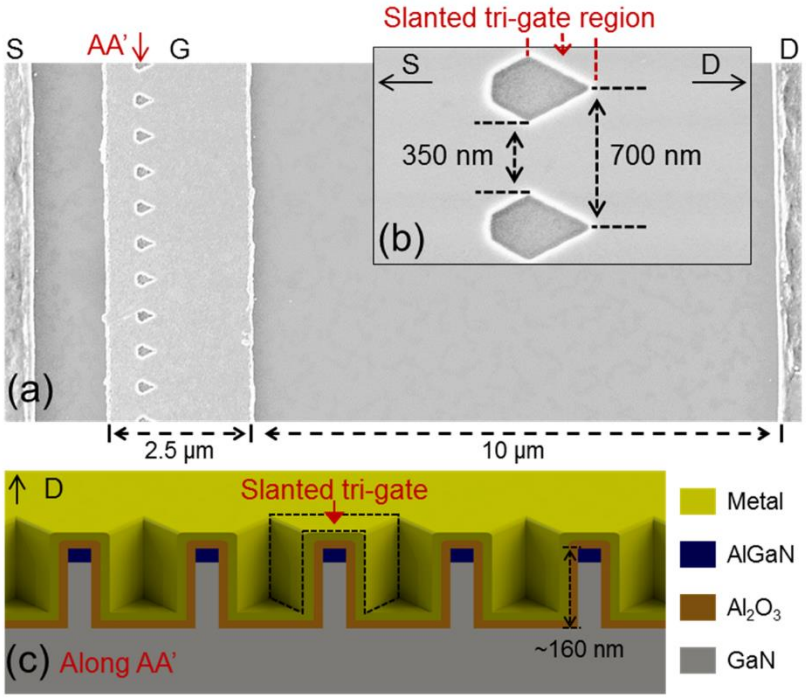

Figure 3.9: Top-view SEM images of the slanted tri-gate MOSHEMT (a) with and (b) without the gate dielectric and the metal. (c) A cross-sectional schematic of the slanted tri-gate along the arrow AA'. Published in Ref. [31].

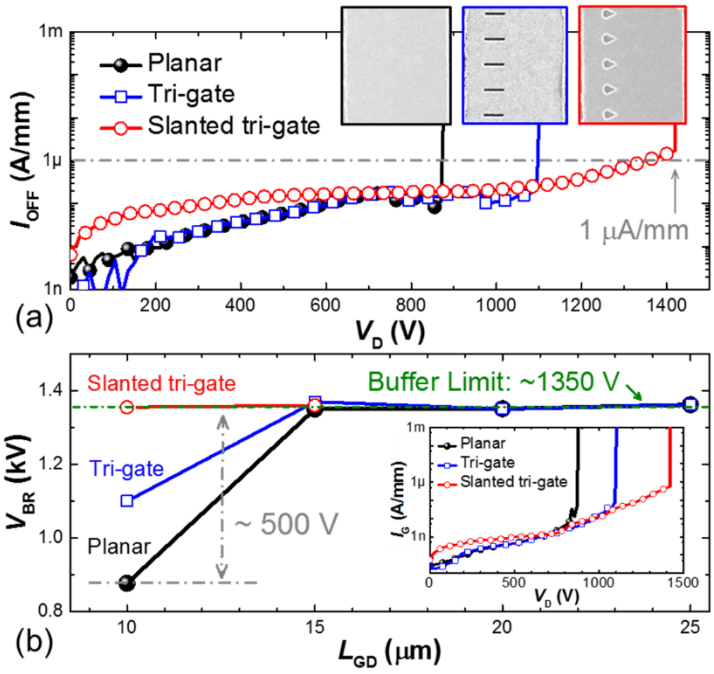

Figure 3.9: Typical breakdown characteristics of the MOSHEMTs with planar gates, tri-gates and slanted tri-gates and (b) their L_{GD}-dependent V_{BR} (at 1 μA/mm), measured at V_G of -10 V with a floating substrate. The insets in (a) show the top-view SEM images of the gate region of the three types of devices. The inset in (b) shows the gate leakage current of the devices. The L_{GS}/L_GL_{GD} are 1.5/2.5/10 μm, respectively. Published in Ref. [31].

pinch-off voltage. The remainder of the device structure and fabrication process is exactly the same of the planar device. The larger I_{OFF} of the slanted tri-gate device at small voltages is likely due to its much smaller effective gate length, since the three devices have the same buffer leakage current as

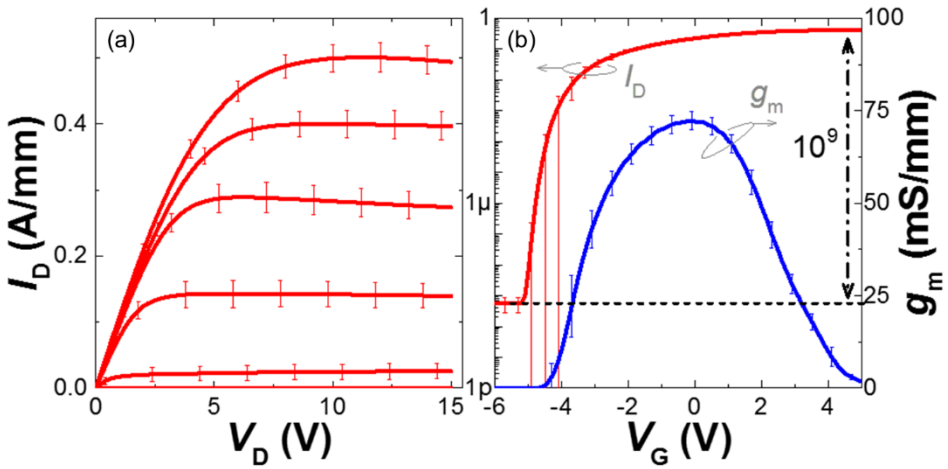

Figure 3.10: (a) Average output and (b) transfer characteristics of the slanted tri-gate devices, normalized by their foot-print width. The error bars were determined from measurements on six devices. The $L_{GS}/L_G/L_{GD}$ were 1.5/2.5/10 µm, respectively. Published in Ref. [31].

they were fabricated on the same chip, and exhibited small gate leakage currents ≤ 2 nA/mm at 750 V (the inset of Fig. 3.9(b)). The I_{OFF} of the slanted tri-gate devices at high voltages was similar to the other devices, which shows that the larger I_{OFF} at low biases does not degrade the value of the slanted tri-gate in enhancing the V_{BR} of the device.

In addition to the high V_{BR}, the slanted tri-gate device also exhibited excellent ON-state characteristics (Fig. 3.10), presenting a high ON/OFF-current ratio over 10^9 and a maximum g_m of 72.4 ± 2.4 mS/mm (at V_D of 5 V), higher than in the planar device (66.1 ± 2 mS/mm). The R_{ON} was 9.4 ± 0.5 Ω·mm, very close to that of the planar device (9.1 ± 0.2 Ω·mm) despite the removal of carriers in its gate region during the nanowire etching, thanks to the small length of the fins with respect to the large distance between the source and drain as discussed in Section 2.4.2.

The slanted tri-gate devices were benchmarked against state-of-the-art GaN (MOS)HEMTs on silicon substrates (Fig. 3.11). The high V_{BR} of 1350 V at 1 µA/mm presented in this work is comparable to the best-reported value of V_{BR} (1460 V) [118] but with a 14-µm-smaller L_{GD}, resulting in a 3.6x-smaller $R_{ON,SP}$. The high-power FOM of the slanted tri-gate transistors was up to 1.2 GW/cm^2, which is a record value to the best of our knowledge and reveals the significant value of the slanted tri-gate for the enhancement of V_{BR} in GaN power devices while maintaining small L_{GD} and R_{ON}.

3.5 Conclusion

In this chapter we presented the concept of novel FP structures using the tri-gate technology, which rely on a lateral scheme to tailor the V_p by simply tuning the w_{fin} using lithography. This technology does not require complicated fabrication process as compared to the conventional vertical scheme for the FPs by tuning the FP oxide layer, and greatly facilities the fabrication and optimization of optimal

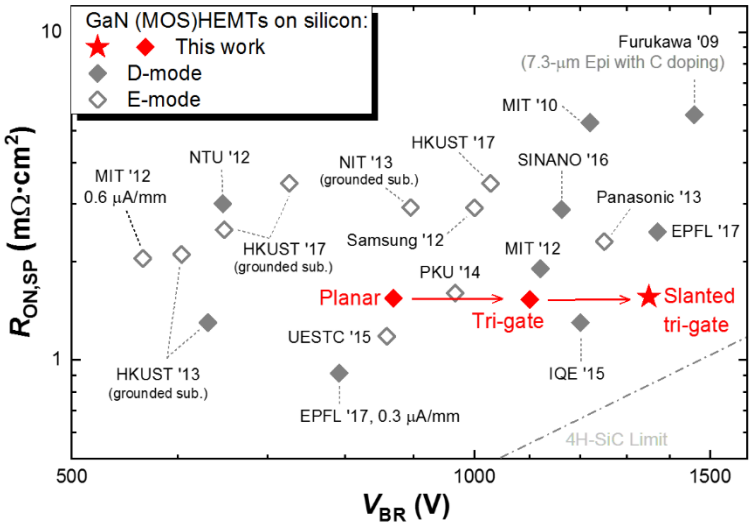

Figure 3.11: Specific on-resistance ($R_{ON,SP}$) versus V_{BR} benchmarks of the slanted tri-gate MOSHEMTs against state-of-the-art GaN E/D-mode (MOS)HEMTs on silicon by defining the V_{BR} at $I_{OFF} \leq 1$ μA/mm. A 1.5-μm transfer length for each ohmic contact was considered for calculation of the $R_{ON,SP}$, and the V_{BR} for all reference devices was re-calculated based on the reported data following the definition of V_{BR} at $I_{OFF} \leq 1$ μA/mm. Published in Ref. [31].

FP structures.

We firstly demonstrated this concept in tri-gate GaN-on-Si power MOSHEMTs. By including the tri-gate into a conventional planar gate, a portion of the planar gate was converted into an integrated gate FP and the V_{BR} was greatly enhanced. The common issue of large R_{ON} in tri-gate GaN transistors was also resolved, resulting in zero degradation in R_{ON} as compared to planar MOSHEMTs, along with benefits of diminished I_{OFF}, reduced *SS*, and increased on/off ratio. With L_{GD} of 5 μm, the tri-gate MOSHEMTs exhibited V_{BR} of 792 V at as small I_{OFF} of 0.3 μA/mm, along with a small specific on-resistance ($R_{ON,SP}$) of 0.91 ± 0.08 mΩ·cm^2, which is the smallest R_{ON} among GaN-on-Si MOSHEMTs with VBR > 500 V and can be highly promising for 200 V applications. With L_{GD} of 15 μm, high V_{BR} of 1370 V at I_{OFF} = 1 μA/mm was achieved, rendering excellent high-power figure of merits comparable to state-of-the-art planar GaN-on-Si (MOS)HEMTs.

We further developed the tri-gate into a novel slanted tri-gate structure, whose V_p can be tailored laterally by varying *w* with lithography to form a gradient of V_p as in conventional slant FPs, but with the advantages of a much easier fabrication process with way higher controllability. Our slanted tri-gate GaN-on-Si MOSHEMTs presented a large increase of ~500 V in V_{BR} compared to the counterpart planar devices, a high V_{BR} of 1350 V at 1 μA/mm with a small L_{GD} of 10 μm, and a record high-power FOM of 1.2 GW/cm^2 among GaN-on-silicon lateral transistors. This slanted tri-gate technology can greatly the device size (L_{GD}) and R_{ON} for 650 V-rated devices, resulting in a higher R_{ON}·*A* product that is highly demanded for efficient power conversion.

In summary, the tri-gate technology provides a new degree of freedom to engineer the distribution of electric field in GaN power devices for enhanced voltage-blocking performance of the devices, and opens enormous opportunities for nanostructured GaN devices in future power applications.

Chapter 4 Tri-gate technologies for high-voltage and low-leakage SBDs

4.1 Introduction

SBDs are indispensable devices in power electronics, and GaN-on-Si SBDs are highly promising for power diodes, thanks to the remarkable materials capabilities of GaN and the low cost of large size Si substrate [123]–[130]. In addition, GaN-on-Si SBDs are typically based on a lateral AlGaN/GaN heterostructure, sharing the same material platform as GaN power (MOS)HEMTs, which can be monolithically integrated with GaN HEMTs to form advanced power ICs with greatly enhanced efficiency, frequency and compactness of future power converters [131]–[137].

Despite these advantages, a major obstacle for GaN-on-Si SBDs is their limited voltage-blocking performance. Efficient power devices must present high breakdown voltage (V_{BR}) and small reverse leakage current (I_R), which are however very challenging in GaN SBDs. Firstly, the I_R in GaN SBDs is typically large, being dominated by many non-ideal effects that are very difficult to eliminate, such as tunneling[138]–[146]. Secondly, although a small Schottky barrier (Φ_B) leads to a small V_{ON}, it also increases the I_R, thus there is a natural trade-off between good ON- and OFF-state performances. Finally, the lateral current conduction in GaN SBDs results in an inhomogeneous distribution of the electric field, which severely limits their V_{BR} [23], [24], despite the resistivity of their buffer layers. Consequently, the poor voltage-blocking capability in GaN-on-Si SBDs is usually limited by the device architecture [33], rather than their buffer layers. As an example, the voltage-blocking performance of GaN-on-Si SBDs is still much inferior than that of GaN-on-Si transistors, even though they share the same material platform. While GaN-on-Si power transistors have been commercialized for applications up to 650 V, GaN-on-Si SBDs for such ratings are still missing. When defining the V_{BR} at I_R of 1 μA/mm as typically reported in the literature, only a few SBDs with V_{BR} over 500 V have been reported at the time [123], [125], [127], [130], [147], and the highest value is only about 900 V [123], along with large I_R that is far beyond 0.1 μA/mm at even a small reverse bias of 100 V, which are not promising for practical power applications.

In this chapter, we will illustrate the unique value of the tri-gate technology for high-voltage and low-leakage lateral GaN SBDs, propose a general model of reducing the pinch-off voltage (V_p) of the field

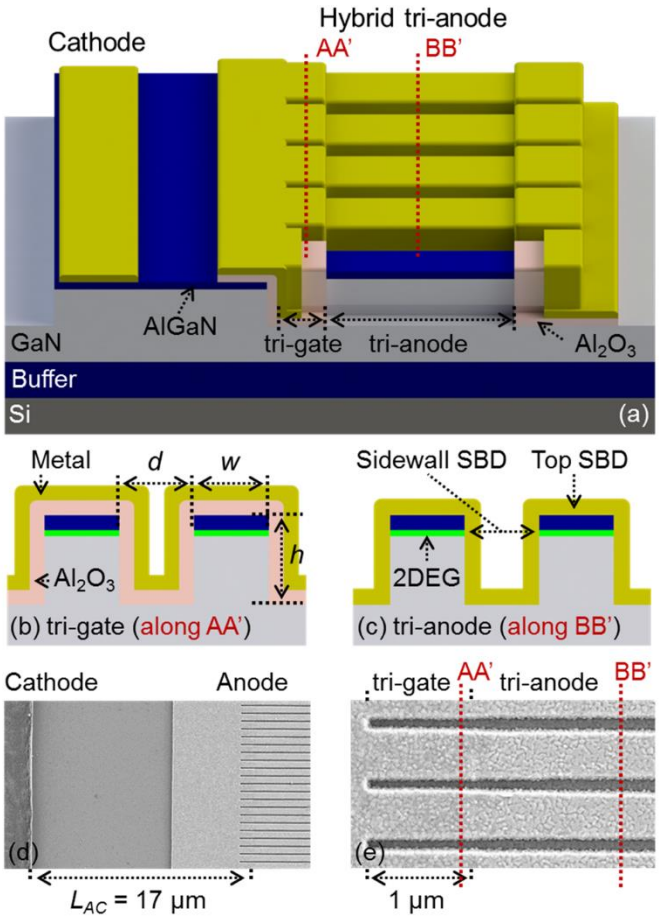

Figure 4.1: (a) Schematic of the tri-anode SBDs. Cross-sectional schematics of (b) the tri-gate region along line AA' and (c) the tri-anode region along line BB'. (d) Top-view SEM image of the fabricated hybrid tri-anode SBDs. (e) Zoomed-in SEM image of the tri-gate and tri-anode regions. Published in Ref. [34].

plate (FP) for low leakage current, and demonstrate slanted tri-gate GaN-on-Si SBDs with unprecedented blocking voltage (2 kV at 1 µA/mm) and state-of-the-art reverse-blocking GaN-on-Si power transistors with slanted tri-gate Schottky drain electrodes.

4.2 High-voltage tri-anode GaN-on-Si SBDs with low leakage current

In this section we present AlGaN/GaN-on-Si Schottky barrier diodes (SBDs) with high V_{BR} and low I_R, based on a hybrid of tri-anode and tri-gate architectures (Fig. 4.1(a)). The hybrid tri-anode integrates a tri-anode, tri-gate MOS and planar field plate (FP) regions. The tri-anode contacts directly the 2DEG for a small V_{ON} (Fig. 4.1(c)), and, in OFF state, pins the voltage drop at the Schottky junction to the value of its pinch-off voltage, which is very small for a small w_{fin}, resulting in a small I_R. The tri-gate region (Fig. 1(b)) works as tri-gated FPs to shield the tri-anode region from high voltages, which along with the planar FP improves the V_{BR}. The reduction in I_R by the hybrid tri-anode will be explained with more details in the next section.

The AlGaN/GaN epitaxy used for the SBDs consisted of 3.75 µm of buffer, 0.3 µm of un-doped GaN (u-GaN) channel, 23.5 nm of AlGaN barrier and 2 nm of u-GaN cap layer. The fabrication was similar

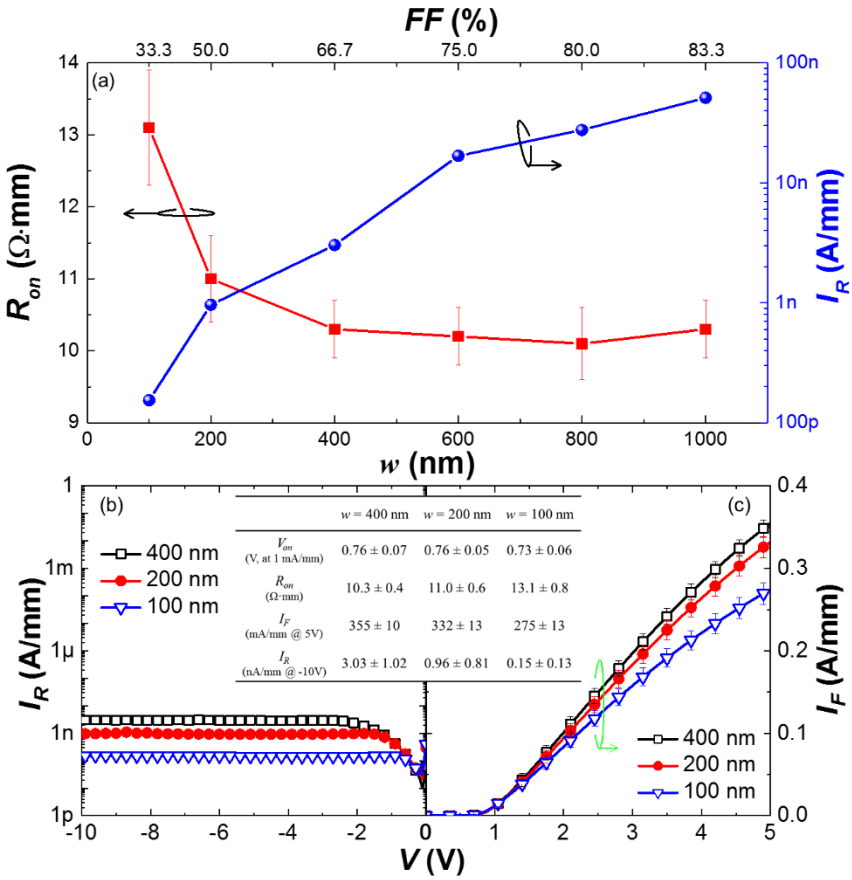

Figure 4.2: (a) R_{ON} and I_R (at -10 V) of tri-anode SBDs with different w_{fin}. (b) Reverse and (c) forward *I-V* characteristics of the tri-anode SBDs with w_{fin} of 400, 200 and 100 nm, normalized by the width of device footprint. The inset summarizes the performance of tri-gate SBDs with different w_{fin}. Published in Ref. [34].

to that for the tri-gate MOSHEMTs described in Section 3.3. The height of the fins was 166 nm, and the w_{fin} varied from 100 to 1000 nm, while the spacing was fixed at 200 nm. Figures 4.1(d) and (e) show the top-view SEM images of the SBD and the hybrid tri-anode, respectively. All current values such as forward current (I_F) and I_R were normalized by the width of the device footprint (60 µm), and the error bars were determined from measurements on up to 10 separate devices of the same kind.

The impact of w_{fin} on the R_{ON} and I_R of the tri-anode SBDs is presented in Fig. 4.2(a). The observed reduction of R_{ON} with *w* increasing from 100 to 400 nm is mainly attributed to the increasing filling factor (*FF*), which preserved more 2DEG in the tri-gate region and hence reduced the resistance of the integrated tri-gate transistors. After w_{fin} reached 400 nm (*FF* = 66.7%), the R_{ON} saturated regardless of the increasing w_{fin}, or equivalently the *FF*, at about 10.2 ± 0.45 Ω·mm, and the I_R, taken at *V* = -10 V, kept reducing with decreasing w_{fin} due to the enhanced gate depletion of the integrated tri-gate transistor with narrower fins. With w_{fin} below 400 nm, the I_R of all tri-anode SBDs was below 10 nA/mm at a bias of -10 V, and a *w* of 400 nm yielded a good balance between I_R and R_{ON}. The I_R and I_F of the tri-anode SBDs with w_{fin} of 400, 200 and 100 nm are plotted versus anode voltage (*V*) in Figs. 4.2(b) and (c), respectively, with their detailed characteristics listed in the inset in Fig. 4.2. The

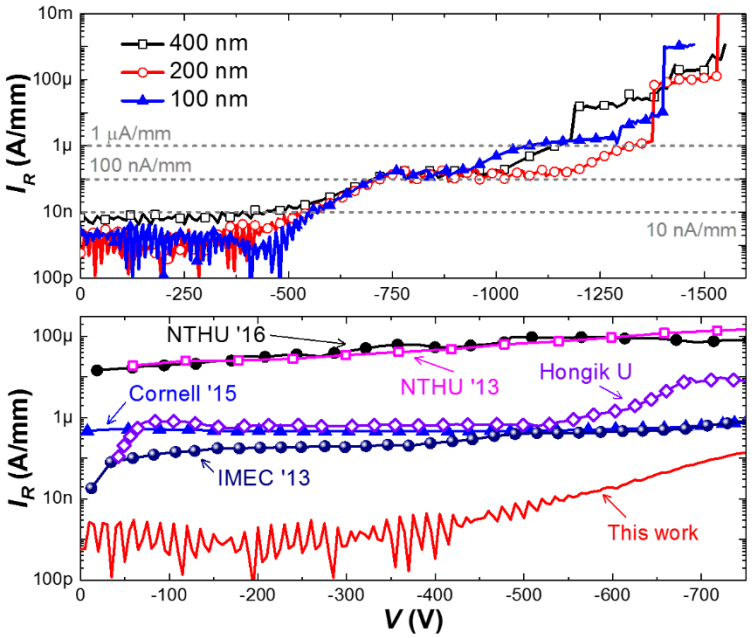

Figure 4.3: (a) Reverse-bias characteristics of the tri-anode SBDs versus anode bias for different wfin and (b) comparison of I_R of the tri-anode SBD (w_{fin} = 200 nm) and state-of-the-art high-voltage GaN-on-Si lateral SBDs. The I_R for the SBDs with w_{fin} of 200 and 100 nm was likely around or below the measurement limit of our setup. Published in Ref. [34].

tri-anode SBDs with w_{fin} of 100 nm exhibited I_R of 0.15 ± 0.13 nA/mm, which is, to the best of our knowledge, the smallest I_R for GaN lateral SBDs up to date.

Figure 4.3(a) presents the I_R of the tri-anode SBDs versus V. All devices exhibited very small I_R below 10 and 100 nA/mm with V up to about 500 and 700 V, respectively. For V below 400 V, the I_R of the tri-anode SBDs with w_{fin} of 200 and 100 nm was close or below the measurement limit of our setup, hence large oscillations in current were observed. The best V_{BR} measured at I_R = 1 µA/mm was 1140, 1325 and 1075 V for the tri-anode SBDs with w of 400, 200 and 100 nm. We have not observed a clear dependence of the V_{BR} on w_{fin} in this work, and the difference in V_{BR} was likely impacted by local variations in oxide quality or possible fabrication misalignments. Nevertheless, the I_R profile was quite consistent up to 900 V among all devices with w_{fin} from 100 to 400 nm, as well as their hard breakdown voltage at around 1400 - 1550 V.

The reverse leakage current of the tri-anode SBDs (w_{fin} = 200 nm) was much lower than that from state-of-the-art high-voltage GaN-on-Si lateral SBDs (with hard breakdown voltage beyond 1000 V) in the literature, as plotted in Fig. 4.3(b). For reverse voltages below 500 V, the I_R of the tri-anode SBD was about 2 orders of magnitude lower with respect to the smallest I_R [126] among these references and over 4 orders of magnitude as compared to the reference SBD with the highest reported hard V_{BR} [124]. Most of the references presented I_R beyond 100 nA/mm and 1 µA/mm at V of -100 and -650 V, respectively. In contrast, the I_R of the tri-anode SBD did not reach 100 nA/mm until -725 V and was as small as 41 nA/mm at -650 V. Such significant reduction in I_R can potentially improve

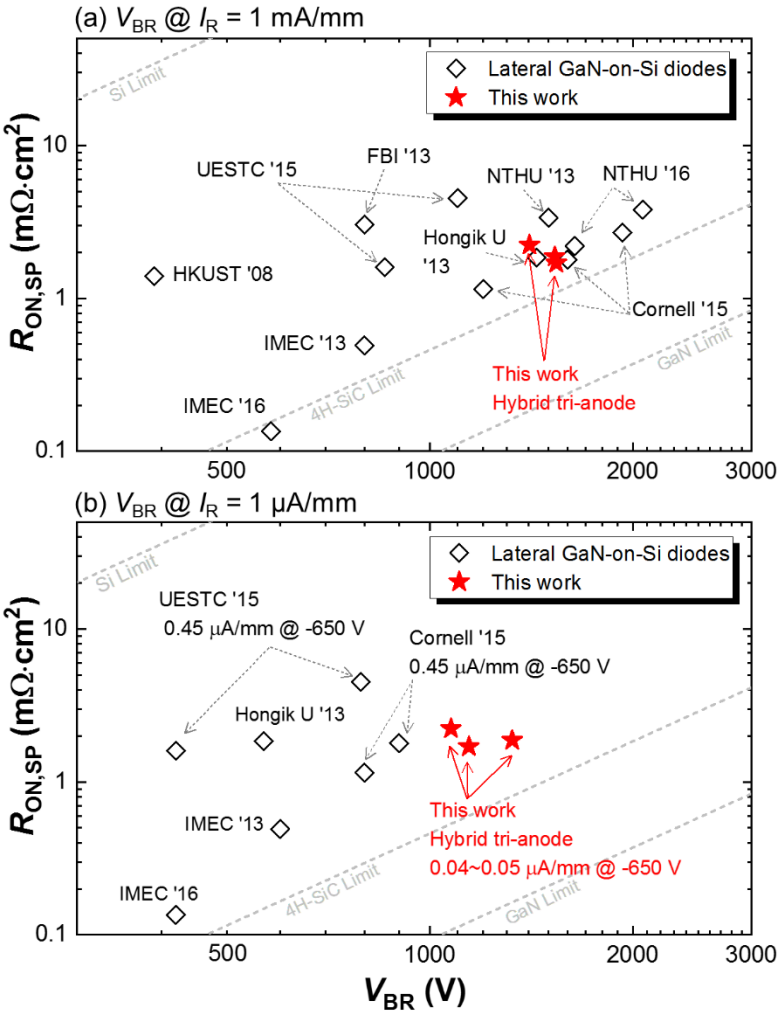

Figure 4.4: $R_{ON,SP}$ versus V_{BR} benchmarks of the tri-anode SBDs with state-of-the-art GaN lateral power diodes by defining V_{BR} at I_R = 1 mA/mm (a) and 1 μA/mm (b). For fair comparison, literature results with unspecified $R_{ON,SP}$ or I_R were not included. Published in Ref. [34].

the reliability of the device, and more importantly, reduce the off-state power dissipation and increase the efficiency of power converters. The off-state power dissipation, calculated using $Power = I_R \times V$, varied from 0.31 - 78 mW/mm at -650 V for the reference SBDs, while that of the tri-anode SBD was several orders of magnitude smaller, below 0.03 mW/mm.

The tri-anode SBDs presented in Fig. 4.3 were benchmarked against state-of-the-art lateral GaN-on-Si diodes, as shown in Fig. 4.4. Two commonly used definitions of V_{BR} for GaN power devices were adopted, taken at I_R = 1 mA/mm and 1 μA/mm. In the benchmark considering V_{BR} at I_R = 1 mA/mm (Fig. 4.4(a)), the tri-anode SBDs with w_{fin} of 400, 200 and 100 nm exhibited high power FOMs of 1355, 1255 and 865 MW/cm^2, respectively, which are comparable to the best results for GaN lateral diodes on silicon and even other substrates [147]–[149]. Since 1 mA/mm is a large leakage current level to define the V_{BR} for power devices, 1 μA/mm level is becoming more commonly used to compare more fairly the blocking performance of power devices. Figure 4.4(b) shows the benchmark with

V_{BR} at I_R = 1 μA/mm. The V_{BR} for all reference devices was re-calculated based on the reported data, following the definition of V_{BR} at I_R = 1 μA/mm. The tri-anode SBDs with w_{fin} of 400, 200 and 100 nm presented FOM values of 747, 939 and 518 MW/cm^2. These are high FOM values with record V_{BR} among up-to-date GaN lateral power diodes on silicon, which in addition to the low turn-on voltage, low I_R and small on-resistance, reveal the extraordinary value of nanowire-based approaches for GaN power electronics.

4.3 Field plate design for low leakage current in lateral GaN SBDs

A major obstacle for current lateral AlGaN/GaN SBDs is their large I_R, mostly over 0.1 μA/mm at a reverse bias as small as 100 V, as efficient and reliable power conversion requires devices with small I_R below 1 μA/mm or preferably 0.1 μA/mm at high blocking voltages [150]. While many techniques have been proposed to address this issue, their effect is limited by parasitic leakage paths under high biases, such as thermionic field emission and trap-assisted tunneling [138]–[146]. In last section we have significantly diminished the I_R ($\leq$ 0.1 μA/mm at -700 V) in GaN SBDs using the tri-gate technology. Yet the physical origin of such improvement is not clear. More importantly, a general model for the reduction of I_R is still missing, which is crucial to unleash the full potential of lateral SBDs for the next generation of power converters.

In this section we present a general approach to reduce the I_R in SBDs by designing the V_p of their FPs, which, in addition to explaining the improvement in the tri-anode SBDs, provides a pathway for low leakage lateral GaN power Schottky diodes. A reduction of V_p results in a decreased voltage drop at the Schottky junction (V_{SCH}) in OFF state and correspondingly a smaller I_R. We verified this model using a tri-gate structure to reduce the V_p in AlGaN/GaN SBDs, which resulted in very small I_R, below 10 nA/mm at -500 V, along with an enhancement over 800 V in V_{BR}.

The I_R in SBDs is determined by three components: 1. Leakage by thermionic emission, which comprises the I_R of an ideal SBD; 2. Thermionic field emission, tunneling and other similar non-ideal effects ($I_{FE,T}$), which dominate the I_R in real devices [138]–[146]; 3. Leakage through buffer layers, which is negligible under low voltages for SBDs on high-resistivity buffer layers. Many sophisticated schemes have been proposed to reduce the $I_{FE,T}$ by reducing defects and traps [151]–[154], yet the I_R is still large in most of GaN-on-silicon SBDs. This is likely due to the high electric field under large reverse biases and also the high defect density in GaN on Si.

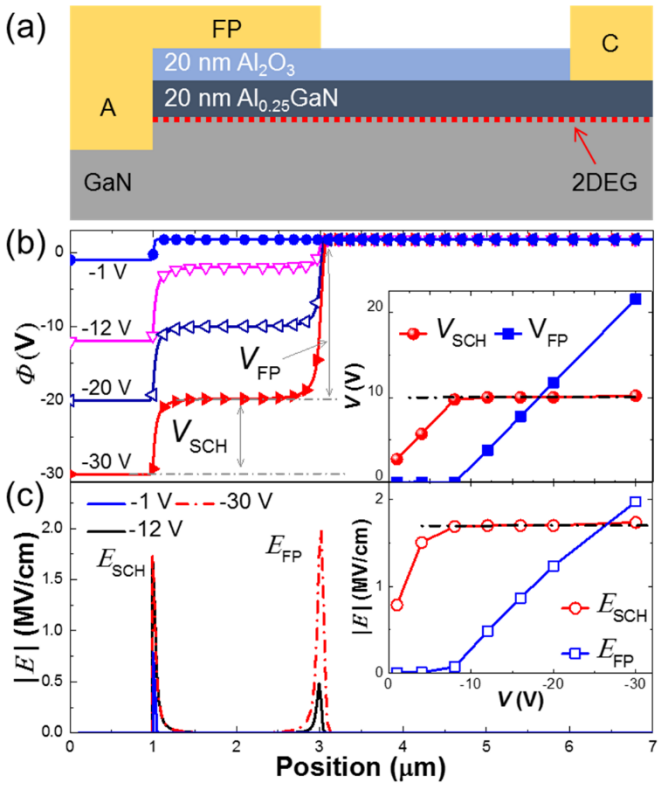

Figure 4.5: (a) A cross-sectional schematic of a lateral AlGaN/GaN SBD with typical planar FP. Simulated distributions of (b) potential (Φ) and (c) electric field (E) at the channel in OFF state for different anode voltages, in which only in-plane electric field was considered. The insets show the summarized dependences of the V_{SCH} and the E_{SCH} on the voltage. Published in Ref. [33].

However, $I_{FE,T}$ is not only determined by the density and energy levels of the traps, but also increases with the voltage drop at the Schottky junction (V_{SCH}) (or the electric field (E_{SCH})). In this work we propose an approach to reduce the V_{SCH} and E_{SCH} by reducing the $|V_p|$ of the FPs, which in addition to reducing the I_R also increases the V_{BR} of the SBDs. To illustrate the principle, we simulated the distribution of potential (Φ) and electric field (E) in a typical SBD with a recessed anode and a conventional planar FP in OFF state (Fig. 4.5), using ATLAS SILVACO. When the reverse bias in the anode is smaller than $|V_p|$, which in this case is about 10 V (extracted by simulating a transistor with the FP as the gate), the voltage drops only at the Schottky junction (inset of Fig. 4.5(b)). As the reverse bias reaches $|V_p|$, the FP depletes the channel beneath and the voltage starts to drop at the cathode-side edge of the FP, resulting in a second peak of electric field. Then V_{SCH} saturates at $|V_p|$, regardless of further increase of the bias, as summarized in the insets of Figs. 4.5(b) and (c), respectively. These results agree well with Refs. [23] and [24], and suggest that the FP can be used to control the I_R in SBDs, as a smaller $|V_p|$ reduces the maximum V_{SCH} and E_{SCH} at the Schottky junction and hence diminishes the I_R.

To reduce the $|V_p|$, a few ways can be adopted including a partial recess of the AlGaN barrier layer and so on. However, a precise control to obtain a series of V_p with these methods is very challenging,

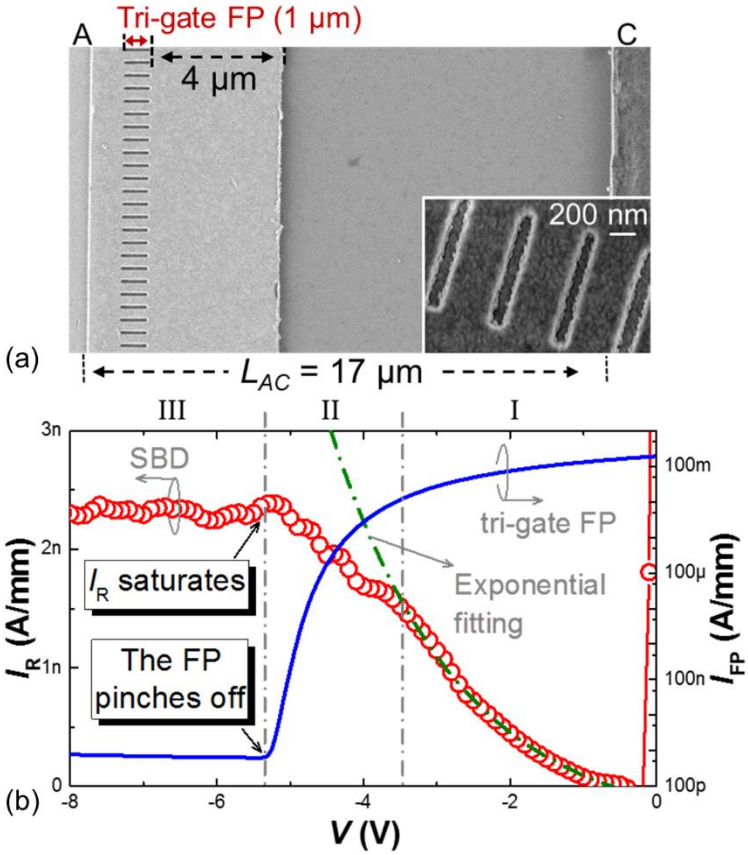

Figure 4.6: (a) Top-view SEM images of the fabricated AlGaN/GaN SBD with a tri-gate FP. (b) I_R of the SBDs and the pinch-off characteristic of the tri-gate FPs as a function of the voltage. All characteristics were averaged from about 8 devices of the same kind and normalized by the width of the device footprint (60 µm). The turn-ON voltage (V_{ON}) of these SBDs was 0.9 ± 0.1 V, extracted at a forward current of 1 mA/mm. Published in Ref. [33].

which makes them less suited to explore the $|V_p|$ dependence of the I_R. Here we used a tri-gate structure to reduce the $|V_p|$ [31], as it offers great control to tune the V_p by changing the w_{fin} in the tri-gate. We implemented tri-gate FPs in SBDs for both conventional recessed anodes and novel tri-anodes [34] to justify our approach, and compared them with other literature results to show the generality of the model. All these SBDs were fabricated on the same chip, sharing similar device dimensions such as a cathode-to-anode separation (L_{AC}) of 17 µm and the same width of device footprint (60 µm), by which all current values in this section were normalized.

According to the model we developed, the I_R should saturate when the V_{SCH} is pinned after the pinch-off of the FP. To verify this, we compared the I_R of an SBD and the pinch-off characteristics of its FP (Fig. 4.6). The SBD had 1 µm-long tri-gate FPs (Fig. 4.6(a)), in which the w_{fin} and the spacing of the nanowires were 300 nm and 200 nm, respectively. These SBDs had recessed anodes with a recess depth of ~160 nm. The average pinch-off characteristic of the tri-gate FPs, shown in Fig. 4.6(b), was determined from transfer characteristics of tri-gate GaN MOSHEMTs on the same chip at V_{DS} of 5 V. The nanowires in the MOSHEMTs had a w_{fin} of 300 nm with a length of 700 nm. As shown in Fig. 4.6(b), I_R increases exponentially with the reverse bias in Region I, which is dominated by $I_{FE,T}$. As

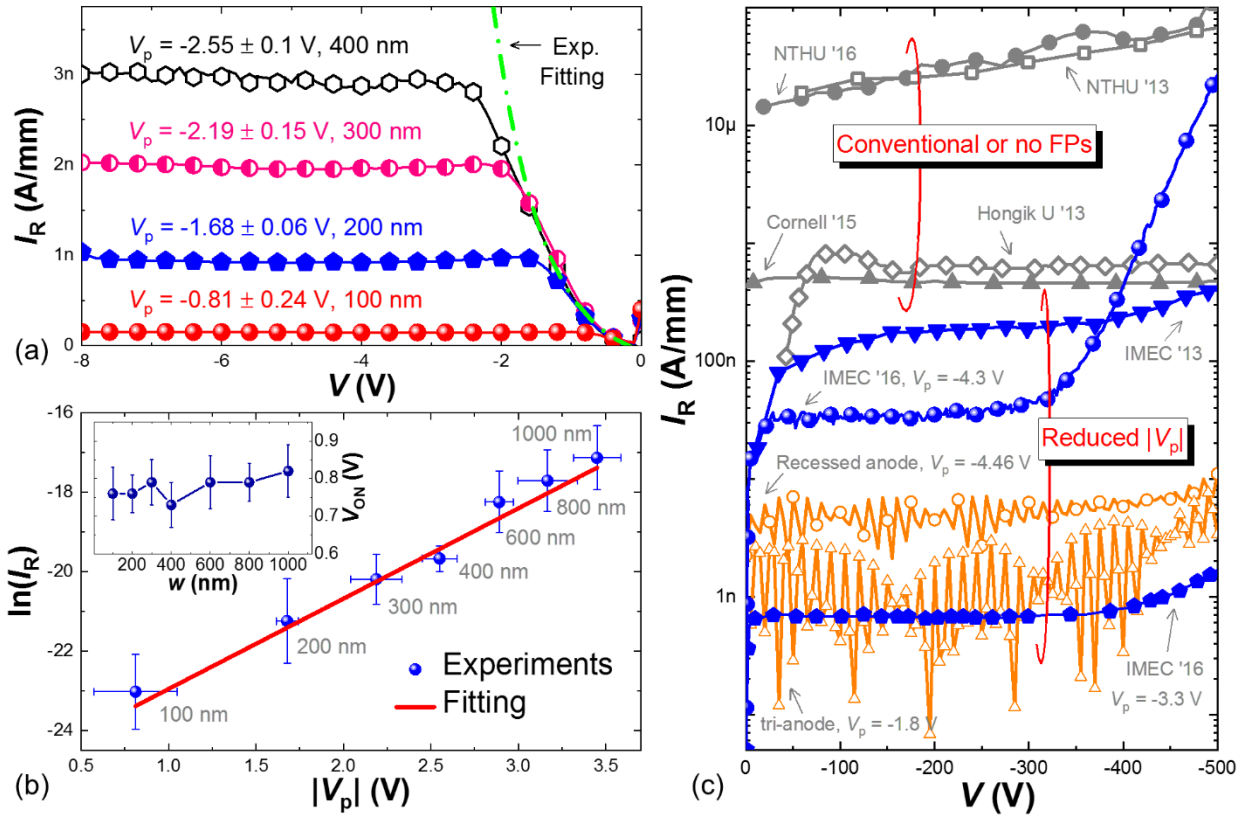

Figure 4.7: (a) Comparison of the I_R in hybrid tri-anode SBDs with different w_{fin} and thus different V_p. (b) A linear fitting of the ln(I_R) at -10 V and the $|V_p|$. The inset shows the V_{ON} of these devices as a function of w_{fin}. The spacing between nanowires in these devices was 200 nm. I_R was normalized by their total width of 60 µm (the width of the device footprint) and the error bars were determined from about 8 devices of each kind. (c) Comparison of I_R from AlGaN/GaN-on-Si SBDs with various FP designs in the literature and this thesis. Published in Ref. [33].

the FP starts to pinch off the channel, the increase of I_R slows down (Region II). Finally I_R saturates as the FP completely pinches off the channel (Region III), agreeing well with our model.

To demonstrate the dependence of the I_R with the $|V_p|$, we studied the tri-anode SBDs discussed in Section 4.2, since their $|V_p|$ can be reduced by decreasing the w of the tri-anode (which are basically tri-gate HEMTs without the oxide). Figure 4.7(a) shows the I_R of tri-anode AlGaN/GaN SBDs with different w_{fin}, thus different V_p, which follow a similar exponential increase before the pinch off of their FPs and then saturate as V reaches V_p. As $|V_p|$ decreases for narrower nanowires, the saturated I_R diminishes due to the reduced V_{SCH}. This reduction of I_R is not likely caused by the change of the Schottky barrier height, as we observed little dependence of the V_{ON} on the w_{fin} (the inset of Fig. 4.7 (b)). Figure 4.7 (b) shows a linear relationship of the $ln(I_R)$ with $|V_p|$, due to the exponential increase of I_R before the pinch off of the FPs (Fig. 4.7(a)). Such linear dependence was not affected by the choice of normalization of the I_R (either by with of device footprint, effective channel width or number of fins).

The reduction of I_R with $|V_p|$ can be generally applicable to devices with different approaches to tune

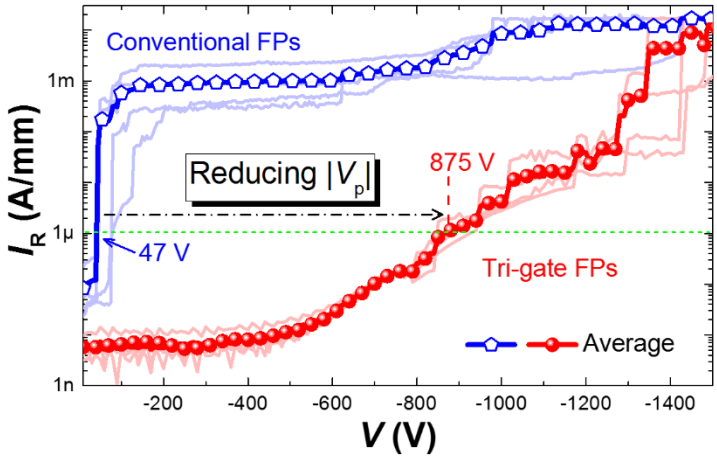

Figure 4.8: Breakdown characteristics of the SBDs with and without the tri-gate FPs, measured with floating substrates. Published in Ref. [33].

the pinch-off voltage, not only to tri-anode SBDs. For instance, a reduced $|V_p|$ was achieved by recessing the AlGaN barrier in the FP [130] or by thinner FP oxide [155], both of which led to a significant reduction of I_R. The I_R from state-of-the-art AlGaN/GaN-on-Si SBDs with different FP designs were compared in Fig. 4.7(c). SBDs with no FPs or conventional FPs (grey) exhibited large I_R beyond 0.1 μA/mm at very small biases, while the I_R was much smaller in SBDs with reduced $|V_p|$ by either AlGaN recess (blue) or tri-gate FPs (orange). This observation from different groups in the literature supports our model correlating small I_R with small $|V_p|$, despite the different fabrication process and epi-layers.

One crucial benefit of the reduced I_R by decreasing the $|V_p|$ is the enhanced soft V_{BR}. Conventional FPs are usually based on oxide/AlGaN/GaN structures, which have large negative V_p due to the high carrier concentration in the 2DEG and possible charges in the oxide. This leads to a large V_{SCH}, causing the I_R to increase rapidly to 1 μA/mm (at which the V_{BR} is typically defined), and resulting in a very small V_{BR}. As the $|V_p|$ is reduced, the leakage current through the Schottky junction saturates at smaller levels, until it is dominated by the highly resistive buffer layers at larger voltages, rather than only by the leaky Schottky junction. This leads to a significantly improved V_{BR}, which is over 800 V in our case (Fig. 4.8).

To sum up, in this section we proposed a general approach to reduce the I_R in SBDs by reducing the $|V_p|$ of their FPs, which led to ultra-low I_R below 10 nA/mm at -500 V and enhanced the V_{BR} by over 800 V. These results revealed the importance of a proper FP design for reducing the I_R in SBDs, unveiled the significant potential of the tri-gate FPs, and can pave the path for efficient lateral architecture for future power SBDs.

4.4 2000 V slanted tri-gate SBDs with ultra-low leakage current

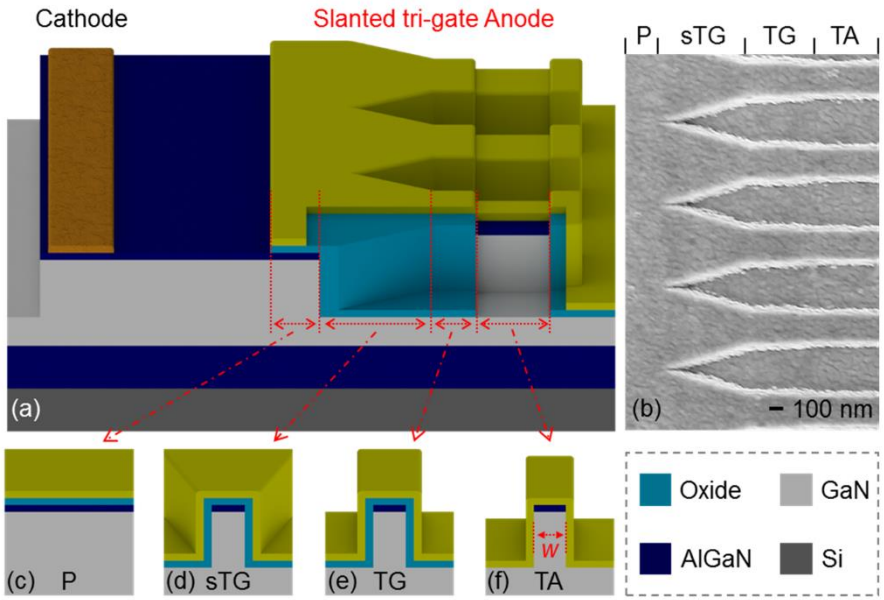

Figure 4.9: (a) Schematic of the slanted tri-gate SBD and (b) a top-view scanning electron microscopy (SEM) image of the anode region. Cross-sectional schematics of the (c) planar (P), (d) slanted tri-gate (sTG), (e) tri-gate (TG) and (f) tri-anode (TA) regions composing the anode. Published in Ref. [35].

In this section we demonstrate high-performance GaN-on-Si power SBDs with superior voltage-blocking capabilities (2 kV at 1 μA/mm), by integrating hybrid tri-anode (Section 4.2) and slanted tri-gate (Section 3.4) architectures. The hybrid tri-anode reduced the I_R by controlling the V_{SCH} with w_{fin}, resulting in an ultra-low I_R of 51 ± 5.9 nA/mm at -1000 V, and in a small V_{ON} of 0.61 ± 0.03 V. The slanted tri-gate provided a continuous gradient of pinch-off voltage (V_p) from the anode towards the cathode, spreading effectively the electric field in OFF state, leading to a record V_{BR} of 2 kV at 1 μA/mm. These results establish a milestone for GaN power devices, and could lead to enormous opportunities for future monolithic GaN power circuits.

The devices were fabricated based on an $Al_{0.25}Ga_{0.75}N$/GaN heterostructure grown on Si substrate with 5 μm-thick buffer layers. The fabrication of the slanted tri-gate SBDs (Fig. 4.9) started with e-beam lithography to define the fins in the anode, which were etched by inductively coupled plasma with a depth of ~180 nm. The w_{fin} and spacing of the fins in the tri-gate and tri-anode regions were 200 nm and 400 nm, respectively, while the w_{fin} in the slanted tri-gate region increased continuously from 200 nm to 600 nm towards the cathode. The devices were isolated by mesa etching, and the cathode ohmic contact was formed by alloying Ti/Al/Ti/Ni/Au at 830 ºC. Then 10 nm SiO_2 and 10 nm Al_2O_3 were deposited by atomic layer deposition and selectively removed in the tri-anode region. Finally the anode contact was formed with Ni/Au. The oxide in the access and ohmic regions was removed by wet etching, which did not affect the I_R in this work. The length of the planar (L_{FP}),

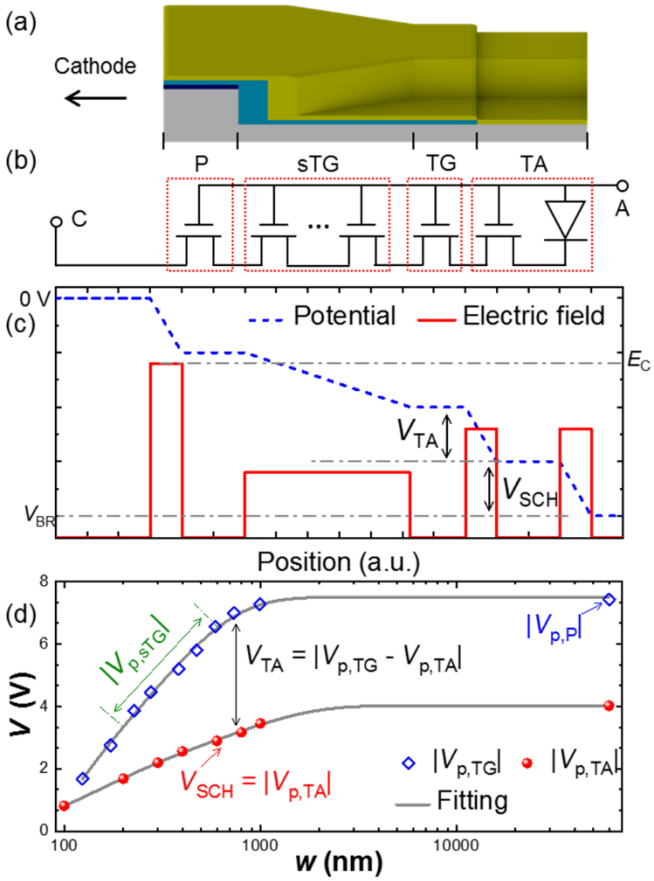

Figure 4.10: (a) Schematic and (b) equivalent circuit of the slanted tri-gate SBDs. (c) Schematic showing the distribution of potential and electric field at the 2DEG channel in the SBD under large reverse bias. (d) Averaged absolute value of the pinch-off voltage ($|V_p|$) as a function of the fin width (w_{fin}) in tri-gated AlGaN/GaN structures, determined from about eight devices of the each type fabricated on a control sample with 20 nm Al_2O_3 as the oxide. Published in Ref. [35].

slanted tri-gate (L_{sTG}), tri-gate (L_{TG}) and the tri-anode (L_{TA}) regions was 1.3 µm, 0.7 µm, 0.5 µm and 4 µm, respectively (Fig. 4.9). All current values in this work were normalized by the width of the device footprint (60 µm).

The schematic and equivalent circuit of the nanostructured anode are shown in Figs. 4.10(a) and (b), respectively. It consists of a tri-anode SBD connected in series with a tri-gate, a slanted tri-gate and a planar-gate transistors. The main idea is to design the distribution of potential along the device in OFF state, by engineering the profile of V_p with w in a single fabrication step, to obtain small I_R and high V_{BR}. More specifically, the purpose of each component can be briefly explained as follows:

(1) The tri-anode (TA) was designed for small V_{ON} [28], [47] and low I_R [34]. In ON state, the metal contacts the 2DEG directly at the sidewalls and hence leads to a small V_{ON}. In OFF state, when the voltage is below the V_p of the tri-anode ($V_{p,TA}$), the V_{SCH} is pinned at $|V_{p,TA}|$ (Fig. 4.10(c)), which fixes the I_R at a constant level. $|V_{p,TA}|$ can be reduced continuously with smaller w (Fig. 4.10(d)), resulting in a smaller V_{SCH} and hence in an exponentially lower I_R, as quantified in our previous study [33].

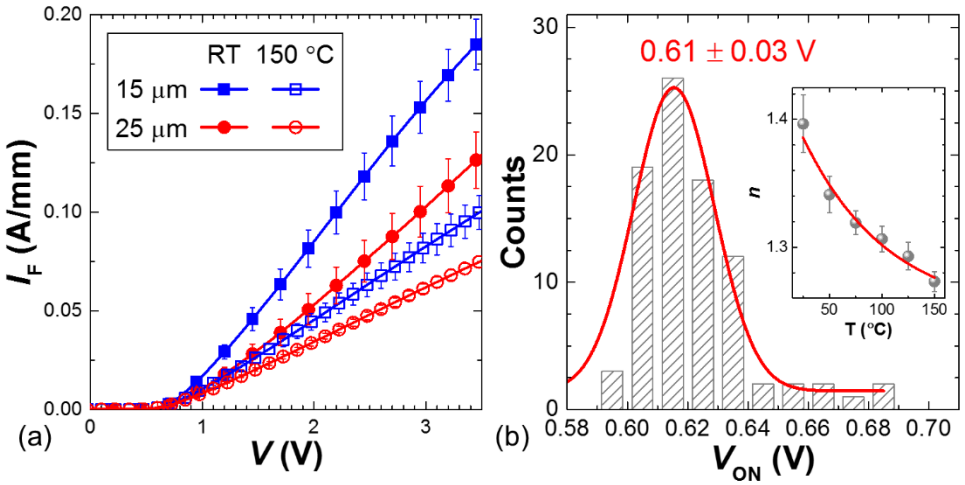

Figure 4.11: (a) Forward *I-V* characteristics and (b) distribution of V_{ON} of the slanted tri-gate SBDs. The inset shows the dependence of the estimated ideality factor (n) upon the temperature (T). Published in Ref. [35].

Therefore, here the I_R is controlled by V_{SCH}, instead of by the Φ_B, so it can be reduced without sacrificing the V_{ON}, which decouples the I_R and V_{ON} [33].

(2) The tri-gate region (TG) was inserted to shield the tri-anode, since the TA is vulnerable to high electric fields, which are concentrated at its cathode-side edge, and can lead to large I_R and even early breakdown of the device [33]. By connecting the TG in series with the TA, the voltage drop at the cathode-edge of the TA (V_{TA}) is pinned at $|V_{p,TG} - V_{p,TA}|$ (Fig. 4.10(c)), which can be also reduced with a smaller w_{fin} (Fig. 4.10(d)), when w_{fin} is below 1 µm, shielding the TA from large reverse biases. More details about the impact of the w on devices characteristics the can be found elsewhere [34].

(3) The slanted tri-gate (sTG) was included to enhance the V_{BR} [31]. It was patterned with a slanted w_{fin}, increasing towards the cathode. Since the $|V_p|$ in a tri-gate MOS structure reduces with smaller w_{fin} (Fig. 2(d)), the sTG works as many incrementally-stepped field plates (FPs)[16] with a continuous gradient of $|V_{p,sTG}|$ increasing towards the cathode. As a result, the electric field is spread along the entire sTG, which significantly improves the V_{BR} (Fig. 4.10(c)), similarly to conventional slanted FPs, but with the advantage of a much easier and more controllable fabrication by simply tuning the w_{fin} lithographically in a single step.

(4) The long planar region (P) works as a planar FP to further improve the V_{BR}, since the V_p of the planar region ($V_{p,P}$) is more negative with respect to the most negative value of the $V_{p,sTG}$ [32].

The slanted tri-gate SBDs presented very good ON-state performance as shown in Fig. 4.11(a), despite the partial removal of the 2DEG in the anode. The R_{ON} was 13.9 ± 1.3 Ω·mm and 22 ± 2.9 Ω·mm at room temperature for devices with L_{AC} of 15 µm and 25 µm, respectively, and increased to 27.6 ± 2.9 Ω·mm and 37 ± 1.8 Ω·mm at 150 ºC. The V_{ON} was as small as 0.61 ± 0.03 V (Fig. 4.11(b)),

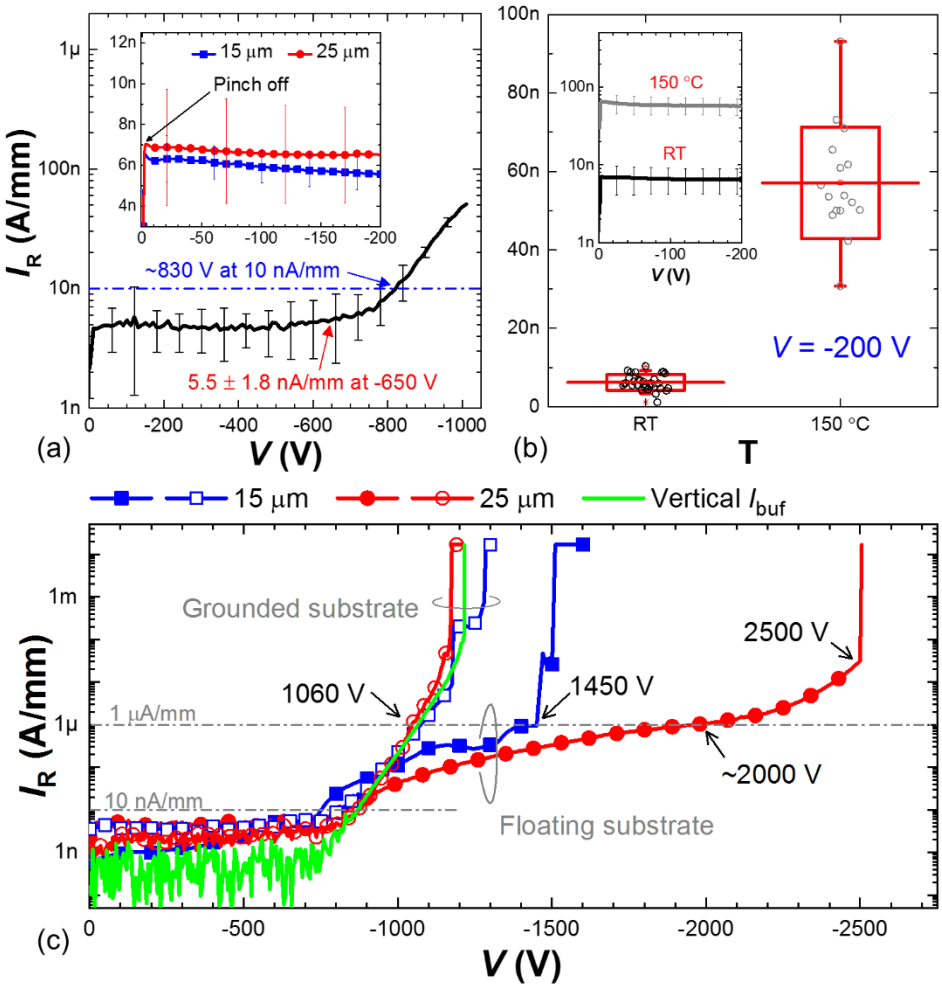

Figure 4.12: (a) Average I_R from ten devices measured at room-temperature (RT), which was independent on the substrate connection when V was below -900 V. (c) Breakdown characteristics of the slanted tri-gate SBDs. The inset in (a) shows the I_R with 15 µm and 25 µm of L_{AC} at RT. (d) I_R at RT and 150 ºC measured under a voltage of -200 V. The inset in (b) shows the reverse I-V characteristics at different temperatures. Published in Ref. [35].

determined at 1 mA/mm. The ideality factor (n) was 1.40 ± 0.02 at RT and reduced to 1.27 ± 0.01 at 150 ºC (inset in Fig. 4.11(b)), indicating the high quality of the sidewall Schottky contacts despite the etching.

In OFF state, the I_R of the slanted tri-gate SBDs was saturated after the pinch-off of the tri-anode at about -1.7 V (the inset in Fig. 4.12(a)) due to the fixed V_{SCH}, which was not affected by L_{AC}, and thus the I_R was nearly constant at 5.5 ± 1.8 nA/mm until -650 V, and did not reach 10 nA/mm until -830 V (Fig. 4.12(a)). Extremely low I_R of 51 ± 5.9 nA/mm was observed at -1000 V, which is significantly smaller than in any other reports of GaN-on-Si SBDs. For voltages below -900 V, there was no significant difference in I_R measured with floating and grounded substrates. From RT to 150 ºC, the I_R increased by only ~50 nA/mm (inset of Fig. 4.12(b)), and at 150 ºC, the I_R at -200 V was as small as 57 ± 13 nA/mm (the inset in Fig. 4.12(d)). This is the smallest I_R among reported lateral GaN SBDs at such high temperature.

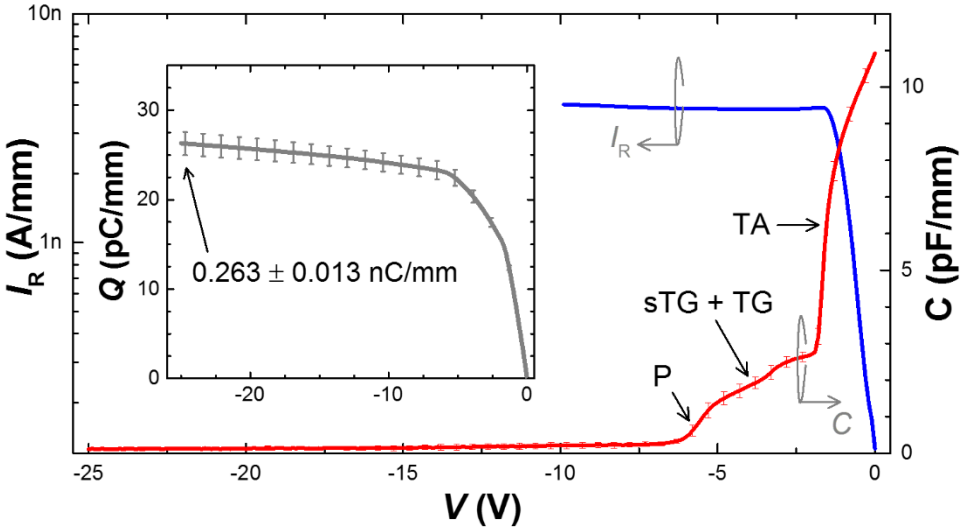

Figure 4.13: The capacitance-voltage (*C-V*) characteristics of the SBDs along with their I_R. The inset shows the cumulative charge (Q_C) of the devices. The *C-V* measurements were performed at 1 MHz at room temperature, with negligible hysteresis observed from double-sweep measurements. Published in Ref. [35].

In addition to their small V_{ON} and ultra-low I_R, the slanted tri-gate SBDs also presented high V_{BR} (Fig. 4.12(c)). With floating substrate, the V_{BR} at 1 µA/mm was -1450 V and -2000 V, and the hard breakdown was -1500 V and -2500 V for devices with L_{AC} of 15 µm and 25 µm, respectively, corresponding to a critical breakdown field of 1 MV/cm (estimated from the hard breakdown voltage versus L_{AC}). With grounded substrate, the V_{BR} at 1 µA/mm for both L_{AC} was about -1060 V, while the hard breakdown was up to -1200 V, which is comparable to current 650 V-rated GaN-on-Si power transistors [156]–[159] and is limited by the vertical breakdown of the buffer layers [160]. These results indicate that the 15 µm-L_{AC} SBDs can fulfill the voltage-blocking requirements of 600/650 V applications, even for those requiring grounded substrate connection, and the 25 µm-L_{AC} SBDs can be used for 1200 V applications (with floating substrate connection [160]), both providing a safety margin in breakdown of about 100 % (from the rated voltage to the hard breakdown).

Figure 4.13 shows the *C-V* measurement characteristics of the slanted tri-gate SBDs plotted along with the I_R. The slanted tri-gate SBDs presented ultra-low I_R, because their V_{SCH} was pinned and the I_R saturated at the pinch-off of the tri-anode, at about -1.7 V (Fig. 4.13), instead of increasing exponentially with the voltage. This decouples the I_R from the V_{ON}, allowing an independent design of the forward and reverse performance of the SBD, which is a major feature of this architecture. The high V_{BR} of the slanted tri-gate SBDs was due to the better-distributed electric field along the device. The continuity of the *C* in the slanted tri-gate region (sTG + TG region in Fig. 4.13(b)) indicates a gradual depletion of the channel with increasing reverse bias, due to the gradient of V_p, which spread effectively the electric field and greatly improved the V_{BR}. Such effect is similar to conventional slant FPs [115], [116], but obtained here with a more precise and controllable way of tuning the w_{fin} lithograph-

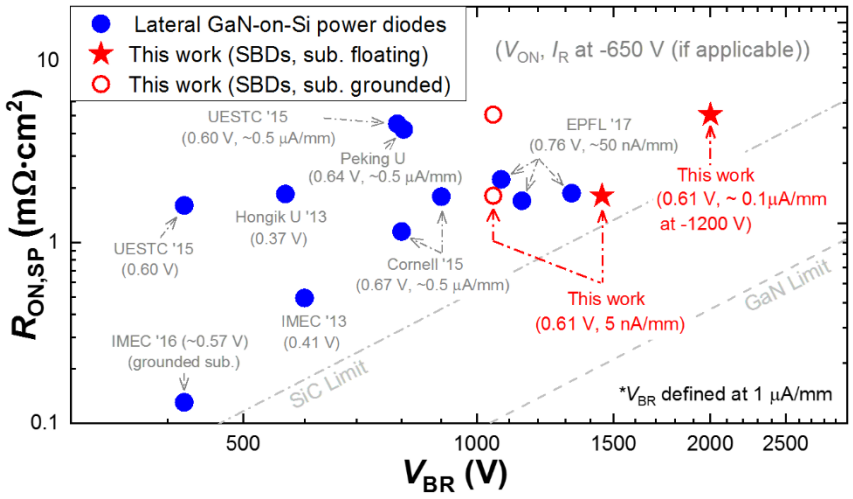

Figure 4.14: Specific on-resistance ($R_{ON,SP}$) versus V_{BR} benchmark of the slanted tri-gate SBDs against state-of-the-art lateral GaN-on-Si SBDs by defining the V_{BR} at I_R = 1 μA/mm. The V_{BR} for all reference devices was re-calculated based on the reported data following the definition of V_{BR} at I_R = 1 μA/mm. For fair comparison, devices with unspecified R_{ON} or I_R were not included. Published in Ref. [35].

ically, instead of the complex sloped etch of the FP oxide. The slanted tri-gate SBDs are also promising for fast switching, due to their small capacitive charge (Q_C) of 0.263 ± 0.13 nC/A (inset of Fig. 4.13), which is comparable to or below reported values for fast-switching GaN power SBDs on Si (0.415 nC/A) [161] and SiC (0.213 nC/A) [147] substrates. The switching time estimated from Q_C, was ~ 263 ps, which is about 25% shorter than that of conventional high-voltage GaN SBDs with double FPs [123].

The high performance of the slanted tri-gate SBDs makes them excellent power rectifiers (Fig. 4.14), presenting the highest V_{BR}, the lowest I_R of 5.5 ± 1.8 nA/mm at -650 V (or ~0.1 μA at -1200 V), a small V_{ON} of 0.61 ± 0.03 V, and an excellent high-power FOM up to 1.16 GW/cm^2, as compared with existing GaN-on-Si power diodes with conventional technologies, rendering a breakthrough for the family of GaN-on-Si power devices.

4.5 650 V reverse-blocking MOSHEMTs with slanted tri-gate Schottky drain

Lateral GaN-on-Si (MOS)HEMTs are very promising for power applications, yet their bi-directional conduction is not ideal in many topologies of power converters. To achieve high-voltage reverse-blocking (RB) capability, a power diode is added in series with the HEMT, which complicates the circuit design, increases the ON-resistance (R_{ON}) and parasitic elements, and degrades the efficiency of power conversion. HEMTs with integrated RB capability (RB-HEMTs) would therefore be highly desirable to address these issues, however, in the few reports on RB-HEMTs in the literature [162]–[168], the devices exhibited a relatively large V_{ON}, a significant increase in forward voltage (ΔV_F), a small V_{RB} as well as a large reverse leakage current (I_R), limited by the SBDs integrated in their drain electrodes.

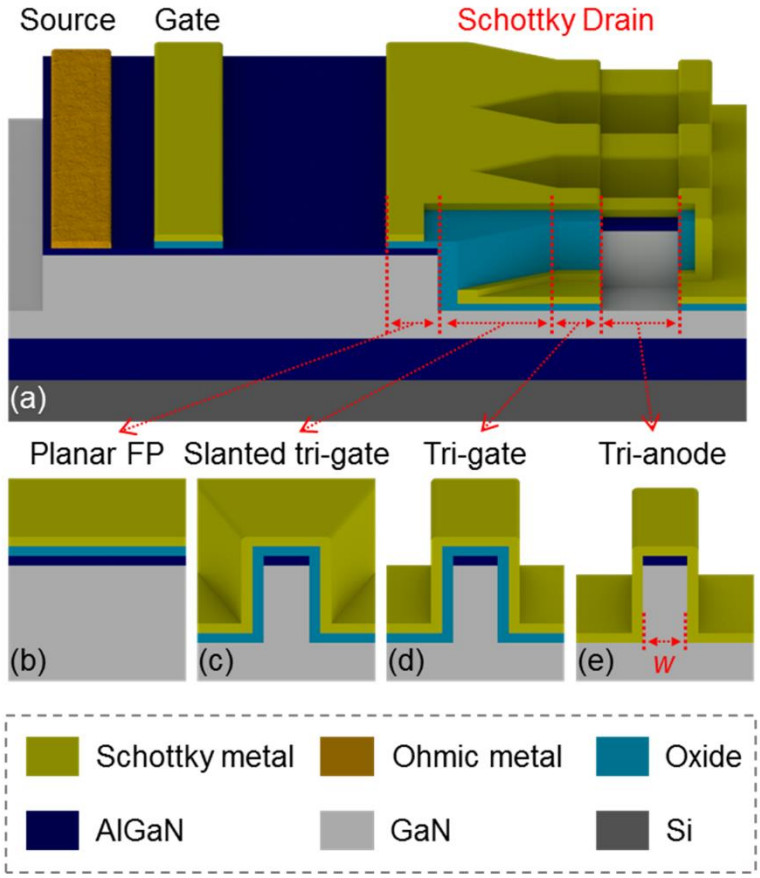

Figure 4.15: (a) Schematic of the MOSHEMTs with the slanted tri-gate Schottky drain. Cross-sectional schematics of the (b) planar FP, (c) slanted tri-gate (sTG), (d) tri-gate (TG) and (e) tri-anode (TA) regions. Published in Ref. [36].

Our proposed and demonstrated slanted tri-gate GaN SBDs have shown remarkable voltage-blocking performance, and paved the path for power GaN RB-HEMTs. In this section we extend this concept to demonstrate GaN-on-Si MOSHEMTs with state-of-the-art reverse-blocking performance, using a novel tri-anode Schottky drain integrated with slanted tri-gate FPs.

The devices with the tri-anode Schottky drain (tri-SCH) were fabricated on an AlGaN/GaN-on-silicon wafer, and their schematics are shown in Figs. 4.15(a)-(e). The fabrication process started with e-beam lithography to define the fins, which were then etched by inductively coupled plasma with a depth of ~180 nm. The w_{fin} and spacing in the tri-gate and tri-anode region were both 300 nm, while the w_{fin} in the slanted tri-gate region increased continuously from 300 nm to 600 nm towards the gate. The devices were isolated from each other by mesa etching with a depth of ~350 nm, followed by deposition and annealing of ohmic metals as source electrodes. A stack of 10 nm SiO_2 and 10 nm Al_2O_3 was deposited by atomic layer deposition as the gate dielectric, and then selectively removed in the tri-anode region. Finally the tri-anode and the gate were formed using Ni/Au, which was later used as the mask to remove the oxide in access/ohmic regions. The gate-to-source length (L_{GS}), gate length (L_G) and gate-to-drain length (L_{GD}) were 1.5 μm, 2.5 μm and 12.5 μm, respectively. The lengths

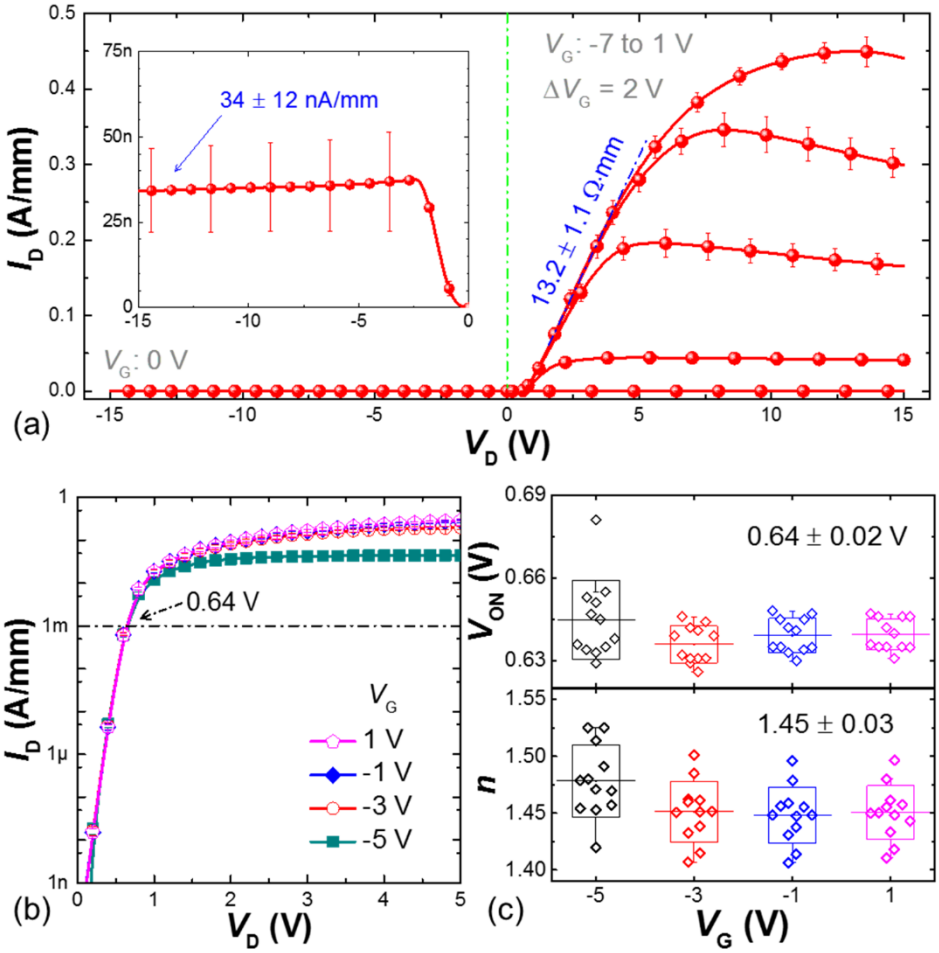

Figure 4.16: (a) Output characteristics of devices with the slanted tri-gate SCH drain (tri-SCH), in which the inset shows the I_R in the tri-SCH at V_G = 0 V, and (b) their turn-on characteristics. (c) Dependence of the V_{ON} and the ideality factor (n) on V_G. Published in Ref. [36].

for the planar FP (L_{FP}), slanted tri-gate (L_{sTG}), and tri-gate (L_{TG}) regions were 1.3 μm, 0.7 μm and 0.5 μm, respectively.

MOSHEMTs with the same dimensions but conventional ohmic (OHM) and planar Schottky drain (p-SCH) electrodes were also fabricated on the same chip as references. All devices shared the same dimensions as the tri-SCH except for the different drain electrodes. The ohmic drain was formed by alloying Ti/Al/Ti/Ni/Au, which was the same as the source electrode. The planar Schottky drain was the same as the tri-anode Schottky drain, however without the patterned features. All current values in this work, such as I_R and drain current (I_D), were normalized by the width of the device footprint, which was 60 μm. Twelve devices of each type were randomly chosen for the investigation, which defined the error bars presented in the results.

Figure 4.16(a) shows the output characteristics of the tri-SCH, presenting its excellent performance as a uni-directional switch. Under forward V_D, the differential R_{ON} and the maximum I_D were 13.2 ± 1.1 Ω·mm and 450 ± 17 mA/mm, respectively. Under reverse biases, the I_R was 34 ± 12 nA/mm at V_D = -15 V and V_G = 0 V. The V_{ON} was as small as 0.64 ± 0.02 V (Fig. 4.16(b)) at I_D = 1 mA/mm,

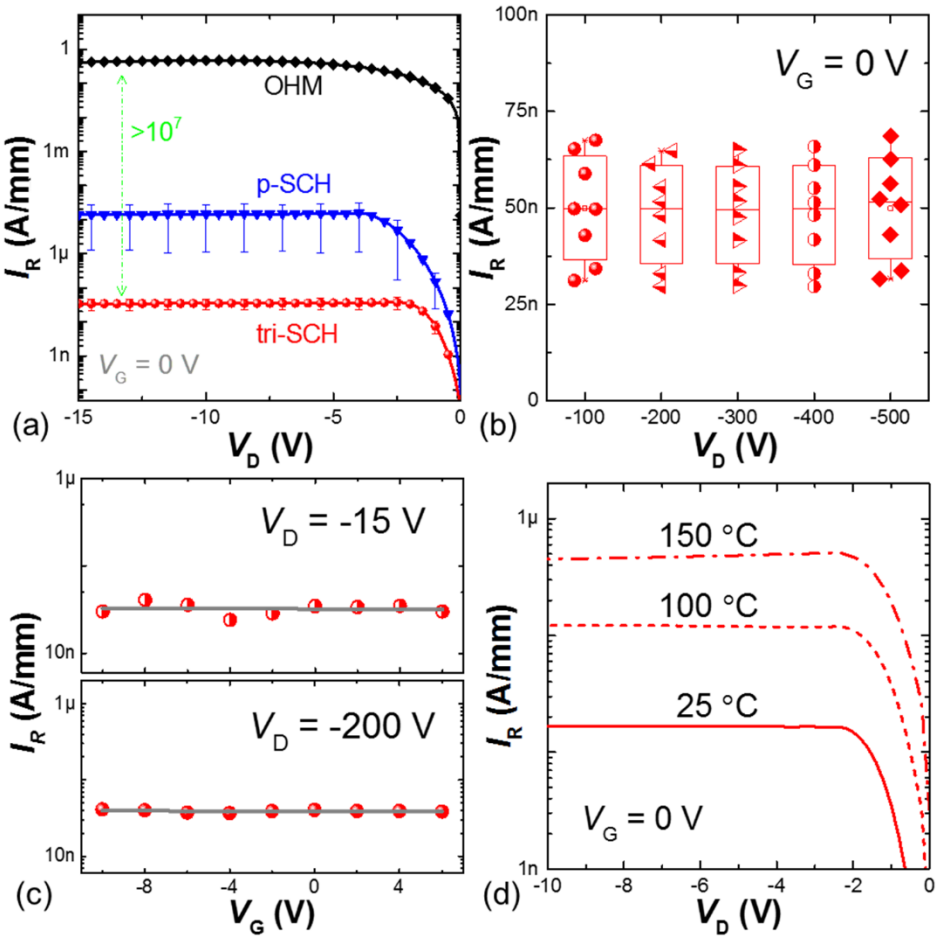

Figure 4.17: (a) Comparison of I_R in devices with ohmic (OHM), planar Schottky (p-SCH) and tri-anode Schottky (tri-SCH) drains. Dependence of the I_R on V_D (b) and V_G (c) in the tri-SCH. (d) Dependence of the I_R in tri-SCH on temperature. Published in Ref. [36].

due to the direct contact of the metal to the 2DEG at the sidewalls of the fins [28], [47]. The ideality factor (n) was 1.45 ± 0.03, indicating the high quality of the Schottky contact despite the etching. Figure 4.16(c) plots the V_{ON} and n at different V_G, revealing very little dependence on V_G.

The I_R in OHM, p-SCH and tri-SCH are compared in Fig. 4.17(a), all measured at V_G = 0 V. While the bi-directional nature of the OHM resulted in large reverse currents, reverse-blocking capability was achieved in p-SCH by replacing the ohmic drain with a planar Schottky drain. However, a large I_R was observed, similarly to other reports in the literature, leading to a small V_{RB} (defined at 0.1 µA/mm) of -0.9 V. This reveals the unsuitability of the planar Schottky drain for practical and efficient power applications. The I_R was dramatically reduced by over two orders of magnitude in tri-SCH. This is because the voltage drop at the Schottky junction (V_{SCH}) was pinned at a smaller value in the tri-anode, compared with the planar Schottky structure. As V_{SCH} was fixed and did not increase with the reverse bias, the I_R was constant even at high reverse biases (Fig. 4.17(b)), and was not affected by the V_G for a large range of voltages from -10 V to 6 V (Fig. 4.17(c)). Another improvement with the tri-anode Schottky drain was the better uniformity of the I_R. The variation of the I_R is about

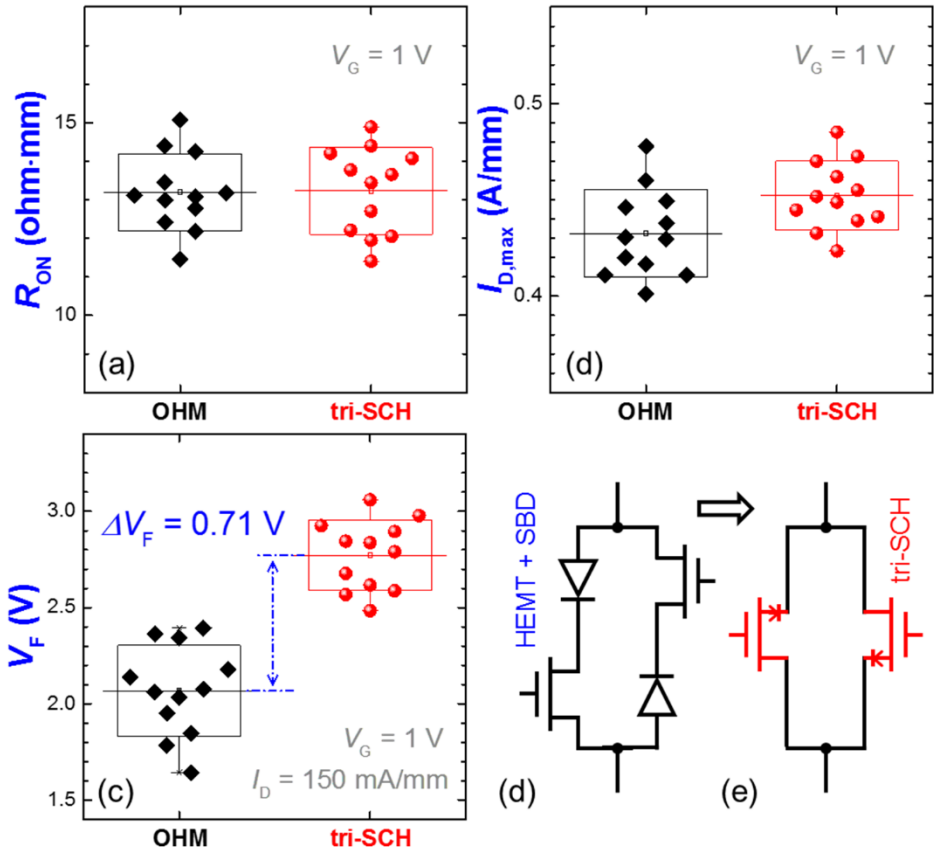

Figure 4.18: Comparison of the tri-SCH and OHM in (a) R_{ON}, (b) maximum I_D ($I_{D,max}$) and (c) forward voltage (V_F). Examples of bi-directional power switches using (d) a conventional scheme including two HEMTs and two SBDs and (e) a more advanced scheme using only two reverse-blocking transistors as demonstrated in this work (tri-SCH). Published in Ref. [36].

three orders of magnitude for the p-SCH, while less than 50 nA/mm for the tri-SCH. As shown in Fig. 4.17(d), the I_R of the tri-SCH was small and below 1 µA/mm at even 150 ºC, revealing the excellent value of this structure for high-temperature applications.

In addition to its excellent reverse blocking capability, the tri-anode Schottky drain did not degrade the ON-state characteristics of the transistors. The R_{ON} and I_D of the tri-SCH were about the same as those of the OHM (Figs. 4.18(a) and (b)). The forward voltage (V_F) for the tri-SCH and the OHM was 2.77 ± 0.17 V and 2.07 ± 0.17 V, respectively, extracted at I_D = 150 mA/mm, rendering a small ΔV_F of 0.7 V (Fig. 4.18(c)) which was very close to the V_{ON} of the tri-anode SBD. This is very important to improve the efficiency while reducing the size and complexity of power converters. For instance, the number of components in a bi-directional power switch can be reduced from four to two using the tri-SCH (Figs. 4.18(d) and (e)), and the resistive loss from the SBDs can be eliminated as the ΔV_F is so close to the V_{ON} and the R_{ON} of the tri-SCH is about the same as that of the OHM.

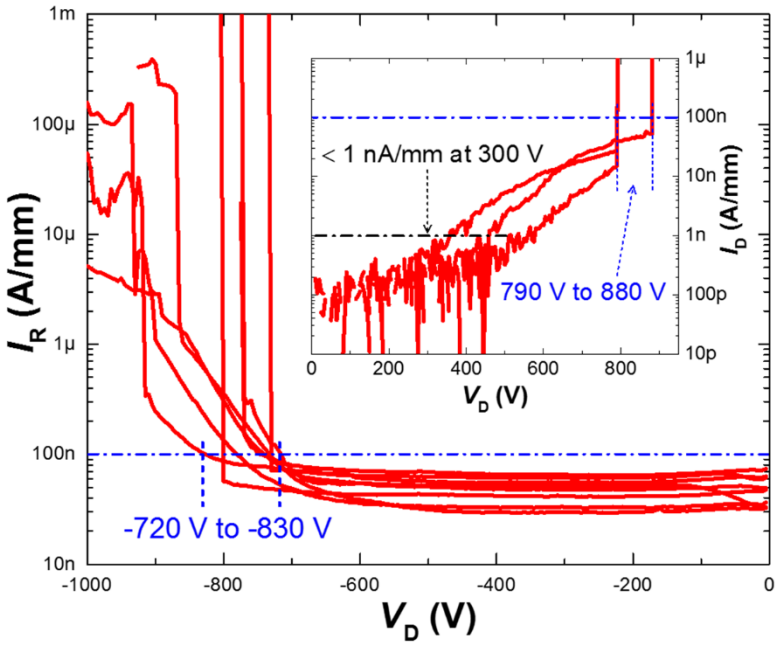

Figure 4.19: Room-temperature breakdown characteristics of the tri-SCH, measured with grounded substrate. The V_G for measuring the V_{RB} and V_B was 0 V and -10 V, respectively. Published in Ref. [36].

Figure 4.19 shows the breakdown characteristics of the tri-SCH under both forward and reverse drain voltages. The breakdown voltage in this work was defined at a leakage current of 0.1 μA/mm with the Si substrate grounded. The reverse breakdown voltage (V_{RB}) varied from -720 V to -830 V under V_G = 0 V, along with a consistently small I_R of 65 ± 11 nA/mm at -700 V. The forward breakdown voltage (V_B) varied from 790 V to 880 V (the inset of Fig. 4.19), which was measured under a V_G of -10 V.

Table 4.1: Comparison of the tri-SCH in this work with other reverse-blocking GaN (MOS)HEMTs in the literature. [a]Substrate connection was not reported. [b]Results were obtained from simulation. Published in Ref. [36].

	sub.	V_{RB}	I_R (μA/mm)	V_{ON} (V)	ΔV_F (V)
This work	Si	-759 ± 37 V at 0.1 μA/mm (grounded sub.)	0.065 ± 0.011 at -700 V (grounded sub.)	0.64	0.7
[166]	Si	-200 V at 1 mA/mm (grounded sub.)	≥ 10 at -75 V (floating sub.)	0.55	1.25
[164]	SiC	-110 V at 10 mA/mm	≥ 1000 at -20 V	--	--
[168]	Si	-685 V at hard breakdown[a]	~ 6 at -100 V[a]	0.4	--
[165]	Al_2O_3	-49 V at 1 mA/mm	> 100 at -25 V	1.7	≥ 2
[167]	Si	--	~0.4 at -20 V (floating sub.)	1.91	--
[162]	Si	-650 V at ~0.15 mA/mm[a]	--	1.5	--
[163]	Si	-900 V at 1 μA/mm[b]	~0.25 μA/mm at -700 V[b]	0.38	--

The tri-SCH was compared with other reverse-blocking GaN transistors in the literature in Tab. 1. The tri-SCH presented the highest V_{RB}, the lowest I_R and the smallest ΔV_F, despite the grounded substrate

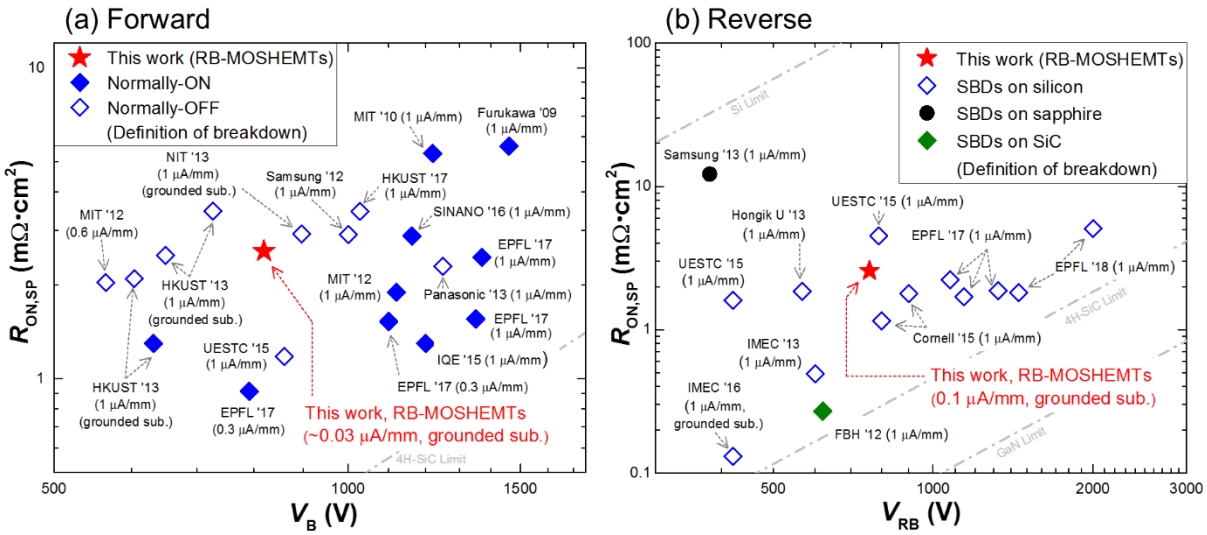

Figure 4.20: $R_{ON,SP}$ versus breakdown voltage benchmarks of (a) the forward characteristics of the tri-SCH (RB-MOSHEMTs) against discrete lateral GaN-on-silicon power (MOS)HEMTs and (b) their reverse characteristics against discrete lateral GaN SBDs on various substrates. The breakdown voltage for all reference devices was re-calculated based on the reported data following the definition of V_B at $I_{OFF} \leq 1$ μA/mm. For fair comparison, literature results with un-specified R_{ON} or I_R were not included. Published in Ref. [36].

and the much stricter definition of V_{RB} in this work, along with a small V_{ON} comparable to the state-of-the-art results.

The forward and reverse characteristics of the tri-SCH were further benchmarked against state-of-the-art discrete lateral GaN-on-Si power (MOS)HEMTs and SBDs in Fig. 4.20, respectively. For calculation of the figure-of-merit (FOM) in this work, average R_{ON} (13.2 ± 1.1 Ω·mm), V_{RB} (-759 ± 37 V at 0.1 μA/mm) and V_B (820 ± 42 V at 0.1 μA/mm) were adopted, along with a total transfer length of 3 μm, accounting for both source and drain contacts. The tri-SCH presented high V_B and V_{RB}, comparable to state-of-the-art discrete devices measured with grounded substrates, but at a much smaller current, revealing its excellent performance as uni-directional power switches. More importantly, these high blocking voltages under both forward and reverse biases were achieved in a single integrated device, instead of using a discrete transistor in series with an SBD, which can greatly simplify the circuit design, reduce its size, resistance and parasitic components, and improve the efficiency of power converters.

4.6 Conclusion

In this chapter we presented high-voltage and low-leakage GaN-on-Si SBDs using a hybrid of tri-gate and tri-anode structures and revealed the designing principle of FPs for low leakage current in lateral GaN SBDs. In addition, we demonstrated novel slanted tri-gate GaN-on-Si SBDs with unprecedented voltage-blocking capability (2 kV at 1 μA/mm), along with state-of-the-art reverse-blocking

GaN-on-Si power transistors with slanted tri-gate Schottky drain electrodes, unleashing the tremendous potential of tri-gate technologies for high-performance GaN power SBD.

Chapter 5 Multi-channel tri-gate technologies for ultra-low on-resistance

5.1 Introduction

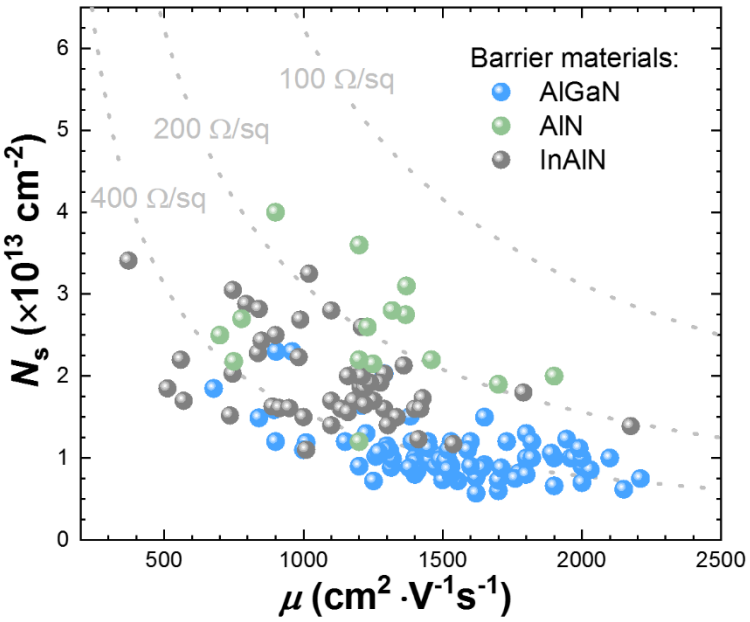

Figure 5.1: Transport characteristics of the 2DEG in GaN heterostructures with different barrier materials.

The exceptional properties of GaN heterostructures have led to the development of AlGaN/GaN HEMTs, demonstrating outstanding value for high-voltage applications. Nevertheless, the performance of current GaN (MOS)HEMTs is still far below the prospect promised by this material. Further improvements require a significant reduction in R_{ON}, increase in V_{BR}, while maintaining fast switching at high switching frequencies.

Among these factors, R_{ON} is intrinsically determined by the electric conductivity of the 2DEG channel at the AlGaN/GaN interface, given by the product of its sheet carrier concentration (N_s) and mobility (μ). In typical AlGaN/GaN heterosturctures, the Al composition and thickness of the AlGaN barrier layer are about 25% - 30% and 20 nm, respectively, resulting in a sheet resistance (R_s) of 300 - 400 ohm/sq (Fig. 5.1). High-Al-content barrier materials have been intensively explored to increase the N_s, which however results in a reduced μ (Fig. 5.1) in addition to a more challenging epitaxial growth. Moreover, the increased N_s yields a more negative V_{TH} and makes it much more difficult to achieve normally-off operation.

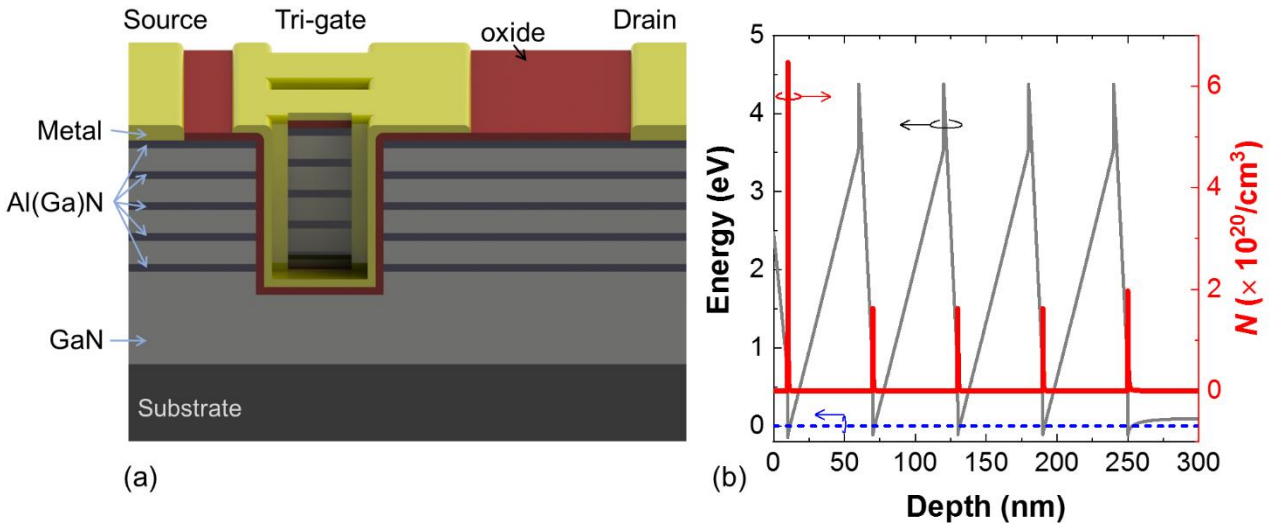

Figure 5.2: (a) Schematic of proposed multi-channel tri-gate GaN MOSHEMT and (b) simulated energy band structure of a multi-channel AlGaN/GaN heterostructure showing five parallel 2DEG channels.

Another way to reduce the R_s is to use a multi-channel structure [169]–[182], which contains multiple 2DEG channels and the R_s can be decreased by increasing the number of channels (N_{ch}), resulting in much better channel conductivity over conventional single-channel structures. Up to date, an ultra small R_s down to 37 Ω/sq has been achieved in Ref. [170] based on n a 9x-channel AlN/GaN structure grown molecular beam epitaxy (MBE), along with high N_s of 1.08×10^{14} /cm^2 and high hall mobility (μ_{Hall}) of 1567 cm^2/V·s. This renders a reduction of about 10 times in R_s as compared to conventional AlGaN/GaN single-channel structures, which is extremely promising for the reduction of R_{ON} surpass the limit of GaN materials capabilities. However, such highly conductive multi-channel structures ($R_s \leq 100$ Ω/sq) are not electrostatistically controllable by conventional planar gates, making their high conductivity less useful.

To address these challenges, we present a novel multi-channel tri-gate technology (Fig. 5.2). This unique architecture offers smaller R_{ON} due to the large N_s and high μ in the multi-channels and superior gate control with 3-dimensional tri-gate structure, integrating multiple parallel devices in a given footprint for enhanced performance and reduce substrate cost. We demonstrate this concept in high-voltage normally-on/off GaN-on-Si MOSHEMTs with a significant reduction in R_{ON} and enhancement of $g_{m,max}$. We also demonstrate multi-channel tri-gate GaN-on-Si power SBDs with small R_{ON} and forward voltage (V_F), due to the multiple 2DEG channels, and large V_{BR} and ultra-low I_R, thanks to the tri-gate, showing state-of-the-art performance for 600 V/650 V ratings. In addition to these excellent results, we will further reveal the remarkable prospects of the multi-channel tri-gate technology using ultra-conductive multi-channel structure, which greatly reduced the R_{ON} of the MOSHEMTs by 6x and increased the I_D by 4x.

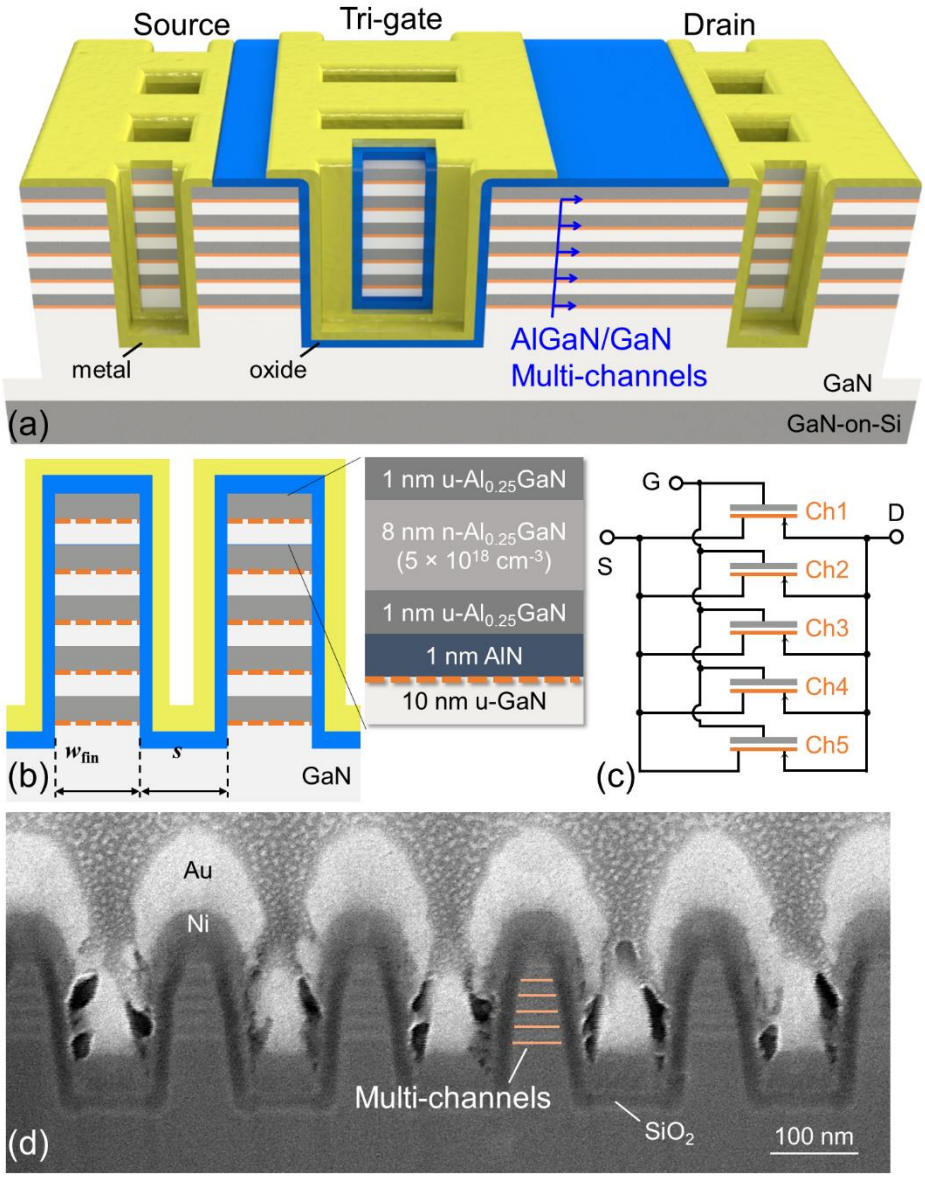

Figure 5.3: (a) Schematic of the multi-channel tri-gate AlGaN/GaN MOSHEMT. (b) Cross-sectional schematic of the tri-gate region. The inset shows the heterostructure forming each of the multi-channels. (c) An equivalent circuit of the multi-channel tri-gate MOSHEMT, integrating multiple parallel transistors in a given device footprint for enhanced performance and reduced substrate cost. (d) A cross-sectional SEM image of the tri-gate region, tilted by 52º. Published in Ref. [38].

5.2 High-voltage normally-on/off multi-channel tri-gate GaN MOSHEMTs

In this section we present multi-channel tri-gate AlGaN/GaN transistors (Fig. 5.3(a)) for high-voltage applications. A heterostructure with multiple AlGaN/GaN layers was used to form five parallel two-dimensional-electron-gas (2DEG) channels to reduce the ON-resistance (R_{ON}) (Figs. 5.3(b) and (c)). Tri-gate electrodes were deployed to control the multiple channels (Figs. 5.4(b) and (d)), and their geometry was optimized for channel control and device performance. With a fin width (w_{fin}) of 100 nm, normally-on multi-channel tri-gate transistors presented 3x-higher maximum drain current ($I_{D,max}$), 47%-smaller R_{ON}, as well as 79%-higher maximum transconductance ($g_{m,max}$), as compared

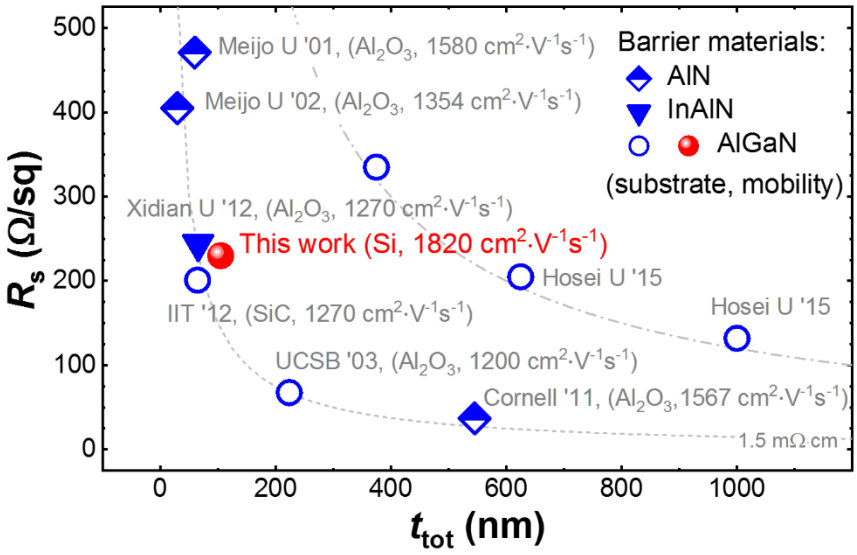

Figure 5.4: Comparison of multi-channel structures in this work with literature results. The t_{tot} refers to the total thickness of the multi-channel structure. For a fair comparison, multi-channel structures with unspecified R_s were not included. Published in Ref. [38].

to counterpart single-channel devices. Using the channel depletion through the tri-gate sidewalls, normally-off operation was also achieved by reducing w below the sidewall depletion width, resulting in a positive threshold voltage (V_{TH}) of 0.82 V at 1 µA/mm. The devices presented a high breakdown voltage (V_{BR}) of 715 V, which reveal a promising platform for high-voltage GaN transistors.

The multi-channel AlGaN/GaN-on-Si heterostructure in this work consisted of 5 parallel 2DEG channels, formed by 10 nm-thick AlGaN barrier, 1 nm-thick AlN spacer and 10 nm-thick GaN channel layers. The barrier layer was partially doped with Si at 5×10^{18} cm^{-3} (Fig. 5.3(b)). Hall measurements revealed small R_s of 230 Ω/sq, N_s of 1.5×10^{13} cm^{-2}, and μ_{Hall} of 1820 $cm^2 \cdot V^{-1}s^{-1}$. A small effective resistivity (ρ_{eff}) of 2.4 mΩ·cm was obtained, comparable to other literature results, but with a smaller total thickness t_{tot} and higher μ (Fig. 5.4). Small ρ_{eff} and high μ_{Hall} are crucial to reduce R_{ON}, and a thin t_{tot} facilitates electrostatic gate control and device fabrication. The tri-gate region was patterned into fins with different w_{fin}, spacings (s), and lengths (l_{fin}), with a fixed height of 200 nm, covered with 25 nm of SiO_2 and Ni/Au. Ohmic regions were patterned with w_{fin} and s of 500 nm to contact the multi-channels. The standard deviation was determined from at least 12 devices of each type.

Tri-gates are uniquely suited to control the multi-channels. To illustrate this, we fabricated multi-channel tri-gate transistors with different w but with a long fixed l_{fin} of 50 µm, which diminishes the impact from access and ohmic regions on the extracted device characteristics. Here the I_D and g_m were normalized by the total width of the long fins, which in this case dominate the device characteristics. More details about these devices can be found in the caption of Fig. 5.5 as well as Tab. 5.1. The MOS channels at trenches were not considered since the measurements were conducted with V_G

below the V_{TH} of the MOS channel, which was ~2 V for our oxides and fabrication process [28], and the conductivity of the MOS channel is much smaller than that of the 2DEG channels [28].

Table 5.1: Tri-gate geometry and device characteristics for the 50 μm-long multi-channel tri-gate transistors presented. The N_s here was normalized by the top surface area of the fins. Published in Ref. [38].

w_{fin} (nm)	s (nm)	FF (%)	l (μm)	Number of fins	Total width of fins (μm)	V_{TH} @ I_D = 1 μA/mm (V)	SS @V_D = 0.5 V (mV/dec)	$g_{m,max}$ @V_D = 0.5 V (μS)	R_{ON} @ V_G = 2 V (Ω)	C_G @ V_G = 2 V (pF)	Q @ V_G = 2 V (pC)	N_s @ V_G = 0 V (10^{13} cm^{-2})
40	160	20	50	300	12	-0.08 ± 0.04	101 ± 12	354 ± 43	1212 ± 134	17.2 ± 0.23	20.3 ± 0.6	0.05 ± 0.01
50	150	25	50	300	15	-0.42 ± 0.04	93.7 ± 10	408 ± 40	929 ± 60	16.7 ± 1.2	22.2 ± 1.8	0.12 ± 0.02
60	140	30	50	300	18	-0.78 ± 0.04	90.0 ± 11	443 ± 16	769 ± 47	16.6 ± 0.84	24.6 ± 1.7	0.19 ± 0.02
70	130	35	50	300	21	-1.14 ± 0.05	89.4 ± 5.3	442 ± 27	664 ± 19	15.9 ± 1.1	26.5 ± 1.5	0.27 ± 0.03
100	100	50	50	300	30	-2.37 ± 0.09	86.0 ± 9.2	430 ± 41	487 ± 13	13.4 ± 0.69	32.0 ± 1.3	0.45 ± 0.02
150	150	50	50	200	30	-4.28 ± 0.14	94.5 ± 7.6	301 ± 33	487 ± 8.4	13.4 ± 0.32	32.9 ± 0.7	0.58 ± 0.01
200	200	50	50	150	30	-6.08 ± 0.12	106 ± 19	264 ± 24	486 ± 11	12.2 ± 0.18	32.7 ± 0.4	0.66 ± 0.01
250	250	50	50	120	30	-7.52 ± 0.15	106 ± 9.1	200 ± 25	489 ± 8.2	11.1 ± 0.59	32.4 ± 0.6	0.72 ± 0.01
300	300	50	50	100	30	-8.69 ± 0.14	109 ± 14	153 ± 15	499 ± 21	10.6 ± 0.28	32.2 ± 0.9	0.75 ± 0.01
400	400	50	50	75	30	-10.5 ± 0.13	111 ± 19	130 ± 12	483 ± 8.1	9.59 ± 0.34	31.8 ± 0.7	0.81 ± 0.01
500	500	50	50	60	30	-11.7 ± 0.18	102 ± 11	116 ± 9.6	473 ± 13	9.03 ± 0.48	32.0 ± 0.6	0.85 ± 0.01
600	600	50	50	50	30	-12.7 ± 0.17	118 ± 15	107 ± 11	470 ± 7.3	8.76 ± 0.33	32.0 ± 0.9	0.87 ± 0.01
750	750	50	50	40	30	-13.8 ± 0.13	119 ± 17	99.3 ± 7.5	463 ± 15	8.48 ± 0.15	32.3 ± 0.6	0.90 ± 0.01
1000	1000	50	50	30	30	-14.9 ± 0.20	125 ± 15	92.2 ± 5.8	449 ± 8.6	7.78 ± 0.66	32.2 ± 0.6	0.93 ± 0.01
2500	2500	50	50	12	30	-17.5 ± 0.24	149 ± 14	85.1 ± 8.1	430 ± 11	6.84 ± 0.80	32.9 ± 0.6	1.01 ± 0.01
Planar	0	100	51	1	60	-22.3 ± 0.20	167 ± 16	81.3 ± 2.0	239 ± 26	6.06 ± 0.12	67.8 ± 0.6	1.14 ± 0.01

Figure 5.5(a) shows the impact of reducing w_{fin} on the transfer characteristics of the devices. Conventional planar gates are not suited to electrostatically control the multi-channel structure, which is indicated by their large V_{TH} of -22.3 ± 0.2 V (at 1 μA/mm), poor subthreshold swing (SS) of 167 ± 16 mV/dec, and small $g_{m,max}$ of 1.63 ± 0.04 mS/mm. The large $|V_{TH}|$ is caused by the large gate-to-channel distance and the screening effect that shields a lower channel from the gate control unless its upper channel is depleted. The small $g_{m,max}$ and the large SS indicate that control of the multi-channels is not simultaneous. The tri-gate addresses this issue by providing additional electrostatic control from its sidewall portions, which can be enhanced by reducing w_{fin}, leading to much improved V_{TH} and SS (Fig. 5.5(b)). At w_{fin} of 40 nm, the channel control is dominated by the sidewalls over the top gate,

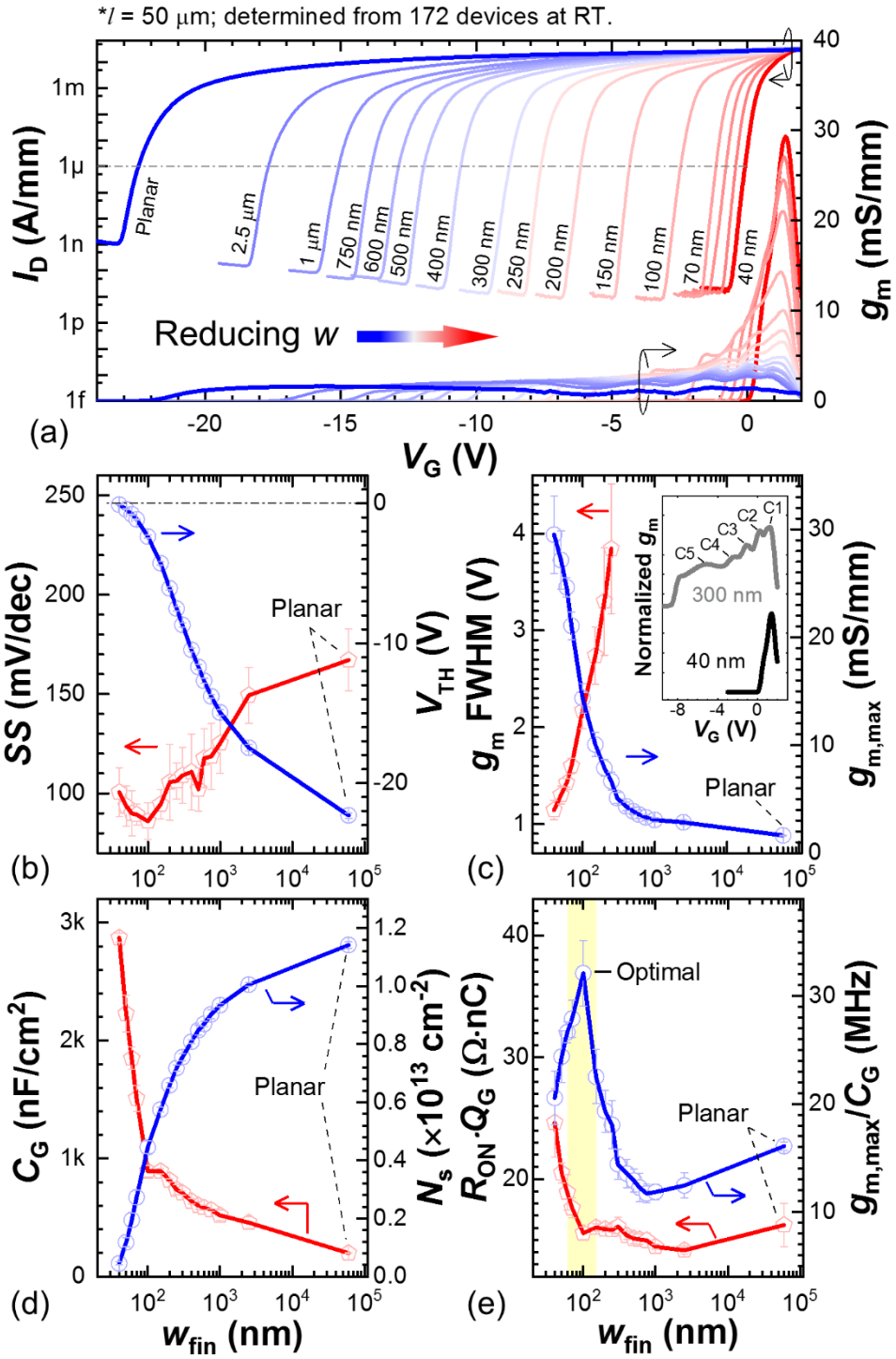

Figure 5.5: (a) Transfer characteristics of multi-channel tri-gate MOSHEMTs with different w_{fin} from 60 μm (planar) to 40 nm, measured at V_D = 0.5 V. Width dependence of (b) *SS* and V_{th} (at 1 μA/mm), (c) $g_{m,max}$ and g_m FWHM, (d) C_G and N_s, and (e) R_{ON}·Q_G (Q_G refers to gate charge) and $g_{m,max}/C_G$ values. The inset in (c) shows normalized g_m-V_G plots of devices with w_{fin} of 40 nm and 300 nm. The R_{ON}, C_G and Q_G was extracted at V_G = 2 V, N_s was extracted at V_G = 0 V, and the $g_{m,max}$ was the maximum value of the g_m-V_G characteristics, regardless of the several g_m peaks in transistors with w > 200 nm. The C_G and N_s were normalized by the top surface area of the fins. The length of the gate electrode here (L_G) was 51 μm, covering the fins and extending 0.5 μm towards the source and drain side. The gate-to-source (L_{GS}) and gate-to-drain (L_{GD}) lengths were 1.5 μm. Published in Ref. [38].

resulting in small V_{TH} of -0.08 ± 0.03 V and improved *SS* of 100 ± 12 mV/dec. The multi-channels are also modulated simultaneously by the tri-gate, as revealed by the g_m-V_G characteristics (Fig.

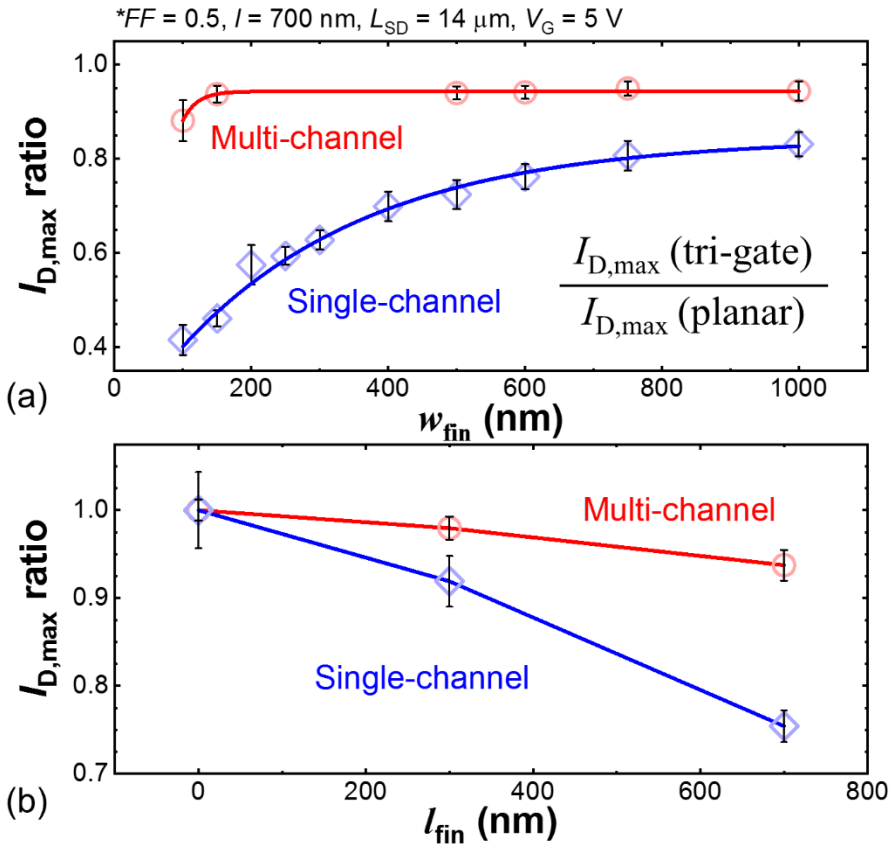

Figure 5.6: Dependence of $I_{D,max}$ on (a) w_{fin} and (b) l_{fin} in single- and multi-channel tri-gate MOSHEMTs, all measured at V_G = 5 V and normalized by the width of device footprint. These devices had different w_{fin} in their tri-gate regions, while sharing the same *FF* of 0.5 and l_{fin} of 700 nm. The distance between source and drain electrodes (L_{SD}) was 14 μm. Published in Ref. [38].

5.5(c)). In transistors with planar gates or wide tri-gates (w_{fin} > 200 nm), the g_m shows clearly five separate peaks, caused by the successive turn on of each of the five channels (inset in Fig. 5.5(c)). By reducing w_{fin}, these peaks merge and their full width at half maximum (FWHM) is reduced, forming finally a single sharp peak at w_{fin} of 40 nm with high $g_{m,max}$ of 29.5 ± 3.6 mS/mm. This is because the V_{TH} of each parallel channel is mainly determined by the sidewall control, thus all channels turn on simultaneously. The enhanced electrostatic control is due to the increased gate capacitance (C_G) and reduced N_s with narrowing tri-gates (Fig. 5.5(d)). Such increase in C_G does not necessarily degrade the transistor frequency performance. An optimized w_{fin} of 100 nm for multi-channel tri-gate devices led to similar R_{ON}·Q_G product (15.6 ± 0.05 Ω·nC) and twice the $g_{m,max}/C_G$ value (32.1 ± 0.3 MHz) as compared with planar-gate devices (16.2 ± 1.77 Ω·nC and 16.1 ± 0.04 MHz), suggesting an enhanced frequency performance (Fig. 5.5(e)).

While tri-gates are uniquely adapted to control the multi-channels, the multi-channel structure is exceptionally suited to address the degraded $I_{D,max}$ caused by the tri-gate. As shown in Fig. 5.6(a), $I_{D,max}$ was greatly reduced by 17% in single-channel devices even at large w_{fin} of 1 μm, and such reduction further increased to 41% as w_{fin} was reduced to 100 nm. In contrast, the $I_{D,max}$ in multi-channel devices

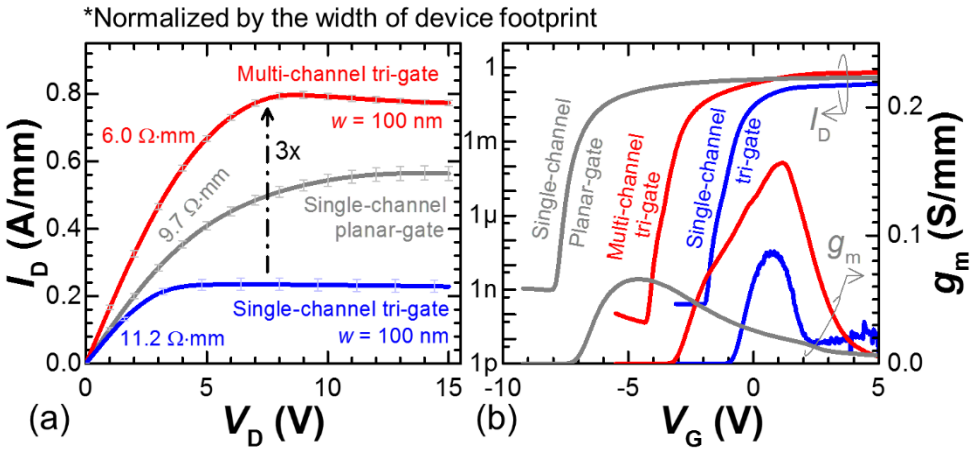

Figure 5.7: (a) Output characteristics at V_G = 5 V and (b) transfer characteristics at V_D = 5 V of the transistors, normalized by the width of device footprint. The w_{fin} and *FF* in single-channel tri-gate and multi-channel tri-gate transistors are 100 nm and 50 %, respectively. Published in Ref. [38].

reduced only by 6% at w_{fin} of 1 μm, and remained constant until w of 150 nm. At w_{fin} of 100 nm, the reduction in the $I_{D,max}$ in multi-channel devices was as small as 12%, much smaller than in single-channel devices. This is because the multi-channel structure mitigates greatly the electron-electron and sidewall scatterings in tri-gate (MOS)HEMTs. In single-channel devices, electrons populate only one channel, resulting a high electron density. In addition to a more pronounced electron-electron scattering, this reduces the effective distance between electrons and sidewalls, causing more sidewall scattering, hence $I_{D,max}$ degrades rapidly with narrower fins. The multi-channel structure addresses this issue by better distributing electrons in multiple parallel channels, instead of only one, reducing the carrier density per channel and the effective distance between electrons and sidewalls, and thus mitigating the degradation and width-dependence of $I_{D,max}$. This explanation is further supported by the dependence of $I_{D,max}$ on l_{fin} (Fig. 5.6(b)). Single-channel devices presented much larger and quicker degradation in $I_{D,max}$ as l_{fin} was increased, than in multi-channel devices, indicating the higher electron velocity in multi-channel devices due to the reduced scattering.

Based on these optimizations, we designed multi-channel tri-gate GaN MOSHEMTs for high voltage applications. The L_{GD} was 10 μm to sustain high voltages, and l_{fin} was 700 nm to decrease the area of etched regions on the 2DEG and reduce R_{ON}. The fins were 100 nm-wide, along with s of 100 nm and *FF* of 50%. The gate metal was 2.5 μm long, covering all the fins, and extended 0.5 μm and 1.3 μm towards the source and drain electrodes, respectively. Single-channel planar-gate and tri-gate GaN MOSHEMTs with similar dimensions were taken as the reference, based on a 20 nm-thick $Al_{0.25}GaN$ barrier layer, which is a typical structure used for GaN power transistors.

The multi-channel tri-gate transistors presented significantly enhanced performance as compared with conventional single-channel tri-gate transistors. As shown in Fig. 5.7(a), the multi-channel tri-

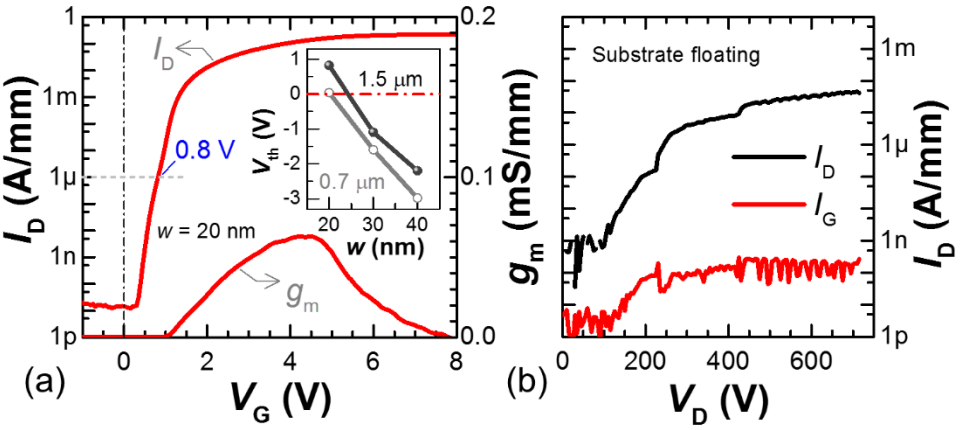

Figure 5.8: (a) Transfer characteristics of multi-channel tri-gate transistors with w_{fin} of 20 nm and *FF* of 10 %. (b) OFF-state breakdown characteristics of the multi-channel tri-gate transistors measured with floating substrate. The inset in (a) shows the dependence of V_{TH} (at 1 μA/mm) in multi-channel tri-gate transistors on w_{fin} and l_{fin}. Published in Ref. [38].

gate architecture reduced the R_{ON} from 11.2 Ω·mm to 6.0 Ω·mm, and greatly increased the $I_{D,max}$ by more than 3.1-fold, from 252 mA/mm to 797 mA/mm (all these measurements for both kinds of devices were normalized by the width of device footprint (60 μm)). These results are remarkable since they indicate that the multi-channel tri-gate technology can lower the conduction losses of the transistor for a given device footprint, or equivalently, deliver a given current rating in a smaller device footprint, both of which are highly beneficial for efficient power transistors.

In addition, the multi-channel tri-gate architecture also addresses the degradation in ON-state performance in single-channel tri-gate transistors (Fig. 5.7(a)), such as the large R_{ON} and significantly diminished $I_{D,max}$ as compared to planar-gate transistors, which is mainly due to narrower effective channels, strain relaxation, and additional spreading resistance. The multi-channel tri-gate architecture overcomes these issues thanks to the highly conductive parallel multi-channels with fewer carriers per channel. Compared with single-channel planar-gate transistors, R_{ON} was reduced by 38% and $I_{D,max}$ was increased by 41% in the multi-channel tri-gate transistor, despite the 50% reduction in effective channel width (*FF* = 50%).

The multi-channel tri-gate improves not only the output characteristics but also the transfer characteristics of the devices (Fig. 5.7(b)). Compared to single-channel planar-gate devices, the V_{TH} in the normally-on transistor was reduced from -7.6 V to -3.6 V, and $g_{m,max}$ was enhanced by 2.4-fold, from 66.1 mS/mm to 156.6 mS/mm in the multi-channel tri-gate devices. The ON-state drain current (I_{ON}) was increased and the OFF-state (I_{OFF}) was suppressed, resulting in a higher on/off ratio over 10^{10}.

The multi-channel tri-gate architecture also provides a promising platform to achieve normally-off operation (Fig. 5.8(a)). While typical methods developed for normally-off single-channel GaN transistors such as gate recess [155] or p-GaN [183] may not deplete all embedded channels, the tri-gate

offers a unique opportunity to use sidewall-depletion effect to deplete the multi-channels and achieve normally-off operation. The sidewall-depletion effect originates from surfaces states at fin sidewalls, the large work function of the gate metals, and the elastic deformation of the fins that causes more strain relaxation in the AlGaN/GaN heterostructure near the sidewalls, depleting the 2DEG in a certain width from the two sidewalls towards the center of the fin. When w is equal to or smaller than the sidewall-depletion width (w_{dep}), 2DEG in the multi-channel fins will be depleted and normally-off operation can thus be achieved. As shown in Fig. 5.8(b), by reducing w to 20 nm (s = 180 nm), the 2DEG in the multi-channel fins was depleted and a positive V_{TH} of was achieved 0.82 V at 1 μA/mm, along with I_{OFF} of only 12 pA/mm at V_G = 0 V, indicating excellent normally-off behavior. In addition, in this work we found that the w_{dep} was 20 nm and 24 nm for l_{fin} of 700 nm and 1.5 μm, respectively (inset in Fig. 5.8(c)), which agrees well with other reports in the literature [91], [92]. The larger w_{dep} for l of 1.5 μm is likely due to the greater strain relaxation within longer fins.

Despite the 3D nature of tri-gates, which leads to an increased surface area compared to conventional planar gates, the multi-channel tri-gate transistors showed very small gate leakage current of only about 0.2 nA/mm even at a high drain bias of 700 V when the transistors were in OFF state (Fig. 5.8(b)). The devices presented a high V_{BR} of 715 V, indicating the potential of the proposed technology for high-voltage applications.

In summary, the high-voltage multi-channel tri-gate GaN MOSHEMTs presented in this section demonstrated a significant reduction in R_{ON} and enhancement of $g_{m,max}$ were demonstrated in normally-on devices, as compared to the counterpart single-channel devices, thanks to the unique combination of multi-channel AlGaN/GaN heterostructures and tri-gate electrodes. Normally-off multi-channel tri-gate MOSHEMTs were also achieved by sidewall-depletion effect, presenting a positive V_{TH} of 0.82 V at 1 μA/mm and a high V_{BR} of 715 V. These results unveil a promising pathway for future efficient GaN power transistors with much reduced R_{ON}.

5.3 High-performance multi-channel tri-gate GaN power SBDs

In addition to MOSHEMTs, the multi-channel tri-gate technology can be used for other types of devices. In this section we demonstrate high-performance lateral GaN power Schottky barrier diodes (SBDs) based the multi-channel tri-gate architecture. We employed periodic AlGaN/GaN heterostructures with multiple 2DEG channels to reduce the R_{ON} and V_F. 3D tri-anode and tri-gate electrodes were implemented to contact and control the multi-channels, resulting in small V_{ON}, low I_R, and high V_{BR}. This unique design significantly enhanced the device characteristics, leading to state-of-the-art

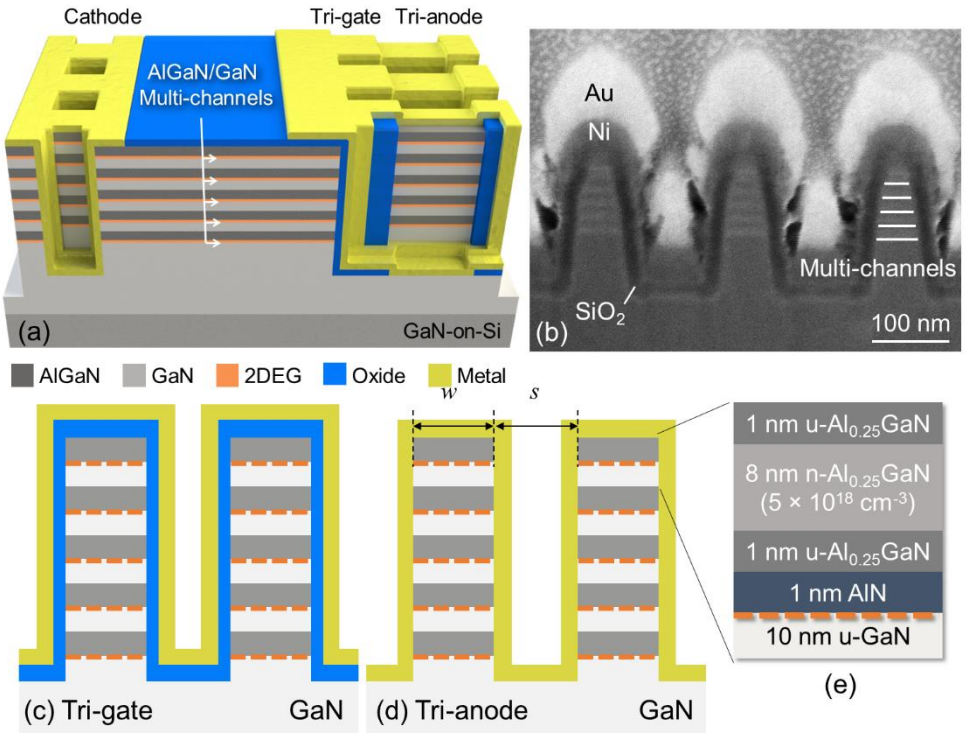

Figure 5.9: (a) Schematic of the multi-channel tri-gate SBD. (b) Cross-sectional SEM image of the multi-channel tri-gate region, tilted by 52°. Cross-sectional schematics of the (c) tri-gate and (d) tri-gate regions. (e) Schematic of the hetero-structure composing each channel in the multi-channel structure. Published in Ref. [39].

lateral GaN-on-Si power SBDs, and unveiled a novel platform to drastically improve the efficiency and reduce the size of GaN-based power devices.

The multi-channel tri-gate SBDs (Fig. 5.9) were fabricate using the same multi-channel AlGaN/GaN heterostructure as introduced in the Section 5.2, which consisted of 5 parallel 2DEG channels. The anode region was selectively patterned into fins with designed height of 200 nm and w_{fin} of 50 nm, using Ar/Cl_2-based inductively coupled plasma etching, on which the tri-gate (Fig. 5.9(b)) and tri-anode were formed over the parallel channels. The lengths of the cathode-to-anode (L_{AC}), tri-gate and tri-anode regions were 15 μm, 1.2 μm and 4 μm, respectively. The tri-anode contacts the multi-channels through the fin sidewalls, resulting in a small V_{ON}. The tri-gate/tri-anode regions shield the sidewall Schottky junction from the high electric fields under large reverse biases to reduce I_R [33]. The tri-gate region serves as a field plate, and converts the planar region of the anode into a second field plate, improving the V_{BR} [32]. The ohmic region in the cathode was patterned with w_{fin} and the spacing of 500 nm, to contact all parallel channels at the fin sidewalls. In the tri-gate region, 25 nm SiO_2 was deposited by atomic layer deposition as the oxide, and Ni/Au were used as the anode metals. Optimal single-channel SBDs with similar device architecture and dimensions in Section 4.4 were used as reference, which have high mobility of 2000 $cm^2 \cdot V^{-1}s^{-1}$ and N_s of 1×10^{13} cm^{-2}. All current values in

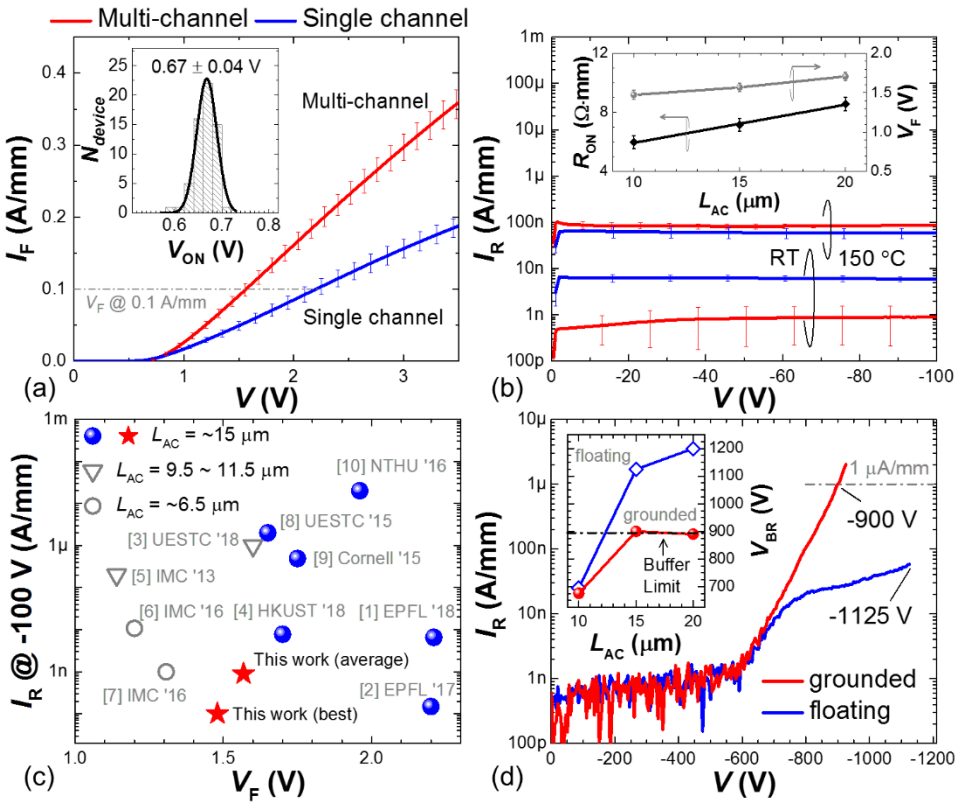

Figure 5.10: (a) Forward and (b) reverse characteristics of the multi-channel tri-gate SBDs. (c) Comparison of I_R and V_F of the GaN-on-Si SBDs in this work and literature. (d) Breakdown characteristics of the multi-channel tri-gate SBDs. The inset in (a) shows the distribution of the V_{ON}. The inset in (b) shows the dependence of R_{ON} and V_F upon L_{AC} in multi-channel tri-gate SBDs. The inset in (d) shows the dependence of V_{BR} upon L_{AC} in multi-channel tri-gate SBDs. Published in Ref. [39].

this work were normalized by the width of the device footprint (60 μm), and the error bars represent the standard deviation determined from at least 12 devices of each type.

The multi-channel tri-gate SBDs exhibited considerably enhanced performance over counterpart single-channel devices. The R_{ON} was reduced by ~50% to 7.2 ± 0.4 Ω·mm, the forward current (I_F) was increased by ~100% at 3.5 V, and V_F was decreased from 2.21 ± 0.14 V to 1.57 ± 0.06 V (at 0.1 A/mm) in multi-channel tri-gate SBDs, while exhibiting a similar V_{ON} of 0.67 ± 0.04 V at 1 mA/mm (Fig. 5.10(a)). In these results, the spacing between the fins was 100 nm, yielding a filling factor (*FF*) of 33 %. The V_F and R_{ON} in multi-channel tri-gate SBDs changed very slightly with the L_{AC} (the inset in Fig. 5.10(b)), which is beneficial for high-voltage lateral devices (requiring a large L_{AC}). In addition to the enhanced ON-state conductivity, the multi-channel tri-gate SBDs exhibited a 6x-smaller average I_R of 0.89 nA/mm at -100 V, which increased to only 86 ± 4 nA/mm at 150 ºC (Fig. 5.10(b)), revealing the excellent electrostatic control of the tri-gate over the multi-channels even at high temperature. The small V_F and I_R in this work yields better device performance, in both ON and OFF states, than in other lateral GaN SBDs with similar dimensions (Fig. 5.10(c)).

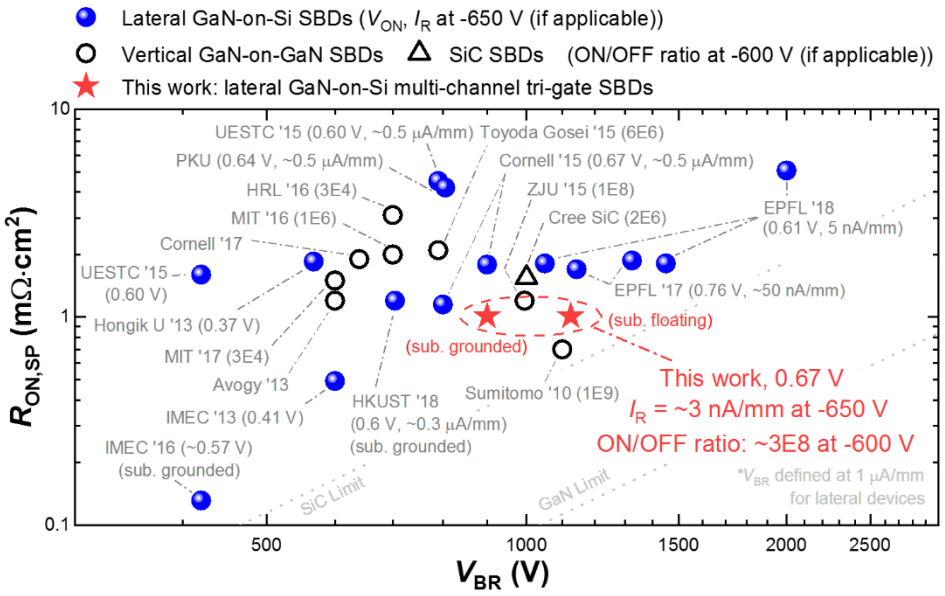

Figure 5.11: Specific on-resistance ($R_{ON,SP}$) versus V_{BR} benchmark of the multi-channel tri-gate SBDs against state-of-the-art lateral GaN SBDs. For fair comparison, the V_{BR} for all lateral devices was re-calculated based on the reported data following the definition of V_{BR} at I_R = 1 μA/mm, and devices with unspecified R_{ON} or I_R were not included. Published in Ref. [39].

The multi-channel tri-gate SBDs also presented excellent voltage-blocking capabilities (Fig. 5.10(d)). The V_{BR} at 1 μA/mm was as high as 900 V with grounded substrate, limited by the 4.3 μm buffer layer (inset in Fig. 2(d)), and the I_R at -650 V was only ~3 nA/mm, which is much smaller than in other reports (Fig. 2(e)). Such high voltage-blocking performance indicate the potential of these devices for 650 V applications, providing an small I_R at the rated voltage and a safety margin of ~50% from the rated voltage to the hard breakdown. In addition, the multi-channel tri-gate SBDs presented excellent high-power figure-of-merit up to 1.25 GW/cm^2 (Fig. 5.11), which is even comparable to state-of-the-art GaN-on-GaN vertical SBDs [184], [185] as well as GaN-on-Si power transistors.

The switching performance in multi-channel tri-gate SBDs is very promising. Despite the ~50% reduction in R_{ON}, the charge (Q) in multi-channel SBDs increased by only 8.4 % to 28.5 ± 1.5 pC/mm (Fig. 5.12(a)), which is smaller than in conventional fast-switching GaN-on-Si power SBDs [147], [161], resulting in a much smaller $R_{ON}\cdot Q$ product and thus offering great prospects for efficient power rectification at high frequencies. The switching characteristics of the multi-channel tri-gate SBDs was investigated using a rectification circuit [186] with minimized parasitic elements through an optimized PCB layout and short interconnections (Fig. 5.12(b)). At a frequency of 1 MHz, the forward-recovery time of the multi-channel tri-gate SBDs was as small as 13.8 ns (Fig. 5.12(c)), along with a very short reverse-recovery time of 8.2 ns (Fig. 5.12(d)), which did not change from 10 kHz to 10 MHz. Figures 5.12(e) and (f) show the V_{in} and V_{out} waveforms as well as Lissajous plots of the I-V

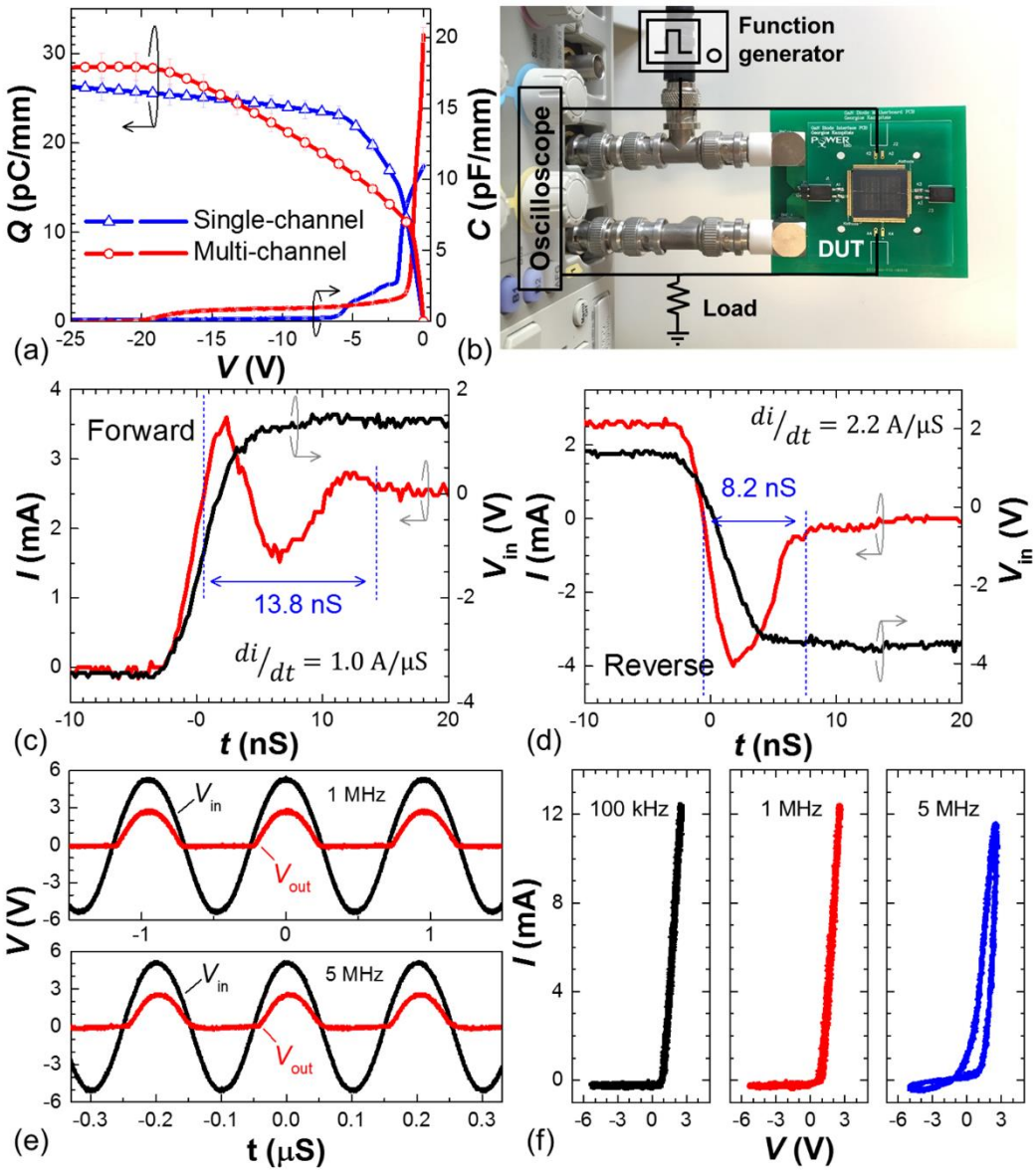

Figure 5.12: (a) Capacitance (*C*) and *Q* in multi-channel and single-channel SBDs. (b) Setup for measuring the switching characteristics. The device was bonded onto a printed circuit board (PCB) and connected directly to the oscilloscope to minimize parasitic elements. (c) Forward- and (d) reverse-recovery characteristics of the multi-channel tri-gate SBDs. The devices were switched between 1.5 V to -3.5 V at 1 MHz (limited by the oscilloscope) using the internal oscilloscope function generator and a 50 Ω resistor as the load. (e) Input (V_{in}) and output (V_{out}) waveforms and (f) Lissajous *I*-*V* plots showing the rectification characteristics of the multi-channel tri-gate SBDs at different frequencies, using an external function generator and a 220 Ω resistor. The small phase shift in (e) between V_{in} and V_{out} was likely caused by parasitic elements in the circuit. Published in Ref. [39].

characteristics of the multi-channel tri-gate SBDs, respectively, which indicate an effective rectification by these devices up to 5 MHz (at this frequency a phase shift between the *V* and *I* was observed).

The high performance of multi-channel tri-gate SBDs depends significantly on the tri-gate/tri-anode geometry to balance the ON-state, OFF-state and switching characteristics. As shown in Fig. 5.13(a), a smaller w_{fin} diminishes I_R and *Q*, but does not significantly degrade R_{ON}, V_{ON} and V_F, thus resulting

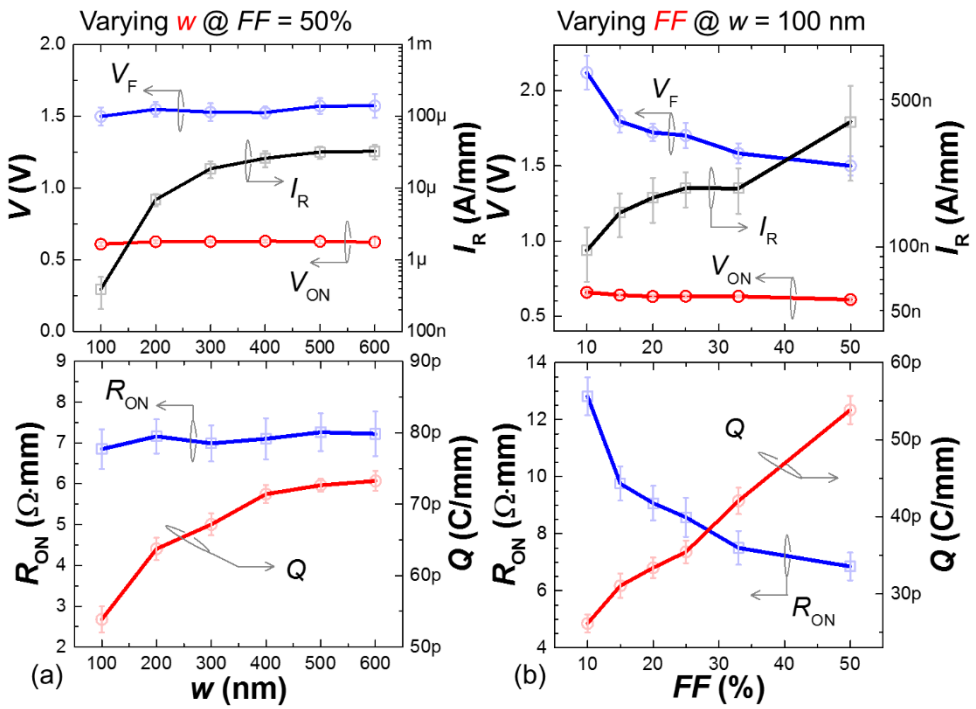

Figure 5.13: Dependence of multi-channel tri-gate SBDs' characteristics upon (a) *w* and (b) *FF* in tri-gate and tri-anode regions. Published in Ref. [39].

in a reduced $R_{ON}\cdot Q$ product. The reduction in I_R is due to the smaller pinch-off voltages in tri-gate/tri-anode regions with decreasing w_{fin}, which lowers the electric field at the Schottky junction and exponentially reduces the I_R [33]. The smaller Q is due to the reduced N_s [29] and smaller threshold voltages in the tri-gate/tri-anode regions as w decreases [35]. Therefore, to have an I_R below 0.1 μA/mm for efficient power devices, w_{fin} needs to be smaller than 100 nm for the heterostructure used in this work. *FF* is another important variable (Fig. 5.13(b)). A decrease in *FF* yields a reduction in I_R and Q, but an increase in V_F, V_{ON} and R_{ON}, thus leading to an optimal *FF* of 33 % for both a small R_{ON} and $R_{ON}\cdot Q$ product.

Another reason for the excellent performance in the multi-channel tri-gate SBDs is the high μ_e in their tri-gate/tri-anode regions. To extract the μ_e, we fabricated multi-channel MOSHEMTs with 50 μm-long planar-gate and tri-gate structures. We measured the R_{ON}, and integrated the measured gate capacitance (C_G) at different gate voltages (V_G) (Figs. 5.14(a) and (b)) to extract the gate charge (Q_G). The μ_e was obtained using $R_{ON} \approx L_G/(W_G\cdot N_s\cdot q\cdot\mu_e) = L_G^2/(Q_G\cdot\mu_e)$, in which L_G and W_G are the gate length and width, respectively, q is the elementary charge, and N_s is the 2DEG concentration in gate region. This method eliminates possible errors in W_G from variation in lithography or normalization. The μ_e in the tri-gate region was as high as 2063 ± 123 $cm^2\cdot V^{-1}s^{-1}$, which is comparable to that in

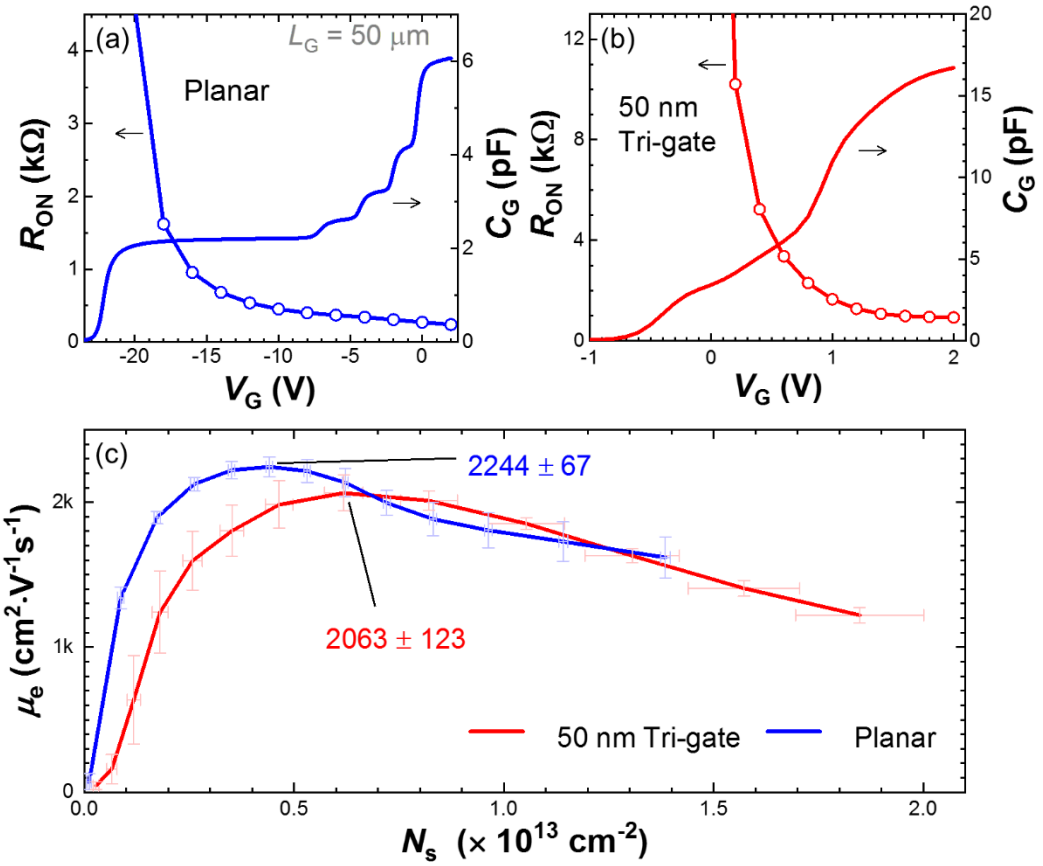

Figure 5.14: Average R_{ON} and C_G in multi-channel MOSHEMTs with (a) planar-gates and (b) 50 nm-wide tri-gates. The L_G was 50 µm for both devices, and the gate-to-source and gate-to-drain distances were both 1.5 µm. R_{ON} was measured using drain voltages below 0.1 V, and C_G was measured at 1 MHz. (c) μ_e versus N_s in the two devices. The N_s was normalized by the top surface area of the fins, which did not impact the determination of μ_e. Published in Ref. [39].

planar-gate multi-channel devices (2244 ± 67 cm^2·V^{-1}s^{-1}) (Fig. 5.14(c)), revealing a negligible reduction in μ_e despite the small w_{fin} of 50 nm, which is much higher than in conventional single-channel AlGaN/GaN fin structures [64], [65], [83].

To conclude this section, the multi-channel tri-gate technology significantly enhanced the performance of power GaN-on-Si SBDs. Compared with reference single-channel tri-gate devices, the multi-channel tri-gate SBDs presented a significantly reduced R_{ON} and a much smaller V_F, along with an ultra-low I_R of ~1 nA/mm at -600 V and high V_{BR} of -900 V at 1 µA/mm with grounded substrate, yielding state-of-the-art power SBDs for 600 V/650 V ratings.

5.4 Multi-channel tri-gate GaN devices with ultra-low on-resistance

While great enhancement in device performance has been achieved in Sections 5.2 and 5.3, based on the multi-channel tri-gate technology, the prospects of this approach can be far beyond by further enhancing the conductivity of the multi-channels.

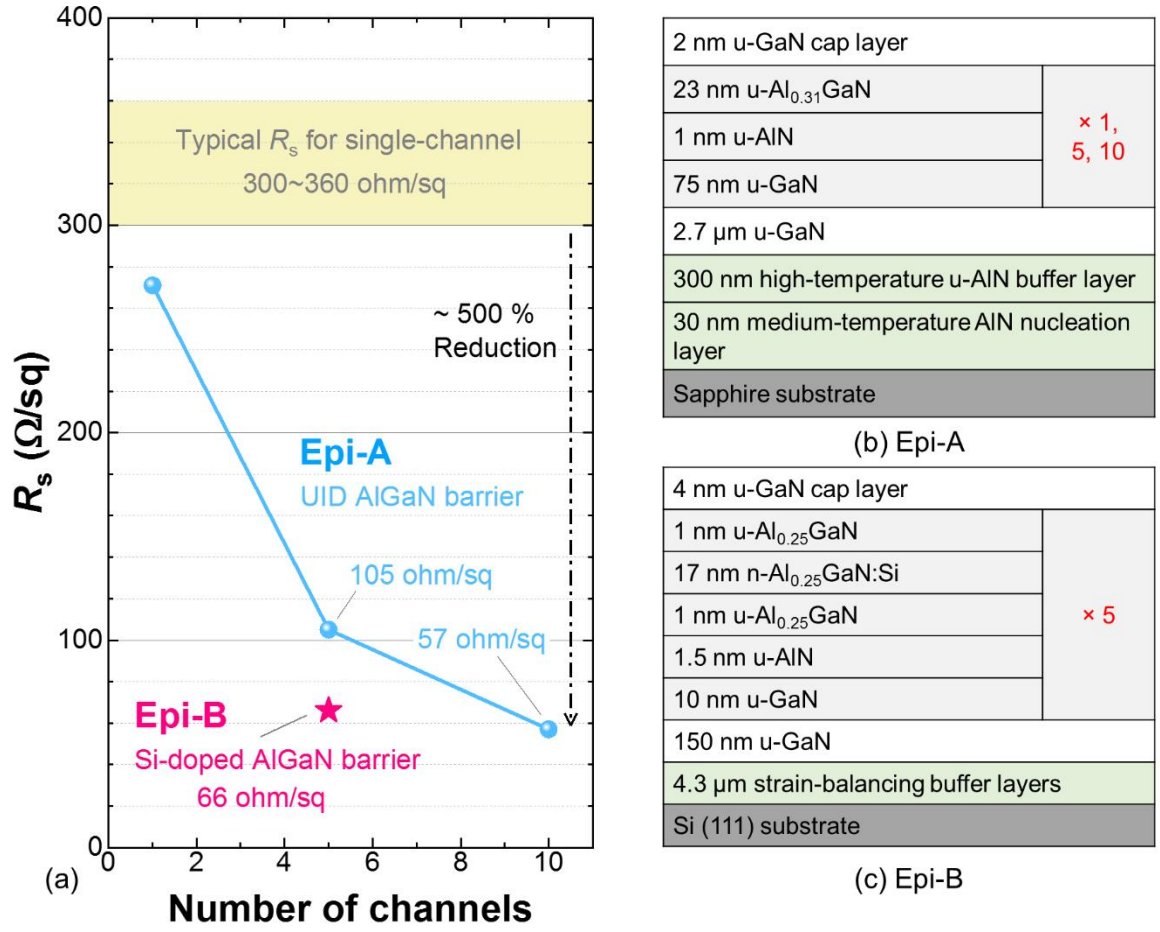

Figure 5.15: (a) Dependence of R_s on the number of 2DEG channels in two types of multi-channel AlGaN/GaN hetero-structures: (b) Epi-A with undoped AlGaN barrier layers and (c) Epi-B Si-doped AlGaN barrier layers. Epi-A was grown in EPFL using a close coupled showerhead (CCS) MOCVD system, and Epi-B was grown on 6 inch Si substrate in collaboration with Enkris Semiconductor Inc.

To further enhance the conductivity of the multi-channel structure, one way is to increase the number of channels to reduce the R_s. As show in Fig. 5.15(a), the R_s was reduced from 271 Ω/sq in a single-channel AlGaN/GaN heterostructure to 57 Ω/sq in a counterpart 10x-channel structure (Epi-A in Fig. 5.15(b)), rendering a large reduction of about 5 folds from typical AlGaN/GaN heterostructure, which is very promising for the reduction in R_{ON} in lateral GaN electronic devices. However, the total thick-ness of Epi-A (Fig. 5.15(b)) was about 1 μm, on which it is extremely challenging to form sub-100 nm-wide tri-gates, limited the difficulties in the etching of high-aspect-ratio multi-channel fins and the formation of 3D electrodes around them.

Another approach to reduce the R_s is to increase the conductivity of each of the multi-channels, by doping AlGaN barrier layers with a large concentration of Si (1×10^{19} cm^{-3}) to boost the N_s (Epi-B in Fig. 5.15(c)). This enables us to thin the GaN channel layers to facilitate the fabrication of multi-channel tri-gate devices. As shown in Figs. 5.15(a) and (c), Epi-B was only about 150 nm thick with 5x-channel, but exhibited a very small R_s of 66 Ω/sq that was close to that of the 1 μm-thick 10x-

channel Epi-A, thanks to the high Si doping in the barrier layers. Such small R_s and total thickness of the Epi-B resulted in a very small equivalent resistivity (ρ_{eff}) of 1 mΩ·cm, which is very promising for high-performance multi-channel tri-gate devices as discussed in Section 5.2.

Table 5.2: Comparison of the multi-channel AlGaN/GaN heterosturcture (Epi-B) in this work with state-of-the-art single- and multi-channel GaN heterostructures in the literature.

	Barrier	Number of channels	substrate	Grown by	R_s (Ω/sq)	Total thickness (nm)	ρ_{eff} (mΩ·cm)	N_s ($\times 10^{13}$ cm^{-2})	μ_{Hall} ($cm^2 \cdot V^{-1}s^{-1}$)
Epi-B	AlGaN (Si doped)	5	Si	MOCVD	66	150	1.0	5.45	1719
[187]	InAlN	1	Al_2O_3	MOCVD	182	--	--	4.2	812
[188]	InAlGaN	1	SiC	MOCVD	195	--	--	1.8	1770
[189]	AlN	1	Si	MOCVD	235	--	--	2.15	1250
[170]	AlN	1	Al_2O_3	MBE	129	--	--	3.2	1513
		3			335	375	12.6	--	--
[176]	AlGaN	5	Al_2O_3	MOCVD	205	625	12.8	--	--
		8			138	1000	13.8	--	--
[170]	AlN	9	Al_2O_3	MBE	37	545	2.0	10.8	1567

We further compared Epi-B in this work with state-of-the-art single- and multi-channel GaN heterostructures in the literature (Tab. 5.2). While Epi-B was grown on Si substrates using MOCVD, it shows a small R_s, a small total thickness of 150 nm, and the smallest ρ_{eff} of 1 mΩ·cm, along with the highest μ_{Hall} of 1719 $cm^2 \cdot V^{-1}s^{-1}$ among the multi-channel structures, which is very promising for high-performance multi-channel tri-gate GaN devices.

We fabricated tri-gate multi-channel GaN-on-Si MOSHEMTs and SBDs based on Epi-B. The device structure of the MOSHEMTs was similar to that has been presented in Section 5.2 (Fig. 5.3), and the architecture of the SBDs was similar to Fig. 5.9 in Section 5.3. The device fabrication started with e-beam lithography to define the fins, which were etched by inductively coupled plasma with a depth of ~250 nm. The w_{fin} was 80 nm and the length of the fins were 1.5 µm long in the MOSHEMTs, while the w_{fin} was 50 nm and the spacing (s) were 100 nm in SBDs. The devices were isolated by mesa etching with a depth of 450 nm, followed by the formation of the source ohmic contact. The

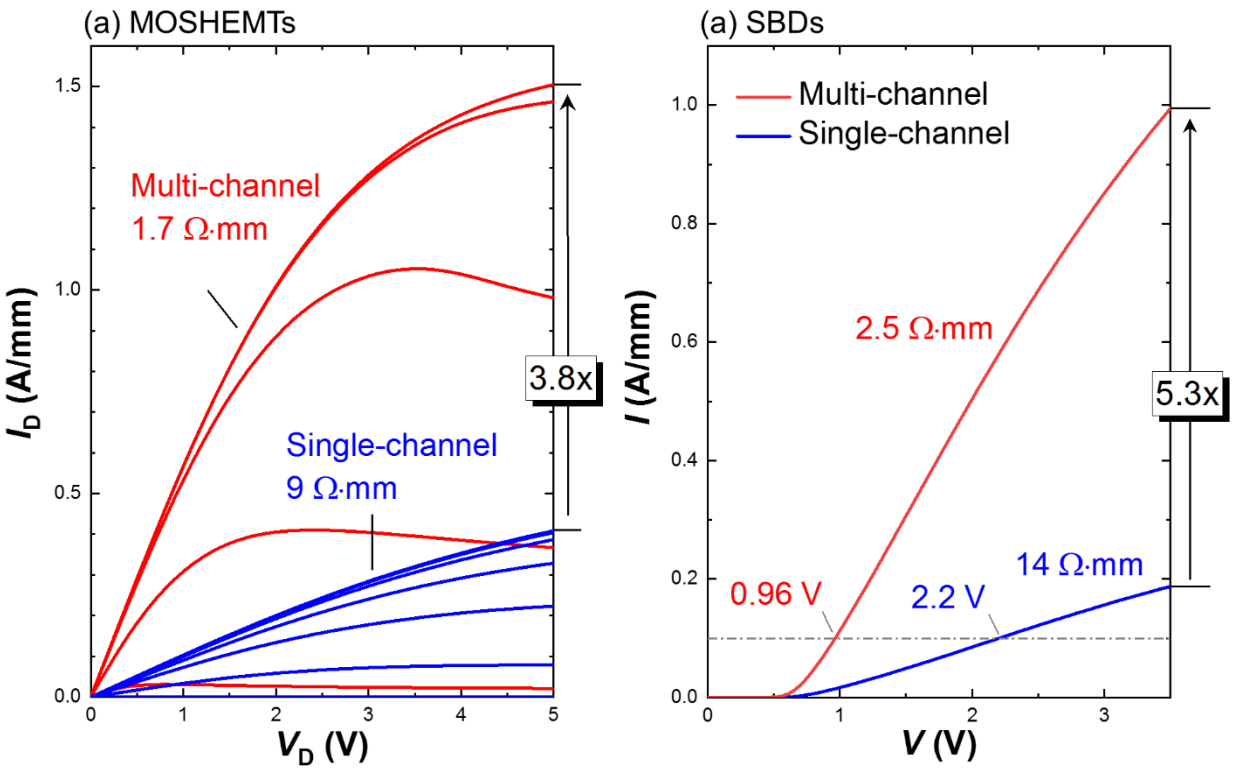

Figure 5.16: (a) Comparison of output characteristics of multi-channel tri-gate and single-channel planar-gate MOSHETMs, in which the maximum V_G was 5 V and the gate-to-drain distance (L_{GD}) was 10 µm for both devices. (b) Comparison of forward performance of multi-channel tri-gate and single-channel tri-gate SBDs, in which the anode-to-cathode distance (L_{AC}) was 15 µm. All current values here were normalized by the width of the device footprint.

ohmic contact was formed by Ti/Al/Ti/Ni/Au (20/120/40/60/50 nm), annealed at 780 ºC in N_2 for 30 sec. Then 23 nm SiO_2 were deposited by atomic layer deposition and selectively removed in the ohmic and tri-anode region. Single-channel MOSHEMTs and SBDs in Sections 3.2 and 4.4, respectively, were taken as the reference devices. All the current values were normalized by the width of the device footprint, which was 60 µm.

The ultra-small R_s of 66 ohm/sq in Epi-B greatly enhanced the ON-state conductance of the devices. As shown in Fig. 5.16(a), the R_{ON} of the MOSHEMTs were reduced remarkably from 9 Ω·mm in a single-channel planar device to 1.7 Ω·mm in the multi-channel tri-gate devices, along with a significant enhancement of 3.8x in the drain current. The SBDs were also greatly enhanced by the multi-channel tri-gate technology, as plotted in Fig. 5.16(b). The R_{ON} was greatly reduced from 14 Ω·mm in a single-channel tri-gate device to 2.5 Ω·mm in a multi-channel tri-gate device, along with a dramatic enhancement of 5.3x in forward current, resulting in a much diminished forward voltage of 0.96 V at 0.1 A/mm. These results reveal that ultra-low R_{ON} can be achieved in many types of devices using the multi-channel tri-gate technology, constituting a high promising platform for future efficient electronic devices.

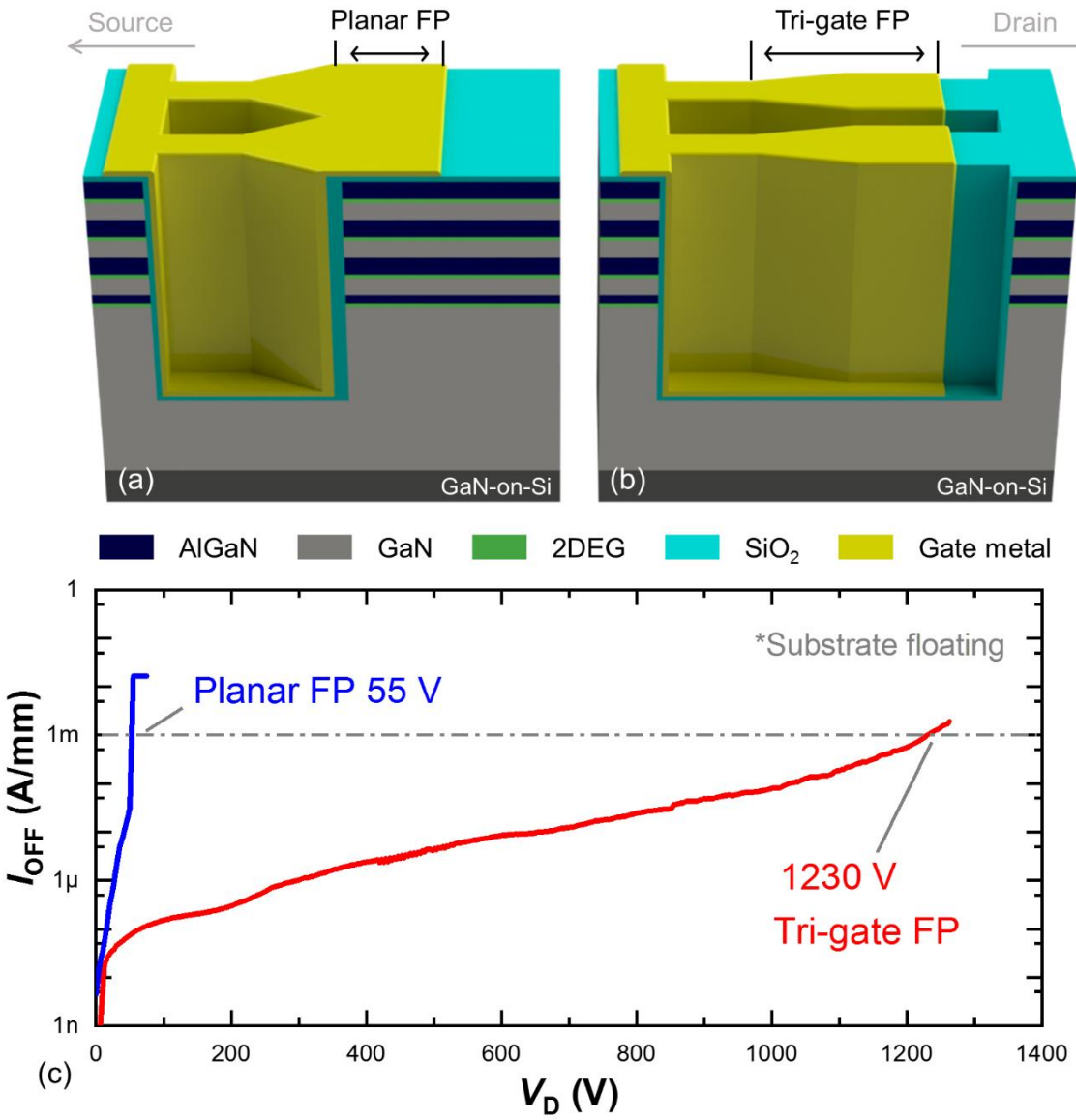

Figure 5.17: Multi-channel tri-gate GaN MOSHEMTs with (a) planar and (b) tri-gate FPs, in which the L_{GD} was 10 μm for both devices. (c) OFF-state breakdown characteristics of the two devices, which were measured with a floating substrate connection. The devices were fabricated using a multi-channel AlGaN/GaN epitaxy with R_s of ~80 Ω/sq and exhibited R_{ON} of ~3 Ω·mm. The V_{BR} here was defined at I_{OFF} = 1 mA/mm.

In addition to the ultra-low R_{ON} in the multi-channel wafers, high blocking voltage can be achieved for multi-channel tri-gate devices based on a judicious design of the tri-gate region. In a multi-channel tri-gate device with ultra-conductive channels, conventional field plates (Fig. 5.17(a)) are no longer functional, because they may not be able to pinch off the buried channels with high N_s. Moreover, the large N_s in the multi-channels results in a very short depletion region (along the source-drain direction), causing a very high electric field at the gate or FP region and hence an early breakdown of the device. These issues can be resolve using the purely the tri-gate slanted tri-gate FPs (Fig. 5.17(b)). As shown in Fig. 5.17(c), the breakdown voltage was greatly enhanced from ~40 V to ~1200 V, by

simply changing the design of the gate region from Fig. 5.17(a) to Fig. 5.18(b), rendering a breakthrough in high-voltage and high-conductivity multi-channel tri-gate devices, and unleashing the significant potential of the multi-channel tri-gate technology in revolutionizing GaN devices for future efficient power applications.

5.5 Conclusion

In this chapter we presented a novel device concept of multi-channel tri-gate architectures, which demonstrated tremendous prospects for future efficient power electronics. The multi-channel tri-gate technology can lead to novel lateral power devices with much smaller R_{ON} and much higher current ratings for a given device area, thanks to its ultra-low R_s, combined with the superior voltage-blocking capabilities of tri-gates and slanted tri-gates. Secondly, this approach can be easily extended for high-voltage normally-on/off multi-channel tri-gate GaN transistors, nanoscale in-plane-gate transistors, and many other devices and applications, yielding a promising platform for future efficient electronic devices. To unleash the full prospects of multi-channel tri-gate technology, an intensive and coupled material research and device engineering are required, which opens tremendous opportunities for future studies in novel epitaxy structures and device designs.

Chapter 6 Conclusion

6.1 Achieved results

To summarize, this thesis addresses three major challenges in lateral GaN-on-Si high-voltage power devices.

The first challenge is to reduce the $R_{ON}{\cdot}A$ for GaN-on-Si power devices. Novel tri-gate FPs were developed to address this challenge, by improving the V_{BR} of the device to minimize the large L_{GD} required for high V_{BR}, which diminishes both the R_{ON} and the A. The tri-gate FPs were designed based on a lateral scheme, by simply tuning the width of fins lithographically, which facilitates and enhances the FPs from the conventional vertical scheme. A novel slanted tri-gate structure was invented to enable high V_{BR} at a smaller L_{GD}, by distributing more homogeneously the electric field, which greatly diminished the $R_{ON}{\cdot}A$ of the device, and resulted in GaN-on-Si power transistors with record high-power figure of merit.

The second challenge is to achieve high-performance GaN-on-Si power SBDs, which was resolved in this work by a judicious design of the anode electrode based on the tri-gate technology. An ultra-low leakage current of 5 nA/mm at -650 V was achieved via a hybrid of tri-gate and tri-anode structures, which minimizes the electric field at the Schottky junction and diminishes the leakage current exponentially. In addition, the slanted tri-gate was further implemented into the anode and resulted in unprecedented V_{BR} of 2 kV at 1 µA/mm, which is significantly higher than in any other GaN-on-Si SBDs and even comparable to state-of-the-art 650 V GaN-on-Si power transistors. The excellent integratability of the slanted tri-gate SBDs were also demonstrated, in reverse-blocking GaN-on-Si power transistors with slanted tri-gate Schottky drain electrodes, presenting the record reverse-blocking performance that is much improved from existing technologies.

The third challenge is the limited figure-or-merit in current power GaN-on-Si devices. To address this challenge, a novel multi-channel tri-gate technology was invented, featuring multiple parallel 2DEG channels for low R_{ON} and 3-dimensional tri-gate electrodes for high V_{BR}. This concept was demonstrated in both multi-channel tri-gate normally-on/off MOSHEMTs and SBDs, presenting much reduced R_{ON} from conventional single-channel devices while maintaining high V_{BR}. The multi-channel tri-gate power devices can be further enhanced based on ultra-conductive GaN-based multi-

channel heterostructures, resulting in an ultra-small R_{ON} down to 1.7 Ω·mm and a high V_{BR} up to 1230 V, which offers a highly promising platform to release the full potential of GaN power solutions.

This work reveals extraordinary values of the tri-gate technologies for high-voltage GaN power devices, presents high-voltage GaN-on-Si power SBDs with unprecedented performance, and demonstrates a novel multi-channel tri-gate structure that dramatically reduce the R_{ON}. The tri-gate technology presented in this thesis enriches the toolbox for lateral GaN-on-Si power devices, and provides a novel platform that can hopefully unleash the full capabilities of GaN for efficient power conversion.

6.2 Future development

Built upon the work of this thesis, some future research directions are suggested as follows.

Normally-off tri-gate GaN devices with low R_{ON}. While most of the transistors demonstrated in this thesis are normally-on, which can be implemented in the cascade configuration to achieve the demanded normally-off operation, further efforts could be made to develop normally-off tri-gate MOS GaN transistors, by combining the tri-gate with other technologies such as p-GaN cap, AlGaN recess or fluorine ions. Such devices can provide a low R_{ON} and a robust gate electrode, thanks to the trench conduction and the gate oxide, respectively, which are important to enhance the efficiency and reliability of power GaN transistors. In this regard, it is crucial to first understand the impact of the p-GaN cap, the AlGaN recess or the fluorine ions upon the V_{TH} in tri-gate devices, and then optimize the fin etching process for less damages to enhance the trench conduction. It will be also important to explore different dielectrics and develop a reliable MOS gate stack for these transistors, for which the SiN deposited by either low pressure chemical vapor deposition or the MOCVD can be promising due to the high process temperature.

High-voltage multi-channel tri-gate devices with ultra-low R_{ON}. In this thesis, a high V_{BR} of 1230 V at 1 mA/mm has been achieved for a multi-channel structure with R_s of ~80 Ω/sq, resulting in a small R_{ON} of ~3 Ω·mm and a record FOM of 2.3 GW/cm^2, which is around 75% higher than in state-of-the-art single-channel GaN-on-Si transistors. While these results are remarkable, the R_{ON} could be further reduced, down to 1.5 Ω·mm for example (Fig. 5.16), using more conductive multi-channel structures. Consequently, it is highly interesting to demonstrate multi-channel tri-gate devices with simultaneously ultra-low R_{ON} and high V_{BR}. To achieve this goal, different multi-channel structures and tri-gate designs must be tested in a highly coupled manner, to understand the root factor that limits the V_{BR} in ultra-conductive multi-channel devices and how it can be resolved. Simulation works may also be important for the optimization of the device.

Monolithic power GaN ICs based on the tri-gate technology. Power AlGaN/GaN-on-Si devices offer great opportunities for advanced power ICs with much higher power density and greater energy efficiency, which can lead to far-reaching changes in current power conversion technologies. The tri-gate, as presented in this thesis, can deliver both high-performance GaN-on-Si transistors and diodes, thus providing a remarkable and highly promising approach to realize high-frequency power GaN-on-Si ICs. Towards this goal, it is of great importance to scale up the tri-gate devices presented in this work, to understand their behavior in real-world power circuits, and monolithically integrate them to construct the power ICs, which should be carefully designed and optimized according to the target application.

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Curriculum Vitae

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Highlights

- Growth, fabrication, and integration of GaN transistors, diodes and LEDs
- 10 years' experience in MOCVD in both academia and industry
- Novel tri-gate technologies for GaN power devices with state-of-the-art performance
- 32 journal papers, 20 conference contributions, and 2 international patents
- The reviewer of *IEEE Electron Device Letters*, *Applied Physics Letters*, *IEEE Transactions on Electron devices*, *Superlattices and Microstructures*, etc.

Education

2015.05 - present **École Polytechnique Fédérale de Lausanne (EPFL), Switzerland**
Ph.D. in microsystems and microelectronics
Thesis: *Tri-gate Technologies for High-Performance Power GaN Devices*
Advisor: Prof. Elison Matioli.

2011.09 - 2014.06 **Hong Kong University of Science and Technology (HKUST), Hong Kong, China**
M.Phil. in electronic and computer engineering,
Thesis: *Performance Enhancement of III-nitride HEMTs Grown by MOCVD and Their Monolithic Integration with LEDs*
Advisor: Professor Kei May Lau.

2005.09 - 2009.06 **Xiamen University, Xiamen, China**
B.Sc. in microelectronics & B.Sc. in economics
Thesis (published): *Growth Kinetic Processes of AlN on The Al-Polar Surface of AlN*
Advisor: Prof. Junyong Kang and Prof. Shuping Li

Working Experience

2010.06 - 2011.08 **Hong Kong University of Science and Technology, Hong Kong, China**
Full-time research assistant in MOCVD

2009.06 - 2010.01 **San'an Optoelectronics Co., Ltd., Xiamen, China**
Epitaxy engineer in LEDs

Research Experience

2009.06 - present **MOCVD growth of GaN and its alloys**

- ✓ Hands-on experience in both academia and industry

- ✓ High-breakdown AlGaN/GaN heterostructures on Si, SiC and sapphire substrates
- ✓ High-performance GaN LEDs on Si and sapphire substrates
- ✓ Ultra-conductive multi-channel AlGaN/GaN heterostructures (R_s < 60 ohm/sq) for high-frequency and high power applications
- ✓ Ultra-thin barrier AlN/GaN heterostructures
- ✓ High-quality *in situ* SiN_x passivation by MOCVD
- ✓ Vertical GaN power devices
- ✓ Regrown n^{++}-GaN source/drain contacts for ultra-low contact resistance

2010.06 - present **GaN electronic devices**

- ✓ Multi-channel tri-gate GaN transistors and diodes with ultra-low on-resistance and high breakdown voltage
- ✓ Multi-channel in-plane-gate GaN transistors with record current and ultra-high trans-conductance
- ✓ Novel slanted tri-gate architectures to enhance the breakdown voltage for lateral GaN power devices
- ✓ Slanted tri-gate GaN-on-Si MOSHEMTs with record high-power figure-of-merit
- ✓ Slanted tri-gate GaN-on-Si power SBDs with record breakdown voltage (2 kV at 1 μA/mm) and leakage current (5 nA/mm at -650 V)
- ✓ 2 kV tri-gate normally-off GaN-on-Si power transistors with record performance
- ✓ E-mode ultra-thin-barrier AlN/GaN transistors with record transconductance
- ✓ Novel *in situ* SiN_x/AlN/GaN MISHEMTs

2010.06 - 2014.04 **GaN optical devices**

- ✓ High-performance GaN-on-Si LEDs with stress/dislocation-engineered AlN/GaN superlattice interlayers
- ✓ The first demonstration of yellow GaN-on-Si LEDs

2010.06 - 2014.04 **Monolithic integration of GaN devices**

- ✓ The first fully integrated surface acoustic wave oscillators using GaN-on-Si
- ✓ Monolithically integrated reverse-blocking GaN-on-Si power transistors with record breakdown voltage and reverse leakage current
- ✓ Monolithically integrated reverse-conducting GaN-on-Si transistors with record breakdown voltage, leakage current and on-resistance
- ✓ Monolithic integration of GaN HEMTs and LEDs with record performance
- ✓ Advanced metal-interconnection-free integration of GaN HEMTs and LEDs

Patents (filed)

1. E. Matioli & J. Ma, "Semiconductor device comprising a three-dimensional field plate," International Patent Application n° PCT/IB2017/055961, Sept. 28, 2017.
2. E. Matioli & J. Ma, "Semiconductor devices with multiple channels and three-dimensional electrodes," International Patent Application n° PCT/IB2017/057083, Nov. 14, 2017.

Journal Articles (First-author)

1. J. Ma, G. Santoruvo, Taifang Wang and E. Matioli, "Impact of fin width on tri-gate AlGaN/GaN MOSHEMTs," submitted.
2. J. Ma, C. Erine, P. Xiang, K. Cheng and E. Matioli, "title confidential," submitted.

3. J. Ma, G. Kampitsis, P. Xiang, K. Cheng and E. Matioli, "Multi-channel tri-gate GaN power Schottky diodes with low on-resistance," ***IEEE Electron device letters*** 40, 275 (2018). (Featured in *Semiconductor Today*)
4. J. Ma, C. Erine, R. Soleimanzadeh, P. Xiang, T. -H Shen, V. Tileli, K. Cheng and E. Matioli, "Multi-channel tri-gate normally-on/off AlGaN/GaN MOSHEMTs on Si substrate with high breakdown voltage and low ON-resistance," ***Applied Physics Letters*** 113, 242102 (2018). (Featured in *Compound Semiconductor* and *Semiconductor Today*)
5. J. Ma and E. Matioli, "2 kV slanted tri-gate GaN-on-Si Schottky barrier diodes with ultra-low leakage current," ***Applied Physics Letters*** 112, 052101 (2018). (Featured in *Semiconductor Today* and *Silicon Valley Microelectronics*)
6. J. Ma, M. Zhu, and E. Matioli, "900 V reverse-blocking GaN-on-Si MOSHEMTs with a hybrid tri-anode Schottky drain," ***IEEE Electron Device Letters*** 38, 1704 (2017). (Featured in *Semiconductor Today* and *Silicon Valley Microelectronics*)
7. J. Ma and E. Matioli, "Slanted tri-gates for high-voltage GaN power devices," ***IEEE Electron Device Letters*** 38, 1305 (2017). (Featured in *Semiconductor Today*)
8. J. Ma, D. C. Zanuz and E. Matioli, "Field plate design for low leakage current in lateral GaN power Schottky diodes: role of the pinch-off voltage," ***IEEE Electron Device Letters*** 38, 1298 (2017).
9. J. Ma and E. Matioli, "High performance tri-gate GaN power MOSHEMTs on silicon substrate," ***IEEE Electron Device Letters*** 38, 367 (2017). (The most popular EDL paper during 2017/01 - 2017/07)
10. J. Ma and E. Matioli, "High-voltage and low-leakage AlGaN/GaN tri-anode Schottky diodes with integrated tri-gate transistors," ***IEEE Electron Device Letters*** 38, 83 (2017).
11. J. Ma, G. Santoruvo, P. Tandon, and E. Matioli, "Enhanced electric performance and heat dissipation in AlGaN/GaN Schottky barrier diodes using hybrid tri-anode structure," ***IEEE Transactions on Electron Devices*** 63, 3614 (2016).
12. J. Ma, X. Lu, X. Zhu, T. Huang, P. Xu and K. M. Lau, "MOVPE growth of *in situ* SiN_x/AlN/GaN MISHEMTs with low leakage current and high on/off current ratio," ***Journal of Crystal Growth*** 414, 237 (2015).
13. J. Ma, X. Lu, H. Jiang, C. Liu and K. M. Lau, "*In situ* growth of SiN_x as gate dielectric and surface passivation for AlN/GaN heterostructures by metalorganic chemical vapor deposition," ***Applied Physics Express*** 7, 091002 (2014).
14. Z. Liu*, J. Ma*, T. Huang and K. M. Lau, "Selective epitaxial growth of monolithically integrated GaN-based light emitting diodes with AlGaN/GaN driving transistors," ***Applied Physics Letters*** 104, 091103 (2014) (*Co-first author). (Featured in *Semiconductor Today*)
15. J. Ma, X. Zhu, K. M. Wong, X. Zou and K. M. Lau, "Improved GaN-based LED grown on silicon (111) substrates using stress/dislocation-engineered interlayers," ***Journal of Crystal Growth*** 370, 265 (2013).
16. J. Ma, Q. Zhuang, G. Chen, C. Huang, S. Li, H. Wang and J. Kang, "Growth kinetic processes of AlN molecules on the Al-polar surface of AlN," ***Journal of Physical Chemistry A*** 114, 9028-9033 (2010).

Journal Publications (Co-author)

17. M. Zhu, J. Ma, N. Luca and E. Matioli, "2 kV normally-off tri-gate GaN power MOSHEMTs with 2.42 $m\Omega \cdot cm^2$," submitted.
18. N. Luca, M. Zhu, J. Ma and E. Matioli, "High-performance nanowire-based e-mode power GaN MOSHEMTs with large work-function gate metal," ***IEEE Electron Device Letters*** 40, 439 (2019).
19. T. Wang, J. Ma and E. Matioli, "1100 V AlGaN/GaN MOSHEMTs with integrated tri-anode freewheeling diodes," ***IEEE Electron Device Letters*** 39, 1038 (2018).
20. X. Lu, J. Ma, H. Jiang, C. Liu, P. Xu, K. M. Lau, "Fabrication and characterization of self-aligned AlN/GaN MISHEMT with *in situ* SiN_x gate dielectric and regrown Source/drain," ***IEEE Transactions on Electron Devices*** 62, 1862 (2015).

21. C. Liu, Y. Cai, Z. Liu, J. Ma and K. M. Lau, "Metal-interconnection-free integration of InGaN/GaN light emitting diodes with AlGaN/GaN high electron mobility transistors," ***Applied Physics Letters*** 106, 181110 (2015). (Featured in *Semiconductor Today*)
22. C. Liu, Z. Liu, T. Huang, J. Ma and K. M. Lau, "Improved breakdown characteristics of monolithically integrated III-nitride HEMT-LED devices using carbon doping," ***Journal of Crystal Growth*** 414, 243 (2015).
23. X. Lu, J. Ma, H. Jiang, C. Liu and K. M. Lau, "Low trap states in *in-situ* SiN_x/AlN/GaN metal-insulator-semiconductor structures grown by metal-organic chemical deposition," ***Applied Physics Letters*** 105, 102911 (2014).
24. Z. Liu, T. Huang, J. Ma and K. M. Lau, "Monolithic Integration of AlGaN/GaN HEMTs on LEDs (HEMT-LEDs) by MOCVD," ***IEEE Electron Device Letters*** 36, 3 (2014).
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26. X. Lu, J. Ma, Z. Liu, H. Jiang, T. Huang and K. M. Lau, "*In situ* SiN_x gate dielectric by MOCVD for low-leakage-current ultra-thin-barrier AlN/GaN MISHEMTs on Si," ***Physica Status Solidi (a)*** 211, 730 (2014).
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31. X. Zou, K. M. Wong, X. Zhu, W. C. Chong, J. Ma and K. M. Lau, "High-performance green and yellow LEDs grown on SiO_2 nanorod patterned GaN/Si templates," ***IEEE Electron Device Letters*** 34, 903-905 (2013). (Featured in *Semiconductor Today*)
32. X. Zhu, J. Ma, T. Huang, M. Li, K. M. Wong and K. M. Lau, "Improved surface morphology and mobility of AlGaN/GaN HEMT grown on silicon substrate," ***Physica Status Solidi (c)*** 9 (3-4), 473 (2012).

Conference contributions

33. J. Ma and E. Matioli, "Tri-gate technologies for high-performance GaN power devices," ***International Workshop on Nitride Semiconductors (IWN)***, Kanazawa, Japan, 2018. (Best Student Paper Award)
34. J. Ma and E. Matioli, "2 kV GaN-on-Si SBDs with a slanted tri-gate architecture," ***Compound Semiconductor Week (CSW)***, Boston, USA, 2018. (Best Student Paper Award Honorary Mention)
35. J. Ma and E. Matioli, "Uni-directional GaN-on-Si MOSHEMTs with high reverse-blocking voltage based on nanostructured Schottky drain," ***International Symposium on Power Semiconductor Devices and ICs (ISPSD)***, Chicago, USA, 2018.
36. J. Ma and E. Matioli, "1370 V tri-gate GaN MOSHEMTs on silicon substrate," ***International Conference on Nitride Semiconductors (ICNS)***, Strasbourg, France, 2017.
37. J. Ma and E. Matioli, "High-voltage AlGaN/GaN MOSHEMTs on silicon with slanted tri-gate structures," ***International Conference on Nitride Semiconductors (ICNS)***, Strasbourg, France, 2017. (Reported in *Compound Semiconductor*)
38. J. Ma and E. Matioli, "1.3 kV AlGaN/GaN nanowire-based Schottky barrier diodes with ultra-low leakage current," ***Compound Semiconductor Week (CSW)***, Berlin, 2017.

39. (Invited) J. Ma and E. Matioli, "Improved electrical and thermal performances in nanostructured GaN devices," ***International Conference on IC Design and Technology (ICICDT)***, Ho Chi Minh City, Vietnam, 2016.
40. J. Ma, X. Zhu, T. Huang, C. Liu, and K. M. Lau, "Improved buffer resistivity for GaN-based HEMTs with a medium-temperature and low-pressure GaN insertion layer," ***International Conference on Metal Organic Vapor Phase Epitaxy (ICMOVPE)***, Lausanne, Switzerland, 2014.
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49. C. Liu, Y. Cai, Z. Liu, J. Ma, and K. M. Lau, "Buffer structure optimization of monolithically integrated HEMT-LED using a metal-interconnection-free integration scheme," ***Electronic Materials Conference(EMC)***, Columbus, Ohio, USA, 2015.
50. X. Lu, J. Ma, P. Xu, H. Jiang, and K. M. Lau, "High Performance Self-aligned AlN/GaN MISHEMT with *In-situ* SiN_x Gate Dielectric and Regrown Source/Drain," ***International Conference on Compound Semiconductor Manufacturing Technology (CS MANTECH)***, Denver, USA, 2014.
51. X. Zou, W. C. Chong, K. M. Wong, J. Ma, and K. M. Lau, "Blue, green, and yellow LEDs grown on Si substrates", ***Asia Communications and Photonics Conference (ACP)***, Beijing, China, 2013.
52. X. Lu, J. Ma, X. Zhu, C. M. Lee, C. P. Yue and K. M. Lau, "A novel GaN-based monolithic SAW/HEMT oscillator on silicon," ***IEEE international Ultrasonics Symposium (IUS)***, Dresden, Germany, 2012.

Appendix-1: the growth recipe for the 10x-channel GaN heterostructure

```
read Macro_Library;

#################################################################
##      GENERAL INFORMATION
##      3x2 GaN CCS (EpiLab platform)
##      Edited by LL - 2012.10.31
##      Adapted from C1004 for n-GaN template (NG)
##      3um n-GaN comme 1149 dm
##
##      CAUTION: temperature setpoints are calculated in the core of the recipe
##      from variables defining expected surface temperatures
##      according to default Argus-based temperature calibration parameters
##
##      Bubbler conditions:
##      All of bubbler pressure set to 1300mbar except TMGa = 1900mbar
##      TMGa: 0C; 1900mbar
##      TMAl: 17C; 1300mbar
##      Cp2Mg: 25C; 1300mbar
##      TMIn: 25C; 1300mbar
##      TEGa: 17C; 1300mbar
#################################################################



#################################################################
##      VARIABLES DEFINITION
##
##      TEMPERATURE CALIBRATION
##      Parameters used to calculate setpoints
##      for the requested surface temperatures
```

```
#       T setting /Hydrogen, coated showerhead
        variable Tcal_H2_HT_Factor = 1.273;
        variable Tcal_H2_HT_Offset = -29.4;

#       Hydrogen, coated showerhead
        variable Tcal_H2_LT_Factor = 1.273;
        variable Tcal_H2_LT_Offset = -29.4;

#       T setting /Nitrogen, coated showerhead T<805C
        variable Tcal_N2_LT_Factor = 1.467;
        variable Tcal_N2_LT_Offset = -210;

#       Nitrogen, coated showerhead T>805C
        variable Tcal_N2_HT_Factor = 1.291;
        variable Tcal_N2_HT_Offset = -72.4;


#       Zone settings for temperatures under H2
        variable ZoneA_H2_LT_Factor = 0;
        variable ZoneA_H2_LT_Offset = 83;
        variable ZoneB_H2_LT_Factor = 0;
        variable ZoneB_H2_LT_Offset = 85;
        variable ZoneC_H2_LT_Factor = -0.037;
        variable ZoneC_H2_LT_Offset = 98.9;

#       Zone settings for temperatures under H2
        variable ZoneA_H2_HT_Factor = 0;
        variable ZoneA_H2_HT_Offset = 83;
        variable ZoneB_H2_HT_Factor = 0;
        variable ZoneB_H2_HT_Offset = 85;
        variable ZoneC_H2_HT_Factor = -0.037;
        variable ZoneC_H2_HT_Offset = 98.9;

#       Zone settings for Nucleation under H2
        variable ZoneA_H2_Nucl_Factor = 0;
        variable ZoneA_H2_Nucl_Offset = 83;
        variable ZoneB_H2_Nucl_Factor = 0;
        variable ZoneB_H2_Nucl_Offset = 85;
        variable ZoneC_H2_Nucl_Factor = 0;
```

```
        variable ZoneC_H2_Nucl_Offset = 63;

#       Zone settings for temperatures under N2 T<805
        variable ZoneA_N2_LT_Factor = 0.084;
        variable ZoneA_N2_LT_Offset = 6.8;
        variable ZoneB_N2_LT_Factor = 0;
        variable ZoneB_N2_LT_Offset = 85;
        variable ZoneC_N2_LT_Factor = 0;
        variable ZoneC_N2_LT_Offset = 52;

#       Zone settings for temperatures under N2 T>805
        variable ZoneA_N2_HT_Factor = 0.058;
        variable ZoneA_N2_HT_Offset = 24.5;
        variable ZoneB_N2_HT_Factor = 0;
        variable ZoneB_N2_HT_Offset = 85;
        variable ZoneC_N2_HT_Factor = 0;
        variable ZoneC_N2_HT_Offset = 56;

##      GENERAL GROWTH CONDTIONS
        variable Total_Flow = 8000;

##      SUBSTRATE PREPARATION
##      High-Temperature H2 Bake-out
        variable Bake_Temp = 1080;
        variable Bake_Time = 600;
        variable Bake_Press = 150; #Trine 100

###############################################################################################
Parameters for layers
###############################################################################################

##      AlN NUCLEATION LAYER
        variable Nitridation_Time = 180;
        variable Nucl_Time = 260;
        variable Nucl_Temp = 825;
        variable Nucl_Press = 100;
#       variable Nucl_Gap = 11;
        variable Nucl_NH3_Flow = 1200;
        variable Nucl_TMAl_Flow = 48;
```

```
##      AlN BUFFER
        variable AlN_buffer_TMAl_Flow = 50;
        variable AlN_buffer_temp_1 = 1000;
        variable AlN_buffer_temp_2 = 1020;
        variable AlN_buffer_Press = 100;
        variable AlN_buffer_Time_1 = 810;
        variable AlN_buffer_Time_2 = 810;
        variable AlN_buffer_NH3_1 = 1200;
        variable AlN_buffer_NH3_2 = 3000;
        variable Ramp_NH3 = 1500;

##      uGaN BUFFER
        variable uGaN_Time_1 = 750;
        variable uGaN_Time_2 = 4650;
        variable uGaN_Temp = 1050;
        variable uGaN_Press_1 = 200;
        variable uGaN_Press_2 = 200;
#       variable uGaN_Gap = 11;
        variable uGaN_NH3_Flow_1 = 2900;
        variable uGaN_NH3_Flow_2 = 2900;
        variable uGaN_TMGa_Flow = 50;

##      uGaN Channel
        variable channel_Time = 140;
        variable channel_Temp = 1050;
        variable channel_Press = 200;
        variable channel_NH3_Flow = 3300;
        variable channel_TMGa_Flow = 50;

##      AlGaN BARRIER
        variable Barrier_Time = 116;
        variable Spacer_Time = 18;
        variable Cap_Time = 5;
        variable Barrier_Temp = 1030;
        variable Barrier_Press = 150;
#       variable Barrier_Gap = 11;
        variable Barrier_NH3_Flow = 3500;
        variable Barrier_TMGa_Flow = 13;
        variable Barrier_TMAl_Flow = 42;
```

```
## STATISTICAL FUNCTIONS
Main_Stat = Position dP_Filter HygrometerN2 HygrometerH2;
GaN_Stat = TMGa_1.source NH3_1.source TMGa_1.press SumMO SumHydride Reactor.press Heater.temp Heater.percent ZoneAVoltage ZoneACurrent ZoneBVoltage ZoneBCurrent ZoneCVoltage ZoneCCurrent;
##########################################

layer {

    1   begin stat Main_Stat;

        BathCheck;
        BaseState;
        CyclePurge;
#       DORCheck;
        DewpointCheck;
        until MaintenanceMode == 0;
        until ShowerheadOutCooling.temp >> 42;

    1   "Gas Manifold Selection",
        H2_Hyd.supply = open,
        N2_Hyd.supply = close,
        H2_Run.supply = open,
        N2_Run.supply = close,
        H2_Blend.supply = open,
        N2_Blend.supply = close,
        H2_MO1.supply = open,
        N2_MO1.supply = close,
        H2_MO2.supply = close,
        N2_MO2.supply = open,
        Liner.switch = open,
        Heater.switch = open,
        Vent.vac = open;

        until Vent.vac == open;

    10  "System Devices",
```

```
        MainPump.power = open,
        Exhaust.vac = open,
        Control = on,
        Pump.bypass2 = open,
        Heater.power = on,
        Rot.speed to 60,
        Cooling.main = on;

10      "Ramping purges, flows and pressure",

        DP_MO1.mode = off,
        Reactor.press to Bake_Press in 240,
        Optical.purge to (Total_Flow/80) in 240,
        Liner.purge to (Total_Flow/16) in 240,
        Heater.purge to (Total_Flow/2.5) in 240,
        RunHyd1.feed1 to (Total_Flow/2) in 240,
        Blend.feed1 to (Total_Flow/4) in 240,
        RunMO1.feed1 to (Total_Flow/4-200) in 240,
        RunHyd1.vent to 500,
        RunMO1.vent to 500,
        DummyMO1.source to 200,
        DummyMO_1.run = on;

SoftStartHeating;

250     "Heating up Reactor to 500°C",
        Heater.temp to 500,
        HeaterzoneA.factor to (500*ZoneA_H2_LT_Factor +ZoneA_H2_LT_Offset),
        HeaterzoneB.factor to (500*ZoneB_H2_LT_Factor +ZoneB_H2_LT_Offset),
        HeaterzoneC.factor to (500*ZoneC_H2_LT_Factor +ZoneC_H2_LT_Offset),
        TMGa_1.push follow (100 - TMGa_1.source),
        TMAl_1.push follow (200 - TMAl_1.source);

480     "Heating up Reactor to bake-out temperature",
        Heater.temp to (Bake_Temp*Tcal_H2_HT_Factor + Tcal_H2_HT_Offset),
        HeaterzoneA.factor to (Bake_Temp*ZoneA_H2_HT_Factor +ZoneA_H2_HT_Offset),
        HeaterzoneB.factor to (Bake_Temp*ZoneB_H2_HT_Factor +ZoneB_H2_HT_Offset),
```

```
        HeaterzoneC.factor to (Bake_Temp*ZoneC_H2_HT_Factor +ZoneC_H2_HT_Offset);


    [Bake_Time]
        "Bake-out";

    60  Heater.temp to ((Bake_Temp*Tcal_H2_HT_Factor + Tcal_H2_HT_Offset) -15),
        NH3_1.line = open,
        NH3_1.source = 500;

##############################################################################################
Nitridation
##############################################################################################

    180 "Begin reducing temp to Nucleation",
        Heater.temp to 870,
        Reactor.press to ((Nucl_Press + Bake_Press)/2);
#       GapPosition to Nucl_Gap;


    360 Heater.temp to ((Nucl_Temp*Tcal_H2_LT_Factor + Tcal_H2_LT_Offset) + 15),
        Reactor.press to Nucl_Press,
        TMAl_1.line = open,
        TMAl_1.source to Nucl_TMAl_Flow;

    15  Heater.temp to ((Nucl_Temp*Tcal_H2_LT_Factor + Tcal_H2_LT_Offset)),
        HeaterzoneA.factor to (Bake_Temp*ZoneA_H2_Nucl_Factor + ZoneA_H2_Nucl_Offset),
        HeaterzoneB.factor to (Bake_Temp*ZoneB_H2_Nucl_Factor + ZoneB_H2_Nucl_Offset),
        HeaterzoneC.factor to (Bake_Temp*ZoneC_H2_Nucl_Factor + ZoneC_H2_Nucl_Offset);

    120 "Temperature stabilization",
        NH3_1.source to Nucl_NH3_Flow,
        RunHyd1.feed1 to (Total_Flow/2 - Nucl_NH3_Flow);

##############################################################################################
Nulceation
##############################################################################################

    [Nucl_Time]
        "Nucleation layer",# should reach 2.5x initial reflectance of sapphire
```

```
                begin stat GaN_Stat,
                TMAl_1.run = open,
                NH3_1.run = open,
                DummyMO_1.run = close;

        ##########################################################################################
        AlN buffer
        ##########################################################################################

            10      "Ramping to AlN buffer layers",
                    end stat GaN_Stat,
                    Heater.temp to ((Nucl_Temp*Tcal_H2_LT_Factor + Tcal_H2_LT_Offset) + 10),
                    TMAl_1.run = close,
                    DummyMO_1.run = open,
                    NH3_1.source to Ramp_NH3,
                    RunHyd1.feed1 to (Total_Flow/2 - Ramp_NH3);

            155     Heater.temp to ((AlN_buffer_temp_1*Tcal_H2_HT_Factor + Tcal_H2_LT_Offset) ),
                    HeaterzoneA.factor to (AlN_buffer_temp_1*ZoneA_H2_HT_Factor +ZoneA_H2_HT_Off-
set),
                    HeaterzoneB.factor to (AlN_buffer_temp_1*ZoneB_H2_HT_Factor +ZoneB_H2_HT_Off-
set),
                    HeaterzoneC.factor to (AlN_buffer_temp_1*ZoneC_H2_HT_Factor +ZoneC_H2_HT_Off-
set),
                    TMAl_1.source to AlN_buffer_TMAl_Flow;

            15      "Setting Growth Conditions",
                    Reactor.press to AlN_buffer_Press,
                    NH3_1.source to AlN_buffer_NH3_1,
                    RunHyd1.feed1 to (Total_Flow/2 - AlN_buffer_NH3_1);

        [AlN_buffer_Time_1-540]
                    "1st HT-AlN buffer growth", begin stat GaN_Stat,
                    TMAl_1.run = open,
                    DummyMO_1.run = close;

            60      Heater.temp to ((AlN_buffer_temp_2*Tcal_H2_HT_Factor + Tcal_H2_LT_Offset) ),
                    HeaterzoneA.factor to (AlN_buffer_temp_2*ZoneA_H2_HT_Factor +ZoneA_H2_HT_Off-
set),
                    HeaterzoneB.factor to (AlN_buffer_temp_2*ZoneB_H2_HT_Factor +ZoneB_H2_HT_Off-
set),
```

```
                HeaterzoneC.factor to (AlN_buffer_temp_2*ZoneC_H2_HT_Factor +ZoneC_H2_HT_Off-
set),
                TMAl_1.source to AlN_buffer_TMAl_Flow;

        480     "Growth of 1st AlN buffer";

        [AlN_buffer_Time_2-240]
                "2nd HT-AlN buffer growth",
                NH3_1.source to AlN_buffer_NH3_2,
                RunHyd1.feed1 to (Total_Flow/2 - AlN_buffer_NH3_2);

        120     TMGa_1.line = open,
                TMGa_1.source to uGaN_TMGa_Flow;

    ##############################################################################################
    u-GaN buffer
    ##############################################################################################

        120     "Ramping to u-GaN layer",
                end stat GaN_Stat,
                Heater.temp to ((uGaN_Temp*Tcal_H2_HT_Factor + Tcal_H2_HT_Offset)),
                NH3_1.source to uGaN_NH3_Flow_1,
                RunHyd1.feed1 to (Total_Flow/2 - uGaN_NH3_Flow_1);

        [uGaN_Time_1-90]
                begin stat GaN_Stat,
                Heater.temp to ((uGaN_Temp*Tcal_H2_HT_Factor) + Tcal_H2_HT_Offset),
                HeaterzoneA.factor to (uGaN_Temp*ZoneA_H2_HT_Factor +ZoneA_H2_HT_Offset),
                HeaterzoneB.factor to (uGaN_Temp*ZoneB_H2_HT_Factor +ZoneB_H2_HT_Offset),
                HeaterzoneC.factor to (uGaN_Temp*ZoneC_H2_HT_Factor +ZoneC_H2_HT_Offset),
                TMGa_1.run = open,
                TMAl_1.run = close,
                TMAl_1.line = close,
                DummyMO_1.run = close;

        90      Reactor.press to uGaN_Press_2,
                NH3_1.source to uGaN_NH3_Flow_2,
                RunHyd1.feed1 to (Total_Flow/2 - uGaN_NH3_Flow_1);

        [uGaN_Time_2-300]
```

```
        "uGaN Growth";

    300 TMAl_1.line = on,
        TMAl_1.source to Barrier_TMAl_Flow,
        TMAl_1.push follow (200 - TMAl_1.source);

##########################################################################################
1st AlGaN barrier
##########################################################################################

    90  "Ramp to 1 AlGaN barrier",
        TMGa_1.run = off,
        DummyMO_1.run = on,
        DummyMO_2.run = on,
        Heater.temp to ((Barrier_Temp*Tcal_H2_HT_Factor) + Tcal_H2_HT_Offset),
        HeaterzoneA.factor to (Barrier_Temp*ZoneA_H2_HT_Factor +ZoneA_H2_HT_Offset),
        HeaterzoneB.factor to (Barrier_Temp*ZoneB_H2_HT_Factor +ZoneB_H2_HT_Offset),
        HeaterzoneC.factor to (Barrier_Temp*ZoneC_H2_HT_Factor +ZoneC_H2_HT_Offset),
        Reactor.press to Barrier_Press,
        NH3_1.source to Barrier_NH3_Flow,
        RunHyd1.feed1 to (Total_Flow/2 - Barrier_NH3_Flow),
        TMGa_1.source to Barrier_TMGa_Flow,
        TMAl_1.source to Barrier_TMAl_Flow,
        DummyMO1.source to 200,
        DummyMO2.source to 100,
        RunMO1.feed1 follow (Total_Flow/4 - 300);

    10  "Stablize";

[Spacer_Time]   TMAl_1.run = on,
        DummyMO_1.run = off;

[Barrier_Time]  TMGa_1.run = on,
        DummyMO_2.run = off;

[Cap_Time] TMAl_1.run = off,
        DummyMO_1.run = on;

##########################################################################################
```

```
2nd GaN channel
##############################################################################################

        90      "Ramping to 2 channel layer",
                end stat GaN_Stat,
                TMGa_1.run = off,
                DummyMO_1.run = on,
                Heater.temp to ((channel_Temp*Tcal_H2_HT_Factor + Tcal_H2_HT_Offset)),
                NH3_1.source to channel_NH3_Flow,
                Reactor.press to channel_Press,
                TMGa_1.source to channel_TMGa_Flow,
                RunHyd1.feed1 to (Total_Flow/2 - channel_NH3_Flow);

        5       "Stablization";

        [channel_Time]  begin stat GaN_Stat,
                TMGa_1.run = on,
                DummyMO_1.run = off;

##############################################################################################
2nd AlGaN barrier
##############################################################################################

        90      "Ramp to 2 AlGaN barrier",
                TMGa_1.run = off,
                DummyMO_1.run = on,
                DummyMO_2.run = on,
                Heater.temp to ((Barrier_Temp*Tcal_H2_HT_Factor) + Tcal_H2_HT_Offset),
                HeaterzoneA.factor to (Barrier_Temp*ZoneA_H2_HT_Factor +ZoneA_H2_HT_Offset),
                HeaterzoneB.factor to (Barrier_Temp*ZoneB_H2_HT_Factor +ZoneB_H2_HT_Offset),
                HeaterzoneC.factor to (Barrier_Temp*ZoneC_H2_HT_Factor +ZoneC_H2_HT_Offset),
                Reactor.press to Barrier_Press,
                NH3_1.source to Barrier_NH3_Flow,
                RunHyd1.feed1 to (Total_Flow/2 - Barrier_NH3_Flow),
                TMGa_1.source to Barrier_TMGa_Flow,
                TMAl_1.source to Barrier_TMAl_Flow,
                DummyMO1.source to 200,
                DummyMO2.source to 100,
                RunMO1.feed1 follow (Total_Flow/4 - 300);
```

```
10      "Stablize";

[Spacer_Time]   TMAl_1.run = on,
                DummyMO_1.run = off;

[Barrier_Time]  TMGa_1.run = on,
                DummyMO_2.run = off;

[Cap_Time] TMAl_1.run = off,
                DummyMO_1.run = on;

##############################################################################################
3rd GaN channel
##############################################################################################


90      "Ramping to 3 channel layer",
                end stat GaN_Stat,
                TMGa_1.run = off,
                DummyMO_1.run = on,
                Heater.temp to ((channel_Temp*Tcal_H2_HT_Factor + Tcal_H2_HT_Offset)),
                NH3_1.source to channel_NH3_Flow,
                Reactor.press to channel_Press,
                TMGa_1.source to channel_TMGa_Flow,
                RunHyd1.feed1 to (Total_Flow/2 - channel_NH3_Flow);

5       "Stablization";

[channel_Time]  begin stat GaN_Stat,
                TMGa_1.run = on,
                DummyMO_1.run = off;

##############################################################################################
3rd AlGaN barrier
##############################################################################################

90      "Ramp to 3 AlGaN barrier",
                TMGa_1.run = off,
```

```
                DummyMO_1.run = on,
                DummyMO_2.run = on,
                Heater.temp to ((Barrier_Temp*Tcal_H2_HT_Factor) + Tcal_H2_HT_Offset),
                HeaterzoneA.factor to (Barrier_Temp*ZoneA_H2_HT_Factor +ZoneA_H2_HT_Offset),
                HeaterzoneB.factor to (Barrier_Temp*ZoneB_H2_HT_Factor +ZoneB_H2_HT_Offset),
                HeaterzoneC.factor to (Barrier_Temp*ZoneC_H2_HT_Factor +ZoneC_H2_HT_Offset),
                Reactor.press to Barrier_Press,
                NH3_1.source to Barrier_NH3_Flow,
                RunHyd1.feed1 to (Total_Flow/2 - Barrier_NH3_Flow),
                TMGa_1.source to Barrier_TMGa_Flow,
                TMAl_1.source to Barrier_TMAl_Flow,
                DummyMO1.source to 200,
                DummyMO2.source to 100,
                RunMO1.feed1 follow (Total_Flow/4 - 300);

        10      "Stablize";

        [Spacer_Time]   TMAl_1.run = on,
                DummyMO_1.run = off;

        [Barrier_Time]  TMGa_1.run = on,
                DummyMO_2.run = off;

        [Cap_Time] TMAl_1.run = off,
                DummyMO_1.run = on;

##############################################################################################
4th GaN channel
##############################################################################################


        90      "Ramping to 4 channel layer",
                end stat GaN_Stat,
                TMGa_1.run = off,
                DummyMO_1.run = on,
                Heater.temp to ((channel_Temp*Tcal_H2_HT_Factor + Tcal_H2_HT_Offset)),
                NH3_1.source to channel_NH3_Flow,
                Reactor.press to channel_Press,
                TMGa_1.source to channel_TMGa_Flow,
                RunHyd1.feed1 to (Total_Flow/2 - channel_NH3_Flow);
```

```
        5       "Stablization";

        [channel_Time]  begin stat GaN_Stat,
                TMGa_1.run = on,
                DummyMO_1.run = off;

##########################################################################################
4th AlGaN barrier
##########################################################################################

        90      "Ramp to 4 AlGaN barrier",
                TMGa_1.run = off,
                DummyMO_1.run = on,
                DummyMO_2.run = on,
                Heater.temp to ((Barrier_Temp*Tcal_H2_HT_Factor) + Tcal_H2_HT_Offset),
                HeaterzoneA.factor to (Barrier_Temp*ZoneA_H2_HT_Factor +ZoneA_H2_HT_Offset),
                HeaterzoneB.factor to (Barrier_Temp*ZoneB_H2_HT_Factor +ZoneB_H2_HT_Offset),
                HeaterzoneC.factor to (Barrier_Temp*ZoneC_H2_HT_Factor +ZoneC_H2_HT_Offset),
                Reactor.press to Barrier_Press,
                NH3_1.source to Barrier_NH3_Flow,
                RunHyd1.feed1 to (Total_Flow/2 - Barrier_NH3_Flow),
                TMGa_1.source to Barrier_TMGa_Flow,
                TMAl_1.source to Barrier_TMAl_Flow,
                DummyMO1.source to 200,
                DummyMO2.source to 100,
                RunMO1.feed1 follow (Total_Flow/4 - 300);

        10      "Stablize";

        [Spacer_Time]   TMAl_1.run = on,
                DummyMO_1.run = off;

        [Barrier_Time]  TMGa_1.run = on,
                DummyMO_2.run = off;

        [Cap_Time] TMAl_1.run = off,
                DummyMO_1.run = on;
```

```
##############################################################################################
5th GaN channel
##############################################################################################

        90      "Ramping to 5 channel layer",
                end stat GaN_Stat,
                TMGa_1.run = off,
                DummyMO_1.run = on,
                Heater.temp to ((channel_Temp*Tcal_H2_HT_Factor + Tcal_H2_HT_Offset)),
                NH3_1.source to channel_NH3_Flow,
                Reactor.press to channel_Press,
                TMGa_1.source to channel_TMGa_Flow,
                RunHyd1.feed1 to (Total_Flow/2 - channel_NH3_Flow);

        5       "Stablization";

        [channel_Time]   begin stat GaN_Stat,
                TMGa_1.run = on,
                DummyMO_1.run = off;

##############################################################################################
5th AlGaN barrier
##############################################################################################

        90      "Ramp to 5 AlGaN barrier",
                TMGa_1.run = off,
                DummyMO_1.run = on,
                DummyMO_2.run = on,
                Heater.temp to ((Barrier_Temp*Tcal_H2_HT_Factor) + Tcal_H2_HT_Offset),
                HeaterzoneA.factor to (Barrier_Temp*ZoneA_H2_HT_Factor +ZoneA_H2_HT_Offset),
                HeaterzoneB.factor to (Barrier_Temp*ZoneB_H2_HT_Factor +ZoneB_H2_HT_Offset),
                HeaterzoneC.factor to (Barrier_Temp*ZoneC_H2_HT_Factor +ZoneC_H2_HT_Offset),
                Reactor.press to Barrier_Press,
                NH3_1.source to Barrier_NH3_Flow,
                RunHyd1.feed1 to (Total_Flow/2 - Barrier_NH3_Flow),
                TMGa_1.source to Barrier_TMGa_Flow,
                TMAl_1.source to Barrier_TMAl_Flow,
                DummyMO1.source to 200,
                DummyMO2.source to 100,
```

```
        RunMO1.feed1 follow (Total_Flow/4 - 300);

    10  "Stablize";

    [Spacer_Time]   TMAl_1.run = on,
        DummyMO_1.run = off;

    [Barrier_Time]  TMGa_1.run = on,
        DummyMO_2.run = off;

    [Cap_Time] TMAl_1.run = off,
        DummyMO_1.run = on;

################################################################################################
6th GaN channel
################################################################################################

    90  "Ramping to 6 channel layer",
        end stat GaN_Stat,
        TMGa_1.run = off,
        DummyMO_1.run = on,
        Heater.temp to ((channel_Temp*Tcal_H2_HT_Factor + Tcal_H2_HT_Offset)),
        NH3_1.source to channel_NH3_Flow,
        Reactor.press to channel_Press,
        TMGa_1.source to channel_TMGa_Flow,
        RunHyd1.feed1 to (Total_Flow/2 - channel_NH3_Flow);

    5   "Stablization";

    [channel_Time]  begin stat GaN_Stat,
        TMGa_1.run = on,
        DummyMO_1.run = off;

################################################################################################
6th AlGaN barrier
################################################################################################

    90  "Ramp to 6 AlGaN barrier",
        TMGa_1.run = off,
```

```
            DummyMO_1.run = on,
            DummyMO_2.run = on,
            Heater.temp to ((Barrier_Temp*Tcal_H2_HT_Factor) + Tcal_H2_HT_Offset),
            HeaterzoneA.factor to (Barrier_Temp*ZoneA_H2_HT_Factor +ZoneA_H2_HT_Offset),
            HeaterzoneB.factor to (Barrier_Temp*ZoneB_H2_HT_Factor +ZoneB_H2_HT_Offset),
            HeaterzoneC.factor to (Barrier_Temp*ZoneC_H2_HT_Factor +ZoneC_H2_HT_Offset),
            Reactor.press to Barrier_Press,
            NH3_1.source to Barrier_NH3_Flow,
            RunHyd1.feed1 to (Total_Flow/2 - Barrier_NH3_Flow),
            TMGa_1.source to Barrier_TMGa_Flow,
            TMAl_1.source to Barrier_TMAl_Flow,
            DummyMO1.source to 200,
            DummyMO2.source to 100,
            RunMO1.feed1 follow (Total_Flow/4 - 300);

      10    "Stablize";

      [Spacer_Time]   TMAl_1.run = on,
            DummyMO_1.run = off;

      [Barrier_Time]  TMGa_1.run = on,
            DummyMO_2.run = off;

      [Cap_Time] TMAl_1.run = off,
            DummyMO_1.run = on;

##########################################################################################
10th GaN channel
##########################################################################################

      90    "Ramping to 7 channel layer",
            end stat GaN_Stat,
            TMGa_1.run = off,
            DummyMO_1.run = on,
            Heater.temp to ((channel_Temp*Tcal_H2_HT_Factor + Tcal_H2_HT_Offset)),
            NH3_1.source to channel_NH3_Flow,
            Reactor.press to channel_Press,
            TMGa_1.source to channel_TMGa_Flow,
            RunHyd1.feed1 to (Total_Flow/2 - channel_NH3_Flow);
```

```
        5       "Stablization";

        [channel_Time]  begin stat GaN_Stat,
                TMGa_1.run = on,
                DummyMO_1.run = off;

    ##########################################################################################
    7th AlGaN barrier
    ##########################################################################################

        90      "Ramp to 7 AlGaN barrier",
                TMGa_1.run = off,
                DummyMO_1.run = on,
                DummyMO_2.run = on,
                Heater.temp to ((Barrier_Temp*Tcal_H2_HT_Factor) + Tcal_H2_HT_Offset),
                HeaterzoneA.factor to (Barrier_Temp*ZoneA_H2_HT_Factor +ZoneA_H2_HT_Offset),
                HeaterzoneB.factor to (Barrier_Temp*ZoneB_H2_HT_Factor +ZoneB_H2_HT_Offset),
                HeaterzoneC.factor to (Barrier_Temp*ZoneC_H2_HT_Factor +ZoneC_H2_HT_Offset),
                Reactor.press to Barrier_Press,
                NH3_1.source to Barrier_NH3_Flow,
                RunHyd1.feed1 to (Total_Flow/2 - Barrier_NH3_Flow),
                TMGa_1.source to Barrier_TMGa_Flow,
                TMAl_1.source to Barrier_TMAl_Flow,
                DummyMO1.source to 200,
                DummyMO2.source to 100,
                RunMO1.feed1 follow (Total_Flow/4 - 300);

        10      "Stablize";

        [Spacer_Time]   TMAl_1.run = on,
                DummyMO_1.run = off;

        [Barrier_Time]  TMGa_1.run = on,
                DummyMO_2.run = off;

        [Cap_Time] TMAl_1.run = off,
                DummyMO_1.run = on;
    ##########################################################################################
```

```
8th GaN channel
##############################################################################################

        90      "Ramping to 8 channel layer",
                end stat GaN_Stat,
                TMGa_1.run = off,
                DummyMO_1.run = on,
                Heater.temp to ((channel_Temp*Tcal_H2_HT_Factor + Tcal_H2_HT_Offset)),
                NH3_1.source to channel_NH3_Flow,
                Reactor.press to channel_Press,
                TMGa_1.source to channel_TMGa_Flow,
                RunHyd1.feed1 to (Total_Flow/2 - channel_NH3_Flow);

        5       "Stablization";

        [channel_Time]  begin stat GaN_Stat,
                TMGa_1.run = on,
                DummyMO_1.run = off;

##############################################################################################
8th AlGaN barrier
##############################################################################################

        90      "Ramp to 8 AlGaN barrier",
                TMGa_1.run = off,
                DummyMO_1.run = on,
                DummyMO_2.run = on,
                Heater.temp to ((Barrier_Temp*Tcal_H2_HT_Factor) + Tcal_H2_HT_Offset),
                HeaterzoneA.factor to (Barrier_Temp*ZoneA_H2_HT_Factor +ZoneA_H2_HT_Offset),
                HeaterzoneB.factor to (Barrier_Temp*ZoneB_H2_HT_Factor +ZoneB_H2_HT_Offset),
                HeaterzoneC.factor to (Barrier_Temp*ZoneC_H2_HT_Factor +ZoneC_H2_HT_Offset),
                Reactor.press to Barrier_Press,
                NH3_1.source to Barrier_NH3_Flow,
                RunHyd1.feed1 to (Total_Flow/2 - Barrier_NH3_Flow),
                TMGa_1.source to Barrier_TMGa_Flow,
                TMAl_1.source to Barrier_TMAl_Flow,
                DummyMO1.source to 200,
                DummyMO2.source to 100,
                RunMO1.feed1 follow (Total_Flow/4 - 300);
```

```
        10      "Stablize";

        [Spacer_Time]   TMAl_1.run = on,
                DummyMO_1.run = off;

        [Barrier_Time]  TMGa_1.run = on,
                DummyMO_2.run = off;

        [Cap_Time] TMAl_1.run = off,
                DummyMO_1.run = on;

    ##########################################################################################
    9th GaN channel
    ##########################################################################################


        90      "Ramping to 9 channel layer",
                end stat GaN_Stat,
                TMGa_1.run = off,
                DummyMO_1.run = on,
                Heater.temp to ((channel_Temp*Tcal_H2_HT_Factor + Tcal_H2_HT_Offset)),
                NH3_1.source to channel_NH3_Flow,
                Reactor.press to channel_Press,
                TMGa_1.source to channel_TMGa_Flow,
                RunHyd1.feed1 to (Total_Flow/2 - channel_NH3_Flow);

        5       "Stablization";

        [channel_Time]  begin stat GaN_Stat,
                TMGa_1.run = on,
                DummyMO_1.run = off;

    ##########################################################################################
    9th AlGaN barrier
    ##########################################################################################

        90      "Ramp to 9 AlGaN barrier",
                TMGa_1.run = off,
```

```
                DummyMO_1.run = on,
                DummyMO_2.run = on,
                Heater.temp to ((Barrier_Temp*Tcal_H2_HT_Factor) + Tcal_H2_HT_Offset),
                HeaterzoneA.factor to (Barrier_Temp*ZoneA_H2_HT_Factor +ZoneA_H2_HT_Offset),
                HeaterzoneB.factor to (Barrier_Temp*ZoneB_H2_HT_Factor +ZoneB_H2_HT_Offset),
                HeaterzoneC.factor to (Barrier_Temp*ZoneC_H2_HT_Factor +ZoneC_H2_HT_Offset),
                Reactor.press to Barrier_Press,
                NH3_1.source to Barrier_NH3_Flow,
                RunHyd1.feed1 to (Total_Flow/2 - Barrier_NH3_Flow),
                TMGa_1.source to Barrier_TMGa_Flow,
                TMAl_1.source to Barrier_TMAl_Flow,
                DummyMO1.source to 200,
                DummyMO2.source to 100,
                RunMO1.feed1 follow (Total_Flow/4 - 300);

        10      "Stablize";

        [Spacer_Time]   TMAl_1.run = on,
                DummyMO_1.run = off;

        [Barrier_Time]  TMGa_1.run = on,
                DummyMO_2.run = off;

        [Cap_Time] TMAl_1.run = off,
                DummyMO_1.run = on;

##############################################################################################
10th GaN channel
##############################################################################################


        90      "Ramping to 10 channel layer",
                end stat GaN_Stat,
                TMGa_1.run = off,
                DummyMO_1.run = on,
                Heater.temp to ((channel_Temp*Tcal_H2_HT_Factor + Tcal_H2_HT_Offset)),
                NH3_1.source to channel_NH3_Flow,
                Reactor.press to channel_Press,
                TMGa_1.source to channel_TMGa_Flow,
                RunHyd1.feed1 to (Total_Flow/2 - channel_NH3_Flow);
```

```
        5       "Stablization";

        [channel_Time]  begin stat GaN_Stat,
                TMGa_1.run = on,
                DummyMO_1.run = off;

##########################################################################################
10th AlGaN barrier
##########################################################################################

        90      "Ramp to 10 AlGaN barrier",
                TMGa_1.run = off,
                DummyMO_1.run = on,
                DummyMO_2.run = on,
                Heater.temp to ((Barrier_Temp*Tcal_H2_HT_Factor) + Tcal_H2_HT_Offset),
                HeaterzoneA.factor to (Barrier_Temp*ZoneA_H2_HT_Factor +ZoneA_H2_HT_Offset),
                HeaterzoneB.factor to (Barrier_Temp*ZoneB_H2_HT_Factor +ZoneB_H2_HT_Offset),
                HeaterzoneC.factor to (Barrier_Temp*ZoneC_H2_HT_Factor +ZoneC_H2_HT_Offset),
                Reactor.press to Barrier_Press,
                NH3_1.source to Barrier_NH3_Flow,
                RunHyd1.feed1 to (Total_Flow/2 - Barrier_NH3_Flow),
                TMGa_1.source to Barrier_TMGa_Flow,
                TMAl_1.source to Barrier_TMAl_Flow,
                DummyMO1.source to 200,
                DummyMO2.source to 100,
                RunMO1.feed1 follow (Total_Flow/4 - 300);

        10      "Stablize";

        [Spacer_Time]   TMAl_1.run = on,
                DummyMO_1.run = off;

        [Barrier_Time]  TMGa_1.run = on,
                DummyMO_2.run = off;

        [Cap_Time] TMAl_1.run = off,
                DummyMO_1.run = on;
```

```
# Toxics off

        2       "Toxic off",
                TEGa_1.line = off,
                TEGa_1.run = off,
                TMIn_1.run = off,
                TMIn_1.line = off,
                TMGa_1.run = close,
                TMGa_1.line = close,
                TMAl_1.run = close,
                TMAl_1.line = close,
                Cp2Mg_1.run = close,
                Cp2Mg_1.line = close,
                N2_Run.supply = close,
                H2_Run.supply = open,
                N2_Hyd.supply = close,
                H2_Hyd.supply = open,
                N2_Blend.supply = close,
                H2_Blend.supply = open,
        #       N2_Vent.supply = close,
        #       H2_Vent.supply = open,
                N2_MO1.supply = open,
                H2_MO1.supply = close,
                N2_MO2.supply = open,
                H2_MO2.supply = close,
                Liner.switch = on,
                Heater.switch = on;


# End
        2       "Toxics off",
                end stat GaN_Stat,
                TMGa_1.run = off,
                TMGa_1.line = off,
                Cp2Mg_1.run = off,
                Cp2Mg_1.line = off,
                SiH4_1.run = off,
                SiH4_1.line = off,
                TMAl_1.run= off,
                TMAl_1.line=off,
```

```
                TMGa_1.source to default,
                TMGa_1.push to default,
                TMAl_1.source to default,
                TMAl_1.push to default,
                Cp2Mg_1.source to default,
                Cp2Mg_1.push to default,
                RunMO1.feed1 = (Total_Flow/4);

        420     "Start cooling reactor",
                NH3_1.source to default,
                Heater.temp to 500;



                CoolDownb;
                BaseState;
                CyclePurge;
                BaseState;

        1       end stat Main_Stat;
}
```

Appendix-2: the code for the ATLAS simulation of SBDs

```
# (c) Silvaco Inc., 2015
#
# ganfetex02.in
#
# In this deck the goal is to examine the breakdown voltage as a function
# of field plate geometry.
#
# This deck is based on Karmalkar and Mishra, ED 48, pp 1515-1521,
# August 2001
#

go internal

########################################################################
VARIABLES
########################################################################

# initial field plate length
set L_FP=2

# thickness of dielectric below the field plate
set t_FP=0.02

# thickness of passivation
set t_PS=0.1

# Anode length
set L_A=1

# Anode-to-Cathode distance
set L_AC=5

# Cathode length
set L_C=1

# AlGaN barrier composition
set x_AlGaN=0.25

# AlGaN barrier thickness
```

```
set t_AlGaN=0.02

# GaN channel thickness
set t_GaN_channel=0.02

# GaN buffer thickness
set t_GaN_buffer=0.18

#set eps0=8.9 - 0.4*$xc

# polarization charge density if set manually
#set ch1=1e13


##############################################################################
MESH
##############################################################################

# x grids: the right-side edge of each region. GS respresents the region between source and gate, similar to GD.
set x_A = $L_A
set x_FP = $x_A + $L_FP
set x_AC = $x_A + $L_AC
set x_C = $x_AC + $L_C

# y grids: the bottom of each region. GS respresents the region between source and gate.
set y_PS = $t_PS
set y_FP = $y_PS + $t_FP
set y_AlGaN = $y_FP + $t_AlGaN
set y_GaN_channel = $y_AlGaN + $t_GaN_channel
set y_GaN_buffer = $y_GaN_channel + $t_GaN_buffer

go atlas

mesh width=1000

# x mesh geometry
x.m l=0.0 s=0.5
x.m l=$x_A s=0.025
x.m l=($x_FP+$L_A)/2 s=0.05
x.m l=$x_FP s=0.025
x.m l=$x_AC s=0.05
x.m l=$x_C s=0.05

# y mesh geometry
y.m l=0.0 s=0.1
y.m l=$y_PS s=0.1
y.m l=$y_FP s=0.001
```

```
y.m l=$y_AlGaN s=0.001
y.m l=$y_GaN_channel s=0.01
y.m l=$y_GaN_buffer s=0.05

###############################################################################
REGIONS AND MATERIALs
###############################################################################
# device structure
# POLAR.SCALE is chosen to match calibrated values of 2DEG charge concentration

#define the dielectric and semiconductor
region num=1 mat=air x.min=0 x.max=$x_C y.min=0 y.max=$y_GaN_buffer
region num=2 mat=sapphire x.min=0 x.max=$x_AC y.min=$y_PS y.max=$y_FP
region num=3 mat=AlGaN x.min=$x_A x.max=$x_C y.min=$y_FP y.max=$y_AlGaN donors=1e16 x.comp=$x_Al-
GaN polarization calc.strain polar.scale=0.85
region num=4 mat=GaN x.min=$x_A x.max=$x_C y.min=$y_AlGaN y.max=$y_GaN_channel donors=1e15 polariza-
tion calc.strain polar.scale=1
region num=5 mat=GaN x.min=0 x.max=$x_C y.min=$y_GaN_channel y.max=$y_GaN_buffer donors=5e16 polariza-
tion calc.strain polar.scale=1 substrate



###############################################################################
ELECTRODES
###############################################################################

#define the electrodes
elect name=cathode x.min=$x_AC x.max=$x_C y.min=$y_PS y.max=$y_FP
elect name=anode x.min=0 x.max=$x_A y.min=$y_PS y.max=$y_GaN_channel
elect name=anode x.min=0 x.max=$x_FP y.min=$y_PS y.max=$y_PS

contact name=anode work=5.25
contact name=cathode work=4.04

###############################################################################
DOPING AND MOBILITY
###############################################################################

mobility region=4 albrct.n
mobility region=5 albrct.n
#mobility region=5 fmct.n
#mobility region=5 GaNsat.n

#doping donor conc=5e16 uniform region=3
#doping donor conc=5e16 uniform region=4

inttrap donor e.level=3.23 density=1e13 degen.fac=2 sign=1e-12 sigp=1e-12 \
      intmaterial="sapphire/AlGaN"
```

```
output con.band val.band band.param charge e.mob h.mob flowlines qss


###############################################################################
FORWARD CURVE
###############################################################################

solve

log outf=forward.log
solve vcathode=0
solve vstep=0.2 vfinal=0 name=anode
solve vstep=0.1 vfinal=3 name=anode
log off

save outfile=forward.str

extract init infile="forward.log"
extract name="Von" xintercept(maxslope(curve(v."anode",i."anode")))


###############################################################################
LEKAGE CURVE
###############################################################################

#method autonr gcarr.itlimit=10 clim.dd=1e3 clim.eb=1e3 nblockit=25
solve init
#
solve nsteps=10 vfinal=0 name=anode

log outf=reverse.log

solve  vstep=-0.1 vfinal=-1  name=anode
save outfile=reverse_2.str
solve  vstep=-0.2 vfinal=-4  name=anode
save outfile=reverse_4.str
solve  vstep=-0.2 vfinal=-6  name=anode
save outfile=reverse_6.str
solve  vstep=-0.2 vfinal=-8  name=anode
save outfile=reverse_8.str
solve  vstep=-0.2 vfinal=-10  name=anode
#save outfile=reverse_10.str
solve  vstep=-0.5 vfinal=-12  name=anode
save outfile=reverse_12.str
solve  vstep=-0.5 vfinal=-14  name=anode
save outfile=reverse_14.str
solve  vstep=-0.5 vfinal=-16  name=anode
```

```
save outfile=reverse_16.str
solve  vstep=-0.5 vfinal=-18  name=anode
save outfile=reverse_18.str
solve  vstep=-0.5 vfinal=-20  name=anode
save outfile=reverse_20.str
solve  vstep=-2 vfinal=-30  name=anode
save outfile=reverse_30.str

# change to current contact to resolve breakdown
contact name=anode current
solve
solve imult istep=1.1 ifinal=1 name=anode
#
save outfile=reverse_final.str
#


##############################################################################
                                                AUTO PLOT
##############################################################################
tonyplot reverse_30.str
tonyplot -overlay forward.log
tonyplot -overlay reverse.log

quit
```

Appendix-3: the process flow of tri-gate GaN devices

Step	Purpose	Description
01	Wafer dicing	Substrate: GaN-on-Si Coat PR before dicing Chip size : 2 cm × 1.8 cm
02	To define the alignment marks	Photolith. Resist: AZ1512 Coating : 1’ @ 6000 rpm Bake : 1’30’’ @ 108 ºC Dose: 42, Defocus: 0 Development: 25’’ in AZ-726MIF
03	To etch the alignment marks	ICP dry etching Etchant: $Ar/Cl_2/BCl_3$ Time: 3’30’’
04	To define the fins and the 1st mesa	Ebeam-lith. Cleaning: O_2 plasma 1’ @ 600 W Resist: HSQ 2% Coating: 1’ @ 4500 rpm Dose: 1650, beta = 0.33, eta = 0.2 Development: 2’15’’ in TMAH 25%
05	To etch the fins and the 1st mesa	ICP dry etching Etchant: Ar/Cl_2 Depth: 150 ~ 250 nm
06	To define the 2^{nd} mesa for isolation	Photolith. Resist: nLOF Coating : 1’ @ 6000 rpm Prebake : 1’15’’ @ 118 ºC Postbake : 1’15’’ @ 118 ºC Dose: 42, Defocus: 0 Development: 50’’ in AZ-726MIF
07	To etch the 2^{nd} mesa for isolation	ICP dry etching Etchant: Ar/Cl_2 Depth: 250 ~ 500 nm
08	PR stripping and chip cleaning	30’’ in Piranha solution
09	Cycled treatment to diminish etch damages	1’ @ 600 W in O_2 plasma 2’ in HCl 37% 1’ @ 600 W in O_2 plasma 2’ in HCl 37% 1’ @ 600 W in O_2 plasma 2’ in HCl 37% 1’ @ 600 W in O_2 plasma 2’ in HCl 37% 1’ @ 600 W in O_2 plasma

10	HSQ removal	1’ in BOE
11	To define the ohmic contacts	E-beam lith. PR PMMA double layer 1st layer: PMMA-495-A8 Coating: 7000 rpm for 1’ Baking: 7’30’’@ 180 ºC Cooling: 3’ 2nd layer: PMMA-495-A4 Coating: 4500 rpm for 1’ Baking: 7’30’’@ 180 ºC Dose: 700, beta = 0.33, eta = 0.6 Development: 3’ in MiBK:IPA 1:3 O_2 plasma : 10’’@ 200 W
12	Ohmic formation	Metal: Ti/Al/Ti/Ni/Au Thickness: 20/120/40/60/50 nm Lift-off: in 1165 @ 80 ºC Annealing: 30’’@ 780 ºC
13	Gate insulator	Atomic layer deposition Precleaning: SiO_2 dummy runs SiO_2 20 nm @ 300 ºC
14	To define the contact via	Photolith. Resist: AZ1512 Precoating : HMDS coating Coating : 1’ @ 6000 rpm Bake : 1’30’’ @ 108 ºC Dose: 42, Defocus: 0 Development: 25’’ in AZ-726MIF
15	Contact opening	Wet ethcing 42’’ in HF 1% Etch rate: > 0.66 nm/s
16	PR and HMDS stripping	5’ in SVC-14 @ 50 ºC O_2 plasma: 30’’@ 600 W
16	Gate lithography	E-beam lith. PR PMMA double layer 1st layer: PMMA-495-A8 Coating: 7000 rpm for 1’ Baking: 7’30’’@ 180 ºC Cooling: 3’ 2nd layer: PMMA-495-A4 Coating: 4500 rpm for 1’ Baking: 7’30’’@ 180 ºC Dose: 700, beta = 0.33, eta = 0.6 Development: 3’ in MiBK:IPA 1:3 O_2 plasma : 10’’@ 200 W
17	Gate formation	Metal: Ni/Au Thickness: 50/100 nm Lift-off: in 1165 @ 80 ºC Annealing: 30’’@ 780 ºC

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