# A 23-pixel SPAD array with 45% PDE, 140 cps DCR and 123 ps timing jitter for advanced scanning techniques

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Single-photon avalanche diodes (SPADs) have been rapidly developing since the first integration in CMOS technology in 2003. Custom process SPADs and silicon photomultipliers (SiPMs) can today achieve high performance and single-photon capability, while CMOS SPADs, in addition to that, can also reach large pixel resolution, and on-chip data analysis and compression [1]. To date, most custom process SPADs and SiPMs have been mostly integrated as single-point detectors, while CMOS SPAD arrays have been exhibiting high dark count rate (DCR) non-uniformity and low fill factor generally not exceeding 20% (while 66% has been reported). Both low DCR non-uniformity and high fill factor are required for advanced microscopy techniques.

We present a 23-pixel SPAD array (Figure 1(a)) designed in a standard CMOS process (scalable), matched with excellent sensor performance and low system complexity. The SPAD active area is 107 μm$^2$. The SPAD pixels feature a PDE of 45%, a DCR of 140 cps (with less than 2% hot pixels), and a FWHM timing jitter of 123 ps at an excess bias of 11 V and room temperature [2]. Afterpulsing and crosstalk are below 0.1%. Measurement results are shown in Figure 1. The maximum counting rate is 7.8 Mcps per pixel using passive recharge, while a 20× improvement is possible using active recharge. The system readout is fully parallel and enables continuous recording of counts and timestamps at the maximum photon rate. This SPAD array represents a compact solution for advanced scanning techniques such as fluorescence lifetime imaging (FLIM), fluorescence correlation spectroscopy (FCS), image scanning microscopy (ISM) and stimulated emission depletion (STED)[3]–[5].

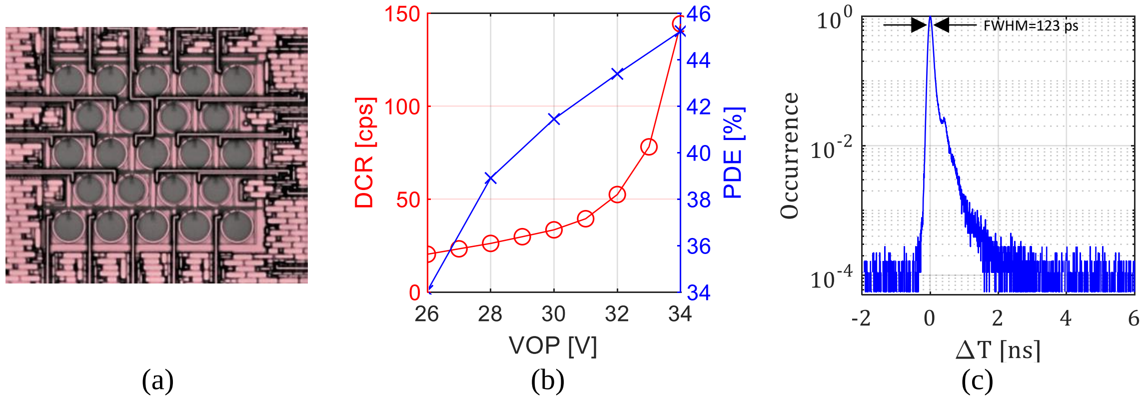


*Figure 1. (a) Micrograph of the 23-pixel SPAD array [2]. (b) Peak PDE and median DCR versus operating voltage VOP. (c) Timing jitter measurements showing 123 ps FWHM.*

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