A manifold microchannel heat sink for ultra-high power density liquid-cooled converters

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***Abstract*—Increase in heat fluxes as a result of the miniaturization of power electronics demands new thermal management solutions such as liquid cooling, because of its high heat extraction capabilities. This work describes a new silicon-based heat sink that takes advantage of the high heat extraction capability of microchannel liquid-cooling at low power consumption by co-designing the heat sink and the electronics. A simple combination of cleanroom microfabricated silicon and laser-cutting of plastics was employed to make a microchannel heat sink that simultaneously cools down 20 active devices (hotspots) of a power electronic converter. By flowing liquid close to the active devices through narrow microchannels, we show that the power requirements of the pump can be minimized, resulting in a compact cooling system that allows integration with small and energy-efficient micropumps. The manifold microchannel heatsink is demonstrated on a ultra-high power density magnetic-less 10x-step-up DC/DC converter resulting in a smaller volume and higher cooling capability than conventional heat sinks. The converter was tested up to an output power of 1.2 kW, with an overall efficiency of 96%, and an average temperature rise of only 12.6 ºC. The converter and heatsink occupy a volume of 260 mL, resulting in a maximum demonstrated power density of 4.62 W/cm^3, and a potential to reach a power density up to 26.9 W/cm^3.**

Keywords—thermal management, liquid cooling, transformer-less DC/DC converters, high power density, microchannel heat sink, GaN transistors

I. Introduction

Wide bandgap semiconductor devices, such as Gallium Nitride High Electron Mobility Transistors (GaN HEMTs) push miniaturization of transistors and diodes for power electronics applications because of their higher breakdown voltage at the same on-resistance [1], [2]. At the same time, GaN HEMTs enable switching at higher frequencies [3] resulting in smaller passive components on the converter. This increase in frequency, however, results in higher switching losses and the smaller component size leads to increased heat fluxes and associated temperature rise of the transistors. This elevated temperature degrade both the device performance and reliability. The thermal management of this class of systems introduces new challenges: The limits of heat extraction using conventional air cooling are easily exceeded in high power density designs [4]. Additionally, fans and heatsinks for forced convection cooling increase the auxiliary power consumption and volume of the system. In order to obtain a high power density and efficiency, small and efficient thermal management solutions are required. Forced liquid cooling offers a high heat transfer coefficient compared to forced air cooling and is therefore an attractive option to cool down high fluxes [5], but the size and power consumption of external pumps is often a drawback. Liquid-cooled cold plates for example, need a high flow rate, which requires large pumps that can be of the same size as the converter itself and have significant power consumption that negatively impacts the efficiency in small systems (few kW range) such as photovoltaic converters [6]. To benefit from forced liquid cooling in a small form factor, a system needs an optimized ratio of heat extraction to pumping power by cooling down the hotspots of the power system in an efficient way, which consequently allows the use of small and energy-efficient integrated micropumps [7]. Reducing the microchannel dimensions increases the heat transfer of the heatsink because of the increased surface-area-to-volume ratio, thus increasing the efficiency of the cooling system at the cost of an increased pressure drop [5], [8], [9]. By dividing the microchannels into multiple parallel sections, the pressure drop can be reduced, while benefitting from the high heat transfer of microchannels [10].

In this work, a new method is proposed to co-design parallel microchannel heat sinks that are in close contact with the HEMTs on an innovative GaN-based magnetic-less 10x-step-up DC/DC power converter [11], in which a manifold distributes the de-ionized water uniformly over each transistor. Since the output power of this converter is solely limited by the heating of the HEMTs, we investigate how the power density of the system can be increased by locally applying liquid cooling to these heat sources with minimal increase in system volume. First, a new technique is presented to fabricate a fluidic manifold by laser cutting of acrylics and water-resistant double-sided adhesive. This manifold connects 10 microchannel heat sinks in parallel that are created using cleanroom fabrication on silicon wafers. This heatsink is subsequently analysed on a printed circuit board (PCB) with resistors emulating the heat sources, in order to characterize the thermal and hydraulic propertiers of the heat sink. Next, a *full-scale heat sink* is designed to cool down 20 GaN transistors on a high power-density 10x step-up DC/DC converter.

II. Theoretical analysis

This section will provide a theoretical motivation for the use of a manifold microchannel heat sink. First, a thermal

resistance model will be presented that describes which parameters determine the temperature rise of the chip. Next, this model is used to motivate what steps should be taken in order to reduce the hot-spot temperatures.

A. Thermal resistance model

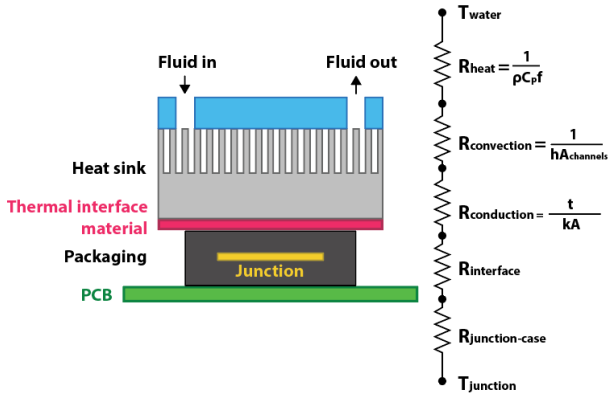


Fig 1. Thermal resistance model of the liquid cooled transistor. The PCB is considered as an adiabatic boundary condition and all heat is assumed to be dissipated by the microchannel heat sink on top.

Fig. 1 shows the schematic design of a liquid cooled transistor and a simplified one-dimensional thermal resistance model that represents the path of the heat flux between the junction and the water. $T_{junction}$ indicates the temperature of the hot spot, and $R_{junction\text{-}case}$ is the thermal resistance determined by the packaging of the transistor, specified by the manufacturer. $R_{interface}$ is the thermal resistance due to the contact between the transistor and the heat sink. $R_{conduction}$ is the thermal resistance due the heat traveling through a solid layer, which is defined as:

$$R_{conduction} = t/kA \quad (1)$$

where t is the thickness of the layer, k is the thermal conductivity of the solid and A is the surface area for conductive heat transfer. $R_{convection}$ is the thermal resistance due to the convective heat transfer between the solid material and the liquid, defined as [12]:

$$R_{convection} = 1/hA_{channels} \quad (2)$$

where h is the convective heat transfer coefficient and $A_{channels}$ is the effective surface area for convection. R_{heat} is the thermal resistance due to the water heating up as it absorbs heat and is defined as:

$$R_{heat} = 1/\rho C_p f \quad (3)$$

where ρ is the density of the cooling medium, C_p is the heat capacity of the cooling medium at constant pressure and f is the flow rate. T_{water} is the inlet temperature of the liquid, which is the ambient temperature of 24 ºC in this case.

B. Optimization

The temperature rise between the ambient and the junction, ΔT, for a certain power dissipation Q can be calculated by combining all series thermal resistances:

$$\Delta T = Q\,(R_{junction\text{-}case} + R_{interface} + R_{conduction} + R_{convection} + R_{heat}) \quad (4)$$

Thus the junction temperature can be decreased by reducing all terms of the thermal resistance:

- $R_{conduction}$ can be reduced by flowing the liquid closer to the chip, such that t will be reduced, and by choosing a material with a high thermal conductivity for the heat sink.
- $R_{convection}$ can be reduced by increasing the surface area for convective heat transfer, which can be done by using high aspect ratio microchannels with small spacing since the surface area of a microchannel heat sink and the channel width are inversely related to each other.
- R_{heat} can be minimized by choosing a liquid with a high heat capacity, such as water, and by increasing the flow rate of the liquid.

A higher flow rate, however results in an increased pressure drop as can be seen in (5) [5], where the flow through the high aspect ratio microchannels is assumed to be a laminar parallel-plate flow. The terms P, L, v, μ and w_c denote respectively the pressure drop, length of the microchannel, liquid velocity, liquid viscosity and microchannel width.

$$P = 12\mu Lv/w_c^2 \quad (5)$$

Equation (5) further shows that making the microchannels narrower results in a quadratic increase in pressure drop. Therefore, in order to benefit from the enhanced heat transfer of microchannels without a high pressure drop, the microchannel length L should be minimized by dividing all microchannels into short sections such that the liquid flows only through a narrow microchannels close to the hot-spots where it needs to absorb the heat, and through larger sized channels in a manifold that spreads the liquid over these multiple parallel microchannel sections.

III. Design and Fabrication

A. Prototype heat sink

A prototype multi-layer manifold microchannel (MMC) heat sink was fabricated out of 3 layers laser-cut transparent acrylic (PMMA) with water-resistant double sided adhesive on the bottom side, and a 500 µm layer of silicon with 50 µm x 400 µm deep-reactive-ion-etched (DRIE) microchannels, as can be seen in Fig. 2. This heatsink will be referred to as the *prototype heat sink* and will be used to characterize the thermal and hydraulic properties of the cooling system. The PMMA layers were bonded together using double sided adhesive, and inlet and outlet ports were threaded to mount connectors that are sealed using silicone O-rings. The middle PMMA layers function as a manifold that spreads the de-ionized water over the 10 microchannel sections in the silicon bottom plate, while the transparency of the PMMA allows flow visualization. The complete assembled *prototype heat sink* is shown in Fig. 3, along with a micropump, able to supply the required pressure and flow rate.

B. Full-scale heat sink

A second version of the MMC heat sink was designed together with the 10x-step-up DC-DC converter to cool down

all transistors on the PCB simultaneously. This heat sink is referred to as the *full-scale heat sink*. Because of the larger size of the heat sink, it is no longer cost effective to make the microchannel section out of a single piece of silicon. sixty-nine 9 mm x 9 mm silicon dies with microchannels, as show in the scanning electron microscopy (SEM) images in Fig 4, were fabricated on a single wafer. As can be seen, by using the DRIE process, high aspect ratio microchannels with a width of 50 µm and a height of 400 µm with straight sidewalls can be obtained, which results in a large surface area for heat transfer.

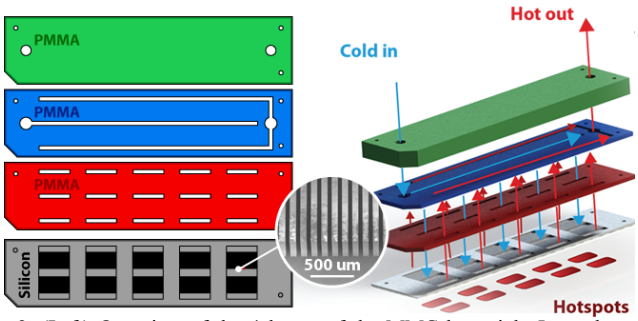


Fig 2. (Left) Overview of the 4 layers of the MMC heat sink. Inset shows a SEM image of the microchannels. (Right) Illustration of the operating principle of the MMC heat sink. The middle PMMA manifold spreads the water to 10 microchannel section on the silicon bottom layer where the heat of the hotspots is being absorbed

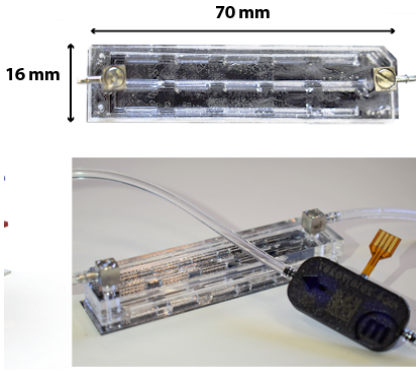
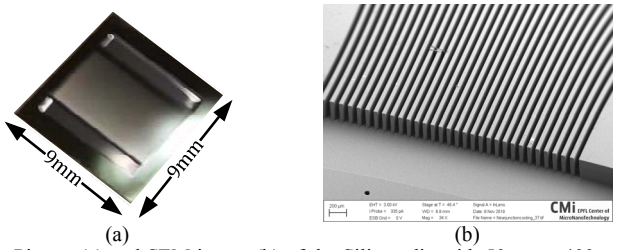


Fig 3. Picture of the assembled *prototype heat sink* (top) and a picture of the heat sink together with a piezoelectric micropump (bottom)

The *full-scale heat sink* was assembled in the same way as the *prototype heat sink*, but the 20 silicon dies were stuck one by one to the double-sided adhesive on the bottom PMMA layer. The trade-off of this design is that the heat can no longer spread between hot spots since the silicon dies are no longer connected. The top two PMMA layers were fabricated out of 8 mm thick acrylic to obtain more stiffness, such that the heat sink can be tightly mounted on the PCB without bending. The assembled *full-scale heat sink* is shown in Fig. 5



(a) (b)

Fig 4. Picture (a) and SEM image (b) of the Silicon die with 50 um x 400 um microchannels

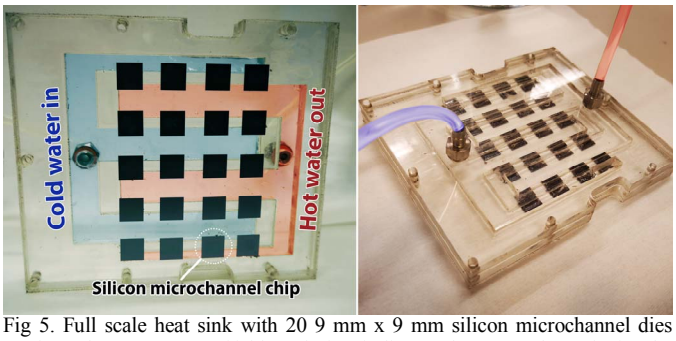


Fig 5. Full scale heat sink with 20 9 mm x 9 mm silicon microchannel dies stuck to the PMMA manifold. Coloring indicates the entry channels for the cold water and the outlet channels for the hot water.

IV. Experimental Evaluation

A. *Prototype heat sink*

The *prototype heat sink* was placed on top of a PCB with 10 surface mount resistors. By dissipating power in these resistors, the heating of the transistors during operation of a converter is mimicked. The benefit of this approach is that, in contrast to a transistor in a power converter circuit, the power dissipation per resistor can accurately be determined. An inlet reservoir of de-ionized water is pressurized using an Elveflow OB1-MK3 pressure controller in order to flow the liquid through the heat sink, while the flow speed of the water is measured using an Elveflow FS1 flow sensor.

1) Hydraulic resistance:

Fig. 6 shows the flow speed versus pressure drop of the prototype heatsink (red line). The green curve corresponds to the flow speed after connecting a 20 µm sintered filter to prevent clogging of the microchannels. As can be seen, the filter used in these experiments accounted for the majority of the pressure drop, which can be easily mitigated by a more appropriate choice of filter. Fig. 6 also shows the output line of the low-power piezoelectric micropump of Fig 3, which operates at less than 100 mW (compared to ~2-5W of a typical fan) [13]. The operational points, where the pump and heat sink curves cross, indicate the flow speed of the water through the complete setup. It can be seen that flow speeds between 4 ml/min and 6 ml/min can be obtained with the presented combination of pump and heat sink. For comparison, Fig. 7 shows the flow speed versus pressure drop for the *full-scale heat sink*.

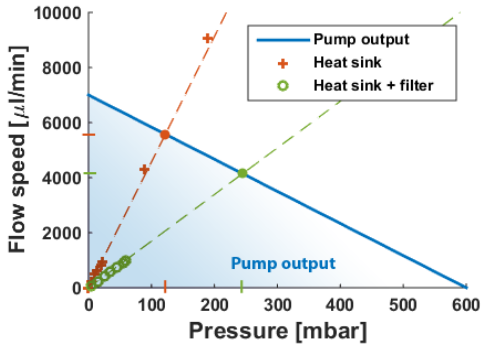


Fig 6. Pressure drop over the prototype microchannel heat sink with filter (green) and without filter (red). The blue area indicates the piezoelectric

micropump can obtain.

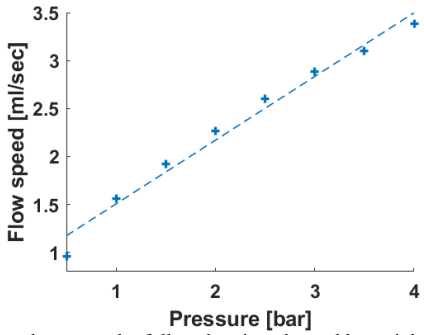


Fig 7. Pressure drop over the full-scale microchannel heat sink

2) Thermal analysis:

Experiments with the *prototype heat sink* under different pumping pressure have been performed on a PCB with 10 resistors that mimic the transistors in a converter. Temperature rise was measured using a thermocouple mounted to the backside of the center resistor, while the power dissipation was regulated using a DC-power source. As can be seen in Fig. 8, the thermal resistance of this resistor decreased from 288 K/W in absence of a heatsink, down to 18 K/W for a pressure of 400 mbar, corresponding to a significant reduction of up to 94%.

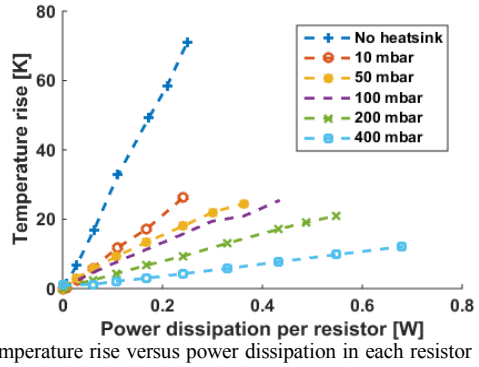


Fig 8. Temperature rise versus power dissipation in each resistor in case of no heat sink, and with the liquid cooled *prototype heat sink* at pressures of 10 mbar, 50 mbar, 100 mbar, 200 mbar and 400 mbar. Increasing the pressure results in a lower thermal resistance due to the decreased heating of the water

Fig. 9 shows the thermal resistance as a function of the inverse of the flow rate. Equation (3) suggests a linear relationship between R_{heat} and *1/f*. By fitting a linear function and taking the intercept at the theoretical point of 1/f = 0, i.e. at infinite flow rate, R_{heat} was determined and subtracted from the total thermal resistance, resulting in a remaining thermal resistance of 13.4 K/W. $R_{junction\text{-}case}$ of the resistor is 11 K/W according to the datasheets [14]. $R_{conduction}$ is approximately 0.05 K/W, based on the surface area of the resistors, a distance of 150 µm between the bottom of the silicon dies and the microchannels and a thermal conductivity of silicon of 148 W/mK. Using the same calculation as [5], $R_{convection}$ for 50 µm microchannels is estimated to be smaller than 1 K/W [5]. The remaining part of the thermal resistance can be accounted to the interface between the transistor and the heatsink, which is around 2 K/W. This result shows the importance of a good contact between the heat sink and the transistor, since the interface easily becomes the dominating term in the total thermal resistance. It should be noted that no force was applied on the heat sink, it was standing freely on top of the transistors with a thermal interface material in between.

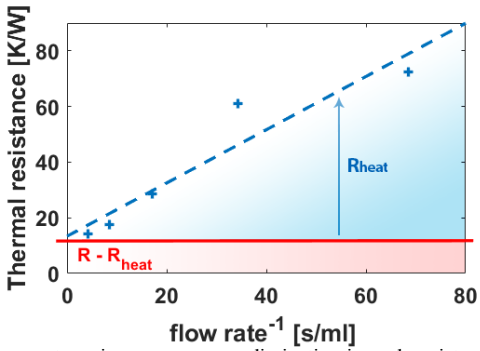
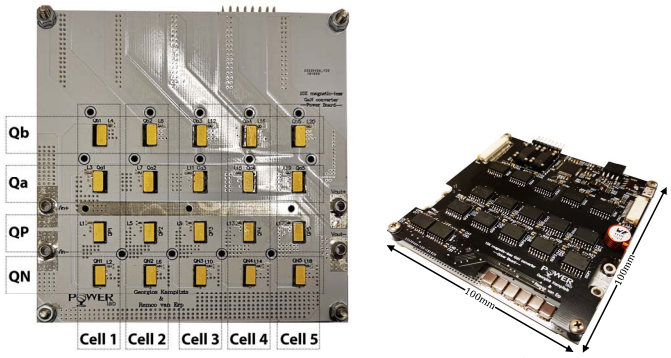


Fig 9. Temperature rise versus power dissipation in each resistor in case of no heat sink, and with the liquid cooled *prototype heat sink* at pressures of 10 mbar, 50 mbar, 100 mbar, 200 mbar and 400 mbar. Increasing the pressure results in a lower thermal resistance due to the decreased heating of the water

B. *Full-scale heat sink*

Finally, the full-scale MMC heat sink was demonstrated on a high power density magnetic-less 10x step up DC-DC converter, as shown in Fig. 10. The converter consists of two PCBs: a power board, that contains the 20 GaN transistors together with a temperature sensor to continuously monitor the temperature of each transistor during operation, and a logic board with microprocessor. The temperature rise during operation of the converter using the liquid cooled heat sink was compared to the performance of a conventional heat sink and fan setup. The nX topology offers an interesting showcase: because of the absence of magnetics, the densely packed GaN HEMTs are the only major heat sources. Furthermore, the GaN transistors used in this board, GaN Systems GS61008T and GaN Systems GS66508T, have a thermal pad on the top of their packaging, and a low $R_{junction\text{-}case}$ of 0.5 K/W and 0.55 K/W, respectively [15], [16]. This low thermal resistance to the top of the transistor allows efficient cooling from the top side by connecting the *full-scale heat sink* to the thermal pad using a thermal interface material. The *full-scale heat sink* was designed in such a way that it can be tightly screwed on top of the PCB to ensure good thermal contact and to reduce the contribution of the interface thermal resistance.



(a) (b)

Fig 10. (a) Power board with with 20 GaN transistors. Rows are labelled as Q_b, Q_a, Q_P and Q_N, and columns are labelled as cell 1-5. (b) Complete converter with the logic board (in black) on top of the power board (in white).

1) Temperature rise

Fig. 11 compares the average temperature rise versus output power of the converter for the liquid heat sink at 0.5 bar, 1 bar, 2 bar and 3 bar, as well as the temperature rise for the converter with a 40 mm-high aluminum heat sink without fan, and with forced air cooling at 33.6 CPM. The converter with the 40 mm-high aluminum heat sink and no fan shows an average temperature rise of 42.83ºC. The converter with the same aluminium heat sink and forced air convection at 33.6 CFM shows an average temperature rise of 25.85 ºC, whereas the liquid cooled heat sink at a pressure of 3 bar results in an average temperature rise of merely 10.37 ºC. The liquid cooled reduces the temperature rise with 76% and 60% compared to the aluminium heat sink with natural and forced convection, respectively, within a smaller volume. Moreover, Fig 11 shows that increasing the pressure from 0.5 to 3 bar, which corresponds to a flow rate of 1.0 and 3.4 ml/sec, respectively, does not reduce significantly the thermal resistance. Based on the same analysis as on *the prototype heat sink*, this illustrates that the thermal interface between the heat sink and the transistor again makes a major contribution to the total thermal resistance.

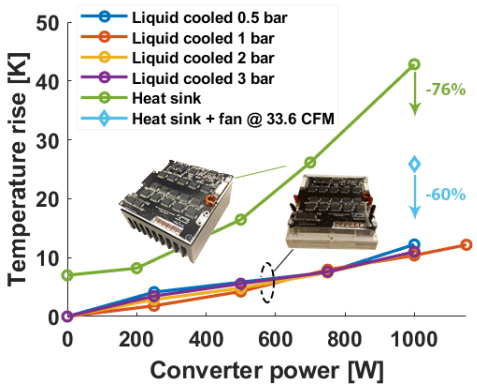


Fig. 11. Temperature rise versus converter output power for the liquid cooled heat sink at pressures of 0.5 bar, 1 bar, 2 bar and 3 bar, the same converter with a solid, 40mm high aluminum heat sink and the converter with the 40mm high solid aluminum heat sink and a fan for forced convective air cooling at a air flow speed of 33.6 CFM.

2) Power density

Table 1 summarizes the temperature rises and volumes of the three configurations and the resulting power densities. Based on the thermal measured temperature increase at 1 kW, the projected maximum output power of the converter is calculated, assuming a maximum temperature rise of 70ºC. Even though the GaN transistors are rated to operate up to 150ºC [16], this upper limit was chosen to prevent the water from boiling in the microchannels causing rapid expansion which leads to flow instabilities and maldistribution over the manifold. As can be seen in this table, the highest demonstrated power density using the liquid cooled MMC heat sink is 4.62 W/cm^2, and based on the average thermal resistance of 0.010 K/W, a potential maximum power of 7 kW can be achieved below a temperature rise of 70ºC, which results in a power density of 26.9 W/cm^2. This projection, however, assumes a constant efficiency, while in reality the conduction losses in the transistors increase as the temperature rises. The maximum power in this experiment was limited by the available power supply, so further work should validate to what extent this potential power density is achievable.

TABLE I. AVERAGE TEMPERATURE RISE, THERMAL RESISTANCE, VOLUME AND POWER DENSITIES FOR THE CONVERTER USING DIFFERENT COOLING TECHNIQUES

	ΔT *at 1 kW* [K]	**R [K/W]**	**P_{max} [W]**	**Volume [cm^3]**	**Power density [W/cm^3]**	
					Demonstrated	**Potential**
Heat sink	42.83	0.043	1628	510	1.96	3.19
Heat sink + fan @ 33.6 CFM	25.85	0.026	2692	610	1.64	4.41
Liquid cooled	10.37	0.010	7000	260	4.62	26.9

3) Temperature uniformity

Fig. 12a shows the measured temperature map of the 20 GaN HEMTs at an output power of 1 kW using the full-scale MMC heat sink. Fig 12b shows the temperature map of the same converter together with a conventional aluminum heat sink with 40 mm-high fins with a fan under a flow rate of 33.6 CFM as comparison. As can be seen in the temperature maps, the temperature sensors at cell 1, and especially $Q_a(1)$ show a significantly higher temperature than the other transistors. This is not in agreement with the theoretical simulations, as cell 1 is subjected to only half the voltage as the other 4 cells [11]. IR measurements were performed to investigate the heating of the first cell, shown in Fig. 13. As can be seen, the hotspot of the PCB appears to be on the inductor at a temperature of 63.1 ºC, higher than the temperature measured at the temperature sensor on transistor $Q_a(1)$. Furthermore, it can be seen that the copper traces connected to the inductor have an increased temperature, which indicates that the high temperature on the first cell is due to the heating of the inductor. Fig. 14 shows the transient temperature profiles of all 20 temperature sensors at an output power of 1 kW. As can be seen, the temperatures at cell 1 are significantly higher, but also do not seem to reach equilibrium. This confirms that the elevated temperatures at cell 1 are because of the increasing temperature of the PCB, which takes more time to reach steady state. In this case, the actual junction temperature of the transistor is likely to be lower than the measured temperature since the transistors have a thermal resistance of 5 K/W between the junction and the PCB and 0.5 K/W between the junction and the top-side thermal pad [15], [16]. Therefore, the junction of the transistor is being cooled down more efficiently than the pad connected to the temperature sensor.

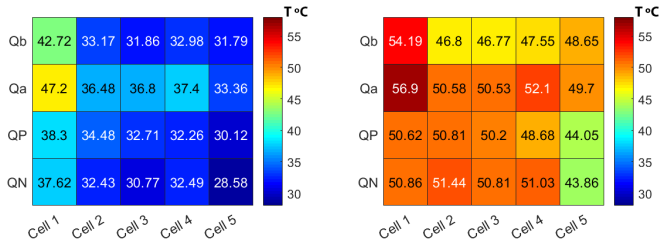


Fig 12. Heat maps of steady state temperatures of the 20 transistors in case of liquid cooling at 3 bar (a) and in case of a 40 mm high aluminum heat sink with forced convective air cooling at a flow speed of 33.6 CFM (b). Both images use the same temperature scale. Using the liquid cooling results in significantly lower transistor temperatures, even with reduced heat spreading because the silicon microchannel heat sinks are separated.

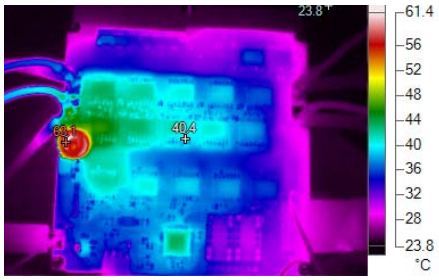


Fig. 13. IR image of the converter operating at 1 kW output power. The hotspot of 63.1ºC is measured on the inductor, that was painted black for increasing the IR emissivity. It can be seen that the traces in the PCB that are connected to the inductor significantly heat up.

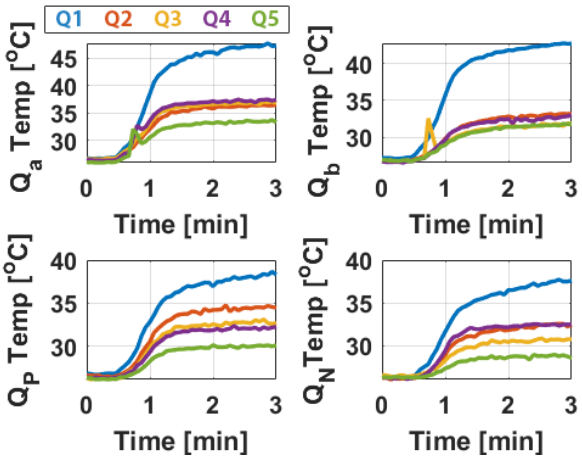


Fig 14. Temperature profiles for the 20 transistors on the 10x step-up DC-DC converter operated at 1 kW. Q_b, Q_a Q_P and Q_N refer to the first, second, third and fourth row of transistors as indicated in fig. 8. With exception of the transistors in the first cell, thermal equilibrium is achieved within 3 minutes.

V. Conclusions

In this work, a simple method was demonstrated to fabricate a manifold microchannel heat sink out of three layers of PMMA with double sided adhesive and a micro-fabricated silicon cold plate that is co-designed with the electronics to efficiently cool local hotspots on a PCB at a low pressure drop. A *prototype heat sink* was developed and tested on a PCB with resistors to determine the thermal resistance. Analysis of this *prototype heat sink* showed that a large part of the thermal resistance can be accounted to the interface between the heat sink and the transistor, which stresses the need to optimize this interface by applying sufficient force to the heat sink and by choosing the right thermal interface material. A full scale manifold microchannel heat sink was designed in parallel with a 10x step-up high power-density DC/DC converter to demonstrate the potential of this technology. At an output power of 1 kW, the average temperature rise is 10.37K, which is a reduction of 76% and 60% compared to a conventional heat sink with natural convection and forced air cooling, respectively.

The projected power density by allowing a temperature rise of 70K would be 26.9 W/cm^3 at an output power of 7 kW. The maximum demonstrated converted output power was 1.2 kW, which was only limited by the maximum output of the power supply. This work demonstrates the high heat extraction capabilities of liquid cooling with minimum added volume to the system. Furthermore, it shows that by designing the electronics and cooling together as a complete system, very high power densities can be obtained.

Acknowledgment

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