The White Rabbit Time Synchronization Protocol for Synchrophasor Networks

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Abstract—Within the context of time dissemination techniques for power systems applications, the paper discusses the use of the White Rabbit (WR) protocol for synchrophasor networks. Specifically, the paper presents a Phasor Measurement Unit (PMU) integrating the WR technology and its experimental validation with a focus on the synchrophasor phase estimation in steady state conditions, by using a PMU calibrator generating the reference signals. We further compare the accuracy of the developed PMU with other state-of-the-art time synchronization technologies for PMUs, i.e., Global Positioning System (GPS) and Precision Time Protocol (PTP), demonstrating applicability of WR for PMU sensing networks.

Index Terms—Phasor Measurement Unit (PMU), synchrophasor network, time synchronization, White Rabbit

I. INTRODUCTION

Synchrophasor technology is the leading edge of timing use for power systems as Phasor Measurement Units (PMUs) cannot be adopted for mission-critical or automated actions, unless coupled with an appropriate time dissemination technique. The IEEE Std. C37.118.1 requires a maximum uncertainty in the synchrophasor time stamp of 1 μs [1]. Indeed, in order to properly phase-align and report synchrophasors measured by PMUs located in geographically-distant substations, the network nodes have to share a common, accurate and reliable time reference. Poor time-synchronization causes inaccurate phasor estimations (particularly relevant for phase estimations) that, if undetected by the overlying applications (e.g., state estimators bad data processes [2]), may cause incorrect interpretations of the grid conditions and inappropriate actions [3]. This is particularly critical for distribution networks since they require an increased level of PMU accuracy [4].

The time synchronization of PMUs typically relies on the Global Positioning System (GPS) as it represents a good trade-off between performance and cost. GPS provides an accuracy in the order of ±50 ns when coupled with modern GPS-receivers. However, the GPS is vulnerable to timing attacks and is not always physically accessible (consider for instance the case of underground substation without an access to the sky) [5]. As suggested in [3], until timing challenges have been resolved and time dissemination reliability assured, PMUs cannot be used for mission-critical operations, such as protection or automated control. To improve timing redundancy and reliability, given the potential vulnerability of GPS, synchrophasor applications should use multiple timing sources, for instance deployable over the legacy power system telecom infrastructure. As a matter of fact, any PMU-based monitoring or control application relies on a telecom infrastructure to stream PMU data and the same physical layer may be used for time dissemination purposes. In this context, the paper investigates alternative or complement solutions to the GPS, with particular focus on cases when the sky is not accessible and the Ethernet-based telecom infrastructure is already available (e.g., urban areas). Among the possible alternatives, the paper presents the White Rabbit (WR) Time Protocol [6]–[8], and compares its performance with respect to the GPS and the Precision Time Protocol (PTP) [9].

PTP was introduced by the IEEE Std. 1588 in order to provide a hardware-level time accuracy using a standard Local Area Network (LAN) connection (e.g., Ethernet) [9], and is characterized by an accuracy of 1 μs. As an evolution of PTP, the WR time synchronization protocol is a low-latency, time-deterministic Ethernet-based time dissemination technique, developed for distributed sensing systems [6]. The project was initiated at CERN (European Organization for Nuclear Research) to develop an ultra-precise timing system for CERN accelerator complex. The WR is based on the standards Ethernet (IEEE 802.3) [10] and Synchronous Ethernet (SyncE) [11]. It enables the synchronization of thousands of devices connected in a network spanning several kilometers through already existing communication networks. The accuracy, is meant to achieve the sub-nanosecond, assuming only fiber interconnections and dedicated telecom switches. Moreover, the protocol features a reliable and deterministic data delivery.

Within this context, the scope of this paper is twofold. First, we present a PMU (also called WR-PMU) integrating the WR protocol as time dissemination technology. We describe all technological aspects of the timing architecture and its integration in an embedded device. Second, we assess the performance of the developed WR-PMU. We experimentally validate the phase estimation stability over the short, medium and long term, by means of reference signals generated by a PMU calibrator [12]. A preliminary analysis has been presented in [13]. In the current manuscript, we present an enhanced version of the WR-PMU that integrates an internal clock regulated by a PI controller. Furthermore, we compare
II. Time Synchronization Techniques for PMUs

Time synchronization is a key factor in any PMU-based monitoring systems [3]. The IEEE Std. C37.118.1 [1] defines the phase of a synchrophasor as the instantaneous phase angle relative to a cosine function at the nominal power system frequency, synchronized to Coordinated Universal Time (UTC). In that sense, any uncertainty in the time synchronization translates in a phase uncertainty \( \Delta \varphi \), depending on the instantaneous frequency \( f \) of the signal:

\[
\Delta \varphi = 2\pi f \Delta t + \varepsilon_{\text{alg}} + \varepsilon_{\text{acq}}
\]

where \( \varepsilon_{\text{alg}} \) and \( \varepsilon_{\text{acq}} \) account for two additional uncertainty sources, i.e., the phase error introduced by the adopted synchrophasor estimation algorithm and the phase noise produced by the acquisition process (including the measurement chain from the sensor to the PMU analog input), respectively. Since these errors come from independent devices, we assume these two contributions to be statistically independent and uncorrelated, and we focus mainly on the synchronizer uncertainty (see Section V for more details). The same standard further requires that synchrophasor measurements are reported by PMUs at a specific reporting rate, with the first frame within the second at the UTC-second rollover.

The IEEE Std. C37.118.1 [1] suggests a maximum uncertainty in the synchrophasor time stamp of 1 \( \mu s \). This value is indirectly determined by the requirement for a maximum Total Vector Error (TVE) of 1 \%. The TVE is defined as the Euclidean distance between the true and estimated synchrophasors, normalized with respect to the amplitude of the true synchrophasor. As such, it is a performance indicator that accounts for a component due to the measurement of amplitude and a component due to the measurement of phase. Let us suppose that the contribution of the amplitude error to the TVE is negligible and therefore the TVE is only influenced by the phase error. Simple trigonometry will lead to the fact that, regardless of the angle being measured, a phase uncertainty of 0.01 rad will itself cause a 1\% TVE. If we consider the synchronous grid of Continental Europe characterized by a nominal frequency of 50 Hz, according to (1), this corresponds to an error of \( \pm 31 \mu s \), when time is the only source of error. A reliable time source should be characterized by an uncertainty at least 10 times better, giving some allowance for sources of error other than synchronization, leading to the recommended time uncertainty of 1 \( \mu s \).

However, it is well-established that PMUs operating in distribution networks are expected to meet more stringent accuracy requirements, at least two orders of magnitude lower than those met by transmission PMUs (TVE lower than 0.01\%) [4]. Therefore, the uncertainty contribution coming from the timing unit should be reduced the order of tens of ns [3].

In the following, two time dissemination technologies that are currently being used for PMU applications are described: (i) satellite and (ii) network-based synchronization systems, making reference to their functional features and performance. We discuss their applicability to synchrophasor technology and their vulnerability to timing-attacks [3].

A. Satellite-based Time Synchronization Systems

The operation principle of satellite systems is based on the time measurement of synchronizing signals between satellites and terrestrial receivers. The satellites are equipped with atomic clocks, daily monitored and controlled to be highly synchronized and traceable to the UTC time. The receivers are equipped with an internal clock, and are able to determine the actual UTC time by collecting and processing messages from several satellites. GPS receivers are often used as primary absolute timing source for most of time dissemination techniques.

As known, PMU applications generally rely on the GPS that provides an accuracy in the order of \( \pm 100 \) ns when coupled with commercial GPS-receivers (e.g., [14]), although modern units can nowadays reach accuracy lower than \( \pm 50 \) ns. In such scenario, a dedicated GPS receiver must be installed at every PMU location, and the same applies to Phasor Data Concentrators (PDC) in case time-stamping functionalities are implemented at data collection.

To correctly lock satellites, the GPS receiver requires a clear view of the sky. Indeed, being in an enclosed space such as a high rise urban environment, reduces the number of tracked satellites and determines signal reflections and wakening, resulting in a degradation of the time information accuracy [15].

Regarding security, the GPS signals can be easily spoofed resulting into complex and potentially dangerous time attacks [16]. Among different types of attacks, GPS spoofing is the most malicious and difficult to detect [5]. It is achieved by superimposing a fake signal with a higher signal-to-noise ratio, which would enable an attacker to manipulate the GPS clock. With particular reference to the GPS-based PMUs, a spoofing attack can cause the GPS receiver of a PMU to compute an erroneous clock offset, resulting in an erroneous time stamp calculation, which introduces an error in the PMU’s phase measurement. The failure to deliver data to concentrators and applications within acceptable latency periods causes data gaps that could corrupt early warning information about dynamic grid conditions.

B. Packed-Switching Synchronization Messaging Protocols

Typically, synchrophasor networks use the Ethernet network protocol as physical layer to transfer data. The protocol, introduced by the IEEE Std. 802.3, represents a well-established and very high-performance solution, that is capable of supporting the high-throughput of synchrophasor data streams.
The Precision Time Protocol (PTP) was introduced by the IEEE Std. 1588 in order to provide time accuracies beyond those attainable using NTP, thanks to a technique called hardware time-stamping [9]. The most recent PTP version 2 (PTPv2) provides 1 μs accuracy, measured as the deviation of each node with respect to the UTC.

The core element of the PTP is the exchange of time-tagged messages in a peer-to-peer link between master and slave clocks, used to calculate the link delay between the two clocks. Specifically, at time $t_1$ the master node sends a Sync message, that is received at time $t_2$ by the slave. Similarly, at time $t_3$, the slave node sends a message, received at time $t_4$ by the master. Knowing these four time-stamps, the one-way delay between the two clocks can be estimated as:

$$\delta = \frac{(t_2 - t_1 + t_4 - t_3)}{2} \quad (2)$$

The slave node can account for this offset when adjusting its clock time with respect to the one of its master clock.

The PTP assumes that all network nodes are equipped with PTP-aware routers or switches, implementing the so-called hardware-assisted time-stamping, a technique to measure and compensate for the time spent by messages in queuing at their own ports.

The first limitation of the PTP is that it assumes the one-way delay is exactly half of the two-way delay, which, due to link asymmetry is true only as long as the cable is very short. The second limitation is that the final PTP accuracy is limited by the precision and resolution of the master and slave clocks to measure the time when sending or receiving messages, typically of 100 ppm. The third limitation is that these clocks are typically free-running oscillators, without any guarantee of synchronism between oscillators at different nodes. This results in uncontrolled time drift between masters and slaves. The higher the exchange rate of PTP messages, the lower the time drift, the higher the bandwidth needed for PTP-related traffic.

The security of PTP (as well as WR) against cyber-attacks is studied in [18] by using a so-called delay-box that introduces a malicious offset of a few microseconds in the slave clock. Nevertheless, the attack can be counteracted by using redundant and disjoint communication paths or using the GPS as a redundant time source.

An extended profile for the use of PTP in power system applications is specified in [19] and, for instance, used in [20]. With a specific reference to PMUs, the protocol has been integrated into synchrophasor networks to distribute the time [21], [22].

III. THE WHITE RABBIT TIME SYNCHRONIZATION PROTOCOL

Recently, the WR protocol, also known as PTP version 3 (PTPv3), has been developed and used at CERN to align the clocks of their accelerator complex [6]–[8]. The protocol enables the synchronization of thousands of devices connected in a network spanning several kilometers through already existing Ethernet-based networks. The accuracy, measured as the deviation of each node with respect to the UTC, achieves the sub-nanosecond, assuming only fiber interconnections. Moreover, the protocol features a reliable and deterministic data delivery. The project is open source [23].

These features make the WR an appropriate time synchronization protocol for smart grids applications [24]–[26]. Indeed, the accuracy on 1 ns exceeds the one of synchrophasor needs. Also, the superior determinism with respect to PTP is good for reliability and mission-critical applications. This technology represents an appropriate alternative or complement to the GPS with particular focus on the cases when (i) the sky is not accessible (e.g., urban areas), (ii) the telecommunication infrastructure is already available, and (iii) the typical length between two PMUs is less than 10 km (e.g., sub transmission or power distribution networks). The main limitation of the WR technology for synchrophasor networks arises when the electrical grid is not equipped with fiber-optic cables. Indeed, from an economical perspective, refurbishing the feeder with fiber links may result in large installation costs that could hinder the cost-benefit analysis related to the WR solution.

It is worth mentioning that recent studies have demonstrated the stability of the WR protocol over fiber links up to 950 km [27], [28]. Further studies have addressed the problem of temperature-related hardware delays [29].

A. The White Rabbit Network Architecture

Figure 1 shows the layout of a typical WR network, that is composed of WR nodes and WR switches, interconnected by fiber links\(^1\). Data-wise it is a standard Ethernet switched network, i.e., there is no hierarchy: any node can talk to any other node in the network. Regarding time synchronization, there is a hierarchy, that goes from the top, namely from the WR master, down to other WR switches and consequently nodes. The WR switch, key element of any WR network, is

\(^1\)Although fiber is the preferred physical layer for WR technology, copper (1000BaseT) can be also used in small portions of the network with less-stringent timing requirements [30].
similar to a standard Ethernet switch, but it is also able to precisely distribute the WR master clock over the network thanks to a technique called precise phase measurement [31].

The uppermost switch in the hierarchy, also called grand-master, receives the absolute clock from an NTP source (e.g., the NTP daemon running on a computer), together with the pulse-per-second (PPS) and the 10 MHz from an external reference (e.g., a GPS receiver or a Cesium clock). At start-up, the WR switch uses the NTP and the PPS to determine the absolute UTC time. Then, it calculates the time using only the 10 MHz signal. After the switch has completed the rebooting routine, i.e., few minutes after powering it on, the NTP service and the PPS are not needed anymore and the grand-master switch could be potentially disconnected from these sources. The accuracy of the round-trip time measurement is mostly determined by the accuracy of the 10 MHz source. The grand-master switch then distributes the time information to further WR nodes via intermediate WR switches. It is worth pointing out that the subsequent switches do not have to be connected to a 10 MHz source.

In the power system context, it is reasonable to expect that the grand-master WR switch is located in a safe location, such as the control room of the network operator. To guarantee reliability, the grand-master switch as well as the 10MHz sources should be powered via an uninterruptible power supply (UPS). It is also reasonable to expect that the grand-master switch is rebooted only if needed, few times over the lifetime of the synchrophasor network, for instance at the same time of rebooting the central phasor data concentrator (PDC) or updating PMUs firmware.

Finally, the security of WR against delay-attacks is studied in [18], and countermeasures for this type of attack are proposed.

B. The White Rabbit Synchronization Scheme

The WR is based on existing standards, namely Ethernet (IEEE 802.3) [10], Synchronous Ethernet (SyncE) [11], IEEE 1588 (PTPv2) [9] and adopts a technique called Precise Phase Measurement. The combination of these technologies, further described in this section, enables to achieve the sub-nanosecond accuracy [32].

1) PTPv2: The same process described in Section II-B holds for calculating the one-way transmission delays. However, in a WR network, PTP messages are managed not only by the grand master clock, but also by the WR switches. This method prevents PTP messages to be exchanged between long links from the master to a far side slave, reducing the unavoidable jitter introduced by each switch. Also, the number of messages between master and slaves is reduced, reducing the PTP-related throughput and allowing more bandwidth for mission-critical data exchange.

2) SyncE: Typical PTP implementations use free-running oscillators in each node, resulting in growing time drifts between master and slaves. This is solved by the SyncE protocol, a technique to transfer the frequency over the Ethernet physical layer, in order to lock all the network nodes to beat at exactly the same rate. Every WR switch uses the clock recovered by the data link to sample the incoming data. Then, it uses an embedded PLL-based oscillator, locked to the recovered clock, for transmission. This procedures ensures high level jitter elimination. Since it acts on the physical layer, its accuracy is independent of data transmission (packet delay or traffic load). The technology has been proven to be able to transfer very accurate timing over long distances [7], [11].

3) Precise Phase Measurement: The accumulation of phase noise degrades the performance of network-based synchronization protocols. To this end, every WR switch is equipped with a phase measurement module based on phase/frequency detectors that periodically measures the phase difference between the recovered clock and the master clock [33]. The calculated phase difference is transmitted to a slave node for further compensation of the round-trip link delay with sub-nanosecond accuracy.

IV. INTEGRATION SCHEMES OF TIME REFERENCES INTO A DEDICATED PMU

In order to compare the performance of the time synchronization techniques under investigation, we develop three PMUs based on the same synchrophasor estimation algorithm and the same hardware. The only difference among the three is the adopted technique to synchronize to the absolute time reference: the so-called GPS-PMU is based on the GPS time dissemination technique, and is further described in Section IV-C, the PTP-PMU is based on PTPv2 and is described in Section IV-D, whereas the WR-PMU is based on the WR protocol and its implementation details are given in Section IV-E. The main features of the three devices are very similar to those of the PMU described in [14]: any difference or similarity is illustrated in this section, with a focus on all implementation details that condition time accuracy.

To limit any discrepancy introduced by the synchrophasor estimation process, the three PMUs are based on the same synchrophasor estimation algorithm of [14], an enhanced version of the interpolated Discrete Fourier Transform (DFT), hereafter called e-IPDFT, that compensates for the effects of spectral leakage coming from the negative image of the tone under analysis. Such PMU was developed at the Distributed Electrical Systems Laboratory (DESL) or EPFL. Further details are provided in Section IV-A.

As in [14], the hardware platform of the three devices is based on the National Instruments compactRIO (cRIO) system, an embedded industrial controller with a real-time processor, a user-programmable Field Programmable Gate Array (FPGA) and reconfigurable IO modules [34]. It is worth to point out that in the designed architecture, the three main processes, i.e., (i) PMU time synchronization, (ii) signal acquisition and (iii) synchrophasor estimation, run at the FPGA level. Indeed, FPGAs provide hardware-timed speed and reliability, that are two essential features for PMUs.

The sampling of the voltage and current waveforms is realized by means of two parallel 24-bits delta–sigma converters, module NI 9225 and 9227 respectively, characterized by a sampling rate $F_s$ of 50 kHz and an input range of 300 V$\text{RMS}$ for the voltage and 5 A$\text{RMS}$ for the current [35], [36].
A. The Synchrophasor Estimation Algorithm

The developed PMUs adopt the e-IpDFT algorithm to estimate the synchrophasors, i.e., the frequency \( f \), amplitude \( A \), phase angle \( \varphi_0 \) and the Rate-of-Change-of-Frequency (RO-COF) associated to the fundamental tone of the power system signal under analysis. This technique is specifically designed to mitigate the effects of long-range spectral leakage produced by the negative image of the fundamental component.

Algorithm 1 The e-IpDFT synchrophasor estimation.

1: \( x[n] := \{x(t_n) \mid t_n = n T_s, n = \{0, \ldots N - 1\} \in \mathbb{N}\} \)
2: \( X(k) = \text{DFT}[x[n] \cdot w[n]] \)
3: \( \{\hat{f}_0, \hat{A}_0, \hat{\varphi}_0\} = \text{IpDFT}(X(k)) \)
4: for \( p = 1 \to P \)
5: \( \hat{X}^{p-}(k) = w(k) \left( -\hat{f}^{p-1}, \hat{A}^{p-1}, -\hat{\varphi}^{p-1} \right) \)
6: \( \hat{X}^{p+}(k) = X(k) - \hat{X}^{p-}(k) \)
7: \( \{\hat{f}_p, \hat{A}_p, \hat{\varphi}_p\} = \text{IpDFT}(\hat{X}^{p+}(k)) \)
8: end for

As described in Algorithm 1, the PMU first acquires a discrete time-series of samples \( x[n] \), where \( x(t) \) is the time-variant signal under analysis. \( N \) is the number of samples that compose the considered observation interval \( T \) and \( F_s = T_s^{-1} \) is the sampling rate (line 1). The signal is windowed with the Hanning function \( w[n] \) to reduce spectral leakage effects, then the DFT of the weighted signal \( X(k) \) is computed (line 2).

A preliminary estimate of the fundamental parameters is obtained by processing the highest DFT bins via the IpDFT technique (line 3). Specifically, the fractional correction term \( \delta \), indicating the location of the actual signal frequency with respect to the location of the highest amplitude bin \( k_m \), is calculated as follows:

\[
\delta = \varepsilon \cdot \frac{2 \cdot |X(k_m + \varepsilon)| - |X(k_m)|}{|X(k_m + \varepsilon)| + |X(k_m)|} \quad (3)
\]

The latter is used to estimate the fundamental component parameters based on the following expressions:

\[
\hat{f} = (k_m + \delta) \Delta f \quad (4)
\]

\[
\hat{A} = |X(k_m)| \left( \frac{\pi \delta}{\sin(\pi \delta)} \right) |\delta^2 - 1| \quad (5)
\]

\[
\hat{\varphi}_0 = \angle X(k_m) - \pi \delta \quad (6)
\]

being \( \Delta f = 1/T \) the DFT frequency resolution. These values enable the reconstruction of the component’s negative image \( \hat{X}^-(k) \), whose analytic expression is known for the Hanning function (line 5). The negative image is subtracted from the original DFT bins, that now should account only for the fundamental component’s positive image \( \hat{X}^+(k) \) (line 6). Finally, the IpDFT is applied to such spectrum, resulting in an enhanced estimation of the fundamental tone parameters \( \{\hat{f}, \hat{A}, \hat{\varphi}_0\} \) (line 7). The e-IpDFT adopts a reporting rate \( F_r \) of 50 frames per second (fps) to report the synchrophasors.

It is worth observing that the compensation of the spectral interference produced by the negative image of the fundamental component can be repeated a predefined number of times \( P \). In the PMU described in [14], the procedure was repeated only once. More recent findings have demonstrated that setting \( P \) equal to 2 leads to a significant improvement of the e-IpDFT estimation accuracy [37]. Therefore, in the developed PMU, this compensation routine is performed twice.

It is also worth mentioning that the higher the observation interval over which synchrophasors are measured, the higher the accuracy of the estimates. The IEEE Std. C37.118.1 [1] introduces two PMU performance classes: P-class PMUs are meant for protection applications, and require responsiveness rather than accuracy, M-class PMUs are meant for measurement applications, and require an increased level of synchrophasor estimation accuracy. The PMU proposed in [14] adopts an observation interval \( T \) of 60 ms, and represents a P-class PMU. In the current implementation, the observation interval \( T \) can be increased to 100 ms, that is a value typical of M-class PMUs.

In this regard, Fig. 2 compares the phase estimation errors obtained with a P-class and an M-class algorithm, and with \( P \) equal to 1 and 2. The test is performed with simulated waveforms in steady-state test condition. Specifically, the amplitude and the initial phase are equal to 1 pu and 0 respectively, the frequency varies between 47.5 and 52.5 Hz, i.e., within the PMU pass-bandwidth considering the nominal frequency at 50 Hz and the reporting rate of 50 fps. In order to reproduce measurement noise coherent with the signals experimentally acquired in Section V, the waveforms are corrupted by an additive uncorrelated white Gaussian noise, whose variance is scaled to reproduce an overall signal-to-noise ratio (SNR) of 85 dB. In this context, it is interesting to observe that for P-class configuration the second iteration provides a significant performance enhancement in case of non-nominal frequency values, with a phase error not exceeding 5 \( \mu \)rad. For the M-class configuration, already with \( P \) equal to 1 the phase error does not exceed 4 \( \mu \)rad.

Considering the uncertainty balance in Eq. (1), we are able to quantify both \( \varepsilon_{\text{alg}} \) and \( \varepsilon_{\text{acq}} \) of our test-bed. The synchrophasor estimation uncertainty \( \varepsilon_{\text{alg}} \) is rather constant in the considered spectral bandwidth and lower than 5 \( \mu \)rad, whereas the measurement noise exceeds the quantization noise of the acquisition module and thus makes negligible its uncertainty contribution \( \varepsilon_{\text{acq}} \).

B. The Free-Running Sampling Process

Regardless of the adopted time dissemination technique, the sampling process of the waveforms is free-running and the
UTC-time synchronization is achieved a posteriori. Specifically, at the FPGA level, we derive form the UTC-PPS signal a sub PPS square waveform (hereafter called subPPS), locked to the UTC-PPS and characterized by a frequency corresponding to the PMU reporting rate $F_r$. The signal acquisition, the synchrophasor estimation, and the synchrophasor time-stamping are triggered by the rising edge of such subPPS. However, there is no guarantee that the sampling process is locked to such subPPS signal: there must be an a posteriori time refinement.

Specifically, two delays need to be compensated. The first one results from the fact that the sampling frequency might drift from its nominal value, due to oscillator degradation or environment conditions variation (such as temperature). We measure this frequency drift over observation windows of $M$ samples, with $M >> N$ (such as few seconds windows). If the sampling process was uniform, such window would account for an ideal amount of time $MT_s$. In real operating conditions, the actual difference between the time instant when the last sample is acquired $t_{M-1}$ and the time instant when the first sample is acquired $t_0$, might differ from the ideal delay. The clock drift is defined as the normalized difference between these two delays:

$$f_D = \frac{(t_{M-1} - t_0) - MT_s}{MT_s}$$

Every time the clock drift is updated, the DFT frequency resolution $\Delta f = 1/T$ can be adequately compensated as:

$$\Delta f_c = \Delta f (1 - f_D)$$

and therefore the frequency estimation improved $\hat{f}_c$.

The second delay is due to the possible offset between the two clocks. Indeed, in ideal operating conditions, i.e., if the sampling process was locked to the subPPS, the time delay between the rising edge of the subPPS $t_{subPPS}$ and the time instant when the first sample of the related window is acquired $t_0$ would be exactly zero. In real operating conditions, there could be a delay that would result in bad initial phase estimations. We measure this time delay at every subPPS and compensate for it by updating the estimated phase as follows:

$$\hat{\phi}_{0,c} = \hat{\phi}_0 + 2\pi \hat{f}_c(t_0 - t_{subPPS})$$

C. GPS Time Synchronization

The GPS-PMU is based on the cRIO-9068 controller, embedding a reconfigurable Xilinx Zynq 7020 FPGA with an on-board clock frequency of 40 MHz, 106400 flip-flops, 53200 look-up tables (LUTs), 4480 kbits of block RAM and 203800 look-up tables (LUTs), 16020 kbits of block RAM and 840 DSP slices [41]. The PTP-PMU is based on the cRIO-9039 controller, characterized by a reconfigurable Xilinx Kintex-7 FPGA with a 25 X 18 multiplier, 4480 kbits of block RAM and 220 DSP slices (each one characterized by a 25 X 18 multiplier, an adder and an accumulator) [38]. The UTC-GPS signal is acquired by means of the NI 9467 GPS time-stamping and synchronization module, that is directly coupled with the on-board FPGA clock [39]. This enables to timestamp each tick of the 40 MHz clock with real-world time, accurate to within ± 100 ns. That is to say that the NI GPS module provides a continuous time reference characterized by a time polling resolution corresponding to the FPGA clock. The subPPS is locked to the UTC-GPS.

The GPS module is coupled with a Trimble’s Bullet III GPS receiver, an active GPS antenna with a high-gain preamplifier (35 dB) and dual passband filters [40]. The preamplifier enables preserving the GPS signal even for long cable lengths, whereas the filters improve rejection to interfering radio signals and reliability. The antenna is mounted on the rooftop of DESL laboratory with a full-sky visibility and is coupled to the module via a 30-meters RG-213 shielded cable. The latter, introduces un unavoidable propagation delay of 5.05 ns/m, leading to 151.5 ns (suitably compensated).

D. PTP Time Synchronization

The PTP-PMU is based on the cRIO-9039 controller, characterized by a reconfigurable Xilinx Kintex-7 FPGA with an on-board clock frequency of 40 MHz, 407600 flip-flops, 203800 look-up tables (LUTs), 16020 kbits of block RAM and 840 DSP slices [41]. The PTP distribution is achieved thanks to the NI TimeSync library, that synchronizes the timekeeping clocks of the cRIO. The so-called hardware time-stamping enables to discipline the FPGA clock directly via the UTC-PTP reference. This enables to timestamp each tick of the 40 MHz clock with real-world time, accurate to within ± 1 μs. The TimeSync library provides a continuous time reference, however, since the FPGA clock is locked to the UTC-PTP, the resolution of time stamps corresponds to 25 ns.

The UTC-PTP reference signal is acquired by connecting point-to-point the three-speed RJ-45 Gigabit Ethernet Port to a PTP master clock. The latter is the Network Time Server NTS 100 manufactured by Tekron [42]. The clock receives the absolute time by a Trimble’s Bullet III GPS receiver, whose characteristics have been already discussed in Section IV-C.

E. White Rabbit Time Synchronization

The WR-PMU setup is shown in Fig. 3, and is based on the same hardware platform as the GPS-PMU, i.e., cRIO-9068. The WR-UTC signal is provided by the NI WR cRIO module, a standalone WR node which can be coupled with the NI cRIO platforms to integrate the WR protocol [43]. The module is equipped with a Xilinx Spartan-6 FPGA and can be used in

\[\text{Fig. 3. The experimental WR network composed of a Meinberg GPS180PEX card, a WR switch and a NI-cRIO integrating the WR-cRIO module (i.e., a WR-PMU).}\]
all operation modes defined by the WR protocol, i.e., grand-master, master or slave. Depending on the selected operation mode, a different configuration of input and outputs shall be adopted. A user programmable HDSub-15 I/O module is provided, that can acquire the 10 MHz and PPS inputs (in case of operating the node in grand-master mode) or any sort of external trigger, as well as generate reference clock, PPS outputs or generic triggers. The module is also equipped with a Small Form-factor Pluggable (SFP) cage, for disseminating WR messages over optic fiber transceivers. In particular, when operated in slave mode, such cage is used to connect the module to its master WR switch and to retrieve the time information.

In the developed PMU, the module is operated in slave mode, and is connected point-to-point to a WR switch operated in grand-master mode. The switch is manufactured by Seven Solutions [44]. Ethernet frames are exchanged through 18 ports equipped with SFP sockets, connected directly to a Xilinx Virtex-6 FPGA characterized by very low latency. An ARM CPU running Linux helps with less time-sensitive processes like remote management and keeping the frame filtering database in the FPGA up to date. The clocking resources block contains PLLs for cleaning up and phase-compensating the system clock, as well as for generating the frequency-offset clock. It provides deterministic delivery and a reliable communication using redundant network topology. It allows many hops (14 tested keeping subnanosecond accuracy).

The NTP service, used to determine the absolute time and date at reboot, is provided by a Windows machine connected point-to-point to the RJ-45 management port of the WR switch via an Ethernet cable. The computer is equipped with a Mem- berg 180 PEX card that disciplines the system time as well as the NTP service [45]. The card is coupled with an active GPS receiver, mounted on the rooftop of DESL laboratory, via a 30-meters RG-213 shielded cable. The card compensates for the delay introduced by the cable (as already discussed in Section IV-C). The card further generates reference PPS and 10 MHz signals, that are fed to the WR switch.

Due to hardware limitations, the UTC-WR polling is limited by the module’s FPGA clock running at 50 kHz, therefore, the WR cRIO does not provide a continuous time reference. Also, the UTC-WR reading introduces a deterministic delay, that needs to be compensated. The next paragraph describes the implementation details that enable us to overcome these two limitations.

1) On the Retrieving of the WR Time: To retrieve the UTC-WR from the WR cRIO, we generate a trigger characterized by a frequency of 50 kHz, i.e., the maximum value attainable in the WR cRIO FPGA. The procedure illustrated in Algorithm 2 is implemented to trigger the UTC-WR acquisition, to freeze the time, and to acquire it. Specifically, when the state is Wait for Node Start, the trigger is generated and the WR cRIO acquires the reference time. The UTC-WR is frozen and acquired in the next states. Then the node is set in Idle mode until the next trigger. The time acquisition process is not continuous but the UTC-WR is updated in a discrete manner, determined by the trigger period $T_{\text{trig}}$ of 20 µs. This lower bound is limited by the FPGA integrated in the NI cRIO, characterized by a finite and deterministic time polling resolution, not appropriate for PMU applications.

To overcome this hardware limitation, an additional internal free-running clock is implemented. Such clock is disciplined by the FPGA clock and is implemented at every tick, i.e., every 25 ns. As long as the UTC-WR is not updated, the free-running clock governs the PMU time. Every time the UTC-WR is acquired, the free-running clock is overwritten by the updated reference time.

As it is known, the FPGA clock could drift even in the short interval between two consecutive triggers, biasing the attainable sub-nanosecond accuracy. Therefore, every time the UTC-WR is acquired, the deviation between the free-running clock and the UTC-WR is computed, and this error is used by a PI controller to condition the free-running clock.

The structure of the free-running clock and its PI controller is shown in Fig. 4: the PMU time is made of the second and nanosecond counters and the correction $\gamma(n)$ is added to a femtosecond counter at each tick. The PMU time is therefore corrected only when this counter has an overflow or an underflow. The tuning of the PI controller has been done empirically: the proportional coefficient $K_p$ has been chosen to average the error entering the PI controller over a period of 10 ms, which gives a very low jitter. The integrator is built as a counter that is incremented or decremented according to the sign of the error. Its resolution has been set to 1 fs (i.e. the highest possible), which allows to compensate the steady-state error without introducing additional jitter. The implemented internal clock is explained in Algorithm 3.

It is worth noting that, due to hardware limitations, there is a delay in acquiring the UTC-WR. However, the use of the FPGA makes this delay time-deterministic (in the order of few

### Algorithm 2 Retrieving the WR time.

```
1: while True
2:    Go to normal operation
3:  Start
4:  while $T_{\text{trig}}$
5:    Wait for node start
6:  end
7: Read UTC-WR
8: Idle
9: end
```
In addition to greater resolution, the internal free-running clock also has much less jitter than the WR time, as shown in Table I. The calculation of jitter is done by computing the standard deviation (i.e., WR time together with the internal free-running clock) between two successive triggers $T_{\text{trig}}$. The standard deviation is then computed with 1000 samples. The performance of this implementation, characterized by the jitter, is appropriate for a PMU application.

Algorithm 3 Internal free-running clock.

1: if $T_{WR}(n) \neq T_{WR}(n-1)$
2: \[
\varepsilon(n) = T_{WR}(n) - T_{PMU}(n)
\]
3: \[
\gamma(n) = K_p \varepsilon(n) + \sum_0^n \text{sign}(\varepsilon(k))
\]
4: \end
5: $T_{PMU}(n) = T_{PMU}(n) + \Delta T + \gamma(n)$

This algorithm is used to calculate the time steps of the WR time $T_{WR}$ and the PMU clock $T_{PMU}$ (i.e., WR time together with the internal free-running clock) between two successive triggers $T_{\text{trig}}$. The standard deviation is then computed with 1000 samples. The performance of this implementation, characterized by the jitter, is appropriate for a PMU application.

V. PERFORMANCE ASSESSMENT

The performance of the described PMUs is assessed using the test-bed illustrated in Fig. 6, i.e., by means of the dedicated PMU calibrator described in [12], that enables us to validate the conformity of the PMU under test with respect to the IEEE Std. C37.118 [1]. The calibrator, generates reference signals whose true parameters are known with a TVE in the order of $10^{-4} q_e$, obtained in case of static signals. The true parameters are determined by the well-known Levenberg-Marquardt algorithm, based on a nonlinear least-squares method. Such procedure, described in [46], has been proven to provide a unique and robust solution within the whole range of static tests required by [1].

The forward path of the calibrator generates a set of static reference waveforms characterized by a sampling rate of 500 kHz, peak amplitude of 10 V, 0 rad phase and frequency varying in the range $[47.5, 52.5]$ Hz (i.e., the PMU passband considering a nominal frequency at 50 Hz and the reporting rate of 50 fps). These signals are amplified by a CMS-356 OMICRON precision voltage and current amplifier, characterized by an amplification gain of 30, and simultaneously acquired by the three PMUs under test [47]. The final waveforms are characterized by a signal-to-noise-ratio (SNR) of 85 dB. It is worth pointing out that, as highlighted in Fig. 6, the master clocks of the three PMUs and the one of the PMU calibrator use separate GPS receivers, thus guaranteeing the non correlation among the various absolute times.

As known, the uncertainty requirements are expressed in terms of TVE, Frequency Error (FE), and ROCOF Error (RFE). However, the analysis of amplitude and phase error separately provides a deeper understanding about eventual error sources. More specifically, every inaccuracy related to a poor time-synchronization of the PMU under test, expresses itself in a phase error. Also, since the synchrophasor estimation algorithm and the hardware platform are identical for the three PMUs, the time synchronization protocol mainly affects the phase estimation.

For each PMU configuration and for each nominal frequency we evaluate the phase estimation accuracy over a test duration of 24 hours. We present the results by means of two performance indicators. First, we evaluate the cumulative distribution function (CDF) of the unbiased normalized phase errors. Second, we quantify the stability of the adopted time dissemination technology computing the Allan deviation [48].

![Fig. 5](image1.png)

Fig. 5. The structure of the internal conditioned clock together with the $T_{WR}$.

![Fig. 6](image2.png)

Fig. 6. Measurement setup for the performance assessment. The PMU calibrator generates user-defined test waveforms, that are amplified up to 300 V by the CMS 356 OMICRON amplifier, and then supplied to the three considered PMUs, relying on GPS, PTP and WR time dissemination.

| TABLE I |
|-----------------|-----------------|
|                 | $T_{WR}$ | $T_{PMU}$ |
| Jitter [ns]     | 2.89     | 0.42     |

<table>
<thead>
<tr>
<th>WR cRIO</th>
<th>GPS180PEX</th>
</tr>
</thead>
<tbody>
<tr>
<td>GPS169PCI</td>
<td>Meinberg</td>
</tr>
<tr>
<td>PXI 6682</td>
<td>GPS PMU</td>
</tr>
<tr>
<td>NTS100</td>
<td>PTP PMU</td>
</tr>
<tr>
<td>WR Switch</td>
<td>WR PMU</td>
</tr>
<tr>
<td>CMS356 OMICRON</td>
<td>WR PMU</td>
</tr>
<tr>
<td>Tekron</td>
<td>WR Switch</td>
</tr>
<tr>
<td>10 MHz</td>
<td>10 MHz</td>
</tr>
<tr>
<td>10 VRMS</td>
<td>300 VRMS</td>
</tr>
<tr>
<td>10 MHz</td>
<td>10 MHz</td>
</tr>
<tr>
<td>GPS PMU</td>
<td>GPS169PCI</td>
</tr>
<tr>
<td>WR PMU</td>
<td>WR cRIO</td>
</tr>
<tr>
<td>GPS180PEX</td>
<td>PXI 6682</td>
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<td>NTS100</td>
</tr>
<tr>
<td>WR PMU</td>
<td>WR Switch</td>
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<td>WR PMU</td>
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</table>
Fig. 7. P-class: phase error cumulative distribution functions as provided by GPS (blue), PTP (red) and WR (green) PMUs over a 24-hour test. The test waveform consists of a single fundamental tone whose amplitude, frequency and phase are set equal to 300 V, 50 Hz, and 0 rad, respectively.

Fig. 8. P-class: phase error cumulative distribution functions as provided by GPS (blue), PTP (red) and WR (green) PMUs over a 24-hour test. The test waveform consists of a single fundamental tone whose amplitude, frequency and phase are set equal to 300 V, 47.5 Hz, and 0 rad, respectively.

Fig. 9. P-class: phase error cumulative distribution functions as provided by GPS (blue), PTP (red) and WR (green) PMUs over a 24-hour test. The test waveform consists of a single fundamental tone whose amplitude, frequency and phase are set equal to 300 V, 52.5 Hz, and 0 rad, respectively.

Fig. 10. P-class: phase error Allan deviation as function of the time interval $\tau$, for GPS (blue), PTP (red) and WR (green) PMUs over a 24-hour test. The test waveform consists of a single fundamental tone whose amplitude, frequency and phase are set equal to 300 V, 50 Hz, and 0 rad, respectively.

Fig. 11. P-class: phase error Allan deviation as function of the time interval $\tau$, for GPS (blue), PTP (red) and WR (green) PMUs over a 24-hour test. The test waveform consists of a single fundamental tone whose amplitude, frequency and phase are set equal to 300 V, 47.5 Hz, and 0 rad, respectively.

Fig. 12. P-class: phase error Allan deviation as function of the time interval $\tau$, for GPS (blue), PTP (red) and WR (green) PMUs over a 24-hour test. The test waveform consists of a single fundamental tone whose amplitude, frequency and phase are set equal to 300 V, 52.5 Hz, and 0 rad, respectively.
To this end, we consider the M-sample variance, defined as:

$$\sigma^2(\tau) = \frac{1}{M-1} \left[ \sum_{m=0}^{M-1} \delta_{\varphi}^2(m, \tau) - \frac{1}{M} \left( \sum_{m=0}^{M-1} \delta_{\varphi}(m, \tau) \right)^2 \right]$$

$$\delta_{\varphi}(m, \tau) = \frac{\varphi(mT_r + \tau) - \varphi(mT_r)}{\tau}$$

(10)

where $\varphi(mT_r)$ is the phase estimate associated to $mT_r$ time instant, expressed as function of the reporting period $T_r$, $M$ is the sample number for the variance computation, and $\tau$ is the time deviation between two consecutive phase estimates. The Allan variance refers to the specific case where $M$ and $T_r$ are set equal to 2 and $\tau$, respectively, and the Allan deviation is its square root [48]. We evaluate the phase estimation accuracy over different time intervals, varying $\tau$ between $10^1$ to $10^4$ s.

Our analysis has been conducted by coupling for several days the three devices with the PMU calibrator and in the following paragraphs, we present the results obtained for three different scenarios. The first two paragraphs are meant to evaluate the performance during normal operating conditions and refer to P- and M-class PMUs, respectively. The third paragraph instead refers to P-class PMUs during the worst-case condition that has been recorded over various tests and is meant to assess the maximum phase uncertainty that can be introduced by GPS, PTP and WR synchronization schemes.

A. Normal Operating Conditions, P-class

In the first test, we compare the phase estimation accuracy of P-class PMUs obtained in normal operating conditions as function of the fundamental frequency. Specifically, Fig. 7, 8 and 9 present the phase error CDFs for 50, 47.5 and 52.5 Hz, respectively. Independently from the fundamental frequency values, the WR enables us to keep the normalized phase error within $\pm 15$ $\mu$rad, whereas PTP and GPS might exceed 30 $\mu$rad. It is also worth observing that the GPS tends to out-perform the PTP and this performance discrepancy becomes more evident, as we consider non-nominal test conditions, when the sampling rate is not locked to the fundamental frequency.

In the same test conditions, Fig. 10, 11 and 12 evaluate the Allan deviation as function of the time interval $\tau$. Coherently with the previous results, we notice how the WR is characterized by the lowest variability, whereas PTP and GPS provide comparable performance. For instance, at 50 Hz the WR Allan deviation decreases from 0.5 $\mu$rad up to 0.7 nrad, if we enlarge the time interval from $10^3$ up to $10^4$ s. This performance enhancement provided by the WR time dissemination becomes more significant as $\tau$ increases, particularly when asynchronous sampling conditions are considered.

B. Normal Operating Conditions, M-class

Given a fundamental frequency of 50 Hz, Fig. 13 and 14 show the CDF and the Allan deviation for the M-class configuration, respectively. The choice of limiting the analysis to a synchronous sampling condition enables us to limit the uncertainty coming from the synchrophasor extraction process and focus primarily on the stability of the time synchronization source.

As expected, the M-class configuration provides better performance than the P-class one, leading to errors roughly 1 $\mu$rad lower for every considered timing technology. As shown in Fig. 13 the distribution of the errors is in this case sharper and less disperse than the results presented in the previous Section V-A. As regards the Allan deviation, the WR still provides enhanced stability, over any of the considered time intervals.

C. Worst-Case Operating Conditions, P-class

In the third scenario, we extract the worst-case performance associated to each time dissemination and compare them in order to experimentally determine the accuracy limit provided by GPS, PTP and WR-PMUs. As in Section V-B, we limit our analysis to coherent sampling, i.e., we keep the fundamental frequency to the nominal value of 50 Hz.

As shown in Fig. 15, the three PMUs are characterized by different trends of the distribution of the absolute phase error. As expected, the PTP-PMU is characterized by the most
disperse distribution, with a standard deviation of 26 $\mu$rad. The GPS and PTP-PMUs are characterized by non-symmetric tails and a non-null mean value, because the time evolution of the phase errors is characterized by a non-symmetric trend with respect to the respective mean value. The WR-PMU instead always reports a symmetric behavior, thus leading to a balanced CDF. Finally, the WR-PMU exhibits the sharpest CDF trend with a standard deviation of 8 $\mu$rad, demonstrating once again that such synchronization technique is the most deterministic one.

In general, the results in Fig. 15 reflect the accuracy specification of the adopted time synchronization techniques, in the sense that the lower the accuracy of the timing module, the more disperse the phase error distribution. As discussed in Section IV-A, the error introduced by the algorithm is dominating and masking the potential improvement of the phase estimate given by the WR technology. Nevertheless, an improvement of 10 $\mu$rad is achieved for the WR-PMU with respect to the GPS counterpart.

Similar considerations are valid also for the Allan deviations presented in Fig. 16: independently from the considered time interval $\tau$, the WR confirms to be characterized by a lower phase variability (equal to 1 nrad at $10^4$ s), whereas PTP and GPS provide nearly coincident performance.

Finally, in Table II, we report the main features of the phase error statistical distributions obtained in the different operating conditions and PMU configurations. For each time dissemination technique and fundamental frequency value, we compute the minimum and maximum phase error, as well as its standard deviation. In all the considered configurations, the WR outperforms PTP and GPS, with a worst-case standard deviation of 8.1 $\mu$rad. In this regard, it is worth noticing how the WR synchronization produces a phase variability that is comparable with the synchrophasor accuracy limit (i.e., 5 $\mu$rad for P-class and 4 $\mu$rad for M-class). In other words, the WR-PMU is capable of minimizing the time dissemination uncertainty contribution and thus optimizing the performance of the actual synchrophasor estimation algorithm. It is also interesting to observe that GPS is typically characterized by a lower standard deviation, but a larger min-max range than PTP. This phenomenon is due to the fact that even if GPS estimates are characterized by a reduced variability, they might present sudden variations or outliers that affect the definition of maximum and minimum error.

### VI. Conclusion

The paper presented the use of the WR time synchronization protocol for synchrophasor networks. The WR is characterized by a time accuracy of 1 ns, that is superior to those of state-of-the-art time dissemination technologies used for PMU applications, i.e., 50 ns for GPS and 1 $\mu$s for PTP.

The IEEE Std. C37.118.1 requires a maximum synchronization uncertainty of 1 $\mu$s for PMUs operating in transmission networks, but this value is lowered to 10 ns for distribution PMUs. Therefore, the WR is a suitable time distribution technique for PMUs operating at any power system level.

The paper has presented the integration of the WR protocol in a specifically developed WR-PMU, and has assessed its performance with respect to a GPS-PMU and a PTP-PMU. The three PMUs are characterized by the same synchrophasor estimation algorithm and by the same hardware platform,
with the exception of the time synchronization technique. The results demonstrate the advantage of using the WR instead of GPS, as it is characterized by a more deterministic phase error, experimentally quantified in 8 μrad.

REFERENCES

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